

JHU EE787 Fall 2001 MMIC Results

Craig Moore and John Penn

Designs Fabricated by TriQuint Semiconductor

Design Library by Gary Wray—Agilent

ADS software used for student designs

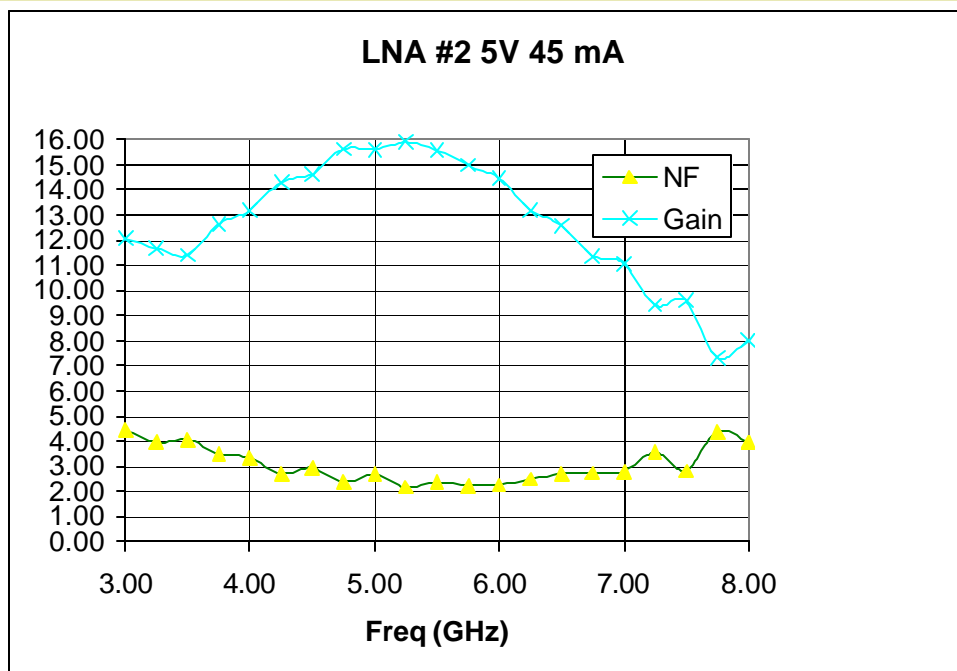
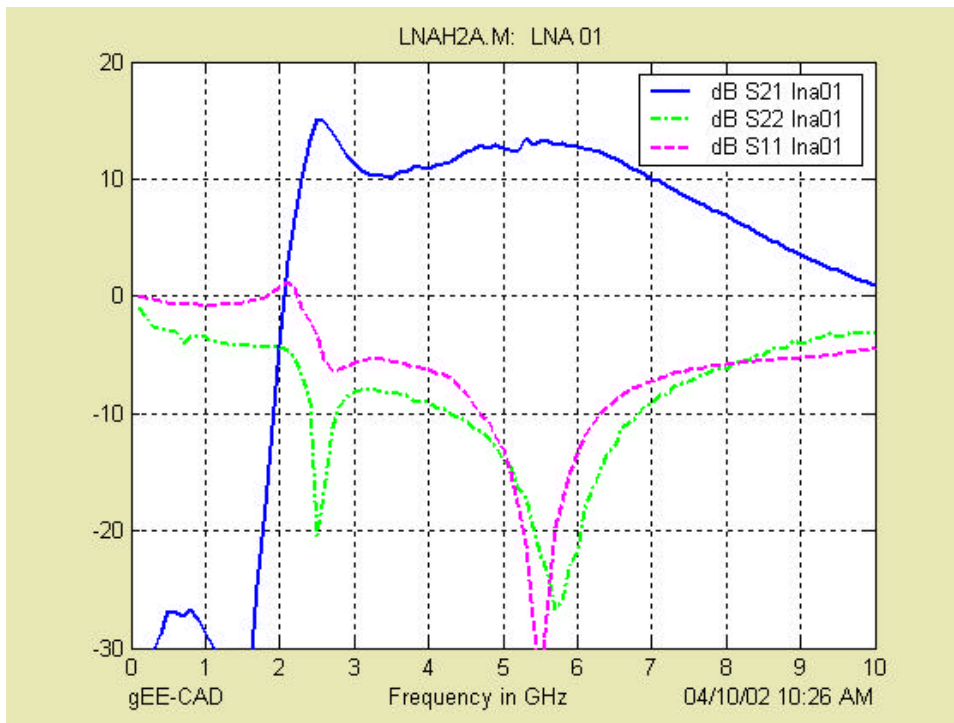
Six MMICs were designed by students for the Fall 2001 JHU MMIC Design Course as part of a C-Band transceiver. The designs were intended to work in a system that could be used at the WLAN band (5.15 to 5.35 GHz) or ISM band (5.725 to 5.875 GHz). All designs were tested in the Spring of 2002 after fabrication by TriQuint Semiconductor. Measurements compare favorably to simulations and all designs were successful. Attached are plots of the results—small signal s-parameters and appropriate performance tests. Some additional test structures and devices were fabricated along with the student designs and are summarized in this report.

Thanks again to TriQuint and Agilent for their wonderful support of the JHU EE787 MMIC Design Course.

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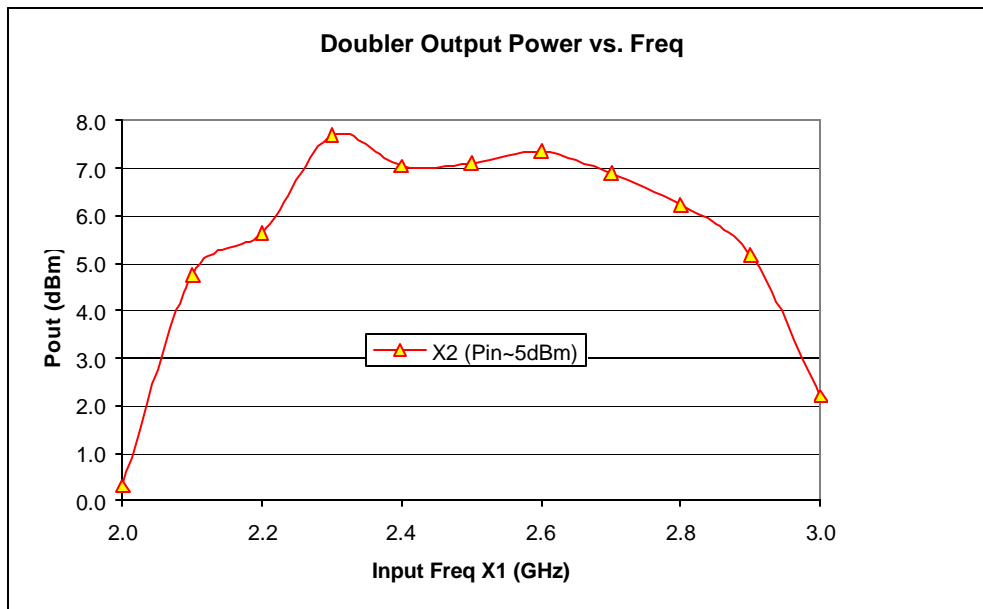
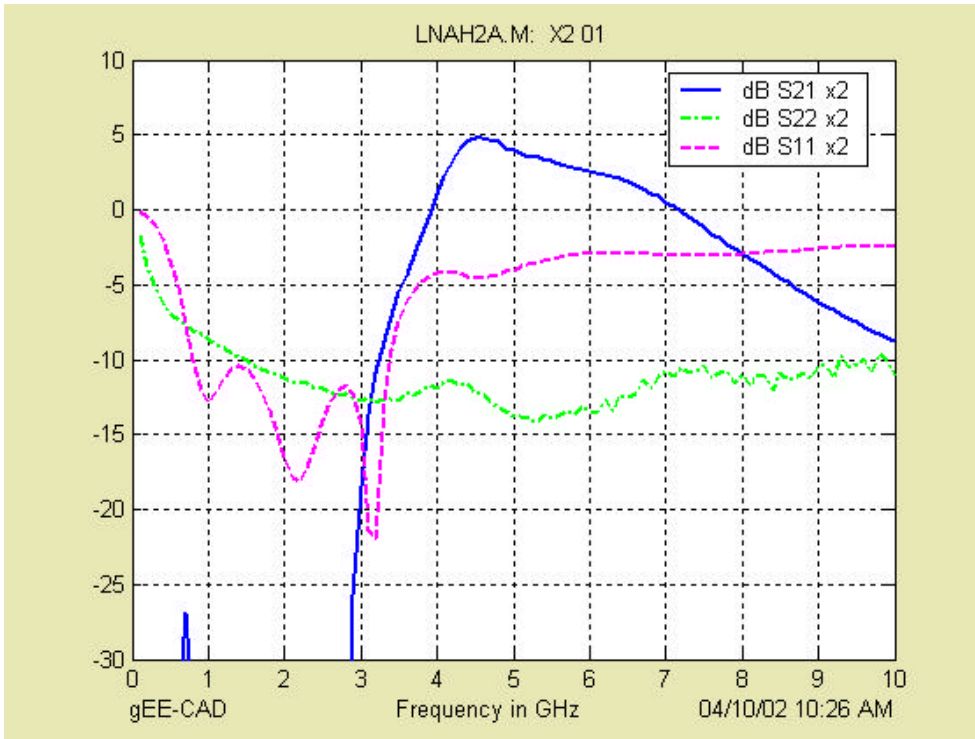
LNA—Low Noise Amplifier by Joe Acoraci and Liewei He.

Shown below is a plot of the LNA s-parameters at nominal bias of 5V and 44-45 mA of current. Bias was close to nominal but gain was a little bit lower than expected. Match looks good through the 5.1 to 5.9 GHz design band. Noise figure data was also taken and plotted following. Design was close to expected results.

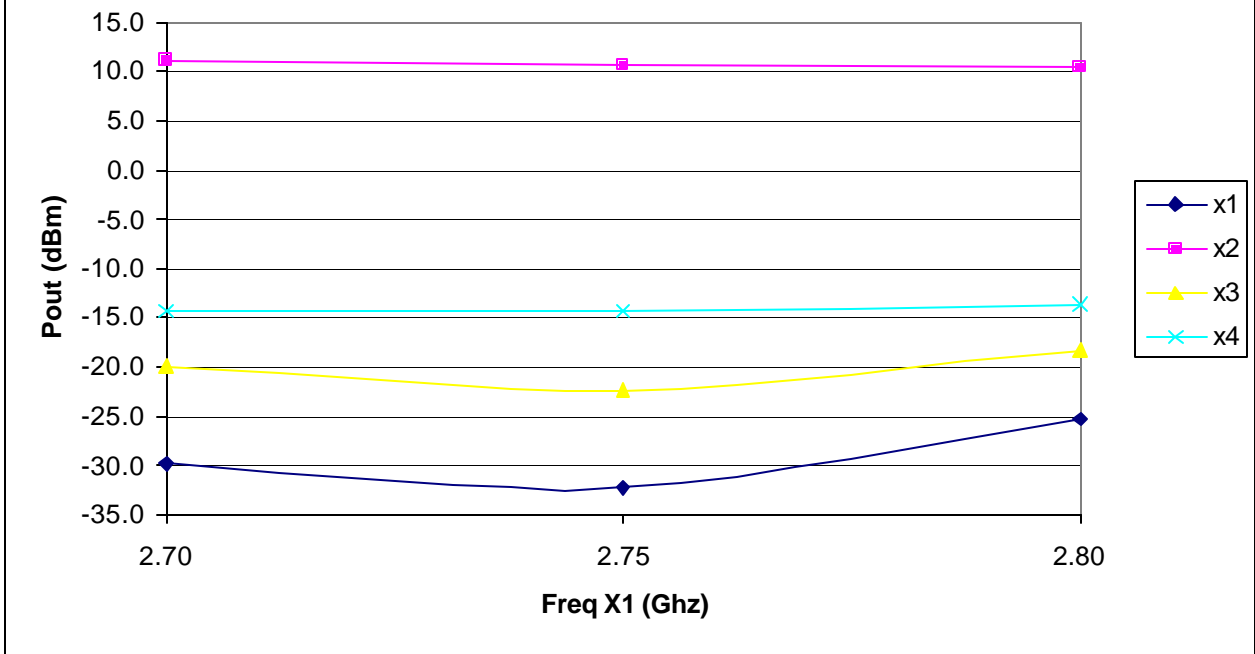


Doubler—Frequency Doubler by Lonnie Glerum and Brent Holm.

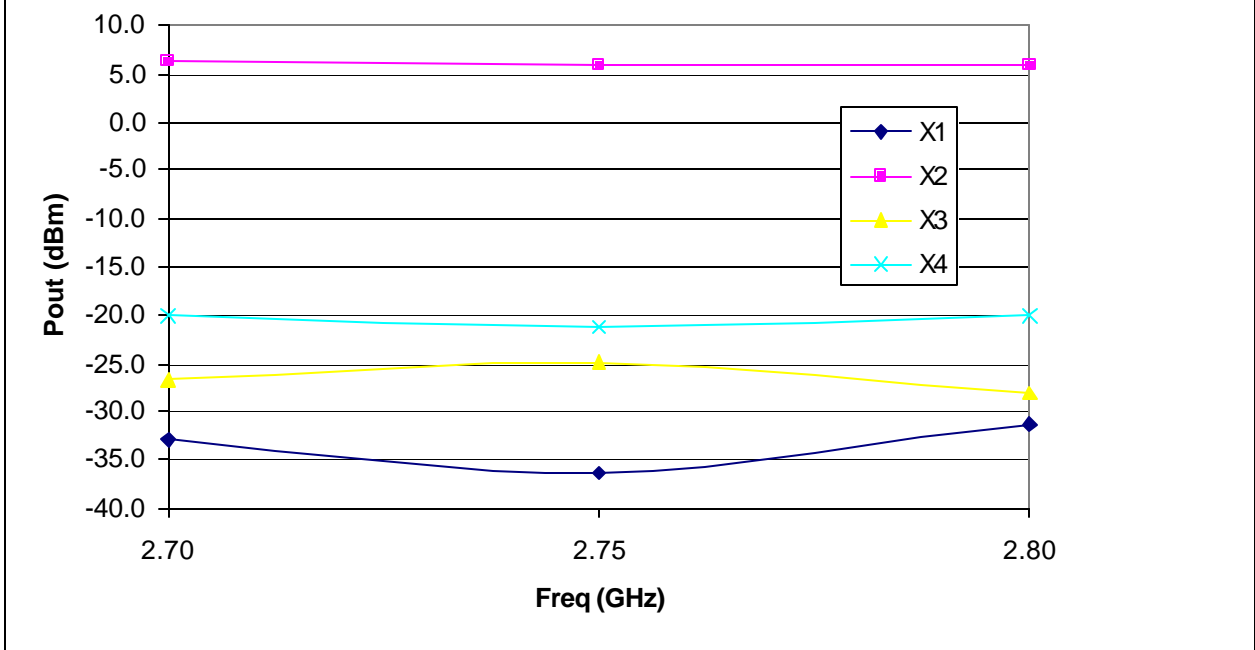
A frequency doubler was designed to have a 2.7 to 2.8 GHz input from the VCO design and double it with sufficient output power to drive the mixer. Below is the s-parameters showing good input match greater than 1-3 GHz with reasonable output match over the doubled output range. Performance plots of the doubler are also included. Bias was 5V at 51-52 mA—close to expectations. Doubler range is about 2.1 GHz to 2.9 GHz with conversion gain > 0 dB. Harmonics are shown for 5 and 10 dBm of input drive over the operating design band of 2.7 to 2.8 GHz.



Harmonic Pout X2 (10 dBm In)



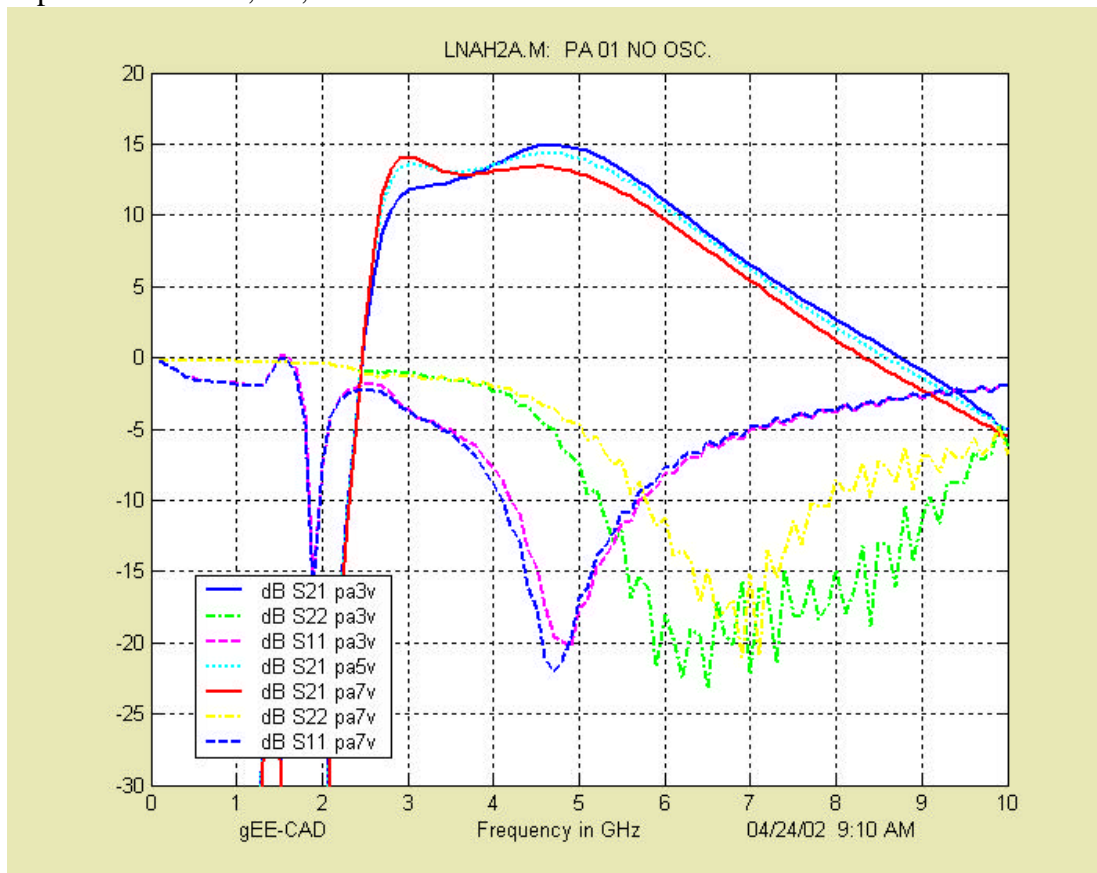
Harmonic Pout X2 (5dBm In)



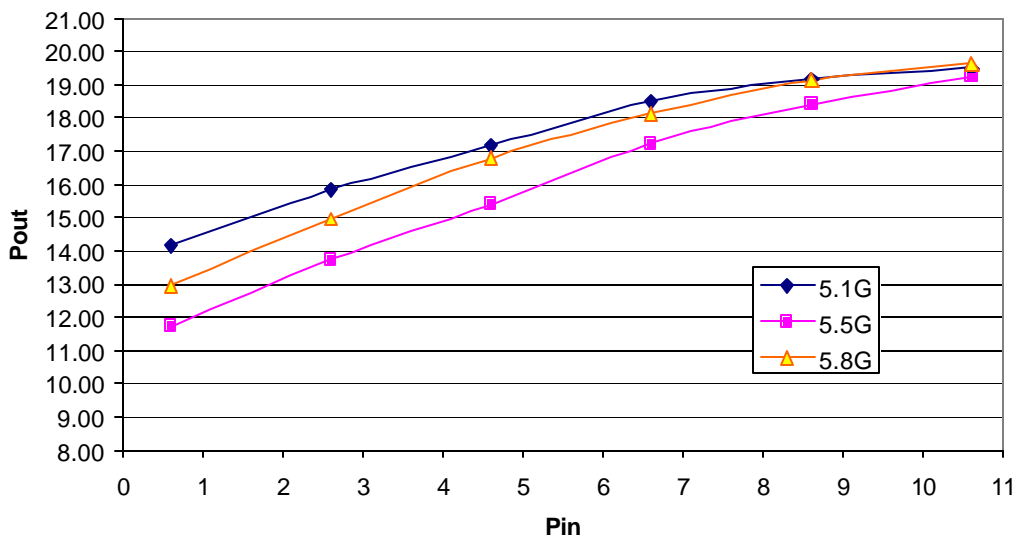
Power Amplifier—By Gary Hoffman.

The power amplifier was intended to be an efficient design with output greater than 24 dBm (250 mW) and 12 dB of gain. A two stage amplifier was designed with the second stage intended to operate in a class F mode. Initially the design had low frequency oscillations around 10 to 50 MHz when probe tested. Several die were silver epoxied to a piece of moly with additional 100 pF single layer capacitors at each of the two gate and two drain bias pads. This allowed stable measurement—with some additional 0.047 uF caps on the DC probes. Shown are the final s-parameters as well as some power measurements at 3, 5, and 7V on the drain. The design was intended for 7V operation but there was insufficient drive level from the test equipment to get full power output and efficiency at 7V. Power added efficiencies in the measured data range from the high 20s to low 30s in percentile. Gain appears slightly lower than expected especially in the performance measurements. Bias was about as expected with around 62 mA bias on the first stage FET and 42 mA on the larger class F second state FET. DC power consumption increases with drive level as shown. Due to limited input drive, the highest measured output powers were 140 mW (21.5 dBm) with 5V operation and 32% PAE (5.8 GHz) and 145 mW (21.6 dBm) with 7V operation and 33% PAE (5.8 GHz). At the 7V level, the power out has not compressed and could possibly increase another 2 dB if sufficient input power was available--based on the approximate 2 dB output power increase from 3 to 5V.

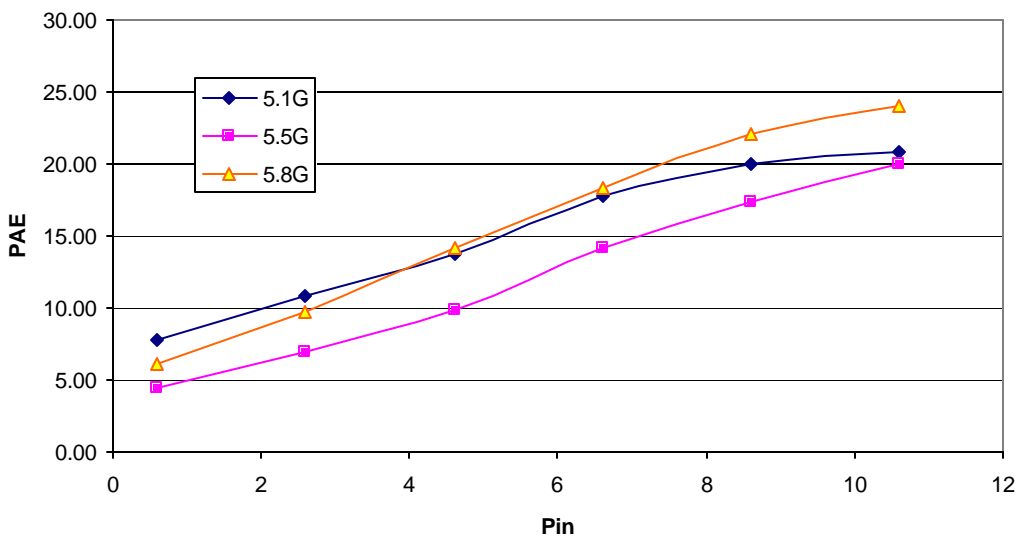
S-parameters at 3V, 5V, and 7V bias.



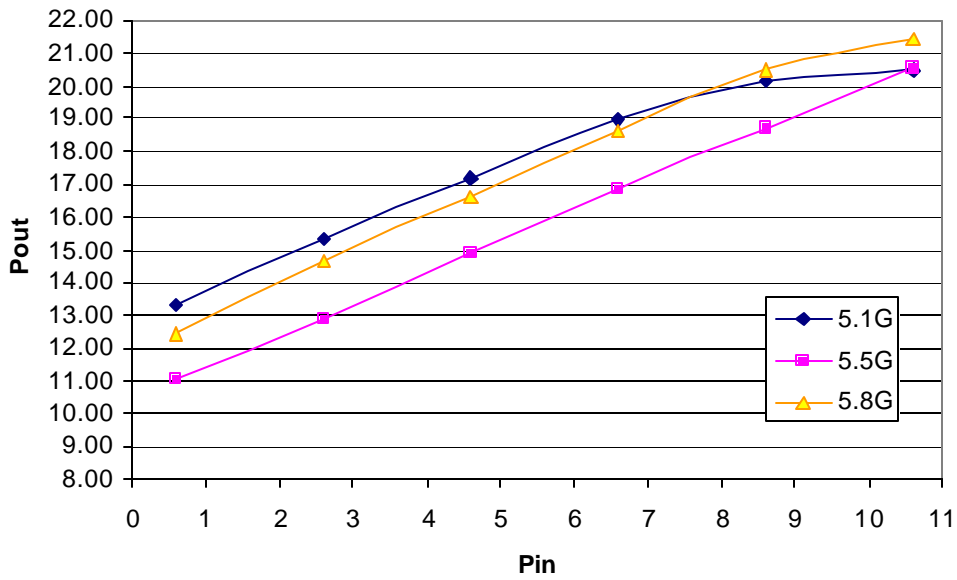
Pout Vs. Pin 3V



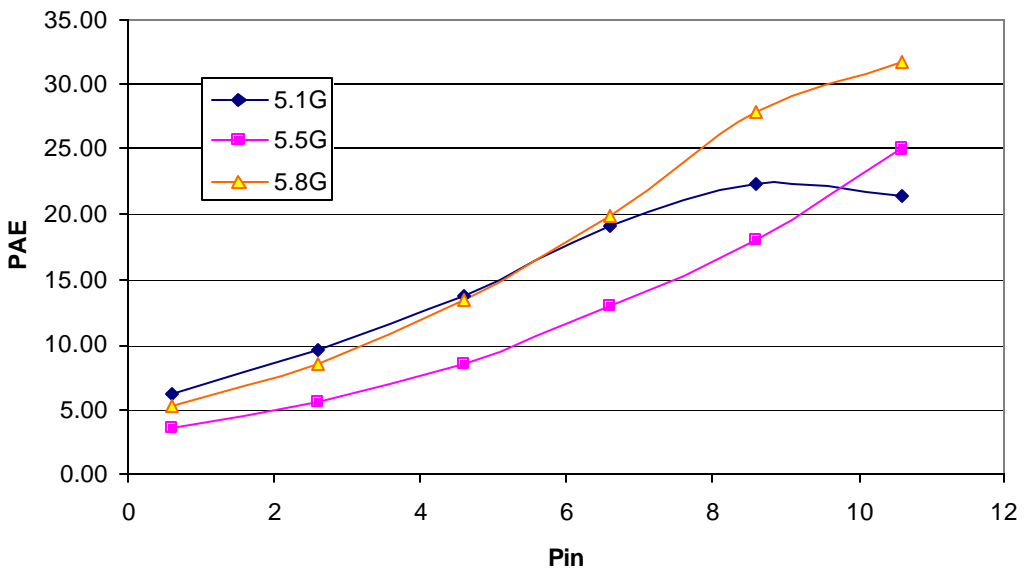
PAE vs. Pin 3V

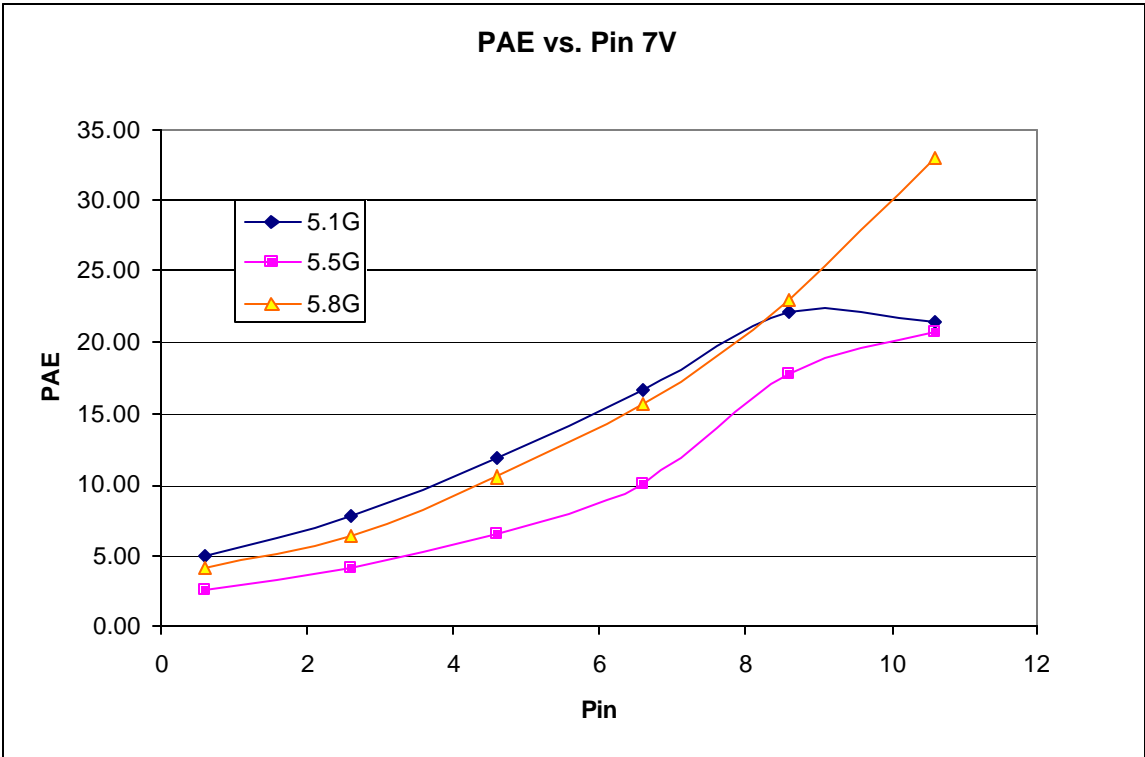
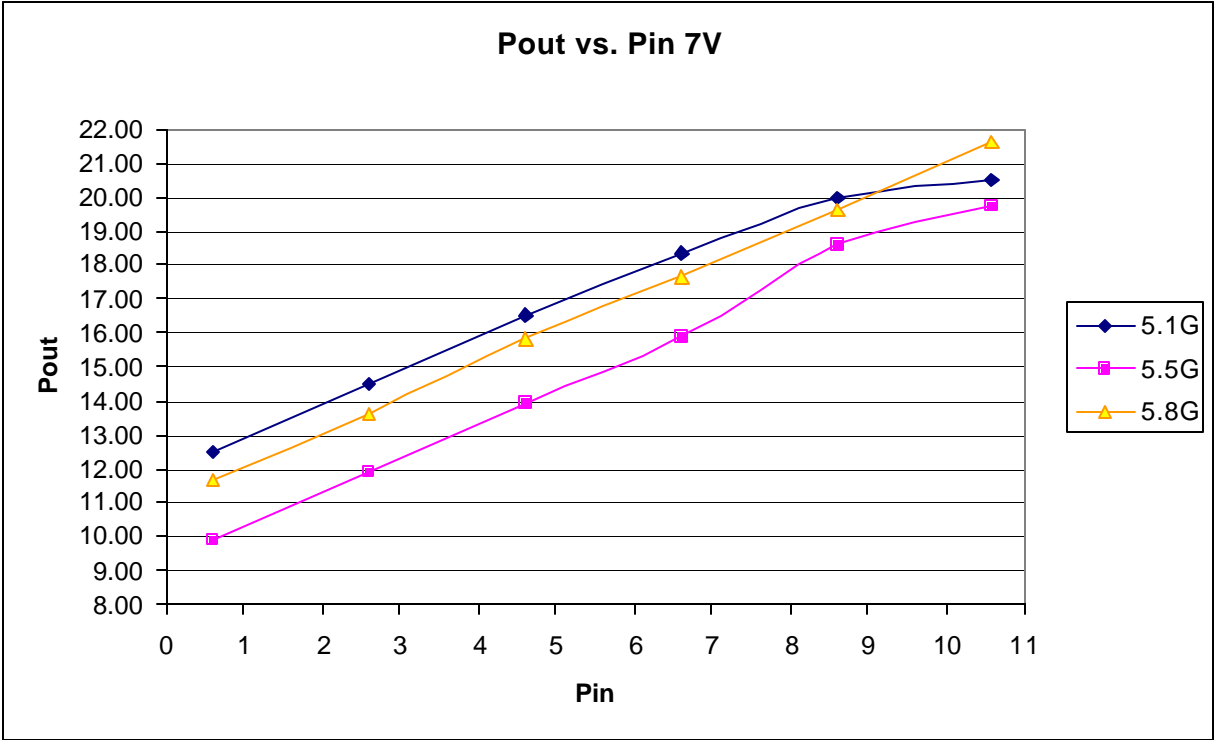


Pout Vs. Pin 5V



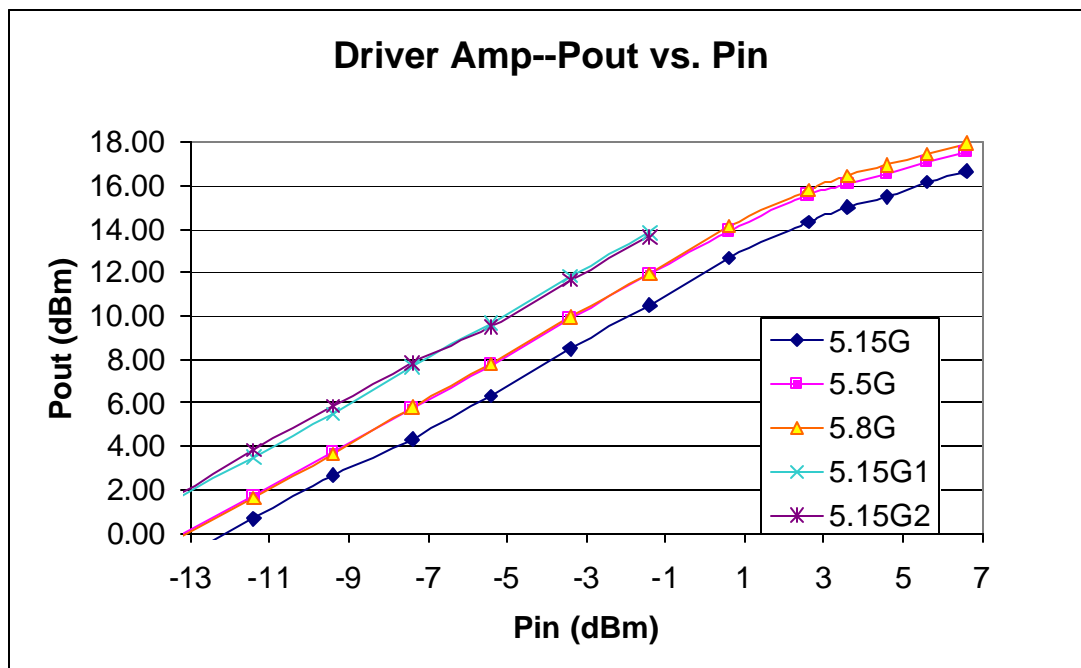
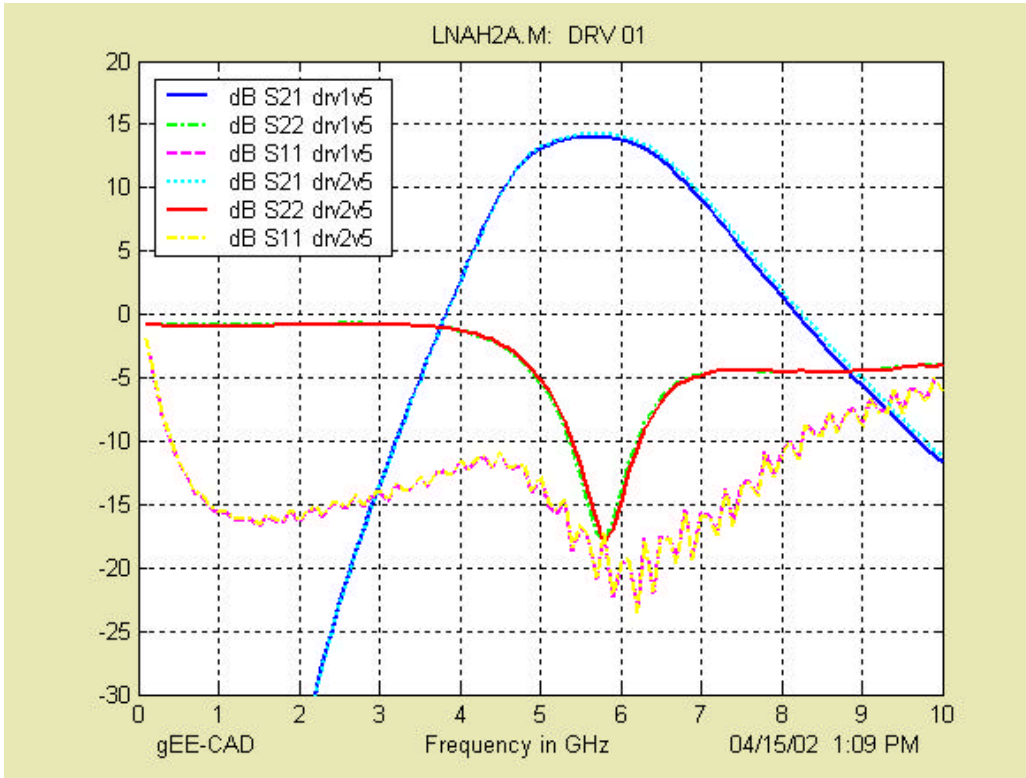
PAE vs. Pin 5V





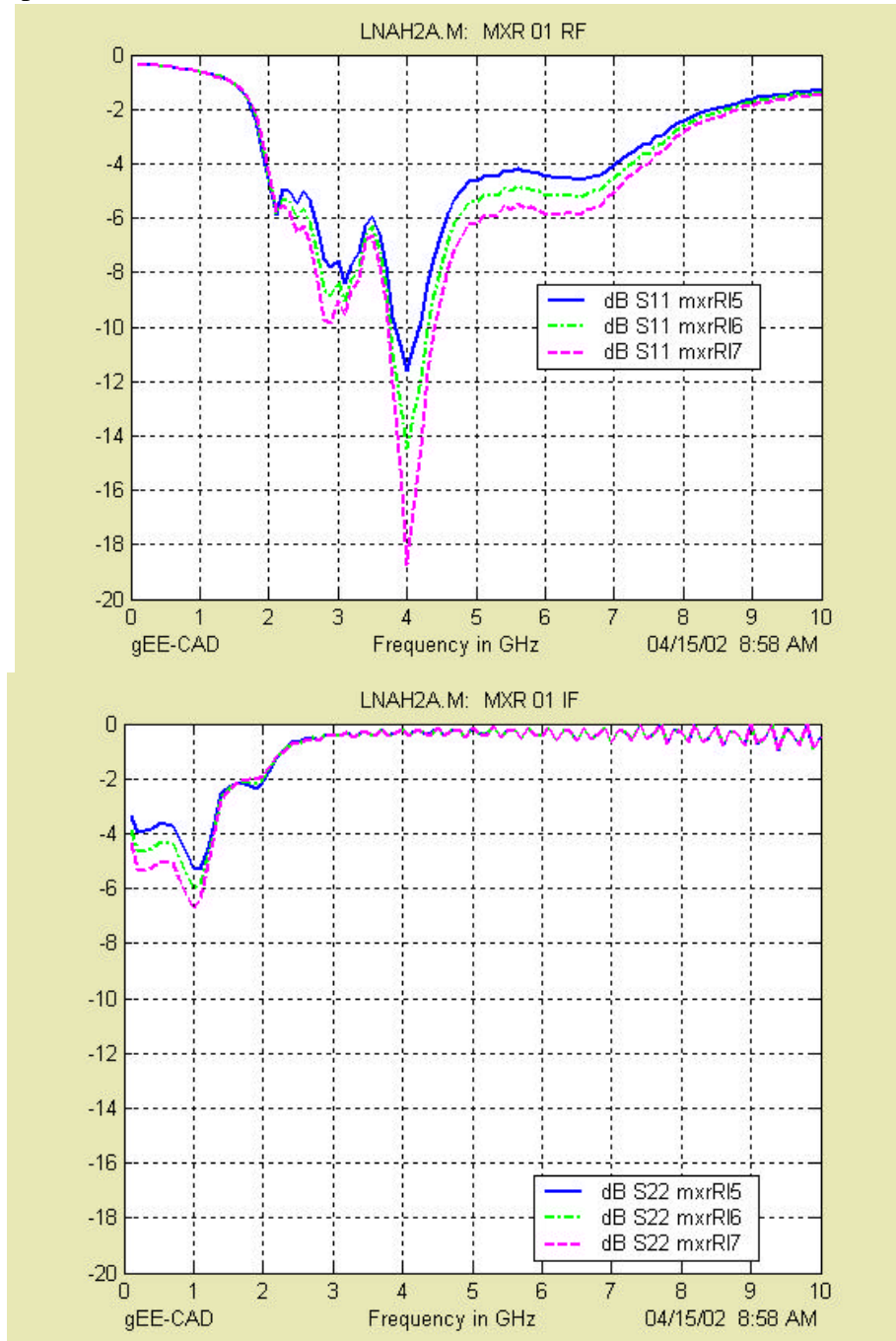
Driver Amplifier—By Ricardo Kanney

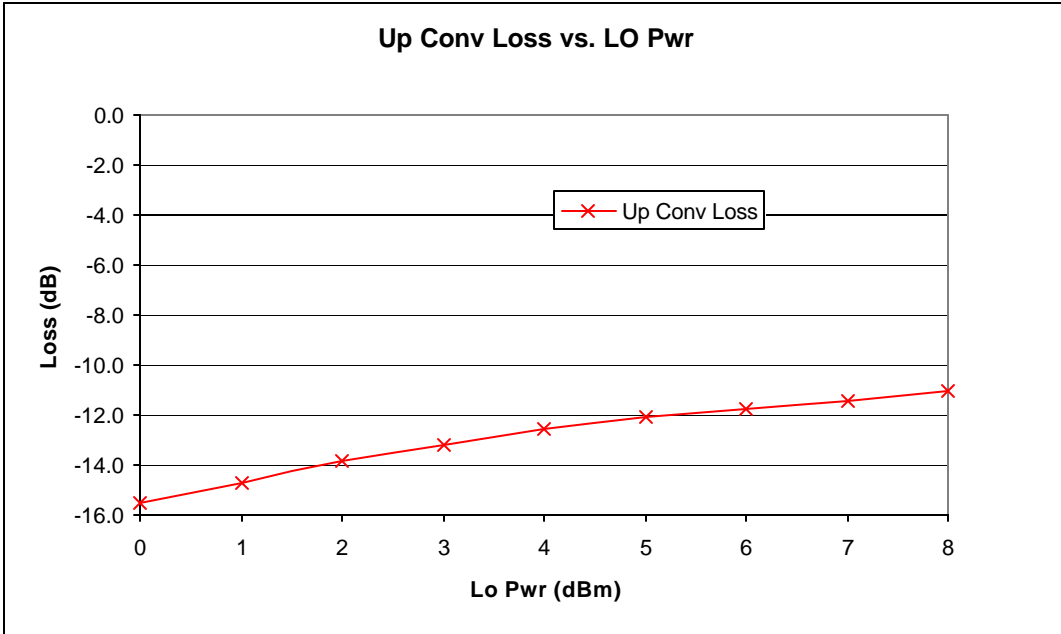
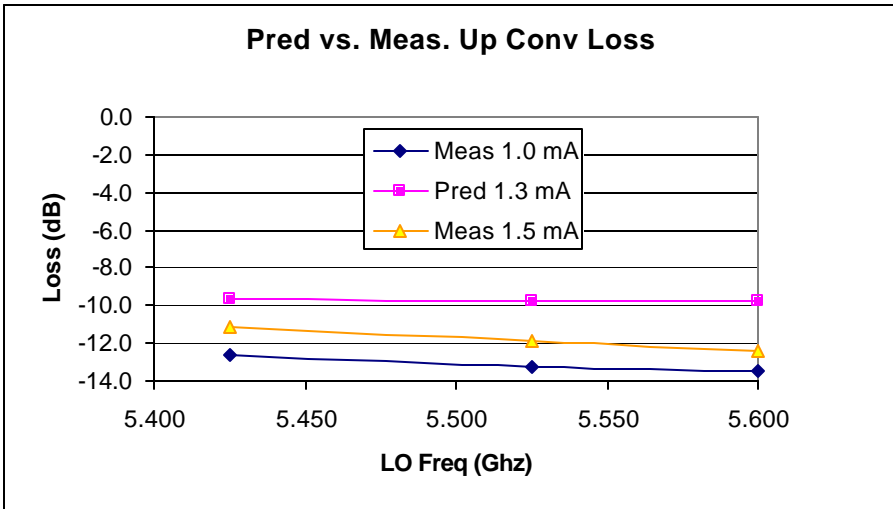
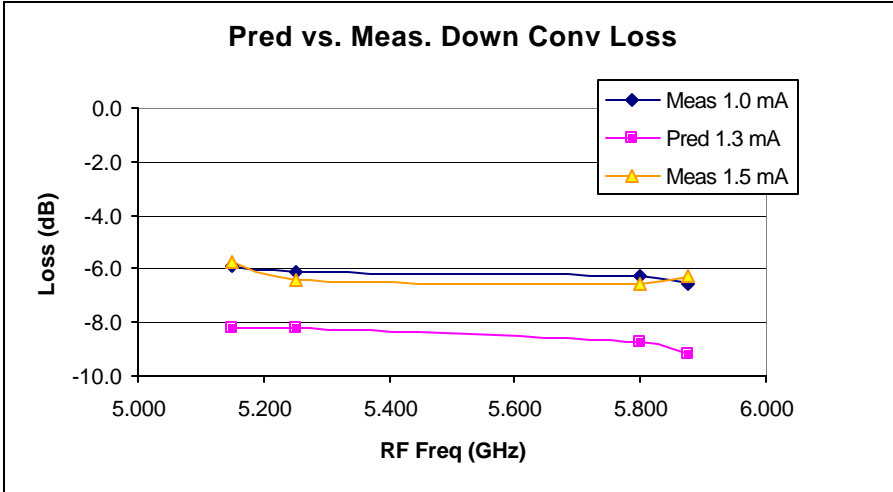
The driver amplifier was intended to operate over the 5.1 to 5.9 GHz band and have a moderate output power of about 15 dBm to drive the power amplifier stage. Bias was about 75 mA from a single +5V supply. Gain was a little lower than predicted but output P1dB was actually higher than predicted. Below are the measured s-parameters and output power versus input power for the driver amp. Peak measured output power was 18 dBm at 5.8 GHz with 5V at 66 mA for an 18% PAE.



Mixer—By Willie Thompson

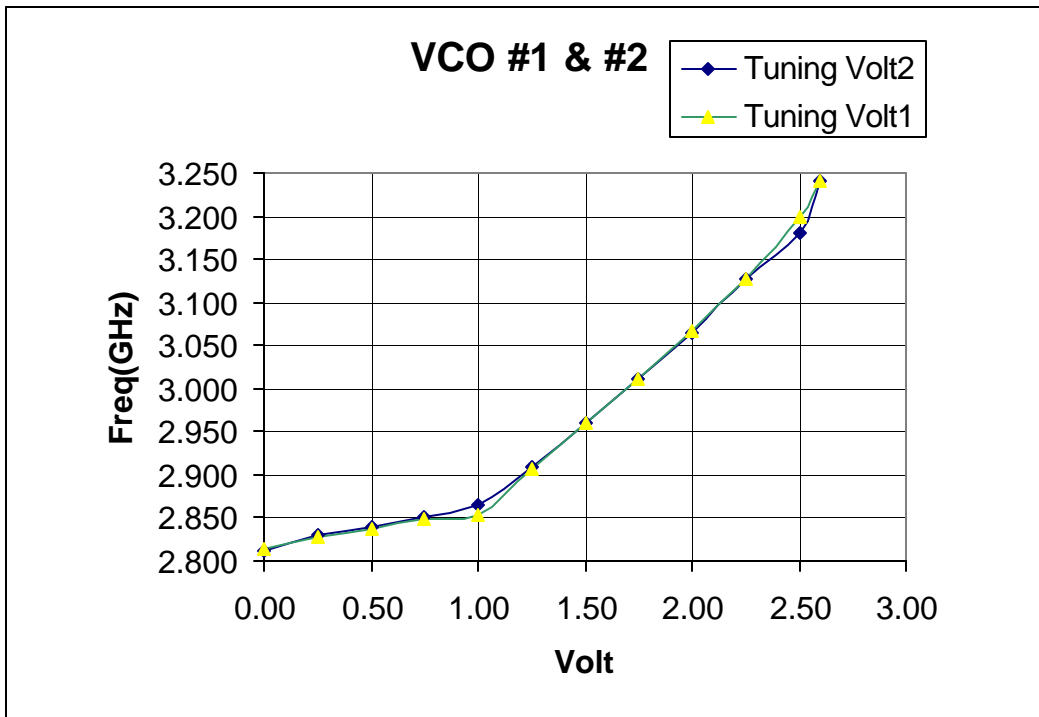
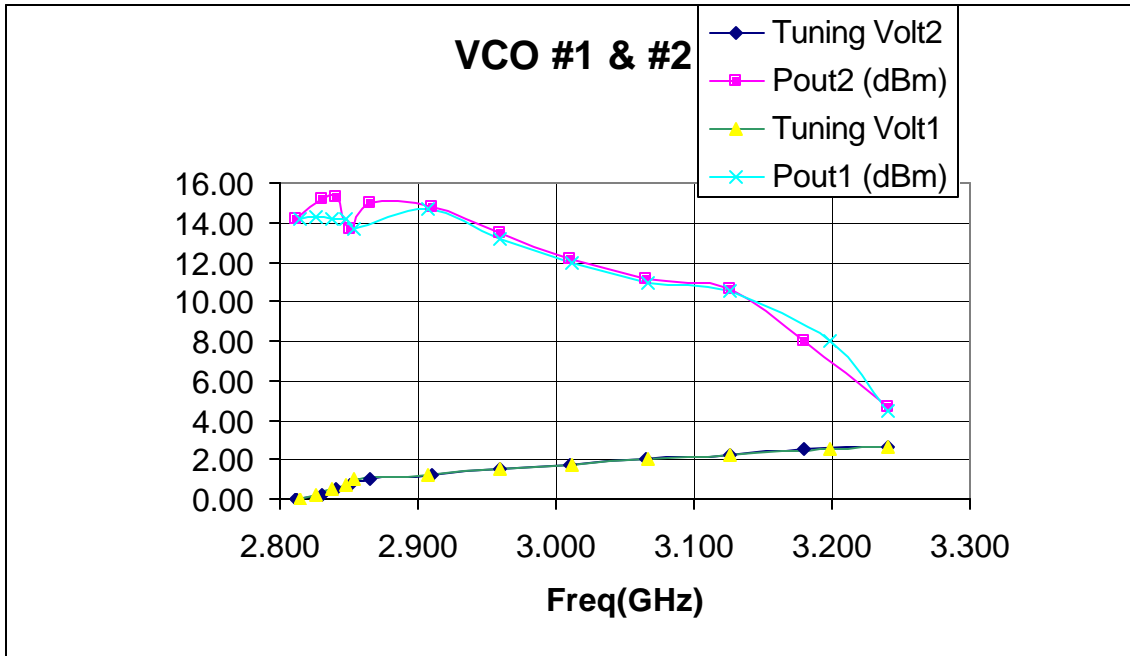
The mixer was designed to down or up convert either band to a 275 MHz IF signal. GFETs configured as diodes were used for the mixer. S-parameters are shown for the RF and IF inputs (LO is missing). Performance plots are shown for upconversion and downconversion mode. Bias was 5V at about 1.3 mA with resistors to drop the input voltage into the diode threshold range. Measurements were made at 5V at about 1.0 mA and 7V at 1.5 mA. Match seemed to improve at 7V but performance varied a bit. Up conversion/down conversion loss is shown over the bands at both bias points as well as up conversion loss vs. LO drive.



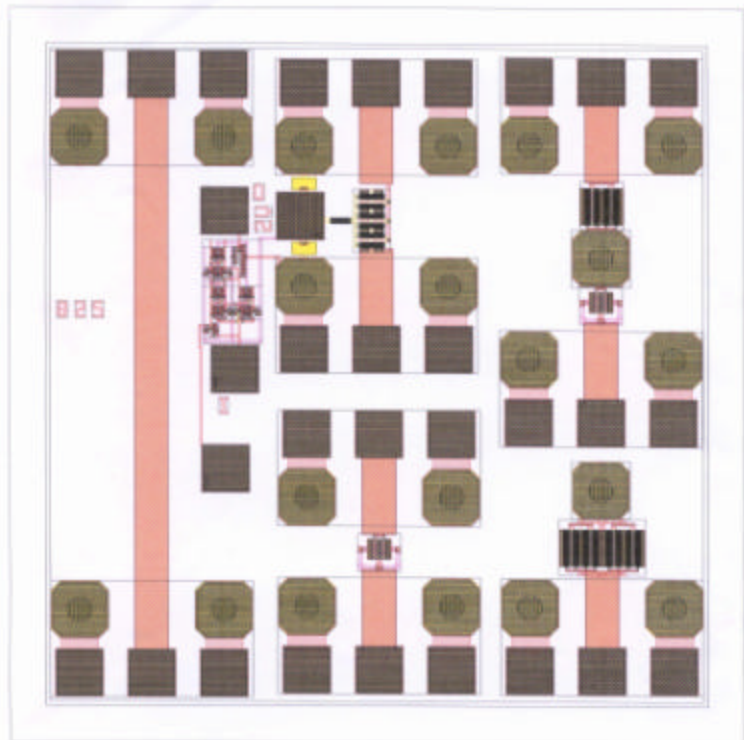
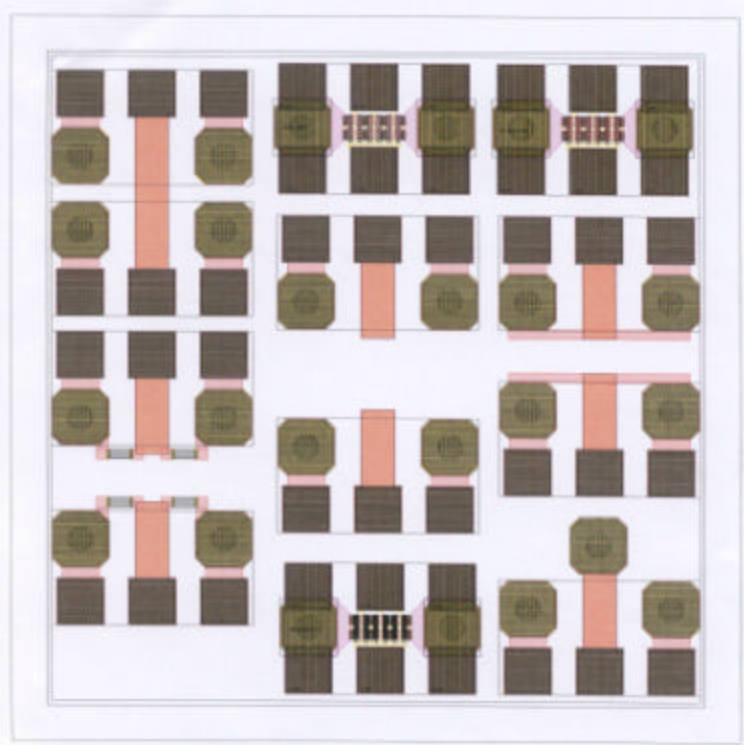


Voltage Controlled Oscillator—By Gary Levy and Steve Williams

The voltage controlled oscillator was designed to output 2.7 to 2.8 GHz which would feed the doubler circuit. Bias was about 66 to 68 mA at +5V. Frequency range exceeded expectations but the low end of the oscillator frequency was a bit higher than the simulations. Shown are output power and tuning voltage required versus the output frequency. The second plot shows output frequency versus control voltage.



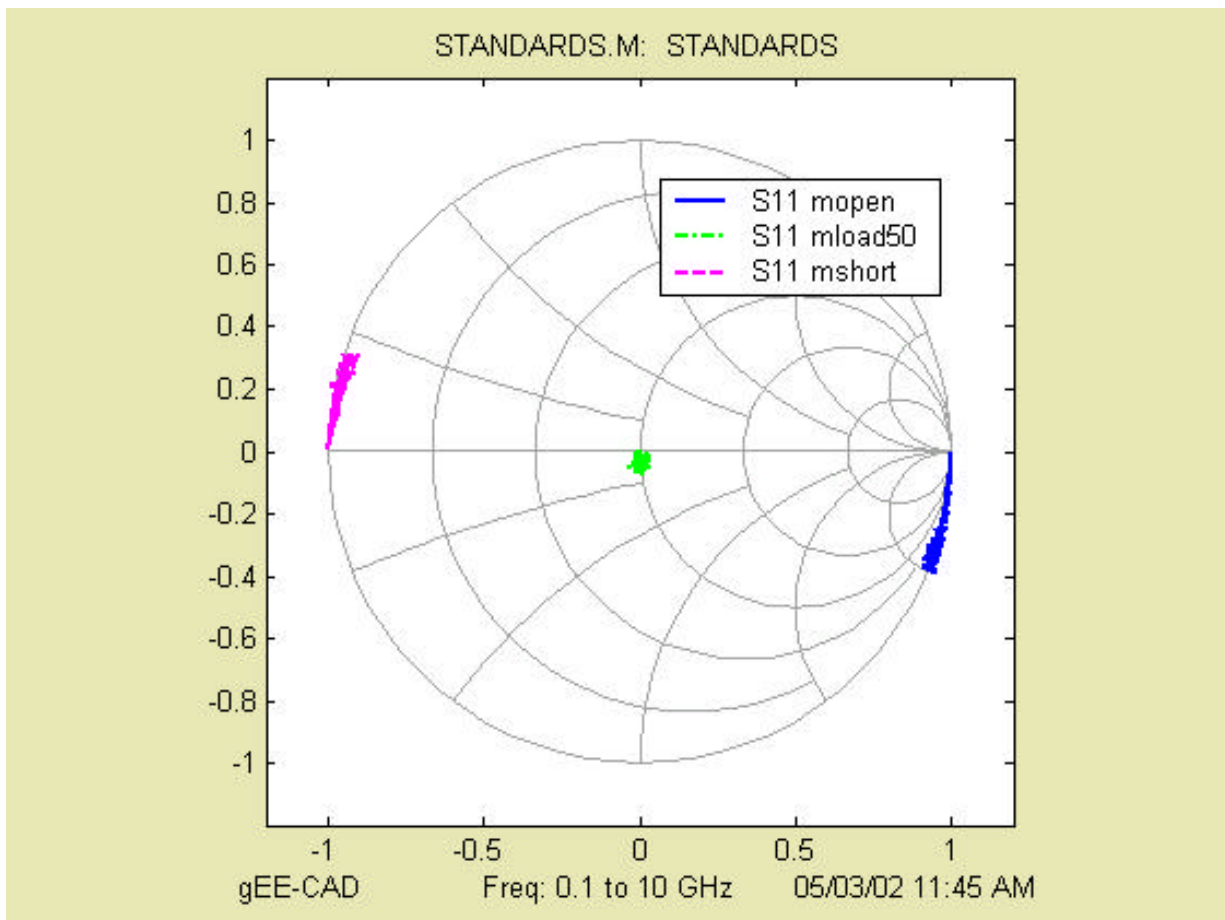
Other: Calibration structures and devices were included and measured. A GFET, DFET, EFET, GFET Switch, GFET diode (mixer), and GFET varactors (VCO) were measured and compared to models. An SOLT calibration was done for the initial measurements. The probe tips used are a little worn leading to “noisy” data.



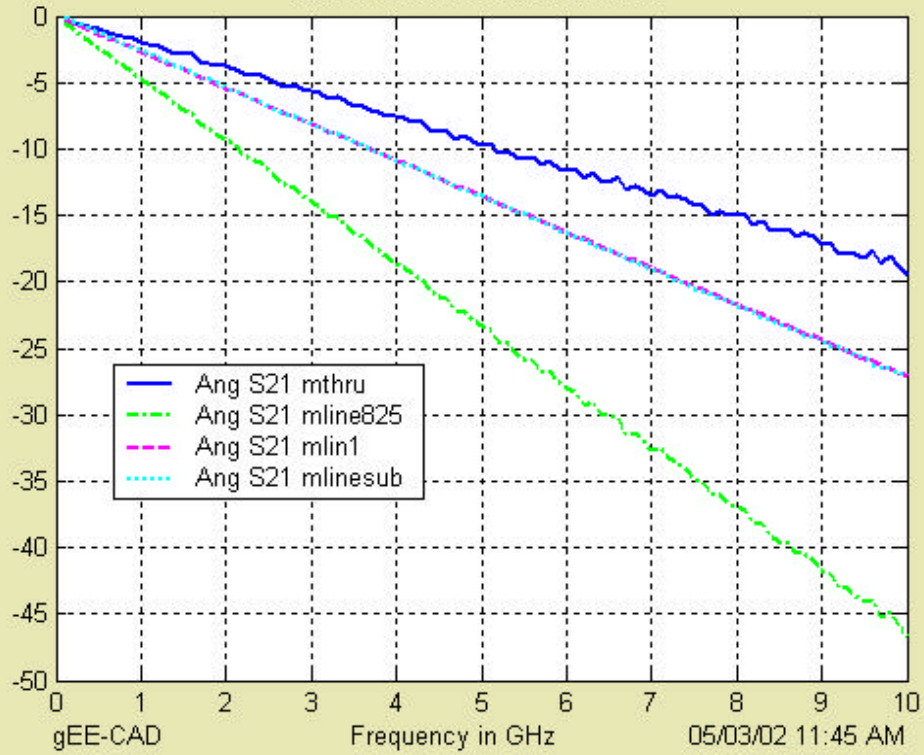
Lines and Standards:

Cal standards included coplanar to microstrip launches with 50 ohm loads (2-100s in parallel), shorts (via), open, a thru, and a line of an extra 825 um length in 50 ohm microstrip. These were used to deembed some of the other measured devices. Shown are some plots of the phase of a modeled 825 um line in GaAs versus the deembeded line length. Also shown are the phase and loss (s21) of the thru and 825 um line standard.

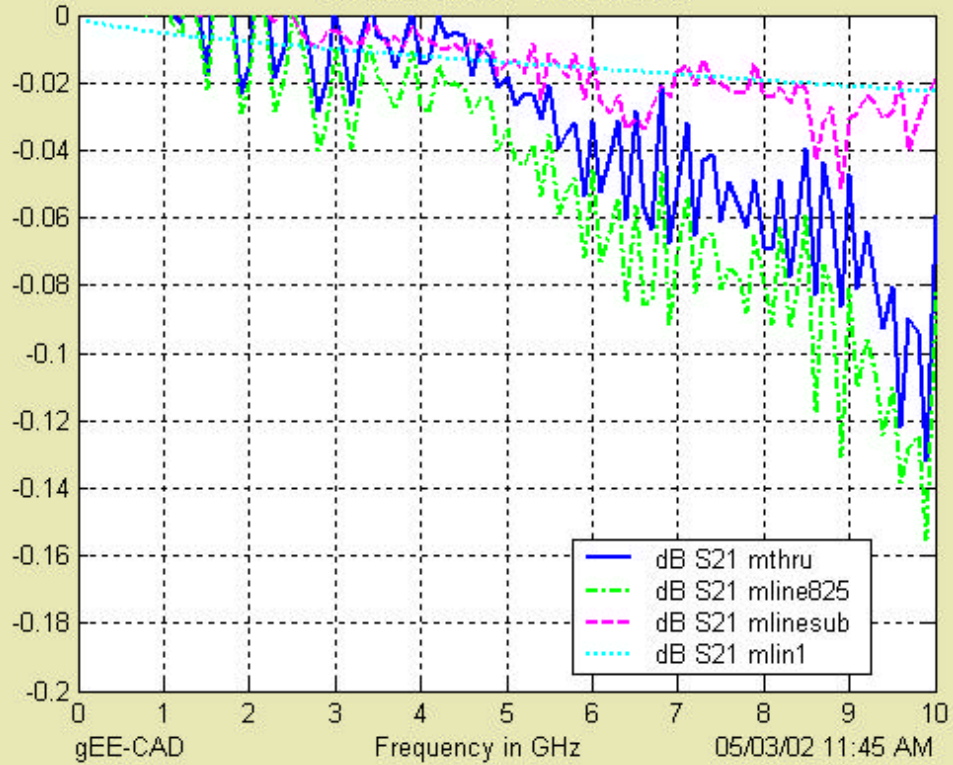
Below is the S11 of the 50 ohm load, short, and open standards. A simple model for the length of the launch is a transmission line of 5 degrees phase at 5 GHz. A mathematical approximation of half of a thru was also calculated and was used for deembedding. The mathematical approximation accounts for some of the “noisy” phase comparisons. “Mlin1” is a model of 825 um of 50 ohm microstrip in GaAs, and “mlinesub” is the measured line (mline825) minus the “thru” (mthru) standard.



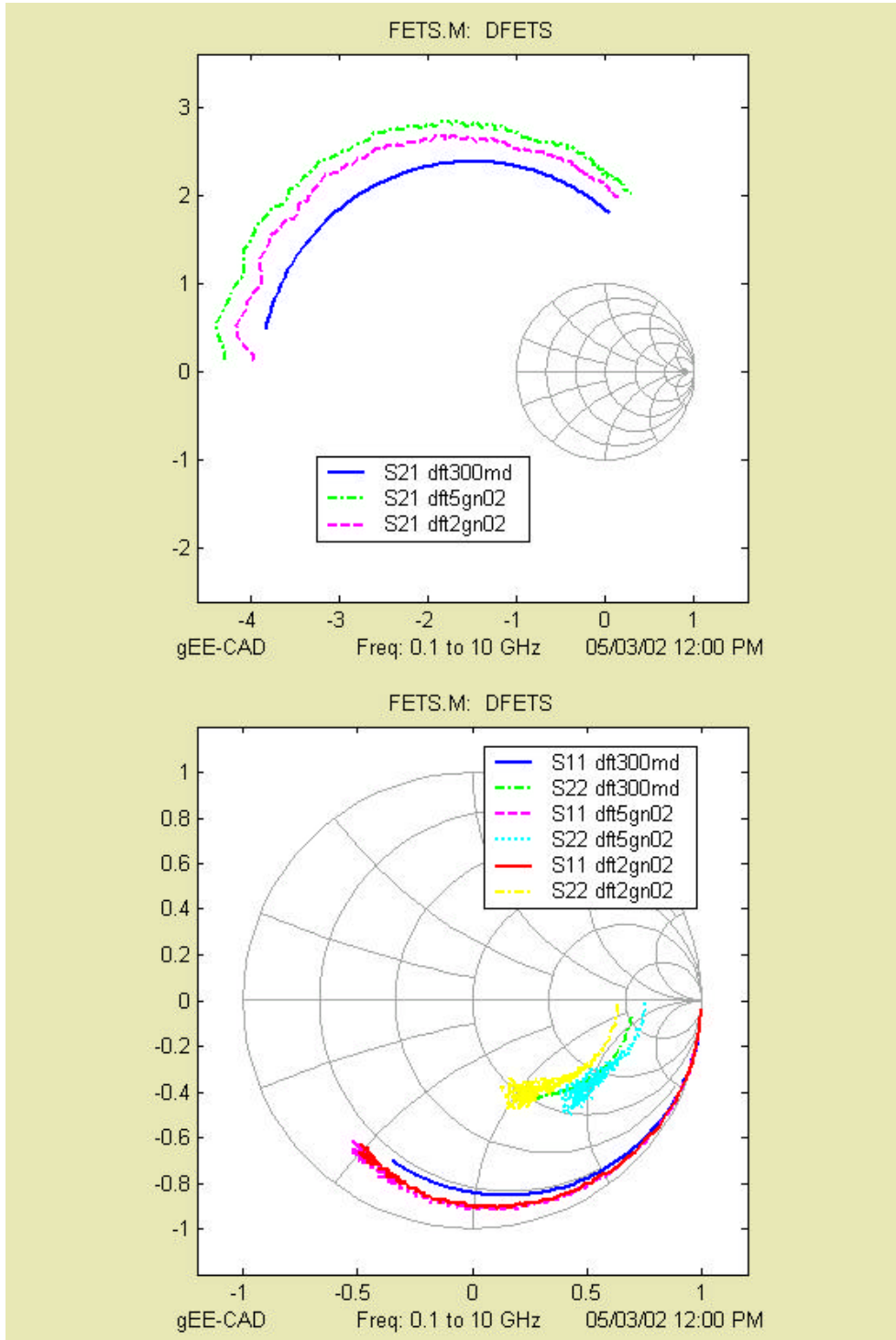
STANDARDS.M: LINES ANGLE



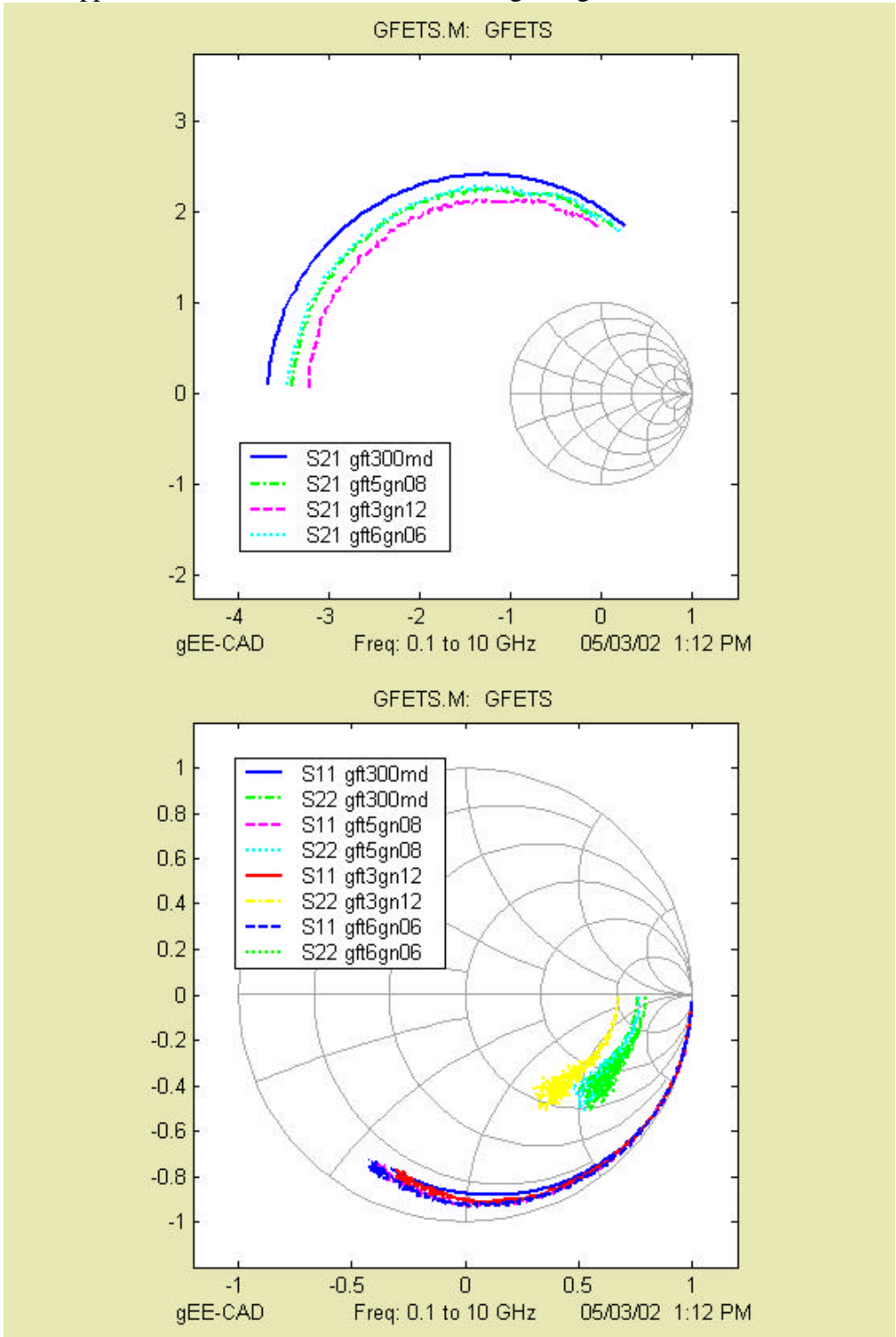
STANDARDS.M: LINES LOSS



DFETs: A standard 300 um DFET was included as a test structure. Measurements were made at various biases. Shown are measurements at 2V and 5V VDS at a VGS of -0.2V versus the typical model 2V VDS at -0.2V VGS (dft300md). Additional measurements were taken of IDS vs. VDS. Pinchoff appears to be nominal but IDSS was about 20% higher than expected which could explain why some of the students designs using DFETs were a little high in current.

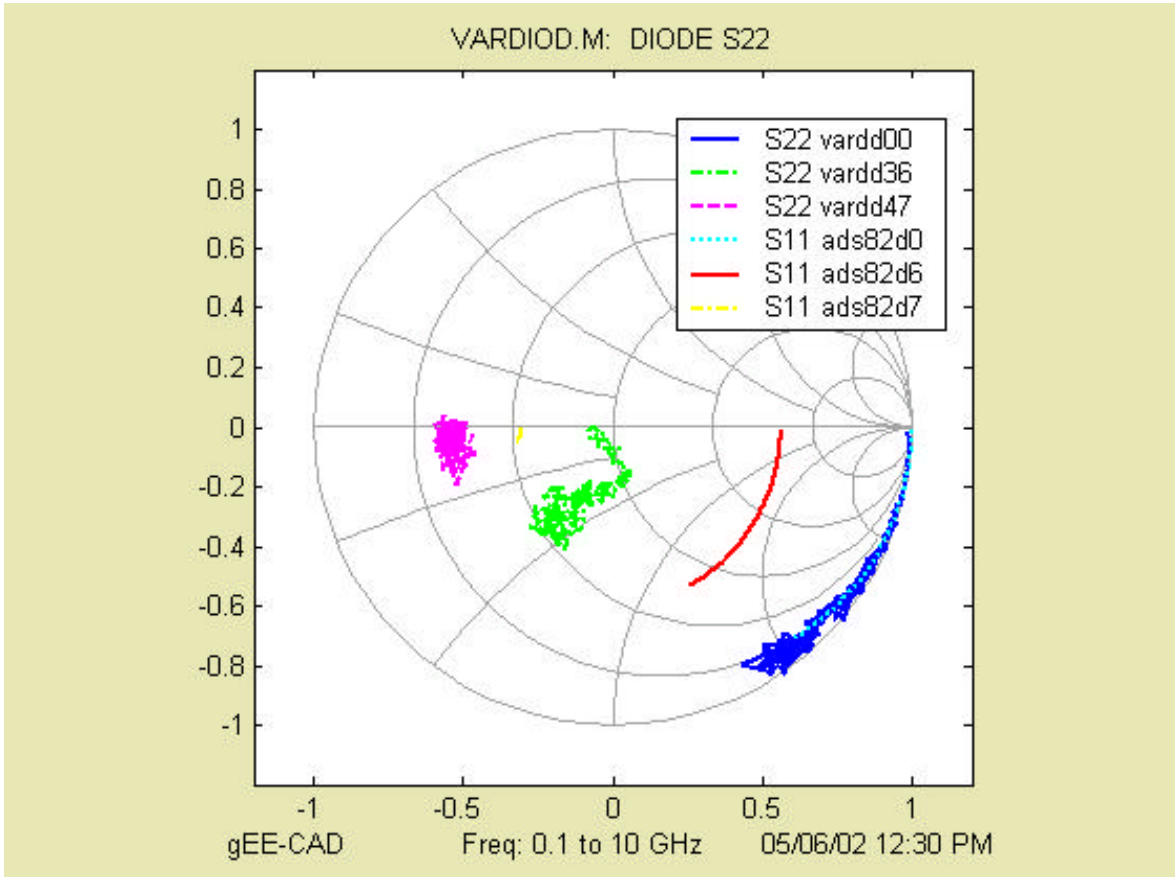


GFETs: A standard 300 um GFET was included as a test structure. Measurements were made at various biases. Shown are measurements at 3V, 5V and 6V VDS at a VGS of -1.2V, -0.8V, and -0.6V respectively versus the typical model 5V VDS at -0.8V VGS (gft300md). Additional measurements were taken of IDS vs. VDS. Pinchoff and IDSS appear to be nominal for this wafer run regarding the GFETs.



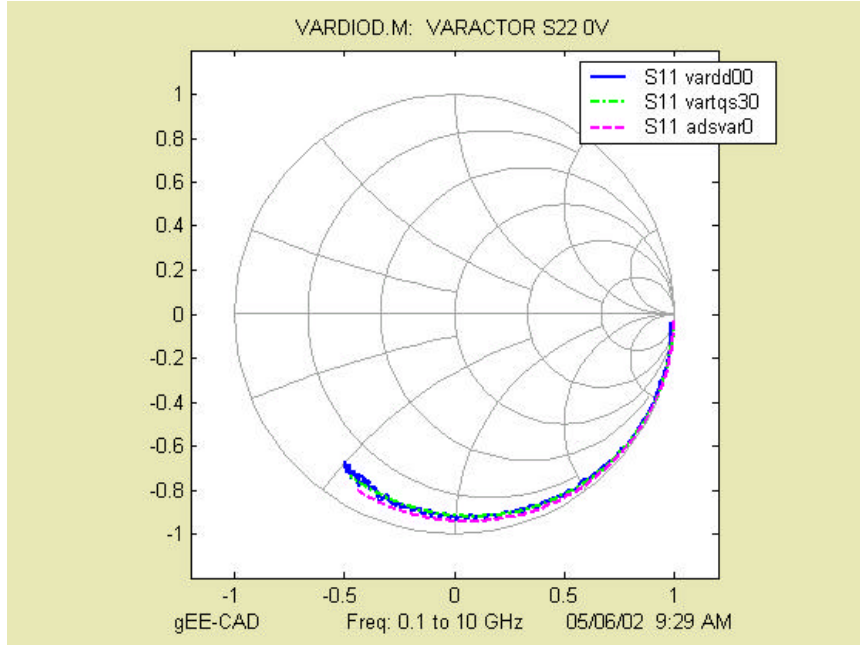
GFET Diode (82 um—2 x 41 um):

Shown are ADS simulations of the 82 um GFET diode at 0V, 0.6V, and 0.7V. This diode was used in the Mixer MMIC Design. The measured data at 0.6V and 0.7V seems to match the “trend” of the ADS simulations but appears to be sensitive to voltage in this range. A simple off model for the diode at 0V would be a capacitor of about 0.18 pF and a simple “on” model for this diode at 0.7V would be a 15 ohm resistor. Scaling the “on” resistance to a 300 um GFET diode would be about 4 ohms which seems about right. Data was also taken of the 82 um diode as a 2 port and of a 300 um diode to ground with similar characteristics (not shown).

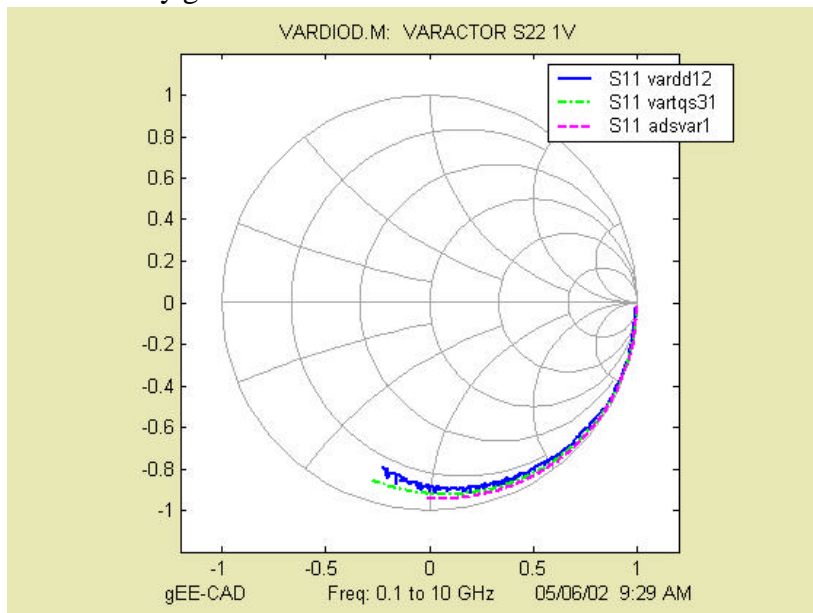


GFET Varactor (300 μm —6 x 50 μm):

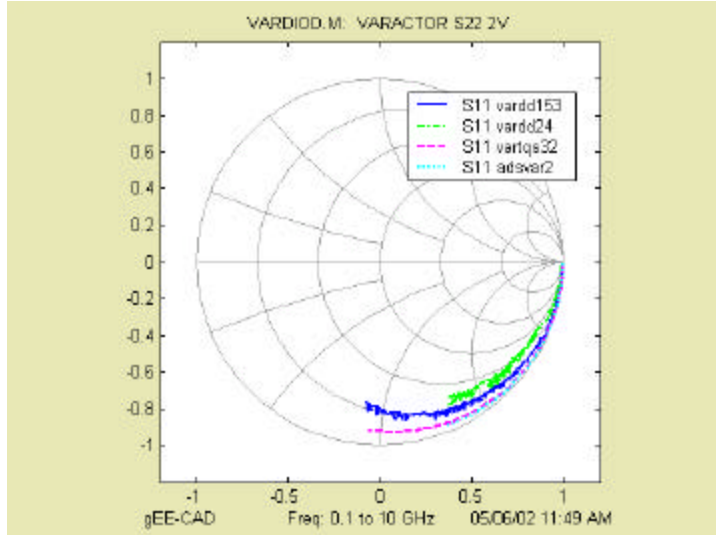
Previously a linear varactor model was fit to TriQuint supplied TOM2 model parameters for a reverse biased GFET (i.e. varactor diode). The linear model is a parallel parasitic capacitance of 0.04 pF with a series resistor plus variable capacitor of 5 ohms resistance and a varying capacitance of 0.3 pf at -2V , 0.4 pF at -1V , and 0.55 pF at 0V . The current ADS TOM3 model was compared to measurements of a 300 μm varactor and a 600 μm varactor as well as this linear model. Below is the plot of the measured varactor versus the ADS TOM3 model and the previously “fit” linear model. While the linear model is an excellent fit, the GFET TOM3 model in the reverse biased diode case is very close up to 10 GHz.



Next, the measured data is shown at -1V again showing excellent fit with the linear model and reasonably good fit with the GFET TOM3 model reverse biased.



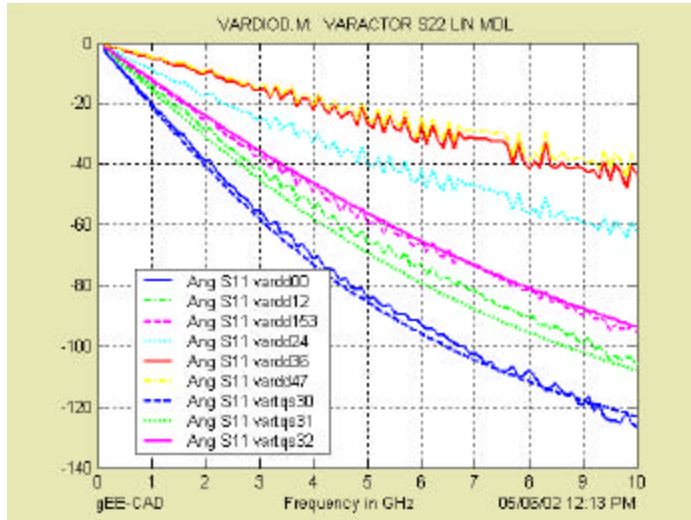
This Plot shows the linear model for $-2V$ versus the ADS model and the measurements at $-1.5V$ and $-2V$. The ADS model seems to be closer in phase while the linear model appears closer to the $-1.5V$ bias. Some of the error as the bias gets closer to pinchoff could be due to processing variations. Also, the measurements at $-1.5V$ and $-2.0V$ appear to be “lossier” than the expected 5 ohm resistance. Not sure why. The varactor capacitance continues to vary up to a useable $-4V$ as shown in the plots.



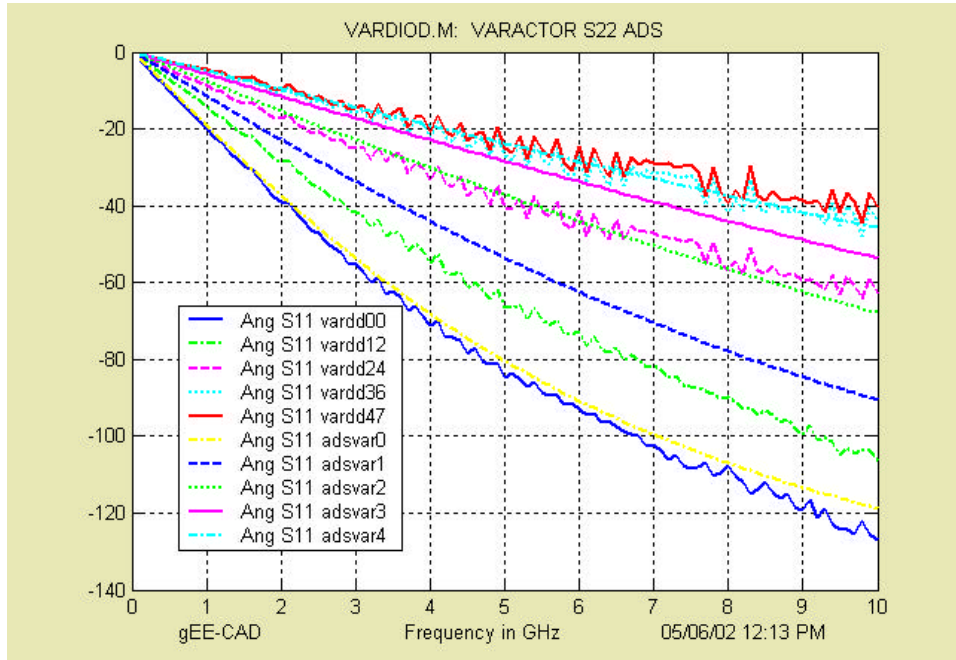
Measurements were made from $0V$ to $-5V$ showing a similar fit to the model over the $0V$ to $-2V$ range. Shown are the old model versus a model “fit” to the current wafer run. Good fit for 0 , -1 , and $-1.5V$.

Parallel capacitance $C_{pp}=0.04\text{pf}$ in parallel with series $R1/CV$.
 $R1=5$ ohms, in series with variable capacitance CV as follows:

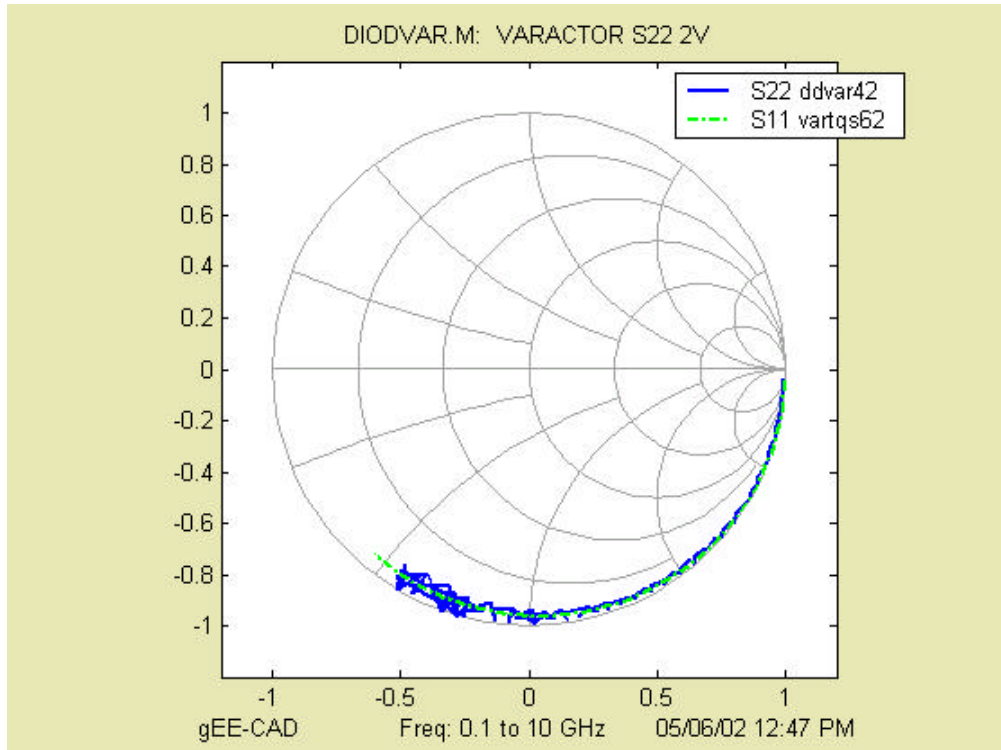
Bias (V)	Old CV	New CV Fit
0	0.55 pf	Same
-1	0.4 pF	Same
-1.5	NA	0.3 pF
-2	0.3 pF	0.18 pF
-3/-4	NA	0.1 pF



Following is a plot of the ADS TOM3 model for a GFET varactor at 0, -1, -2, -3, and -4V. Good fit to phase at 0, -2, and -4V.



Following are the measurements of a 600 μm GFET as a varactor with the linear model scaled ($R=2.5$ ohms, $C_{pp}=0.08$ pF, $C_V=1.1$ to 0.6 pF). Shown is the -2V plot which shows excellent agreement with the scaled model. Likewise the 0V and -1V plots showed excellent agreement. Possibly the discrepancy of the 300 μm varactor at -2V is an error in the measurement. The 600 μm Varactor was used in the VCO MMIC.



GFET Switch (300 μm —6 x 50 μm): Measurements were taken of a 300 μm GFET as a 2 port switch at 0, -1, -2, -3, -4, and -5V. None of the fall 2001 students chose to do the MMIC switch needed for the ISM/WLAN system. For S21, a 7 ohm resistor fits the “on” data well while a 90 fF capacitor fits the “off” data (-4V). Using ADS, a simple model of “on” and “off” states was 8 ohms (which compares well to the IV curves) and 66 fF which seems a bit small for a device of this size. Possibly the modeled 8 ohm “on” state model is a good choice in combination with the measured 90 fF “off” state model.

