JHU EE787 Fall 2004 MMIC Results

Sheng Cheng and John Penn

Designs Fabricated by TriQuint Semiconductor

ADS Support by Gary Wray—Agilent

MWO Support by Mark Saffian—AWR

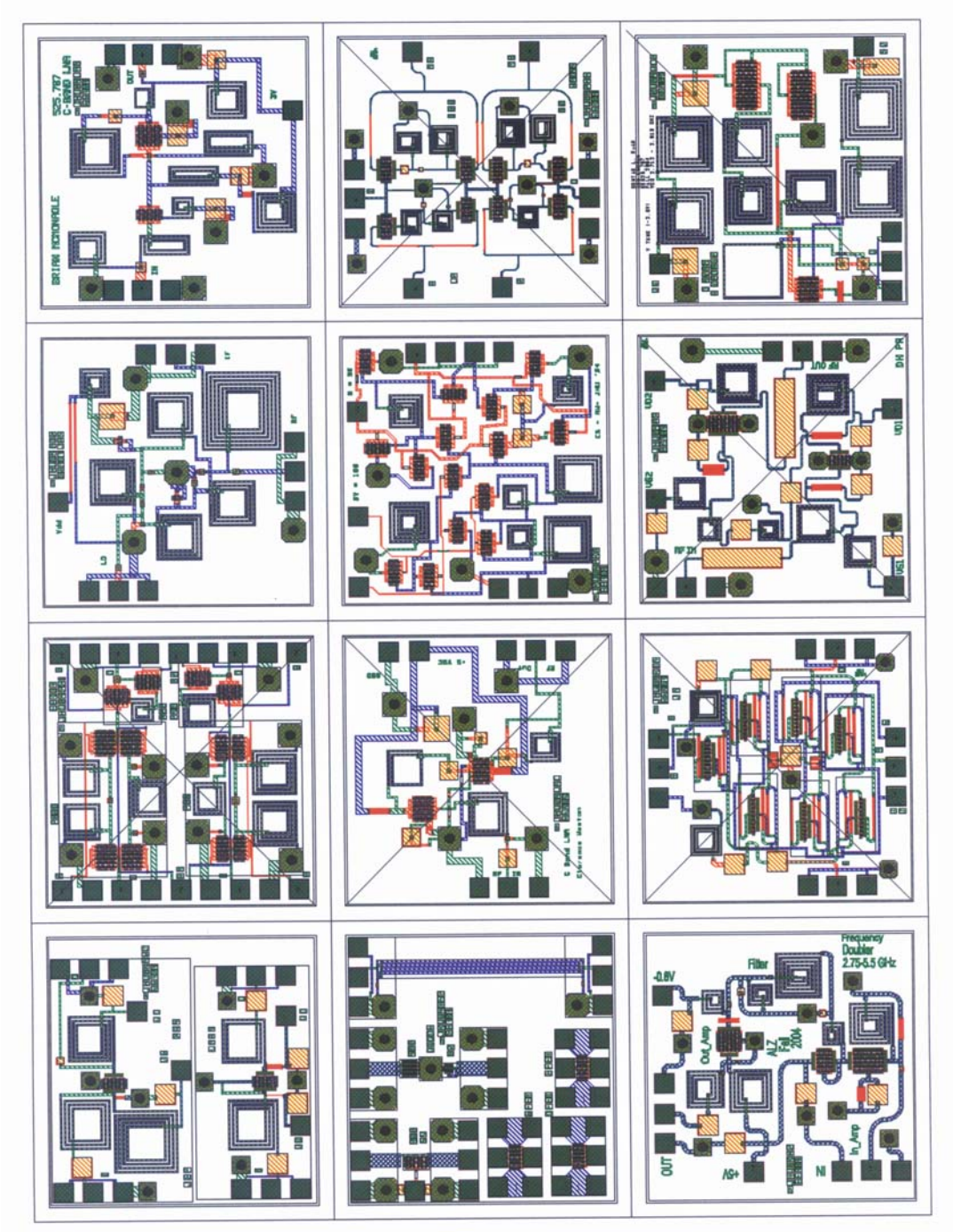
TriQuint TQTRX Library, and ADS or MWO software used for student designs

Nine MMICs were designed by students for the Fall 2004 JHU MMIC Design Course as part of a duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. All designs were tested in the Summer of 2004 after fabrication by TriQuint Semiconductor. The MMIC measurements compare favorably to simulations and all designs were very successful. One phase shifter design had a minor layout problem in its 180 degree bit--one of the two bits in that design. Some MMICs were designed in parallel by different students, so there are two Low Noise Amplifier (LNA) circuits and two Phase Shifter circuits. Two projects had a pair of students working as a team and the other seven designs were solo efforts. In 2003, a simple one stage amplifier and one stage power amplifier were fabricated on a single die to obtain measured data for comparison. Those same circuits were re-layed out in Microwave Office in 2004 and fabricated with comparable performance to the 2003 ADS based design. Attached are plots of the results—small signal s-parameters and appropriate performance tests.

Thanks again to TriQuint, Agilent, and also to AWR (new this year), for their wonderful support of the JHU EE787 MMIC Design Course.

Fall 2004 JHU EE787 MMIC Design Student Projects Supported by TriQuint, AWR, and Agilent EEsof Professors Sheng Cheng and John Penn

Stepped Attenuator—Jacob Morton
Low Noise Amplifier 1—Brian McMonagle
Low Noise Amplifier 2—Clarence Weston
Mixer---Jason Abrahamson
Phase Shifter 1—Henry Weiss
Phase Shifter 2—Andrew Walters & Kevin Shaffer
Power Amplifier—Duane Harvey
Frequency Doubler—Andrew Zundel
VCO—Ade George & Dontae Ryan

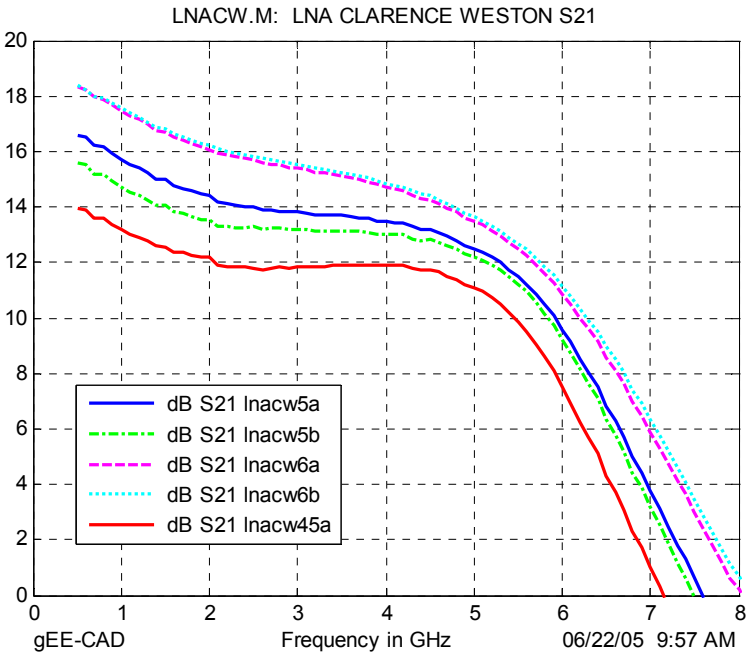


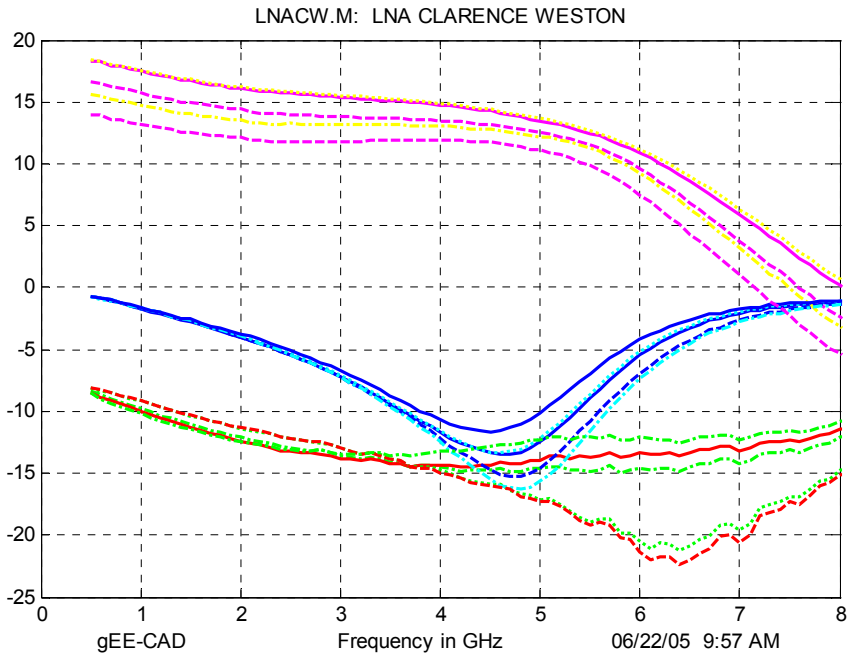
Clarence Weston Low Noise Amp

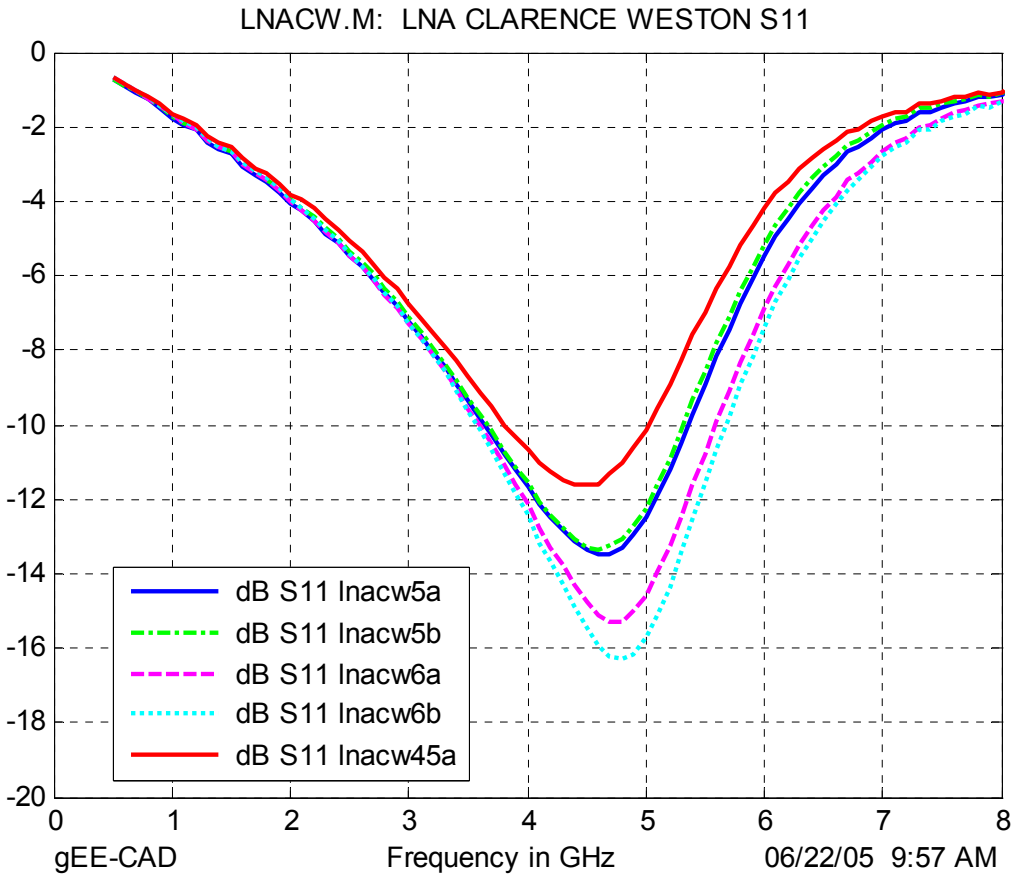
A C-Band LNA was designed for the 5.15 to 5.35 GHz and 5.725 to 5.875 GHz WLAN and ISM bands. The design as measured was close to expectations for the two stage amplifier. It was designed for 5V operation but was tested with good performance from 4.5 to 6V with about the expected bias.

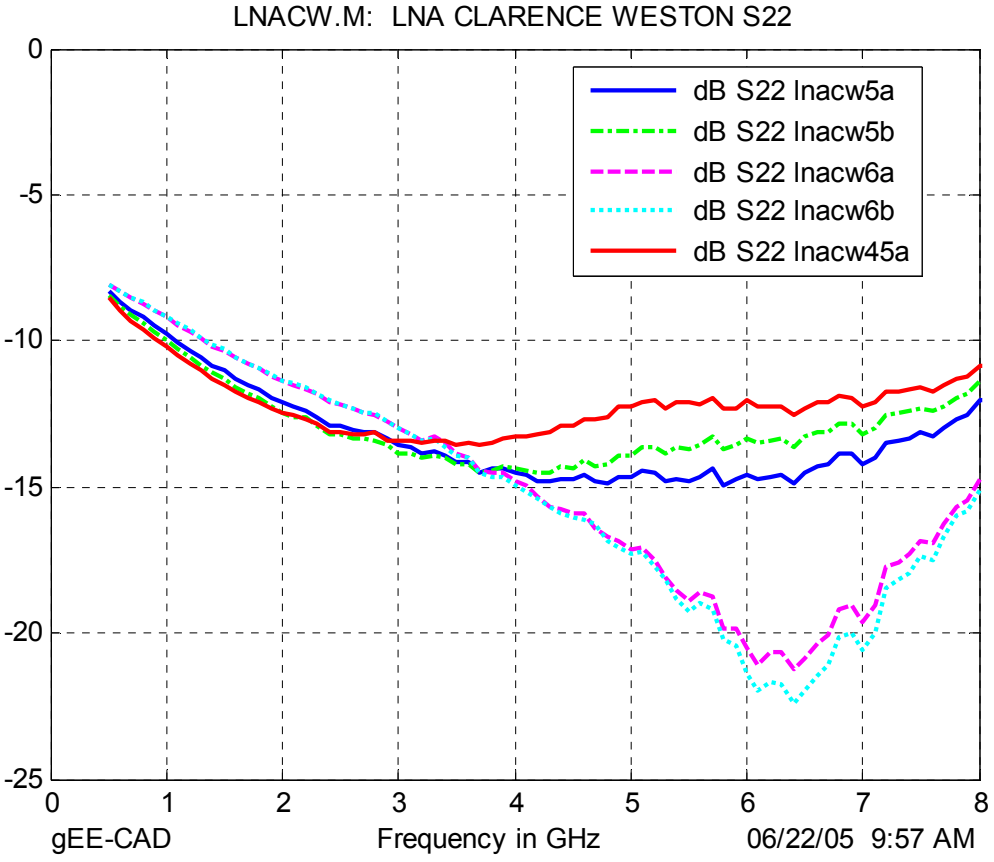
Two Die Measured—Gain dropped off at 4V but looked good between 4.5 to 6V so plot shows Die #1
6V @ 41 mA lnacv6
5V @ 38 mA lnacv5
4.5V @ 37 mA lnacv45

Die #2
6V @ 39 mA lnacv6
5V @ 37 mA lnacv5

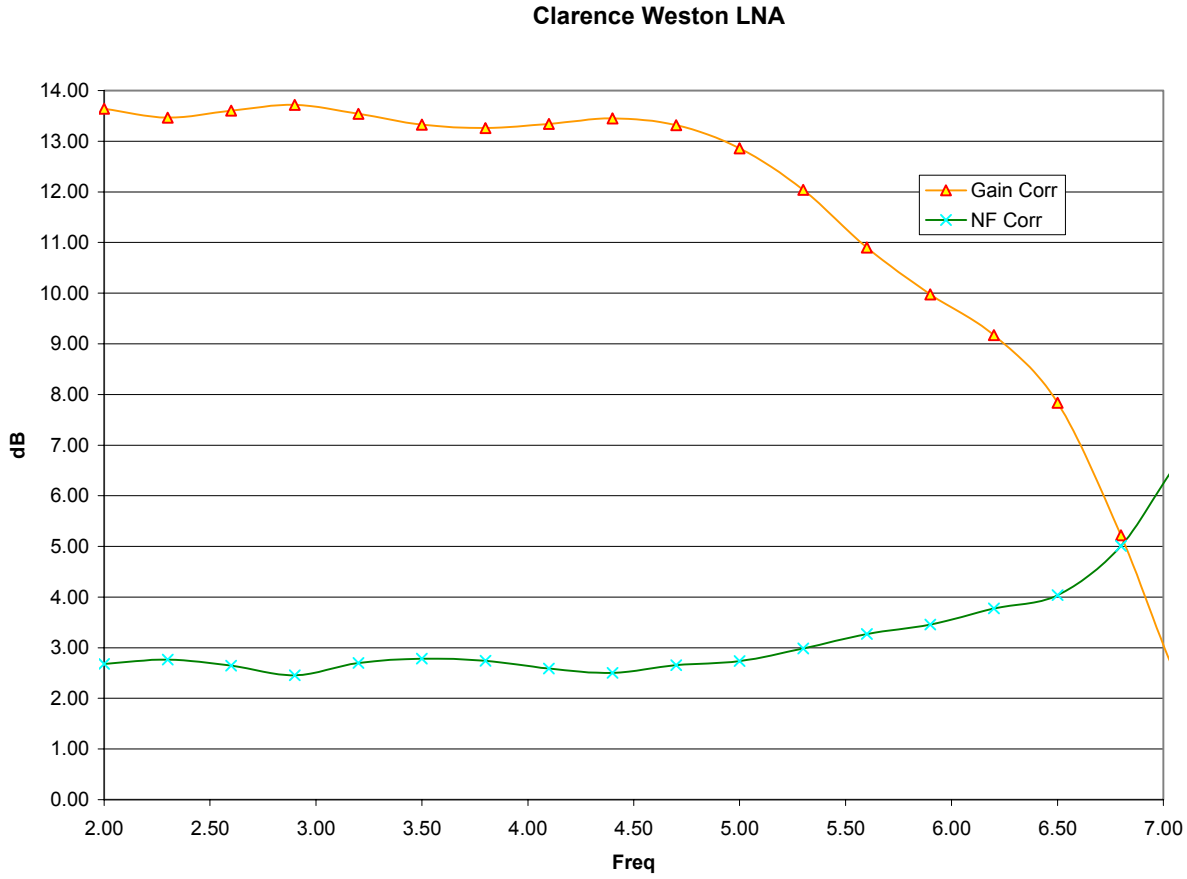








Input and Output Match Plots for two LNA die and various biases.



Freq(Ghz)	Corrected Gain	NF(dB)
2.00	13.64	2.68
2.30	13.47	2.77
2.60	13.61	2.65
2.90	13.72	2.45
3.20	13.54	2.70
3.50	13.33	2.78
3.80	13.26	2.74
4.10	13.34	2.59
4.40	13.45	2.50
4.70	13.32	2.65
5.00	12.86	2.73
5.30	12.04	2.98
5.60	10.90	3.27
5.90	9.98	3.45
6.20	9.17	3.77
6.50	7.83	4.04
6.80	5.22	5.01
7.10	2.11	6.81
7.40	0.49	7.69
7.70	-0.64	8.29
8.00	-1.23	8.62

Measured Noise Figure and Gain after correcting for cable losses (NF ~ 2.5 dB min.).

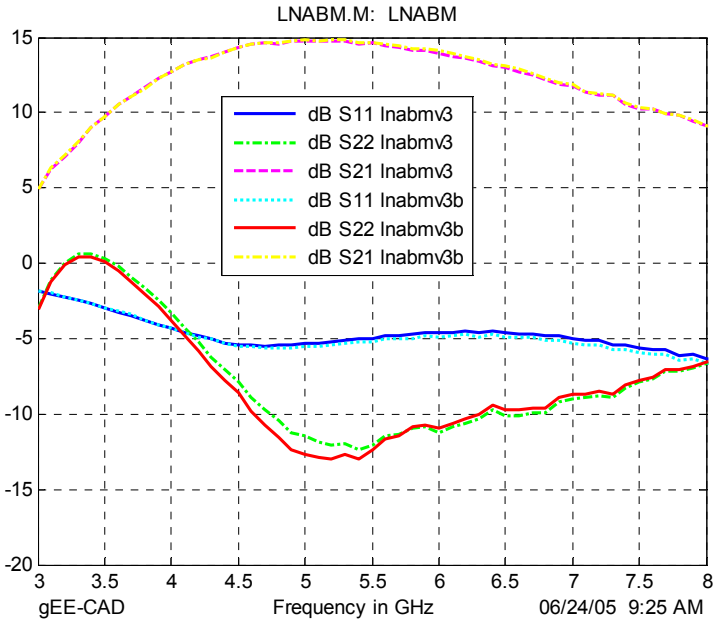
Brian McMonagle Low Noise Amp

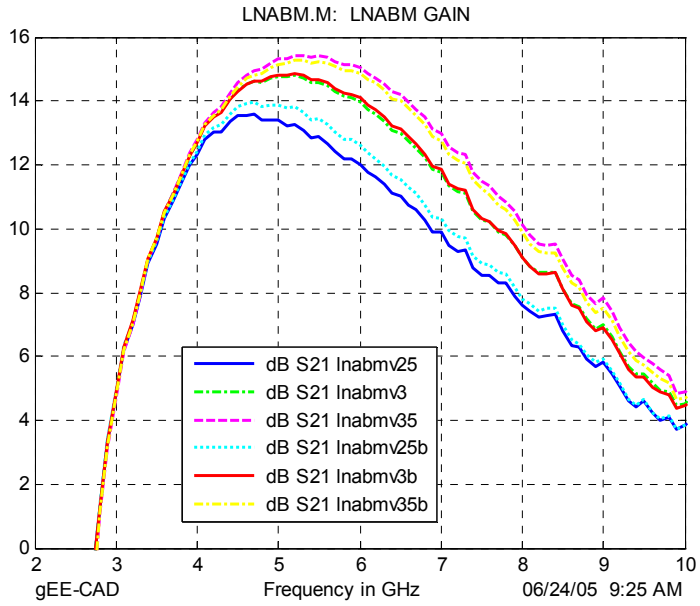
A parallel design of a C-Band LNA for the 5.15 to 5.35 GHz and 5.725 to 5.875 GHz WLAN and ISM bands was created. The design as measured was close to expectations for the two stage amplifier. It was designed for 3V operation but was tested with good performance from 2.5 to 3.5V with about the expected bias.

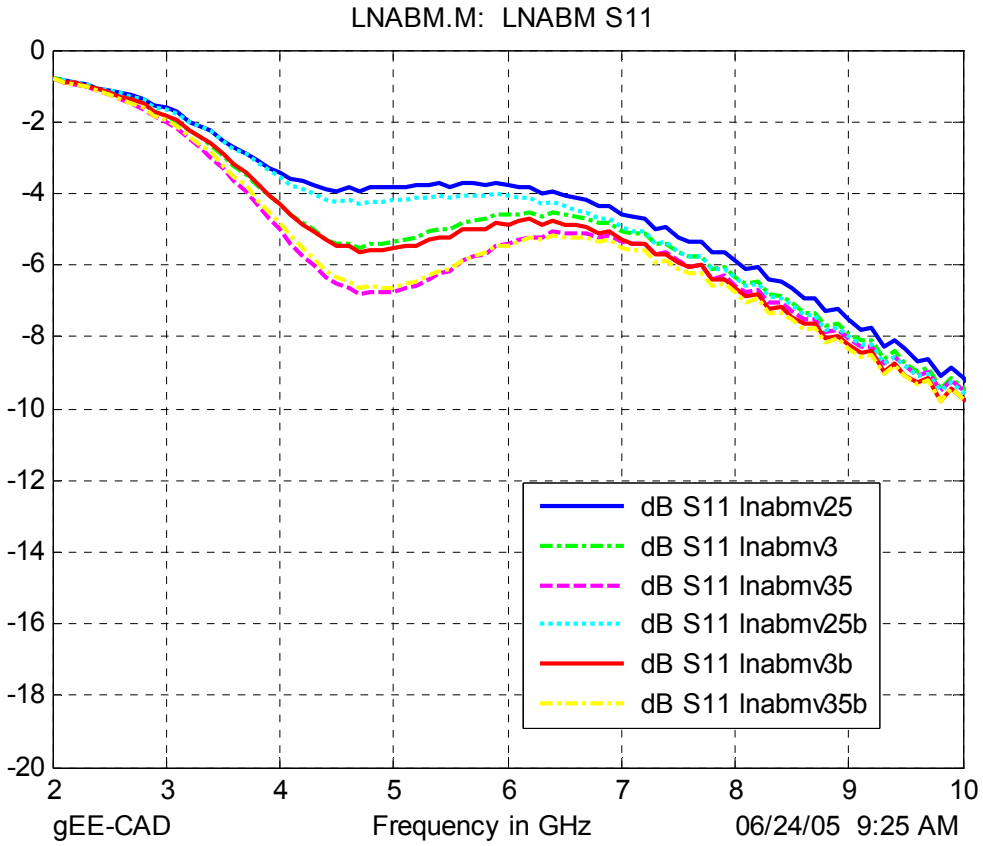
Die #1
2.5V @ 34 mA lnabm25
3.0V @ 34 mA lnabm3
3.5V @ 34 mA lnabm35

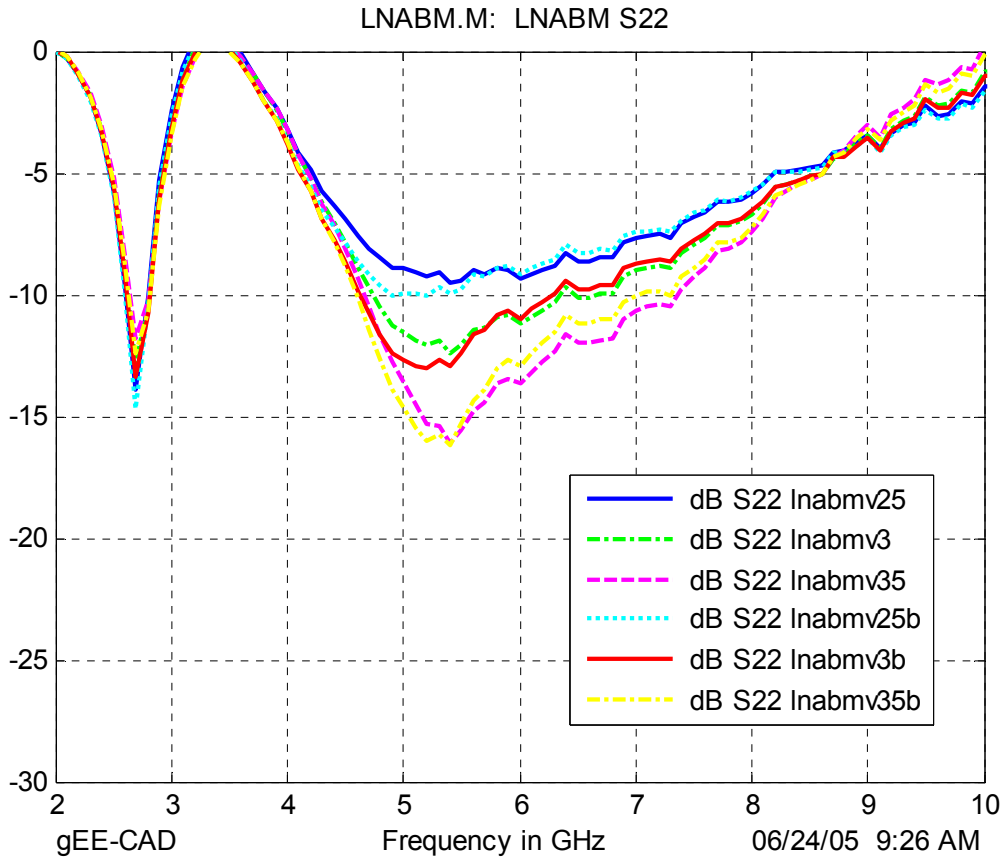
Die #2
2.5V @ 30 mA lnabb25
3.0V @ 31 mA lnabb3
3.5V @ 31 mA lnabb35

Plot of S21, S11 and S22--Two different Die at 3.0V

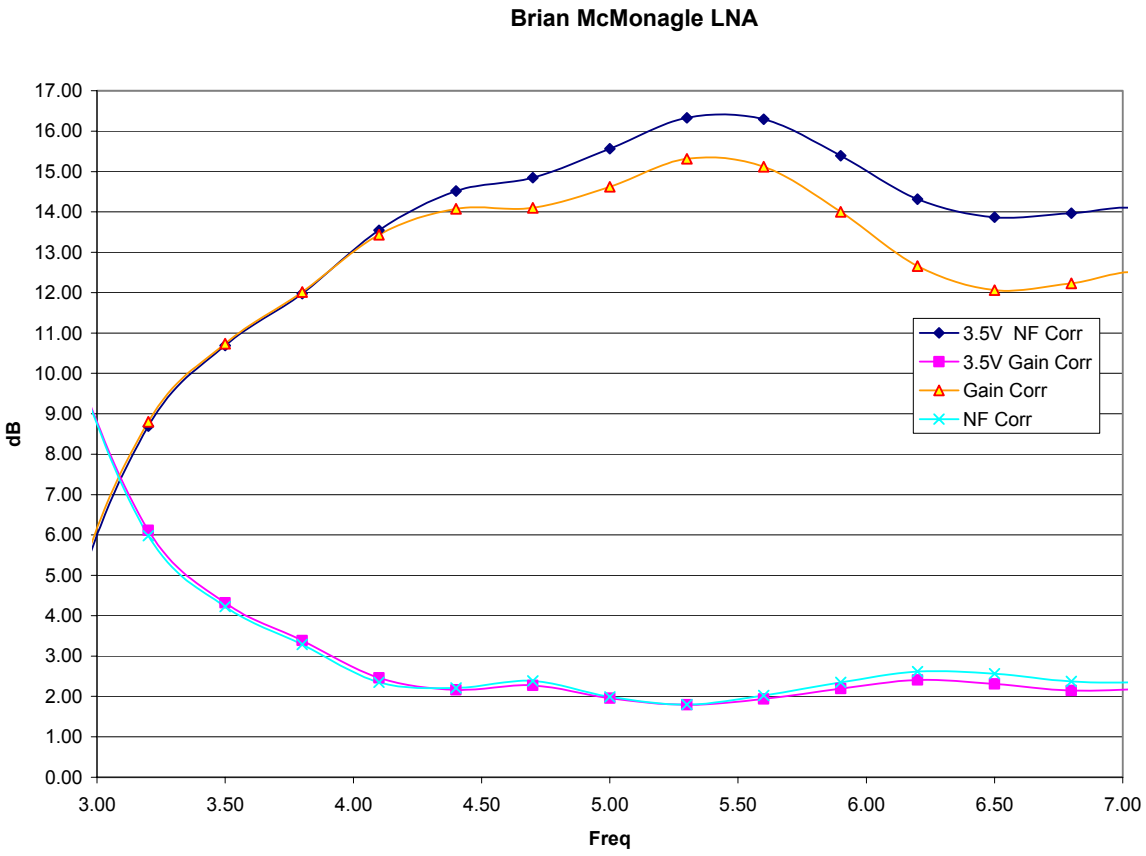


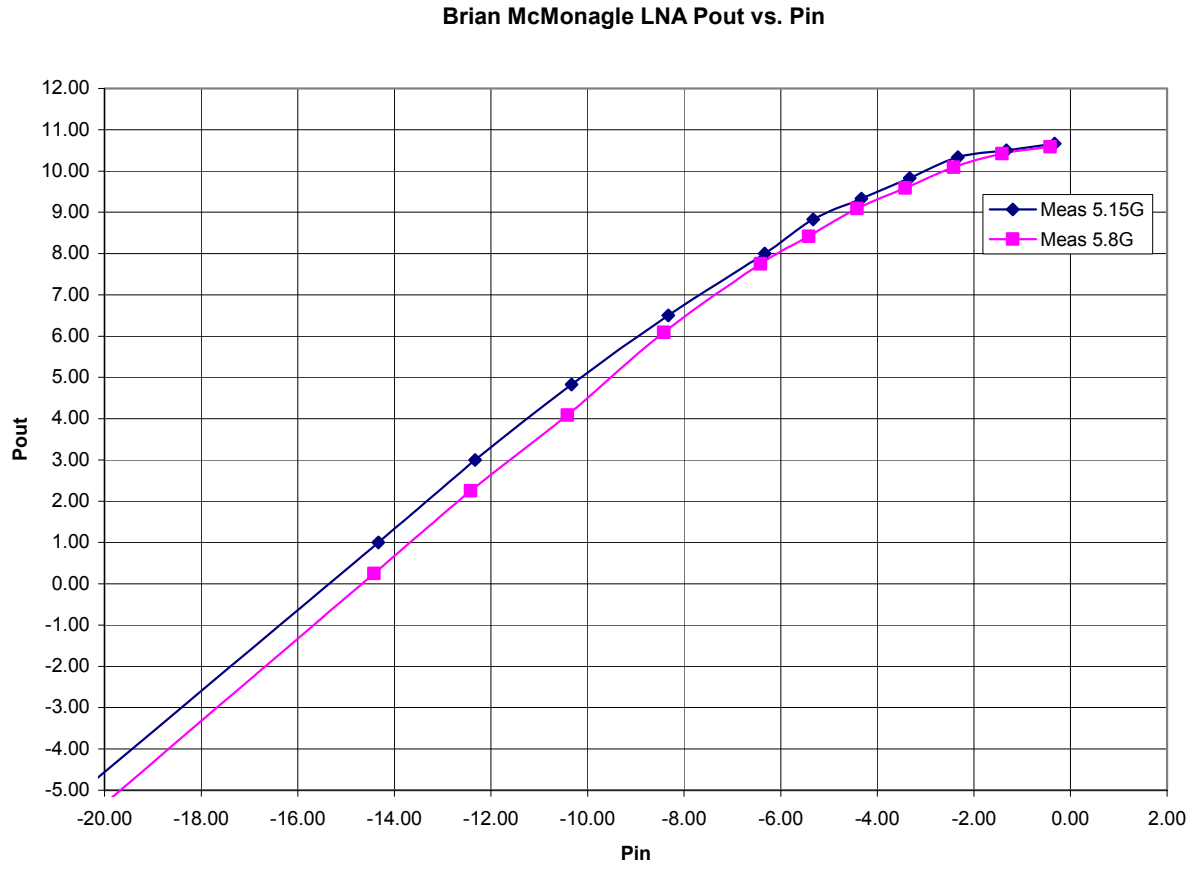






Input and Output Match Plots for two LNA die and various biases.



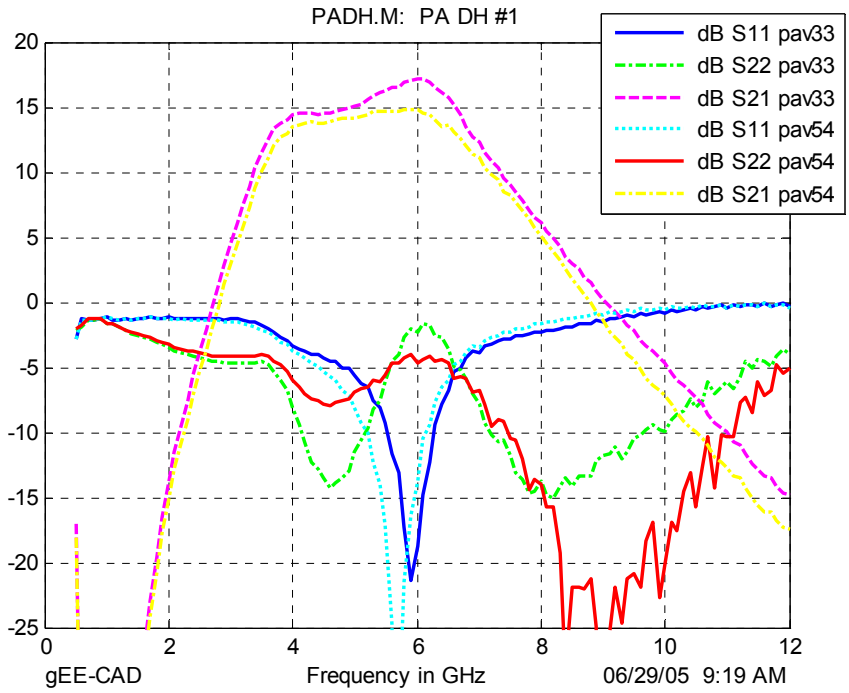


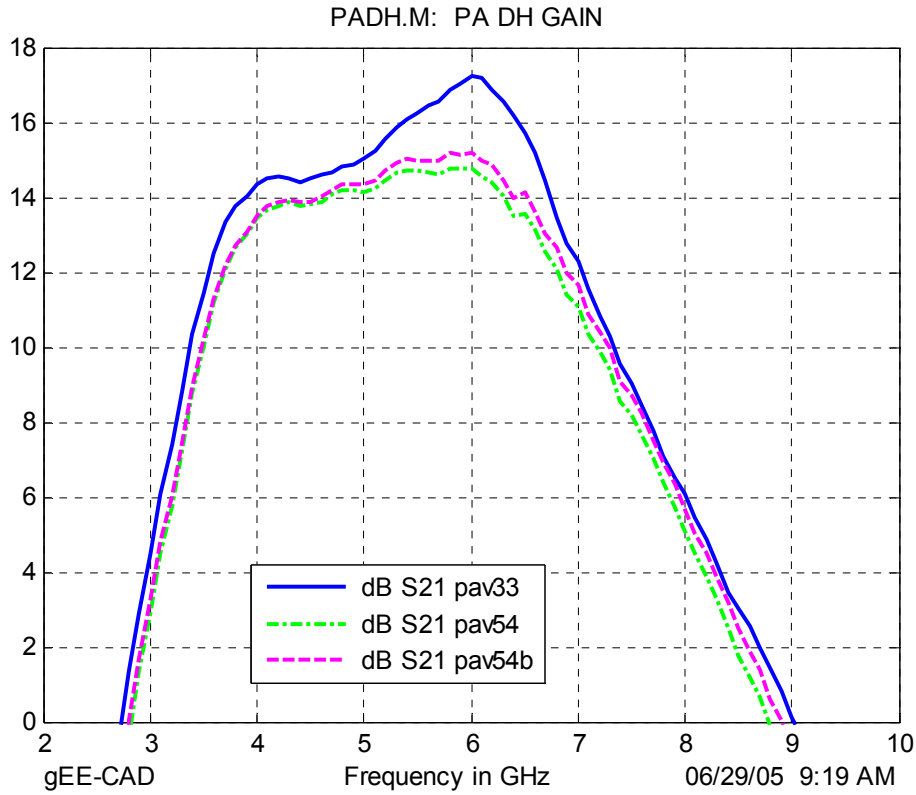
Noise Figure Gain Plot (Top) and Power Output vs. Input for LNA at 3V.

Duane Harvey Power Amp

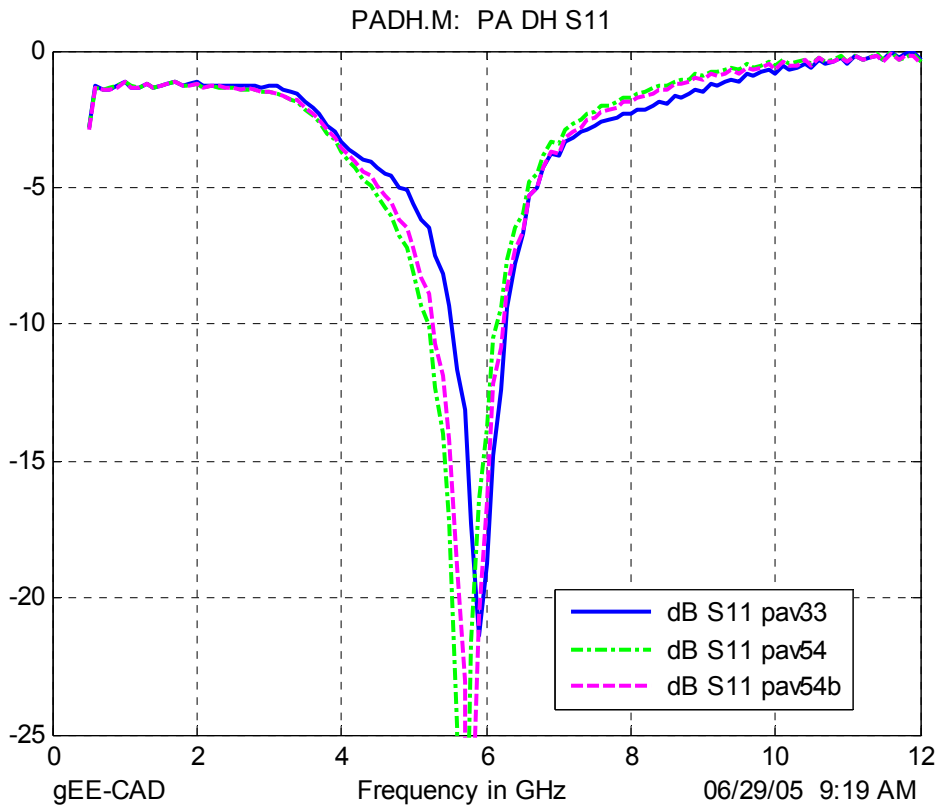
A medium power amplifier (100 mW) was designed for the 5.15 to 5.35 GHz and 5.725 to 5.875 GHz WLAN and ISM bands. The design as measured was close to expectations for the two stage amplifier. It was designed for 4V/5V with separate drain and gate supplies for each stage.

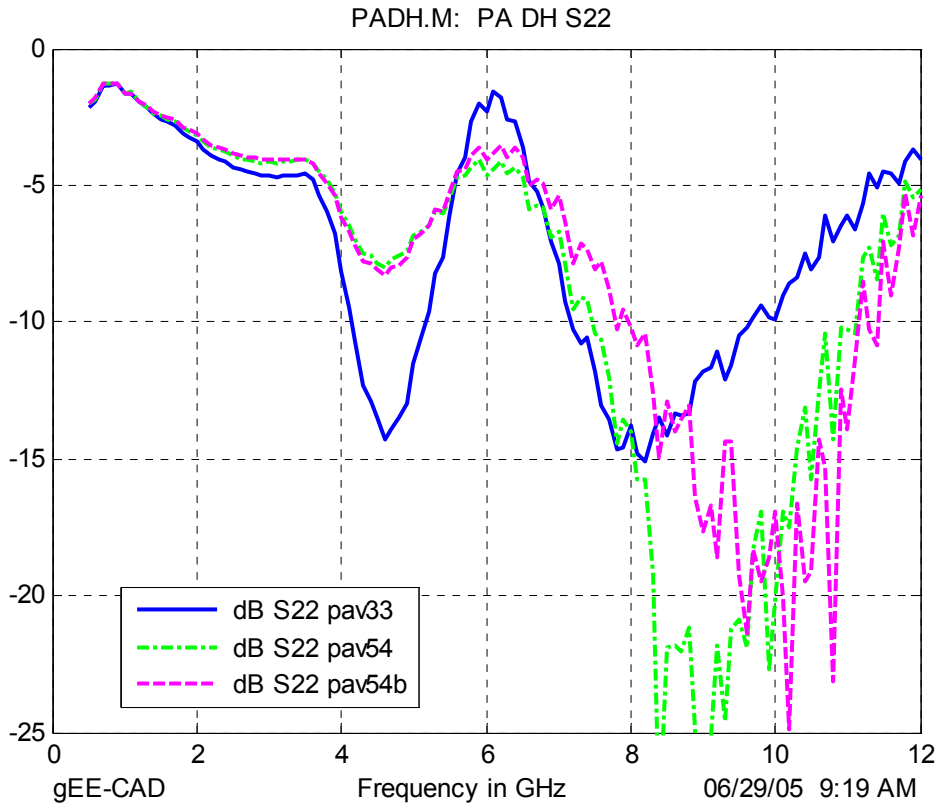
PA33 VD2 3V @ 50 mA VG2 = -0.70V, VD1 3V @ 22 mA VG1 = -0.70V Die #1
PA54 VD2 4V @ 54 mA VG2 = -0.70V, VD1 5V @ 30 mA VG1 = -0.25V Die #1
PA54B VD2 4V @ 61 mA VG2 = -0.70V, VD1 5V @ 25 mA VG1 = -0.57V Die #2





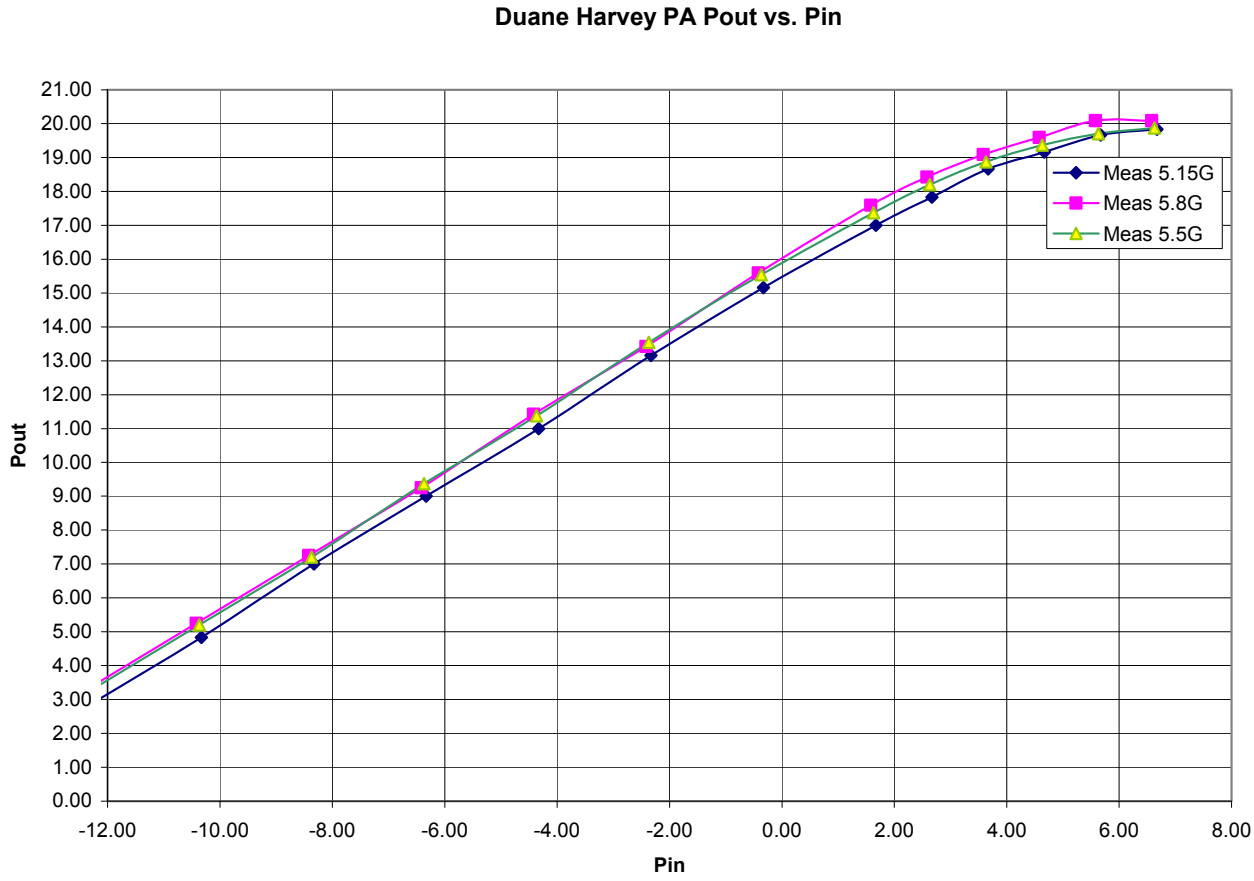
All S-parameters (top) and S21 (bottom) for Power Amp at various biases.

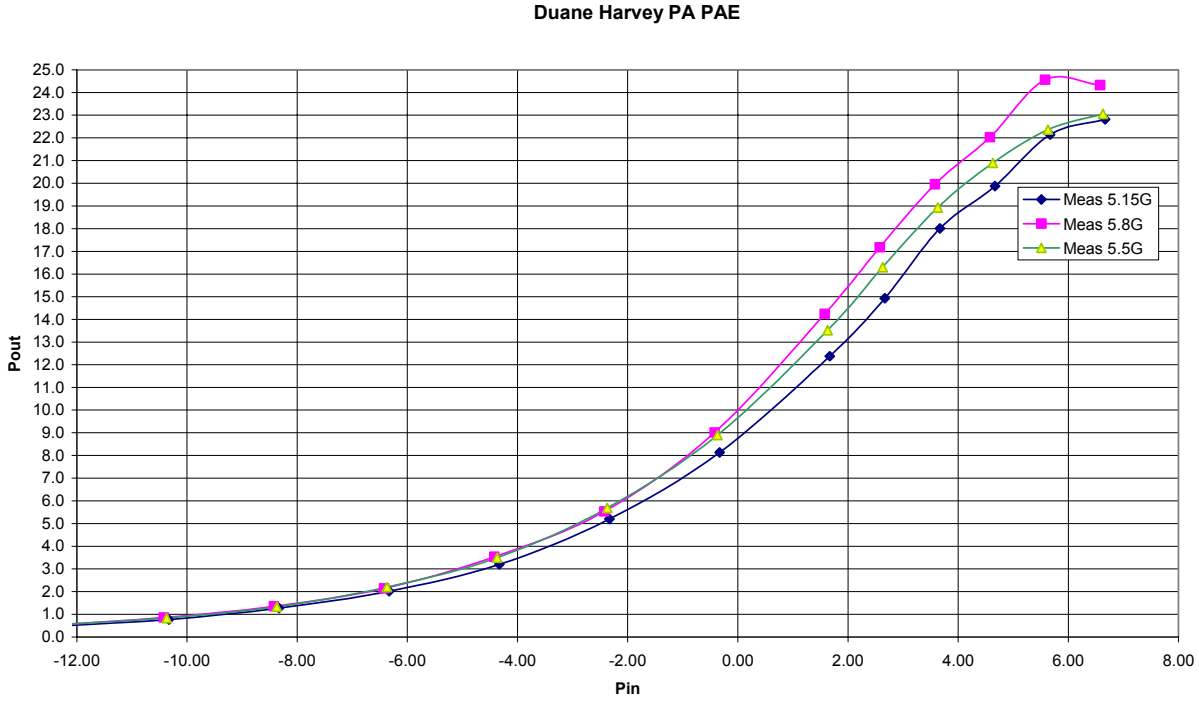




Input (top) and Output (bottom) Match for Power Amp at various biases.

Noted Some Low Frequency Oscillations during power output measurements. ~ 12-13 MHz and sensitive to big caps on gates. Occasionally clean but seemed to be low level oscillations most of the time. Die #2 VD2 4V @ 63 mA -0.7V and VD1 5V @ 26 mA -0.56 V





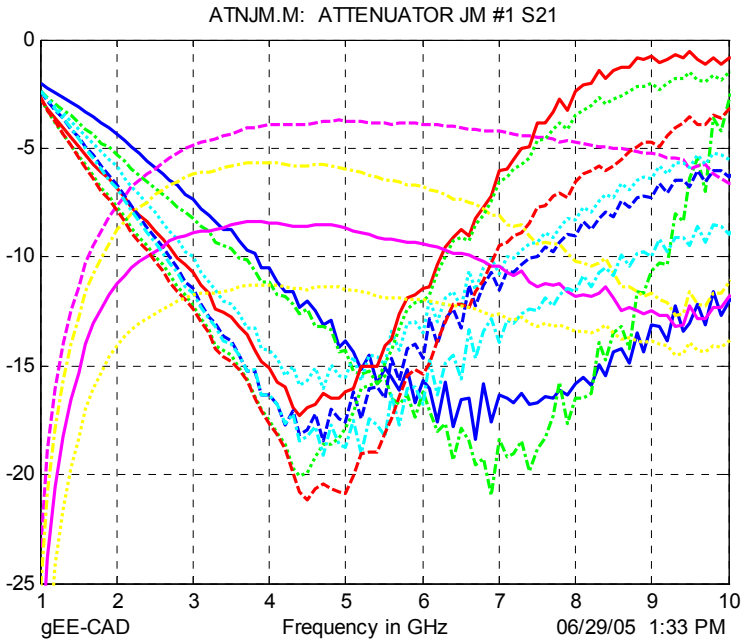
Power Out vs. Power In (top) and Power Added Efficiency (bottom) for Power Amp.

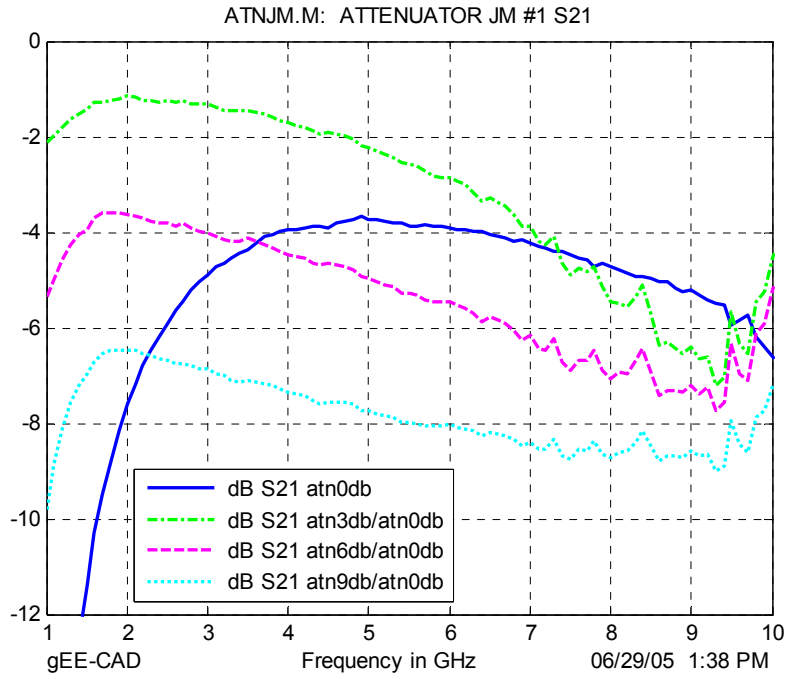
Jacob Morton Attenuator

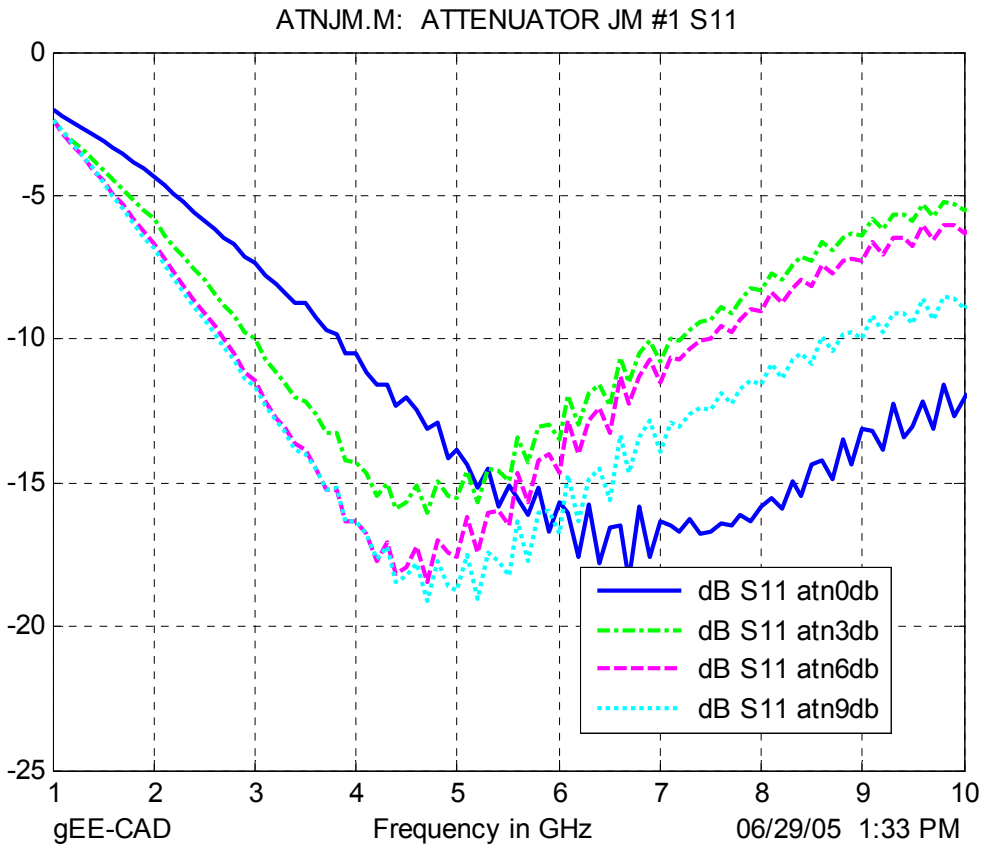
An attenuator MMIC was designed for the 5.15 to 5.35 GHz and 5.725 to 5.875 GHz WLAN and ISM bands. The design was intended to have an offset voltage so that CMOS or TTL drivers could be used to drive the switch inputs directly. As tested, one input pad was grounded and the other three were driven with -5V (off). Choices are 0 dB (nominal), 3 dB, 6 dB, and 9 dB attenuation relative to the low insertion loss state. The design as measured was close to expectations

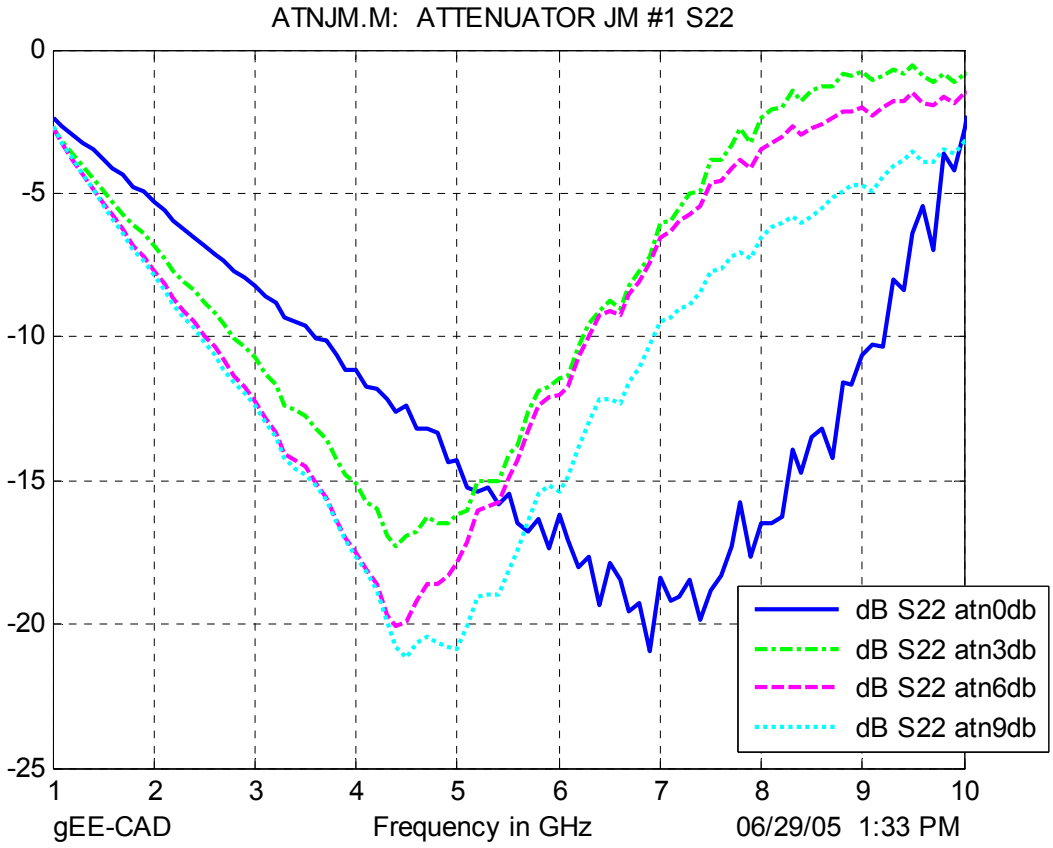
```
%Jacob Morton    6/29/05
% All inputs 0,3,6,9 at -5V except "one" for proper operation
% 0     3    6    9
% GND -5   -5   -5   -3.87 db at 5.5 G
% -5 GND   -5   -5   -6.48 db at 5.5 G
%   -5   -5 GND -5   -9.18 db at 5.5 G
%   -5   -5   -5 GND -11.87 db at 5.5 G
```

Plot of All S-parameters (top) and S21 (bottom Atn0 & 3/6/9 dB rel. attn







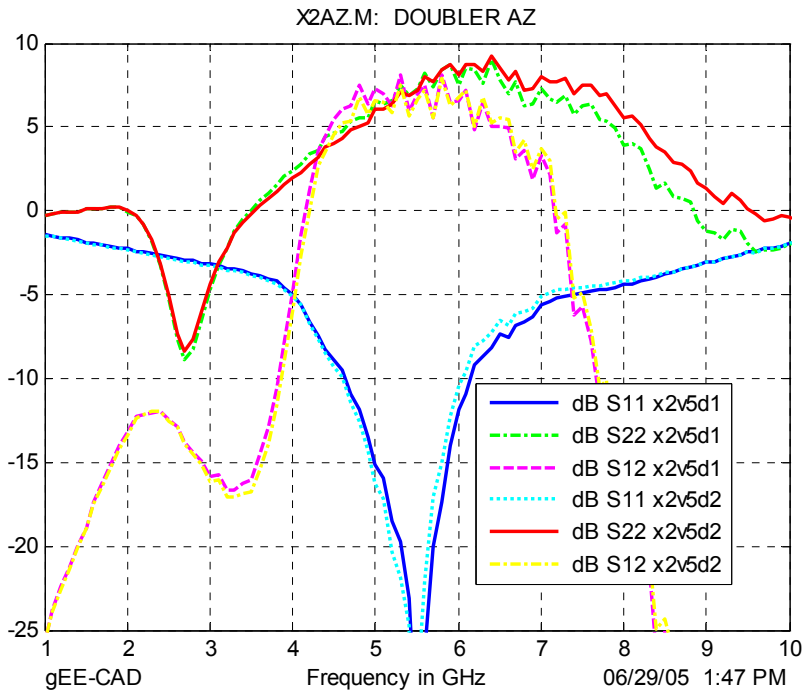


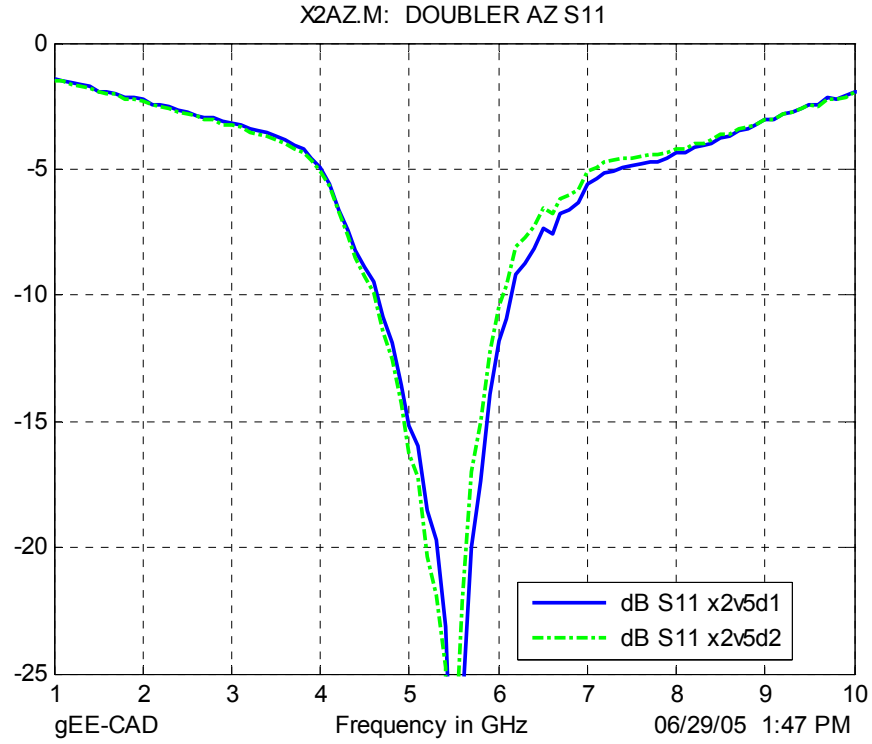
Match--S11 and S22 of Attenuator (-5V to all inputs except GND for 0, 3, 6, & 9 inputs)

Andrew Zundel Doubler

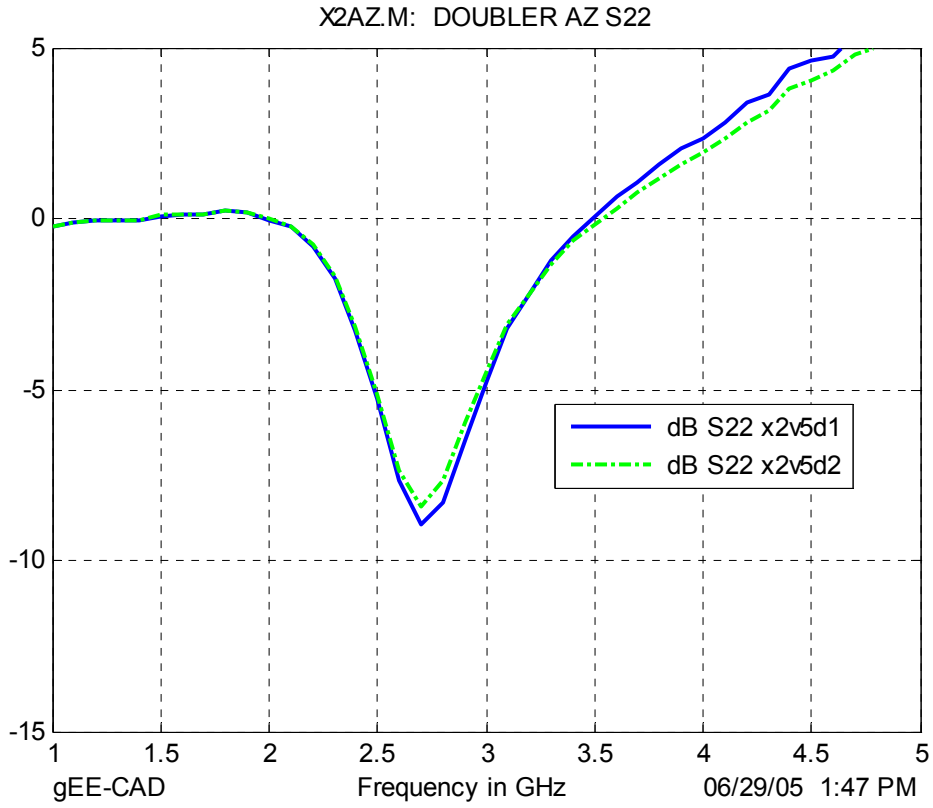
A frequency doubler was designed for an input frequency of 2.712 to 2.813 GHz providing 5.425 to 5.625 GHz at the doubled output. Conversion loss was measured to be 7 to 8 dB for a 2 to 10 dBm input signal. Small signal s-parameters were also recorded (see plots). Note that the MMIC was measured "backwards" meaning S11 is the lower frequency input and S22 is the output.

Die #1 5V @81-83 mA VG= -0.8V
Die #2 5V @66 mA VG= -0.8V
Note Port 1 is Output and Port 2 is Input as Measured! Note potential oscillations S22 at higher frequencies.

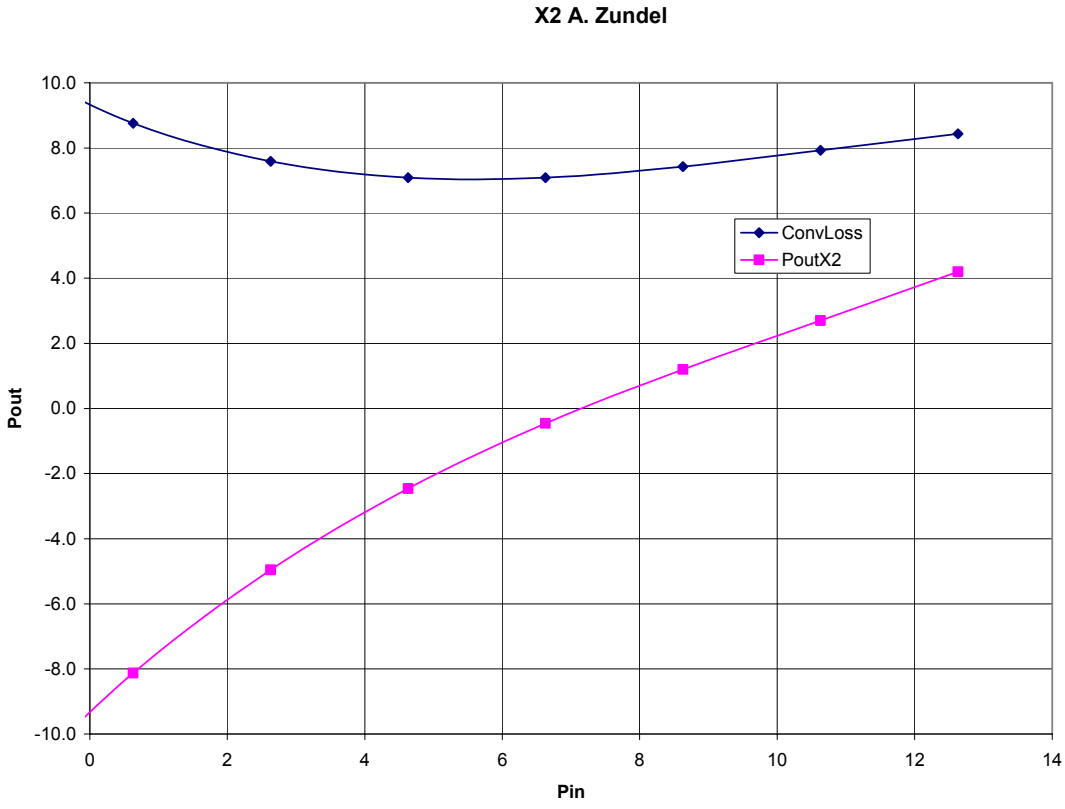




All S-parameters (top) and Output Match (bottom) for Freq. Doubler for two die



Input Match for Freq. Doubler for two die

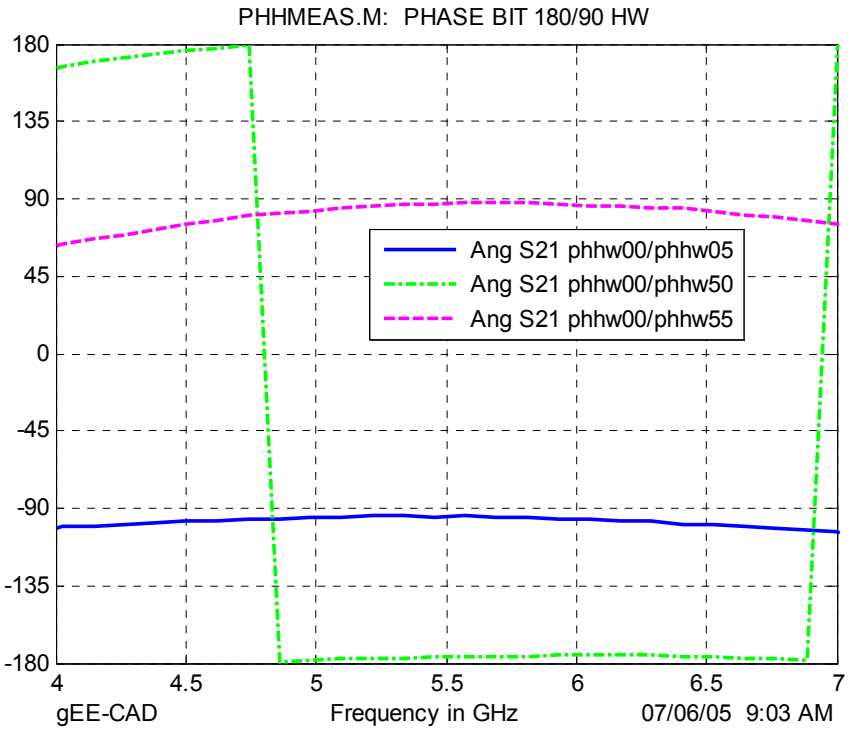


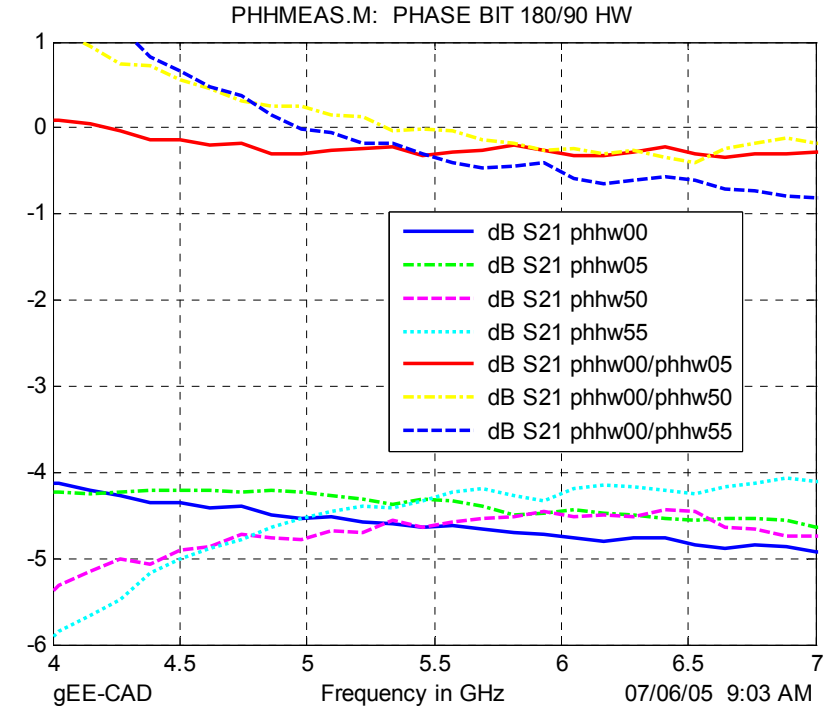
Conversion Loss about 7 dB at 4 to 8 dBm input. Pout (X2) and Conv Loss.

Henry Weiss Phase Shifter

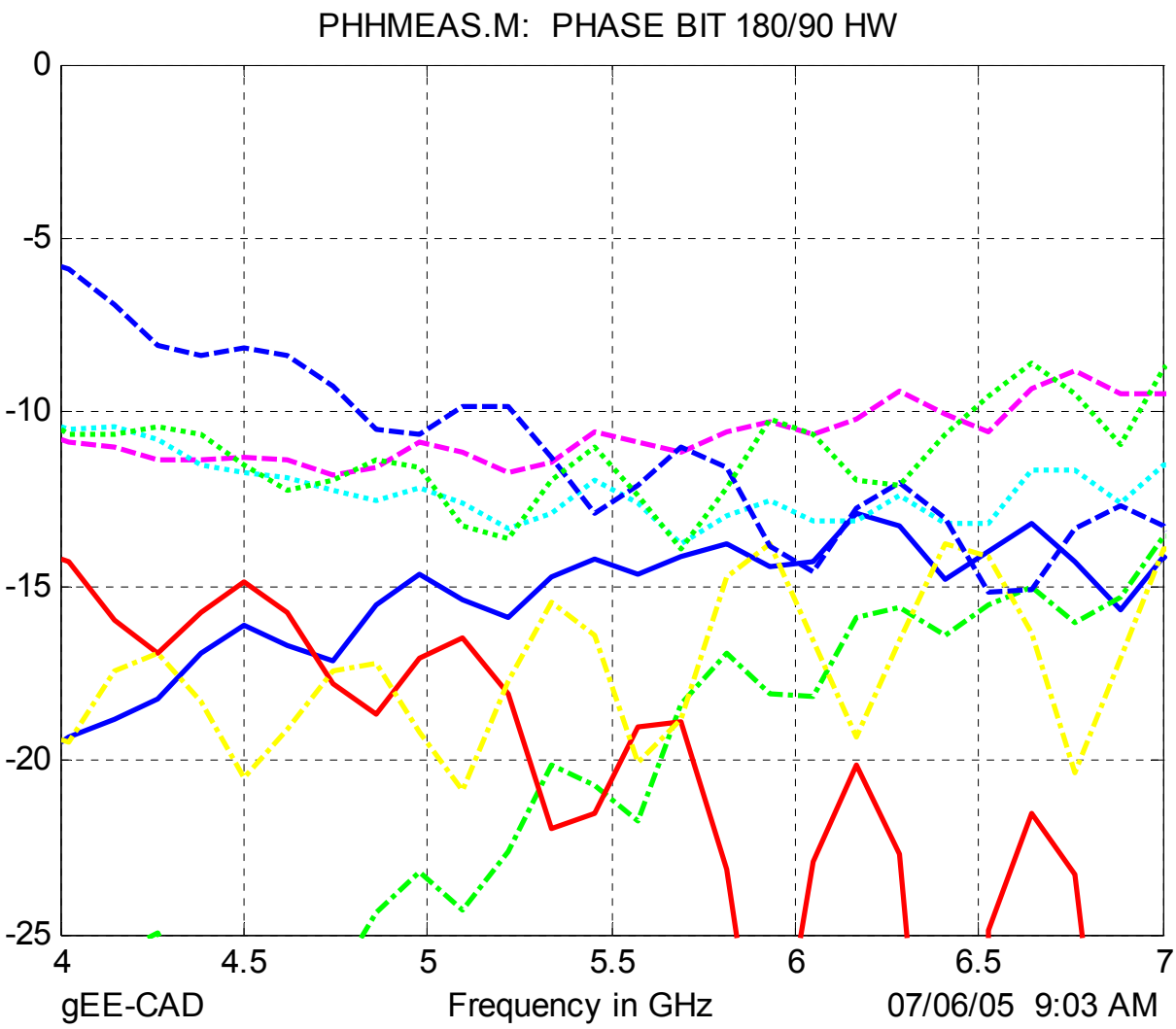
A C-Band Phase Shifter for the 5.15 to 5.35 GHz and 5.725 to 5.875 GHz WLAN and ISM bands was created. The design as measured was close to expectations for the two bit shifter. It was designed for 0V/-5V switch inputs with 0mA bias current.

Die #1 -5V and 0V for switches (< 1 mA)
Die #2 -5V and 0V for switches (< 1 mA)
Measured four phase states (00, 05, 50, 55) for two die and compared amplitude and phase differences. Good insertion balance 5-6 GHz and relative phases of 0, 90, 180, and 270 (within ~10 degrees).





Phase Difference and Amplitude Balance for the four phase states 0, 90, 180, & 270



Match S11/S22 over all four states of phase shifter. S11 is input to 180 bit and S22 is input to 90 bit.

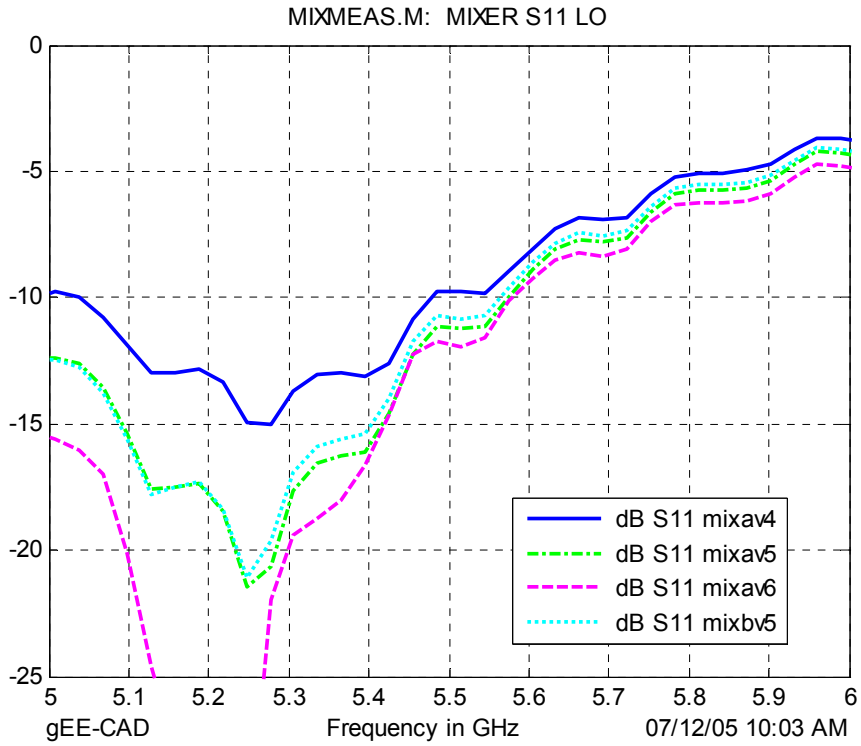
Jason Abrahamson Mixer

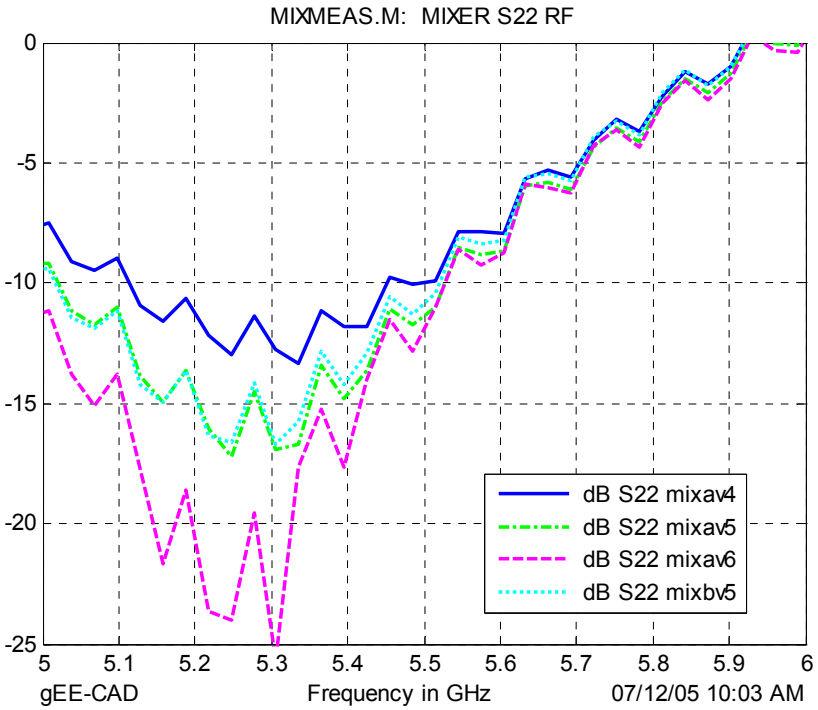
A Mixer was designed for the 5.15 to 5.35 GHz and 5.725 to 5.875 GHz WLAN and ISM bands with an IF of 275 MHz. The design worked well as an up converter or a down converter. While intended for an input bias to the diodes of 5V, it was also tested at 4V and 6V with good match and performance. S-parameters were only taken for the RF and LO ports—see plots.

Die #1 4, 5, & 6V at 2-3 mA

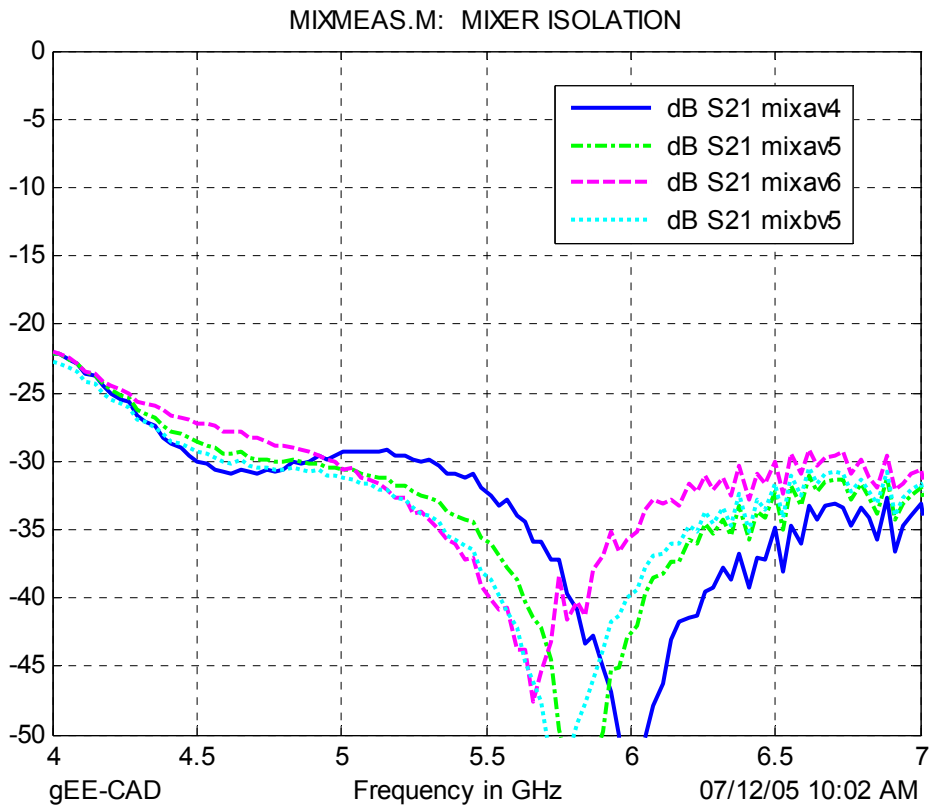
Die #2 5V at 2-3 mA

Measured LO (S11) and RF (S22) match and isolation. Then measured conversion loss up and down at band edges.





Match of LO (S11--top) and RF (S22—bottom)



Isolation of RF/LO (S21) at 4, 5, 6V of bias

Measured Mixer
Jason Abrahamson

5V at 2-3 mA

RF 5.15/5.875 GHz and IF 275 MHz -20 dBm setting
Measured 275 MHz IF into SA

Freq (GHz)	ThruLoss(both)	
5.15	3.68	1.84
5.43	3.78	1.89
5.60	3.82	1.91
5.88	3.95	1.975

1) LO 5.425 GHz
Down Conversion Low End 5.15 GHz

LO (SG)	LO (corr)	RF (corr)	IF (dBm)	Loss (gain)
-5	-6.89	-21.84	-31.3	-9.5
-3	-4.89	-21.84	-30.3	-8.5
-1	-2.89	-21.84	-29.7	-7.8
1	-0.89	-21.84	-29.5	-7.7
3	1.11	-21.84	-29.3	-7.5
5	3.11	-21.84	-29.0	-7.2
7	5.11	-21.84	-29.3	-7.5
9	7.11	-21.84	-29.0	-7.2

1) LO 5.425 GHz
Up Conv Low End 5.15 GHz

LO (SG)	LO (corr)	RF (corr)	RF (dBm)	Loss (gain)
-5	-6.89	-20	-32.7	-10.8
-3	-4.89	-20	-31.5	-9.7
-1	-2.89	-20	-31.0	-9.2
1	-0.89	-20	-30.7	-8.8
3	1.11	-20	-30.3	-8.5
5	3.11	-20	-30.3	-8.4
7	5.11	-20	-30.2	-8.3
9	7.11	-20	-30.2	-8.3

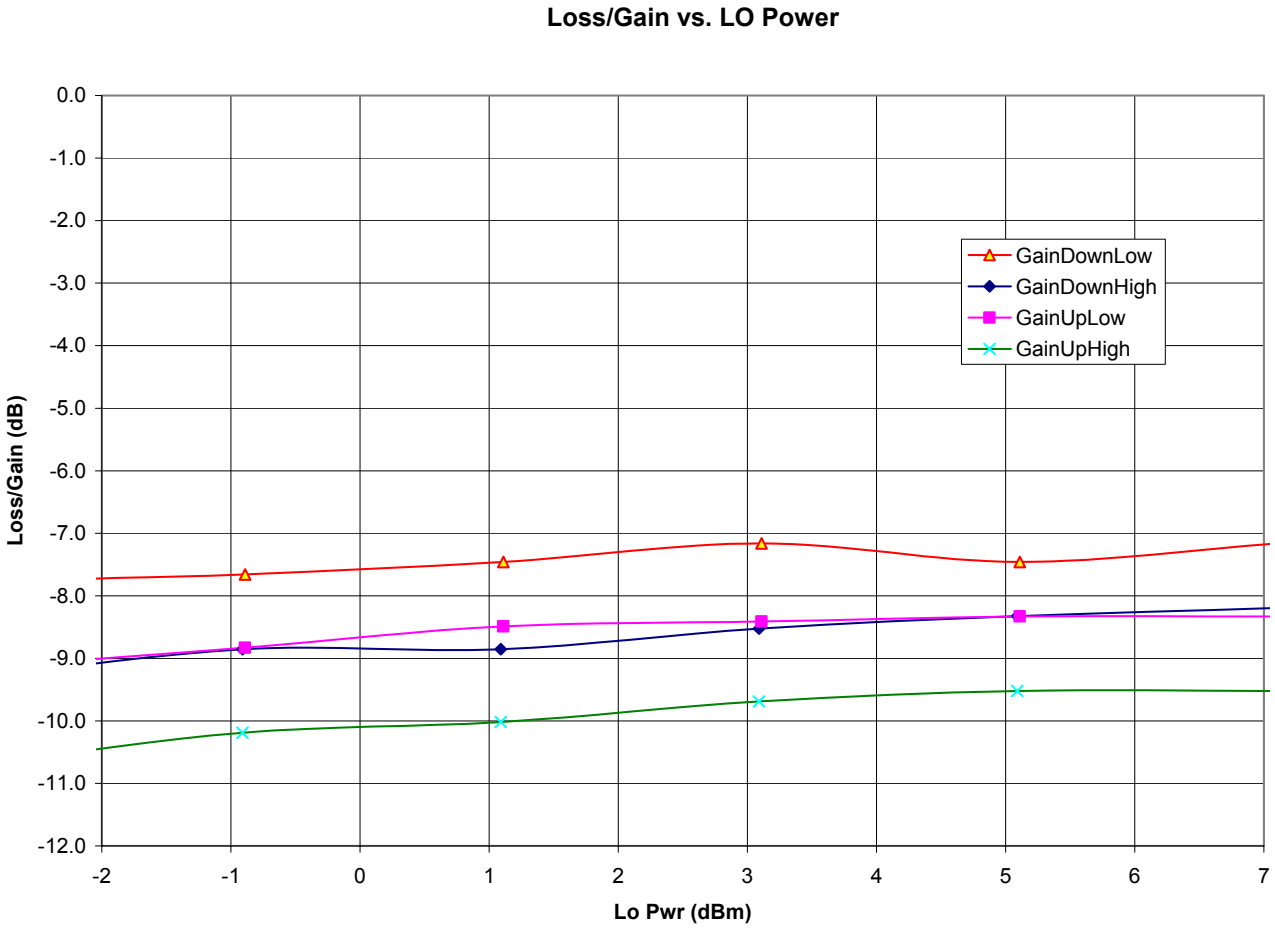
2) LO 5.6 GHz
Down Conversion High End 5.875 GHz

LO (SG)	LO (corr)	RF (corr)	IF (dBm)	Loss (gain)
-5	-6.91	-21.98	-33.0	-11.0
-3	-4.91	-21.98	-32.0	-10.0
-1	-2.91	-21.98	-31.3	-9.3
1	-0.91	-21.98	-30.8	-8.9
3	1.09	-21.98	-30.8	-8.9
5	3.09	-21.98	-30.5	-8.5
7	5.09	-21.98	-30.3	-8.3
9	7.09	-21.98	-30.2	-8.2

2) LO 5.6 GHz
Up Conv High End 5.875 GHz

LO (SG)	LO (corr)	RF (corr)	RF (dBm)	Loss (gain)
-5	-6.91	-20	-34.3	-12.3
-3	-4.91	-20	-33.2	-11.2
-1	-2.91	-20	-32.7	-10.7
1	-0.91	-20	-32.2	-10.2
3	1.09	-20	-32.0	-10.0
5	3.09	-20	-31.7	-9.7
7	5.09	-20	-31.5	-9.5
9	7.09	-20	-31.5	-9.5

Excel Spreadsheet Data of Mixer Performance

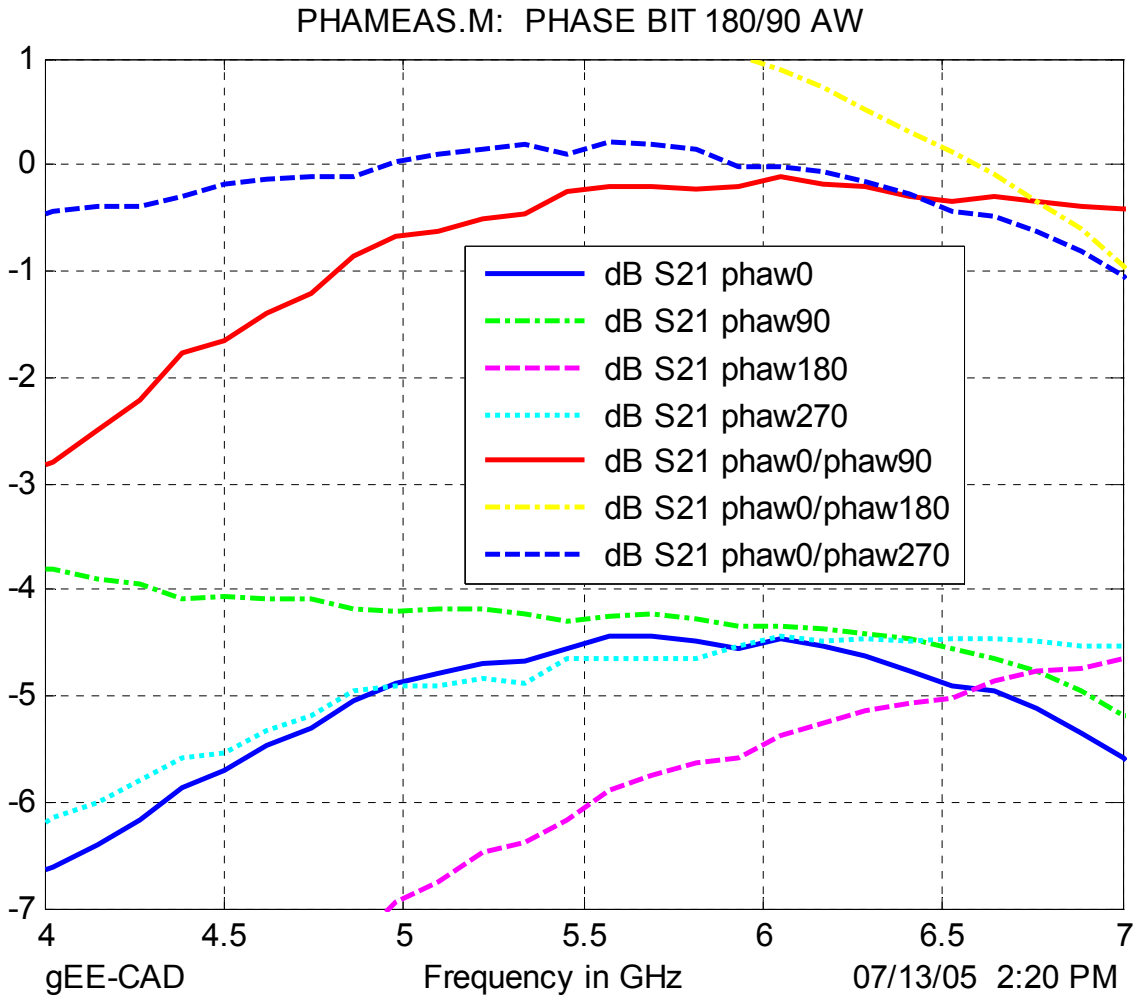


Plot of Conversion Loss UP/Down at Band Edges 5.15 to 5.875 GHz

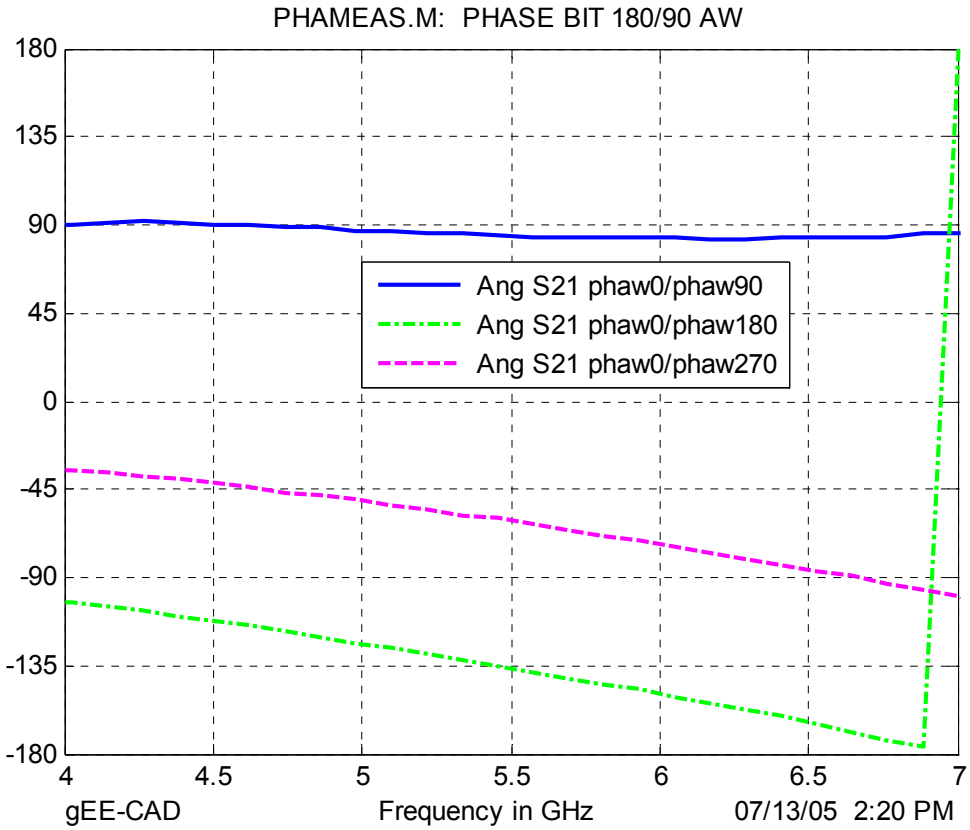
Andrew Walters & Kevin Shaffer Phase Shifter

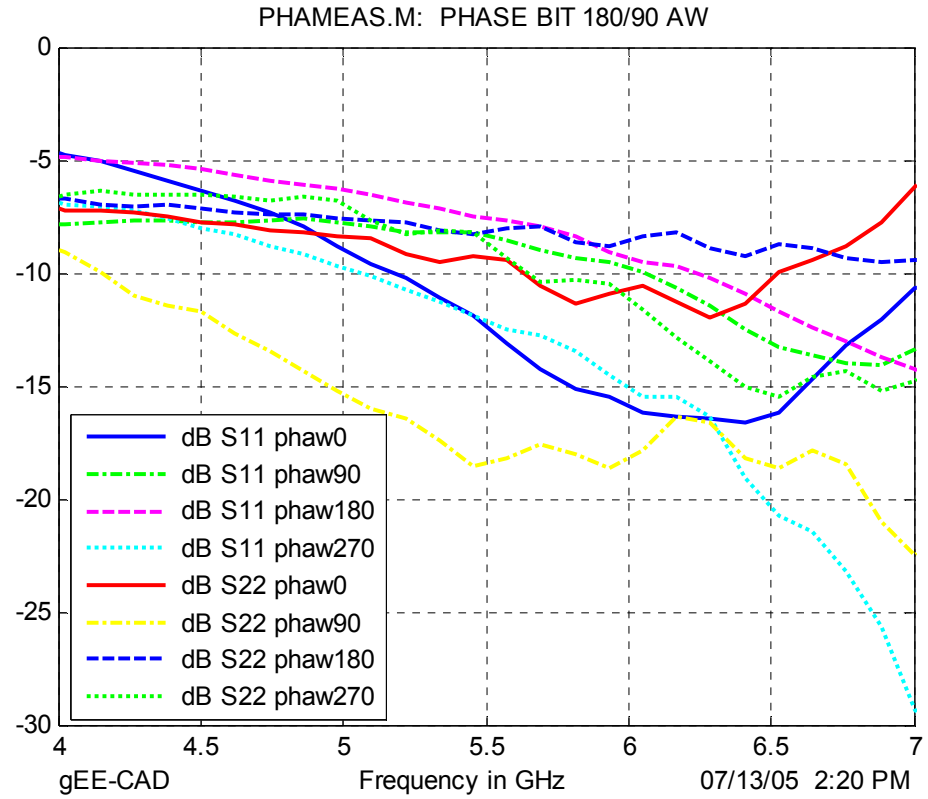
A parallel design of a C-Band Phase Shifter for the 5.15 to 5.35 GHz and 5.725 to 5.875 GHz WLAN and ISM bands was created. The design had a layout error in the 180 degree bit of the two bit shifter. As measured the 90 degree bit worked as expected but the layout error in the 180 bit caused it to be about 135 degrees. It was designed for 0V/-5V switch inputs with 0mA bias current.

Die #1 -5V and 0V for switches (0 mA)
Die #2 -5V and 0V for switches (0 mA)
Measured four phase states (0, 90, 180, 270) for two die and compared amplitude and phase differences. Higher insertion loss for one of four states and match was OK.



Amplitude Balance and insertion loss (S21) for Phase Shifter





Phase Difference (top) and Match (bottom) for Phase Shifter

The 90 degree bit is pretty close in phase, but the 180 bit appears to be about 135 degrees. Insertion loss is balanced pretty well for the 0, 90, and 270 states but is 1-2 dB higher for the 180 state.

Dontae Ryan & Ade George Voltage Controlled Oscillator (VCO)

A VCO was designed for 2.712 to 2.812 GHz output. The final design as measured had about the correct range (100 MHz) but was a bit low in frequency (~2.55 to 2.65 GHz). The design oscillated over an input range to the VCO of -0.4 to 0.7 V and then stopped oscillating for voltages > 0.8V. It has a large DC power consumption to provide the desired 10 dBm of output power but the 2nd and 3rd harmonics are quite low. Data was also measured at 4V and 3V but the design operated best at the intended bias of 5V/136 mA.

Measured ADS VCOs
Dontae Ryan & Ade George Designers

AWR VCO similar to ADS design but could not be simulated with AWR. Layout only.
Loss of output cables and probe estimated to ~1.3 dB X1, 1.8 dB X2, 2.3 dB X3. Add to Pout(measured).

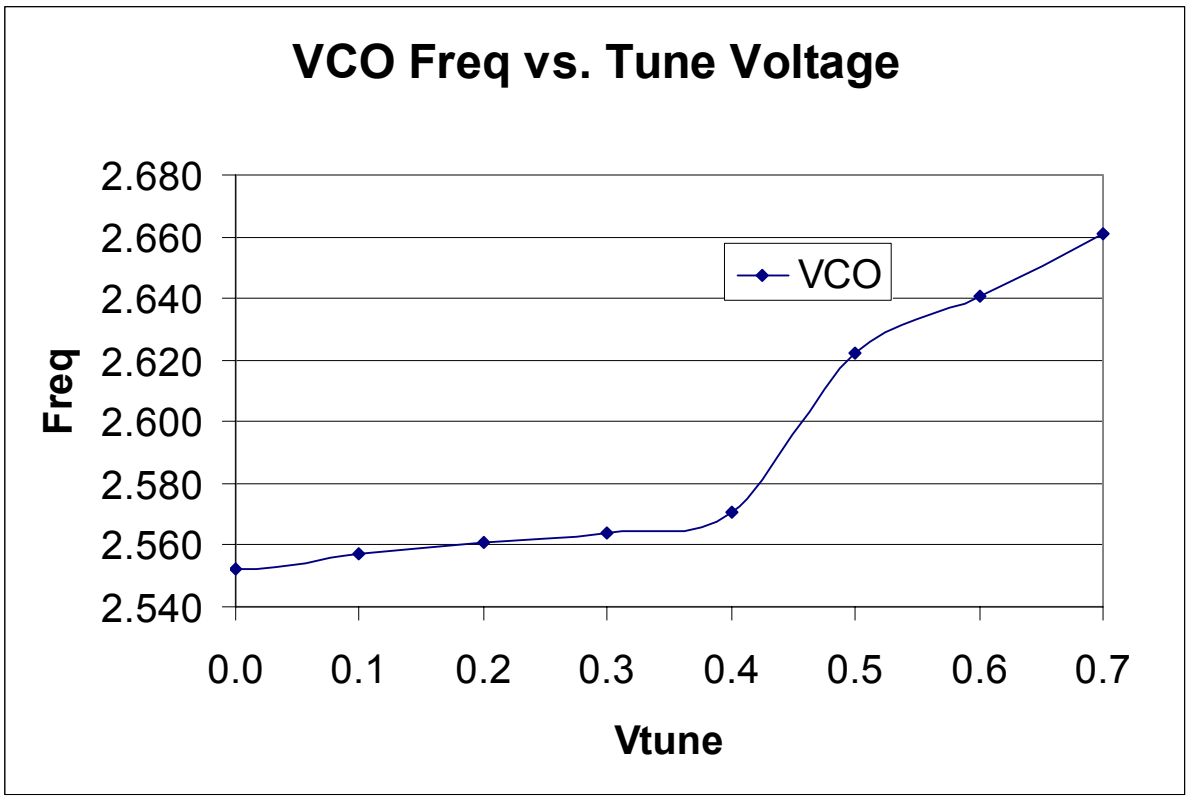
Note: Harmonics	
X2	"-35.6 dBc"
X3	"-54.2 dBc"

ADS VCO 5V at 136mA					
VBias (V)	**Freq (GHz**	**Pout(ms)**	**Pout(corr)**	**X2 Pout(ms)**	**X3 Pout(ms)**
-0.4	2.552	9.0	**10.3**		
-0.2	2.557	9.5	**10.8**		
0.0	2.552	9.0	**10.3**	-27.1	-46.2
0.1	2.557	9.5	**10.8**		
0.2	2.561	9.5	**10.8**		
0.3	2.564	9.5	**10.8**		
0.4	2.571	9.5	**10.8**		
0.5	2.622	6.2	7.5		
0.6	2.641	6.3	7.6		
0.7	2.661	5.2	6.5		
0.8	NO	NO			
Range:	0.109				
Center:	2.607				

ADS VCO 4V at 121mA		
VBias (V)	**Freq (GHz**	**Pout(ms)**
0	2.502	6.17
0.2	2.508	5.67
0.4	2.543	4.83

ADS VCO 3V at 111mA		
VBias (V)	**Freq (GHz**	**Pout(ms)**
-0.4	2.420	-1.67
-0.2	2.428	-1.00
0	2.442	-2.33
0.2	2.490	-3.50
0.4	2.545	-5.83
0.6	2.582	-8.00

Design Goal: 2.712 to 2.812 GHz



Oscillator Frequency Vs. Tuning Voltage

Class Design Examples: Low Noise Amplifier and Power Amplifier (4 GHz) by John Penn

During the course the students are shown a design example of a low noise amplifier and a medium power amplifier at 4 GHz. In 2003 a layout was completed for each design in ADS and both were combined on a single 60 x 60 mil die (54 x 54 after dicing). This year (2004), the same designs were re-layed out using Microwave Office and fabricated. Measured data was taken of the two designs and plotted. The results are similar to last year's fabrications. For future JHU MMIC Design classes, these design examples will show measured data compared to simulations with ADS. Note the similarities between the two different fabrications with measured data from the ADS layout (lna4jp) and measured from the MWO layout (lna4mw) vs. the original ADS simulations (lna4adsl). There are also some comparisons to a generic simulator. For the Power Amp, only the measured data for the ADS layout of 03 (pa4jpv4) and the MWO layout of 04 (pa4mwv4) are shown. There are some tiny differences in the circuit layout between ADS and MWO but they do not seem significant. There does appear to be less gain in the LNA & PA from the 04 fabrication but that may normal process variation and/or measurement/bias errors.

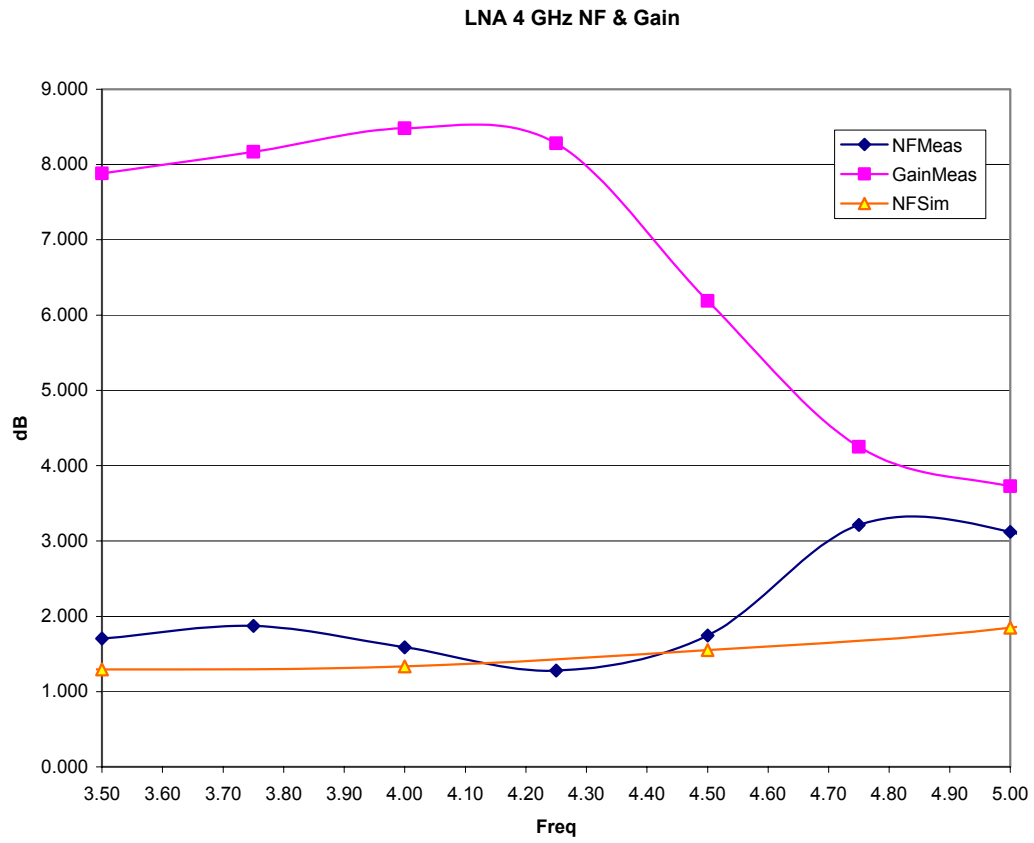
Meas. PA 4 GHz Pout vs. Pin 5V at 51 mA VGS=-0.55\ 6/16/2005
Loss 2.17 dB at 4.0 GHz on input and output

4.0 GHz Pin(SG)	Die#1 Pout(SA)	PA4 Pin(corr)	Pout(corr)	Gain	I(5V)	Corrected PDC(mw)	Pout(mw)	Drn Eff	PAE	Pin(Sim)	Pout(Sim)
-20.0	-15.17	-22.17	-13.00	9.17	51	255	0.05	0.0	0.0		
-10.0	-5.17	-12.17	-3.00	9.17	51	255	0.50	0.2	0.2		
0.0	4.83	-2.17	7.00	9.17	51	255	5.01	2.0	1.7		
2.0	6.83	-0.17	9.00	9.17	51	255	7.94	3.1	2.7		
4.0	8.83	1.83	11.00	9.17	51	255	12.59	4.9	4.3		
6.0	11.00	3.83	13.17	9.34	50	250	20.75	8.3	7.3	0	11.871
8.0	12.83	5.83	15.00	9.17	50	250	31.62	12.6	11.1	2	13.875
9.0	13.83	6.83	16.00	9.17	50	250	39.81	15.9	14.0	4	15.879
10.0	14.67	7.83	16.84	9.01	50	250	48.31	19.3	16.9	6	17.868
11.0	15.33	8.83	17.50	8.67	50	250	56.23	22.5	19.4	8	19.697
12.0	16.00	9.83	18.17	8.34	51	255	65.61	25.7	22.0	10	20.644
13.0	16.50	10.83	18.67	7.84	51	255	73.62	28.9	24.1	12	21.175
14.0	16.67	11.83	18.84	7.01	51	255	76.56	30.0	24.0		
15.0	17.00	12.83	19.17	6.34	51	255	82.60	32.4	24.9		

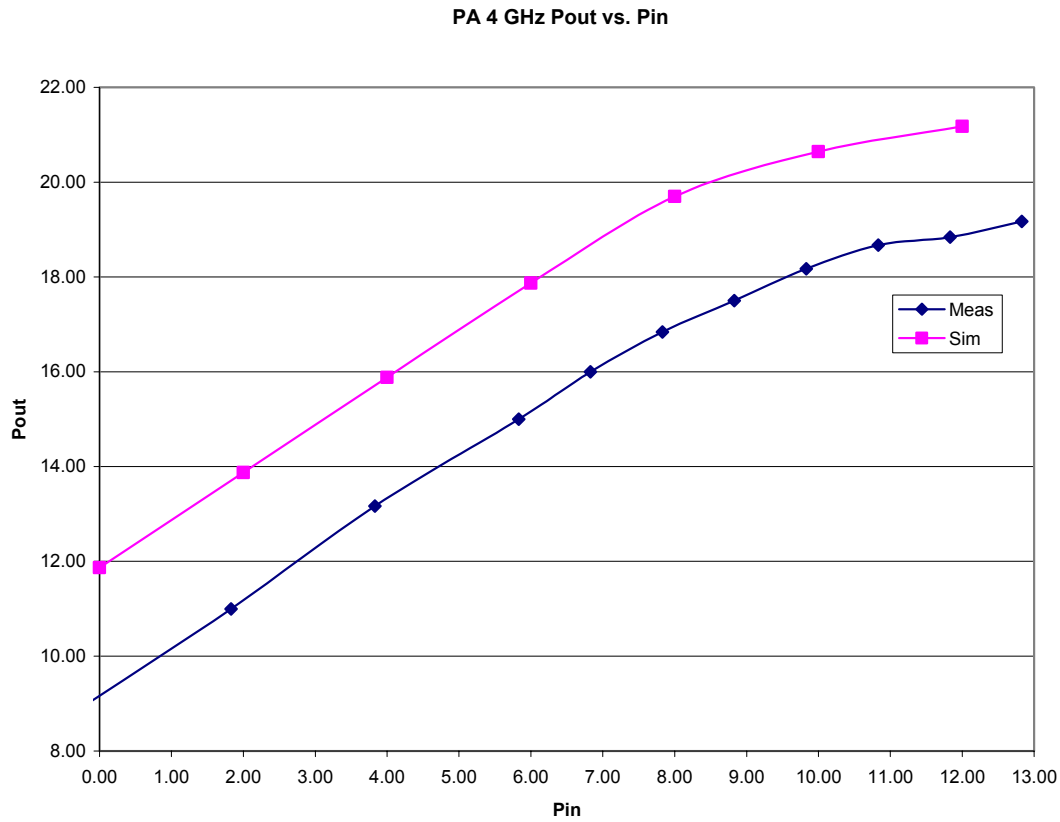
Microwave Office Version Fall 04 4V ~0.01A VGS=-0.1V 6/14/2005

LNA4 Freq(Ghz)	NF	Gain	Thru Freq(Ghz)	LossThru2	X(Gain)	NF(approx)	Gain	NF Corr	NF(dB)	NF(Sim)	NF Meter A NF Thru
3.50	3.12	5.58	3.50	2.30	0.767	1.574	7.88	0.094	1.703	1.901	
3.75	3.43	5.60	3.75	2.57	0.744	1.639	8.17	0.100	1.872	1.769	
4.00	4.29	3.95	4.00	4.53	0.594	1.594	8.48	0.153	1.586	1.622	
4.25	4.15	3.53	4.25	4.75	0.579	1.505	8.28	0.162	1.279	1.478	
4.50	4.04	2.53	4.50	3.66	0.656	1.663	6.19	0.169	1.746	1.357	
4.75	4.92	1.50	4.75	2.75	0.729	2.262	4.25	0.166	3.213	1.295	
5.00	4.75	1.15	5.00	2.58	0.743	2.218	3.73	0.167	3.120	1.334	
5.25	4.93	-0.62	5.25	4.07	0.626	1.948	3.45	0.251	2.295	1.55	
5.50	6.24	-0.91	5.50	5.11	0.555	2.336	4.20	0.274	3.143	1.85	
5.75	7.83	-3.00	5.75	5.59	0.525	3.188	2.59	0.352	4.527	2.5	
6.00	6.34	-2.46	6.00	4.23	0.614	2.645	1.77	0.314	3.675	3.1	
6.25	8.02	-4.52	6.25	4.56	0.592	3.750	0.04	0.407	5.242		
6.50	8.25	-3.90	6.50	4.89	0.570	3.806	0.99	0.384	5.343		
6.75	8.65	-5.73	6.75	4.95	0.566	4.145	-0.78	0.475	5.646		
7.00	9.71	-6.60	7.00	5.01	0.562	5.254	-1.59	0.526	6.747		
7.25	11.49	-7.65	7.25	4.98	0.564	7.948	-2.68	0.593	8.666		
7.50	10.69	-8.16	7.50	4.94	0.566	6.637	-3.22	0.628	7.788		
7.75	11.16	-9.18	7.75	5.51	0.531	6.930	-3.68	0.717	7.933		
8.00	12.37	-8.72	8.00	6.07	0.497	8.580	-2.65	0.682	8.975		

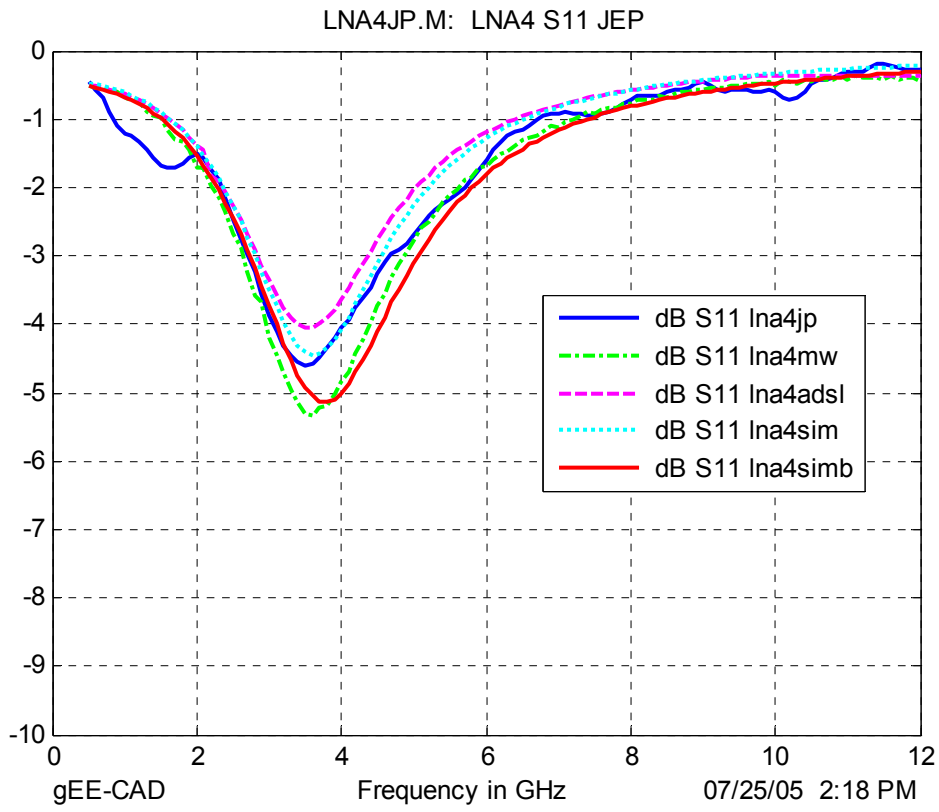
EXCEL data of 4 GHz Power Amp and Low Noise Amp



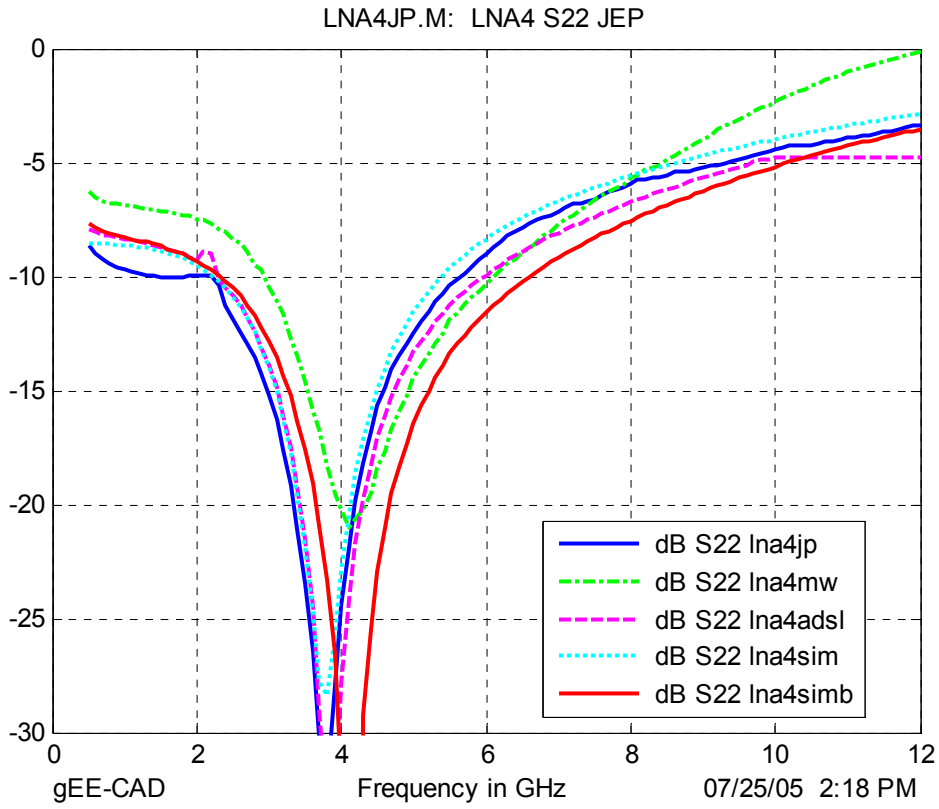
Plot of Gain and Noise Figure vs. Simulated NF of 4 GHz LNA.



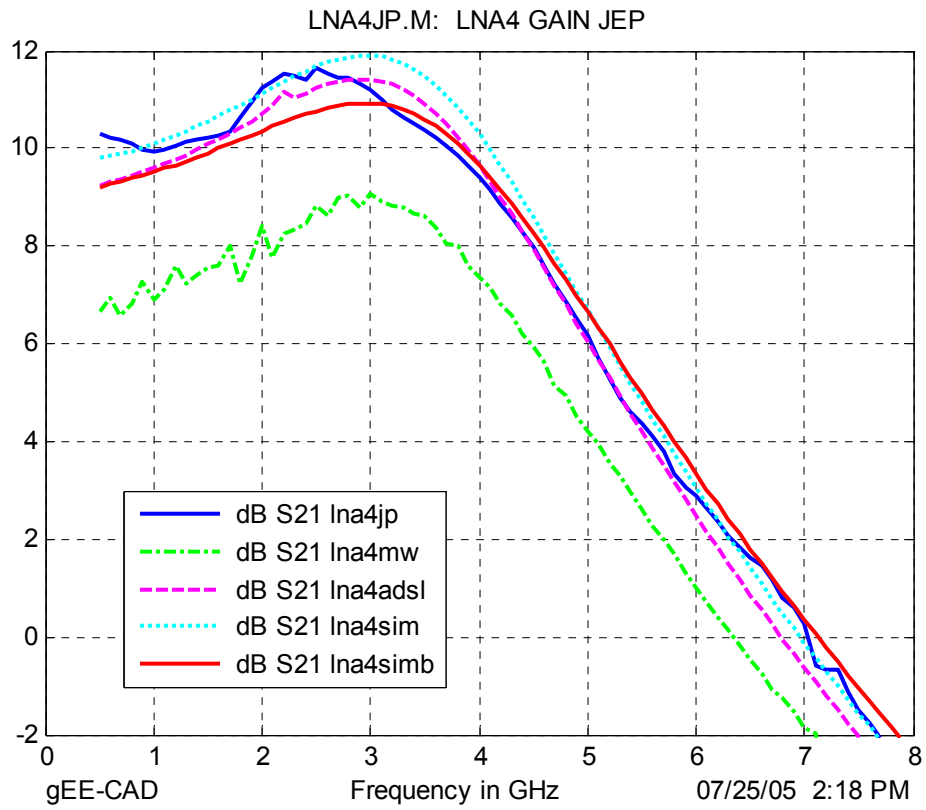
Plot of Power Out vs. Power In—Measured and Simulated 4 GHz PA.



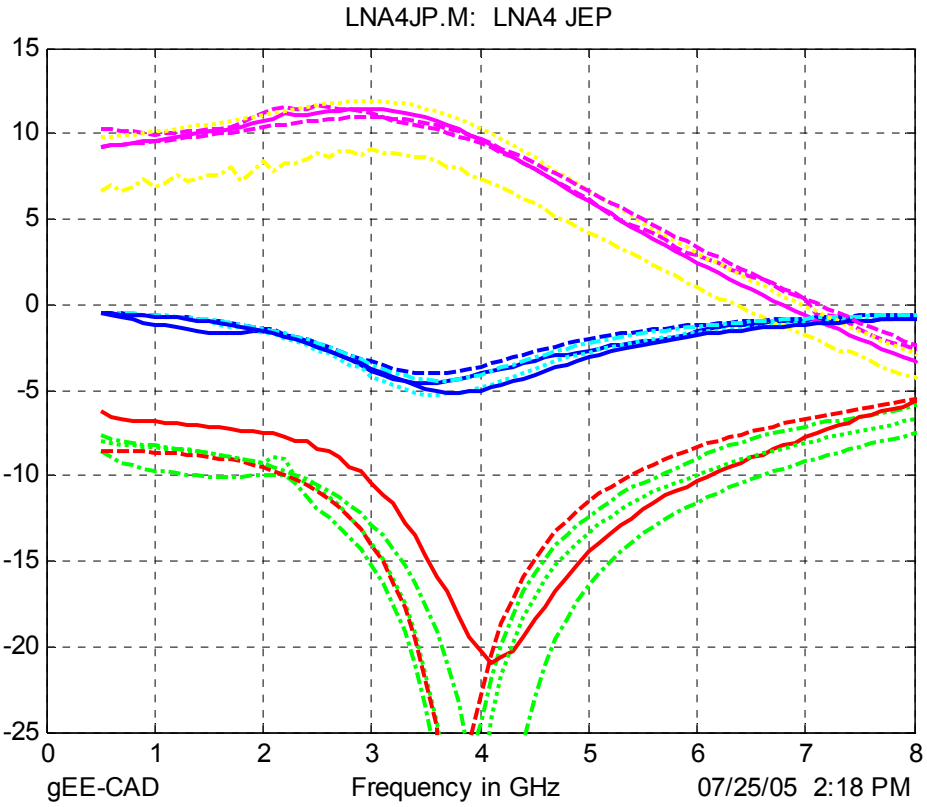
Input Match LNA—lna4jp (03 ADS), lna4mw (04 MWO), lna4adsl (03 ADS Simulation)



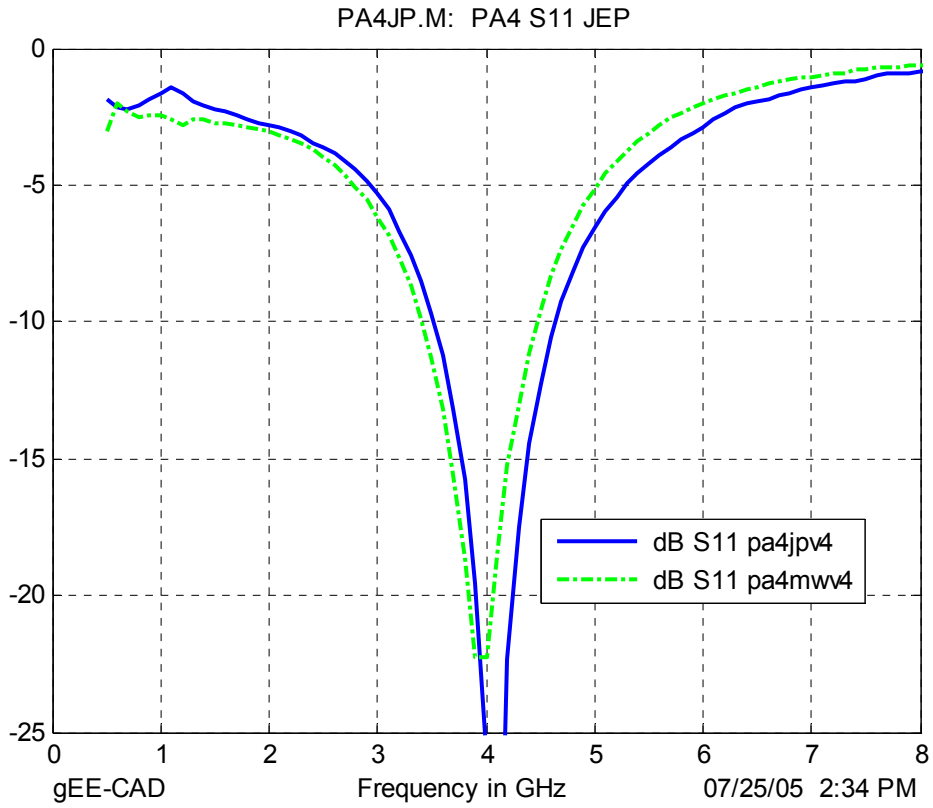
Output Match LNA—lna4jp (03 ADS), lna4mw (04 MWO), lna4adsl (03 ADS Simulation)



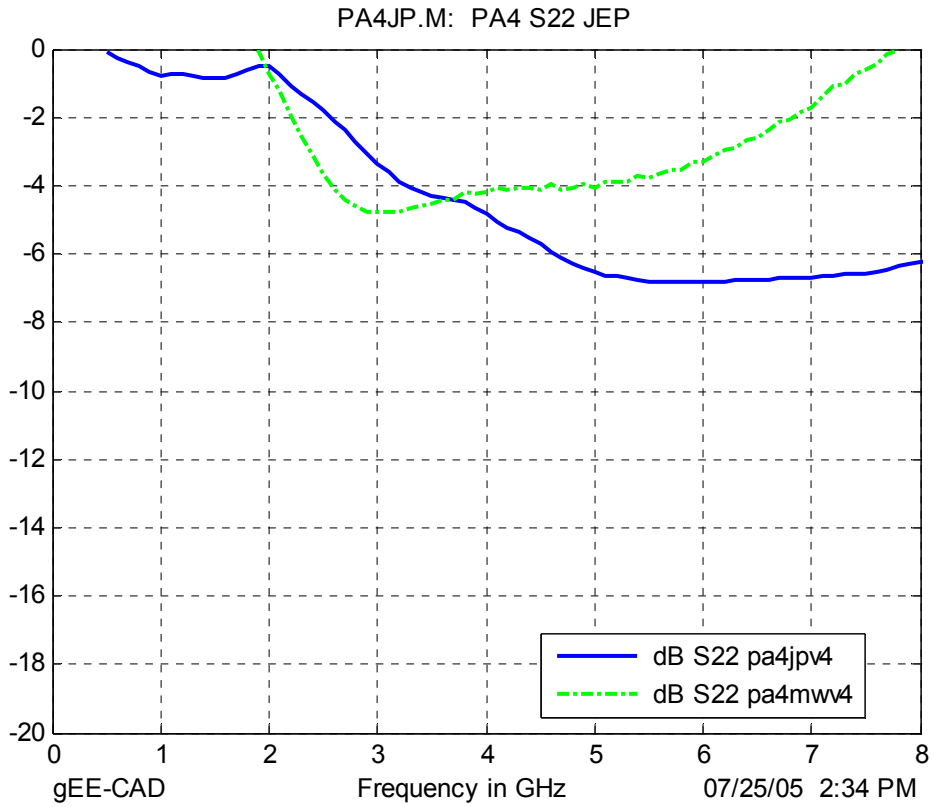
Gain (S21) LNA—lna4jp (03 ADS), lna4mw (04 MWO), lna4adsl (03 ADS Simulation)



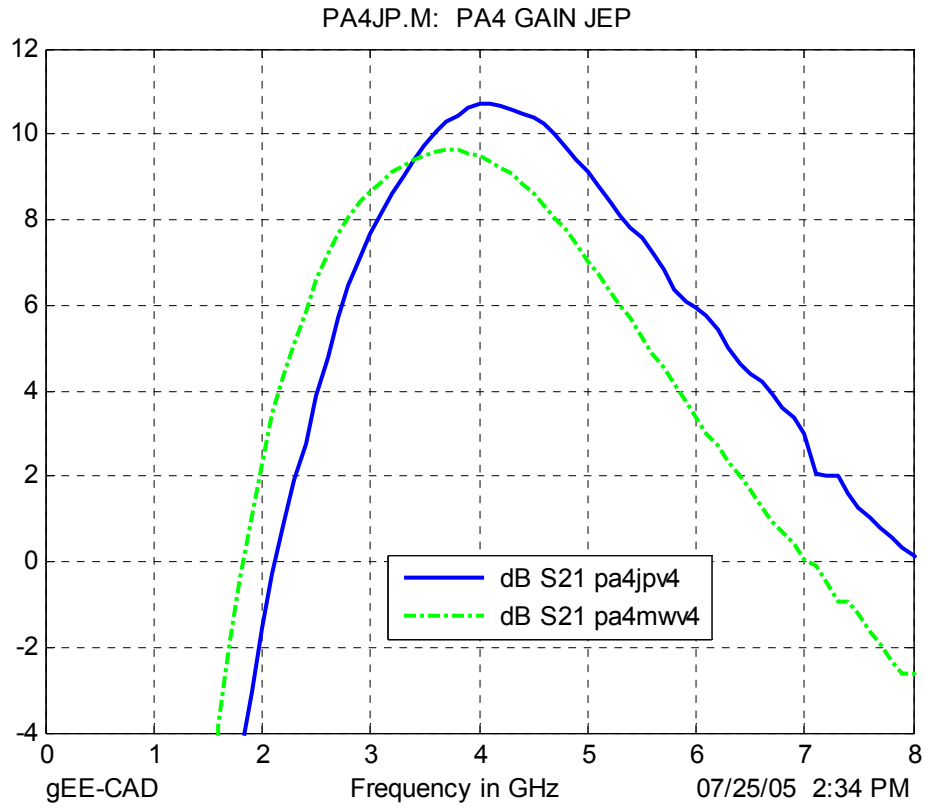
All S-Parameters LNA—lna4jp (03 ADS), lna4mw (04 MWO), lna4adsl (03 ADS Simulation)



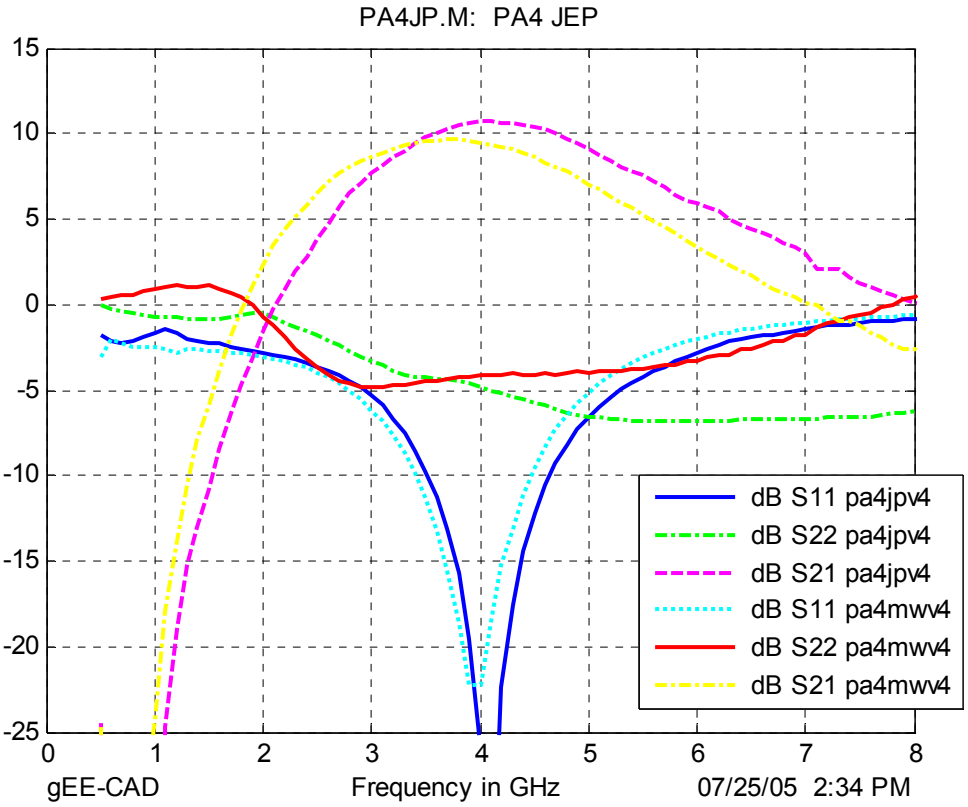
Input Match PA—pa4jv4p (03 ADS), pa4mwv4 (04 MWO)



Output Match PA—pa4jv4p (03 ADS), pa4mwv4 (04 MWO)



Gain (S21) PA—pa4jv4p (03 ADS), pa4mwv4 (04 MWO)



All S-Parameters PA—pa4jv4p (03 ADS), pa4mwv4 (04 MWO)