JHU EE787 Fall 2006 MMIC Results

Dr. Michel Reece and Prof. John Penn

Designs Fabricated by TriQuint Semiconductor

ADS Support by Gary Wray—Agilent

TriQuint TQPED Library, and ADS software used for student designs

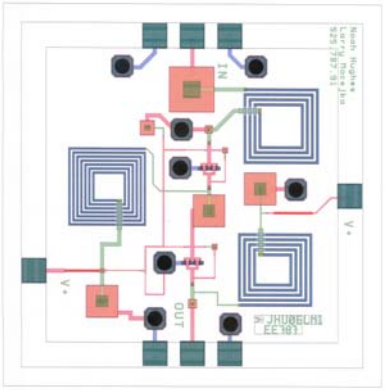
Eight MMICs were designed by students for the Fall 2006 JHU MMIC Design Course as part of a duplex transceiver employing a receive array for the S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies. All designs were tested in the Summer of 2006 after fabrication by TriQuint Semiconductor. The MMIC measurements compare favorably to simulations; overall, the designs were very successful. All designs used TriQuint's TQPED process with 0.5 um PHEMTs. Almost all the designs worked reasonably well and are documented following. The vector modulator MMIC was the first to be tested and it worked very well. Overall, DC biases and small signal parameters were close to simulations. Output powers tended to be several dB below predictions for the amplifier designs.

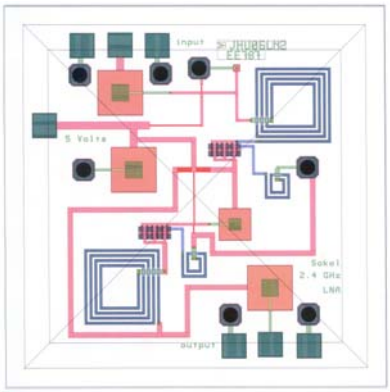
Thanks again to TriQuint, and Agilent for their wonderful support of the JHU EE787 MMIC Design Course.

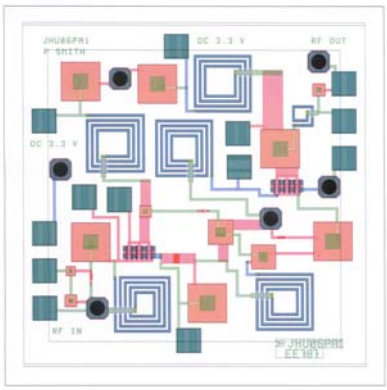
Fall 2006 JHU EE787 MMIC Design Student Projects
Supported by TriQuint, and Agilent Eesof
Professors John Penn and Dr. Michel Reece

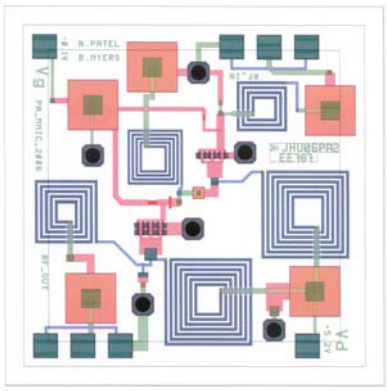
Low Noise Amplifier 1 (Low Power)–N. Hughes & L. Macejka
Phase Shifter – Dave Wendland
Power Amplifier 2 – Ben Myers & Niral Patel
Voltage Controlled Osc. – Dimitrios Loizos

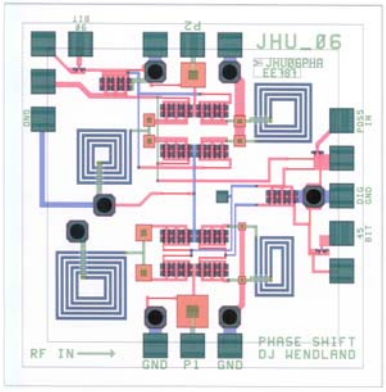
Low Noise Amplifier 2– Dave Sokol
Small Signal Amp – C. Wedderburn
Power Amplifier 1 – Peter Smith
Vector Modulator – Jonathan Egan

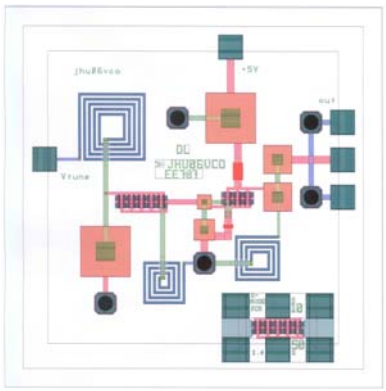


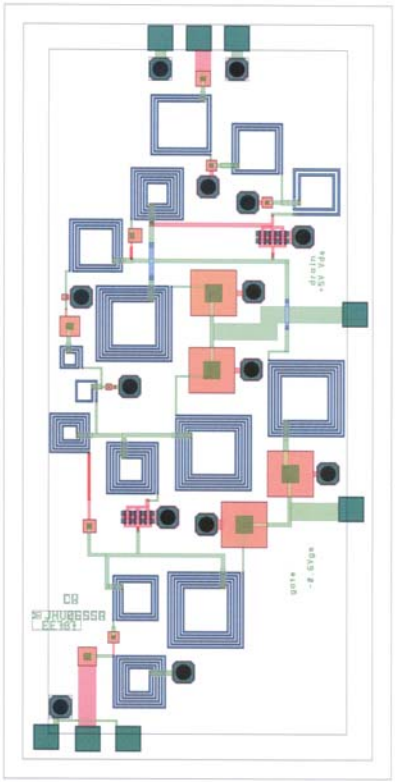


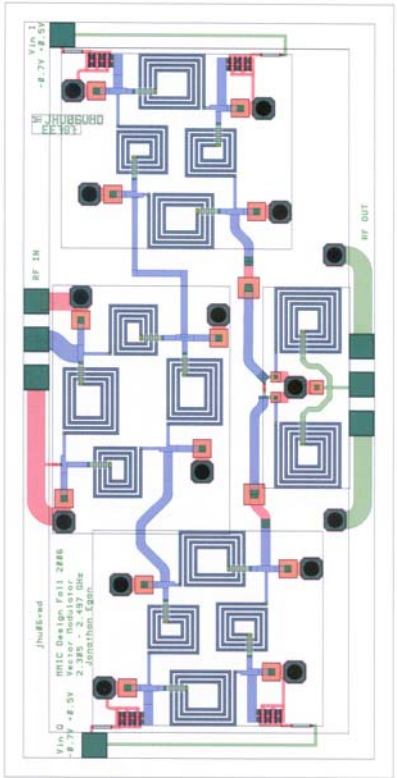






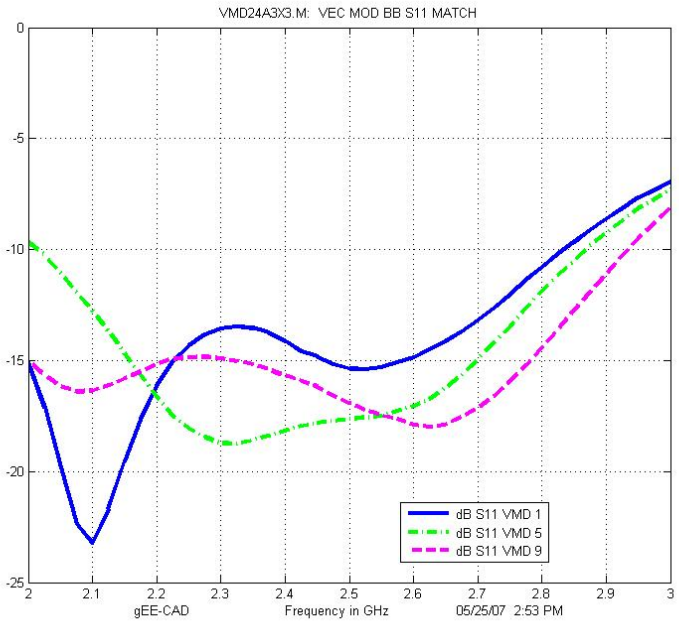


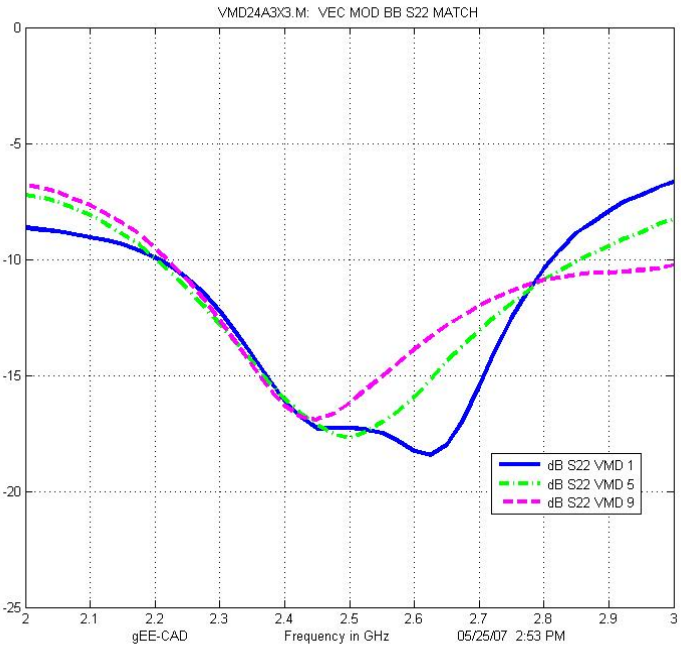




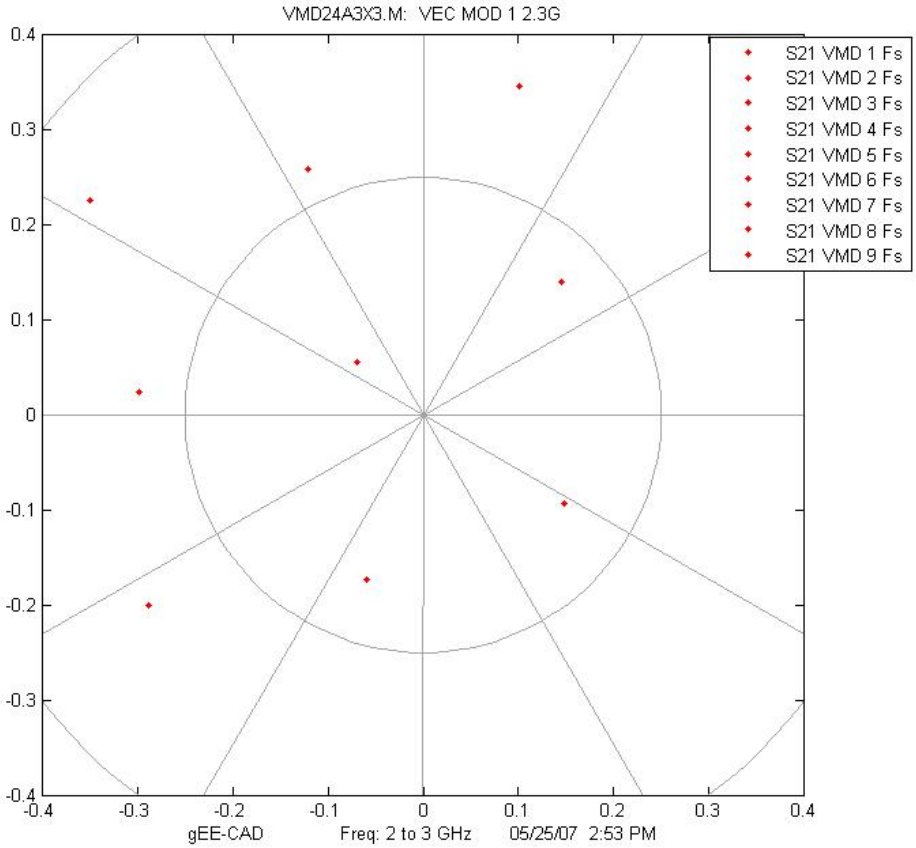
Jonathan Egan – Vector Modulator

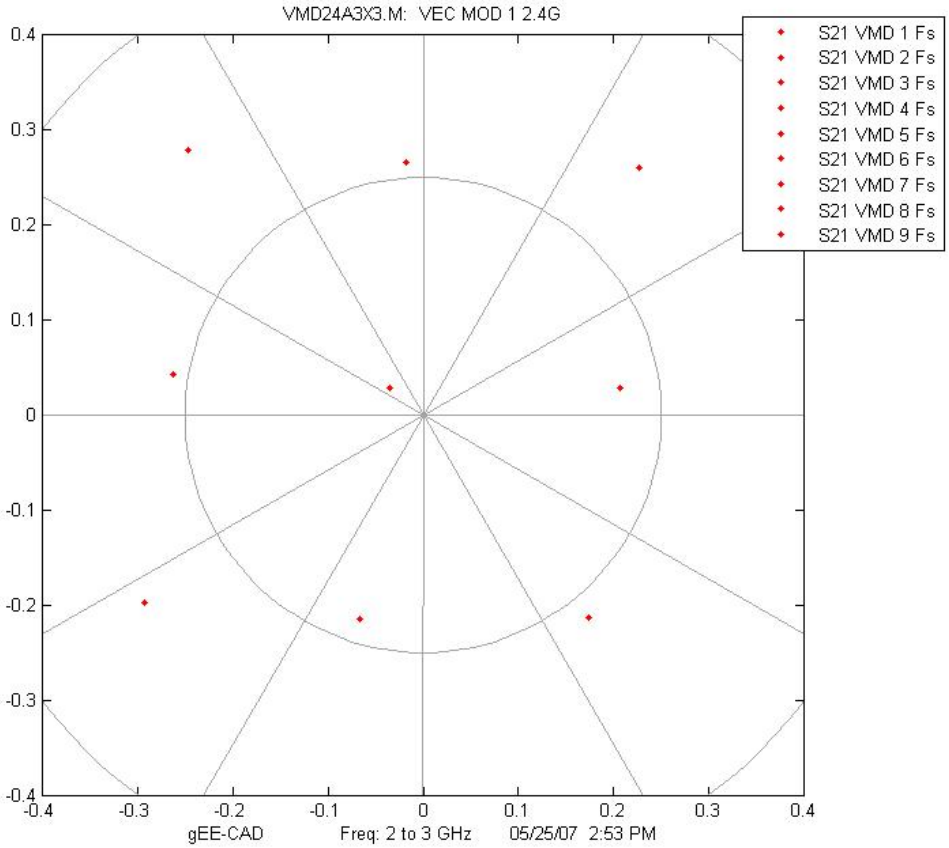
An S-Band Vector Modulator was designed for the 2305 to 2497 MHz WCS and ISM bands. The threshold voltage of the measured switches appeared to be a little different than nominal, so measurements were taken at positive and negative voltages representing fully OFF and fully ON switch states (-1.2V and +0.6V). Next the voltages were adjusted for minimum attenuation (-0.77V), then measurements were made for a 9 x 9 array representing I/Q inputs at –max, min, +max amplitudes. S-parameters were measured at these states and then a 2nd die was checked for comparison. As expected, variation between die in the same wafer run is negligible. Following are plots of a measured 9x9 vector array are shown at various frequencies around the design center and input/output match is shown following. Input and Output match are better than 10 dB from 2.2 to 2.8 GHz. The 9x9 array as measured is centered best from 2.4 to 2.5 GHz. For instance, I/Q control voltages could be adjusted to center the 9x9 array better at 2.3 GHz but some additional insertion loss would be incurred compared to operation at 2.45 GHz.



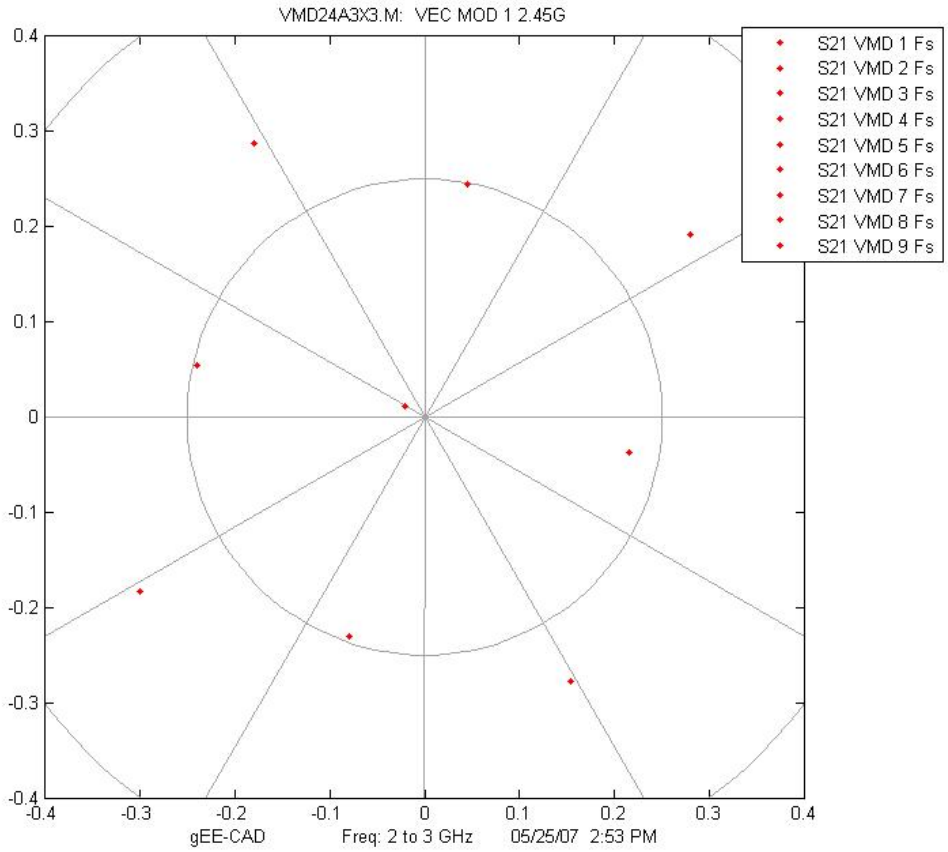


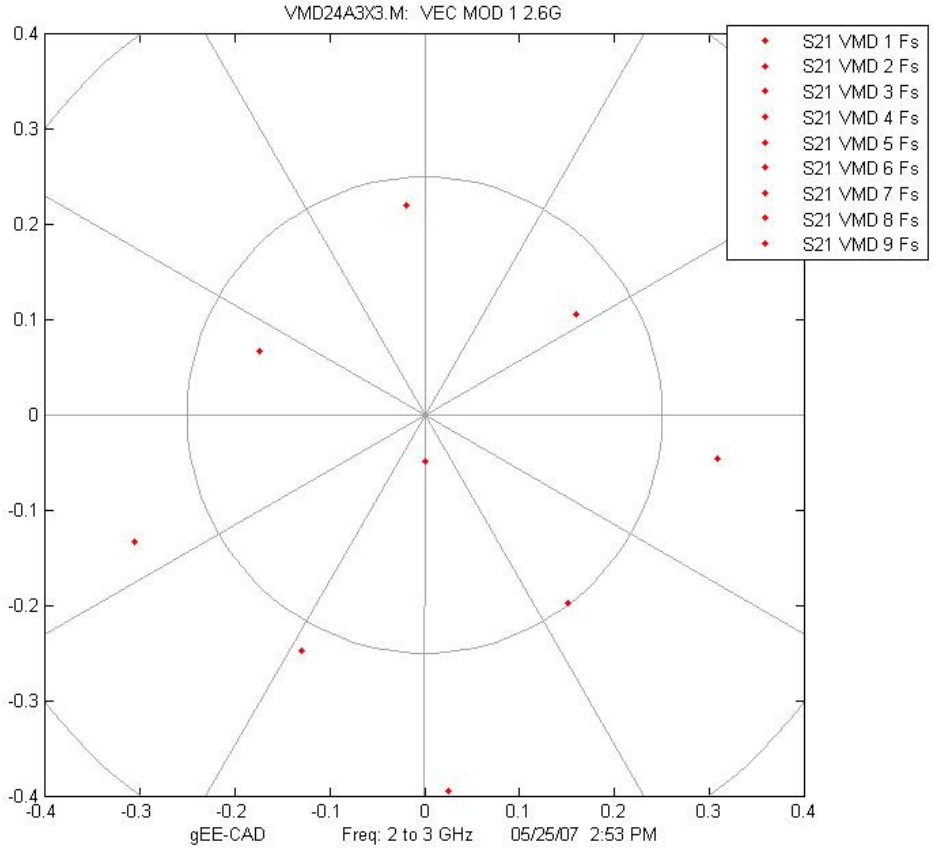
Input and Output Match (S11/S22) of the Vector Modulator at 3 different I/Q control inputs



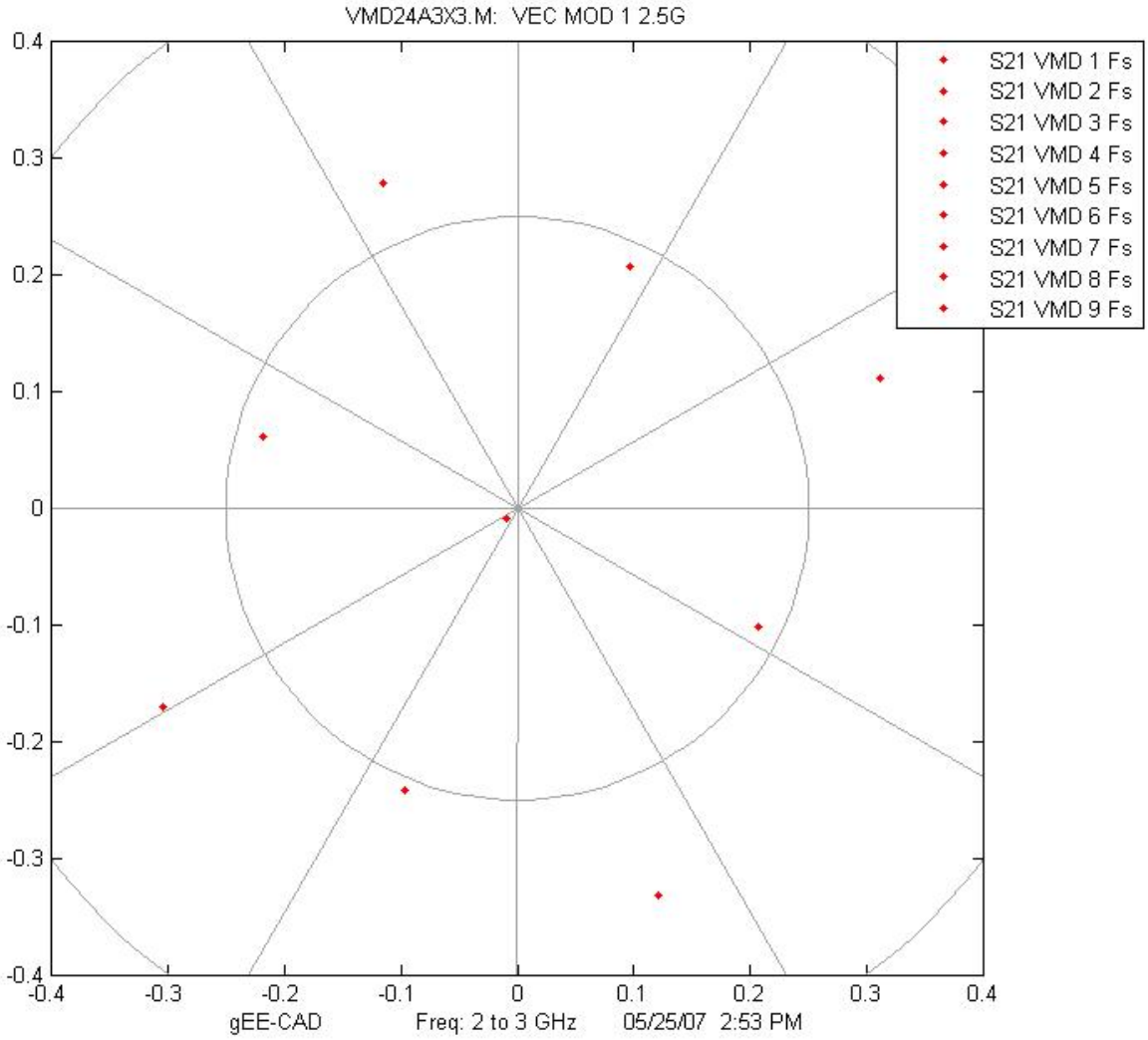


S21 for 9x9 Array of I/Q Inputs (-1.2V, -0.77V, +0.6V) of the Vector Modulator: 2.3 & 2.4 GHz





S21 for 9x9 Array of I/Q Inputs (-1.2V, -0.77V, +0.6V) of the Vector Modulator: 2.5 & 2.6 GHz



Centered 9x9 Array of I/Q Inputs (-1.2V, -0.77V, +0.6V) of the Vector Modulator: 2.45GHz

Medium Power Amp 1 – Peter Smith

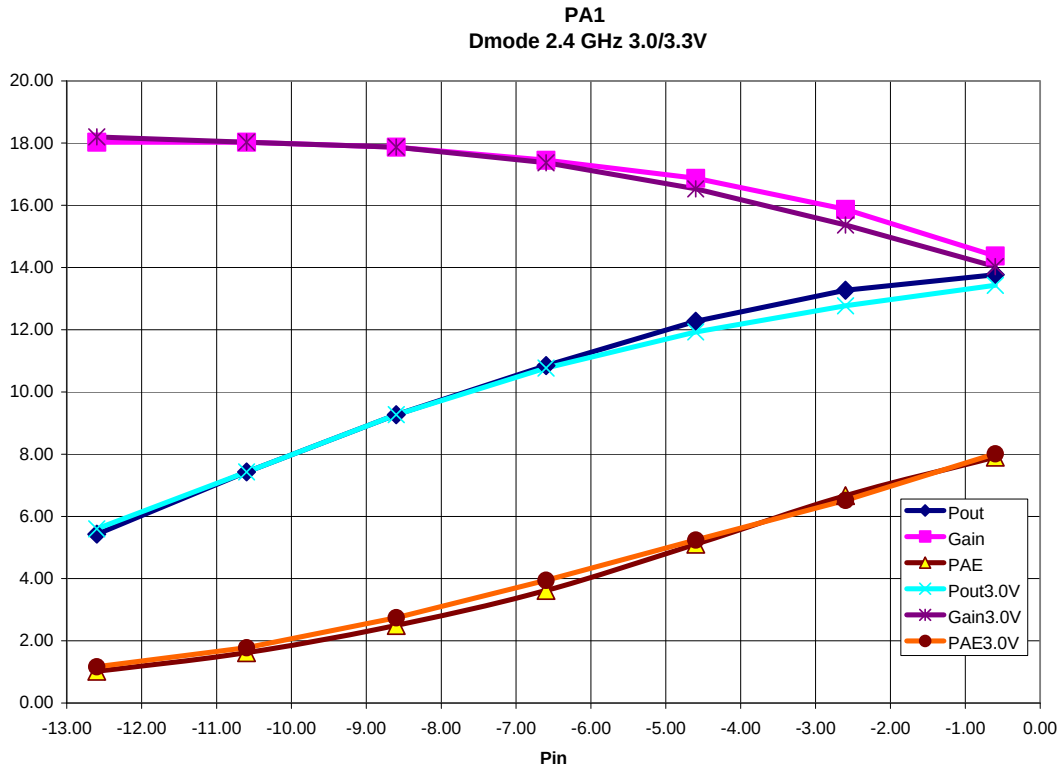
An S-Band Medium Power Amplifier was designed for the 2305 to 2497 MHz WCS and ISM bands. This design uses two stages of amplification to achieve good gain. Measured output power, gain, PAE, and s-parameters are following: The design was at 3.3V but was also measured at 2.0, 3.0, and 3.3V with about 22-24 mA for the first stage and 78-80 mA for the second stage typically. DC current consumption was higher than expected. As is typical for amplifiers in this process the measured output power was lower than expected by about 3 dB. Following are s-parameters for two die that were virtually identical and non-linear performance measurements. Output match was actually better at 2.0 V of bias and got worse at the nominal design voltage of 3.3V. S21 and S11 did not change much between 2.0, 3.0, and 3.3 V of bias. Gain S21 was quite good at better than 17 dB.

Peter Smith

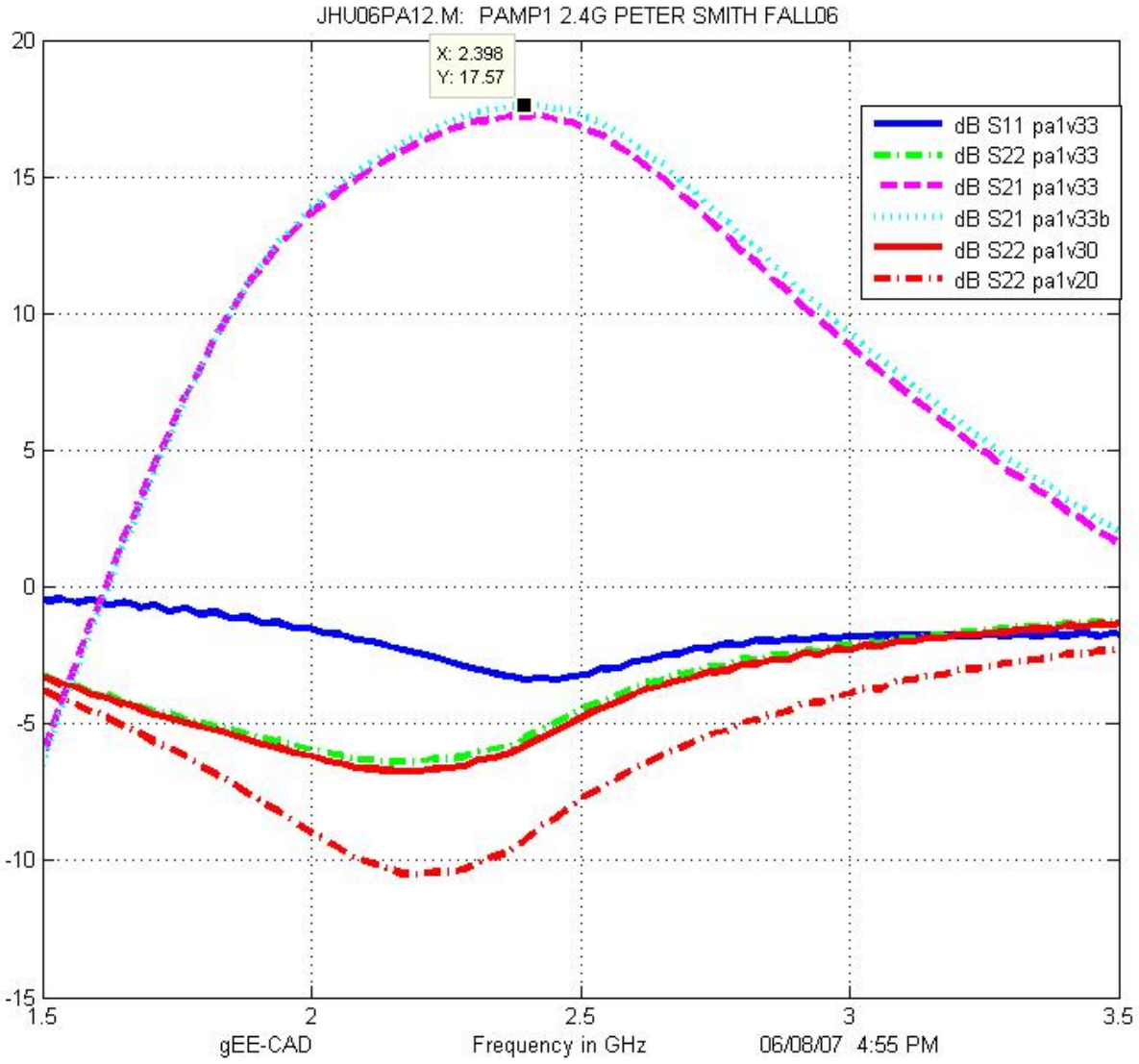
Measured 2.4 GHz Power Amp… 3.3 V 24 & 79 mA

2.4 GHz	Die#1	**PA1 2.4 GHz Dmode Fall06 TQPED**				3.3 V 24 & 79 mA			
Pin(SG)	**Pout(SA)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I2(3.3V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-12.0	4.83	-12.60	5.43	18.03	79	336.6	3.49	1.0	1.0
-10.0	6.83	-10.60	7.43	18.03	79	336.6	5.53	1.6	1.6
-8.0	8.67	-8.60	9.27	17.87	78	333.3	8.45	2.5	2.5
-6.0	10.25	-6.60	10.85	17.45	77	330.0	12.16	3.7	3.6
-4.0	11.67	-4.60	12.27	16.87	75	323.4	16.87	5.2	5.1
-2.0	12.67	-2.60	13.27	15.87	71	310.2	21.23	6.8	6.7
0.0	13.17	-0.60	**13.77**	14.37	65	290.4	23.82	8.2	**7.9**

2.4 GHz	Die#1	**PA1 2.4 GHz Dmode Fall06 TQPED**				3.0 V 24 & 79 mA			
Pin(SG)	**Pout(SA)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I2(3.0V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-12.0	5.00	-12.60	5.60	18.20	79	306.0	3.63	1.2	1.2
-10.0	6.83	-10.60	7.43	18.03	79	306.0	5.53	1.8	1.8
-8.0	8.67	-8.60	9.27	17.87	78	303.0	8.45	2.8	2.7
-6.0	10.17	-6.60	10.77	17.37	76	297.0	11.94	4.0	3.9
-4.0	11.33	-4.60	11.93	16.53	74	291.0	15.60	5.4	5.2
-2.0	12.17	-2.60	12.77	15.37	71	282.0	18.92	6.7	6.5
0.0	12.83	-0.60	**13.43**	14.03	65	264.0	22.03	8.3	**8.0**



Performance (PAE, Pout, Gain) of Power Amplifier Design 1 at 3.0/3.3V DC Bias



S-Parameters of Power Amplifier Design 1 at 3.3V and S22 at 2.0/3.0/3.3V DC Bias

Medium Power Amp 2– Niral Patel & Ben Myers

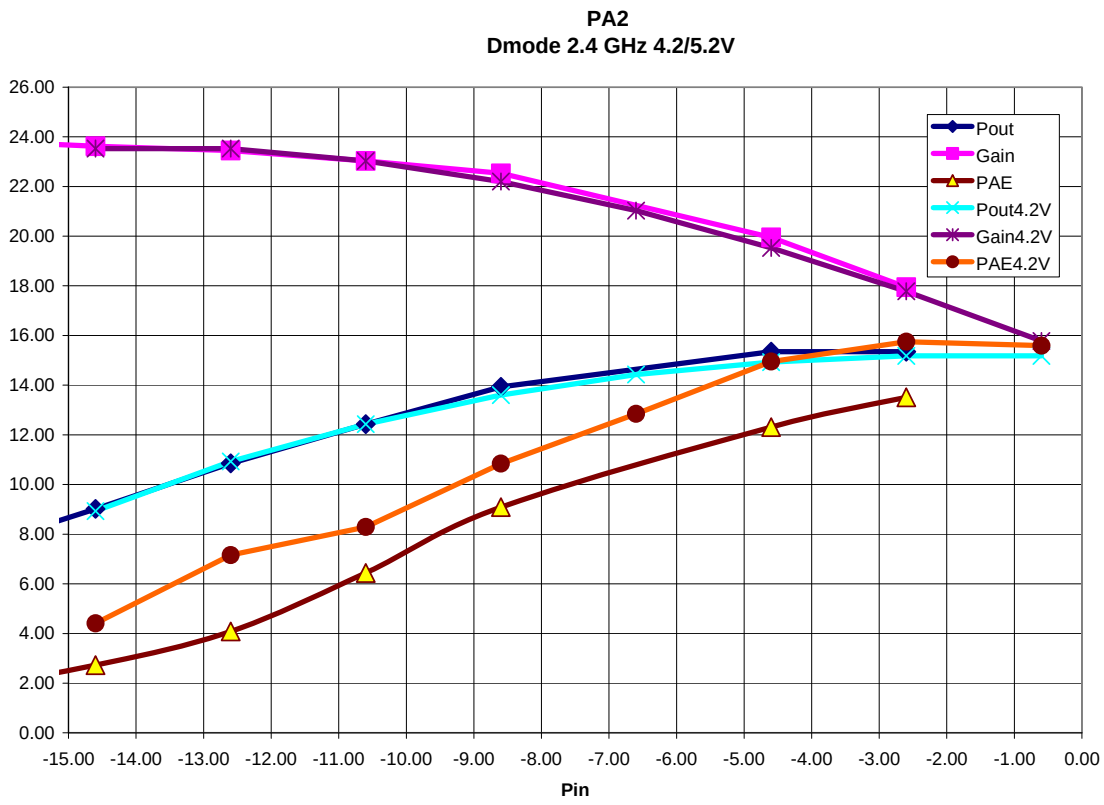
An S-Band Medium Power Amplifier was designed for the 2305 to 2497 MHz WCS and ISM bands. This design uses two stages of amplification to achieve good gain. Measured output power, gain, PAE, and s-parameters are following: The design was at 5.2V but was also measured at 4.2V with comparable output power and gain but with increased efficiency. Output Power was a little lower than predicted (15 dBm vs 21 dbm) but was consistent with other measured devices for this wafer fab. PAE was measured to be about 13% and 15% at 5.2V/4.2V of DC bias compared to a predicted 23%. S-parameters were similar in shape to simulations with slightly less gain (S21). There is little variation between the measured data at 4.2V at 42 mA and 5.2V at 47 mA (VGS=-0.1V). Note there appears to be a potential instability issue at about 1.3 GHz though the design was stable for 50 ohm input/output probe measurements.

Power Amp at 5.2V VDS (2.4 GHz)

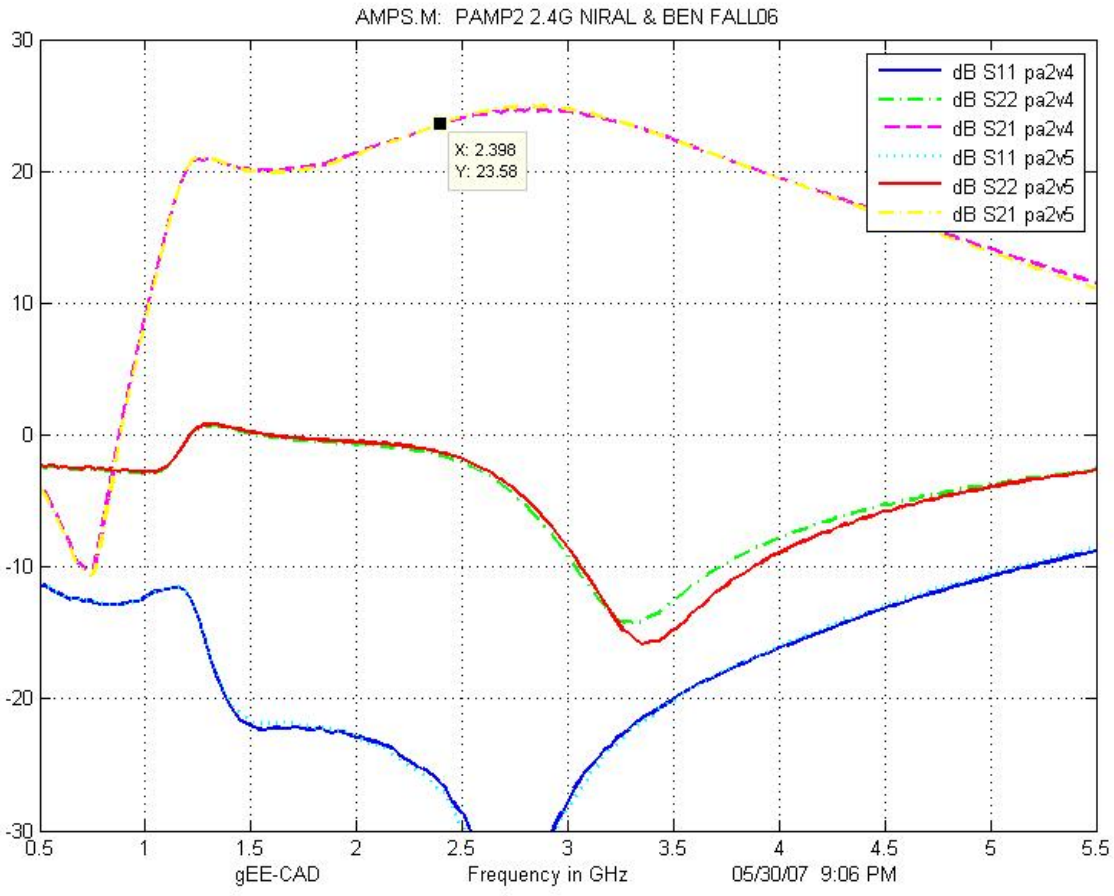
Measured 2.4 GHz Power Amp… 5.2 V 47 mA -0.1V VGS

2.4 GHz	Die#1	**PA2 2.4 GHz Dmode Fall06 TQPED**				5.2V ; 47 mA			
Pin(SG)	**Pout(SA)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I1(5.2V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-20.0	2.58	-20.60	3.18	23.78	42	218.4	2.08	1.0	0.9
-18.0	4.75	-18.60	5.35	23.95	44	228.8	3.43	1.5	1.5
-16.0	6.67	-16.60	7.27	23.87	56	291.2	5.33	1.8	1.8
-14.0	8.42	-14.60	9.02	23.62	56	291.2	7.98	2.7	2.7
-12.0	10.25	-12.60	10.85	23.45	57	296.4	12.16	4.1	4.1
-10.0	11.83	-10.60	12.43	23.03	52	270.4	17.50	6.5	6.4
-8.0	13.33	-8.60	13.93	22.53	52	270.4	24.72	9.1	9.1
-4.0	14.75	-4.60	15.35	19.95	53	275.6	34.28	12.4	12.3
-2.0	14.75	-2.60	**15.35**	17.95	48	249.6	**34.28**	13.7	**13.5**

2.4 GHz	Die#1	**PA2 2.4 GHz Dmode Fall06 TQPED**				4.2V ; 42 mA			
Pin(SG)	**Pout(SA)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I1(4.2V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-14.0	8.33	-14.60	8.93	23.53	42	176.4	7.82	4.4	4.4
-12.0	10.33	-12.60	10.93	23.53	41	172.2	12.39	7.2	7.2
-10.0	11.83	-10.60	12.43	23.03	50	210.0	17.50	8.3	8.3
-8.0	13.00	-8.60	13.60	22.20	50	210.0	22.91	10.9	10.8
-6.0	13.83	-6.60	14.43	21.03	51	214.2	27.73	12.9	12.8
-4.0	14.33	-4.60	14.93	19.53	49	205.8	31.12	15.1	15.0
-2.0	14.58	-2.60	**15.18**	17.78	49	205.8	**32.96**	16.0	**15.7**
0.0	14.58	-0.60	15.18	15.78	49	205.8	32.96	16.0	15.6



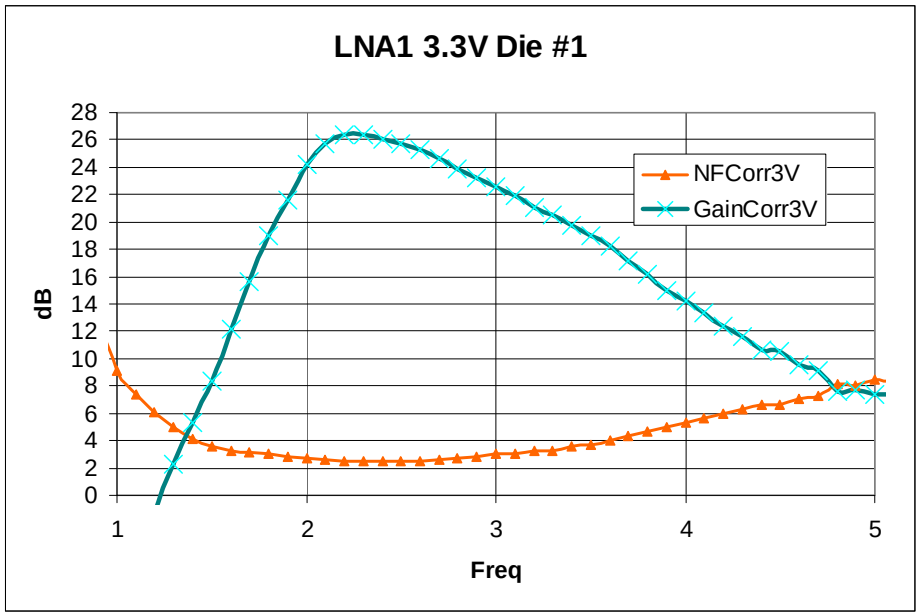
Performance (PAE, Pout, Gain) of Power Amplifier Design at 5.2/4.2V DC Bias

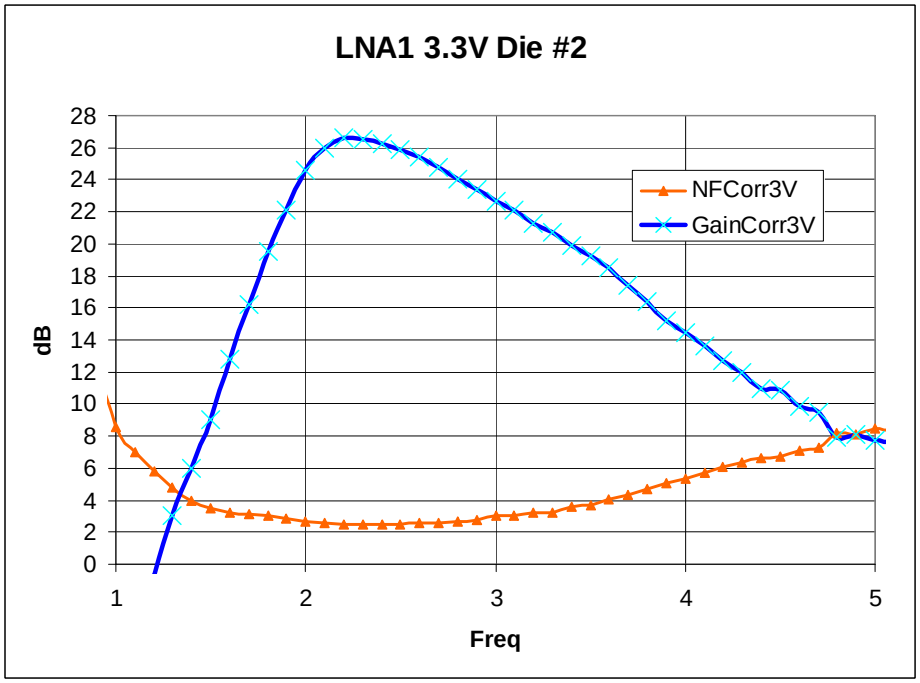


S-Parameters of Power Amplifier Design at 5.2/4.2V DC Bias

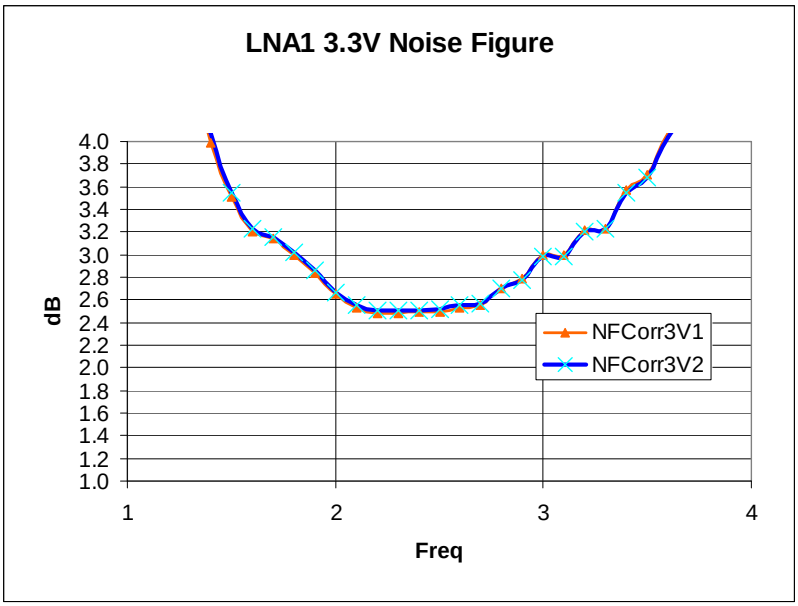
Low Noise Amplifier 1 (Low Power)–N. Hughes & L. Macejka

An S-Band Low Noise Amplifier was designed for the 2305 to 2497 MHz WCS and ISM bands. This design uses relatively small Emode PHEMTs for a very low DC power consumption two stage LNA (~10mW per stage). The design worked very well but could only be measured under compression with the 8510 NWA because the analyzer would lose lock below a certain power level which was still too high for the LNA. Gain was measured with the noise figure analyzer at about 26 dB over the band with about 2.5 dB Noise Figure. Two die were measured with very similar performance characteristics. Each stage required a 3.3V supply and about 2 to 3 mA per stage at 20 mW or less total power consumption.

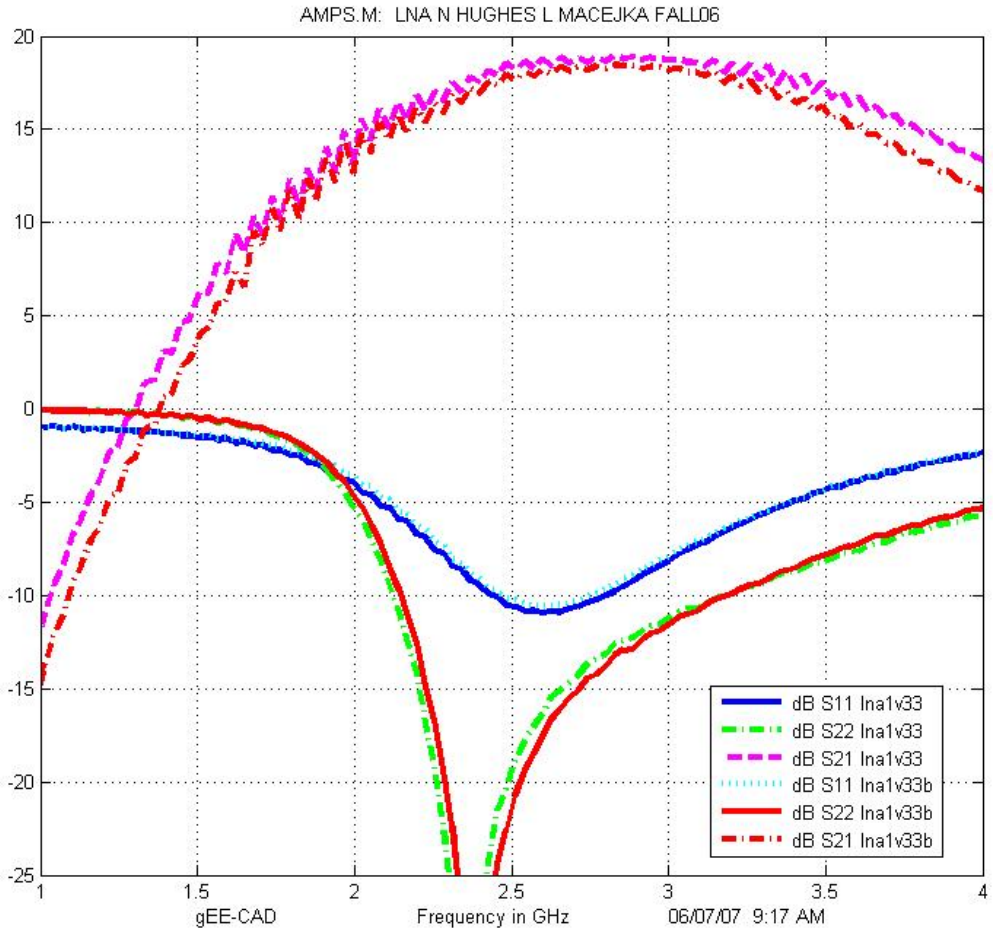




Plots of 2 Die for LNA1 at 3.3V/4-6 mA bias. Corrected Noise Figure Analyzer Data.



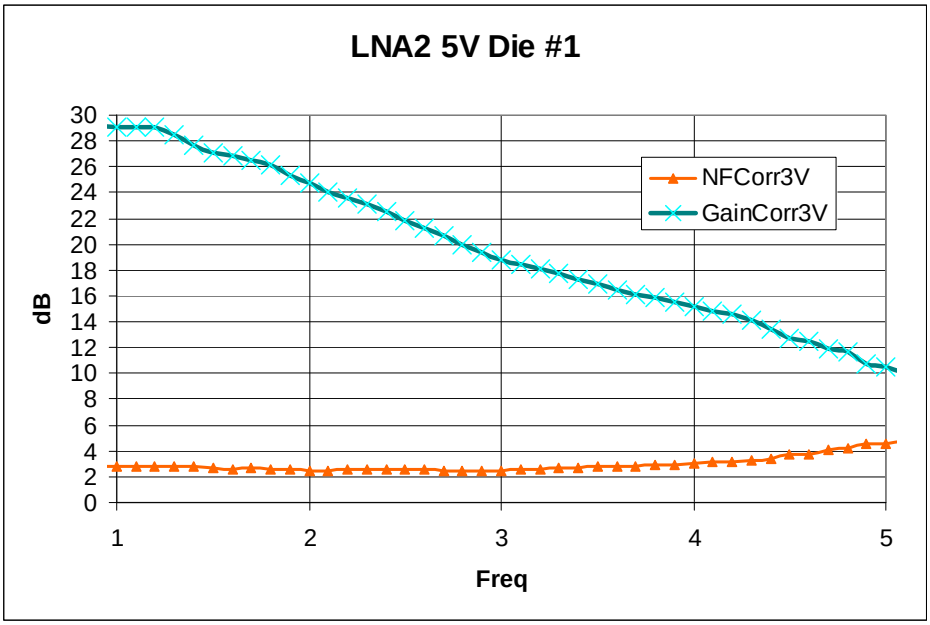
Corrected Noise Figure Only of 2 Die LNA1

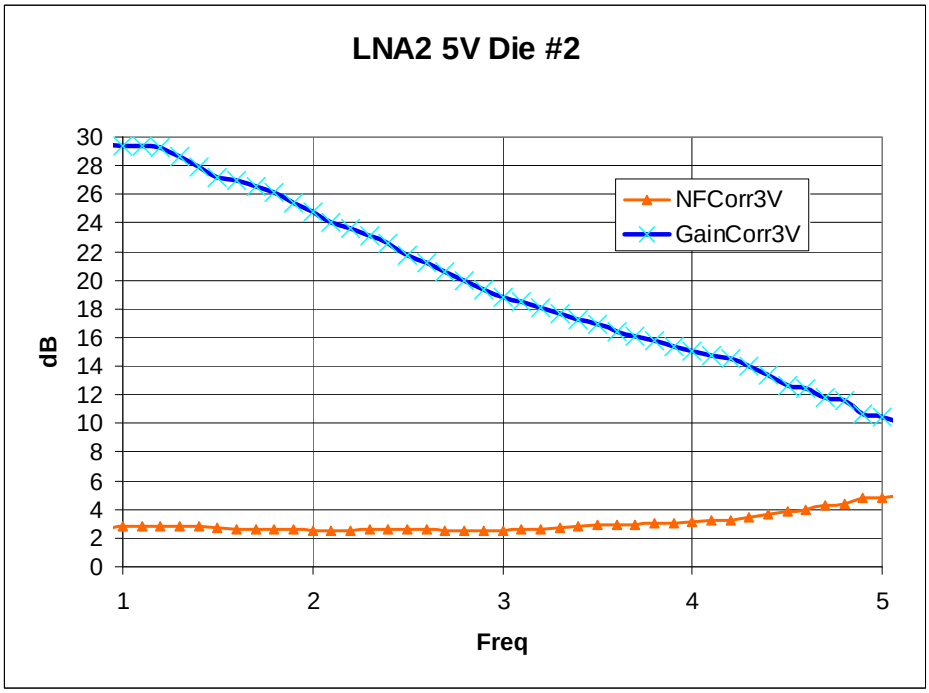


S-Parameters for Low DC Power LNA 1 at 3.3V/4-6 mA bias. S21 is over-driven.

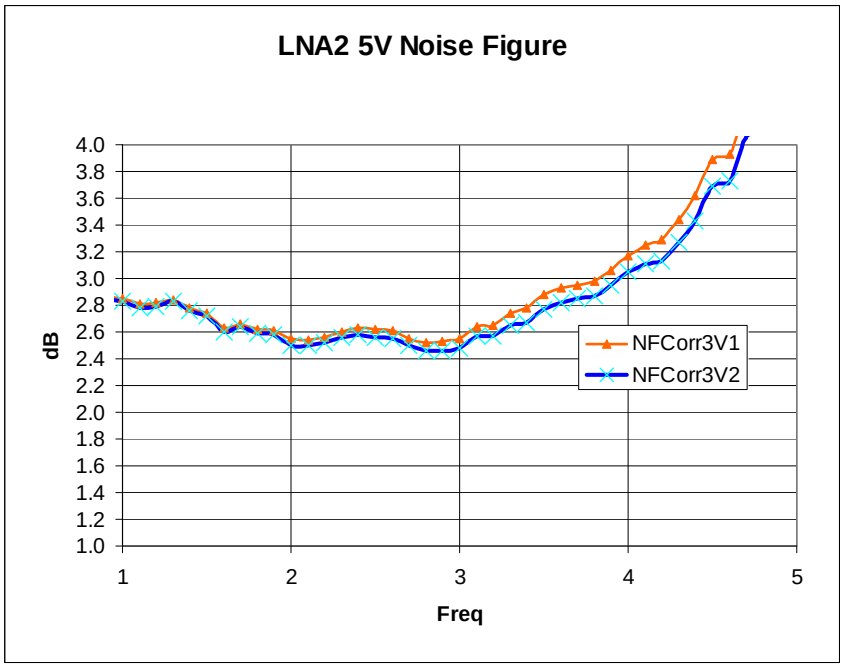
Low Noise Amplifier 2–Dave Sokol

An S-Band Low Noise Amplifier was designed for the 2305 to 2497 MHz WCS and ISM bands. This design uses standard size Emode PHEMTs with a single DC input for a typical bias of 5V and 37 mA. The measured bias matched simulations. The design worked very well and was measured with the 8510 NWA without having to over drive the LNA. Gain was measured with the noise figure analyzer at about 22 dB with about 2.5 dB Noise Figure. Two die were measured with very similar performance characteristics. Each stage required a 5V supply and about 25-37 mA.

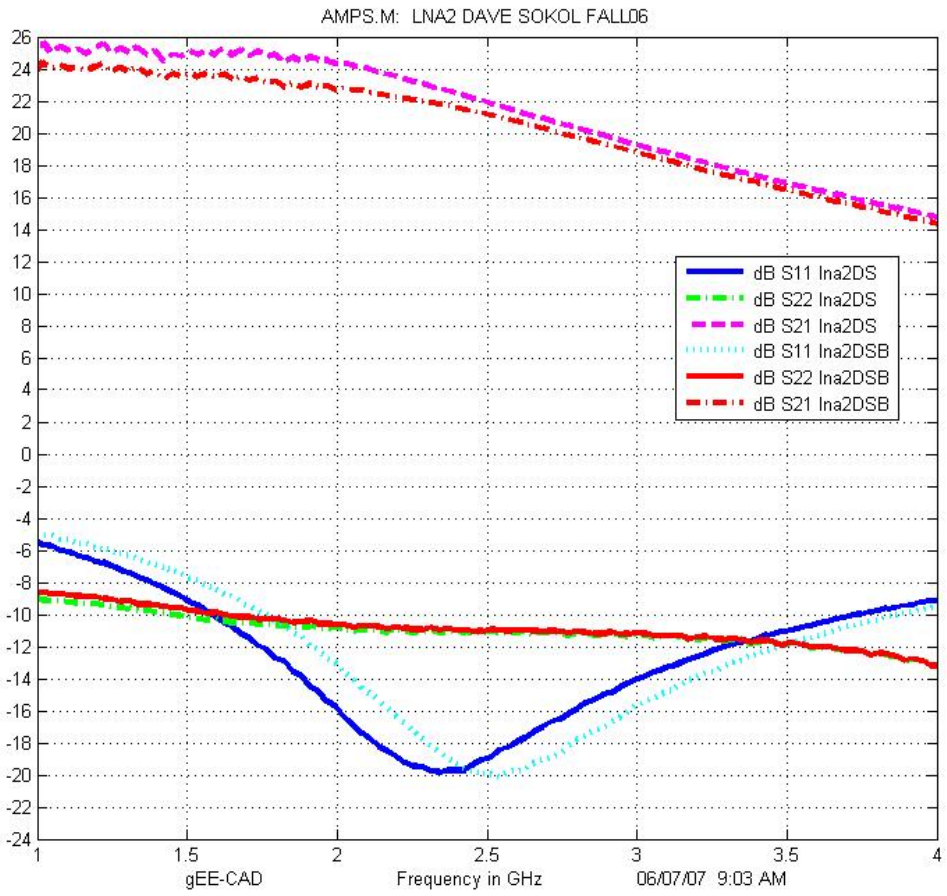




Plots of 2 Die for LNA2 at 5V/25-37 mA bias. Corrected Noise Fig. Analyzer Data.



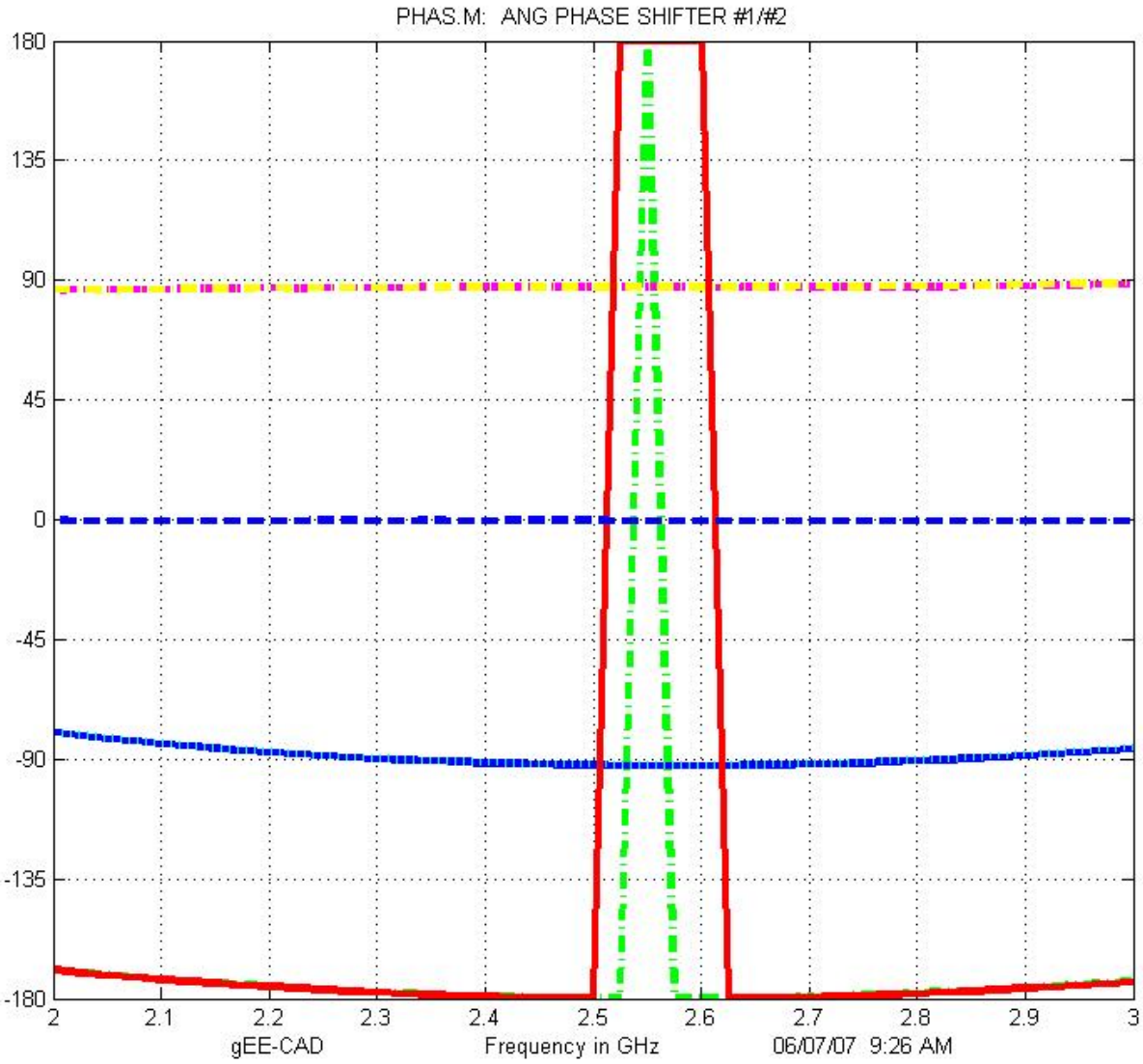
Corrected Noise Figure Only of 2 Die LNA2



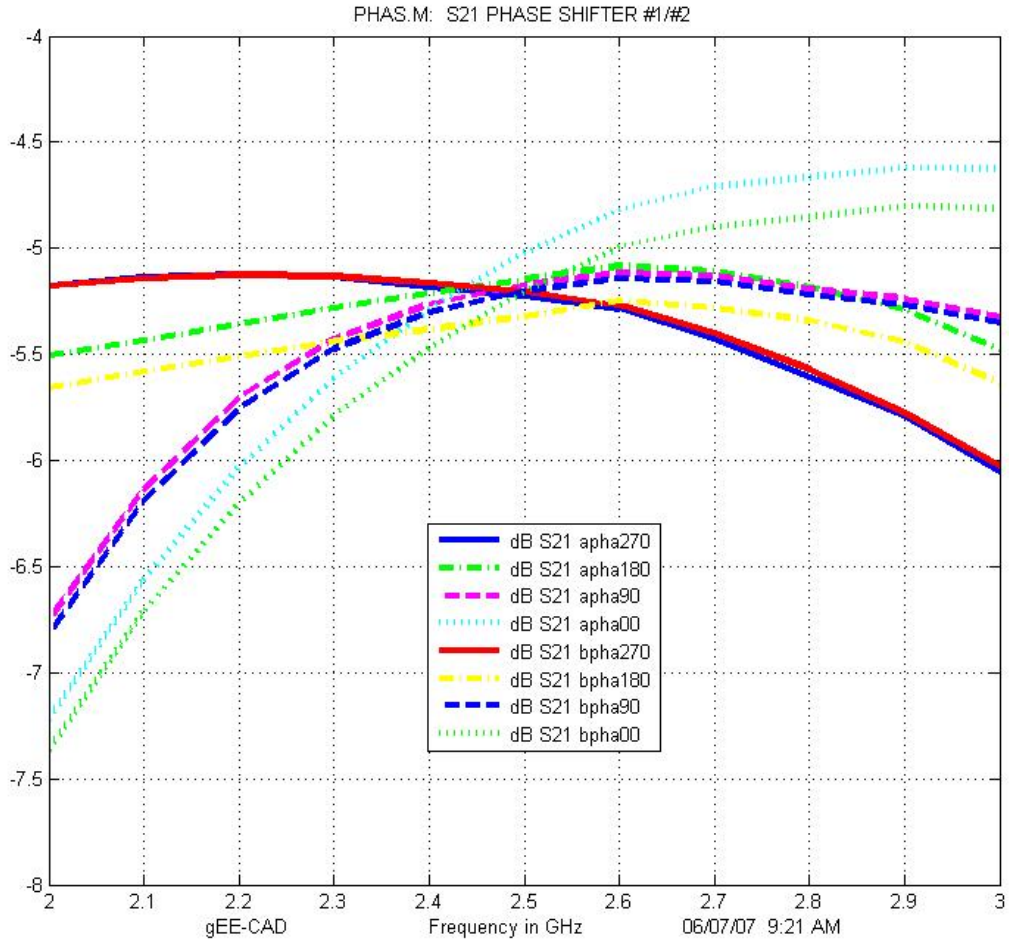
S-Parameters for 2 Die LNA 2 at 5V/25-37 mA bias.

Phase Shifter–Dave Wendland

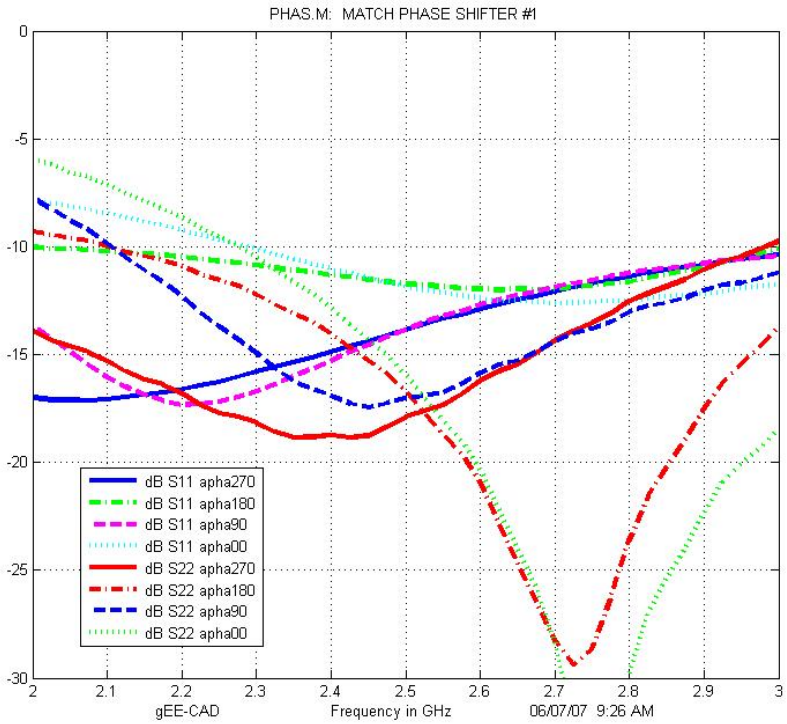
An S-Band 2 Bit Phase Shifter was designed for the 2305 to 2497 MHz WCS and ISM bands. This design uses PHEMTs as switches and generates the complementary switch driver voltages from TTL inputs using a simple efficient circuit. Phase shift measurements were very close to simulations. The driver circuit typically uses +5V at 5 mA with 0V or +5V at 3 mA for the 90 and 180 degree input bits. Testing showed how robust the driver circuit was as it worked with as little as +1V on the +5V input and also on the 90 and 180 degree TTL inputs with no apparent change in the s-parameters. Following are the plots from two different but virtually identical die showing the phase states. The apparent "jumps" in the 180 bit are really small changes between +180 and -180 degrees.



0, 90, 180, 270 Degree Phase Shifts of MMIC 2 Bit Phase Shifter with TTL Driver Circuit.



Insertion Loss S21 for 0, 90, 180, 270 Degree Phase Shifts of MMIC 2 Bit Phase Shifter.



Return Loss S11/S22 for 0, 90, 180, 270 Degree Phase Shifts of MMIC 2 Bit Phase Shifter.

Voltage Controlled Osc. – Dimitrios Loizos

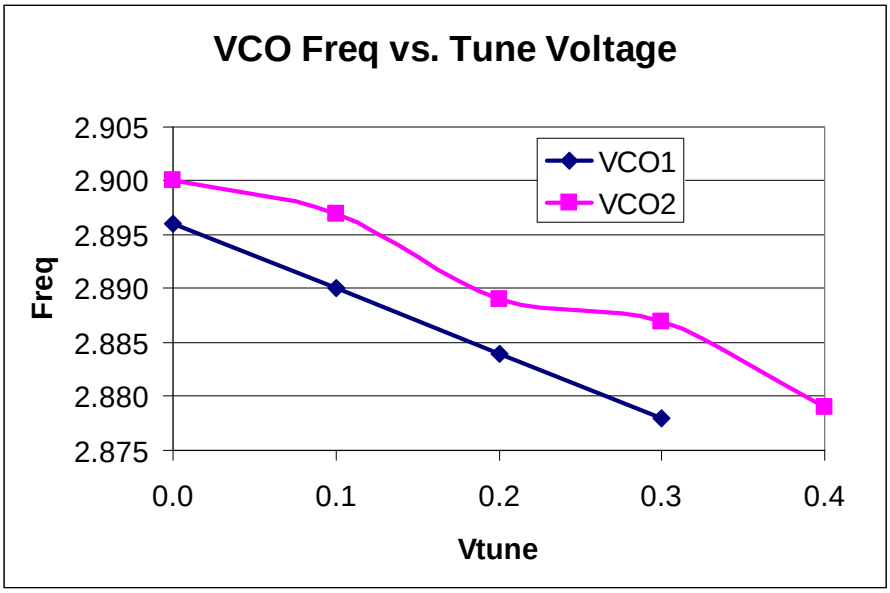
An S-Band Voltage Controlled Oscillator (VCO) was designed for the 2305 to 2497 MHz WCS and ISM bands. Output frequency was a little higher than expected but typical compared to previous VCO designs in the JHU course. The VCO worked fairly well with a little less tuning range and output power than expected. Harmonics were noted to be considerably lower than the fundamental at about 35-40 dBc down. Below are the output powers and frequencies of two measured devices. Bias was 5.0V at 36-37 mA and the tuning range was from 0 to 0.4 V for the varactor.

Measured MWO VCO
Dimitri Loizos

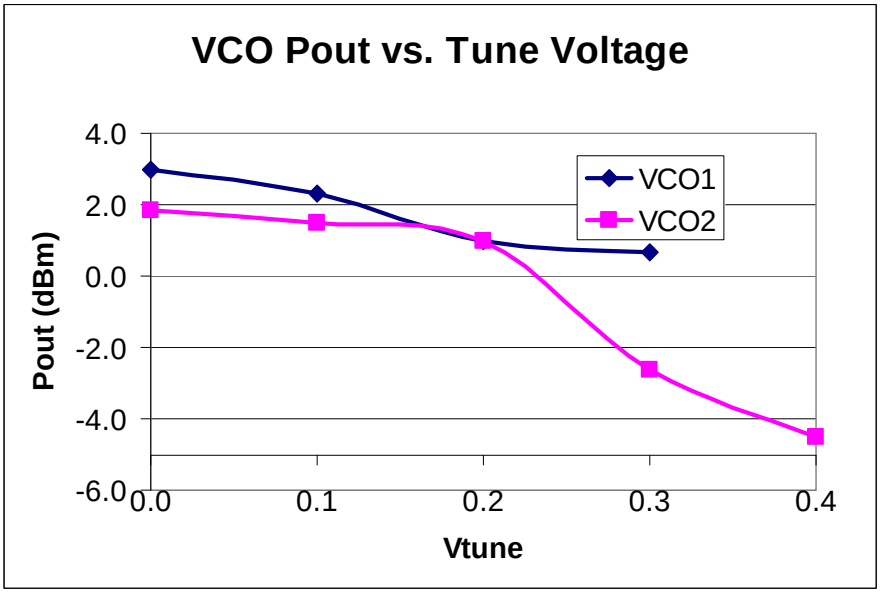
Seemed to drop out around 0.4V but had some tuning range from 0 to 0.4V.
Loss of output cables and probe estimated to ~0.85 dB X1 Add to Pout(measured).
Harmonics > 30 ; 40? dBc

ADS VCO VBias (V)	5V at 36mA Freq (GHz)	Pout(ms)	Die #1 Pout(corr)	X2 Pout(ms)	dbc/hz 100k	dbc/hz 1M
0.0	2.896	1.3	**3.0**			
0.1	2.890	0.7	**2.3**			
0.2	2.884	-0.7	**1.0**			
0.3	2.878	-1.0	**0.7**			

ADS VCO VBias (V)	5V at 37mA Freq (GHz)	Pout(ms)	Die #2 Pout(corr)
0.0	2.900	0.2	**1.8**
0.1	2.897	-0.2	**1.5**
0.2	2.889	-0.7	**1.0**
0.3	2.887	-4.3	**-2.6**
0.4	2.879	-6.2	**-4.5**



Output Frequency Vs. Tuning Voltage VCO

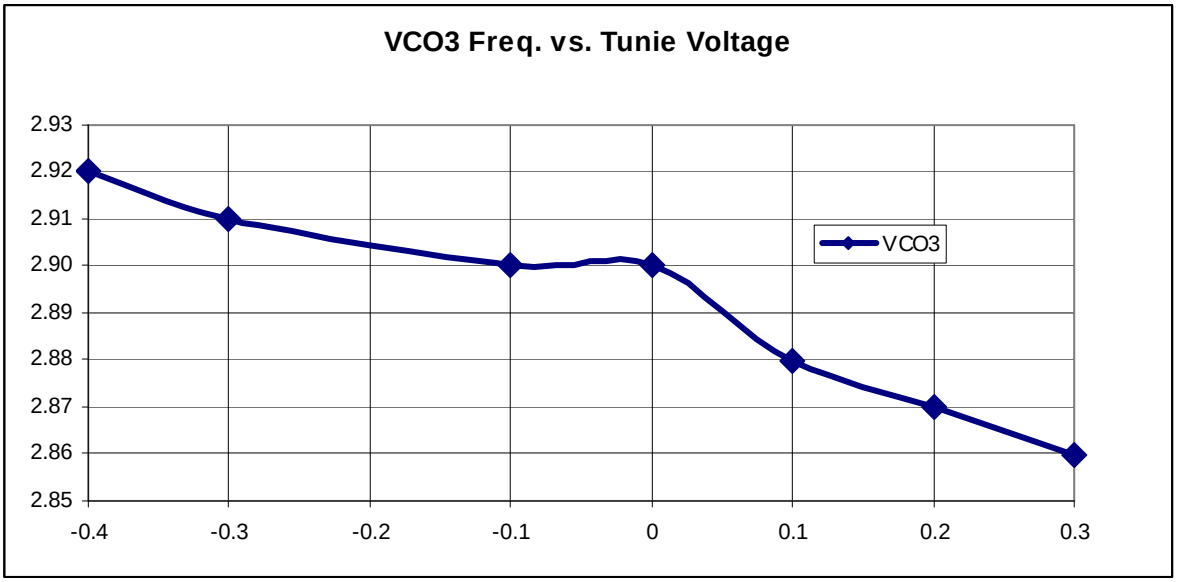


Output Power Vs. Tuning Voltage VCO

The VCO was Re-Measured 7/25/07:

Bias (V)	Freq (GHz)
-0.5	2.92
-0.4	2.92
-0.3	2.91
-0.1	2.90
0	2.90
0.1	2.88
0.2	2.87
0.3	2.86

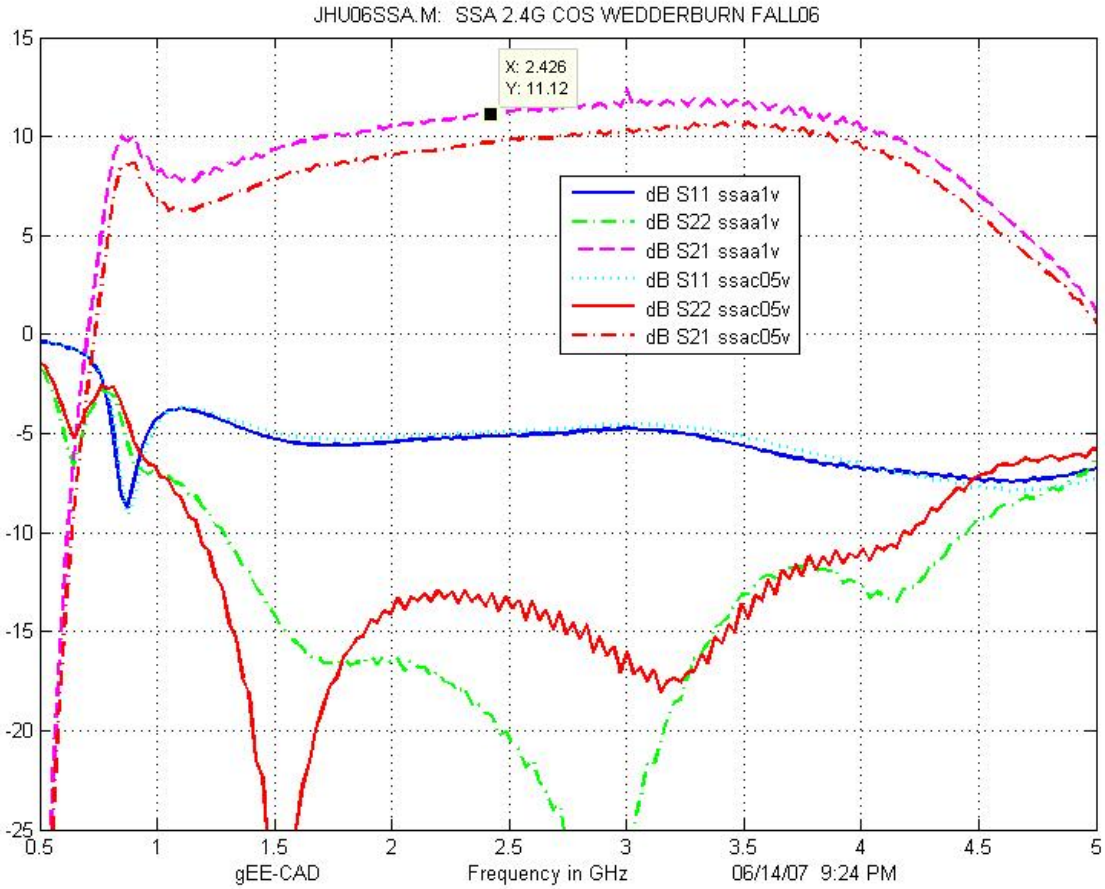
For bias of 0V, the power of the fundamental, second and 3rd harmonic were: 1dBm, -31dBm and -29dBm, respectively.



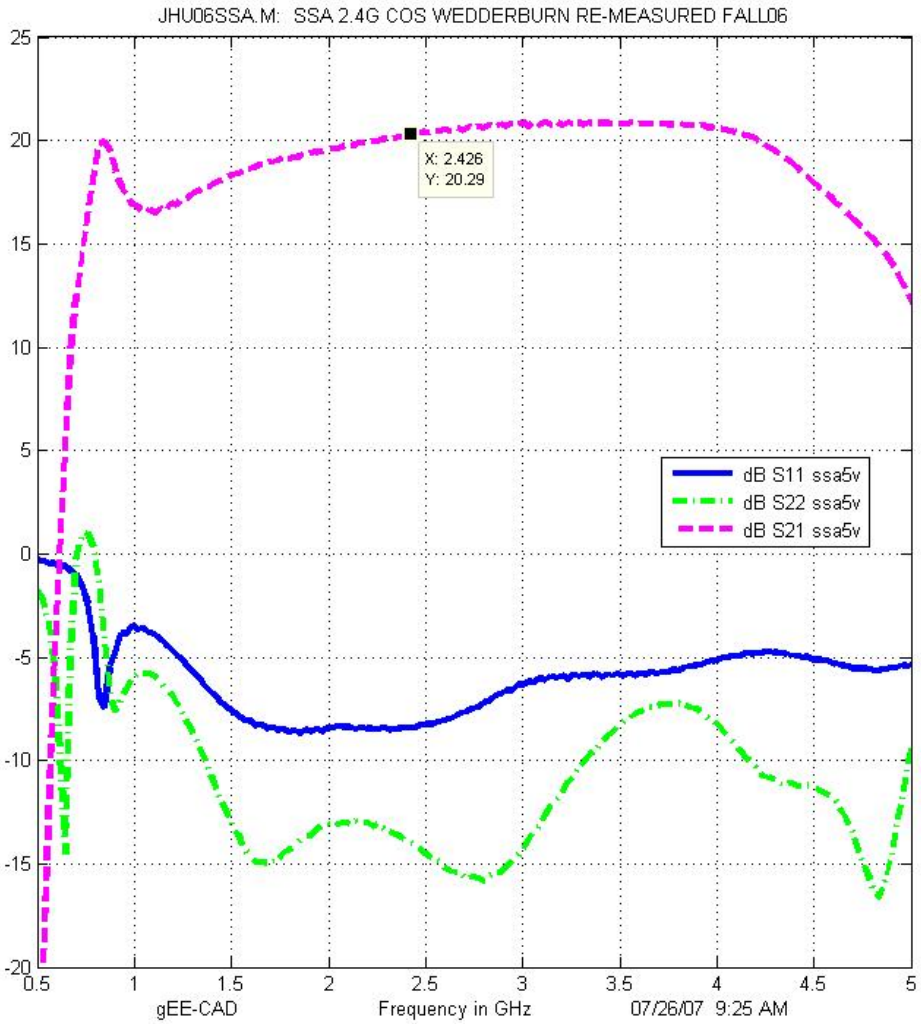
Small Signal Amplifier – Cosburn Wedderburn

An S-Band Voltage Controlled Oscillator (VCO) was designed for the 2305 to 2497 MHz WCS and ISM bands. There appeared to be some low frequency stability issues at higher drain biases. When the voltage was increased on the drain above about 1 V, the 8510 NWA would show a dramatic drop in gain. Input and Output match seemed close to simulated match, but the gain appeared to drop as voltage was increased towards the 5V design bias. Measurements were taken at 5V and 12-15 mA of bias but the best gain was achieved at 1V and 5 mA of bias. Once the gain started to increase above 10-11 dB, the amplifier would appear to oscillate.

Next, a spectrum analyzer and signal generator were used to observe the oscillations. For low drain voltages, there was gain until VDD was increased above 1V and then low frequency oscillations of about 30 MHz would occur. Large capacitors were used on the bias supplies to damp low frequency oscillations and this technique has worked well in past years'. Certainly there is a lot of gain with PHEMTs compared to previous year's MESFET designs. Also, simulations are rarely performed at such low frequencies to insure stability in the MHz range.. Some investigation into why this circuit and a few other circuits oscillate at tens of MHz in spite of large capacitors on the DC needle probes needs to be pursued.



S-Parameters for 2 SSA Die at 1V/5 mA bias.



S-Parameters for SSA Die at 5V/36 mA bias.

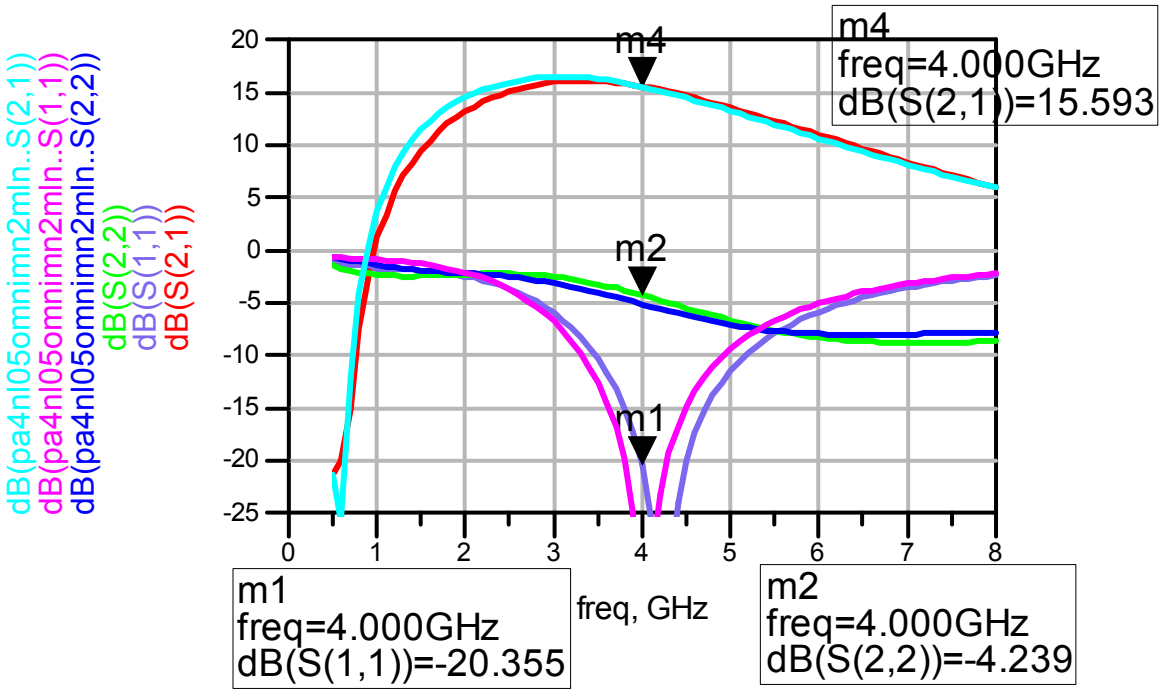
The Small Signal Amplifier was re-measured on July 25, 2007 after re-calibrating and setting up the probe station and NWA for some additional follow up. Stability issues from the previous tests were not evident in this measurement and the bias was increased up to the full 5V supply--as designed. Measured s-parameters were similar to expectations—(see student report). While the new setup was stable at low frequencies for this SSA design, additional attempts to measure other test circuits that previously exhibited low frequency oscillation problems still had those same low frequency problems.

Class Design Examples: Low Noise Amplifier and Power Amplifier (4 GHz) by John Penn

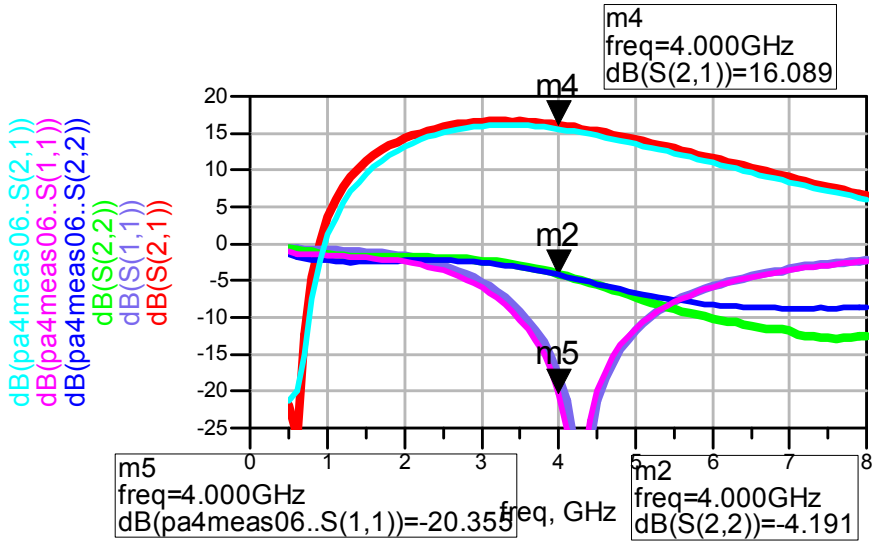
During the course the students are shown a design example of a low noise amplifier and a medium power amplifier at 4 GHz. In previous years, layouts were completed for the LNA and PA design in Agilent's ADS and later Microwave Office MWO on a single 60 x 60 mil die (54 x 54 after dicing) using TriQuint's TQTRX MESFET process. Last year (2005), the LNA and PA examples were re-designed using ADS and TriQuint's 0.5 um PHEMT (TQPED) process. Measured data was taken of the TQPED designs in 2005 and again in 2006 for comparison. Gain and output power were a little better on this 2006 fabrication compared to the 2005 wafer run. DC Bias was comparable between the 2005 and 2006 Power Amps but output power was more than 1 dB higher and gain 2 dB higher resulting in 31% PAE versus 23% at 4.0V and 4.0 GHz. This year measurements were taken at additional drain voltages and also at 4.05 GHz which appeared to be a peak in the performance, close to the design frequency of 4.0 GHz. Output Power was about 17 dBm at 4.05 GHz and 4V dropping to about 16 dBm at 4.0 GHz and 3.0V. Power Added Efficiency (PAE) got better at 3.5V and especially 3.0V of bias peaking at about 40% PAE for 4.05 GHz and 3.0V DC Bias. The Power Amp design agreed well with simulations for s-parameters but was a little lower for non-linear performance predictions (Pout and PAE).

The Low Noise Amplifier showed very good agreement between ADS simulations and measurements. When the Noise Figure meter was used to measure gain and noise figure of the LNA, a through connection was used to subtract out losses for the measurements. The "through" path appeared to be a little low compared to measurements from 2005 and also compared to measurements made with the same setup and a signal generator. This may explain why the noise figure seems a little higher by a few tenths of a dB than predictions—similar shape though—and the gain is lower than that measured with the 8510 NWA for the same LNA at 3.0V DC Bias. If the other 3.75 dB "through" loss at 4.0 GHz were used instead of the 2.3 dB figure from the Noise Figure Instrument, the gain and noise figure at 4.0 GHz would be identical to simulations. Overall, the LNA and the PA designs compared well to simulations at 4.0 GHz.

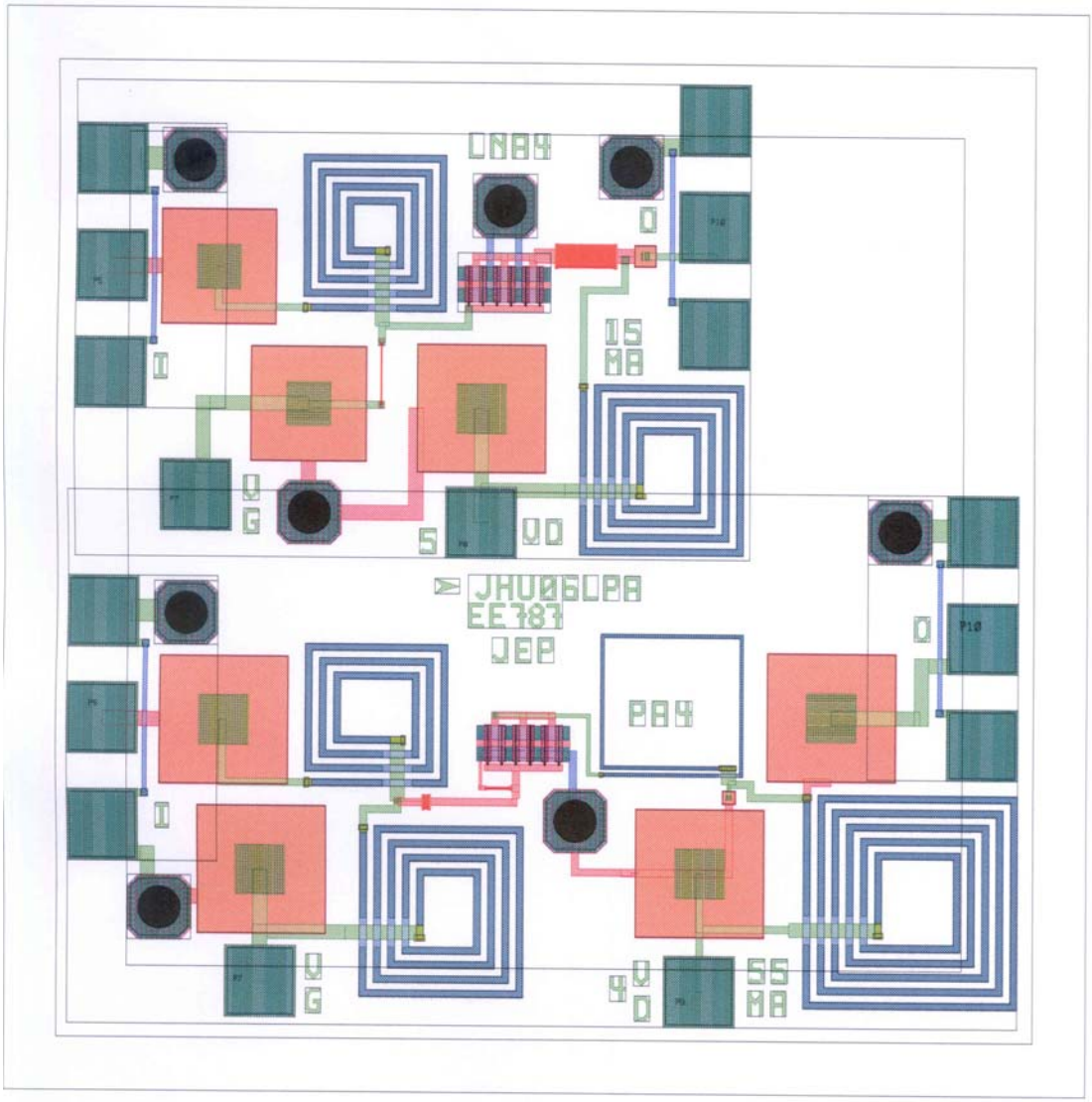
Other test circuits were also designed to be used for future lectures and class examples.



Good Agreement Between Measured and Simulated (ADS) S-parameters for PA at 4.0V



Excellent Agreement: Re-Simulated with Measured device data (S-parameters for PA at 4.0V)



Layout of Class Example Designs: 4 GHz LNA and 4 GHz PA Designs (54 mil x 54 mil

Performance (PAE, Pout, Gain) of Power Amplifier Design at 3.0/3.5,4.0V DC Bias and 4.0 GHz

D Mode Power Amps--4.0 GHz example at 4.0 V
Measured better at lower voltages… Loss 3.5 dB for thru

4 GHz Die#1 **PA4 GHz Dmode Fall06 TQPED** 4.0V ; 40 mA

Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(4.0V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-20.0	-5.33	-21.75	-3.58	18.17	38	152.0	0.44	0.3	0.3
-18.0	-3.17	-19.75	-1.42	18.33	39	156.0	0.72	0.5	0.5
-16.0	-1.17	-17.75	0.58	18.33	39	156.0	1.14	0.7	0.7
-14.0	0.33	-15.75	2.08	17.83	40	160.0	1.61	1.0	1.0
-12.0	2.33	-13.75	4.08	17.83	40	160.0	2.56	1.6	1.6
-10.0	4.50	-11.75	6.25	18.00	40	160.0	4.22	2.6	2.6
-8.0	6.50	-9.75	8.25	18.00	40	160.0	6.68	4.2	4.1
-6.0	8.50	-7.75	10.25	18.00	40	160.0	10.59	6.6	6.5
-4.0	10.17	-5.75	11.92	17.67	41	164.0	15.56	9.5	9.3
-2.0	11.83	-3.75	13.58	17.33	40	160.0	22.80	14.3	14.0
0.0	13.17	-1.75	14.92	16.67	40	160.0	31.05	19.4	19.0
2.0	14.33	0.25	16.08	15.83	38	152.0	40.55	26.7	26.0
3.0	14.67	1.25	16.42	15.17	38	152.0	43.85	28.9	28.0
4.0	15.00	2.25	16.75	14.50	38	152.0	47.32	31.1	30.0
5.0	15.17	3.25	**16.92**	13.67	38	152.0	**49.20**	32.4	**31.0**

4 GHz Die#1 **PA4 GHz Dmode Fall06 TQPED** 3.5V ; 42 mA

Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.5V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-10.0	4.67	-11.75	6.42	18.17	42	147.0	4.39	3.0	2.9
-8.0	6.67	-9.75	8.42	18.17	42	147.0	6.95	4.7	4.7
-6.0	8.67	-7.75	10.42	18.17	42	147.0	11.02	7.5	7.4
-4.0	10.33	-5.75	12.08	17.83	41	143.5	16.14	11.2	11.1
-2.0	11.83	-3.75	13.58	17.33	40	140.0	22.80	16.3	16.0
0.0	13.00	-1.75	14.75	16.50	39	136.5	29.85	21.9	21.4
2.0	13.83	0.25	15.58	15.33	38	133.0	36.14	27.2	26.4
3.0	14.33	1.25	16.08	14.83	38	133.0	40.55	30.5	29.5
4.0	14.67	2.25	**16.42**	14.17	37	129.5	**43.85**	33.9	**32.6**
5.0	14.83	3.25	**16.58**	13.33	38	133.0	**45.50**	34.2	**32.6**

4 GHz Die#1 **PA4 GHz Dmode Fall06 TQPED** 3.0V ; 42 mA

Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.0V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-10.0	4.83	-11.75	6.58	18.33	42	126.0	4.55	3.6	3.6
-8.0	6.83	-9.75	8.58	18.33	42	126.0	7.21	5.7	5.6
-6.0	8.67	-7.75	10.42	18.17	43	129.0	11.02	8.5	8.4
-4.0	10.17	-5.75	11.92	17.67	41	123.0	15.56	12.7	12.4
-2.0	11.50	-3.75	13.25	17.00	40	120.0	21.13	17.6	17.3
0.0	12.50	-1.75	14.25	16.00	39	117.0	26.61	22.7	22.2
2.0	13.33	0.25	15.08	14.83	39	117.0	32.21	27.5	26.6
3.0	13.83	1.25	15.58	14.33	37	111.0	36.14	32.6	31.4
4.0	14.17	2.25	15.92	13.67	38	114.0	39.08	34.3	32.8
5.0	14.33	3.25	**16.08**	12.83	37	111.0	**40.55**	36.5	**34.6**

Performance (PAE, Pout, Gain) of Power Amplifier Design at 3.0/3.5,4.0V DC Bias and 4.05 GHz

Slightly better at 4.05 GHz

4.05 GHz Die#1 **PA4 GHz Dmode Fall06 TQPED** 4.0V ; 34 mA

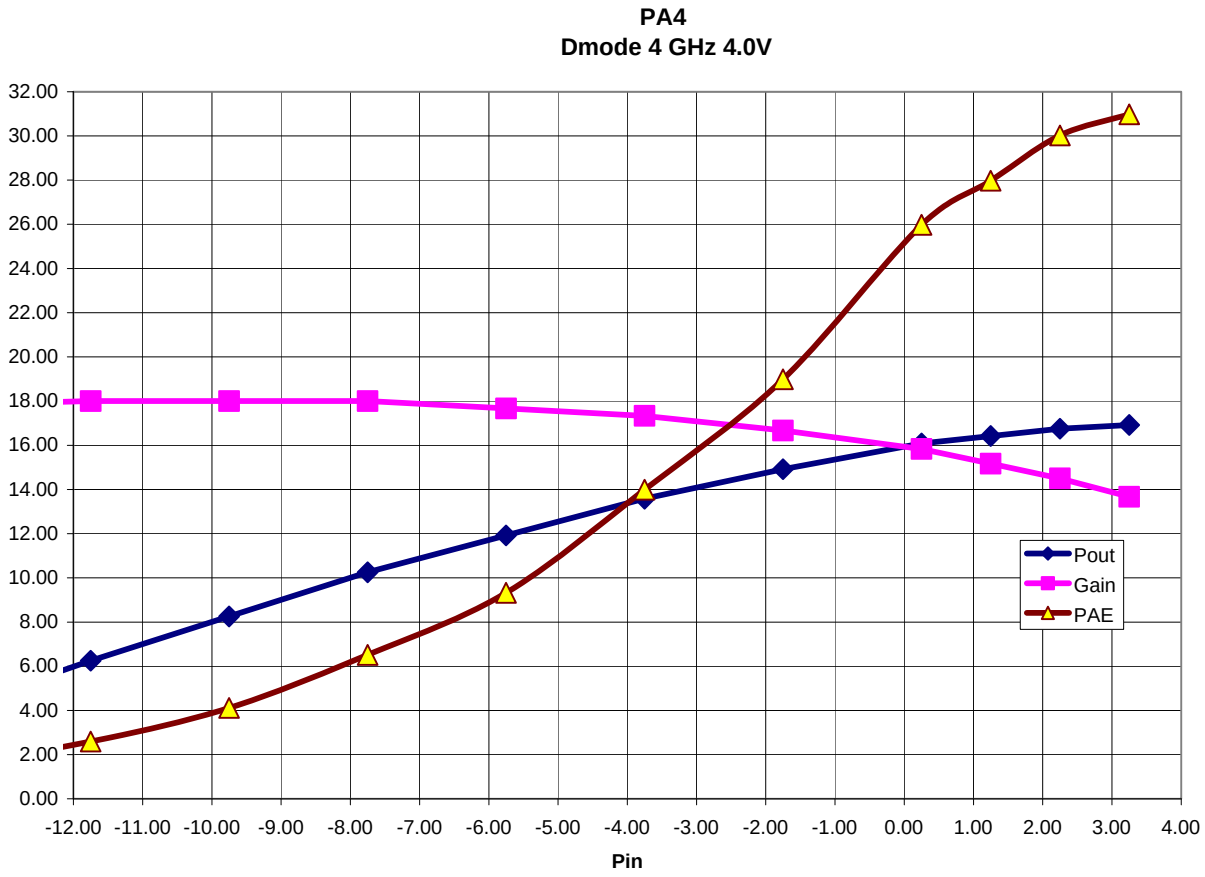
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(4.0V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-10.0	4.75	-11.75	6.50	18.25	34	136.0	4.47	3.3	3.2
-8.0	6.75	-9.75	8.50	18.25	32	128.0	7.08	5.5	5.4
-6.0	8.83	-7.75	10.58	18.33	32	128.0	11.43	8.9	8.8
-4.0	10.50	-5.75	12.25	18.00	33	132.0	16.79	12.7	12.5
-2.0	12.17	-3.75	13.92	17.67	31	124.0	24.66	19.9	19.5
0.0	13.50	-1.75	15.25	17.00	33	132.0	33.50	25.4	24.9
2.0	14.58	0.25	16.33	16.08	33	132.0	42.95	32.5	31.7
3.0	14.92	1.25	16.67	15.42	32	128.0	46.45	36.3	35.2
4.0	15.00	2.25	16.75	14.50	33	132.0	47.32	35.8	34.6
5.0	15.42	3.25	**17.17**	13.92	35	140.0	**52.12**	37.2	**35.7**

4.05 GHz Die#1 **PA4 GHz Dmode Fall06 TQPED** 3.5V ; 38 mA

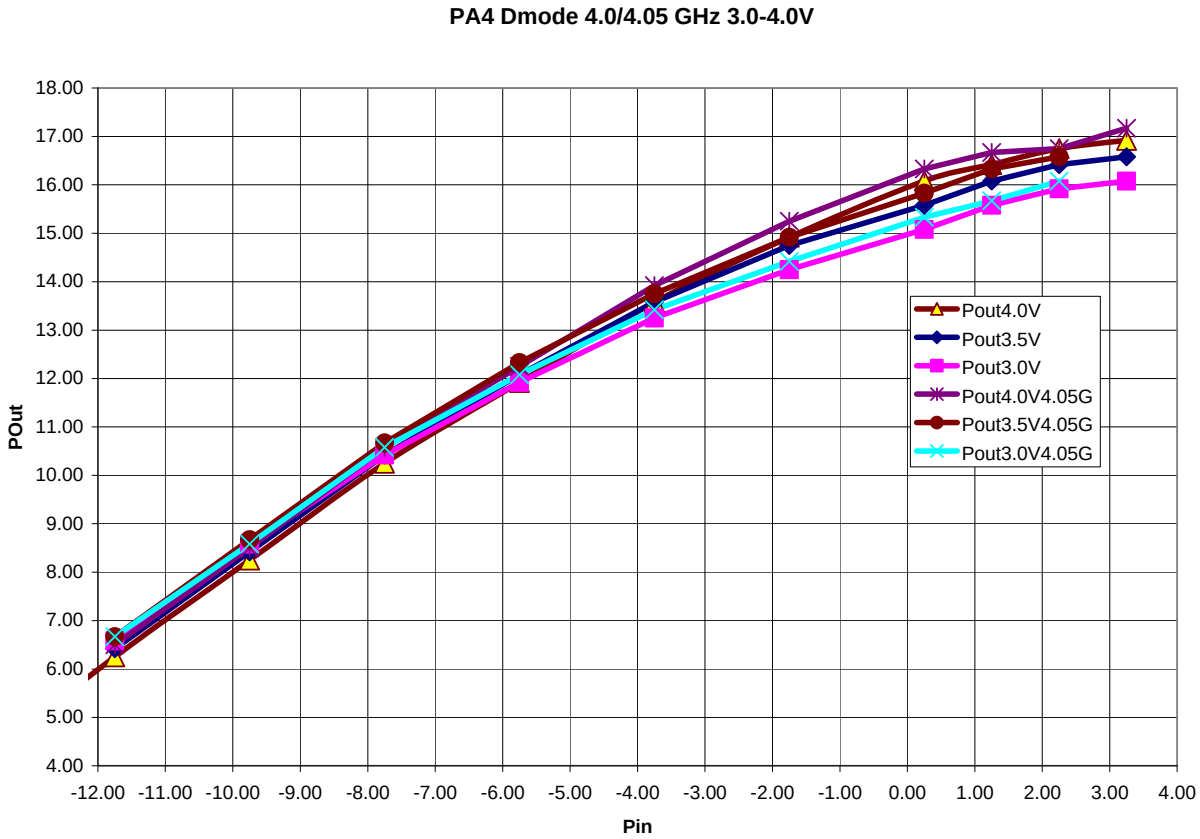
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.5V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-10.0	4.92	-11.75	6.67	18.42	38	133.0	4.65	3.5	3.4
-8.0	6.92	-9.75	8.67	18.42	38	133.0	7.36	5.5	5.5
-6.0	8.92	-7.75	10.67	18.42	38	133.0	11.67	8.8	8.6
-4.0	10.58	-5.75	12.33	18.08	38	133.0	17.10	12.9	12.7
-2.0	12.00	-3.75	13.75	17.50	37	129.5	23.71	18.3	18.0
0.0	13.17	-1.75	14.92	16.67	37	129.5	31.05	24.0	23.5
2.0	14.08	0.25	15.83	15.58	35	122.5	38.28	31.3	30.4
3.0	14.58	1.25	16.33	15.08	35	122.5	42.95	35.1	34.0
4.0	14.83	2.25	**16.58**	14.33	35	122.5	**45.50**	37.1	**35.8**

4.05 GHz Die#1 **PA4 GHz Dmode Fall06 TQPED** 3.0V ; 33 mA

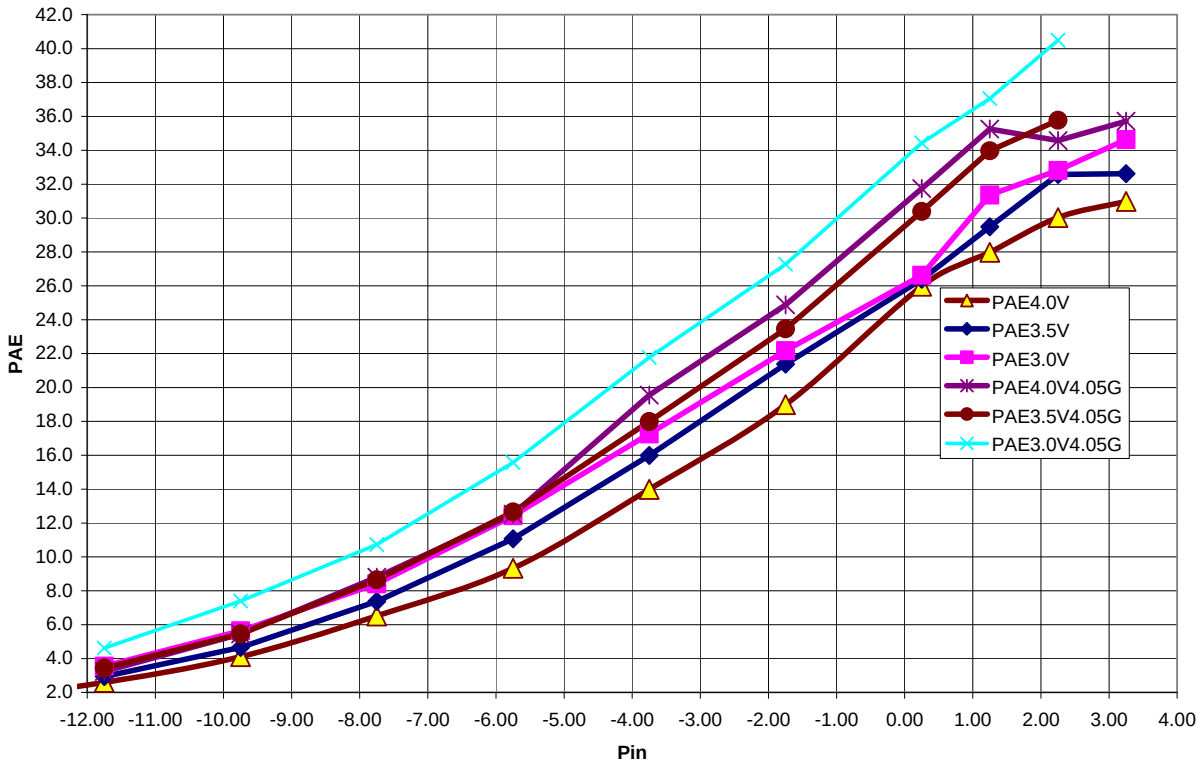
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.0V)	PDC(mw)	Pout(mw)	Drn Eff	PAE
-10.0	4.92	-11.75	6.67	18.42	33	99.0	4.65	4.7	4.6
-8.0	6.83	-9.75	8.58	18.33	32	96.0	7.21	7.5	7.4
-6.0	8.83	-7.75	10.58	18.33	35	105.0	11.43	10.9	10.7
-4.0	10.33	-5.75	12.08	17.83	34	102.0	16.14	15.8	15.6
-2.0	11.67	-3.75	13.42	17.17	33	99.0	21.98	22.2	21.8
0.0	12.67	-1.75	14.42	16.17	33	99.0	27.67	27.9	27.3
2.0	13.58	0.25	15.33	15.08	32	96.0	34.12	35.5	34.4
3.0	13.92	1.25	15.67	14.42	32	96.0	36.90	38.4	37.0
4.0	14.33	2.25	**16.08**	13.83	32	96.0	**40.55**	42.2	**40.5**



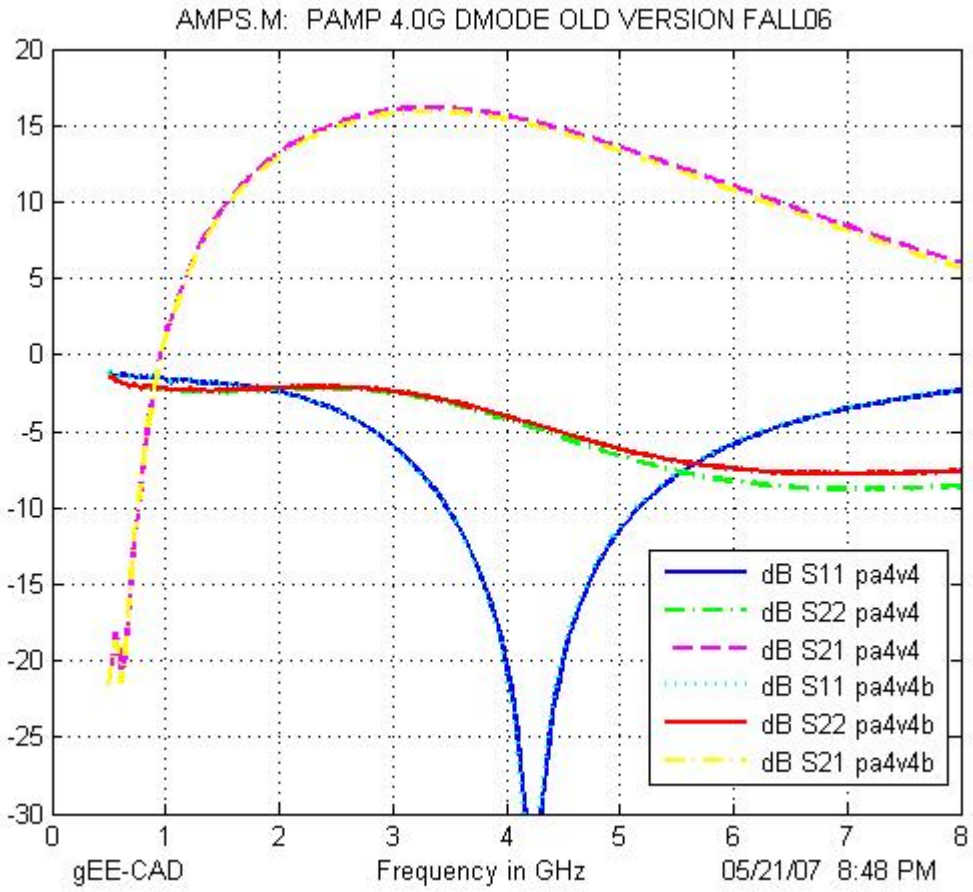
Performance (PAE, Pout, Gain) of Power Amplifier Design at 4.0V DC Bias and 4.0 GHz



Output Power of Power Amp at 3.0, 3.5, and 4.0 V and at 4.0 and 4.05 GHz



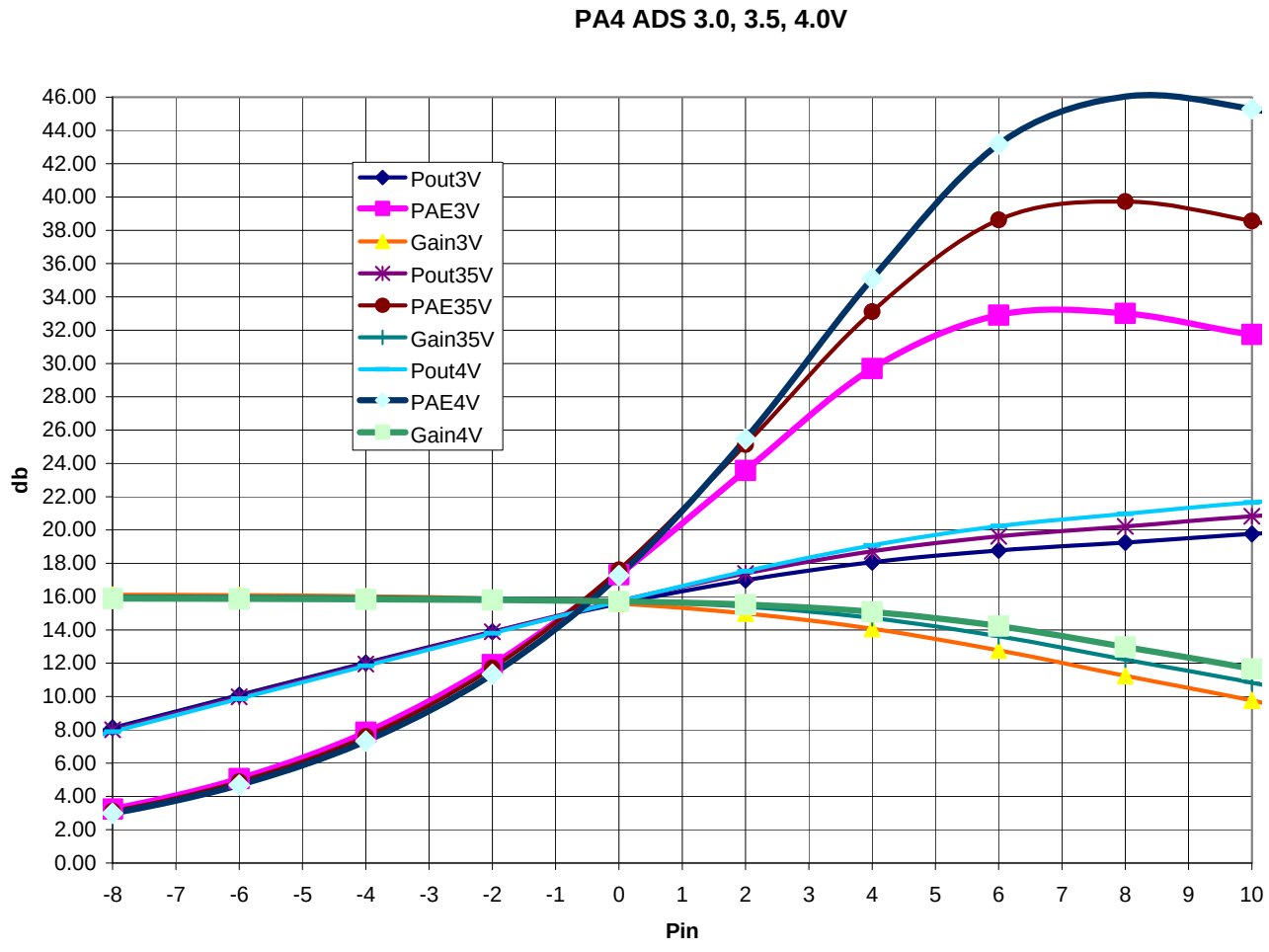
Power Added Efficiency of Power Amp at 3.0, 3.5, and 4.0 V and at 4.0 and 4.05 GHz



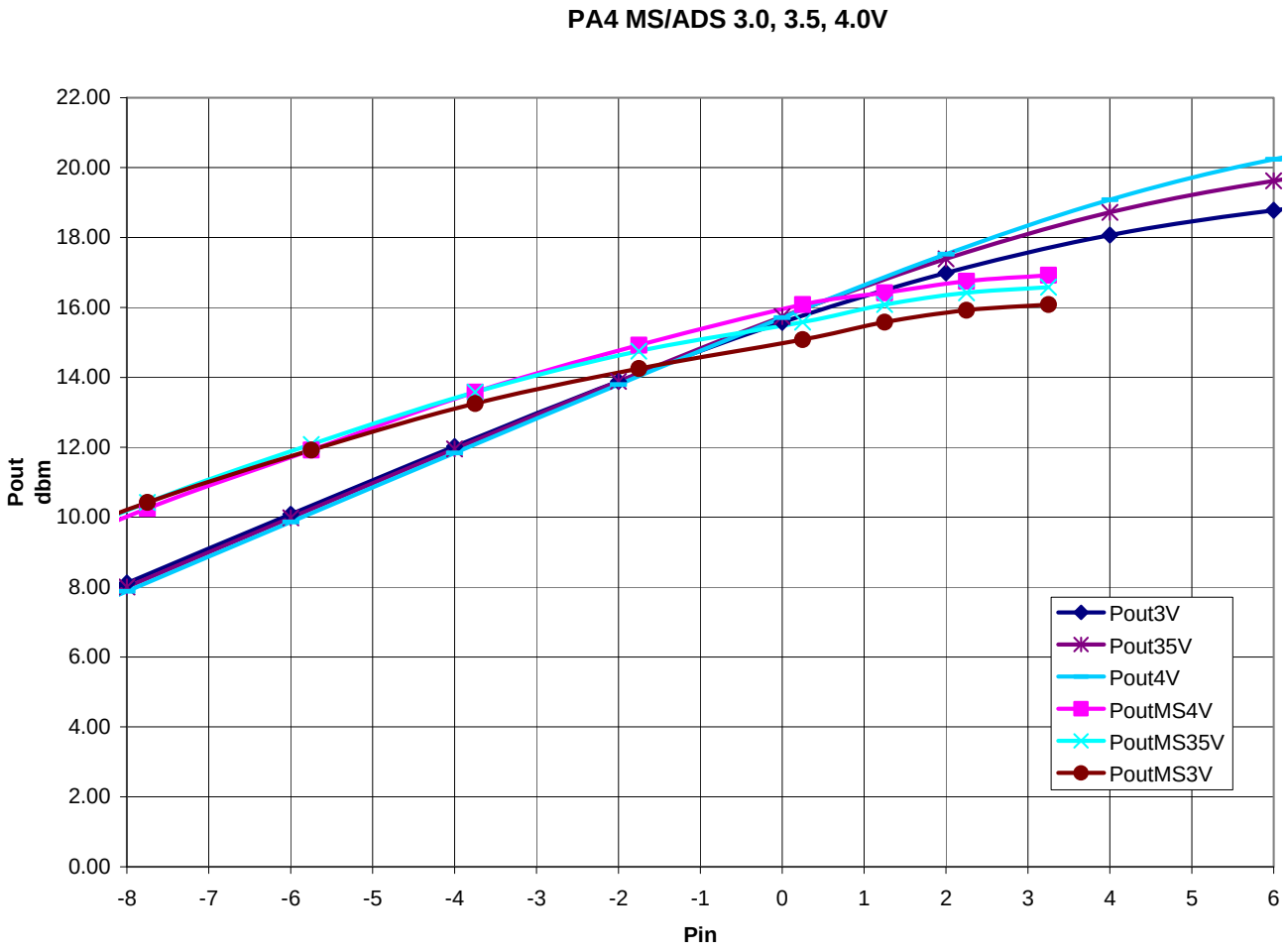
S-Parameters of Power Amplifier Design at 4.0V DC Bias for 2 Die

ADS Simulations PA4	3.0V			3.5V			4.0V		
RFpower	dBm(Vout[1],5	PAE1	P_gain_transduc	dBm(Vout[:	PAE1	P_gain_transduc	dBm(Vout[:	PAE1	P_gain_tra
-10.00	6.13	2.06	16.13	6.01	1.97	16.01	5.89	1.89	15.89
-8.00	8.12	3.24	16.12	8.00	3.11	16.00	7.88	2.98	15.88
-6.00	10.08	5.07	16.08	9.98	4.88	15.98	9.87	4.68	15.87
-4.00	12.02	7.85	16.02	11.95	7.61	15.95	11.84	7.32	15.84
-2.00	13.88	11.91	15.88	13.88	11.72	15.88	13.80	11.33	15.80
0.00	15.58	17.31	15.58	15.74	17.61	15.74	15.71	17.27	15.71
2.00	16.99	23.58	14.99	17.39	25.14	15.39	17.52	25.47	15.52
4.00	18.07	29.69	14.07	18.72	33.12	14.72	19.08	35.10	15.08
6.00	18.78	32.91	12.78	19.62	38.63	13.62	20.24	43.17	14.24
8.00	**19.25**	**33.01**	**11.25**	**20.22**	**39.73**	**12.22**	**20.97**	**46.03**	**12.97**
10.00	19.77	31.75	9.77	20.83	38.56	10.83	21.66	45.28	11.66

ADS Non-Linear Performance Simulations of PA 4.0 GHz 3.0/3.5/4.0V DC Bias



ADS vs. Measured Pout for PA4 at 3.0/3.5/4.0V DC Bias

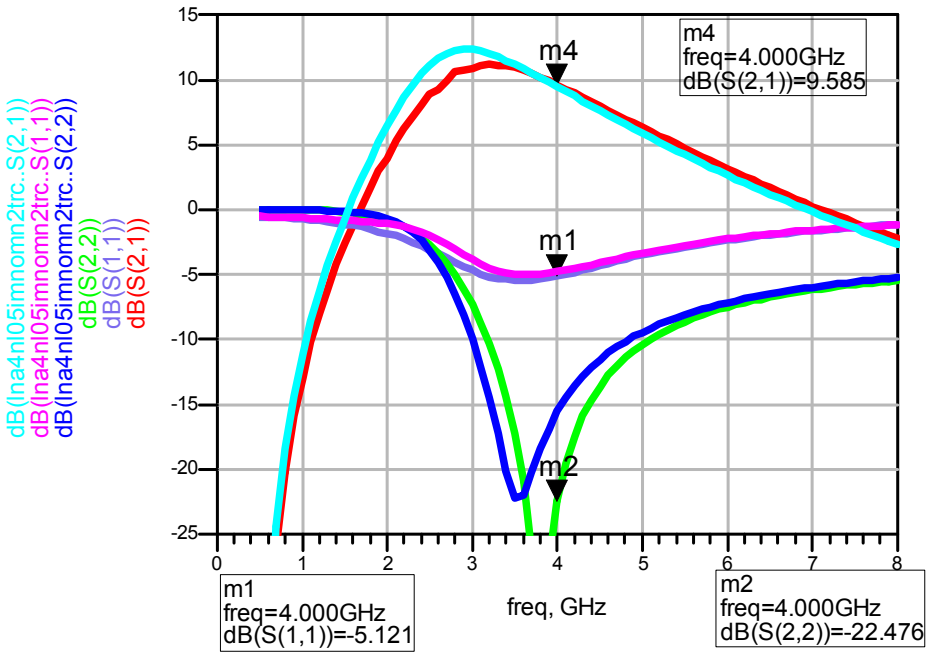


Gain is actually slightly higher in the measured data by about 2 dB but does not vary much with DC bias from 3.0 to 4.0 V. The non-linear models over estimate Output Power. Actual Measurements show better Power Added Efficiency at 3.0 V rather than 4.0V but simulations show the PAE increasing with voltage from 3 to 4 V. Output Power does decrease with lower DC bias as expected but the compression starts earlier and saturates much sooner than expected with increasing input power.

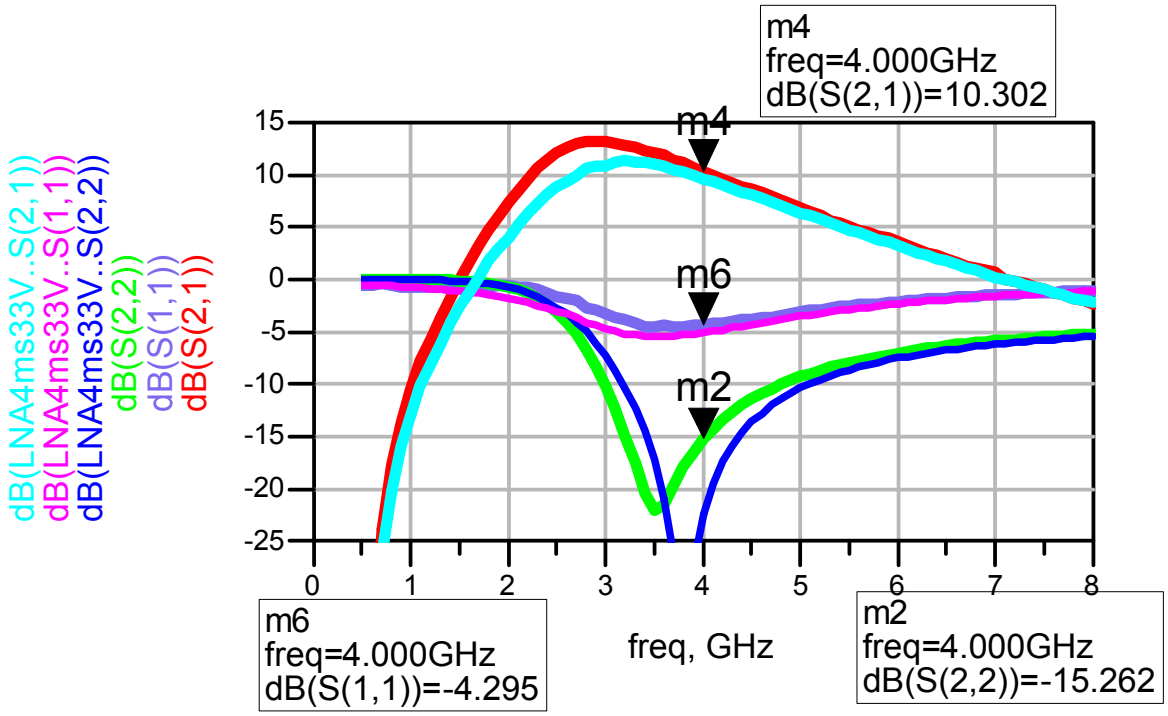
	ADS			Meas		
Summary	GainSS	P3dB	PAE3dB**	GainSS	P3dB	PAE3dB**
3.0V	16.13	18.65	32.60	18.33	15.00	26.00
3.5V	16.01	19.75	39.00	18.17	15.75	28.00
4.0V*	15.89	21.00	46.00	18.17	16.42	28.00

* 4.0V was the design voltage

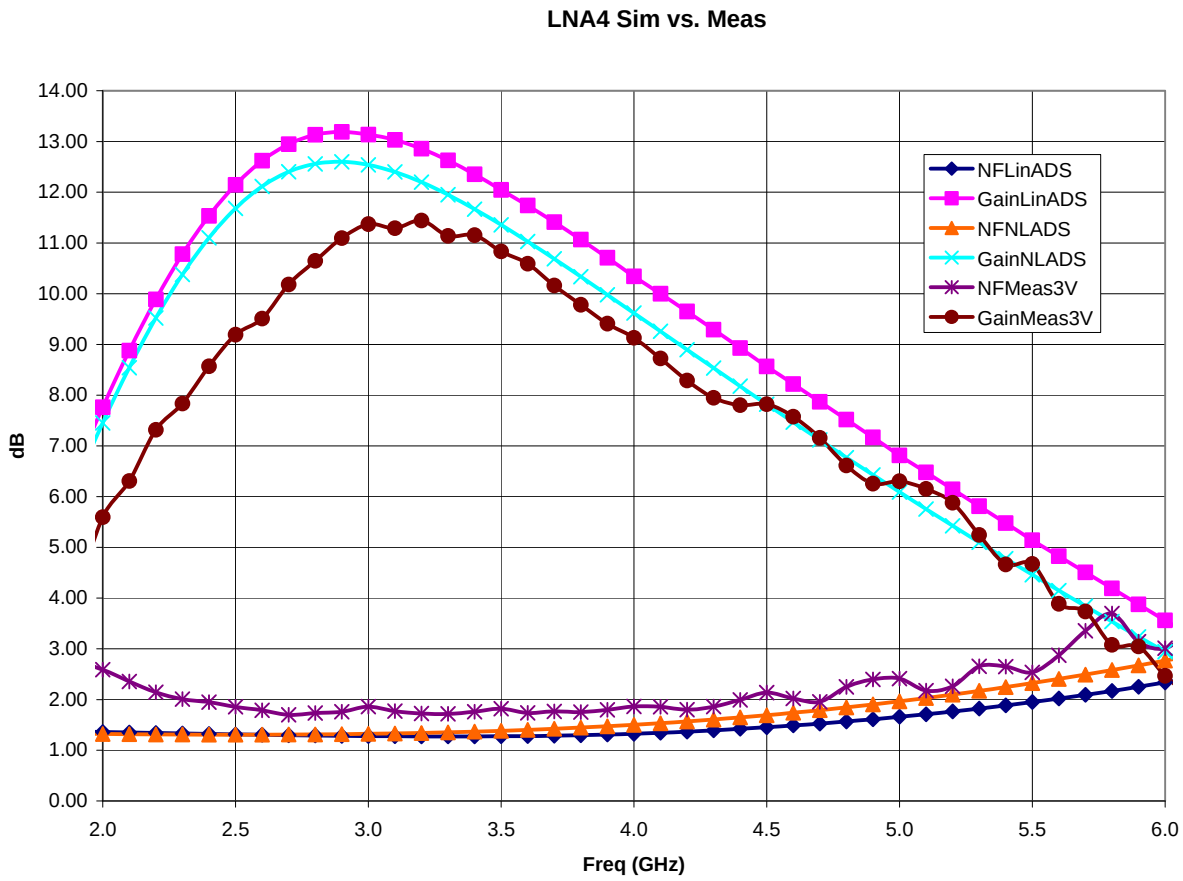
**Best PAE is not necessarily at 3dB, in fact at the lower DC bias voltages, PAE and Pout increase and peak closer to 5 dB compression. If compression is allowed past 3 dB, actual PAE improves as the voltage drops from 4 to 3 V which is the opposite of the model predictions.



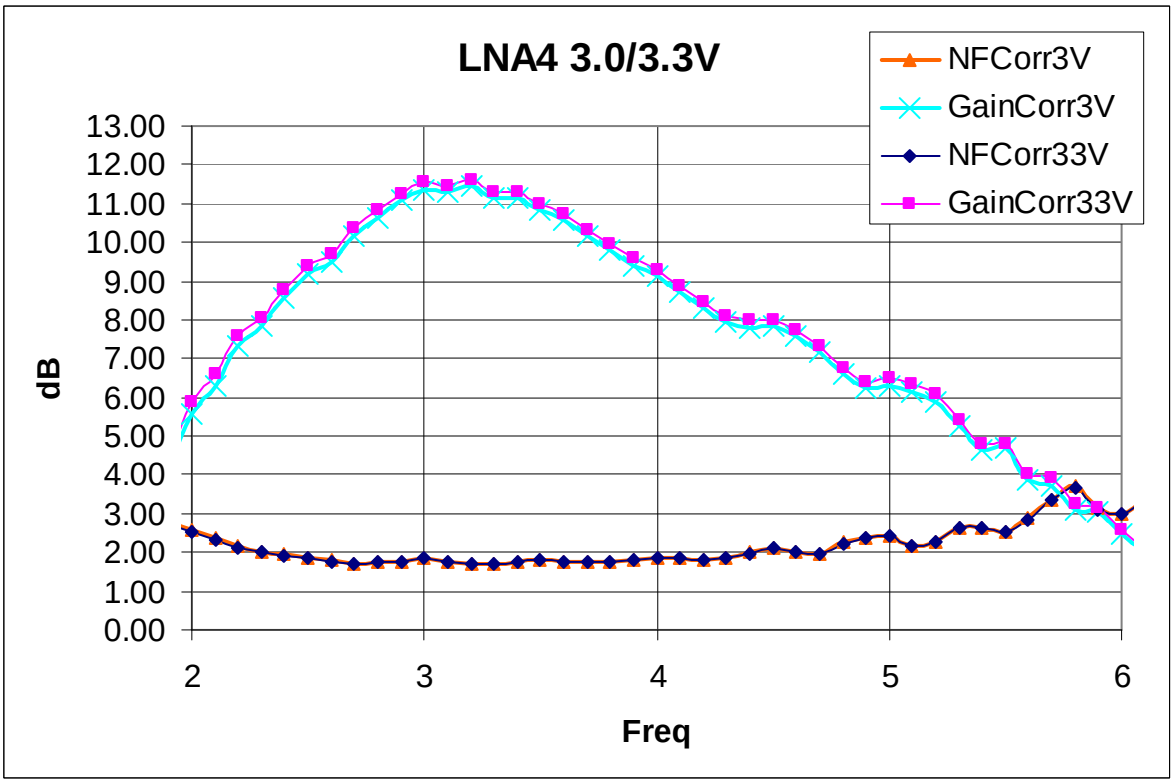
Measured S-Parameters vs. ADS Simulation of Low Noise Amplifier Design at 3.0/3.3V DC Bias



Similar Agreement: Re-Simulated with device data (S-parameters for LNA at 3.3V)



Predicted Noise Figure and Gain of LNA versus Measured (Lin and NonLin ADS Model)



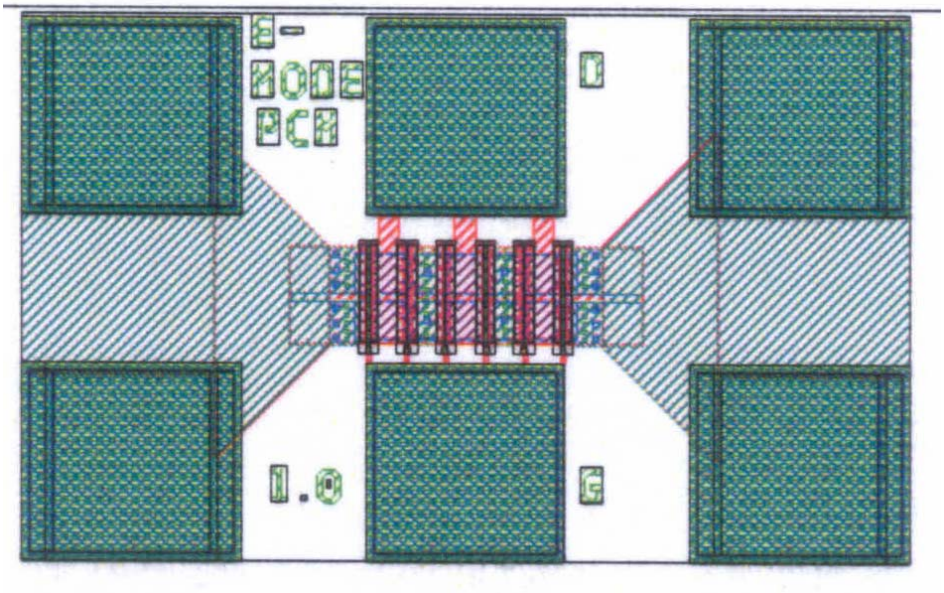
Measured LNA Performance (Gain & NF) at 3.0 V, 12 mA and 3.3V, 15 mA DC Bias

Class Test Devices: Dmode and Emode 300 um PHEMTs

Several test structures were measured. There was very good agreement between given s-parameters and measured 300 um Dmode and Emode PHEMTs.

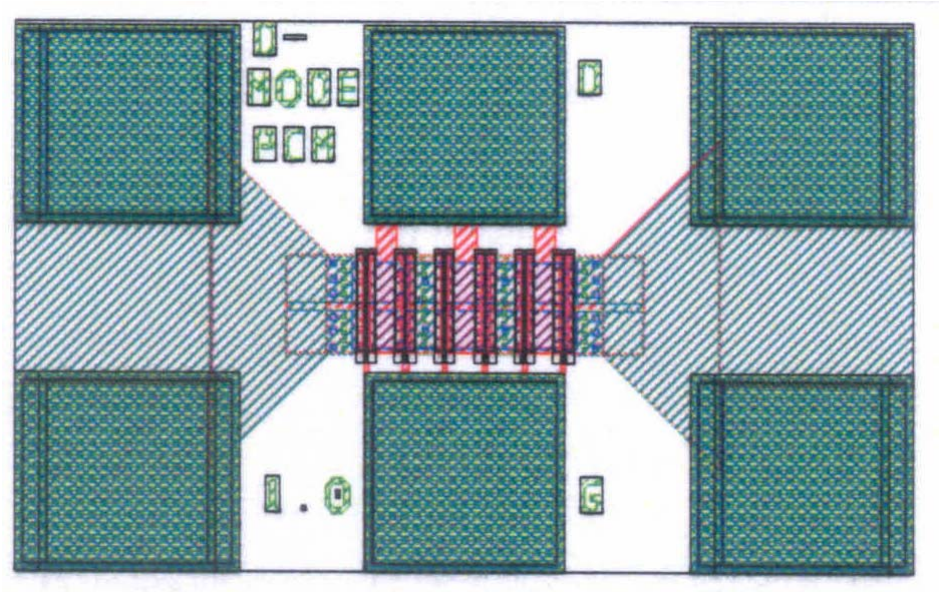
DC Biases for the Emode were:

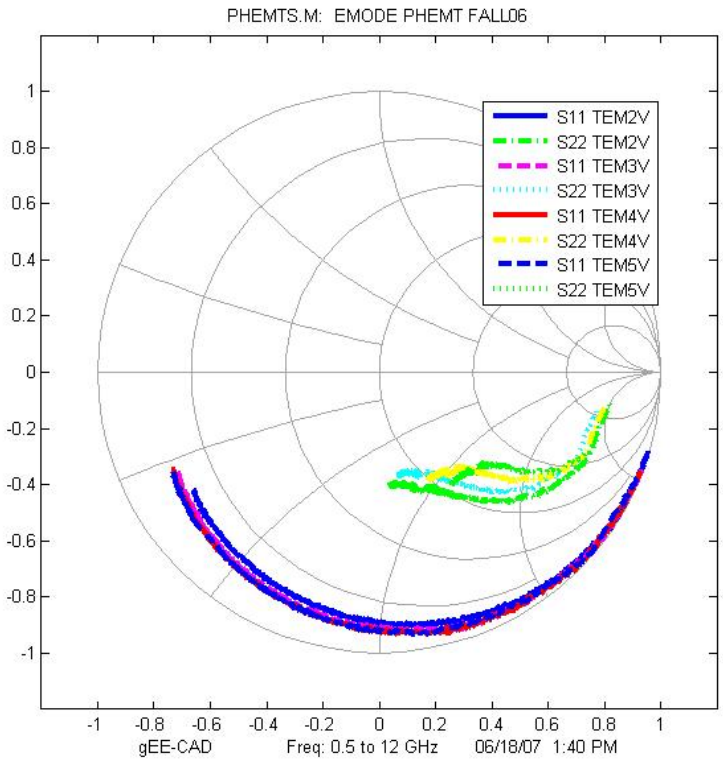
2V @ 9-10 mA	VG = +0.5V	TEM2V
3V @ 23 mA	VG = +0.6V	TEM3V
3.3V @ 9-10 mA	VG = +0.49V	TEM33V
4V @ 32 mA	VG = +0.65V	TEM4V
5V @ 33 mA	VG = +0.65V	TEM5V



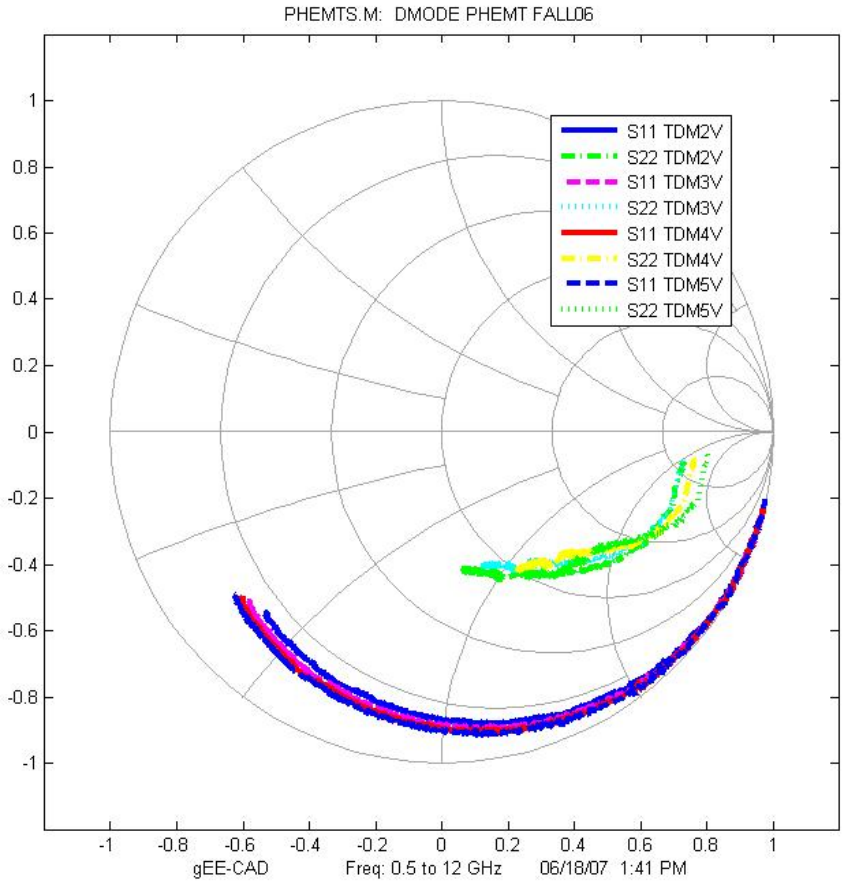
DC Biases for the Dmode were:

2V @ 13 mA	VG = -0.7V	TDM2V
3V @ 24 mA	VG = -0.6V	TDM3V
3.3V @ 15 mA	VG = -0.7V	TDM33V
4V @ 35 mA	VG = -0.5V	TDM4V
5V @ 45 mA	VG = -0.45V	TDM5V

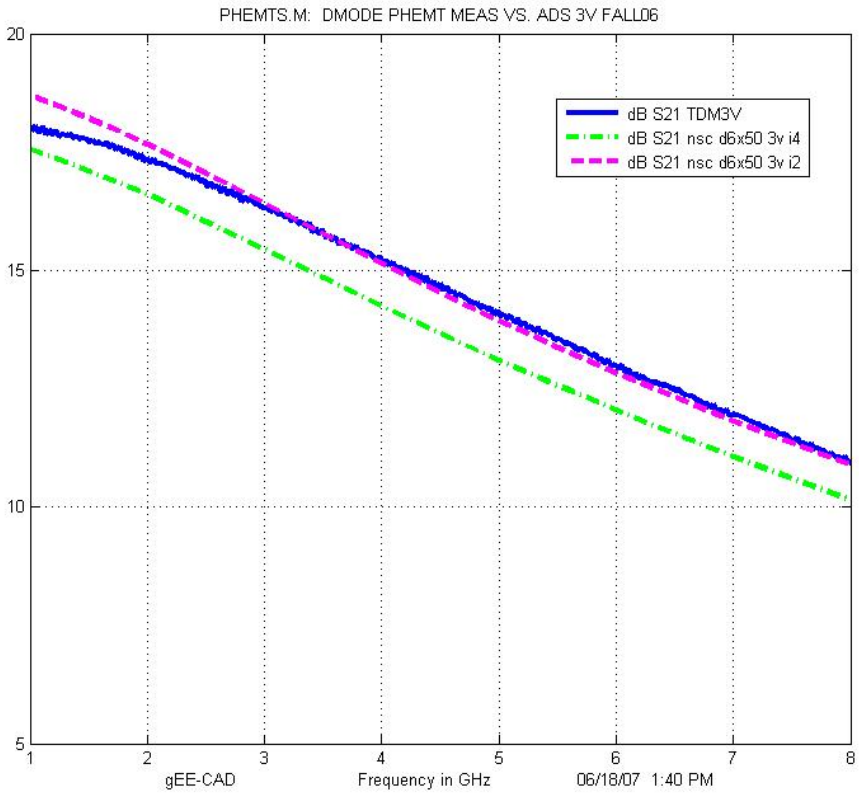




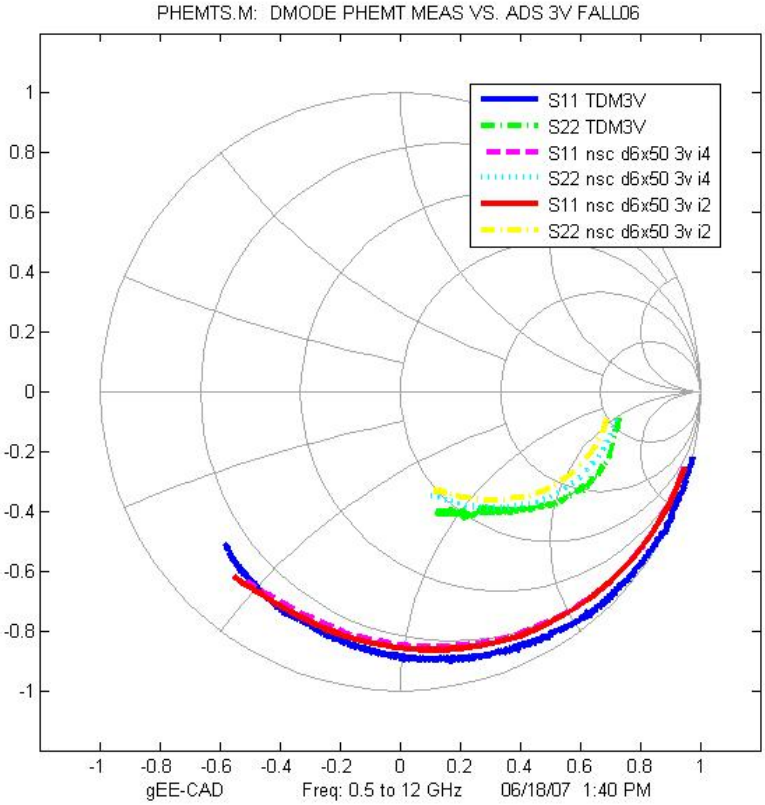
Emode Match 2V to 5V



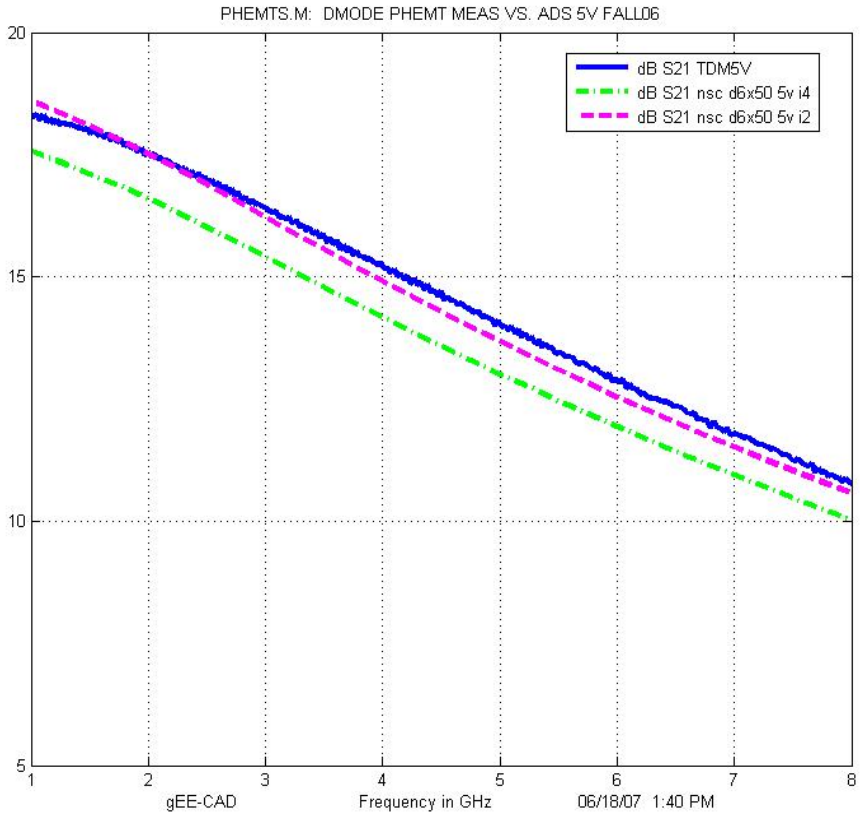
Dmode Match 2V to 5V



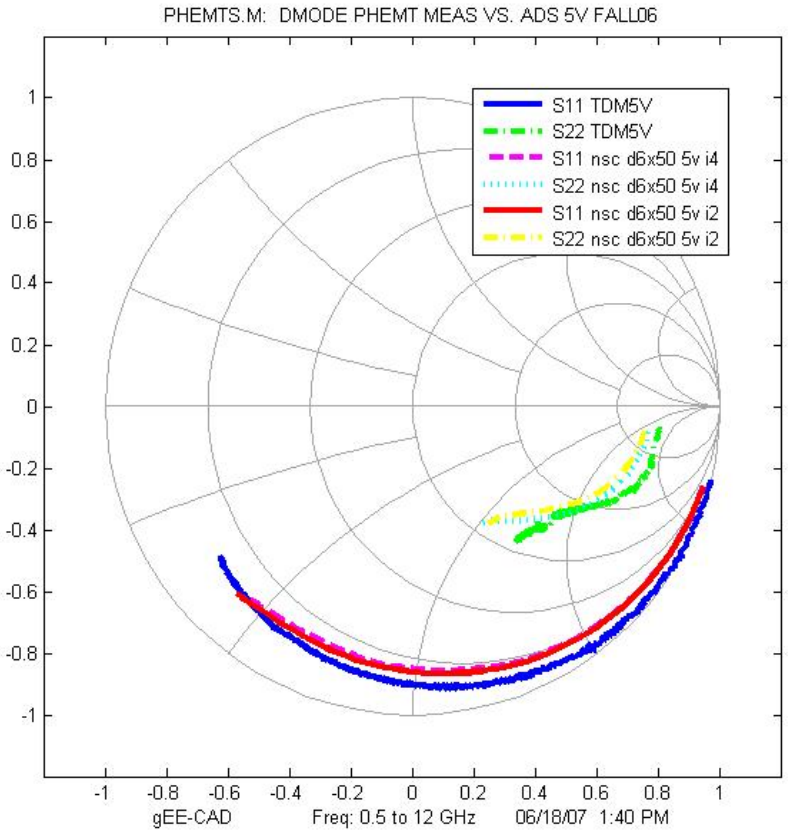
Dmode Gain S21 3V Measured vs. Linear TQS Files



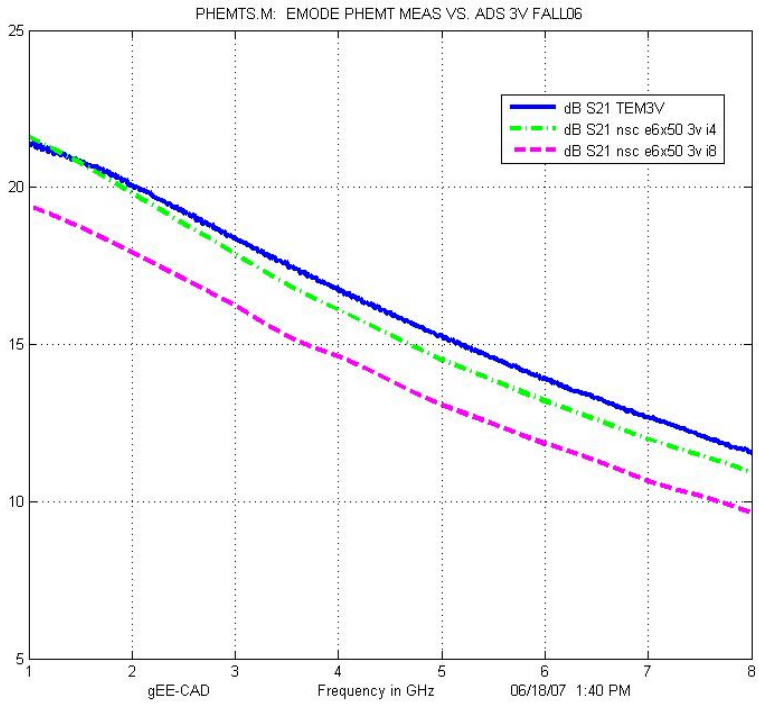
Dmode Match S11/S22 3V Measured vs. Linear TQS Files



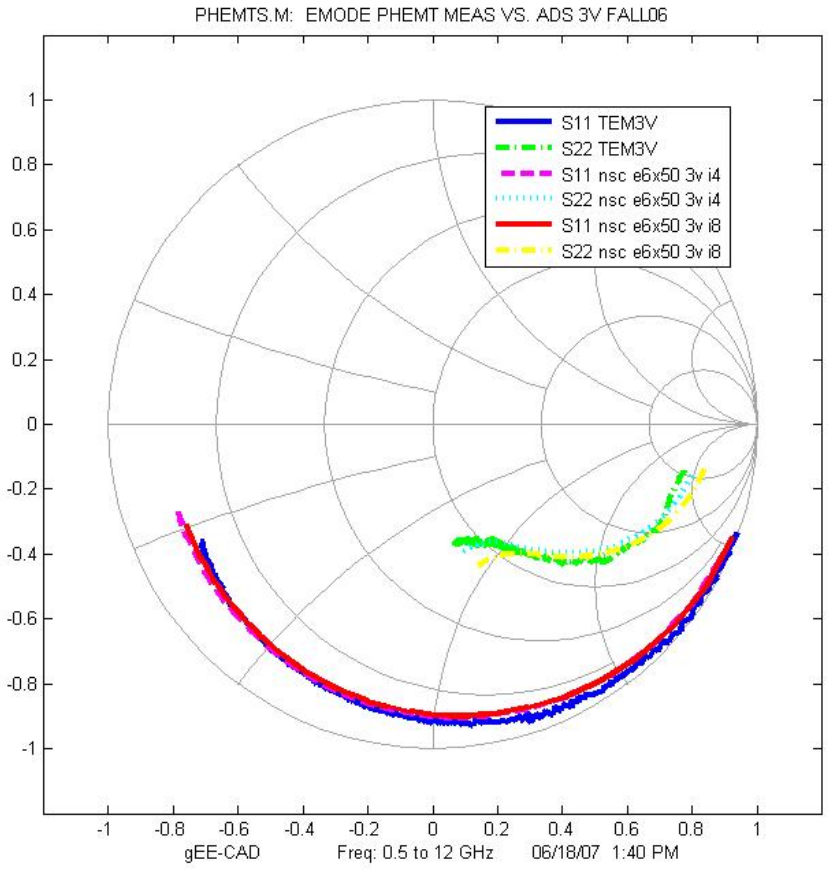
Dmode Gain S21 5V Measured vs. Linear TQS Files



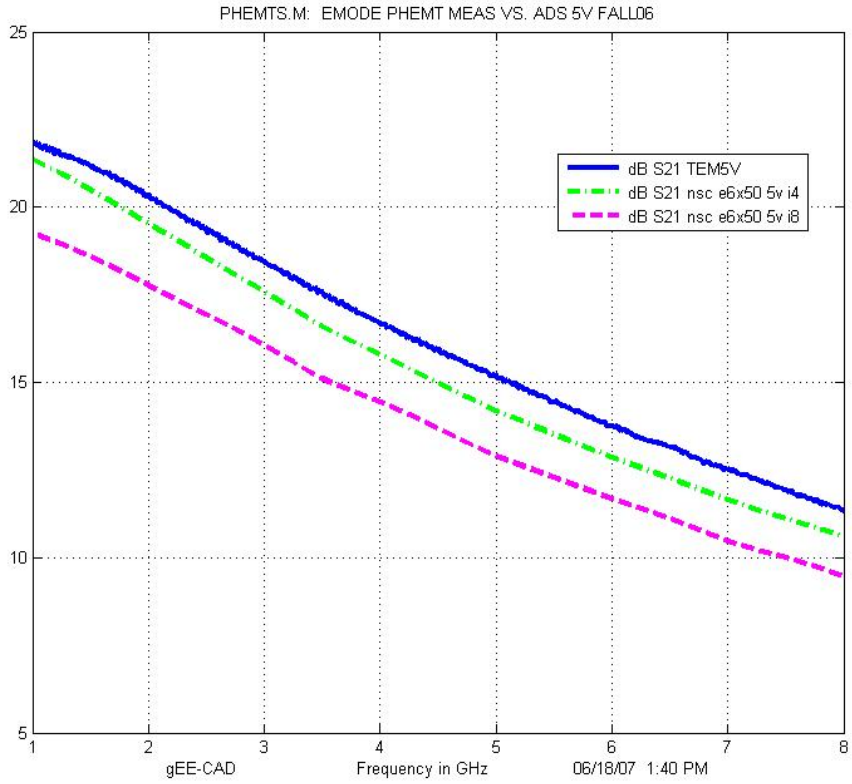
Dmode Match S11/S22 5V Measured vs. Linear TQS Files



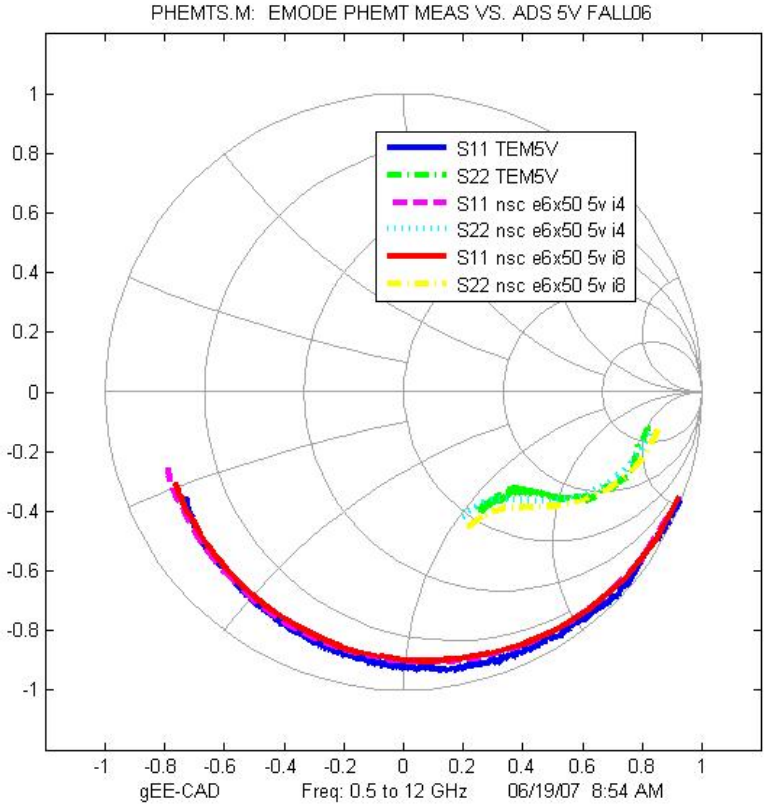
Emode Gain S21 3V Measured vs. Linear TQS Files



Emode Match S11/S22 3V Measured vs. Linear TQS Files



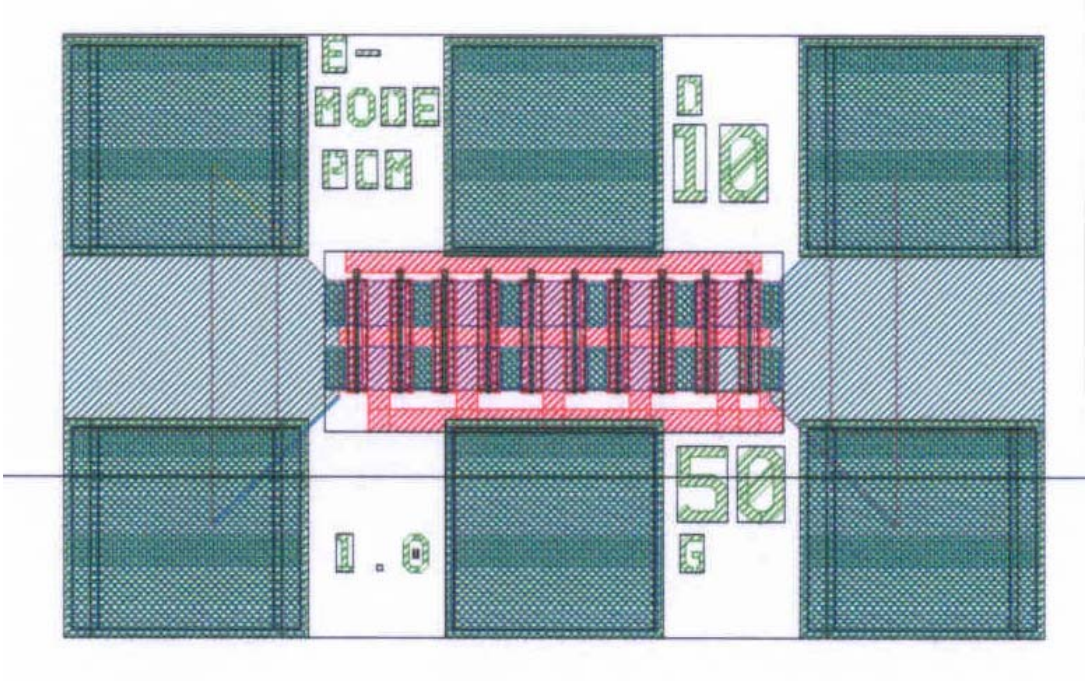
Emode Gain S21 5V Measured vs. Linear TQS Files



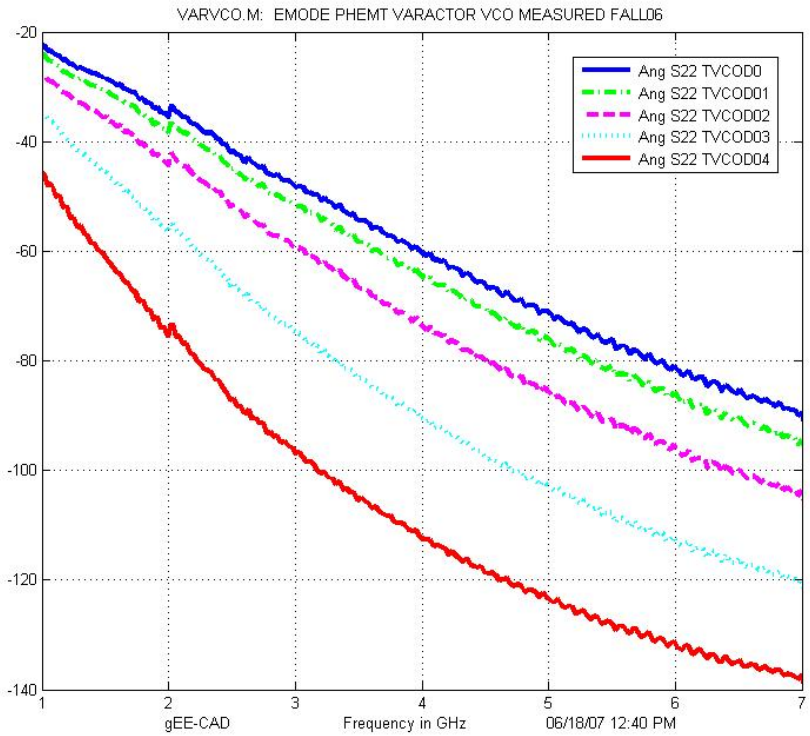
Emode Match S11/S22 5V Measured vs. Linear TQS Files

VCO Varactor Test Circuit Measurements (EMode 0 to 0.4V)

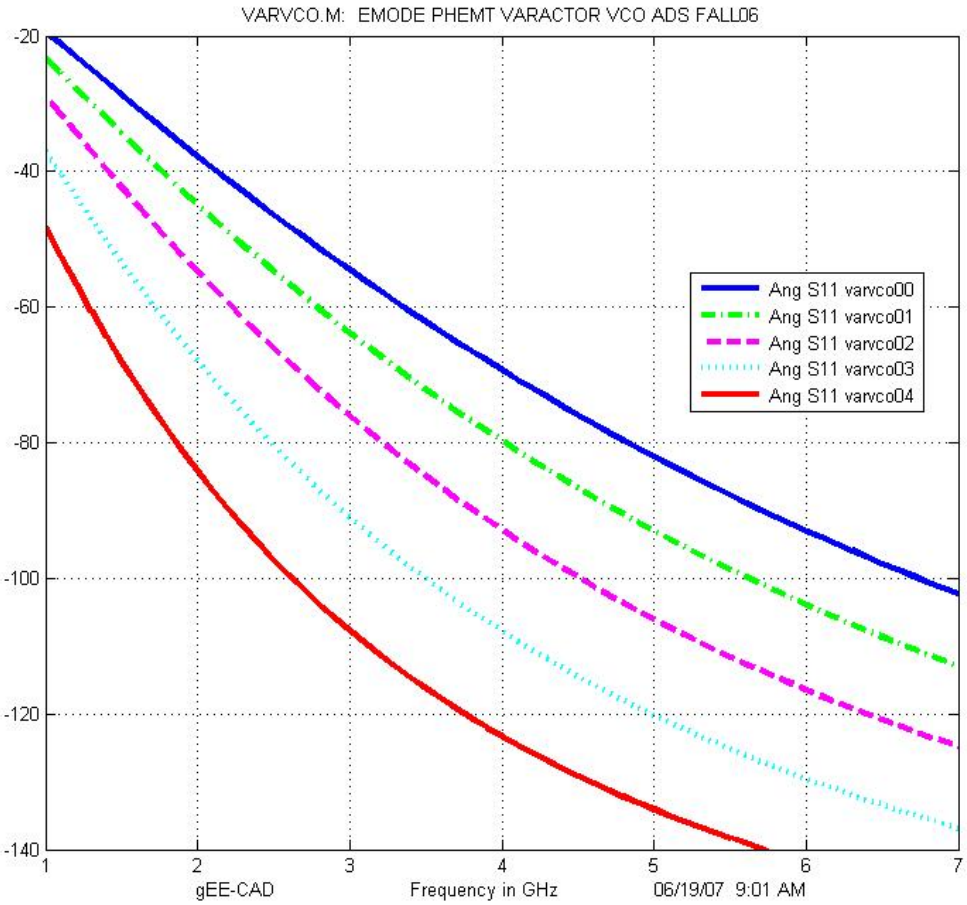
The varactor used for D. Loizos VCO design was measured as a test cell. There was very good agreement between simulated (ADS) and measured data from 0V to 0.4V, the desired tuning range for the VCO design.



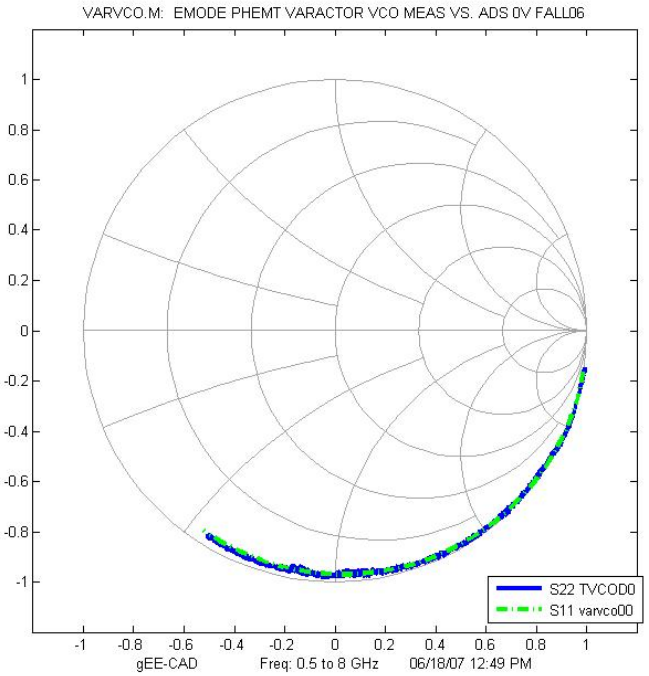
Varactor Test Cell Layout (500 um)



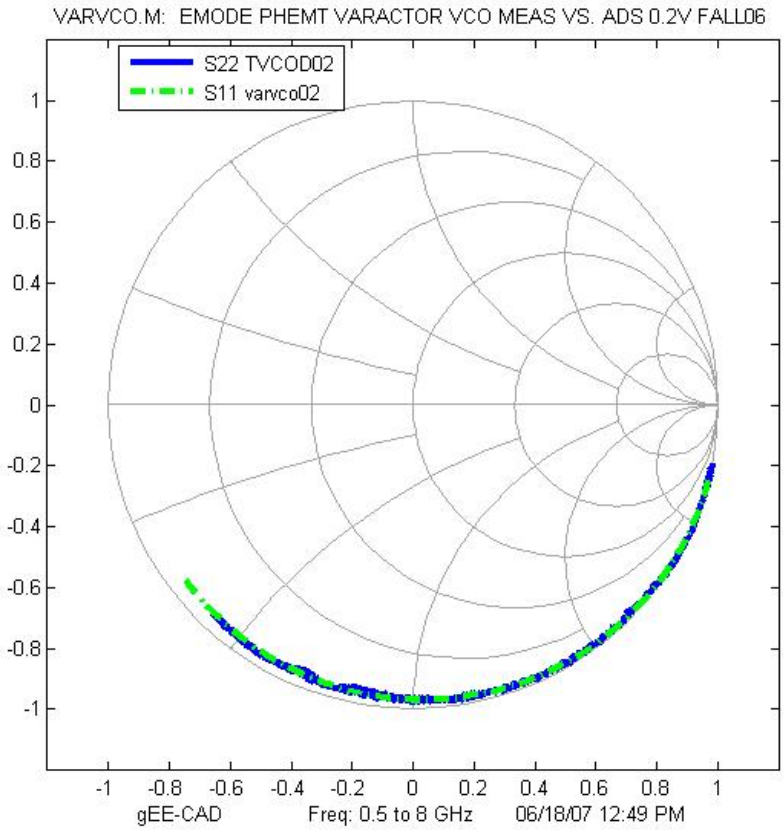
Phase of Emode Varactor Diode (VCO) to Ground, Measured 0V to 0.4V



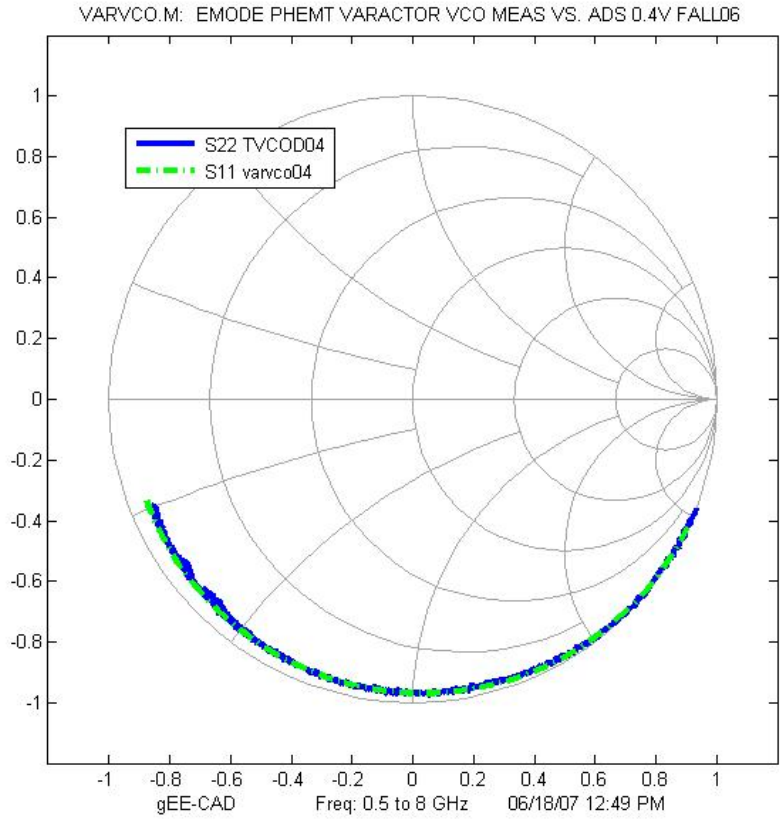
Phase of Emode Varactor Diode (VCO) to Ground, Measured 0V to 0.4V



Measured Vs. Simulated Varactor (VCO) at 0V



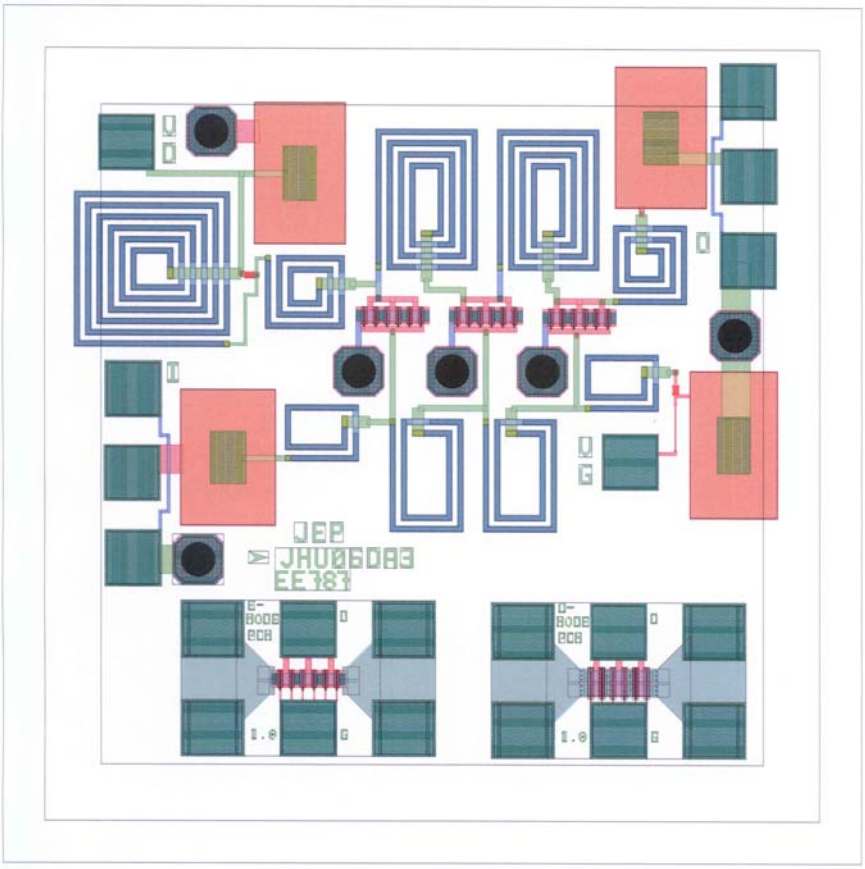
Measured Vs. Simulated Varactor (VCO) at 0.2V

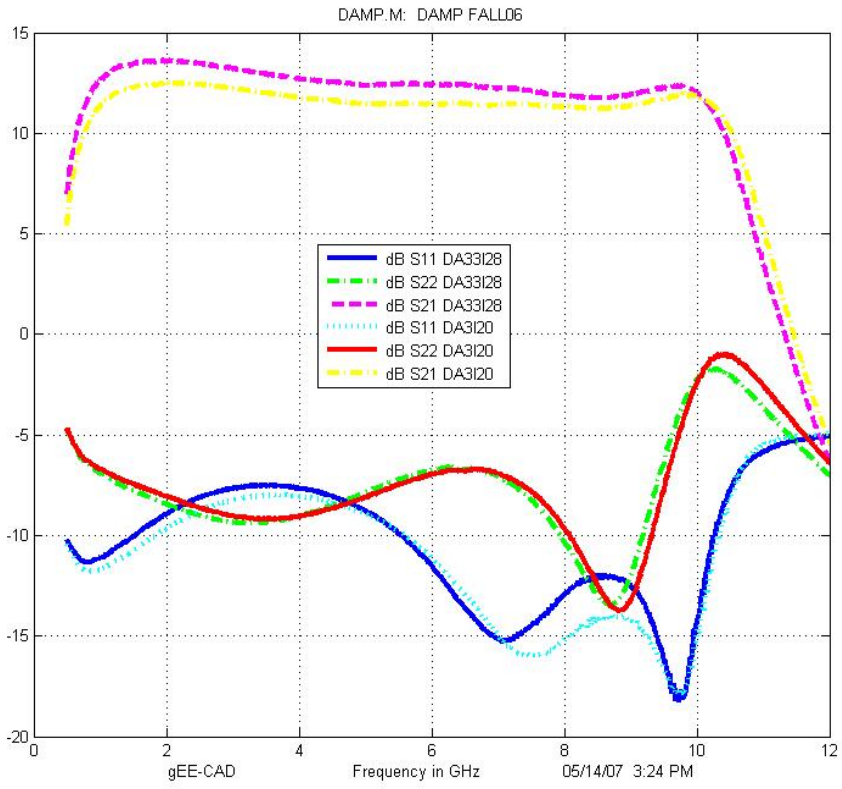


Measured Vs. Simulated Varactor (VCO) at 0.4V

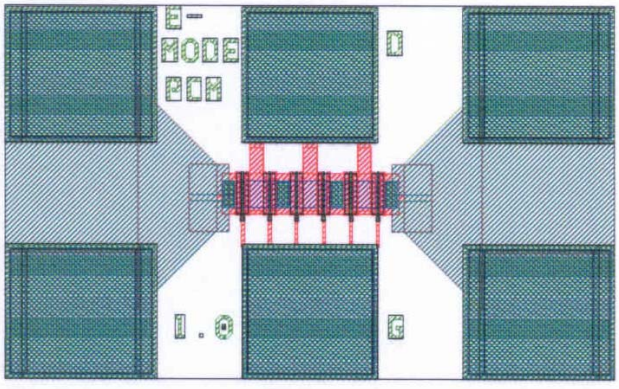
Other Circuits: Distributed Amplifier (John Penn)

There were some other test structures and designs included in the Fall 06 JHU Tile. An updated Distributed Amplifier Design using the 0.5 um PHEMTs had a very good gain response from 1 to 10 GHz. It was designed for battery operation and was measured at 3 V @ 28 mA and 3.3V @ 33 mA.

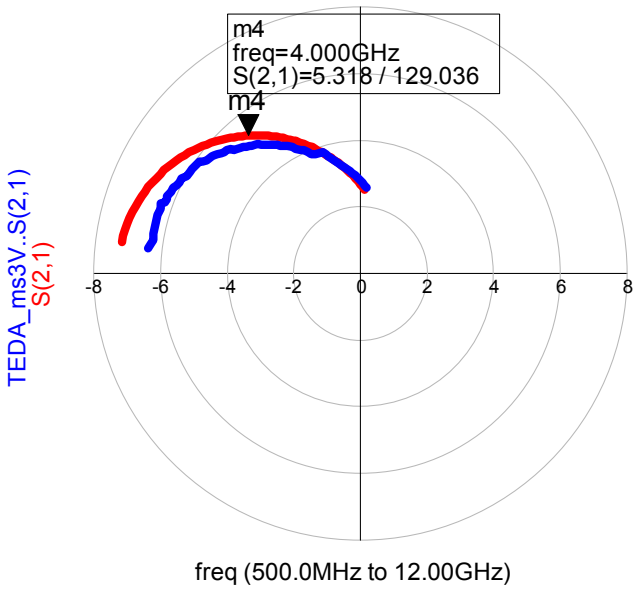




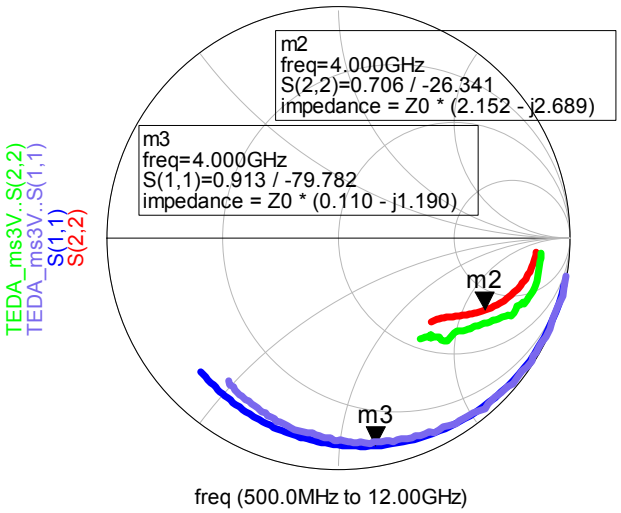
Layout of Distributed Amplifier with Test Cells and Measured S-Parameters



6x30um PHEMT (DA)



S21



S11/S22

Simulated “nominal” Emode 0.5 um PHEMT for a 6x30 um device agrees well with measurements