JHU EE787 Fall 2007 MMIC Results

Designs Fabricated by TriQuint Semiconductor

ADS Support by Gary Wray—Agilent

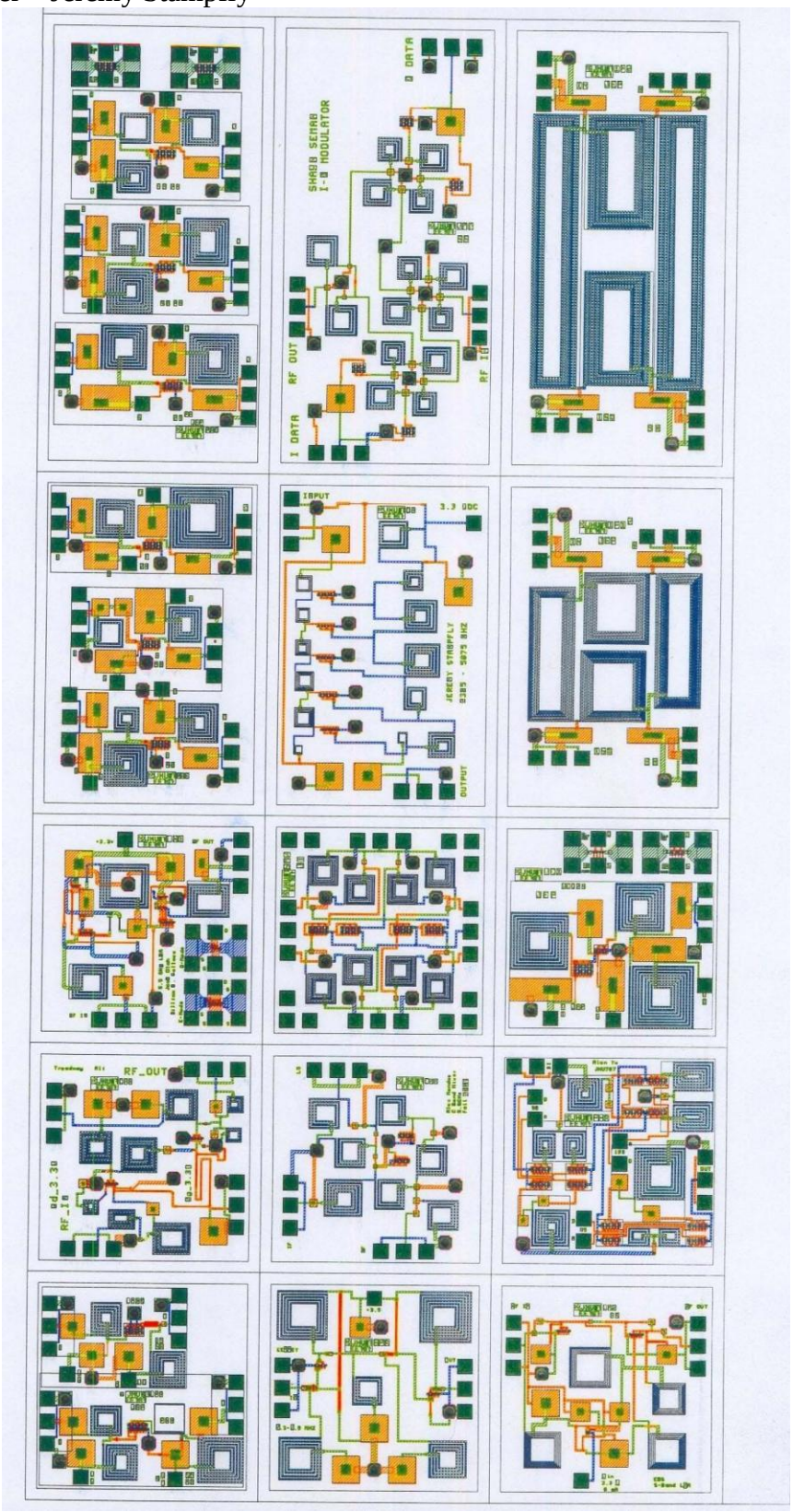
TriQuint TQPED Library, and ADS software used for student designs

Nine MMICs were designed by students for the Fall 2007 JHU MMIC Design. The intent was to design low DC power consumption components (ie. Battery powered) for use with the S-band or C-band wireless communications service (WCS) or industrial, scientific, and medical (ISM) frequencies. All designs were tested in the late Spring of 2008 after fabrication by TriQuint Semiconductor. The MMIC measurements compare favorably to simulations; overall, the designs were very successful. A couple of connection errors cropped up in the designs but were found and hopefully will be re-fabricated in future years with the repairs. All designs used TriQuint's TQPED process with 0.5 um PHEMTs. Most of the designs worked well and are documented following. Overall, DC biases and small signal parameters were close to simulations. Output powers tended to be several dB below predictions for the amplifier designs.

Thanks again to TriQuint, and Agilent for their wonderful support of the JHU EE787 MMIC Design Course.

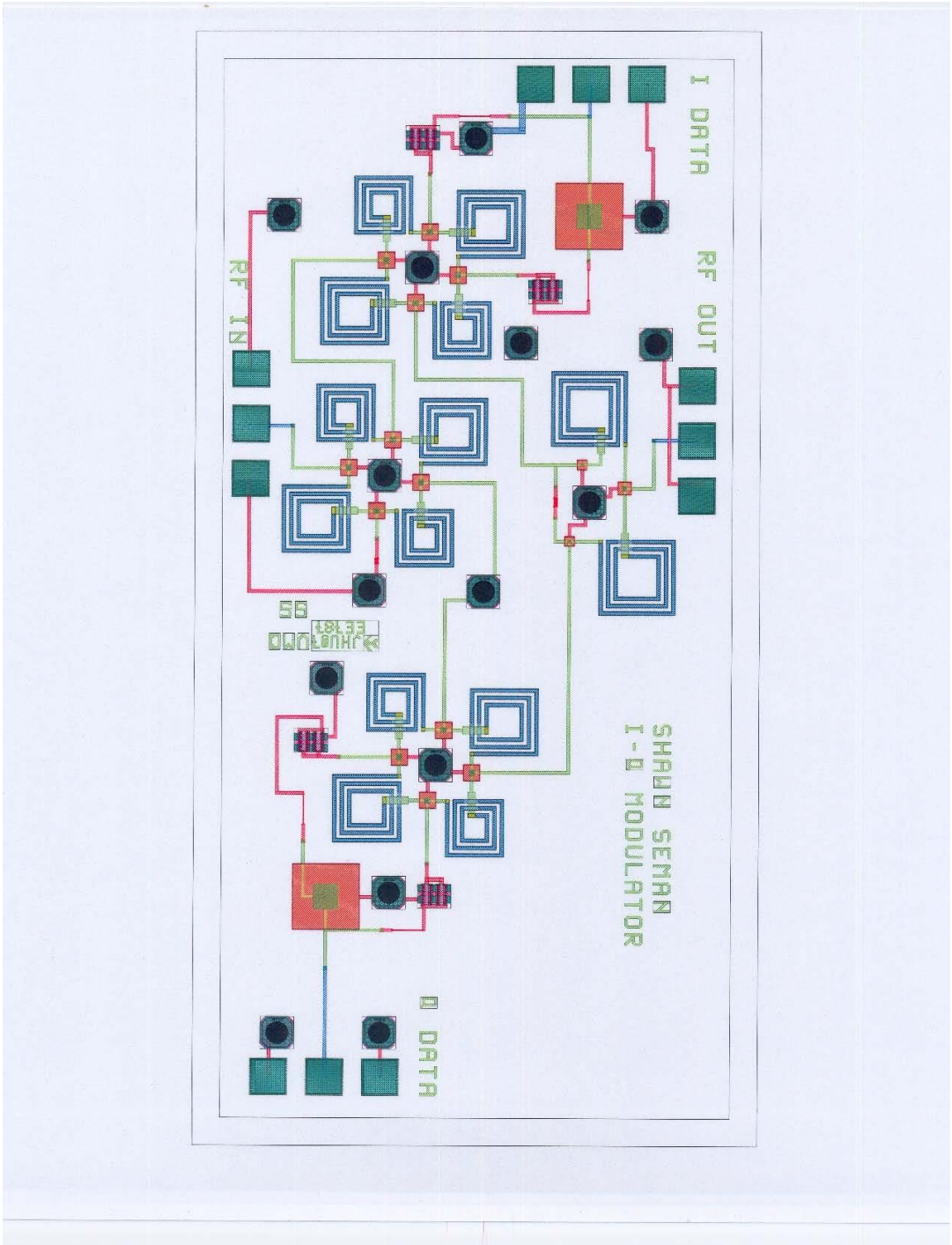
Fall 2007 JHU EE787 MMIC Design Student Projects
Supported by TriQuint, and Agilent Eesof

Low Noise Amplifier C-band—J. Olah & B. Wallace
Phase Shifter – Alan Yu
Mixer S-Band – John Tinsley
Power Amplifier C-band – J. Treadway & Syed Ali
Broadband Amplifier – Jeremy Stampfly
Low Noise Amplifier S-band-E. Simcoe
Mixer C-Band – Alex Mendes
Power Amplifier S-band – D. Kenney
Vector Modulator C-band– Shawn Seman

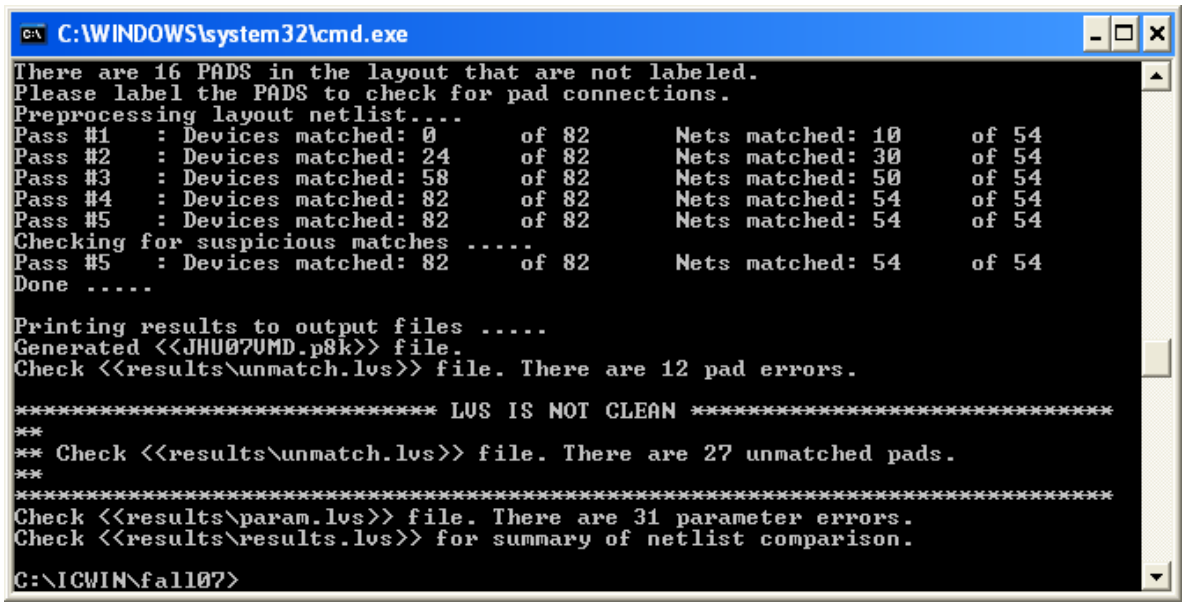


Shawn Seman – Vector Modulator

A C-Band Vector Modulator was designed for the 5150 to 5350 MHz WLAN and 5725 to 5875 MHz ISM bands. During testing, a mistake in the layout was discovered. The PHEMT in the "I" attenuator closest to the large capacitor in the upper right of the plot, does not have a ground connection. The original layout had a metal0 line from the PHEMT to the substrate via next to it, but it appears that in massaging the layout, the trace must have been deleted inadvertantly. It even passed the LVS checks because of the way substrate vias are handled. When the substrate via was labeled, the LVS check notes that the via labeled "P6" does not have any connections. Hopefully the corrected design can be re-fabbed with a future MMIC Design class fabrication.



Plot of JHU07VMD (Note missing connection at upper right between substrate via and PHEMT):

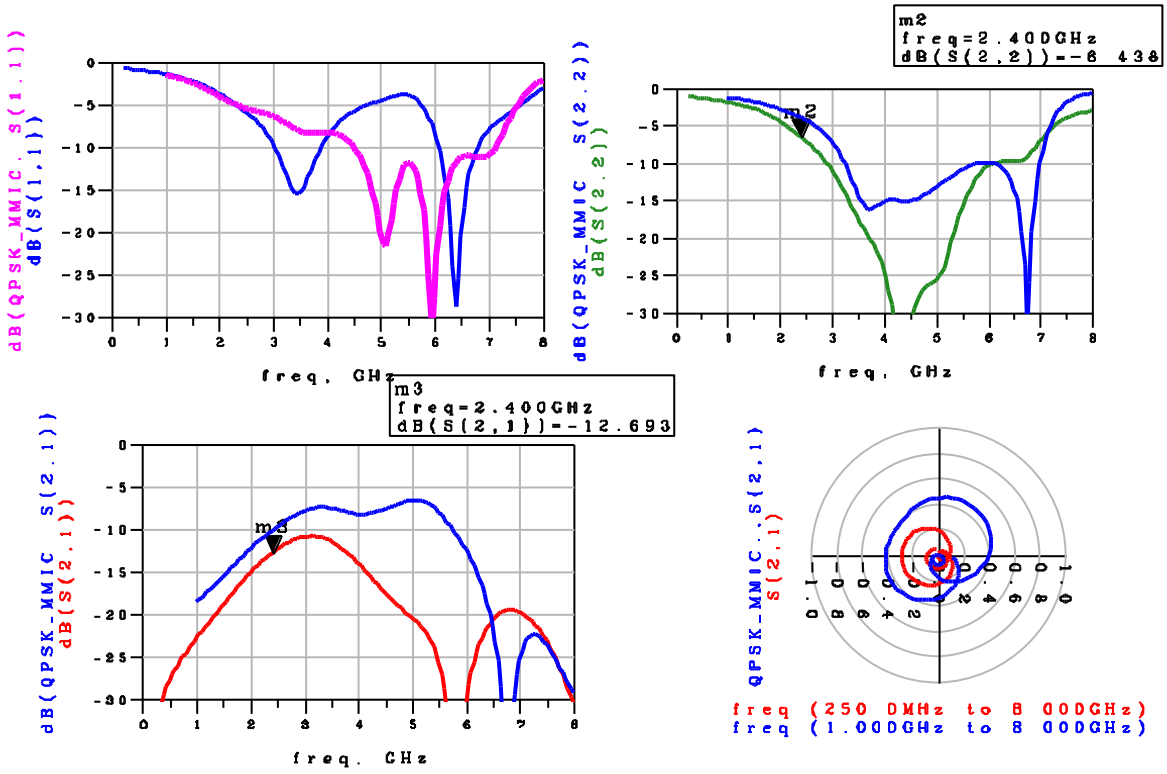


Re-running the LVS check after labeling the substrate via P6 seems to indicate no errors.

An examination of the results file shows that P6 is noted as unconnected.

```
##########################################################################
##      PAD connections are missing for following LAYOUT nets       ##
##              **MISSING PAD CONNECTIONS**              ##
##########################################################################

        LAYOUT NET          |     MATCHED SCHEMATIC NET
                            |
                            |
# :1                        |
59                          | P6
                            |
```



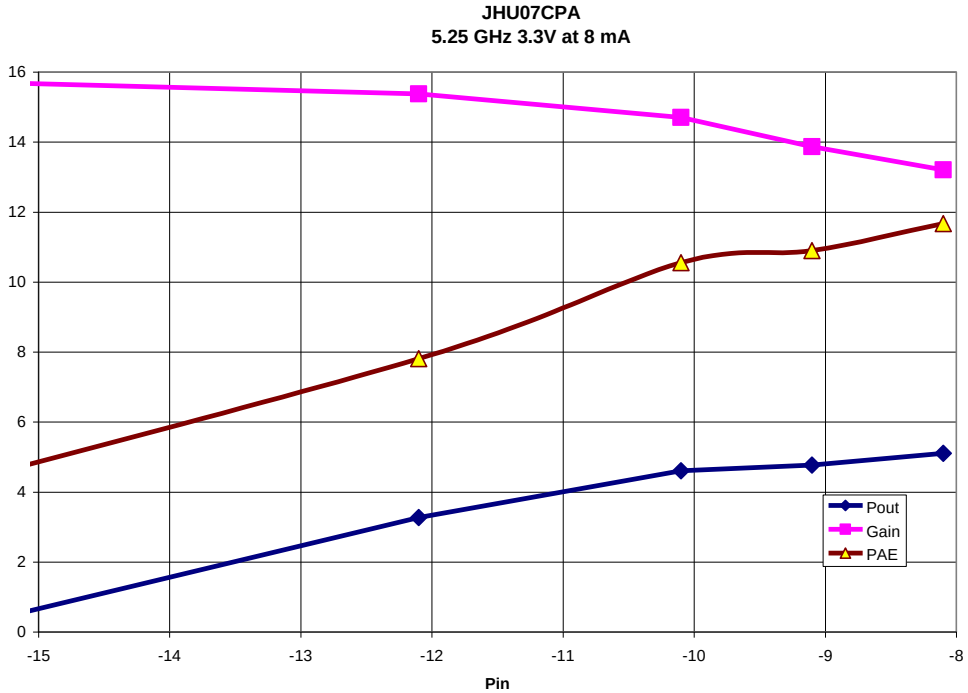
Measured Vector Modulator versus Simulation with missing connection. (+0.5V I/Q)

Medium Power Amp C-band -- Jacob Treadway & Syed Ali

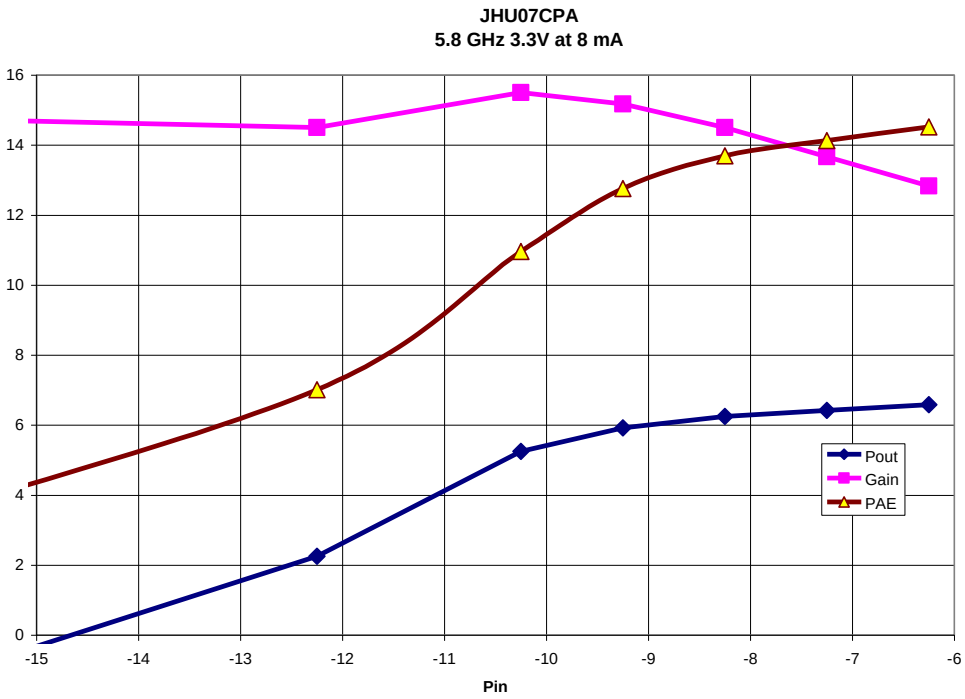
A C-Band Medium Power Amplifier was designed for operation from 5.15 GHz to 5.875 GHz. This design uses two stages of amplification to achieve good gain. Measured output power, gain, PAE, and s-parameters are following: The design was optimized for 3.3V at 10 mA on the drain and a resistor divider was used to provide the correct gate voltage from a 3.3V supply. When measured, it appeared that the drain current was a little low at 5 mA which might be due to the PHEMT threshold voltage being a little bit higher for this fab run. Gain improved when the gate voltage was increased so that the drain current was 10 mA, as designed. A voltage of 4.0V, rather than 3.3V, on the resistor divider network provided good performance. Following are s-parameters for two die that were virtually identical and non-linear performance measurements. Note the very flat gain bandwidth..

5.25 GHz	Die#1	**JHU07CPA Fall07 TQPED**				3.3V ; 8 mA	VG=4V; 1mA		
Pin(SG)	**Pout(SA)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I1(3.3V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-15.0	-3.33	-17.10	-1.23	15.87	8	26.4	0.75	2.9	2.8
-10.0	1.17	-12.10	3.27	15.37	8	26.4	2.12	8.0	7.8
-8.0	2.50	-10.10	4.60	14.70	8	26.4	2.88	10.9	10.6
-7.0	2.67	-9.10	4.77	13.87	8	26.4	3.00	11.4	10.9
-6.0	3.00	-8.10	5.10	13.20	8	26.4	3.24	12.3	11.7

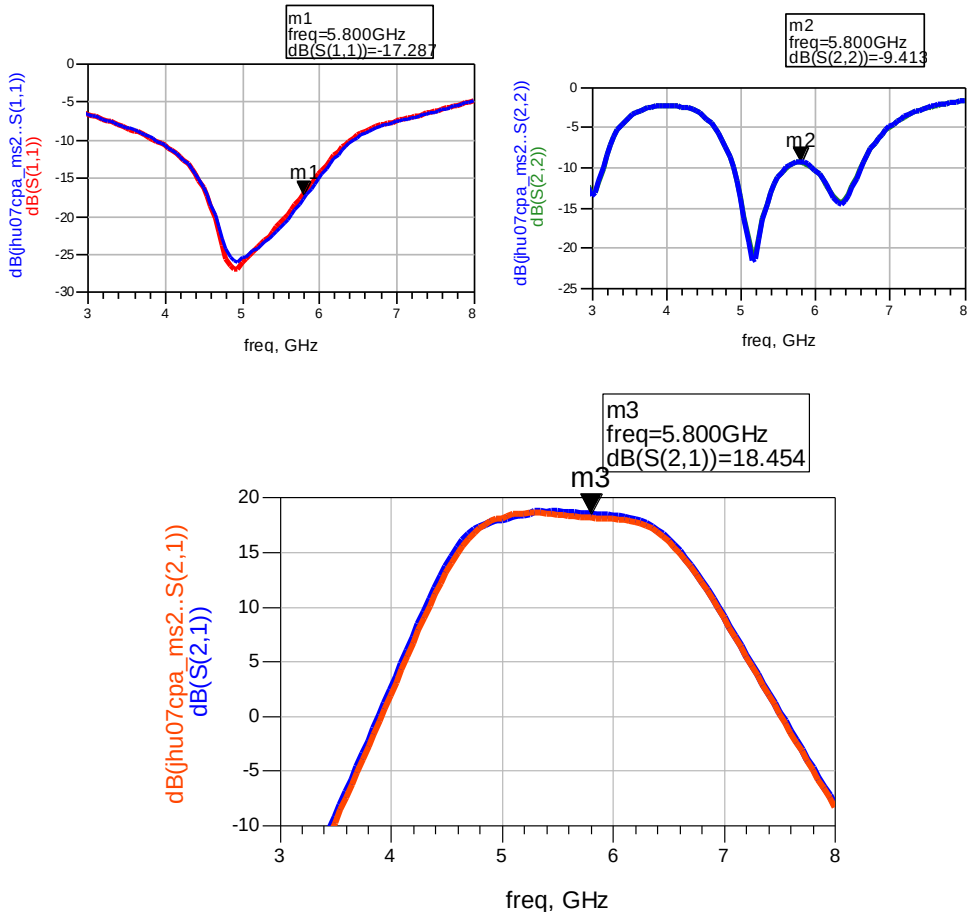
5.8 GHz	Die#1	**JHU07CPA Fall07 TQPED**				3.3V ; 8 mA	VG=4V; 1mA		
Pin(SG)	**Pout(SA)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I1(3.3V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-15.0	-4.67	-17.25	-2.42	14.83	7	23.1	0.57	2.5	2.4
-10.0	0.00	-12.25	2.25	14.50	7	23.1	1.68	7.3	7.0
-8.0	3.00	-10.25	5.25	15.50	9	29.7	3.35	11.3	11.0
-7.0	3.67	-9.25	5.92	15.17	9	29.7	3.91	13.2	12.8
-6.0	4.00	-8.25	6.25	14.50	9	29.7	4.22	14.2	13.7
-5.0	4.17	-7.25	6.42	13.67	9	29.7	4.39	14.8	14.1
-4.0	4.33	-6.25	6.58	12.83	9	29.7	4.55	15.3	14.5



Performance (PAE, Pout, Gain) of Power Amplifier at 5.25 GHz and 3.3V DC Bias



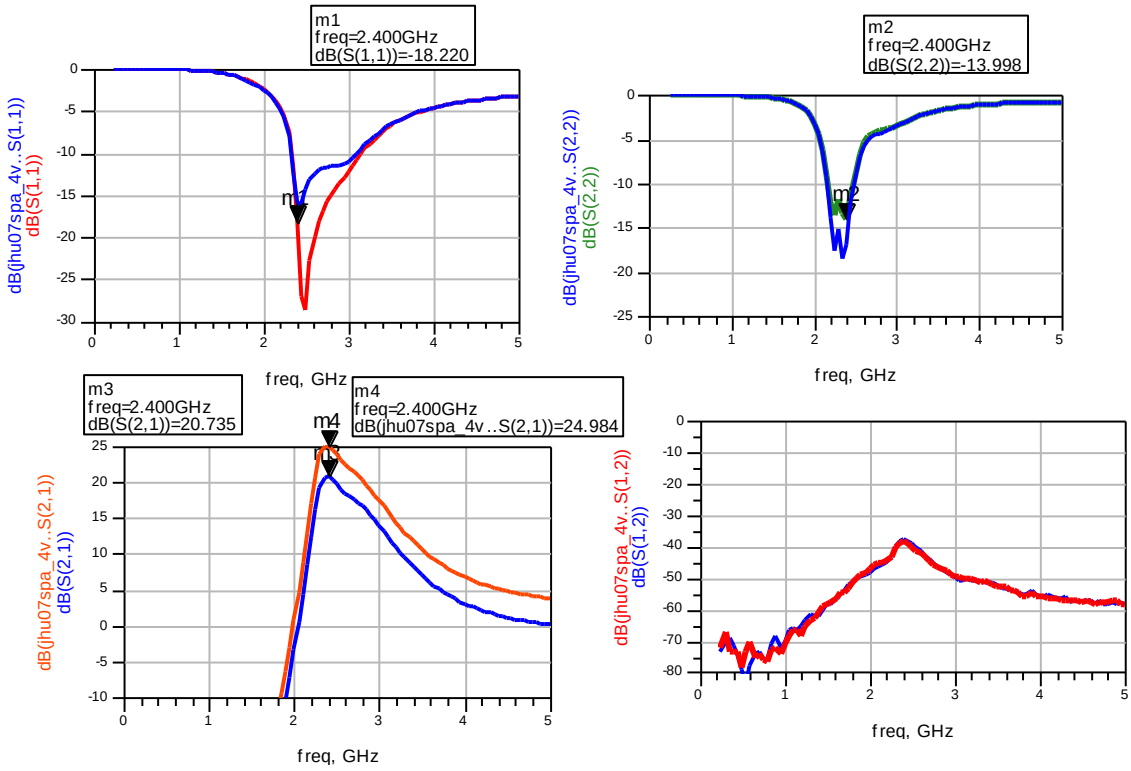
Performance (PAE, Pout, Gain) of Power Amplifier at 5.8 GHz and 3.3V DC Bias



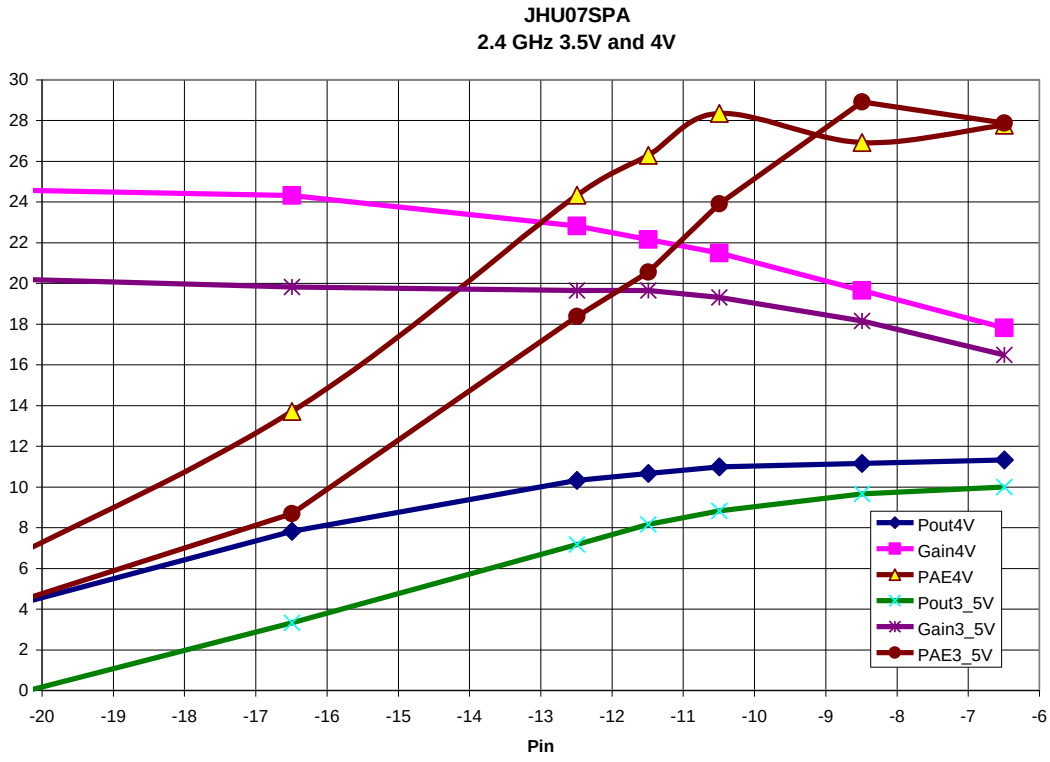
S-Parameters of Power Amplifier at 3.3V DC Bias

Medium Power Amp S-band – David Kenney

An S-Band Medium Power Amplifier was designed for operation around 2.4 GHz. This design uses two stages of amplification to achieve good gain. Measured output power, gain, PAE, and s-parameters are following: The design was optimized for 3.5V at 10 mA on the drain but was also measured at 4.0V with comparable power added efficiencies and slightly more gain. Following are s-parameters and non-linear performance measurements for 3.5V and 4.0V DC bias.



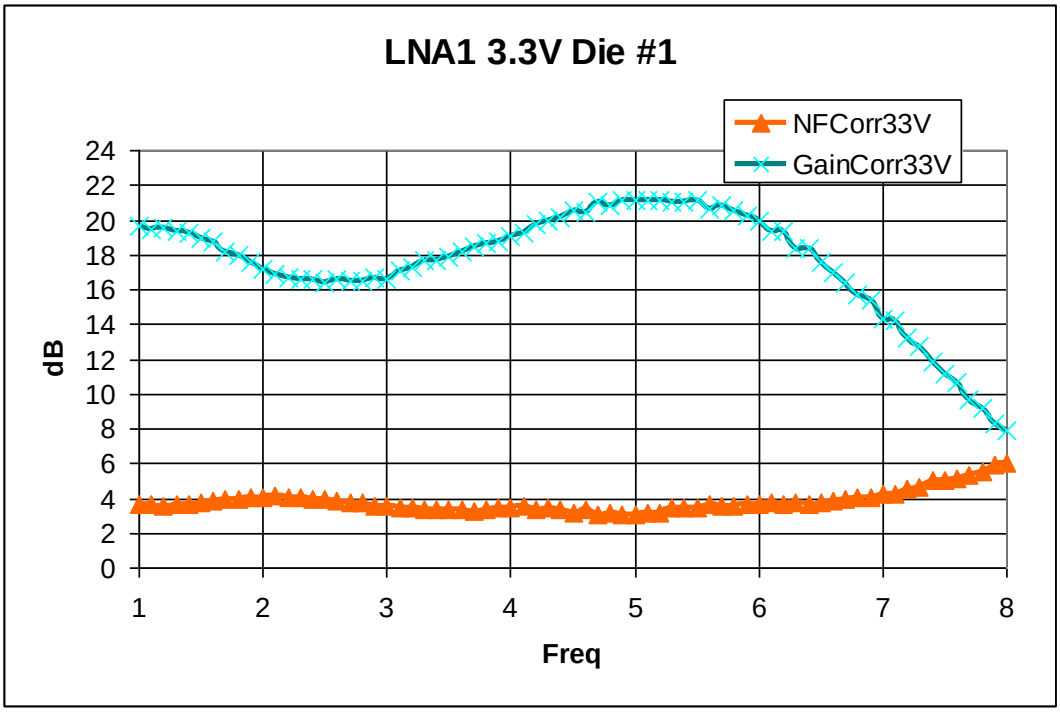
S-parameters of S-band Power Amp at 3.5 and 4V (Note higher gain at 4V)



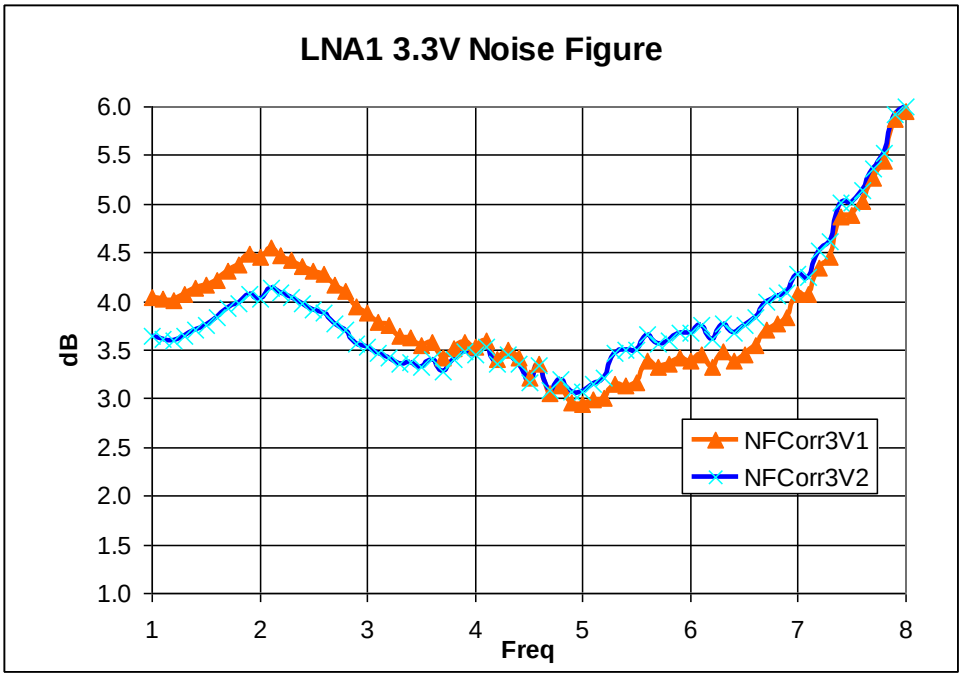
Performance (PAE, Pout, Gain) of Power Amplifier at 2.4 GHz for 3.5V and 4.0V DC Bias

Low Noise Amplifier 1 (Low Power)–Jack Olah & Bill Wallace

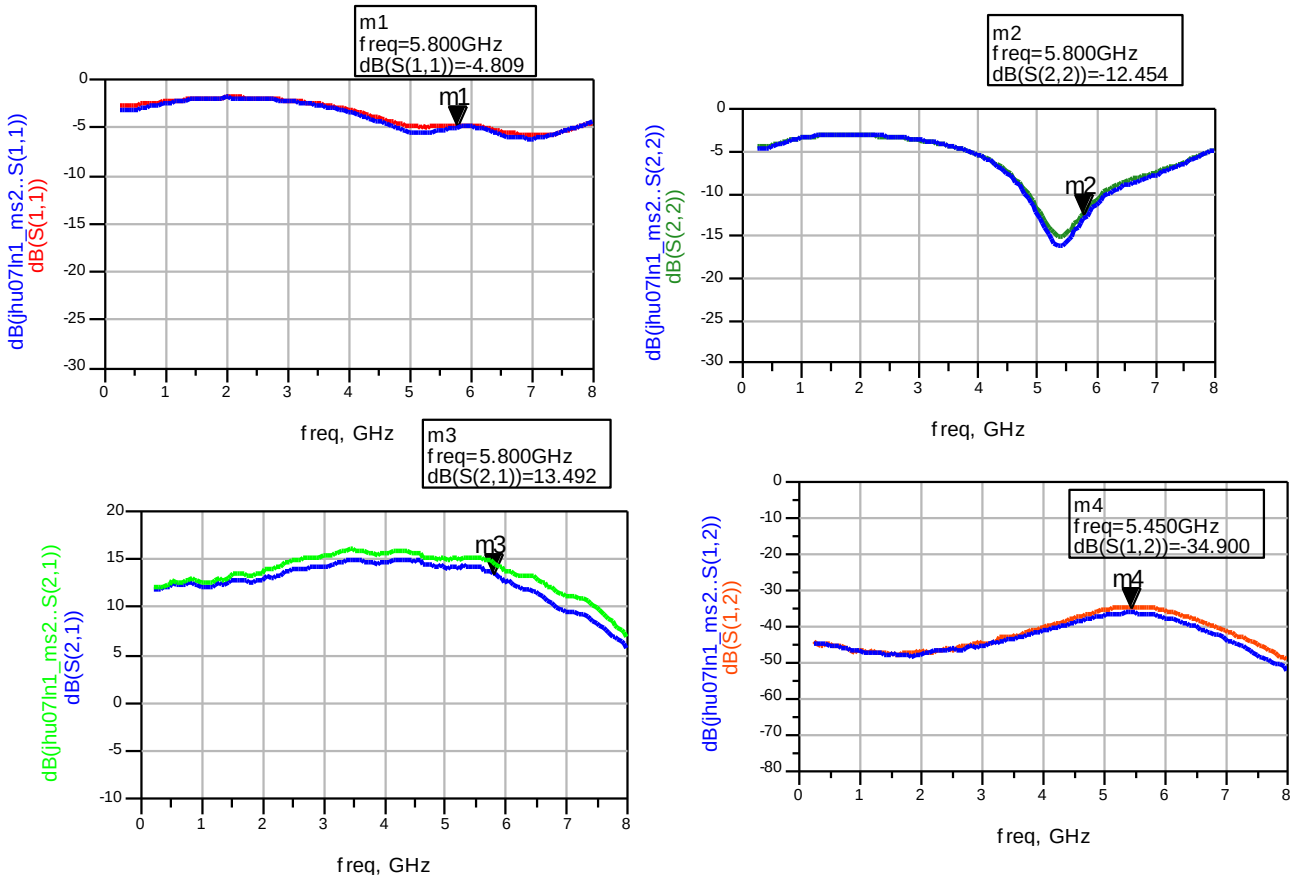
A C-Band Low Noise Amplifier was designed for the 5150 to 5875 MHz. This design uses relatively small Emode PHEMTs for a very low DC power consumption two stage LNA (3.3V at 10 mA). The design worked very well but could only be measured under compression with the 8510 NWA because the analyzer would lose lock below a certain power level which was still too high for the LNA. Gain was measured with the noise figure analyzer to be about 21 dB over the band with about 3 to 3.5 dB Noise Figure. Two die were measured with very similar performance characteristics. Each stage required a 3.3V supply and about 10 mA power consumption.



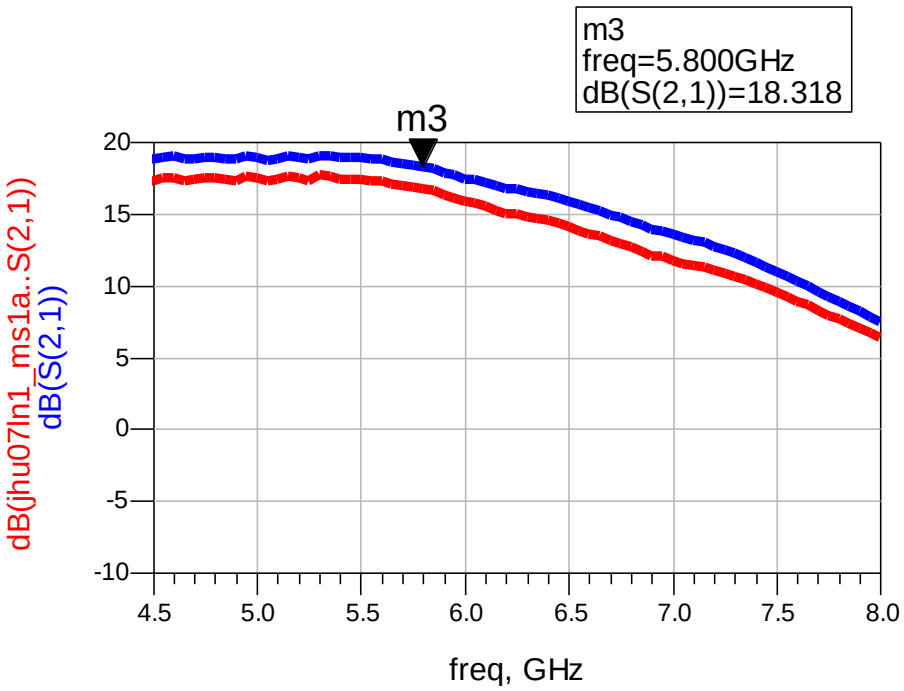
Measured Noise Figure and Gain for LNA1 at 3.3V 10 mA bias (Corrected Data).



Measured Noise Figure of 2 Die for LNA1 at 3.3V 10 mA bias (Corrected Noise Figure Data).



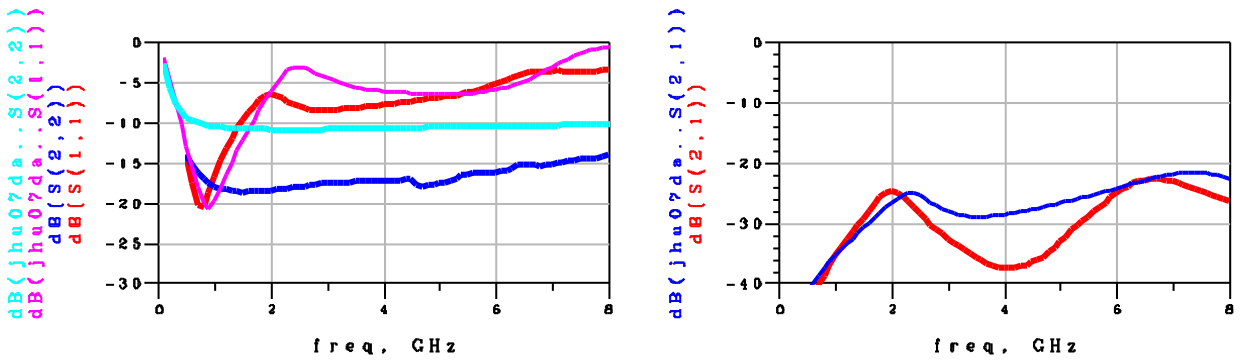
S-Parameters for Low DC Power LNA 1 at 3.3V 10 mA bias. S21 is over-driven.



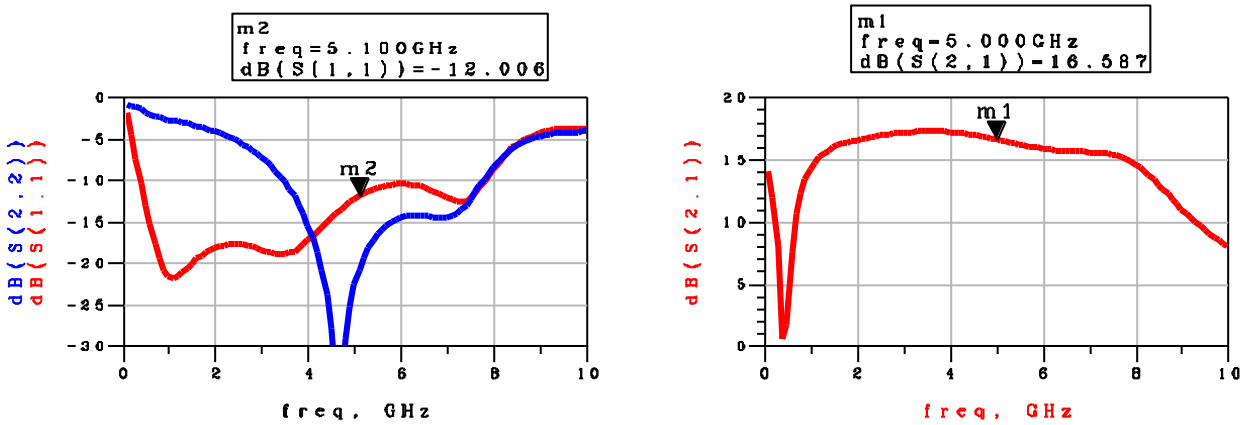
Apparent Gain increase with less input drive on 8510 NWA, still somewhat over-driven.

Distributed Amplifier–Jeremy Stampfly

A broadband distributed amplifier was designed to use relatively little DC power. The design was measured to have decent broadband match but the gain was very low. During design checks, the layout did not pass LVS checks, but the error message implied a problem in the gate transmission line. The actual layout gate line was simulated with Sonnet to verify that there were no errors. Given the actual performance, another look discovered the missing connection and it was on the other side of the chip at the drain transmission line. A metal2 connection to the last PHEMT device did not have a via2 layer to connect it to metal1. There was a via1 layer connecting down to metal0, rather than up to metal2. Re-simulations with ADS after removing the one connection compare favorably to the measured data. Hopefully the corrected design can be re-fabbed with a future MMIC Design class fabrication.



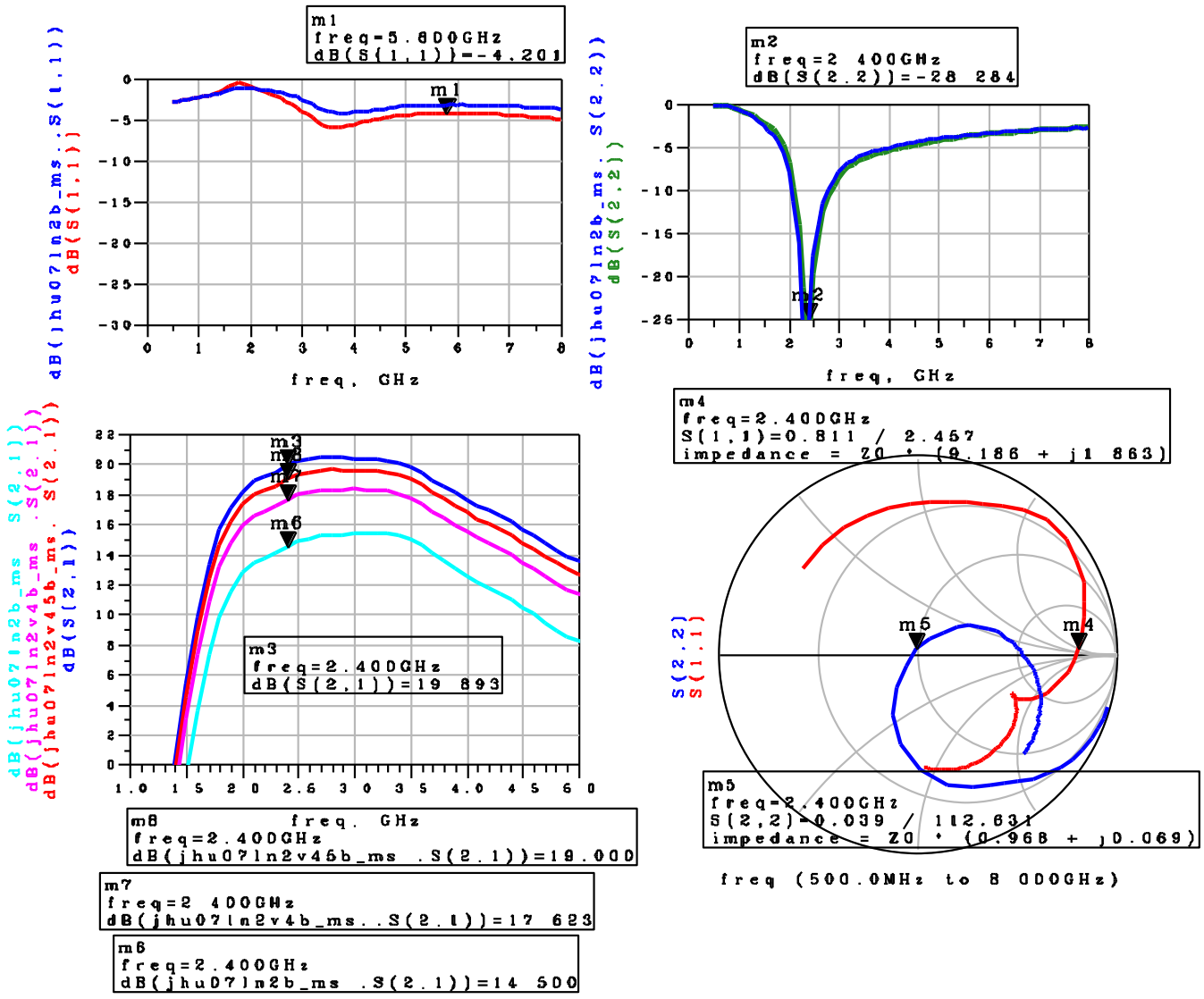
Comparison of Measured Distributed Amplifier vs. Simulation with missing connection.



Original ADS Simulation (excluding interconnect).

Low Noise Amplifier 2–Erica Simcoe

A low power, low noise amplifier was designed for S-band operation around 2.4 GHz. Two die were measured at 3.3V at 5 mA, 4V at 8 mA, and 4.5V at 10 mA with virtually identical operation. The 8510 NWA was over-driving the amplifier so it helped to increase the DC supply to get a better gain measurement. One of the die was also measured from 3.3V at 5 mA to 5V at 11 mA of bias. Plots of S21 at the increasing DC supply voltages show an increase in S21 from 14.5 dB up to 19.7 dB, closer to the expected value but still possibly compressed. S22 is only shown at the highest and lowest bias points with virtually no change and S11 likewise with a small change.



S-parameters of S-band LNA from 3.3V to 5V (nominal bias is 3.3V at about 5 mA).

Mixer S-Band – John Tinsley

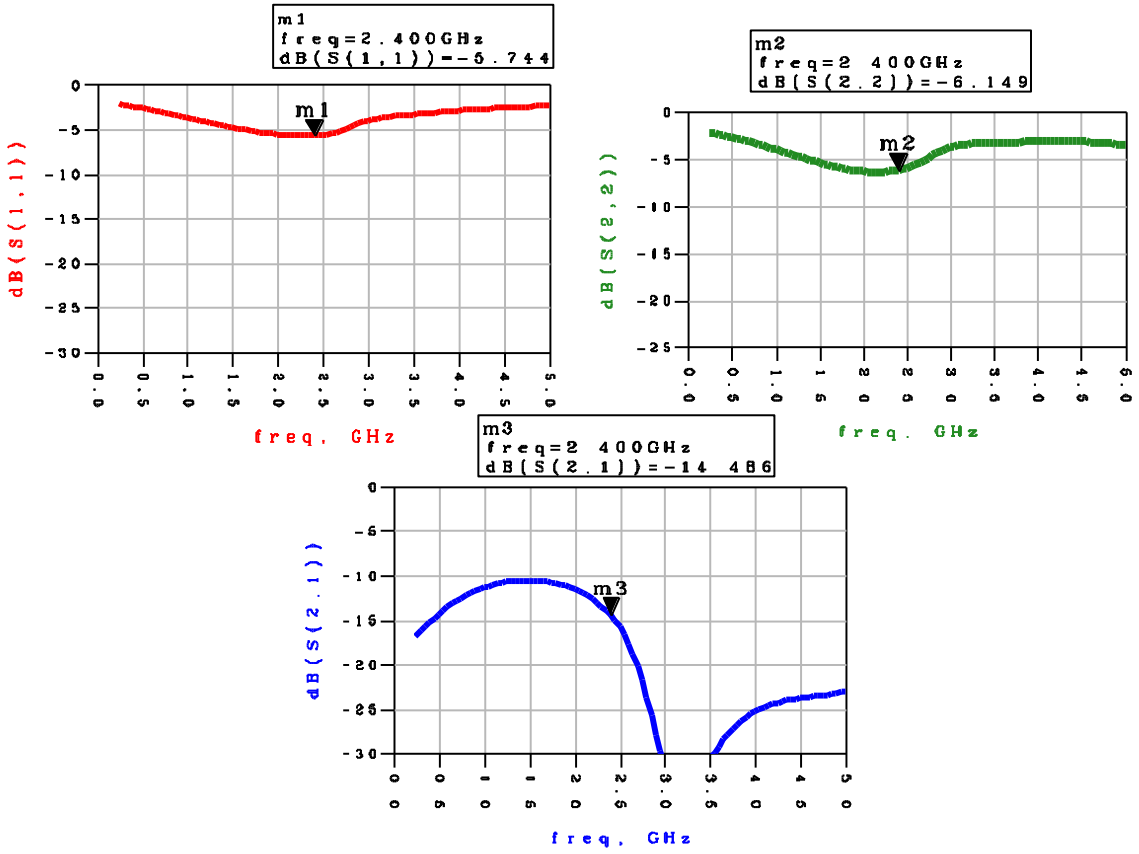
The s-band mixer was measured for down conversion loss which appeared to be quite a bit higher than expected. Conversion loss was estimated at about 6-7 dB but was measured to be about 45 d B. This design did not pass the LVS check initially but no error could be found. The "errors" appeared to be correct and it is difficult to see a problem because there is so much symmetry in the LO and RF sections.

Measured Mixer
John Tinsley

RF = 2.4 GHz initially -5 dBm
1) LO 2.3 GHz
Down Conversion Low End

RF 2.325 to 2.5 GHz and IF 25-200 MHz -5 dBm settir
Measured 2.3 GHz LO
Note: Swept RF 2.325 to 2.5 GHz -- similar low conver

LO (SG)	LO (corr)	RF (corr)	IF (meas)	LO (meas IF)	RF (meas IF)	Loss (gain)	LO/IF (Isol)	RF/IF (Isol)
13	11.51	-6.49	-52.0	3.2	-17.0	-45.5	8.3	9.02



Measured s-parameters of S-band Mixer (LO & RF ports)

Mixer C-Band – Alex Mendes

The C-band Mixer was measured at various LO power levels at 5.8 GHz to determine the up and down conversion loss. The design worked very well and was very broadband, up to 500 MHz IF or RF from 5.3 to 6.3 GHz. Conversion loss was better than 7 dB up and down for the passive mixer. Following is the measured performance:

Measured Mixer
Alex Mendes

RF = 5.7 GHz initially -10 dBm
RF 5.3 to 6.3 GHz and IF 25-500 MHz -10
Measured 5.8 GHz LO
Note: Swept RF 5.3 to 6.3 GHz -- very flat

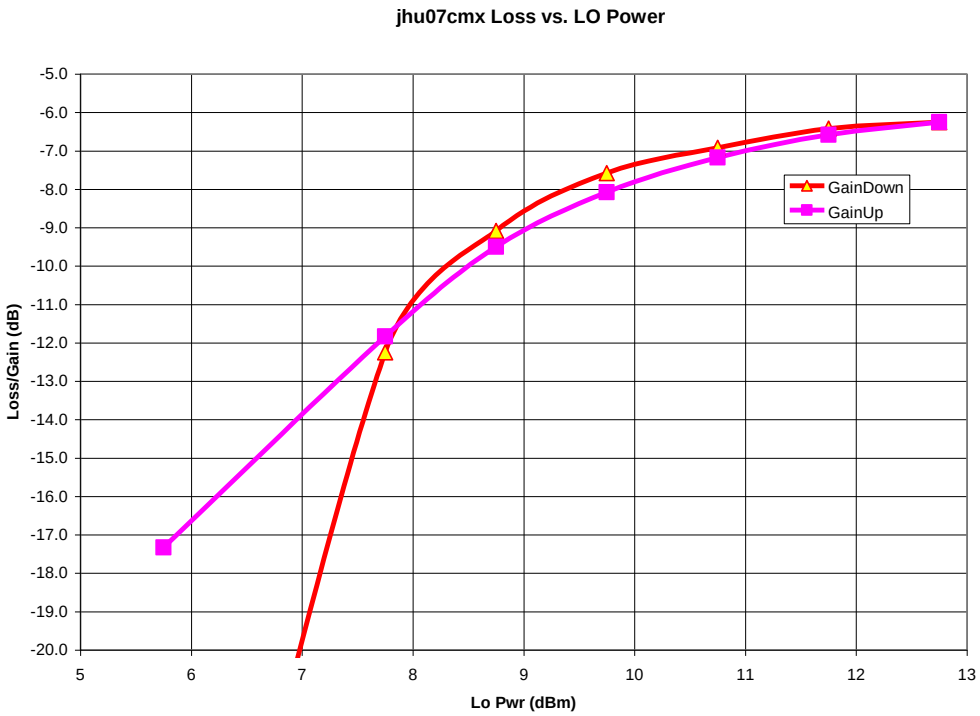
1) LO 5.8 GHz
Down Conversion Low End

LO (SG)	LO (corr)	RF (corr)	IF (meas)	LO (meas IF)	RF (meas IF)	Loss (gain)	LO/IF (Isol)	RF/IF (Isol)
8	5.75	-12.25	-46.0	-20.8	-38.2	-33.8	28.8	23.67
10	7.75	-12.25	-24.5	-19.0	-38.3	-12.3	29.0	23.83
11	8.75	-12.25	-21.3	-18.2	-38.7	-9.1	29.2	24.17
12	9.75	-12.25	-19.8	-17.5	-39.0	-7.6	29.5	24.50
13	10.75	-12.25	-19.2	-17.0	-39.3	-6.9	30.0	24.83
14	11.75	-12.25	-18.7	-16.7	-39.7	-6.4	30.7	25.17
15	12.75	-12.25	-18.5	-16.3	-40.0	-6.3	31.3	25.50
15.5	13.25	-12.25	-18.3			-6.1		

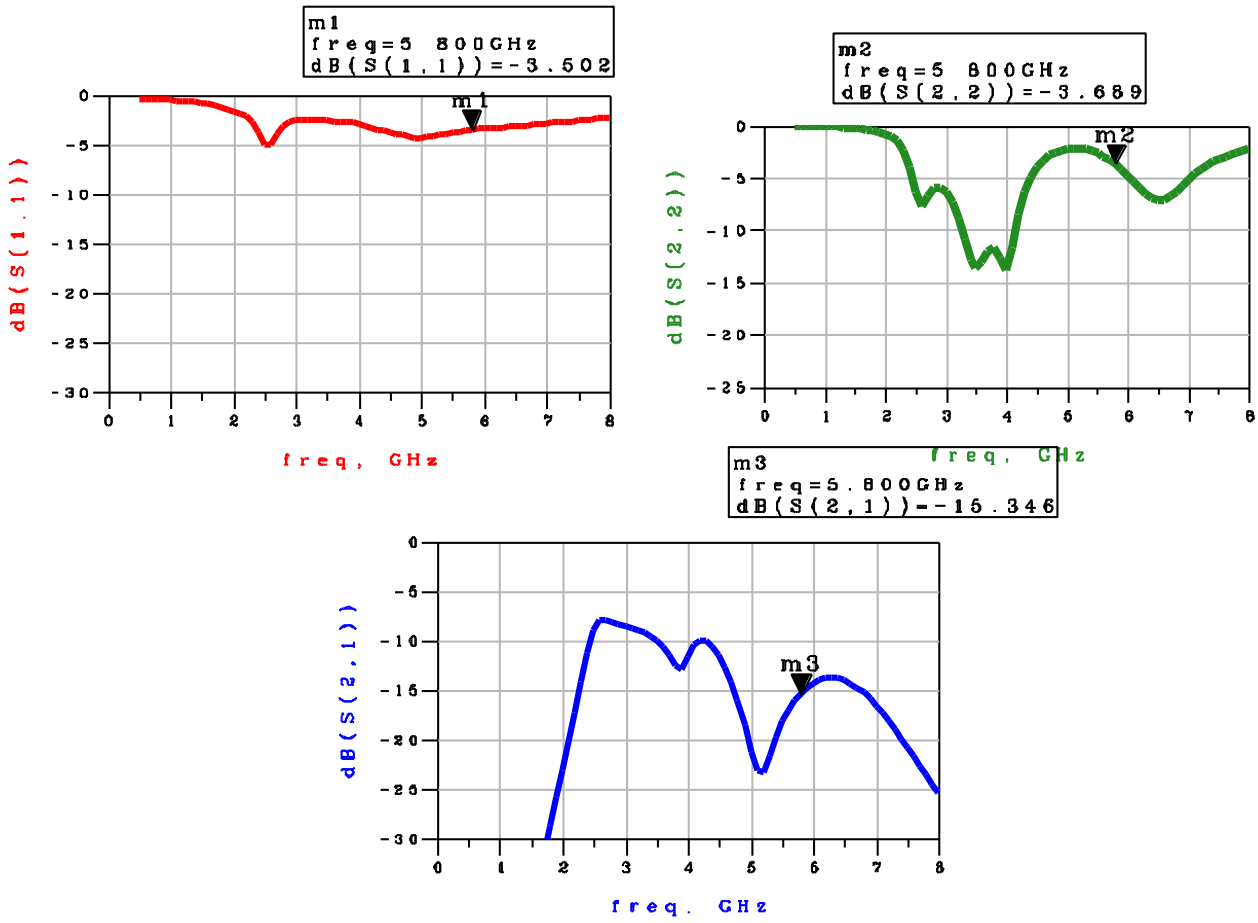
2) LO 5.6 GHz
IF = 0.1 GHz initially -10 dBm
Down Conversion High End

IF 25-500 MHz -10 dBm setting
Measured 5.8 GHz LO
Note: Swept IF 25 MHz to 500 MHz -- very

LO (SG)	LO (corr)	IF (dBm)	RF (meas)	LO (meas RF)	RF (corr)	Loss (gain)	LO/RF (Isol)	RF/IF (Isol)
8	5.75	-10	-29.6	-12.6	-27.3	-17.3	20.6	15.08
10	7.75	-10	-24.1	-10.9	-21.8	-11.8	20.9	9.58
11	8.75	-10	-21.8	-10.5	-19.5	-9.5	21.5	7.25
12	9.75	-10	-20.3	-10.0	-18.1	-8.1	22.0	5.83
13	10.75	-10	-19.4	-9.2	-17.2	-7.2	22.2	4.92
14	11.75	-10	-18.8	-8.2	-16.6	-6.6	22.2	4.33
15	12.75	-10	-18.5	-6.8	-16.3	-6.3	21.8	4.00
15.5	13.25	-10	-18.5					



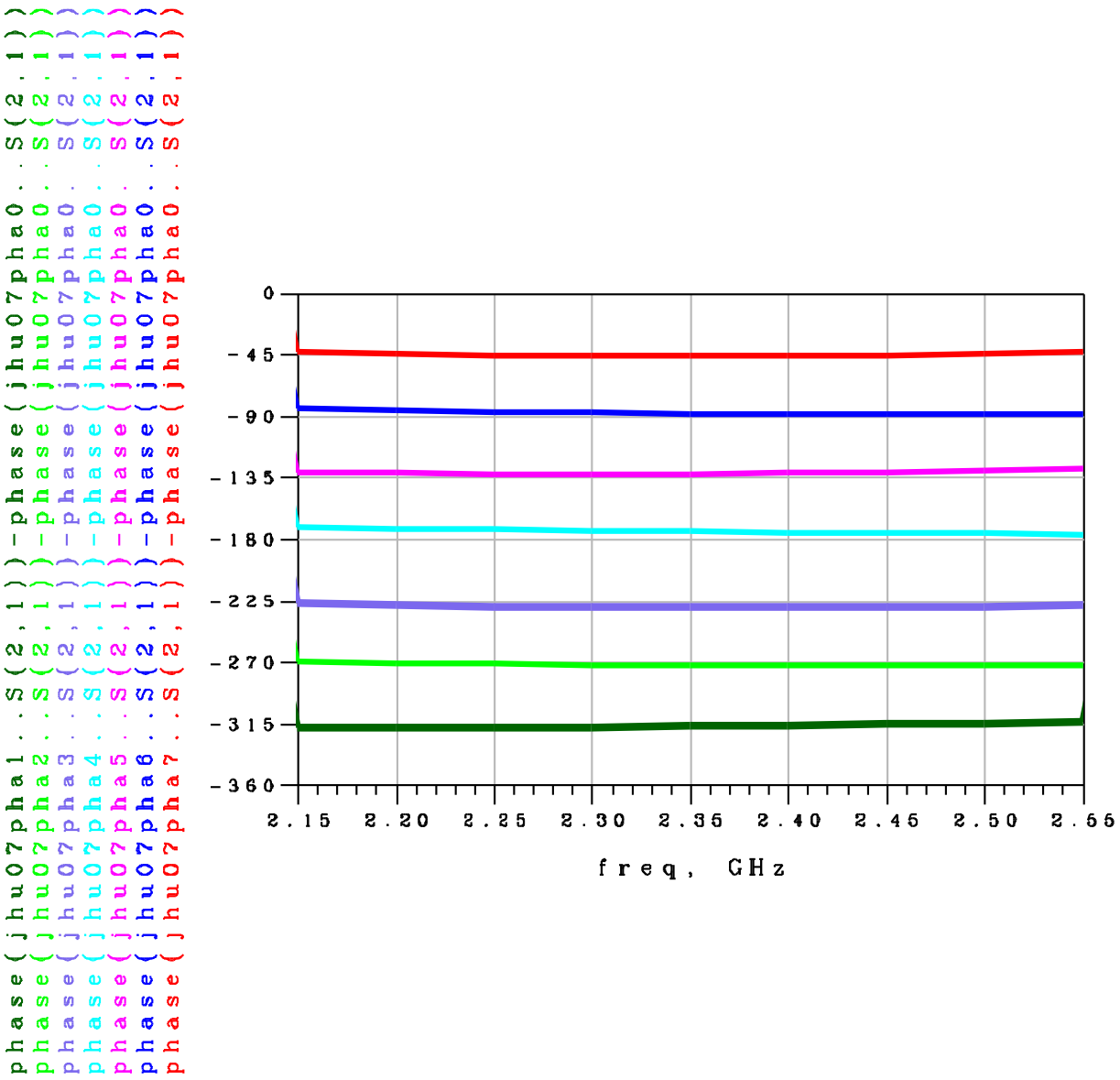
C-Band Mixer Conversion Gain vs. LO Power (Up/Down)



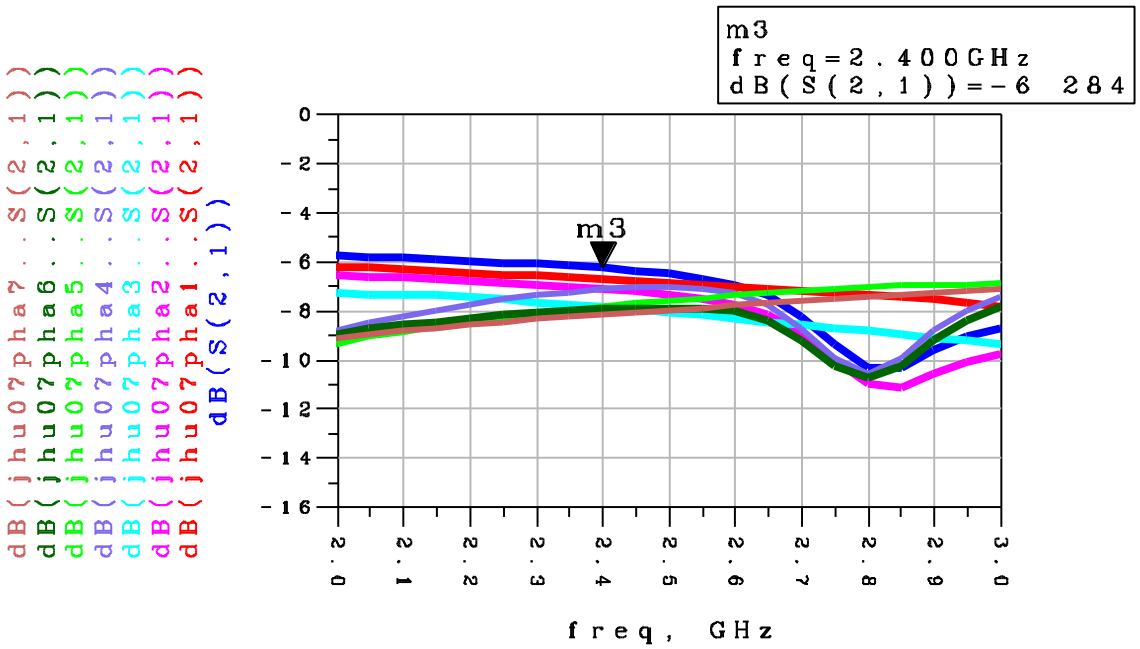
S-parameters of C-Band Mixer; LO is port 1, RF is port 2, RF/LO isolation is S21
Note: drive levels are not the same as for actual mixer operation.

Phase Shifter–Alan Yu

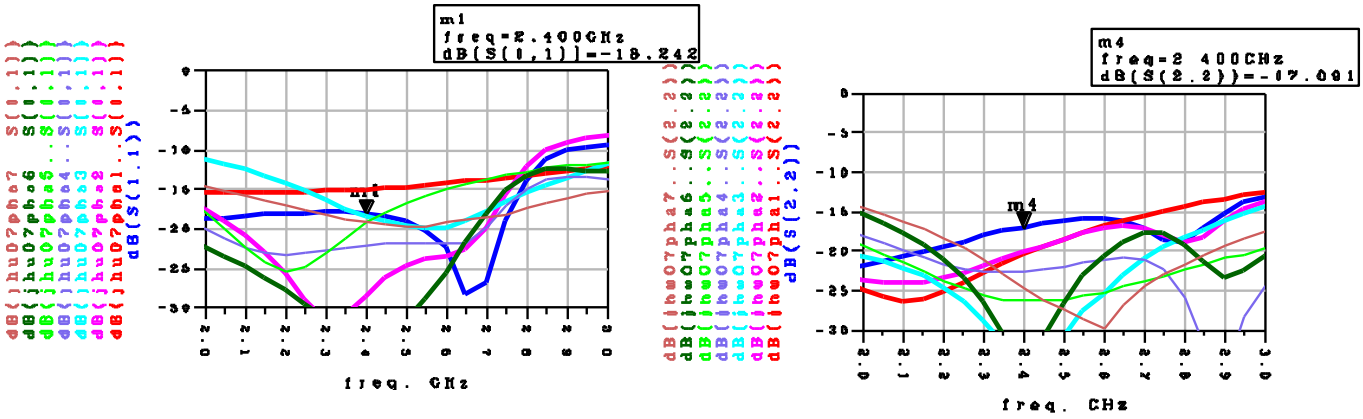
An S-Band 2 Bit Phase Shifter was designed for the 2305 to 2497 MHz WCS and ISM bands. This 3-bit design uses PHEMTs as switches. Phase shift measurements were very close to simulations. DC bias was 0V and -2V for the on/off states of the DC switches. Two different die were measured and were virtually identical. Insertion loss balance was about +/- 1 dB and return loss was better than 10 dB for all states within the S-band operation.



Phase Shifts of MMIC 3 Bit Phase Shifter in 45 Degree steps.



Insertion Loss S21 for all Phase Shift States of MMIC 3 Bit Phase Shifter.



Return Loss S11/S22 All Phase Shifts of MMIC 3 Bit Phase Shifter.

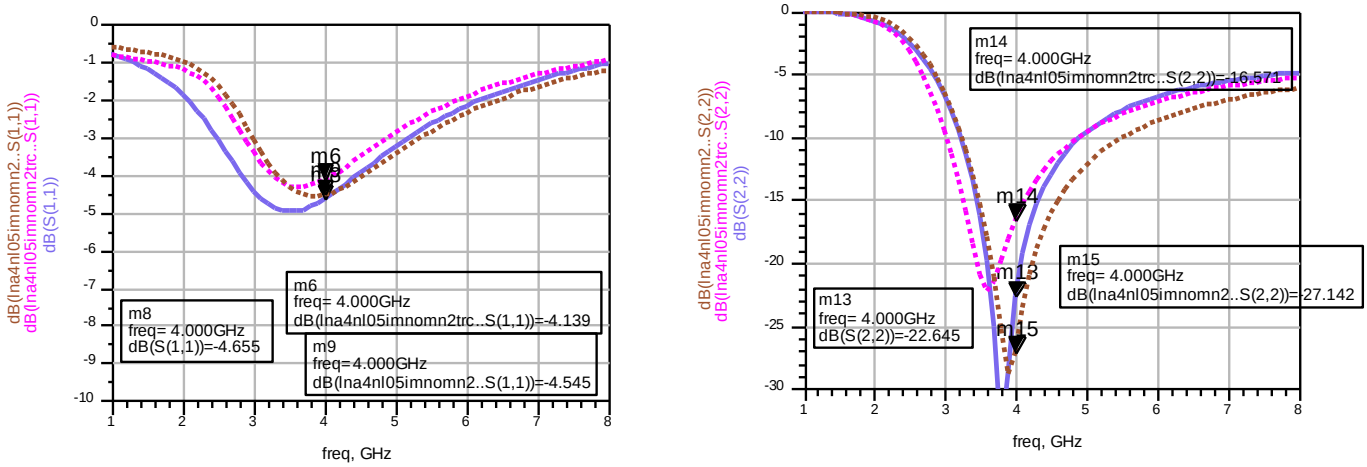
Class Design Examples: Low Noise Amplifier and Power Amplifier (4 GHz) by John Penn

During the course the students are shown a design example of a low noise amplifier and a medium power amplifier at 4 GHz. In previous years, layouts were completed for the LNA and PA design in Agilent's ADS and later Microwave Office MWO on a single 60 x 60 mil die (54 x 54 after dicing) using TriQuint's TQTRX MESFET process. In 2005, the LNA and PA examples were re-designed using ADS and TriQuint's 0.5 um PHEMT (TQPED)

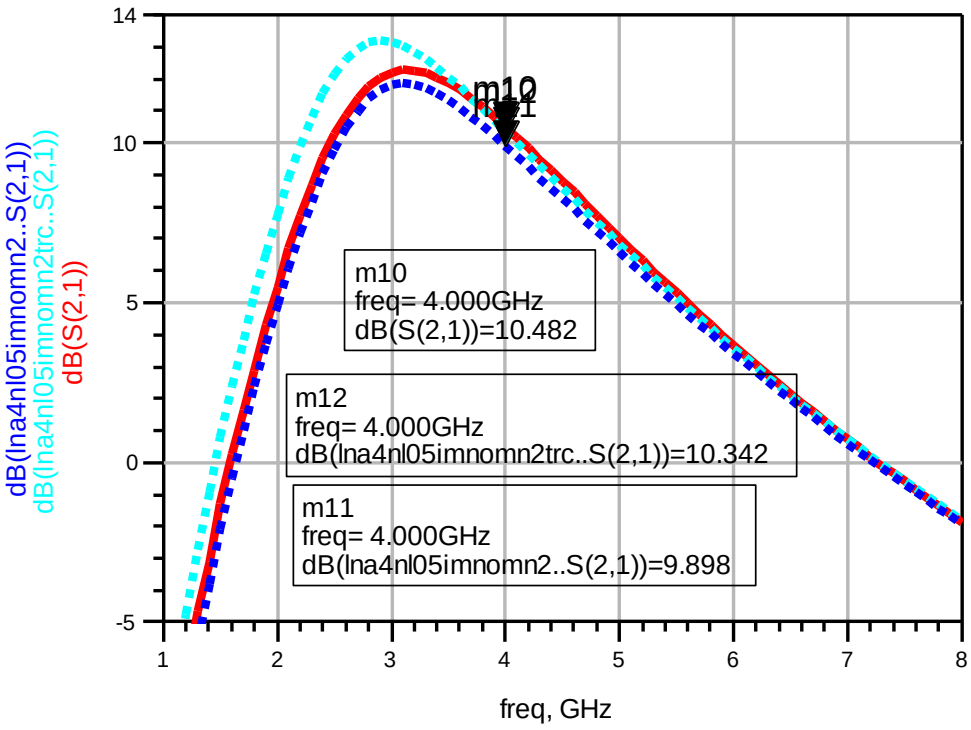
DC Bias was comparable between the 2005 and 2006 Power Amps but output power was more than 1 dB higher and gain 2 dB higher resulting in 31% PAE versus 23% at 4.0V and 4.0 GHz. This year measurements were taken at additional drain voltages and also at 4.05 GHz which appeared to be a peak in the performance, close to the design frequency of 4.0 GHz. Output Power was about 17 dBm at 4.05 GHz and 4V dropping to about 16 dBm at 4.0 GHz and 3.0V. Power Added Efficiency (PAE) got better at 3.5V and especially 3.0V of bias peaking at about 40% PAE for 4.05 GHz and 3.0V DC Bias. The Power Amp design agreed well with simulations for s-parameters but was a little lower for non-linear performance predictions (Pout and PAE).

The Low Noise Amplifier showed very good agreement between ADS simulations and measurements. When the Noise Figure meter was used to measure gain and noise figure of the LNA, a through connection was used to subtract out losses for the measurements. The "through" path appeared to be a little low compared to measurements from 2005 and also compared to measurements made with the same setup and a signal generator. This may explain why the noise figure seems a little higher by a few tenths of a dB than predictions—similar shape though—and the gain is lower than that measured with the 8510 NWA for the same LNA at 3.0V DC Bias. If the other 3.75 dB "through" loss at 4.0 GHz were used instead of the 2.3 dB figure from the Noise Figure Instrument, the gain and noise figure at 4.0 GHz would be identical to simulations. Overall, the LNA and the PA designs compared well to simulations at 4.0 GHz.

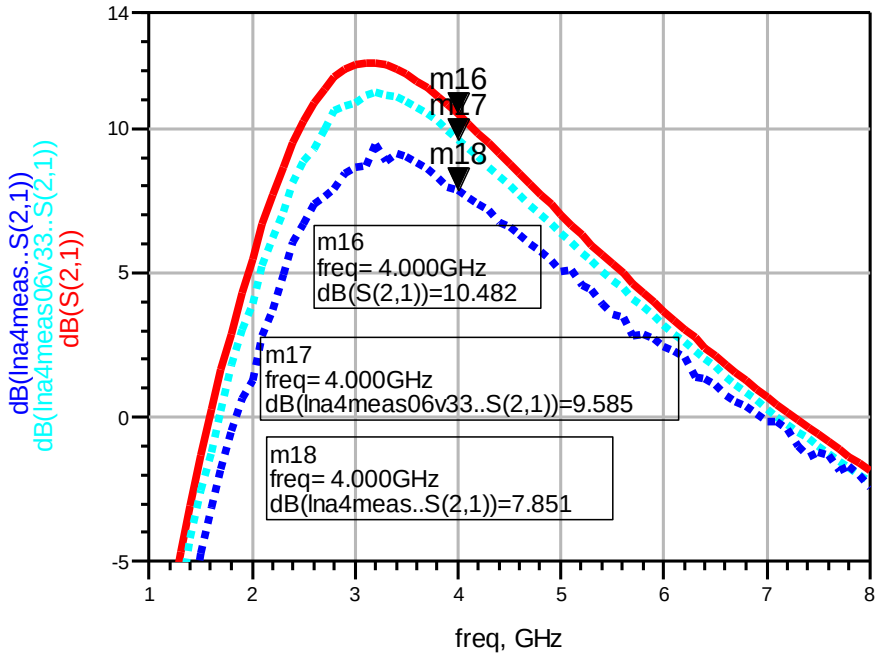
Other test circuits were also designed to be used for future lectures and class examples.



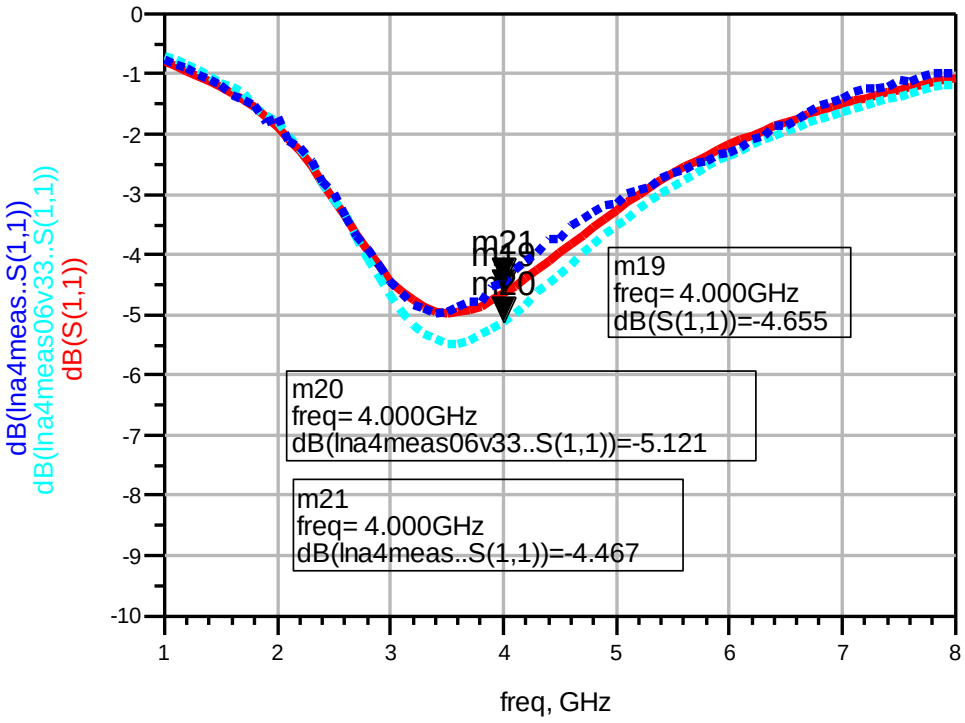
Good Agreement Between Measured and Simulated (ADS) S11/S22 for LNA at 5.0V



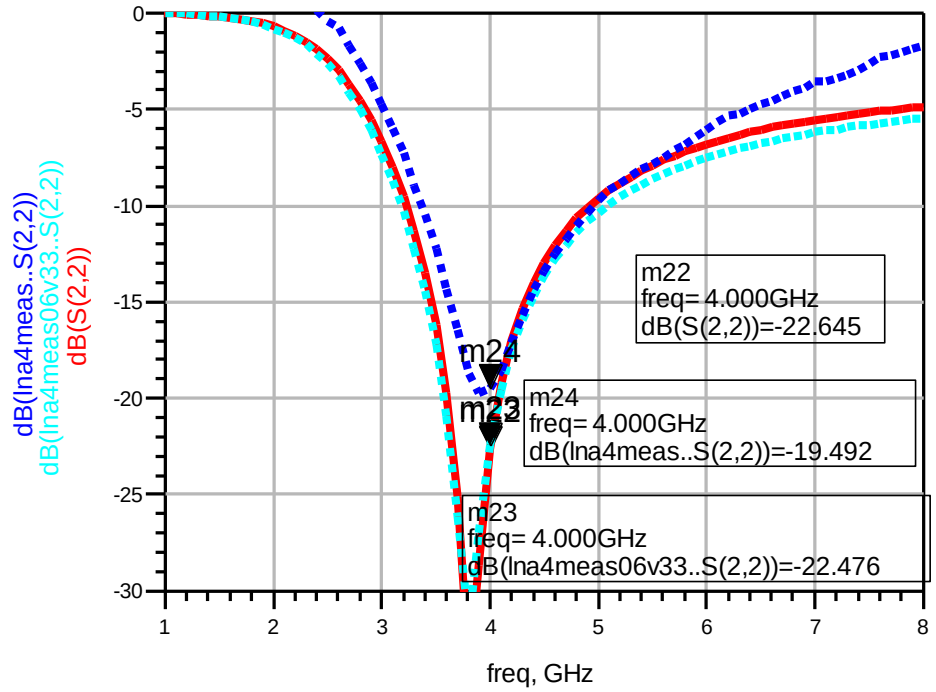
ADS Simulations of LNA4 Gain With and Without Interconnect vs. Measured (solid).



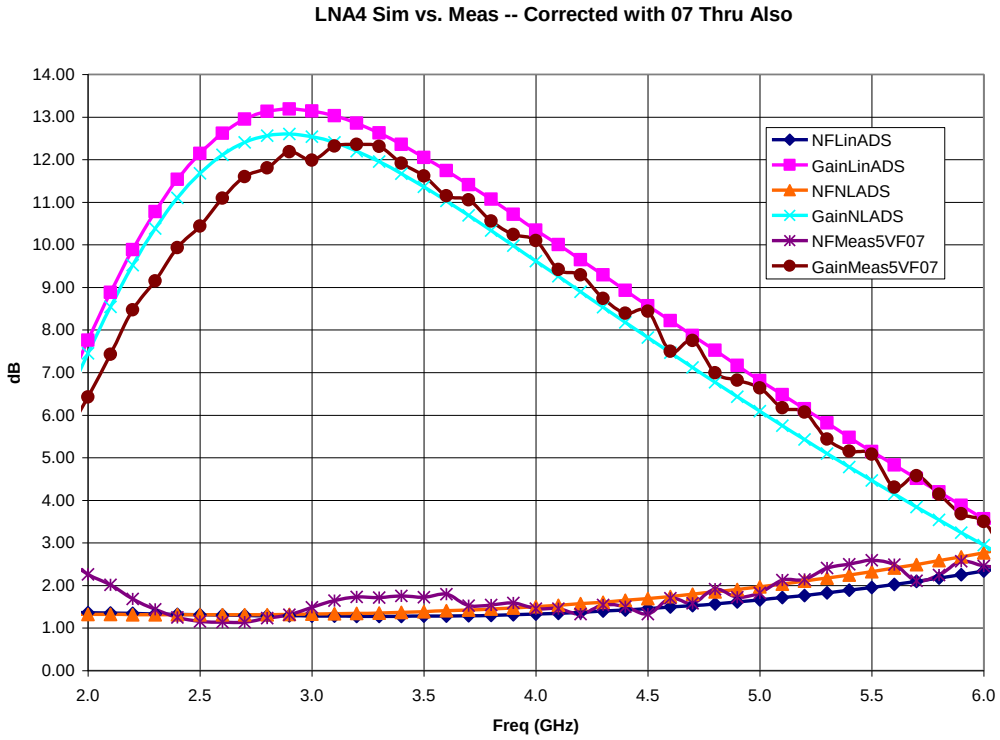
Variation of LNA4 Gain Measured for 2005, 2006, and 2007 (solid).



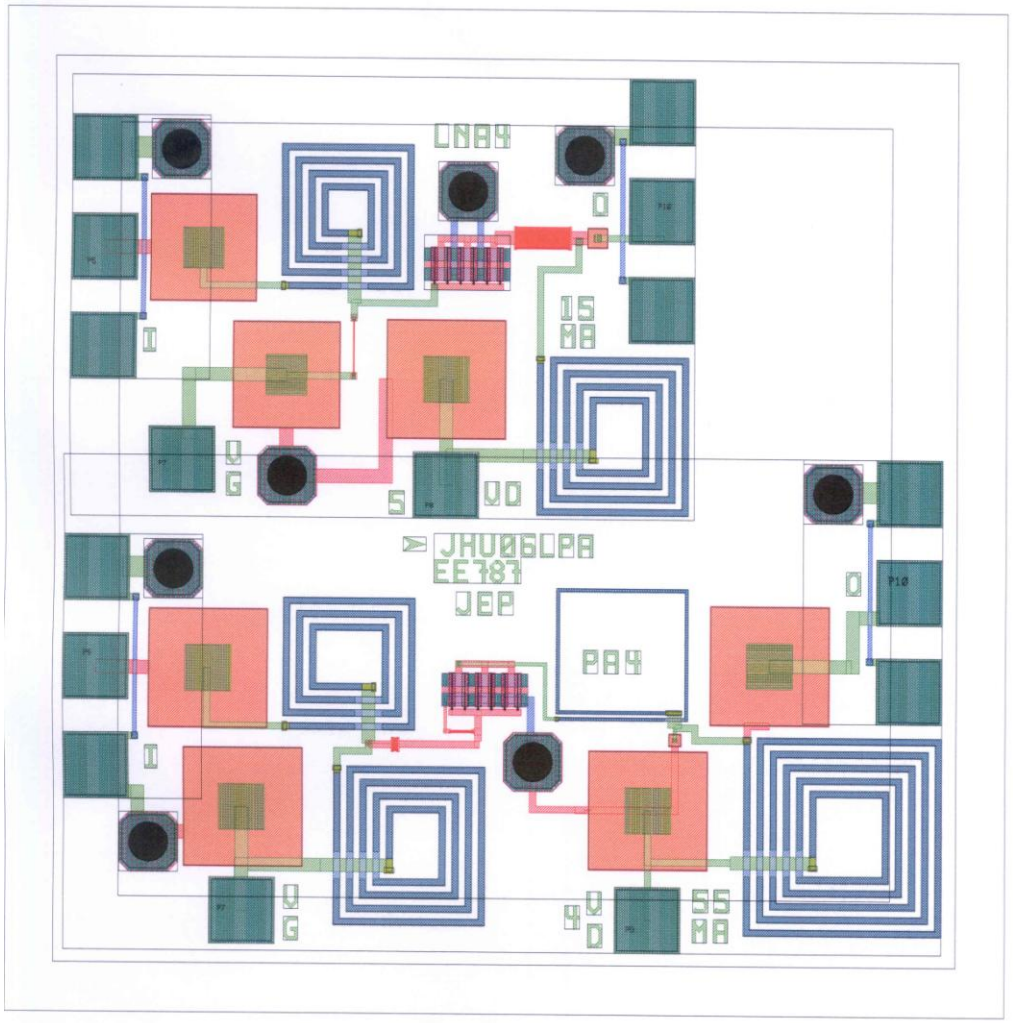
Variation of LNA4 S11 Measured for 2005, 2006, and 2007 (solid).



Variation of LNA4 S22 Measured for 2005, 2006, and 2007 (solid).



Measured Noise Figure and Gain of LNA4 vs. ADS Simulations

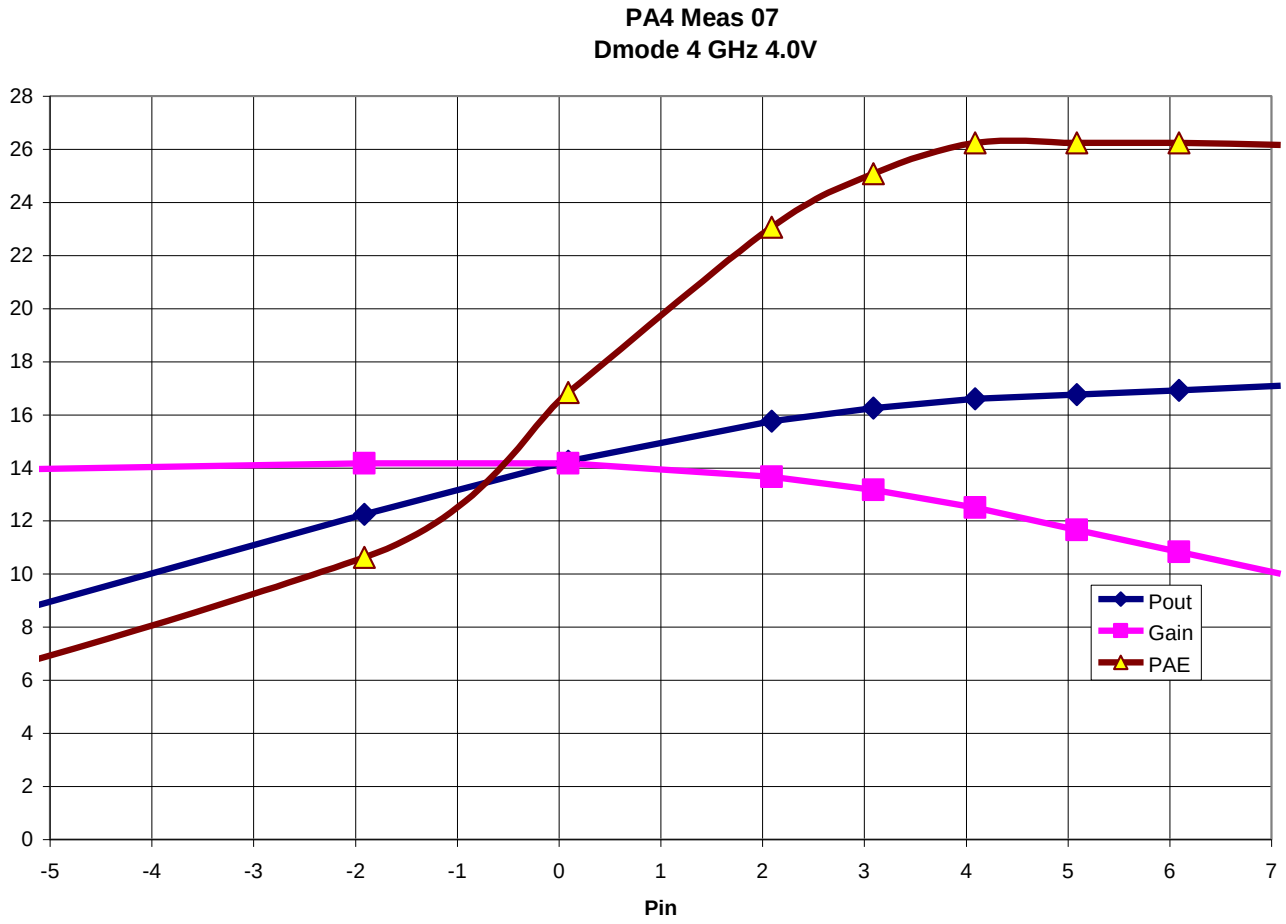


Layout of Class Example Designs: 4 GHz LNA and 4 GHz PA Designs (54 mil x 54 mil

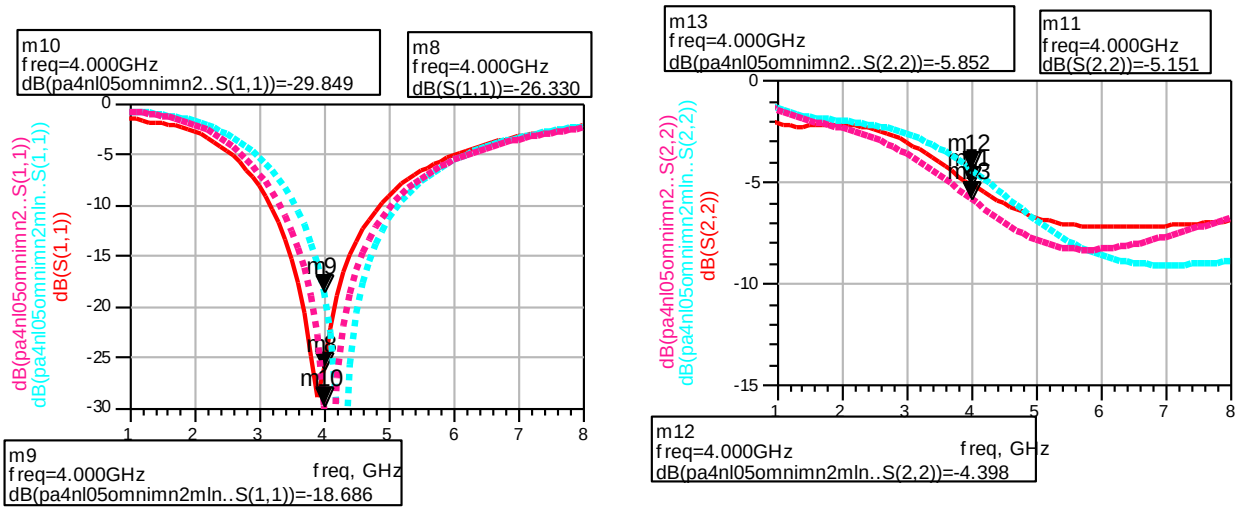
Performance (PAE, Pout, Gain) of Power Amplifier Design at 4.0V DC Bias and 4.0 GHz

D Mode Power Amps--4.0 GHz example at 4.0 V
Measured better at lower voltages… Loss 3.5 dB for thru

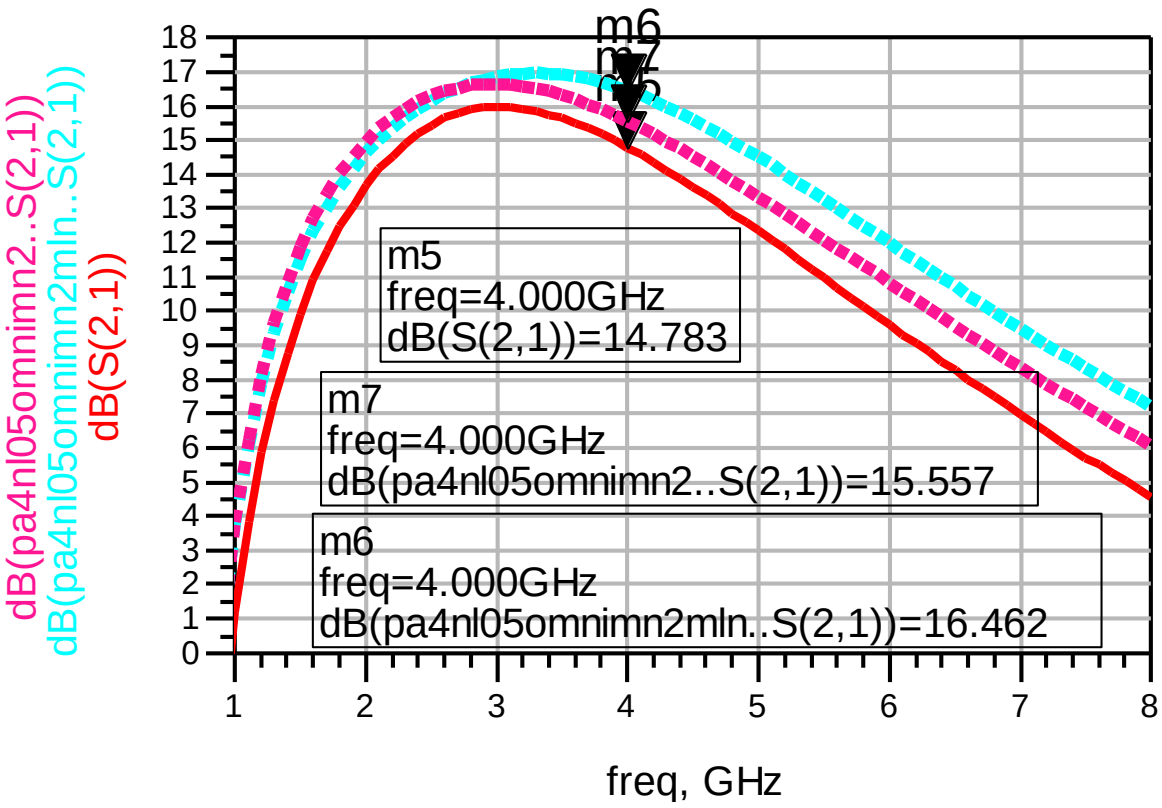
4 GHz	Die#1	**PA4 GHz Dmode Fall06 TQPED**				4.0V ; 40 mA			
Pin(SG)	**Pout(SA)**	**Pin(corr)**	**Pout(corr)**	**Gain**	**I1(4.0V)**	**PDC(mw)**	**Pout(mw)**	**Drn Eff**	**PAE**
-20.0	-10.17	-21.91	-8.25	13.66	38	152.0	0.15	0.1	0.1
-10.0	-0.33	-11.91	1.59	13.50	38	152.0	1.44	0.9	0.9
0.0	10.33	-1.91	12.25	14.16	38	152.0	16.79	11.0	10.6
2.0	12.33	0.09	14.25	14.16	38	152.0	26.61	17.5	16.8
4.0	13.83	2.09	15.75	13.66	39	156.0	37.58	24.1	23.1
5.0	14.33	3.09	16.25	13.16	40	160.0	42.17	26.4	25.1
6.0	14.67	4.09	16.59	12.50	41	164.0	45.60	27.8	26.2
7.0	14.83	5.09	16.75	11.66	42	168.0	47.32	28.2	26.2
8.0	15.00	6.09	16.92	10.83	43	172.0	49.20	28.6	26.2
9.0	15.17	7.09	17.09	10.00	44	176.0	51.17	29.1	26.2
3.9GHz									
7.0	15.00	5.09	16.92	11.83	39	156.0	49.20	31.5	29.5
9.0	15.50	7.09	17.42	10.33	42	168.0	**55.21**	32.9	**29.8**



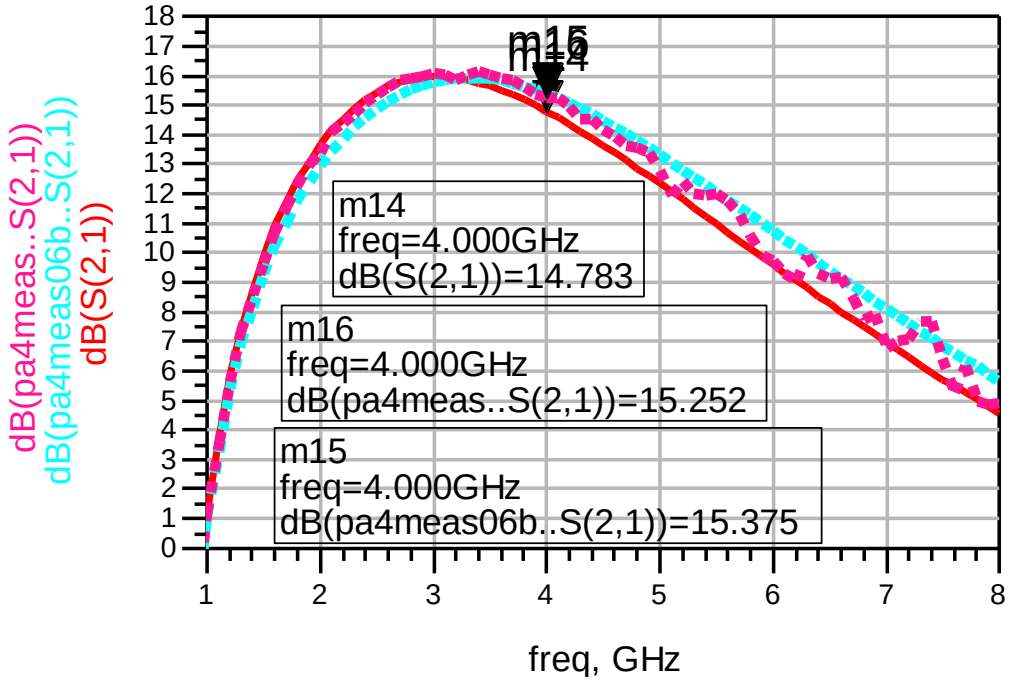
PA4 Pout, Gain, PAE vs. Pin



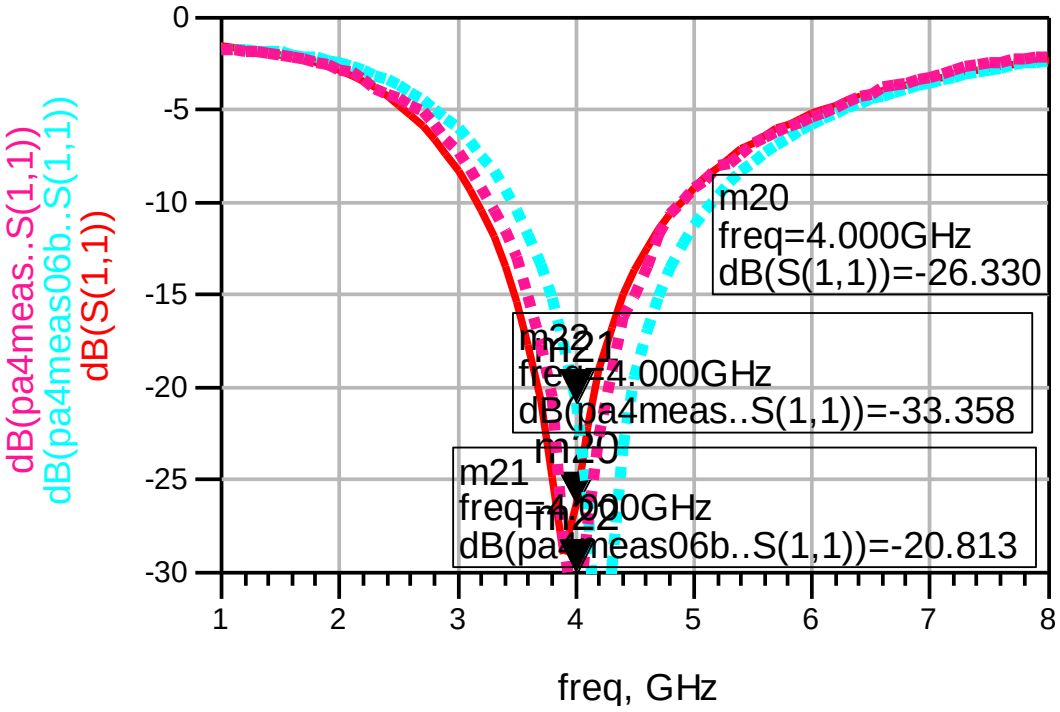
ADS Simulations of PA4 S11/S22 With and Without Interconnect vs. Measured (solid).



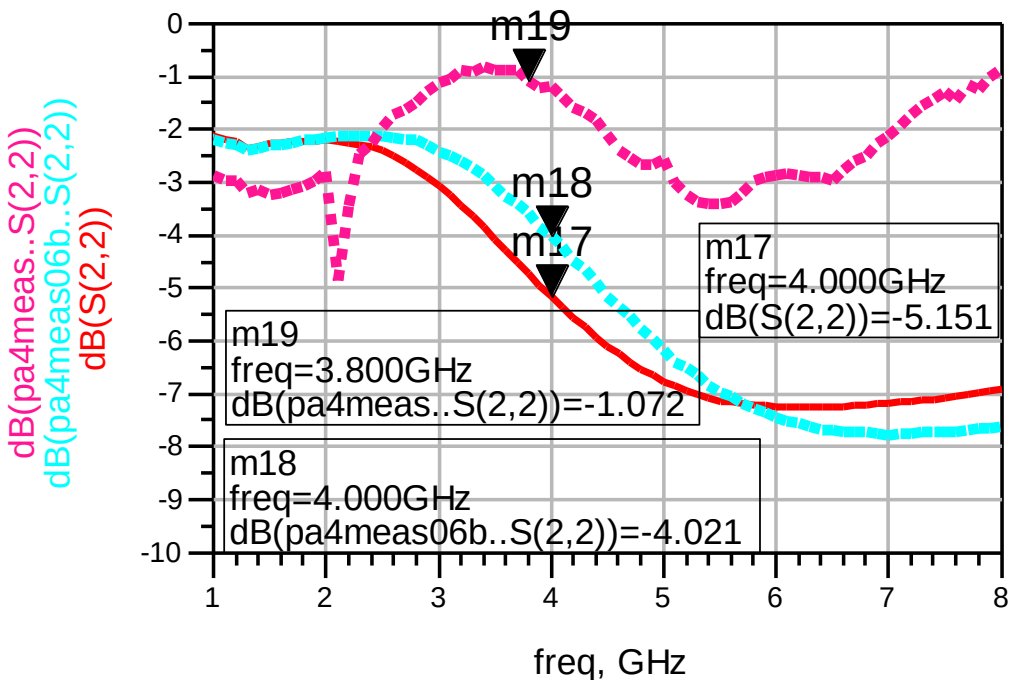
ADS Simulations of PA4 Gain With and Without Interconnect vs. Measured (solid).



Variation of PA4 Gain Measured for 2005, 2006, and 2007 (solid).



Variation of PA4 S11 Measured for 2005, 2006, and 2007 (solid).



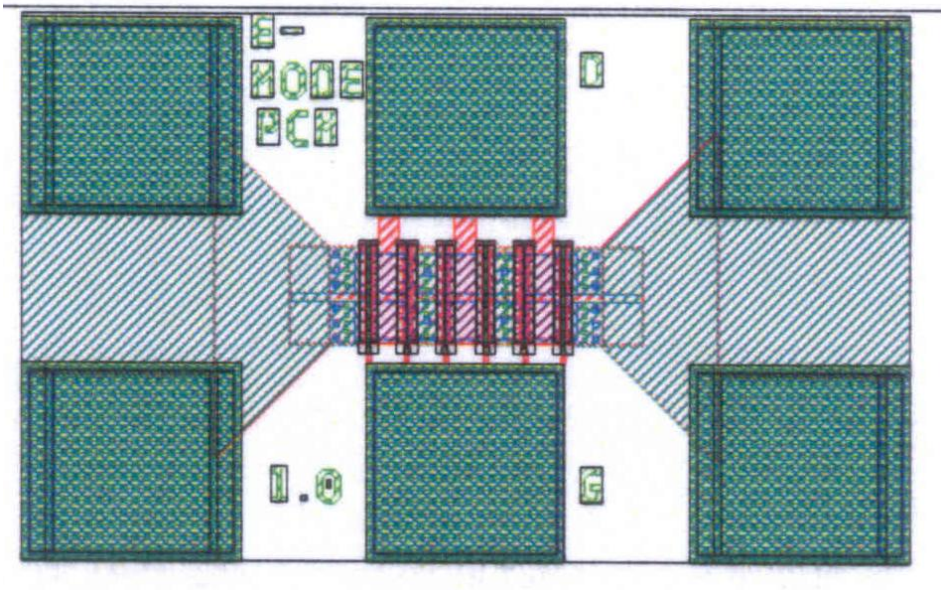
Variation of PA4 S22 Measured for 2005, 2006, and 2007 (solid).

Class Test Devices: Dmode and Emode 300 um PHEMTs

Several test structures were measured. There was very good agreement between given s-parameters and measured 300 um Dmode and Emode PHEMTs.

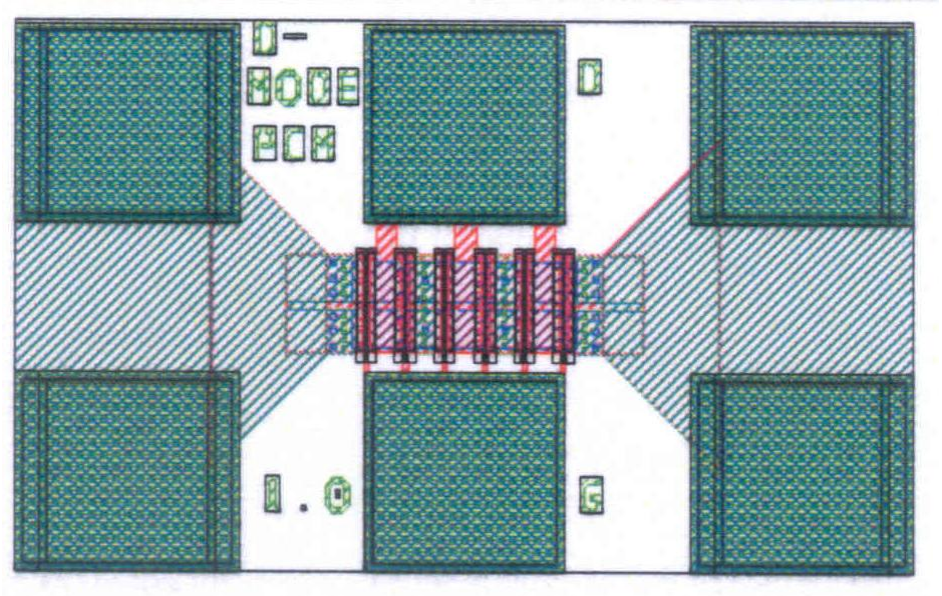
DC Biases for the Emode were:

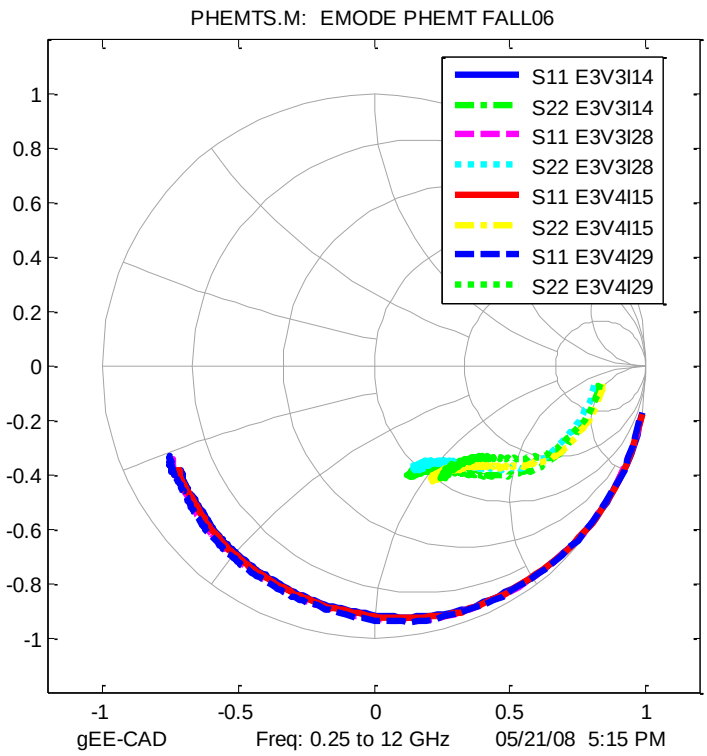
3V @ 14 mA	VG = +0.6V	E3V3I14
3V @ 28 mA	VG = +0.7V	E3V3I28
4V @ 15 mA	VG = +0.6V	E3V4I15
4V @ 29 mA	VG = +0.7V	E3V4I29



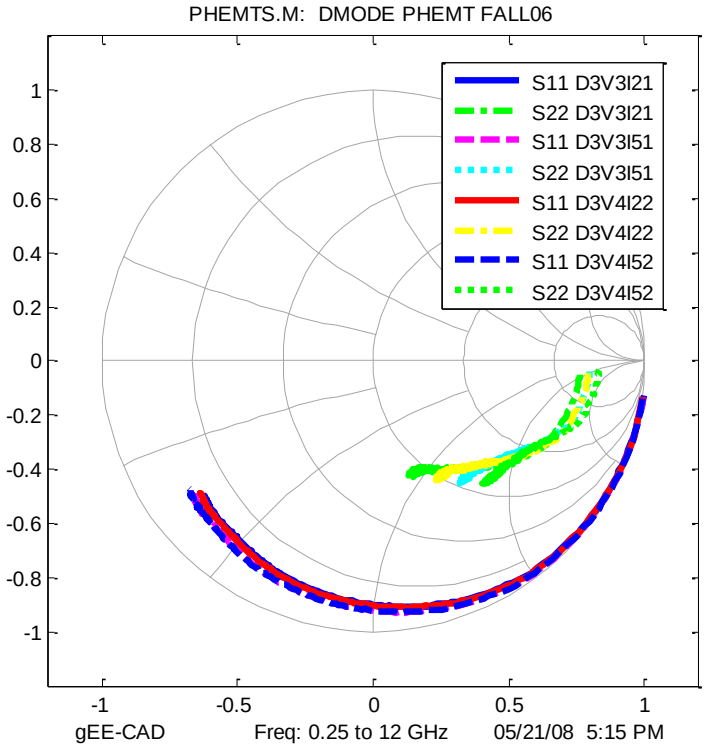
DC Biases for the Dmode were:

3V @ 21 mA	VG = -0.4V	D3V3I21
3V @ 51 mA	VG = -0.1V	D3V3I51
4V @ 22 mA	VG = -0.4V	D3V4I22
4V @ 52 mA	VG = -0.1V	D3V4I52

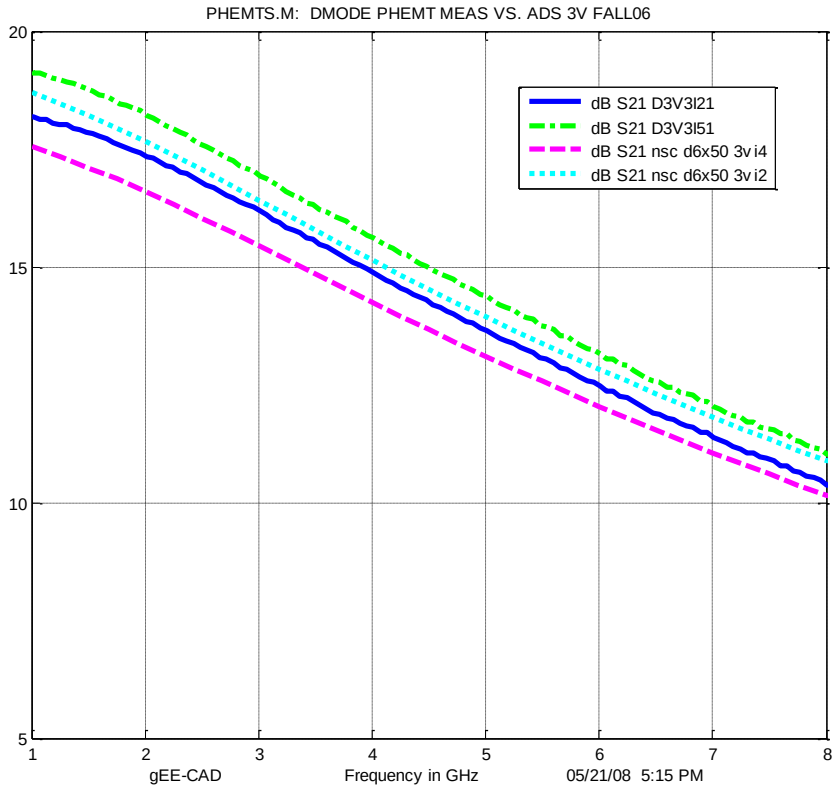




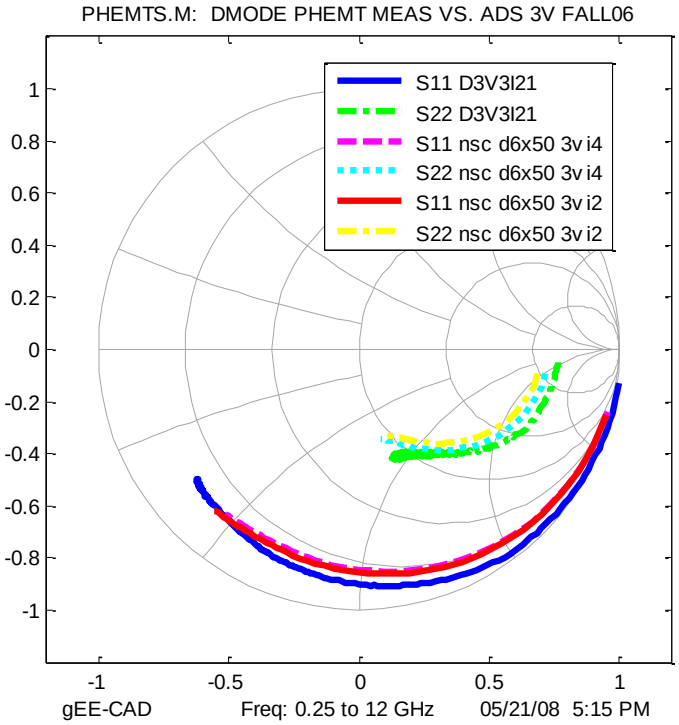
Emode Match 3V to 4V



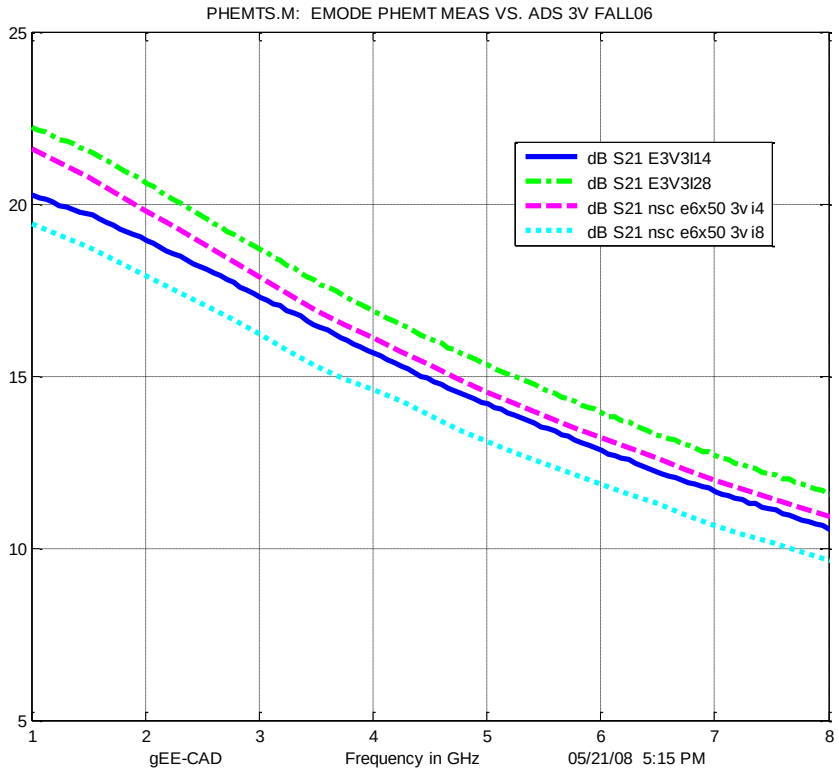
Dmode Match 3V to 4V



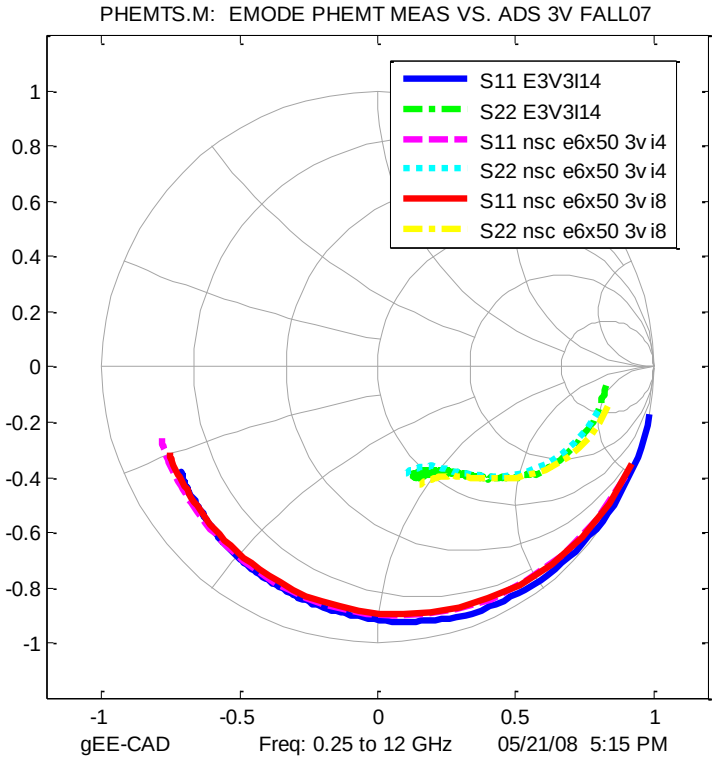
Dmode Gain S21 3V Measured vs. Linear TQS Files



Dmode Match S11/S22 3V Measured vs. Linear TQS Files



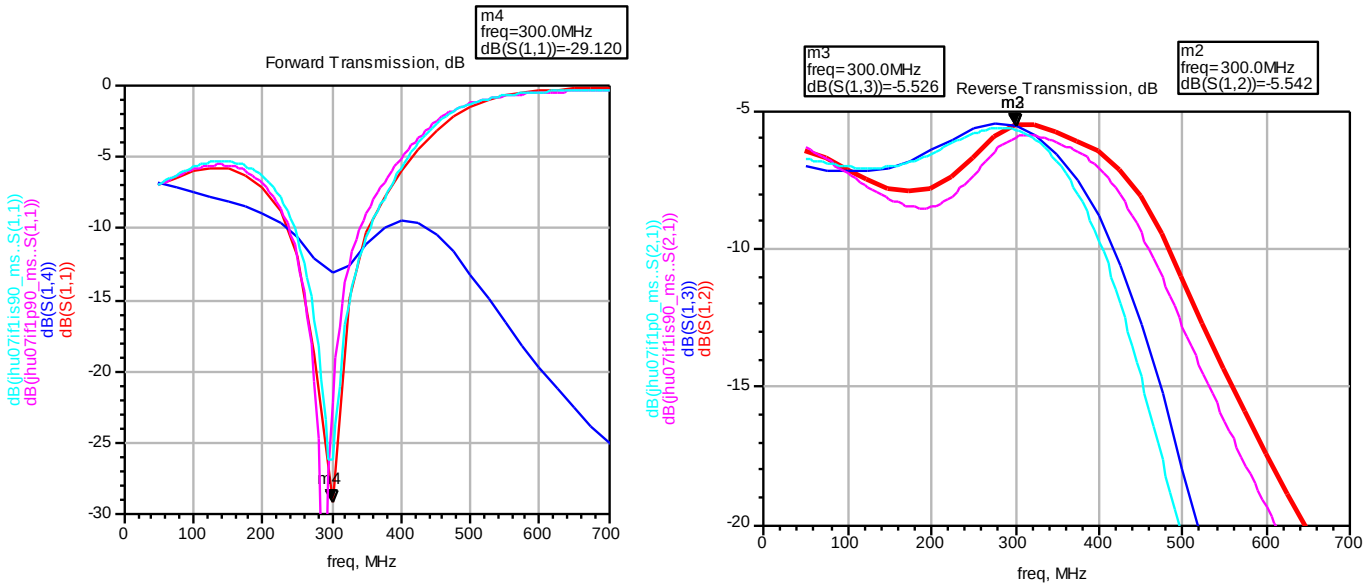
Emode Gain S21 3V Measured vs. Linear TQS Files



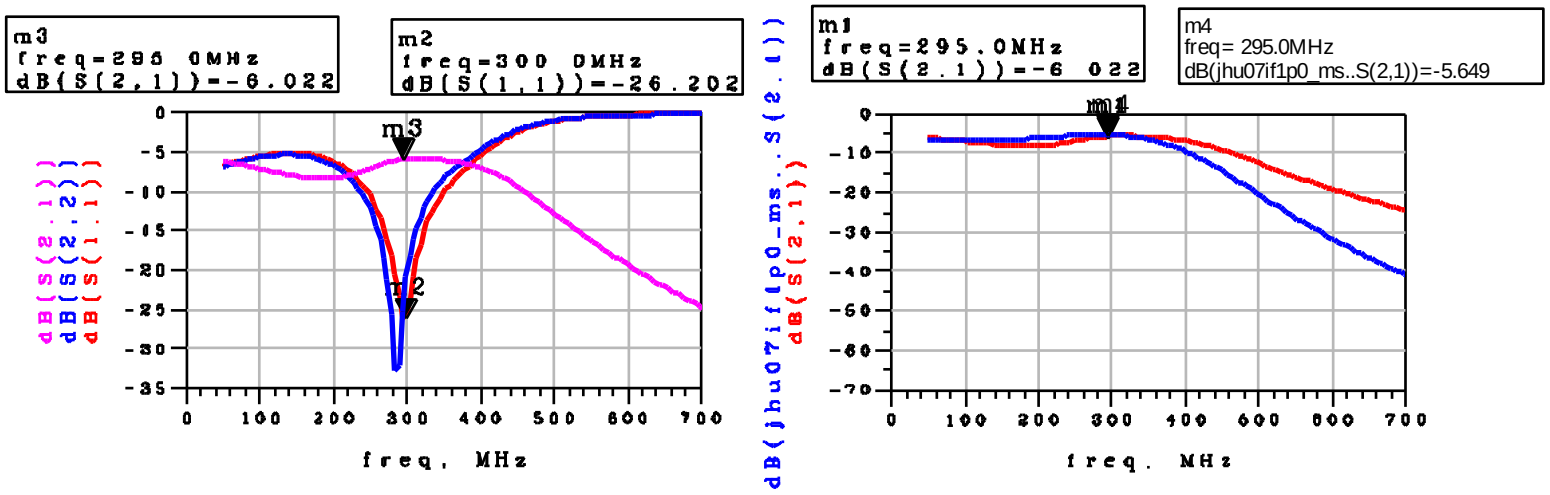
Emode Match S11/S22 3V Measured vs. Linear TQS Files

Class Design Examples: Branchline Hybrid for Image Reject Mixer (300 MHz) by John Penn

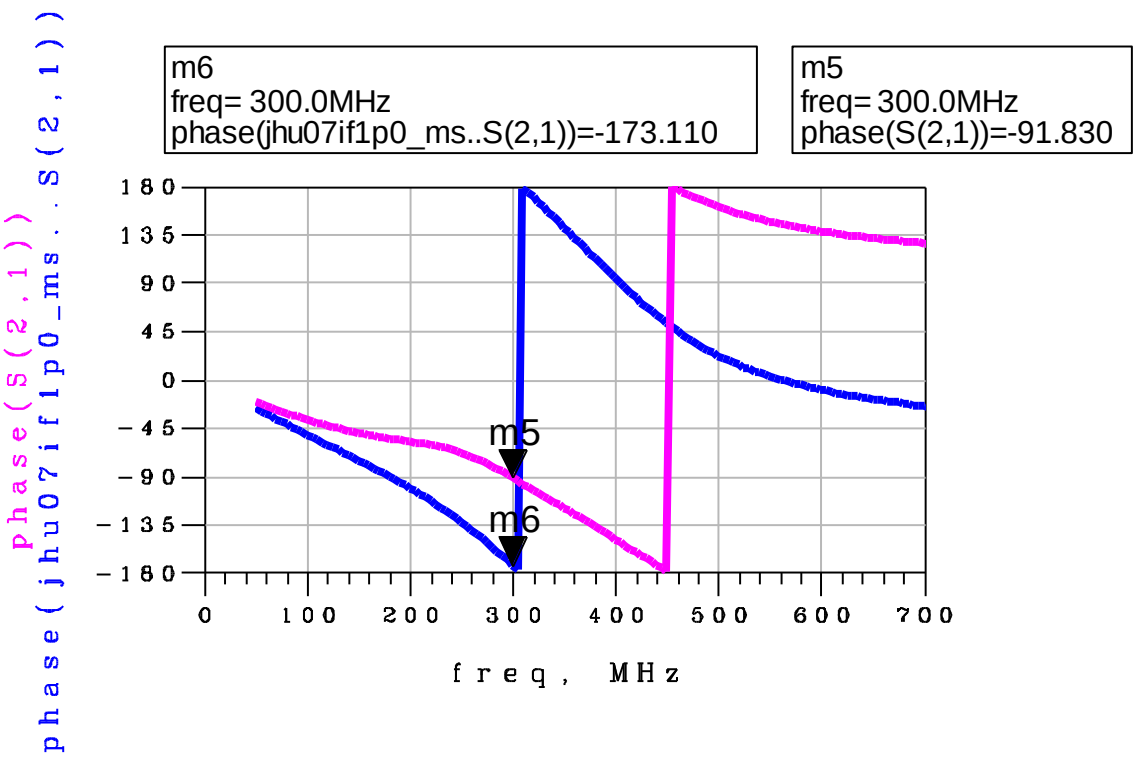
A student in the Fall 2007 MMIC Design course was interested in designing an image reject mixer, but then changed his project to a different topology. Since the branchline hybrid would have large inductor values for an IF combiner as the frequency got lower, an image reject mixer with an IF of 300 MHz was designed. The key limitation for the mixer was size and insertion loss in designing the IF branchline on a GaAs substrate. A couple of designs were performed trading off size versus insertion loss. Following are some measured results of a 300 MHz lumped element hybrid in 60x90 mil die size.



Measured versus Simulated Insertion Loss 300 MHz 90 degree hybrid in GaAs (60x90 mil die)



Measured Insertion Loss and Phase for 300 MHz 90 degree hybrid in GaAs (60x90 mil die)



Insertion Phase (Measured as 81.3 degrees at 300 MHz)