Fall 2012 JHU EE787 MMIC Design Student Projects
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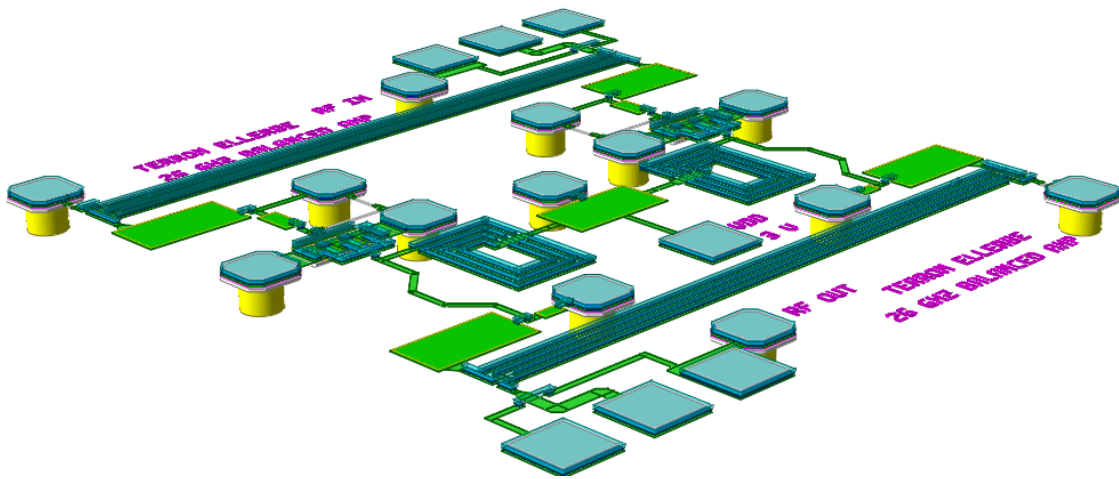
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BroadBand Low Noise Amplifier—John Novak

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Voltage Controlled Oscillator—Zach Ross

JHU12ALL Fall 2012 JHU MMIC Class
TriQuint TQP13 Quarter tile 5x10mm

26 GHz Balanced Amplifier

Terron Ellerbe

MMIC Design – EE 525.787

JHU Fall 2012

Abstract:

This report details the design of a K Band single stage balanced amplifier Monolithic Microwave Integrated Circuit (MMIC) utilizing 90 degree lange couplers. The 300 um amplifiers are designed to operate using a single 3V drain source. This circuit was designed using the TQP13 process and fits within the 60 mil x 60 mil Anachip layout.

1. **Introduction**

    Balanced amplifiers are devices that use ninety degree directional couplers with two identical amplifiers. This circuit takes advantage of the good input and output match and the wide bandwidth of the coupler to improve performance. Any mismatches that the amplifiers see at their input and output are canceled through the couplers in this balanced configuration, so it looks like the circuit is seeing 50 ohms. The balanced amp circuit yields approximately 3 dB more in output power compared to what a single amplifier will see.

2. **Design Approach**
    a. **Design Goals vs. Performance**

        Table 1 - Design Goals versus Expected Performance

Parameter	Design Goal	Expected Performance
Input Return Loss	> -20 dB	~ -21.8 dB
Output Return Loss	> -20 dB	~ -22.3 dB
Gain	> 8 dB	~ 8.5 dB
Noise Figure	< 4 dB	~2.5 dB
Peak Output Power	> 8 dBm	~ 9.6 dBm
Drain Voltage	3 V	3V
Layout	60 mil x 90 mil	60 mil x 60 mil

    b. **Tradeoffs**
        - For this design I went for a simultaneous conjugate match on the amplifier in order to try to attain the best gain and power available. I designed the amp so that the gain peaked at my desired frequency, but this was at the expense of having a more bandwidth.
        - By adding a second ground-via to the source in parallel with the first, I traded some stability on the small signal amplifier in order to achieve more gain by halving the inductance seen at the source.

    c. **Design Methodology**

The original goal of this project was to fit a 26 GHz balanced amplifier in a 60 mil x 90 mil anachip layout. The frequency 26 GHz was chosen due to the fact that it was close to the limit of the equipment available to test the circuit and the higher frequency gave me the best chance to fit the two couplers into the layout. The design of this circuit was done in two stages. The first step was to design the small signal amplifier and coupler circuits individually for performance and lay them out individually. Once these sub-circuits were complete the second step was to combine these circuits in a manner that allows the circuit to fit into the layout while maintaining performance.

Small Signal Amp Design

The first step in designing the small signal amplifier was to look at the stability of the pseudomorphic high electron mobility transistor (PHEMPT) and then add the matching circuitry.   Looking at the stability of the PHEMT device showed that I did not need a stabilizing resistor above 21 GHz, however a large shunt resistor was added to the gate of the PHEMT in order to keep the gate from floating. The next step was to design the input and output matching networks for the amplifier using ideal elements. The input was matched for the best available gain and the output was matched for the best available power. The input matching network consisted of a shunt 0.09 nH inductor and a series 1.41 pF capacitor. The output matching network consisted of series inductance of 0.355 nH and a shunt 0.19 pF capacitor.

The next step in designing the small signal amplifier was to replace the ideal matching elements with lossy elements and add the bias circuitry. The first step in converting the circuit from ideal elements to one using the TQP13 process was replacing the S parameter data for the PHEMT with TOM4 model. The ideal capacitors were replaced with TQP13 capacitors, the ideal inductors were replaced with TQP13 spirals and the ideal grounds were replaced with TQP13 vias. The TQP13 elements take into account resistive and reactive effects that the ideal elements do not, and due to these effects the passive elements needed to be tuned slightly to get the performance back to the same operating frequency. I chose to have the 300 um PHEMT biased at 3V and approximately 30 mA. When adding the DC circuitry to the amplifier I added a large inductor to act as a RF block and a large bypass capacitor. For this design only a drain voltage was added to get close to this bias point but in future iterations circuitry to add a gate supply will probably be added as well.

The final step in this design was to add interconnects and begin working on the circuit layout.   By having the design of the amplifier at 26 GHz, the interconnects needed for the circuit significantly shifted the operating range down in frequency. At

this frequency the interconnects needed to be as small as possible, however this was causing the design to be too compact and coupling between the lines became a concern. In order to avoid this issue I removed the inductor elements from the design and replaced them with microstrip lines of equivalent inductance and retuned the capacitors slightly to get the operating frequency back where I wanted it. This allowed me to keep my input and output match while spreading out the layout enough to avoid lines being too close and coupling with each other.

<u>Coupler Design</u>

For the coupler design I decided to go with the lange coupler instead of the branchline coupler because it would consume less space in the layout. The mlange component in Microwave Office was used to simulate the electrical performance of the lange coupler. The TXLine tool was used to determine a quarter-wave line at 26 GHz. This value used as a baseline for the coupler and then tuned to get the element back to the desired operational frequency range. A line width if 7 um and space of 8 um was chosen to get as close to 3 dB coupling as possible from the device.

<u>Balanced Amplifier Design</u>

With all of the individual circuits completed I placed the individual amplifier and lange coupler circuits in the same schematic. When adding the interconnects in between the sub-circuits and to the RF pads at the edge of the board I had to make sure that I kept the loss of these lines to a minimum so that my performance is not affected too much. In order to accomplish this I either kept lines as short as possible for the normal 10 um line width or made the lines wider for longer line runs. With the sub-circuits connected, the last item to add to the circuit was the ground via for the RF pads.

3. **Simulations**
   a. **Linear**
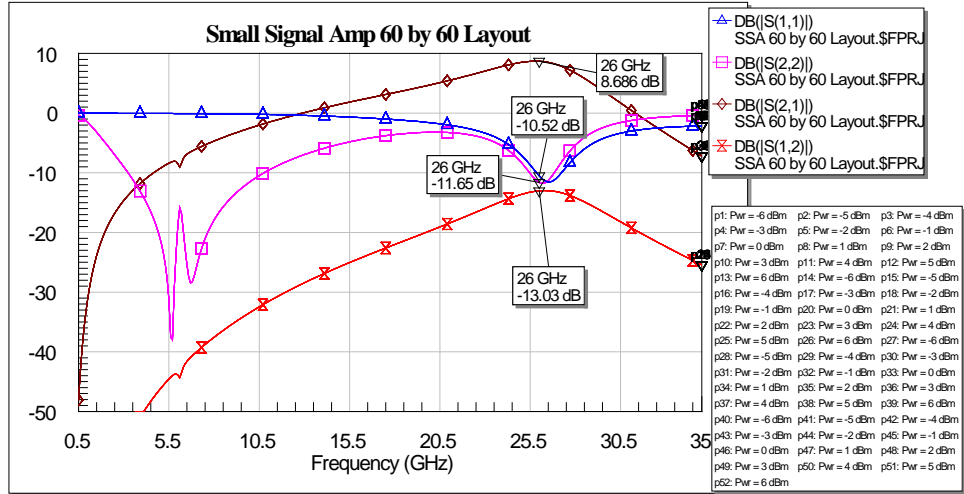   i. **Small Signal Amplifier**

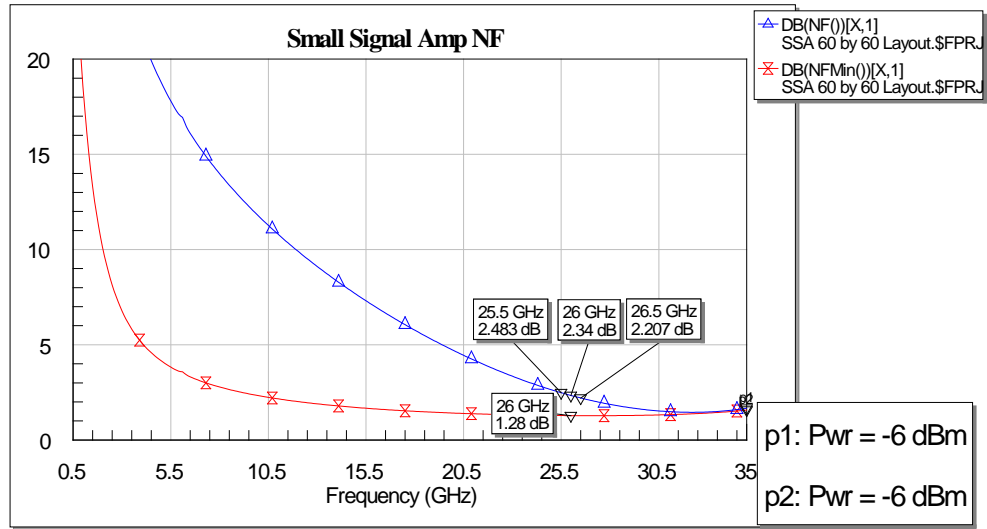**Figure 1 - Small Signal Amplifier S-Parameter Simulation Results**

Figure 2 - Small Signal Amplifier Noise Figure Simulation Results
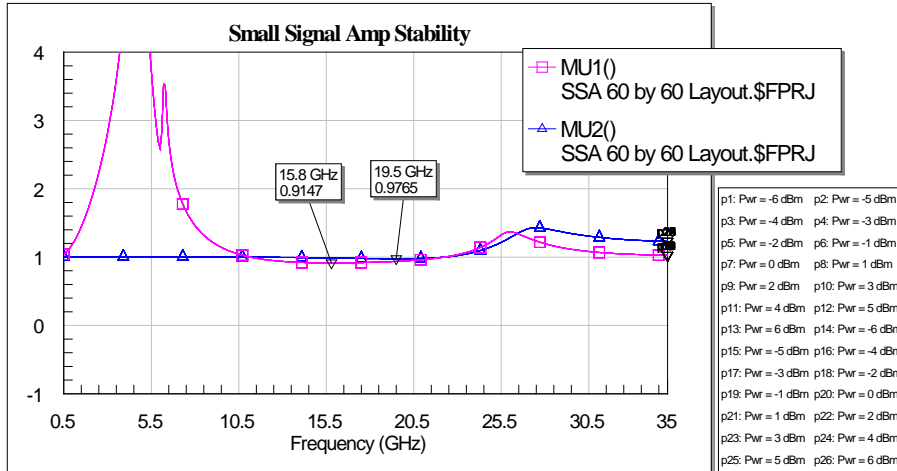
Figure 3 - Small Signal Amplifier Stability Simulation Results

The simulated results for the small signal amplifier show that the amplifier has 8.686 dB of gain at the desired frequency of 26 GHz, but the device is pretty narrow band. The input and output return loss is decent at -10.52 dB and -11.65 dB at 26 GHz and the noise figure less than 2.5 dB over the desired band. By adding the second via to the source of the PHEMPT I was able to achieve more gain for the circuit however, the stability of amplifier went from unconditionally stable up to 35 GHz conditionally stable from 10.5 GHz to 20.5 GHz and unconditionally everywhere else. I did not think this region of conditional stability would cause a problem because the return loss in that region did not go positive in that region. I also felt that the loss of the langes and the interconnects in the final circuit would help with stability.
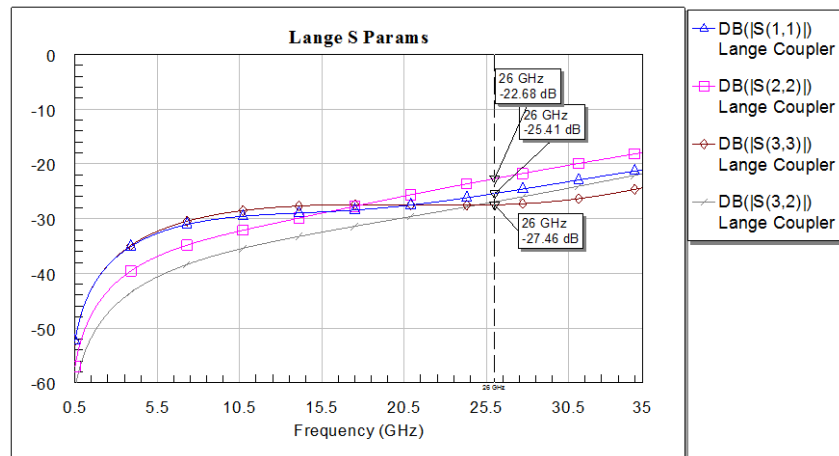
ii. Lange Coupler

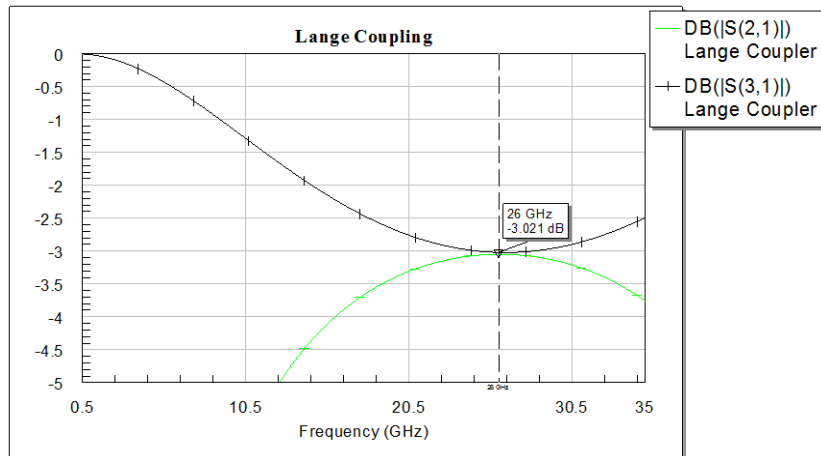**Figure 4 - Lange Coupler S-Parameter Simulation Results**

Figure 5 - Lange Coupler Insertion Loss and Coupling Simulation Results

The lange coupler has broader band performance and input and output return loss values that are better than -20 dB. The simulation also shows that coupling is very close to 3 dB which means that the power delivered to the two amplifiers will be divided evenly.
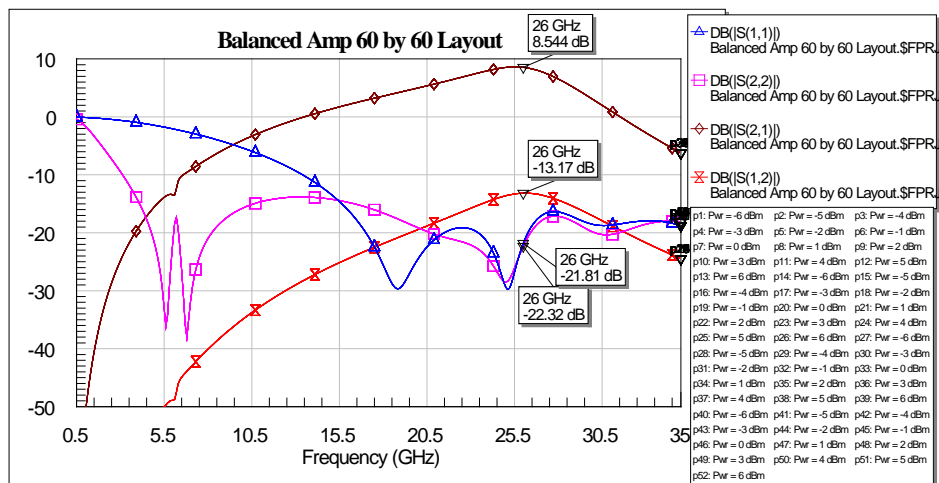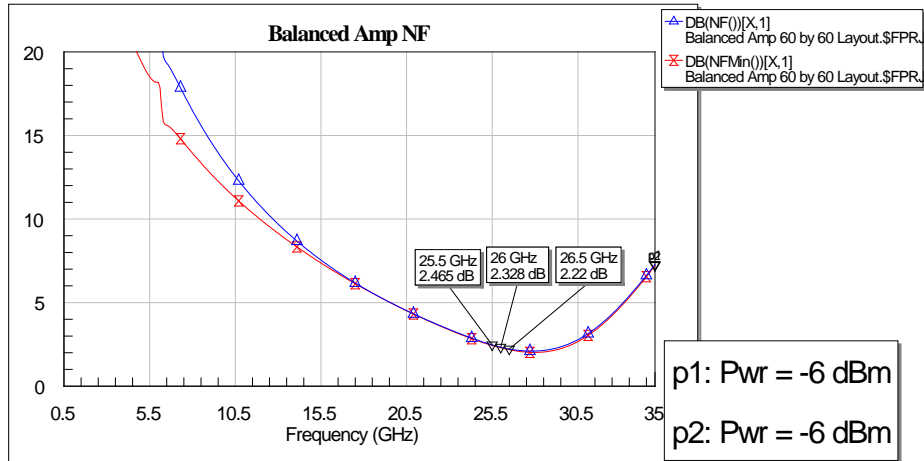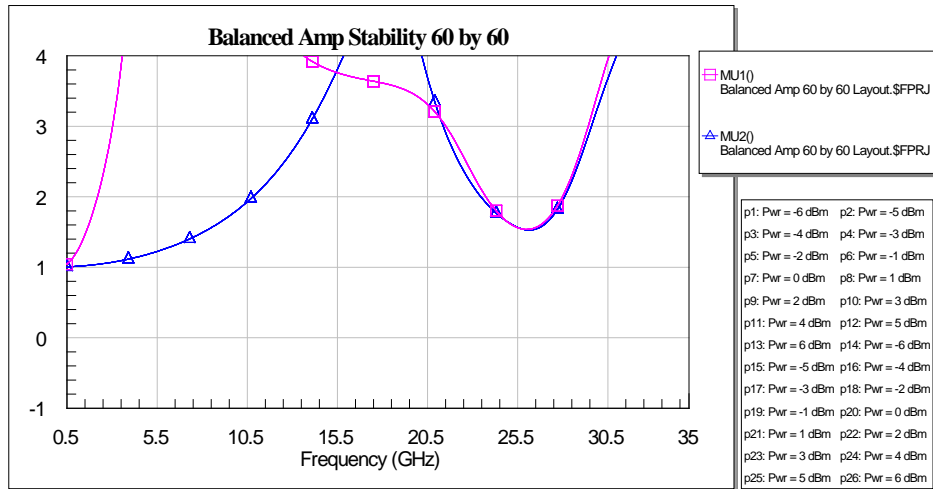
iii. <u>Balanced Amplifier</u>

Figure 6 - Balanced Amplifier S-Parameters Simulation Results

Figure 7 - Balanced Amplifier Noise Figure Simulation Results

Figure 8 - Balanced Amplifier Stability Simulation Results

The simulated results for the balanced amplifier show that the amplifier has 8.544 dB of gain at the desired frequency of 26 GHz. The input and output return loss improved to -21.81 dB and -22.32 dB at 26 GHz due to the return loss of the lange coupler.   The balanced amplifier still has a noise figure less than 2.5 dB over the desired band, but is unconditionally stable up to 35 GHz.

b. Non-Linear

When looking at the non linear performance of the individual small signal amplifier and the balanced amplifier the power of the device in both cases began to saturate and then continues to go linear. I don't believe that this behavior is real, but instead is an artifact of simulation having issues converging at these higher power levels. Assuming that the point where the power first starts the saturate is indeed correct, the peak output power for the small signal amplifier is 7.137 dBm and the peak output power for the balanced amplifier is 9.611 dBm.

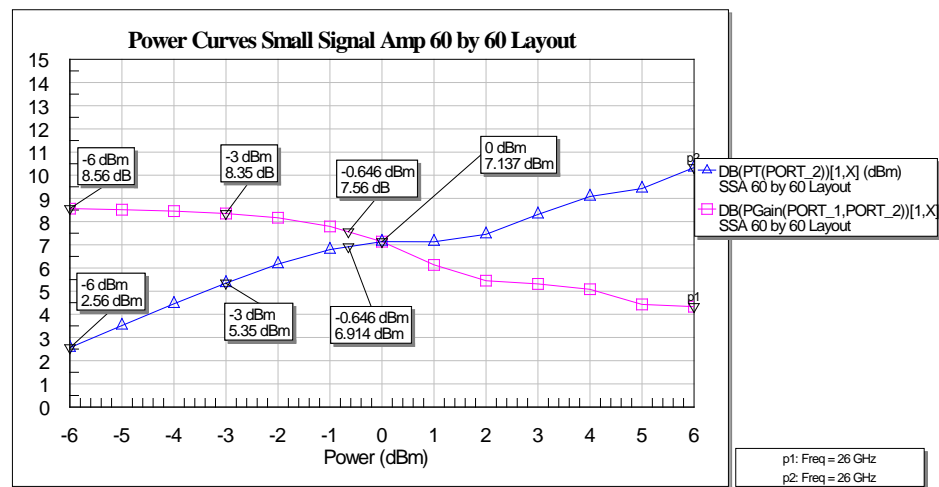### i. Small Signal Amplifier

Figure 9 - Small Signal Amplifier Power Simulation Results
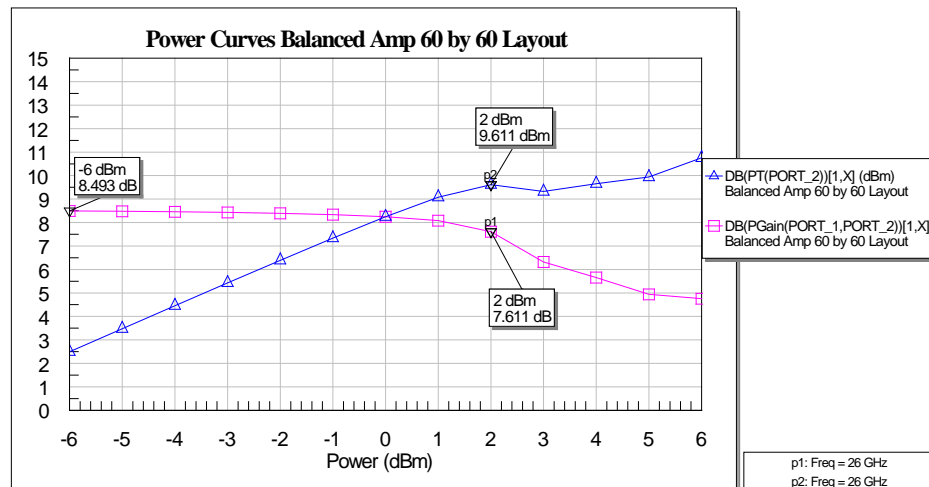
ii. Balanced Amplifier

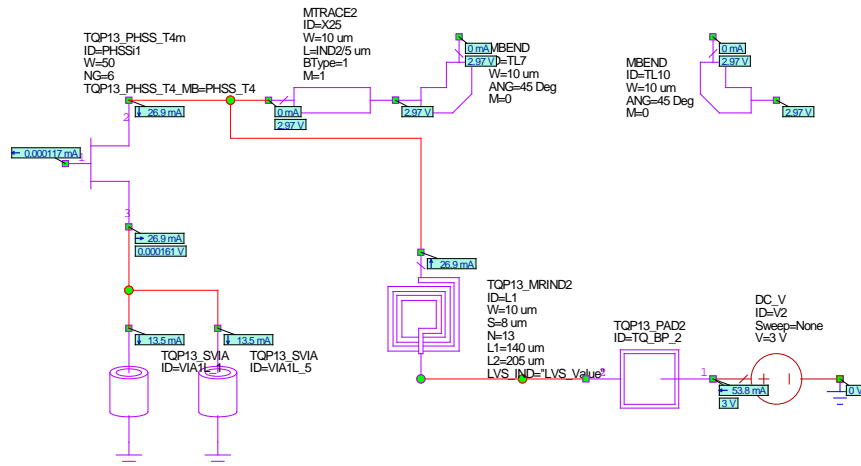**Figure 10 - Balanced Amplifier Power Simulation Results**

Figure 11 - Balanced Amplifier Bias Simulation

With only applying 3 volts applied to the Drain DC pad, the simulation is showing the device is operating at 2.97V and 26.9 mA. The addition of a small gate voltage would help get the circuit to the desired 3V, 30 mA operating point that was desired.
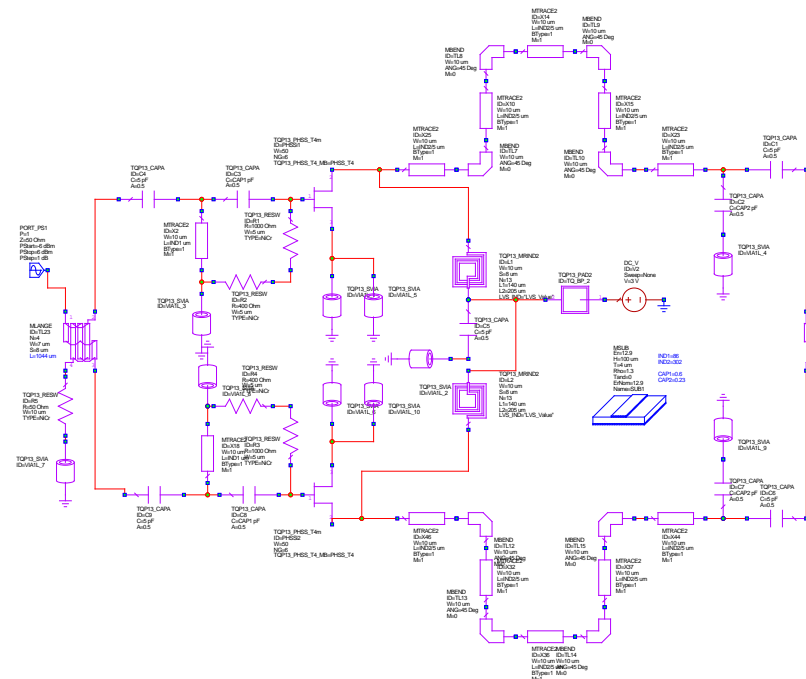
4. Schematic and Layout

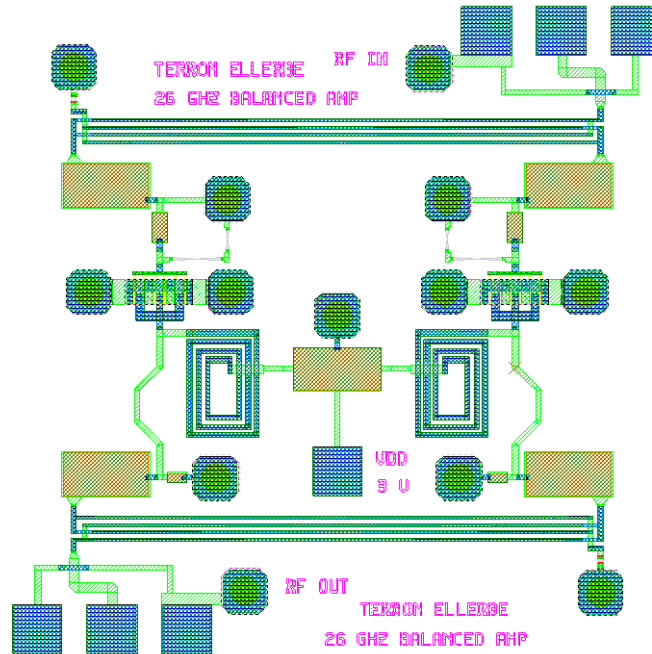**Figure 12 - Balanced Amp Layout Schematic without interconnects**

Figure 13 - Balanced Amp Layout

5. Test Plan

S-Parameter and Power Measurement:

1. Using a power supply and a needle probe apply 3V to the drain of the balanced amp.
2. Add Ground-Signal-Ground (GSG) probes to the network analyzer input and output cables.
3. Characterize cable loss so that it can be taken removed from the measurement results.
4. Apply GSG probes to the RF input and the RF output of the chip
5. Calibrate the Network Analyzer to sweep frequency from 25.5 GHz to 26.5 GHz in 0.1 GHz steps with the input power level set to -6 dBm and take S-Parameter data.
6. Set the network analyzer to 26 GHz and the input power level of -6 dBm and measure the output power.
7. Slowly increase the input power in 1 dB steps and measure the output power at each point until the device compresses.

Noise Figure Measurement:

1. Using a power supply and a needle probe apply 3V to the drain of the balanced amp.
2. Connect a noise source to the input of the circuit and connect the output of the circuit to a noise figure analyzer.
3. Configure the noise figure analyzer to take noise figure measurements from 25.5 GHz to 26.5 GHz.

6. **Summary and Conclusions**

The design met the performance goals that I set for the balanced amp and was able to fit into a smaller layout foot print than I was originally expecting. The next step for this iteration of the design would be running an electromagnetic simulation on the circuit to make sure the circuit will behave as expected. For a second iteration of this design I would look into using the space in the layout more efficiently. This would allow me to broaden the bandwidth of the device by using more elements in the matching networks and add DC circuitry to the gate of the PHEMTs for the addition of a potential gate supply.

2-20GHz LNA Project

525.787 MMIC Design

Brandon Butterworth

Fall 2012

Abstract

The design in this report is a cascode distributed amplifier. The goal of the design was to create an amplifier with a noise figure of <3dB, while still maintaining an output compression point of 17dBm over the range of 2-20GHz. The process used is Triquint's TQP13, and the simulations were performed in Agilent's ADS 2011.10. The final amplifier has >13dB of gain over process variations, an excellent match on the output, and a typical noise figure of 2.0dB.

Introduction

This report outlines the design approach taken for a distributed cascode amplifier, as well as the final results. Included are Monte Carlo simulations, as well as the expected test plan as soon as the die is fabricated. Overall, the simulations appear to be promising for a decent amplifier. Nominally the gain is greater than 14.5dB over the range of 2-20GHz, with a return loss of <-15dB. Furthermore, the noise figure is less than 3dB over the frequency of interest.

Design Approach

The design approach for this amplifier was to initially get a rough idea on what is achievable in this process, and whether the specification and goals seem realistic. So a rough sketch of a distributed amplifier, without any interconnect, was performed. This initial design, which unfortunately was not saved, proved that the design goals seem to be achievable, all except for the gain that I wanted out of the amplifier. The initial distributed amplifier only had 4 stages, and had about 10dB of gain at 20GHz. This was using a 50um, 6 fingered device.

After this point, there was an investigation into a cascade topology. This approach seemed very promising, until I could not get an oscillation quelled at 28GHz once interconnects were added. Cleaning up the layout proved to remove the high frequency oscillations. Ultimately, I adjusted the size of the transistor from 50um, 6 fingers down to 40um, 6 fingers to improve the output return loss.

The final cascode distributed amplifier has a few slight adjustments to the cookbook distributed amplifier topology. The first noticeable change is the termination resistor on the input transmission line. The noise from the 50 ohm termination resistor was dominating the noise figure at low frequencies. This termination resistor as a result was increased in order to decrease the contributions from this noise source. An alternative method that was investigated was to use an active termination, but in order to simplify the biasing, the larger resistor was instead used. As you can see below, at low frequencies the degradation of the noise figure when decreasing the gate line terminating resistor from 70 ohms to 50 ohms is on the order of 0.6dB. The degradation in input return loss was about 2dB. The trade-off therefore was made to degrade the input return loss in order to improve the low frequency noise figure.
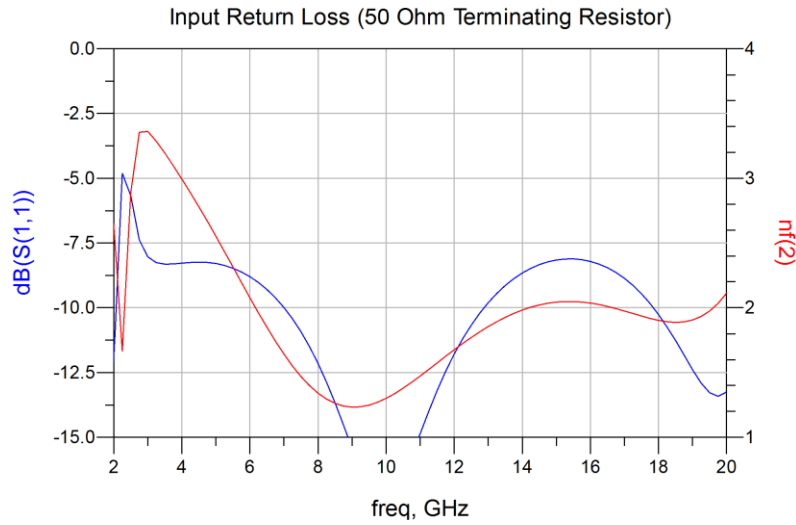
Input Return Loss (50 Ohm Terminating Resistor)

Figure 1 Input Return Loss and Noise Figure (50 Ohm Input Term)

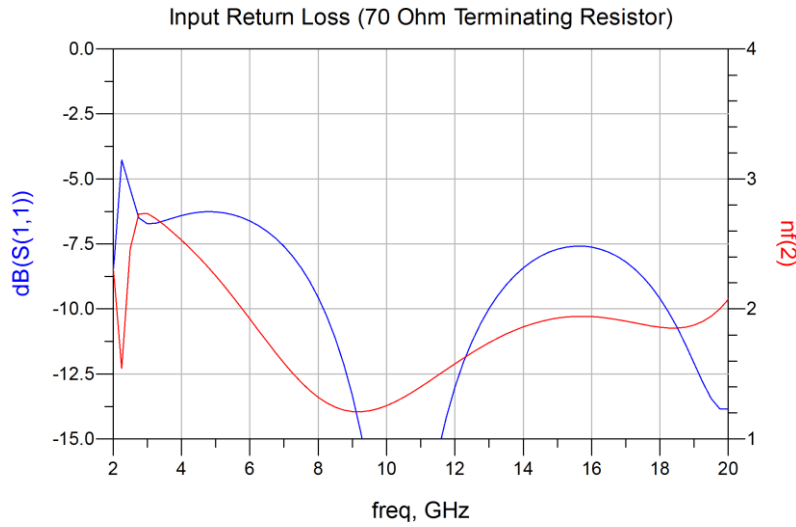Input Return Loss (70 Ohm Terminating Resistor)

Figure 2 Input Return Loss and Noise Figure (70 Ohm Input Term)

Another problem that came up during the design process was the lack of space on the Anachip. As a result, I am missing two inductors on the gate transmission line that could have optimized the gain and return loss of the amplifier.

Parameter	Specification	Goal
Operating Frequency	2 to 20GHz	1 to 22GHz
Gain, S21	> 12dB	>15dB
NF	<3.0dB	<2.5dB
S11	<-5dB	<-10dB
S22	<-10dB	<-15dB
Output P1dB	>+17dBm	>+17dBm
Stability	Unconditionally Stable	Unconditionally Stable
Power Consumption	None	<500mW

Schematic

A simplified schematic is shown below for the cascode distributed amplifier.   Not shown below are the drain stabilization resistors. One note about the schematic is the topic of biasing. Both Vdd and Vgg1 require low frequency terminations in order for this amplifier to work well below 2GHz. The simulations in this report are assuming a low frequency termination, with values of 1000pF and 100pF. The simulations do incorporate 0.4nH of bondwire inductance, as well as an inductance in the capacitors on the order of 0.45nH. None the less if one was to bias the amplifier through the Vdd port, the required voltage is 9V due to the drop across the 50 ohm termination. If a designer does not want to consume 9V @ 65mA, an external bias tee can be used on the RF out port. This will cause the amplifier to operate at 6V 65mA. This reduces the power used of this amplifier from 620mW to 390mW.
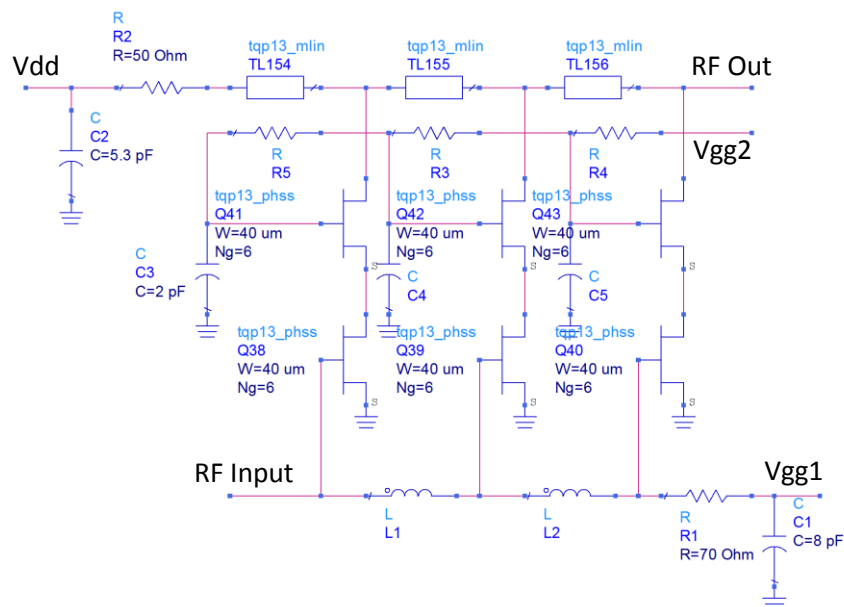

Figure 3 Simplified Schematic

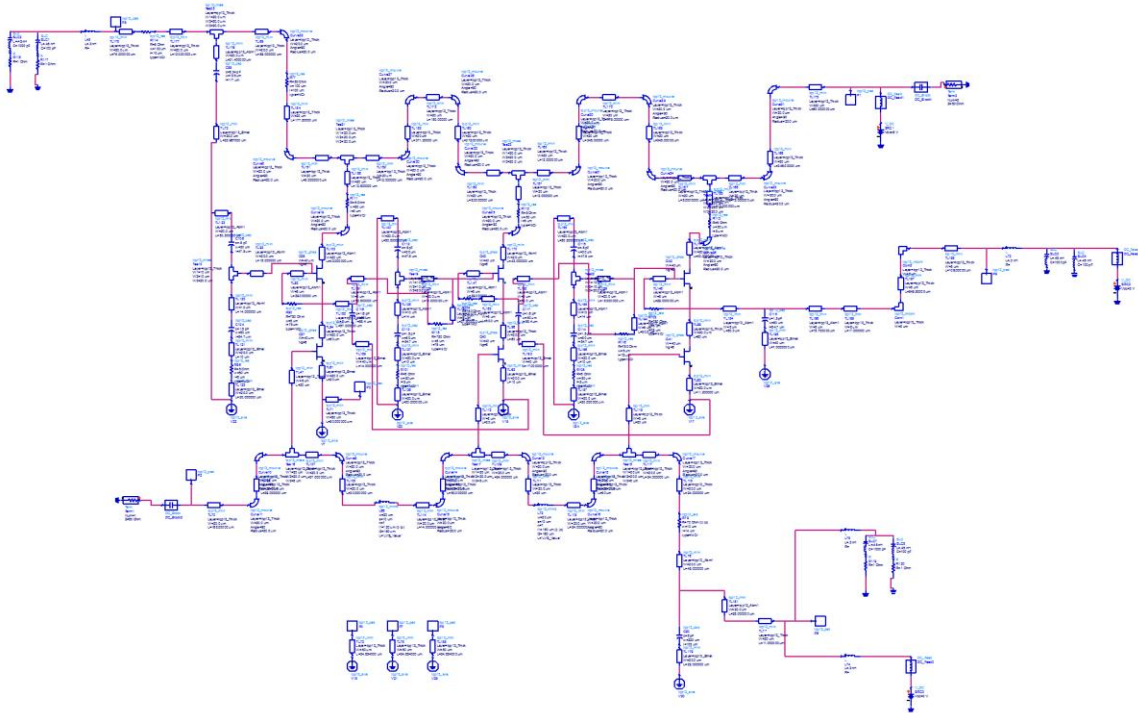The full-schematic is below, including all of the interconnects.

Figure 4 Uncensored Schematic

Simulations

The S-Parameters, and noise figure is below. These results are using the TOM4 Triquint Nonlinear model. The gain of the distributed amplifier is not necessarily flat, but it was not one of the design elements that I placed much emphasis on.
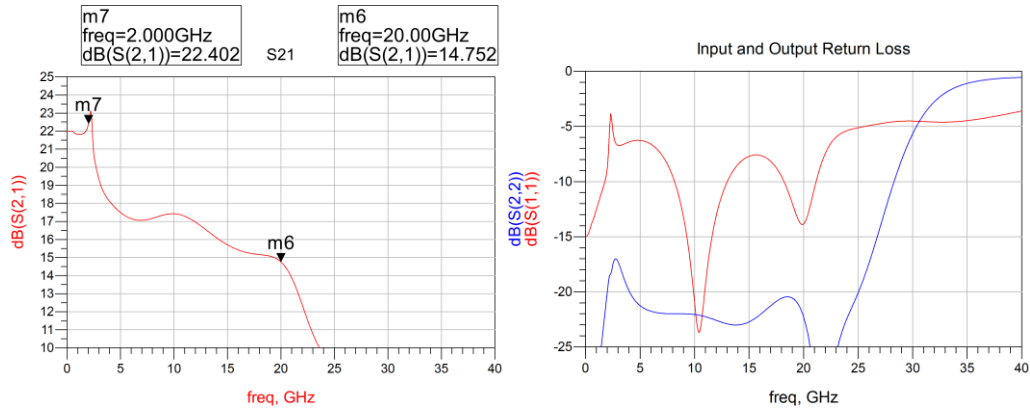

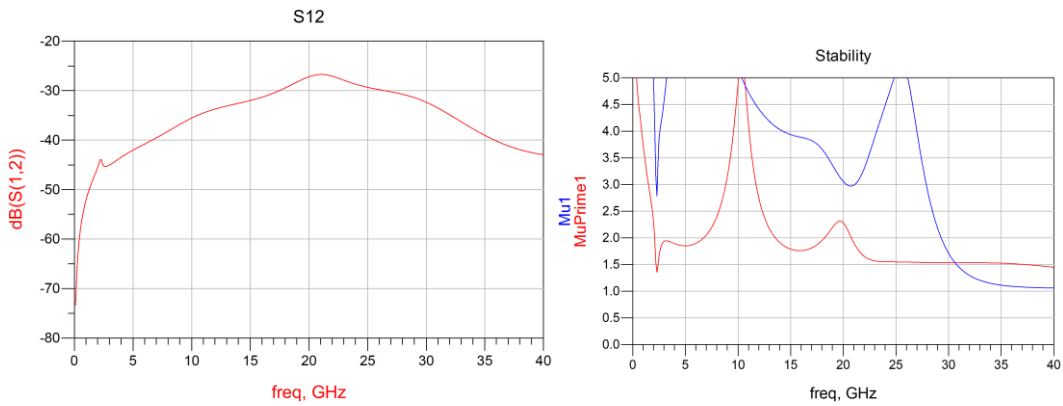
Figure 5 S21 and Input/Output Return Loss

Figure 6 Uncensored Schematic

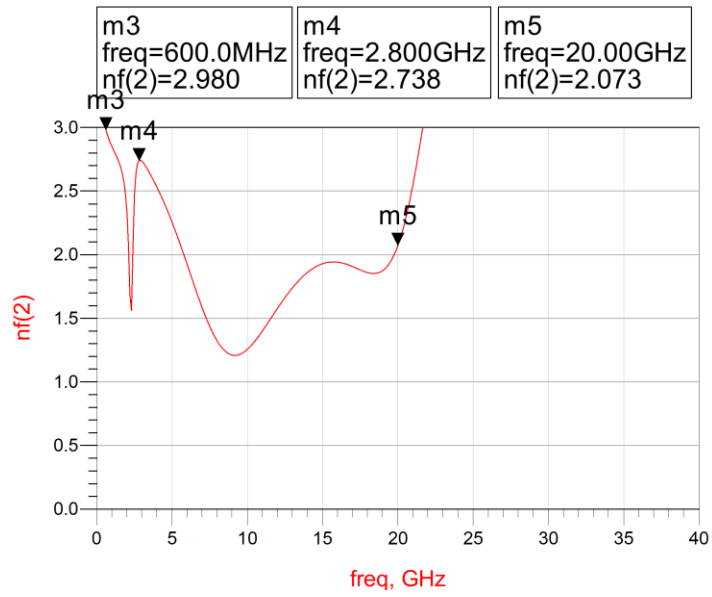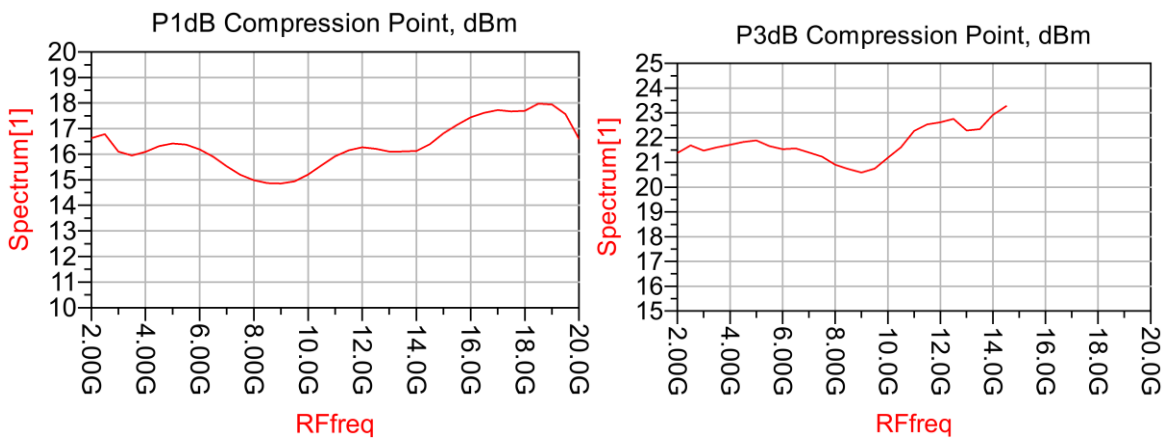| m3	m4	m5
freq=600.0MHz	freq=2.800GHz	freq=20.00GHz
nf(2)=2.980	nf(2)=2.738	nf(2)=2.073

Figure 7 Noise Figure

Figure 8 Compression Points

As a final part of this project, I also decided to perform a Monte Carlo analysis using historically measured values. This Monte Carlo analysis was performed after the submission of the layout. I performed a post-production optimization to the gate voltage of the bottom-FET, and simply added 3V to Vgg1 in order to get Vgg2. The Monte Carlo results are below, and it shows some wide variability due to process sensitivities, and the lack of feedback. The units for the post production current plot below are in Amps.
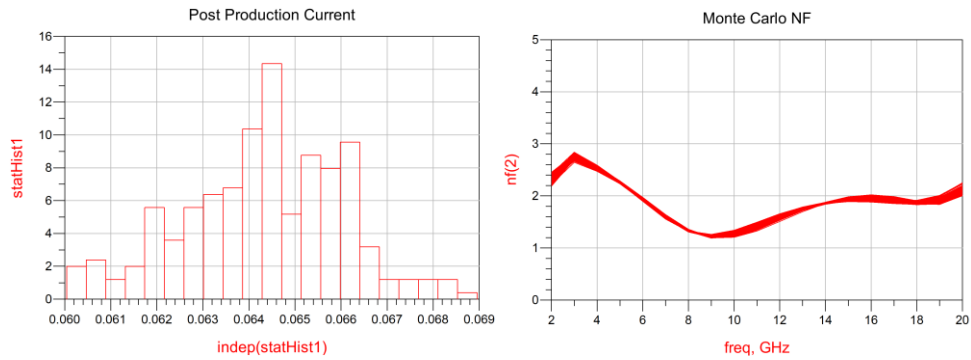

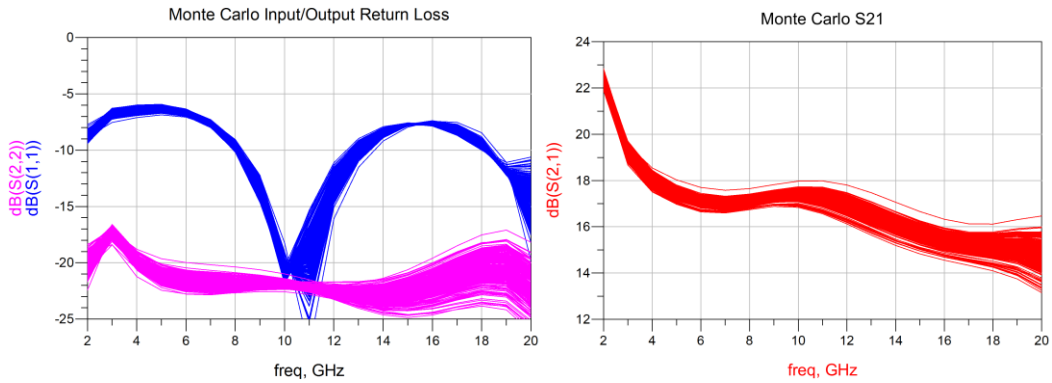**Figure 9 Monte Carlo of Noise Figure and Current(After Gate Voltage Adjust)**
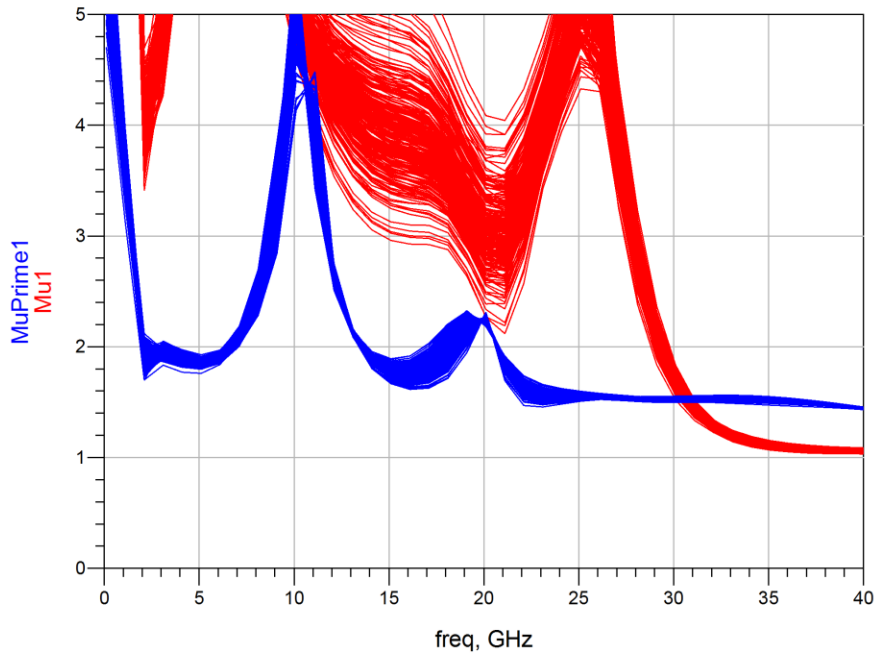

Figure 10 Monte Carlo of S-Parameters

Figure 11 Monte Carlo of Stability

Layout

VDD = 9.5V AT 65MA
-OR- LOW FREQ TERM

EXTERNAL BIAS AT 6V 65MA
RF OUTPUT

RF INPUT

B. BUTTERWORTH
2-20GHZ AMP

VG1   VG2

♦ JHU12BBU
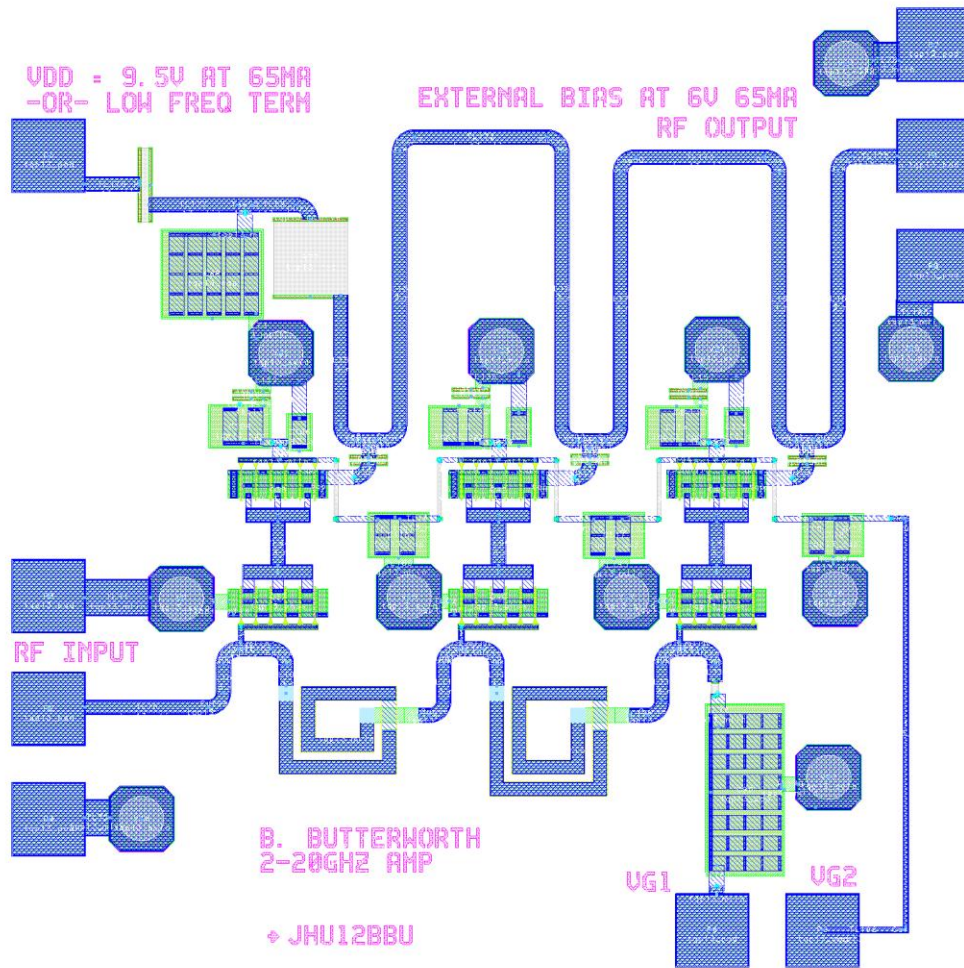
Test Plan

Expected Equipment Requirements:

- 3 DC Probes (Vgg1, Vgg2, Vdd)
- Three RF Probes
- Noise Diode/Analyzer
- Signal Generator
- Network Analyzer
- Spectrum Analyzer

There will be three measurements to be performed. The measurements are to characterize the S-Parameters, the noise, and finally the compression of the amplifier. These various measurements are outlined below, but they all follow the following biasing procedure. These instructions assumes the tester understands that cables are required between the test equipment, and by no means are these instructions intended for a person that doesn't know what RF stands for.

Biasing Procedure

Set Vgg1 to 0V, and Vgg2 toVgg1+3V. If you are biasing from the Vdd line, slowly increase the voltage to 9.25V. Adjust Vgg1 until you get to a quiescent current of 65mA. Maintain the Vgg2=Vgg1+3.0V relationship.

S-Parameter Measurement

Connect the amplifier to the network analyzer using the probe-station. Make sure the input power into the amplifier is <-10dBm in order to accurately measure the small-signal parameters. Furthermore, ensure the network analyzer is properly calibrated. The exact calibration is to be determined.

Noise Figure Measurement

Calibrate the noise figure (ie perform a 2nd stage correction). This removes the noise contribution of the spectrum analyzer or the noise figure meter. From there, connect and bias the amplifier, and measure the noise figure of the device.

Compression Measurement

Determine the losses/inaccuracies out of the signal generator and into the spectrum analyzer over the frequency range of 2-20GHz. Record these values. Sweep in the input power into the amplifier until the gain of the amplifier drops by 3dB. Record the 1dB and 3dB compression points. Perform this measurement between 2-20GHz.

Summary and Conclusions

The table at the end of this section summarizes the design, with that of the specifications and goal. All except for the output power are taken over the process variation.
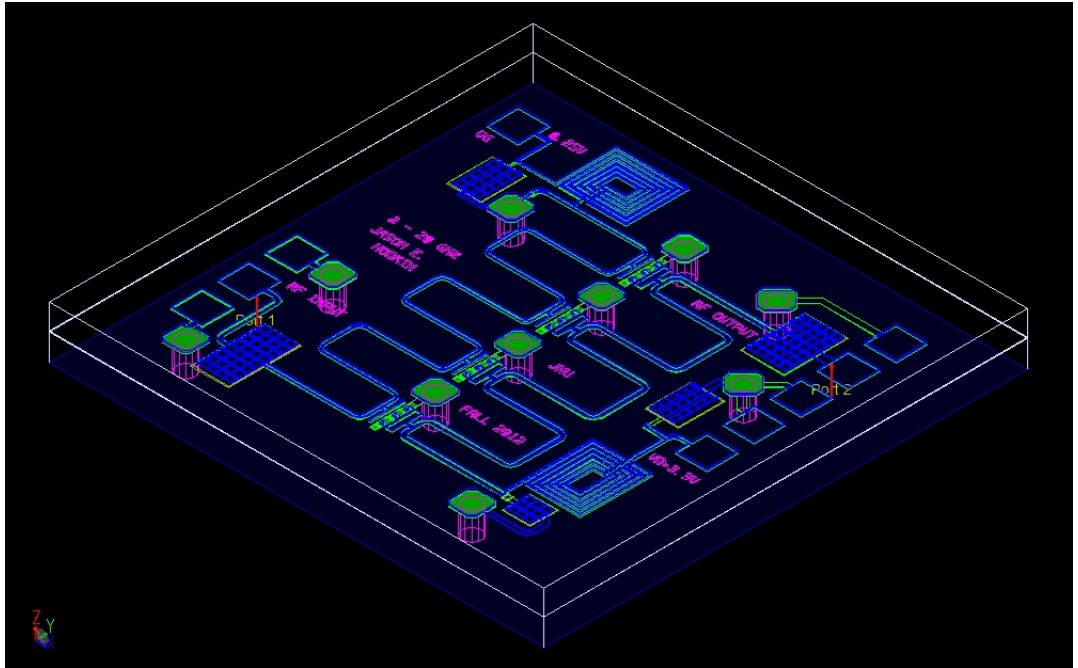
The gain meets the specification, but does not completely hit the goal of 15dB at 20GHz over process variations. This is a little disappointing, but overall the design appears to be relatively solid. Typically that amplifier has a 2.0dB noise figure, output return loss at the worst case is -16.5dB. The output power does miss its specification and goal. This was observed after the submission of the layout. In retrospect, larger transistors may help optimize the output power for the distributed amplifier.

Parameter	Specification	Goal	Design
Operating Frequency	2 to 20GHz	1 to 22GHz	
Gain, S21	> 12dB	>15dB	13dB @ 20GHz Over Process Variations
NF	<3.0dB	<2.5dB	<2.9dB Worst Case <2.0dB typical
S11	<-5dB	<-10dB	<-5.7dB
S22	<-10dB	<-15dB	<-16.5dB
Output P1dB	>+17dBm	>+17dBm	>14.8dBm worst case >16dBm typical
Stability	Unconditionally Stable	Unconditionally Stable	Unconditionally Stable
Power Consumption	None	<500mW	390mW with external bias tee 600mW without external bias tee

2-20 GHz Distributed Amplifier MMIC Design

Jason E. Hodkin

December 8, 2012

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1 Abstract

The distributed amplifier architecture, shown in figure 1, is adopted for a wide-band amplifier design utilizing an advanced low-cost GaAs PHEMT process for high frequency applications. The mmic design utilizes distributed elements for inductive sections, and achieves a moderate gain and output power with reasonable input and output return loss, while only utilizing four devices.
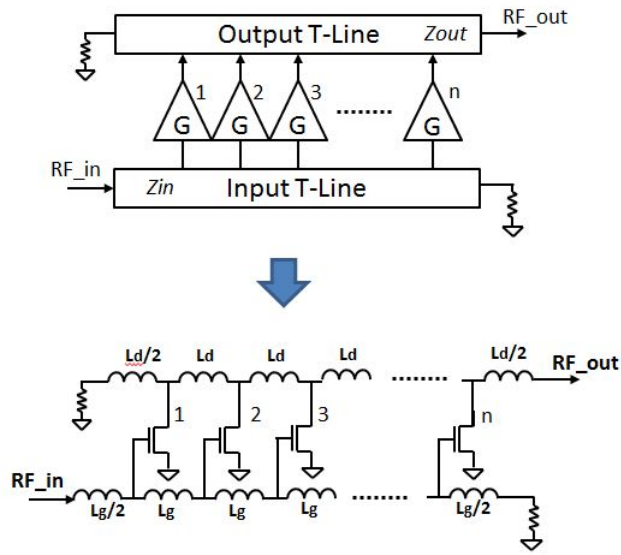
Figure 1: Distributed amplifier block diagram and FET implementation

2 Introduction

The distributed amplifier has been utilized to achieve amplification since the early 20th century[1]. The distributed amplifier as a wide-band amplifier was most notably described by a co-founder of Hewlett-Packard Company[2]. An excellent overview of distributed amplifier mmic design can be found in [3]. The basic underlying concept of the design of a distributed amplifier is the utilization of transistor device capacitances in the synthesis of input and output transmission lines, which effectively acts to absorb device reactive parasitics, enabling wide-band operation. The synthesis of this artificial transmission line involves utilizing the gate capacitance (Cgs) or drain capacitance (Cds) of the FET device in lumped element form of a transmission line, figure 2. This lumped element perspective, however, does not eliminate the use of distributed elements in achieving the required inductance, as will be shown in later sections of this document.

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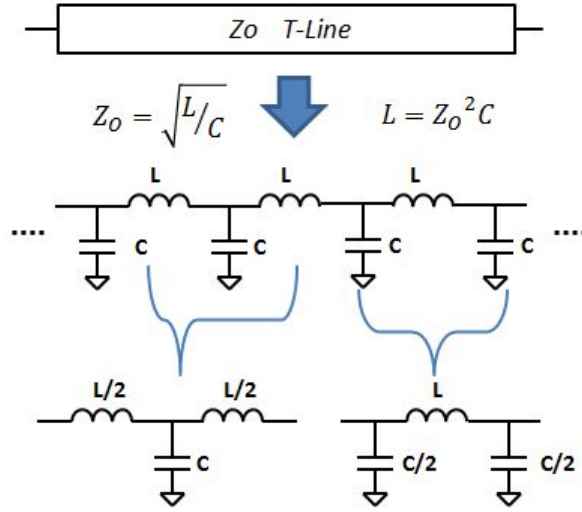
Figure 2: Transmission Line implementation options with lumped elements for distributed amplifiers

The fundamental principle in achieving wide-band operation with this architecture is found by considering the Bode-Fano relation in equation 1 and the linear circuit model of a FET device, figure 3.

$$\int_0^\infty \ln \left| \frac{1}{\Gamma(\omega)} \right| d\omega \leq \frac{\pi}{R_{ds}C_{ds}} \tag{1}$$
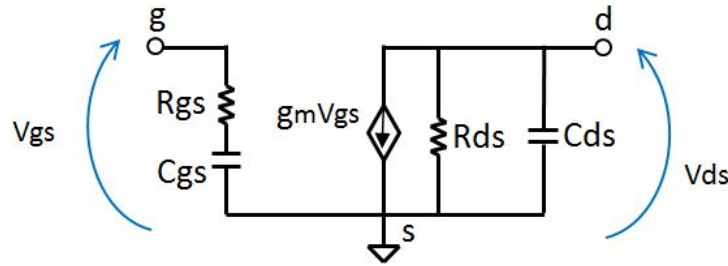
Figure 3: Linear FET model

In terms of the output transmission line for a distributed amplifier, evaluating the integral as described in [4] , gives the bandwidth (BW), as a function of the drain impedance of the device as shown in equation 2. For an assumed constant return loss (RL), as $C_{ds} \to 0$ then $BW \to \infty$. Ideally, achieving $C_{ds} = 0$

5

(or $C_{gs} = 0$ in the case of the input gate line) is accomplished by absorbing the capacitance into the matching network.

$$BW \leq \frac{1}{2R_{ds}C_{ds}\ln|^1/\Gamma|} = \frac{4.343}{R_{ds}C_{ds}RL(dB)} \qquad (2)$$

Since the goal of the distributed amplifier design is to synthesize an input gate transmission line and output drain transmission line utilizing capacitive parasitics, the lumped element equivalent circuit of a transmission line provides the means to absorb device capacitances. This design approach is detailed in following sections.

3   Design Approach

3.1   Design Goals

The distributed amplifier was designed to meet or exceed the design goals of table 1.

Band	2 - 20	[GHz]
Gain	> 8	[dB]
Gain Flatness	±1.5	[dB]
Return Loss, in or out	> 8	[dB]
OTOI	>30	[dBm]
OP1dB	>17	[dB]
Chip Size	1.5x1.5	[mm^2]

Table 1: Distributed Amplifier MMIC Design Goals

3.2   Device Size and Bias

A Class-A bias was utilized and sizing of the device started by assuming a Bragg cutoff frequency (fco) of 20.5GHz, equation 3, and a linear device simulation showed that the largest device possible was 6x23um. However, in order to ensure wide-band operation while also maintaining device size amenable to a low number of stages, a 6x20um (or 120um) device was chosen for this design. This device size provides significant margin on cutoff, resulting in fco=25.36 GHz. It should be noted that a fundamental trade-off with this amplifier architecture resides in the device sizing for wide-band operation and the device periphery typically desired for high power or high linearity operation. It was found that for these devices the high frequency operation was limited by Cgs, that is, Cgs>Cds. The details of the Class-A bias can be seen in figure 4, where Vgs=0.25V with Vds=3.0V at Ids=27mA , with a resulting a load-line resistance of approximately 75.6 Ohms.

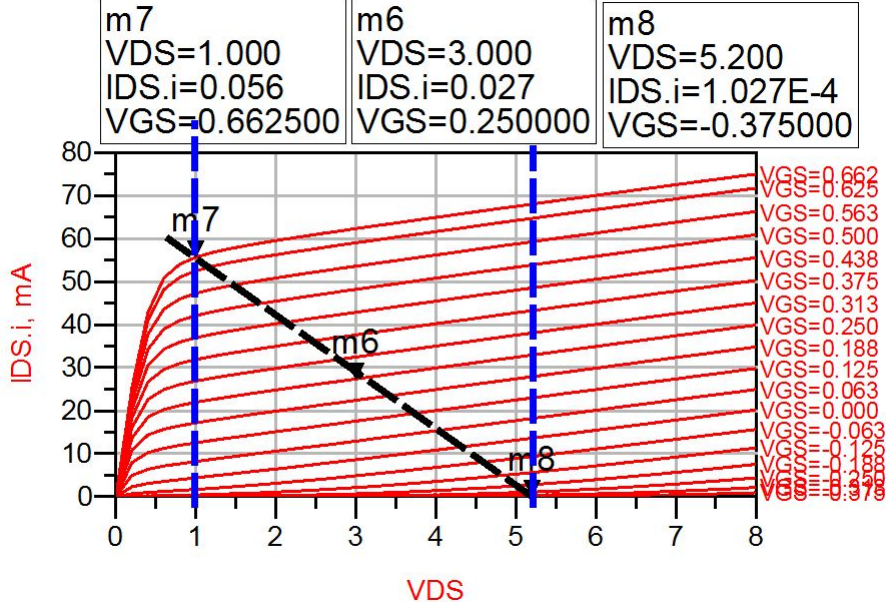$$fco = \frac{1}{\pi \cdot Zo \cdot Cgs} \qquad (3)$$

6

Figure 4: Class-A bias and load-line

Given a device size and bias it is possible to estimate the number of devices required to meet the gain design goal. First an estimate of the device transconductance, gm, is necessary. The gm was extracted from the device dc IV simulation. It should be noted however that this is not the most accurate means of extracting gm, and other methods are described in [5]. It did however prove to be accurate enough for these small devices, and the gm vs. Vgs is shown in figure 5, as well as the 6th order polynomial fit. From the curve fit, the first order transconductance coefficient gm1 is found, along with higher-order gm coefficients. In order to satisfy the gain goal of table 1, equation 4 is used to estimate the number of stages, where n=# of devices and gm is the first order transconductance. It should be noted that equation 4 assumes both the gate and drain lines are of the same impedance. A more general formula for gain is found in [2]. The TQP13 data-sheet specifies a maximum transconductance of 0.75 S/mm, and utilizing this as well as the extracted transconductance yielded two gain estimates, roughly 3dB apart, for n=4. Resulting gain estimates are shown in table 2. While the both the extracted and process specified gm may yield optimistic gain estimates, there is 1.5dB of design margin at choosing n=4 and considering that the device size gives nearly 5Ghz of margin on the cutoff frequency, where gain will likely roll off as frequency increases, it is assumed that this is a good starting point for simulation.

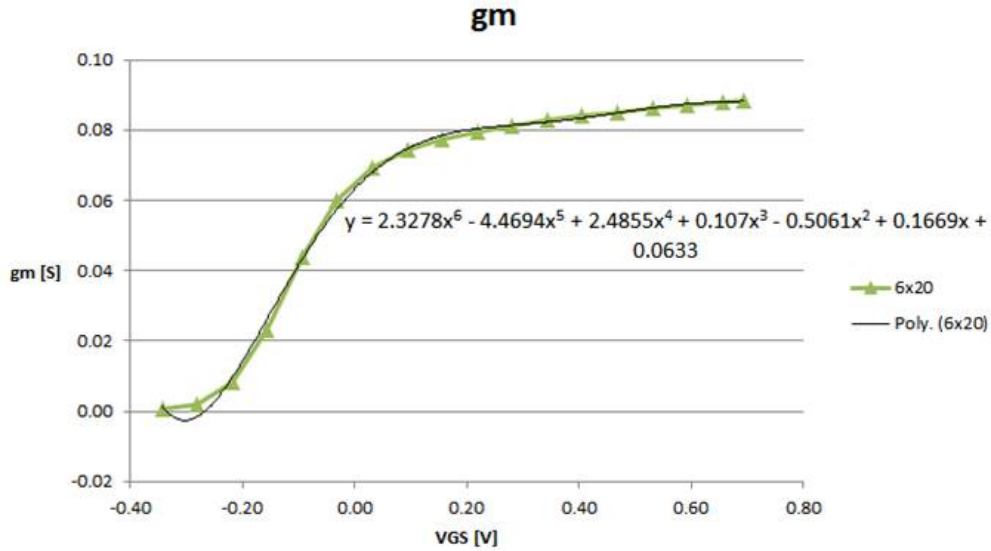$$G_{dB} = 10 * \log_{10}\left(\frac{Z_O \cdot n \cdot gm}{2}\right) \qquad (4)$$

7

Figure 5: Transconductance, gm, and polynomial curve fit.

Parameter	Units	Extracted	Process
n	[]	4	4
Zo	[Ω]	50	50
gm	[S]	0.1669	0.09
G	[dB]	12.2	9.5

Table 2: Gain estimates for n=4 of 120um devices for both the extracted 1st order transconductance and the process data-sheet specified transconductance.

4 Simulations

4.1 Ideal Simulation

Utilizing a 120um device, Cgs and Cds were extracted from a linear simulation, as shown in figure 6. Note that Cgs is relatively flat versus frequency which is beneficial given that this is the dominant parameter in terms of frequency cutoff. Inductance values are calculated for a t-line of characteristic impedance of $Z_O = 50\Omega$, by considering the t-network topology of figure 2, and $L_g = Z_O^2 \cdot C_{gs}$ for Cgs of approximately 0.25pF. The resulting gate and drain inductances required for the gate and drain transmission line synthesis are shown in table 3. Note that for some designs the time delay per t-line segment, $\tau = 1/\sqrt{LC}$, may prove critical, in particular matching the sub-segment delays on the input and output transmission lines. However, for this design, strict adherence was not found to be super critical.

8
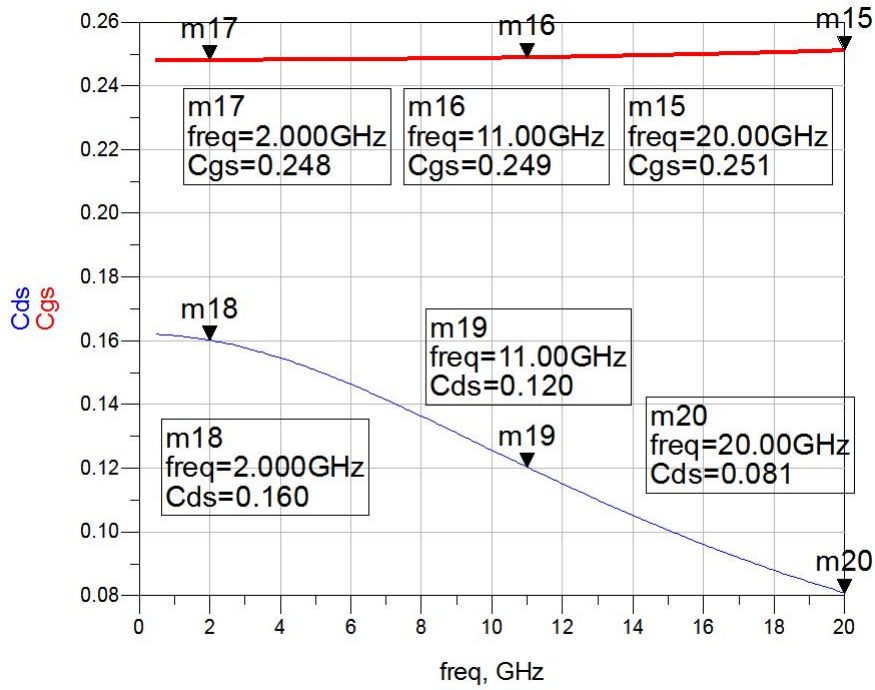
Figure 6: Cgs and Cds vs. frequency of 120um device

freq [GHz]	L_g[nH]	L_d[nH]
2	0.620	0.4
11	0.623	0.3
20	0.628	0.2

Table 3: Gate and drain transmission line inductance lumped element values

With the device input and output T-networks defined, the ideal schematic of figure 7 was simulated to verify gain, match, and bandwidth, shown in figure 8. Gain and bandwidth showed good starting performance, while return losses showed some improvement would be necessary.
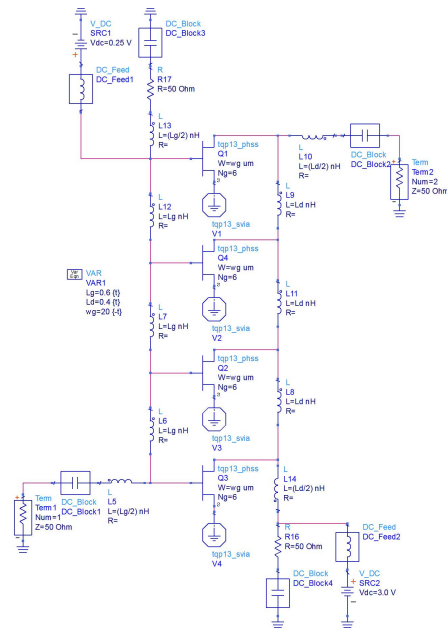
Figure 7: Ideal Distributed Amplifier Schematic

(a) Gain

(b) Return Loss
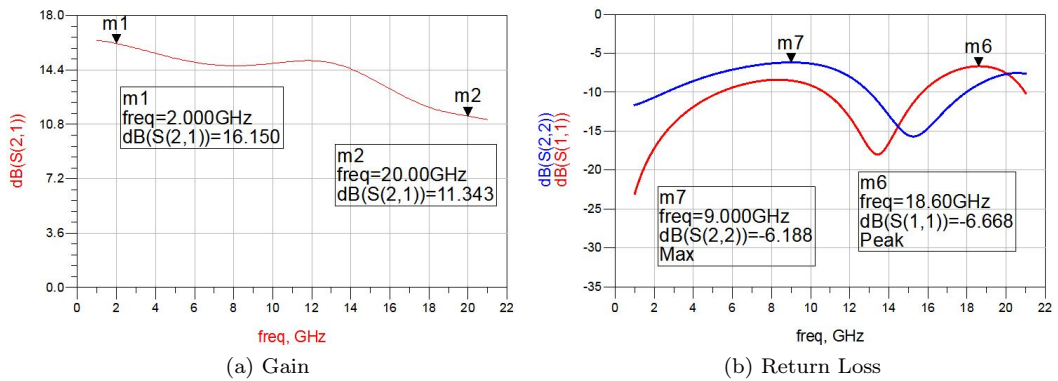
Figure 8: Ideal Distributed Amplifier Simulation Results

4.2   Detailed Simulation

4.2.1   Linear

The final distributed amplifier utilized transmission line elements to realize the necessary inductances. The final schematic is shown in section 5, figure 13. To overcome some dc resistance in the drain t-line, the final drain voltage is Vdrain=3.3V, and due to low current draw the gate supply remained at Vgs=0.25V. Final linear performance to 20GHz is shown in figure 9 and to 50GHz in figure 10.

(a) Gain

(b) Return Loss

(c) Reverse Isolation

(d) Stability, Mu
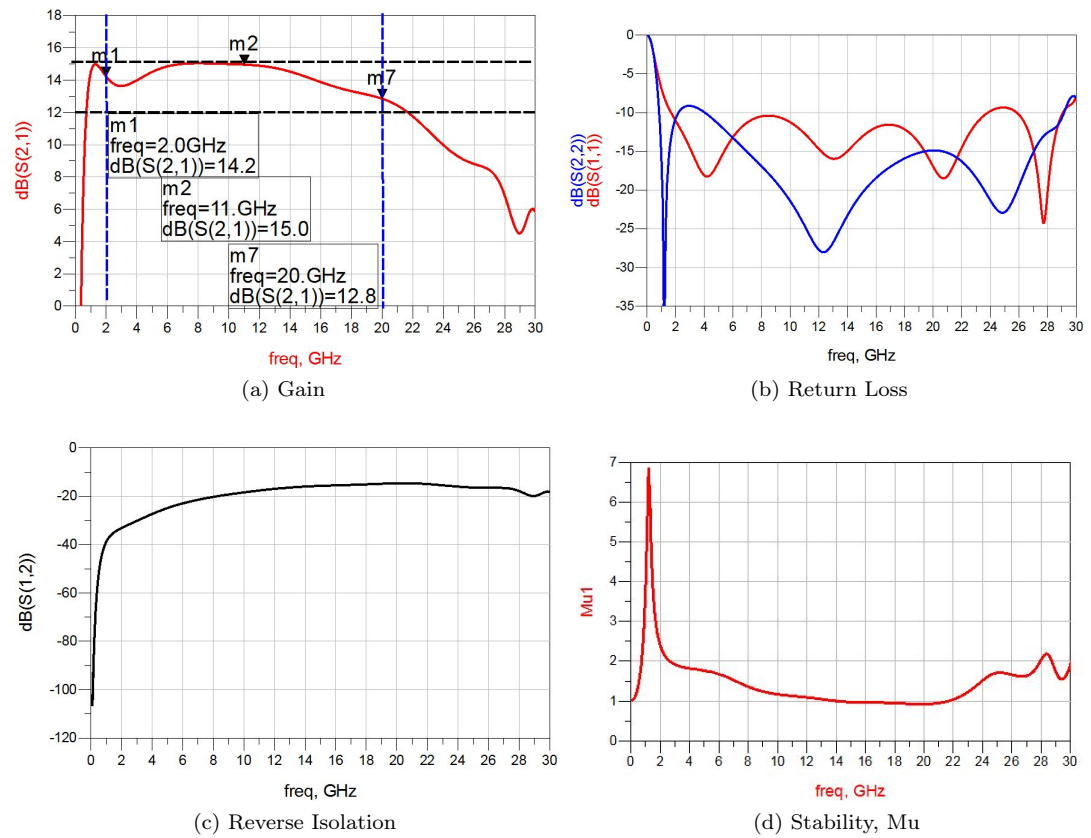
Figure 9: Distributed Amplifier Performance, to 20GHz

11

(a) Gain

(b) Return Loss

(c) Reverse Isolation

(d) Stability, Mu
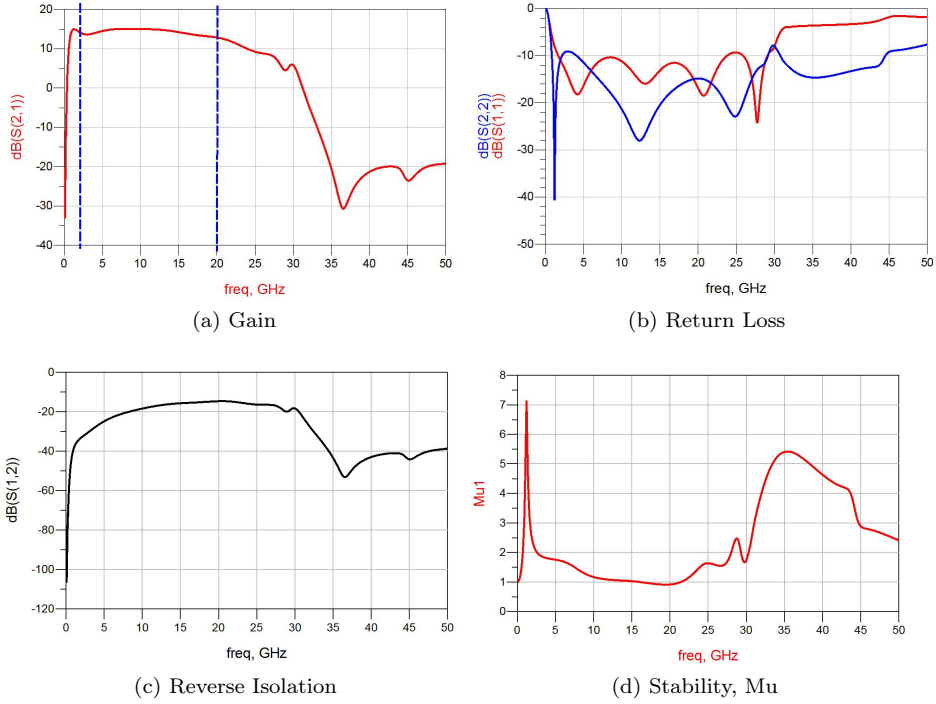
Figure 10: Distributed Amplifier Performance, wide-band

4.2.2 Nonlinear

The final design was characterized in simulation for compression and linearity. Compression characteristics and third-order intercept (TOI) at 2, 11, an 20 GHz are shown in figures 11 and 12, respectively.
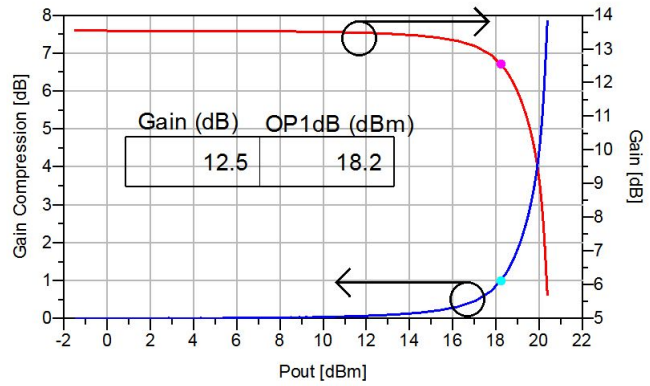
(a) 2 GHz
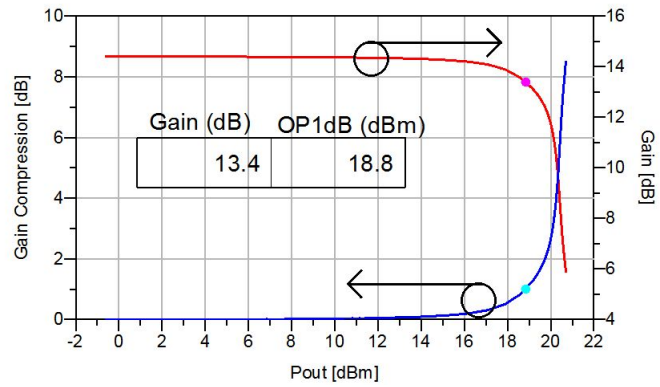
(b) 11 GHz
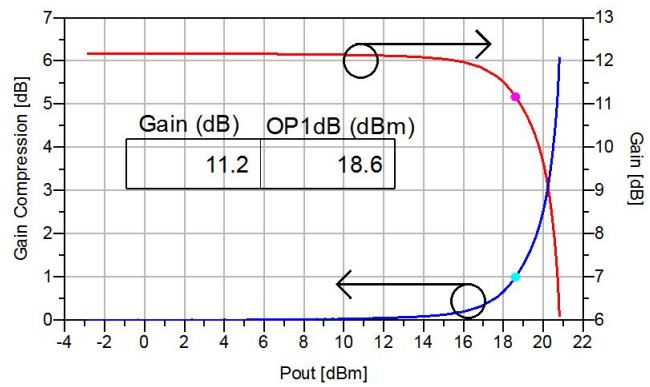
(c) 20 GHz

Figure 11: Gain compression and OP1dB

13
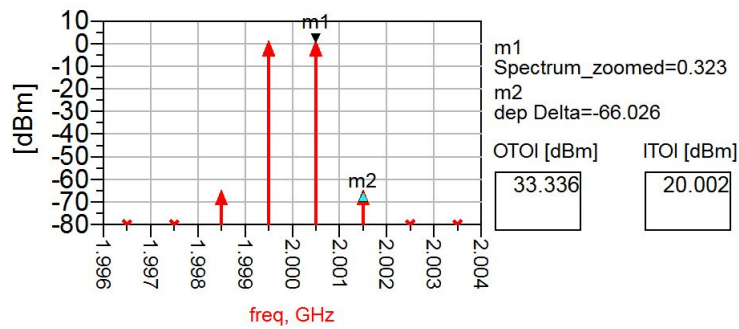
(a) 2 GHz
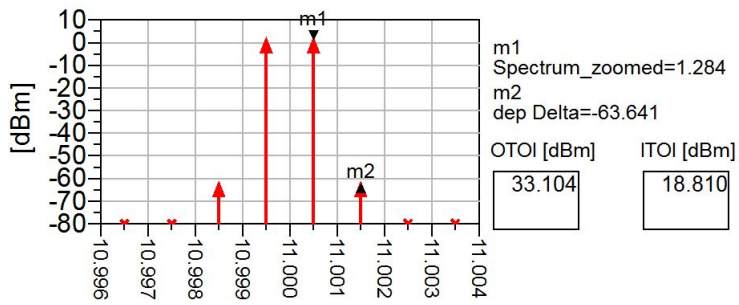
(b) 11 GHz
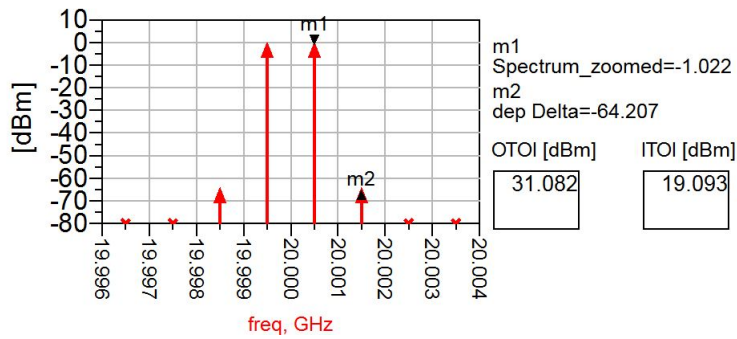
(c) 20 GHz

Figure 12: Third-Order Intercept

14
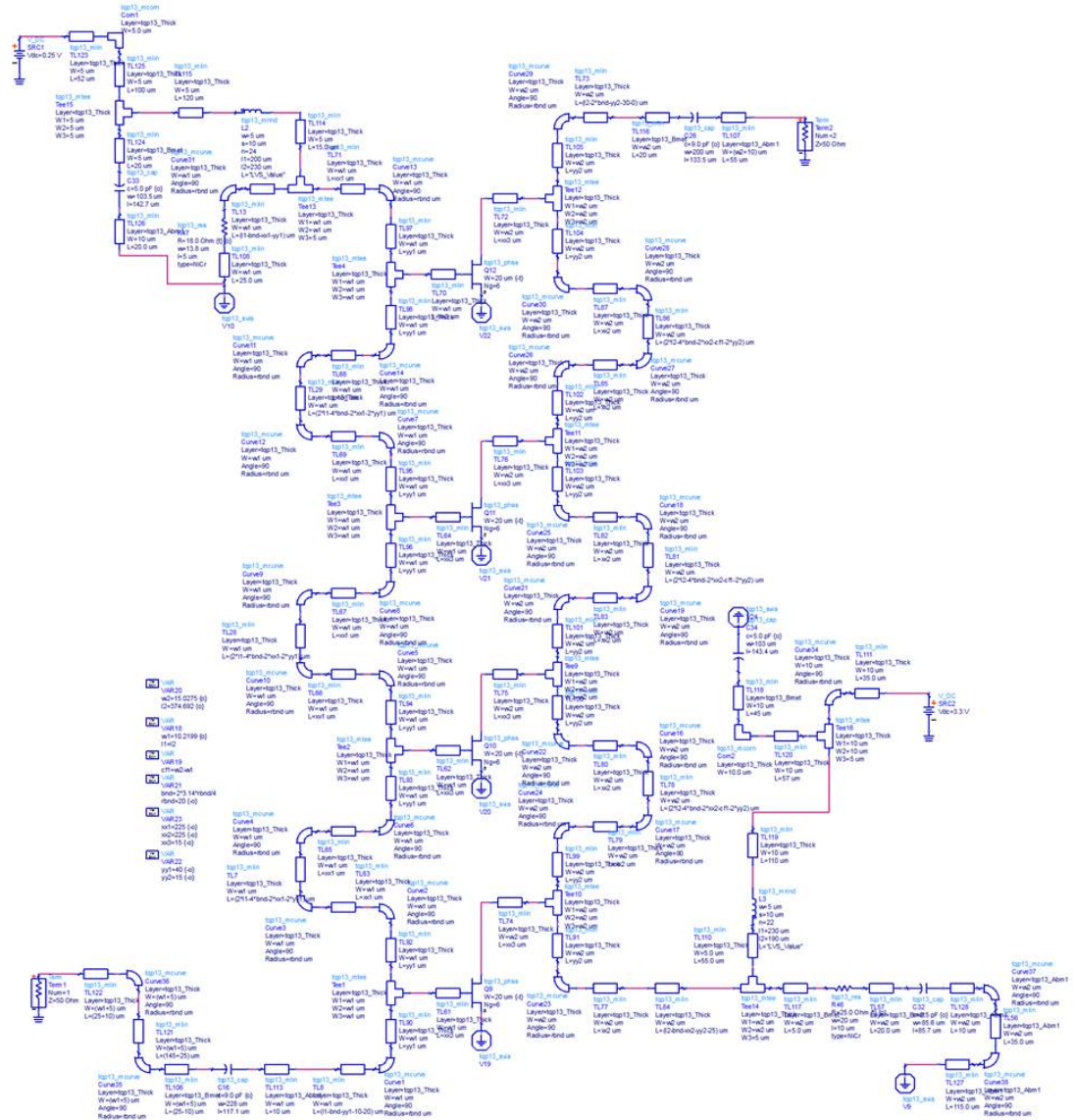
5   Schematic

Figure 13: Final 2-20GHz Distributed Amplifier MMIC Schematic

6 Layout
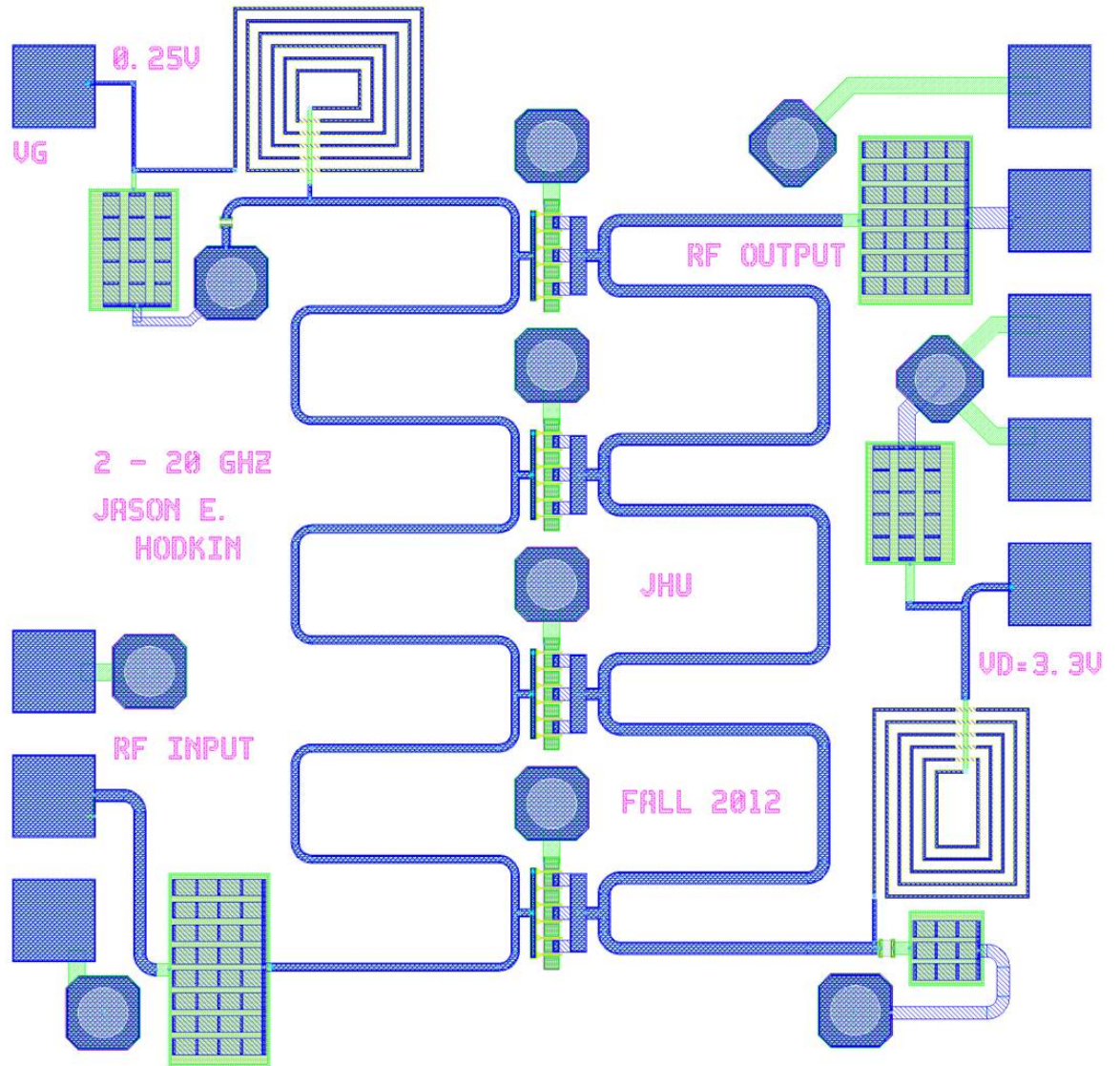
Figure 14: Final 2-20GHz Distributed Amplifier MMIC Layout (ADS Layout)

7 Test Plan

7.1 Linear

Linear s-parameters will be extracted via vector network analyzer (VNA) measurement with calibrated G-S-G probes to 26GHz.

1. Calibrate VNA using probe calibration substrate, 1 to 26 GHz, 1601 points. Port 1 power level should be around -20 dBm.

2. Apply -0.5V to Vgate with needle probe for pinch-off.

3. Apply 3.3V to Vdrain, supply current should be $\ll$ 1mA.

4. Slowly increase Vgate to +0.25V, or until drain supply current reaches around 113mA.

5. Acquire 2-port data.

7.2 Nonlinear

Two tests should obtain verification of TOI and compression characteristics.

TOI: two signal generators, 2-way combiner, and a spectrum analyzer are required. For fc= 2, 11, and 20 GHz, fspace=1MHz:

1. Set one signal generator to f1=fc-fspace/2 and the other to f2=fc+fspace/2, set each to around -10 dBm, turn RF off, and connect to combiner inputs.

2. Connect combiner output to device RF input probe, connect RF output probe to spectrum analyzer.

3. Apply dc as described in linear measurement section above.

4. Turn generator RF on.

5. Use makers on SA to extract all f1, f2, 2f1-f2, and 2f2-f1 tone levels in dBm.

6. For each high and low-side fundamental and intermod, find IMD3=dBm(2f-f)-dBm(f), result in dBc.

7. OTOI=Ptones-IMD3/2, where Ptones=output fundamental power in dBm.

Compression: one signal generator and one calibrated RF power meter are required. For fc= 2, 11, and 20 GHz:

1. Connect disabled signal generator to device RF input.

2. Connect device output to power meter

3. Apply dc as described in linear measurement section above.

4. Set each sig gen and power meter to fc.

5. Step sig gen power level from -30 to 10 dBm and acquire in/out levels at 0.5 or 1dB steps.

6. Plot Pout versus Pin, also calculate Gain=Pout-Pin and plot versus Pout to show gain compression.

8 Summary & Conclusions

Final performance relative to goals is summarized in table 4. A moderate gain, general purpose, wide-band amplifier in a compact layout has been designed, simulated, and readied for foundry fabrication. Upon delivery from fab, testing will ensue according to the test plan, and results compared to simulation.

Parameter	Units	Goals	Full Band	2GHz	11GHz	20GHz	
Gain	[dB]	> 8	>12.8	14.2	14.9	12.8	small signal
Gain Flatness	[dB]	± 1.5	2	-	-	-	
Return Loss, in or out	[dB]	> 8	>9.3	-	-	-	
OTOI	[dBm]	> 30	≥ 31	33.3	33.1	31.0	
OP1dB	[dBm]	> 17	> 18	18.2	18.8	18.6	
*Pdc	[W]	-		0.376			
ηdc	[%]	-		17.5			@P1dB
PAE	[%]	-		16.7			$=\eta$dc(1-1/G)
Chip Size	[mm^2]	1.5x1.5	1.3x1.3	-	-	-	
*Vd=3.3V @ 113mA, Vg=0.25 @ 11.6mA							

Table 4: Performance Summary

References

[1] W. S. Percival, "Thermionic valve circuits," *British Patent Specification No. 460562*, 1937.

[2] E. Ginzton, W. Hewlett, J. Jasberg, and J. Noe, "Distributed amplification," *Proceedings of the IRE*, vol. 36, pp. 956 – 969, aug. 1948.

[3] I. D. Robertson, *MMIC DESIGN*. London: IEE, 1995.

[4] C. Campbell, A. Balistreri, M. Kao, D. Dumka, and J. Hitt, "Gan takes the lead," *Microwave Magazine, IEEE*, vol. 13, pp. 44 –53, sept.-oct. 2012.

[5] S. A. Mass, *Nonlinear Microwave and RF Circuits*. Norwood, MA: Artech House, 2nd ed., 2003.

12/13/2012

2-20 GHz Distributed PA

Design, Simulation, and Test Plan

Shannon Marshall

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2-20 GHz Distributed PA

Design, Simulation, and Test Plan

Abstract

This paper describes the design of a five-stage distributed power amplifier intended for operation between 2 GHz and 20 GHz. The amplifier design presented is based on the architecture depicted in Figure 1 (Mikemoral, 2012), and achieved greater than +23 dBm output power across the operating frequency band with reasonable input and output return loss.
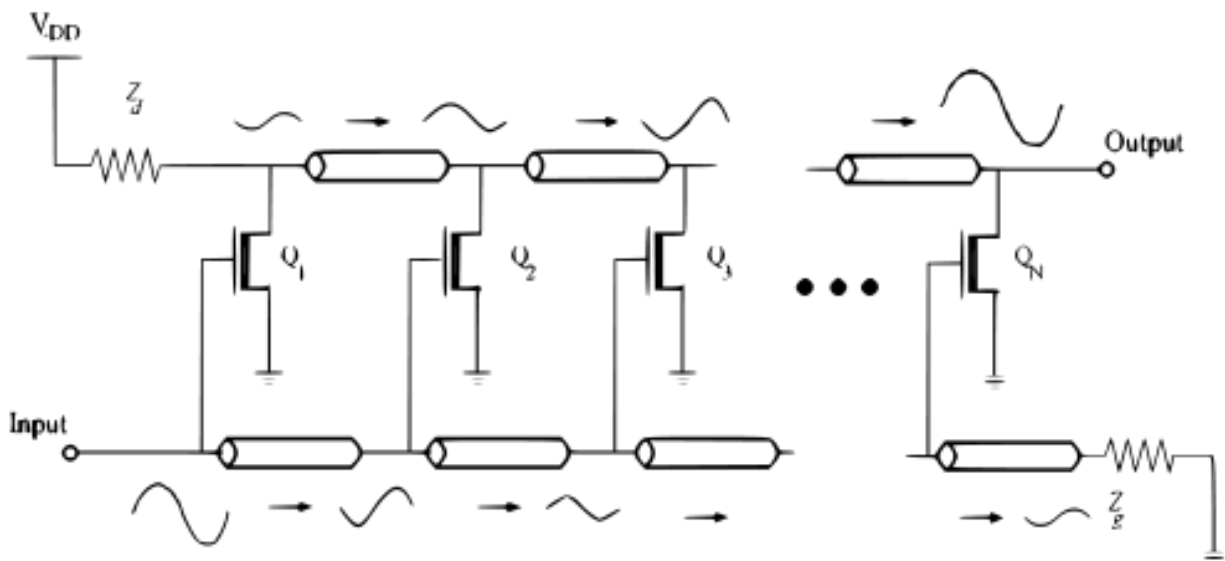
Figure 1 - Distributed Amplifier Architecture[i]

Introduction

 The design presented in this paper attempts to achieve modest RF power output from a distributed amplifier architecture. Performance targets were set by the specifications of the TriQuint TGA8334-SCC power amplifier, which it is intended to replace. The design went through several iterations, which are briefly outlined in the "Design Approach" section of the paper. Linear and nonlinear simulations of the final MMIC showed promising results; a test plan to verify RF performance is outlined in the "Test Plan" section.

Design Approach

The design goals for this amplifier are taken from the TriQuint TGA8334-SCC datasheet (TriQuint Semiconductor, 2003), and are as follows:

- 2 GHz – 20 GHz operating bandwidth
- 0.4 W output power at midband (i.e., +26 dBm)
- On-chip DC blocking capacitors
- 8dB gain +/- 1dB
- -10.8 dB input return loss and -17.7 dB output return loss at midband (1.8:1 input and 1.3:1 output SWR)
- <440 mA drain current draw

To maximize achievable power output, 9V drain bias was selected. +0.35V gate bias yielded a load line with acceptable dynamic range.

The bandwidth of a distributed amplifier is governed by the parasitic capacitance of its transistors, which places an upper limit on the bandwidth of the synthetic transmission line sections.

$$F_{cutoff} = \frac{1}{\pi * Z_0 * C_{gs}} \qquad\qquad F_{cutoff} = \frac{1}{\pi * Z_0 * C_{ds}}$$

Several transistor configurations were simulated to approximate parasitic capacitances; the results appear in Table 1 - parasitic capacitances and cutoff frequencies. The row labeled CASCODE denotes values derived from a cascode arrangement of two n=2, W=50μm PHEMTs.

Vd	Vg	n	W	Cgs	Rgs	Rd	Rds	Cds	G20ghz	Fc
2.8	0.6	2	50	0.18	14	30	360	0.17	11.3	3.54E+10
9	0.35	2	50	0.17	19.8	20	385	0.2	10.91	3.18E+10
9	0.35	4	25	0.17	18	20	385	0.195	8.46	3.26E+10
9	0.35	4	50	0.51	11	11	197.5	0.67	9	9.50E+09
9	0.35	6	50	0.975	7.7	7.8	130	1.4	6.8	4.55E+09
9	0.35	2	100	0.51	15	11	197.5	0.7	8.52	9.09E+09
9	0.35	4	100	1.524	7.9	6	98	2.5	4.65	2.55E+09
CASCODE				0.127	10.1	3	3000	0.047	9.41	5.01E+10

Table 1 - Parasitic Capacitances and Cutoff Frequencies

Of the simulated transistors, the n=2, W=50μm PHEMTs at +0.35V gate bias and +9V drain bias yielded the best combination of cutoff frequency and gain at 20 GHz.

Multiple topologies were evaluated to attempt to balance gain, stability, and output power. Preliminary simulations with ideal circuit elements were performed on the following circuits:

- 3-transistor distributed amplifier (P_{out} too low)
- 4-transistor distributed amplifier (P_{out} too low, difficult to stabilize)
- 5-transistor distributed amplifier (P_{out} too low, difficult to stabilize)
- 5-transistor distributed amplifier with capacitor-coupled gate (Robertson, 5.10.4: High Power Distributed Amplifiers, 2001) (P_{out} too low)
- 3-transistor-pair cascode distributed amplifier (Robertson, 5.8: Distributed amplifier, 2001) (P_{out} too low)
- 4-transistor-pair cascode distributed amplifier (P_{out} too low, difficult to stabilize)
- 5-transistor distributed amplifier with capacitor-coupled gate and n=4 W=50 μm output transistors (Robertson, 5.10.4: High Power Distributed Amplifiers, 2001)

The capacitor-coupled gate amplifier design afforded two advantages over the other topologies: the output power was higher than the other amplifiers, and the gate capacitors afforded a way to trade off circuit bandwidth and gain against overall stability. The 5-transistor capacitor-coupled gate amplifier with n=4, W= 50 μm output transistors shown in Figure 9 - Simplified Amplifier RF Schematic was therefore selected.

Nominal inductor values for this circuit were L_D=0.5 nH and L_G=0.425 nH. After tuning the inductor values to give the best overall performance, linear simulation was used to select TQP13 MLIN lengths of desired shape and equivalent inductance. The inductance wasn't varied for the output stages; this detuning maintained the amplifier bandwidth at the cost of return loss.

Simulations

Linear simulations using TriQuint device models indicate acceptable forward and reverse transmission over the designed operating band; results are shown in Figure 2 - Amplifier Gain and Figure 3 - Amplifier Isolation.
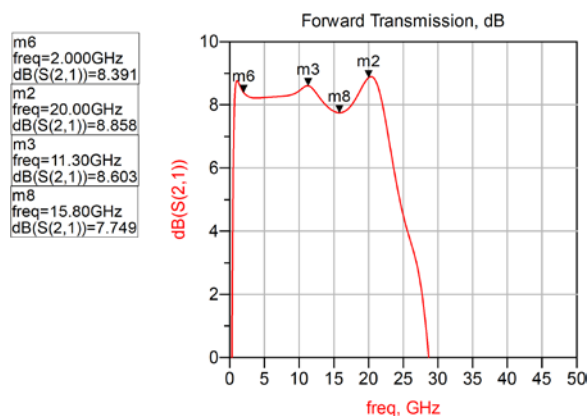
Figure 2 - **Amplifier Gain**
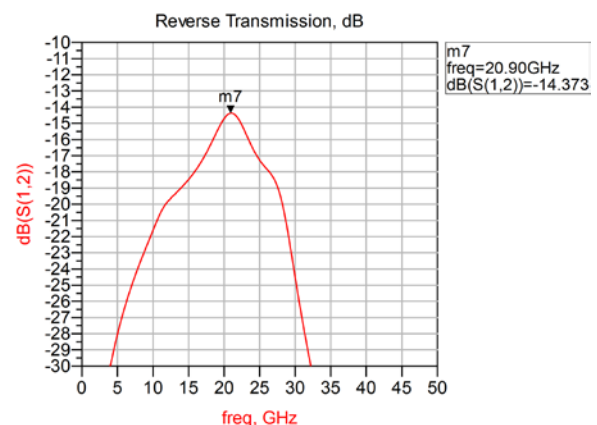
Figure 3 - **Amplifier Isolation**

Input return loss, shown in Figure 4 - Amplifier Input Return Loss, is better than -6 dB over the operating frequency band; output return loss, shown in Figure 5 - Amplifier Output Return Loss, is better than -4 dB over the operating band.
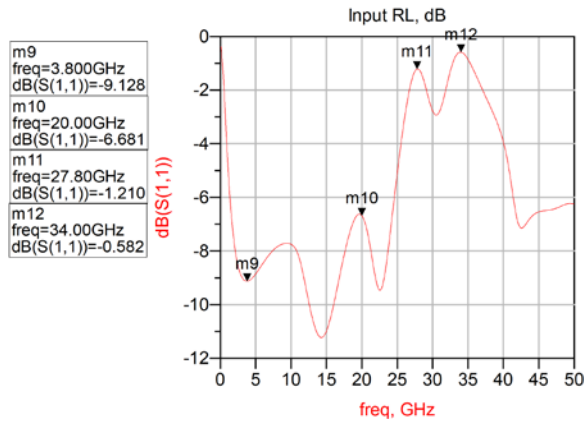
Figure 4 - Amplifier Input Return Loss
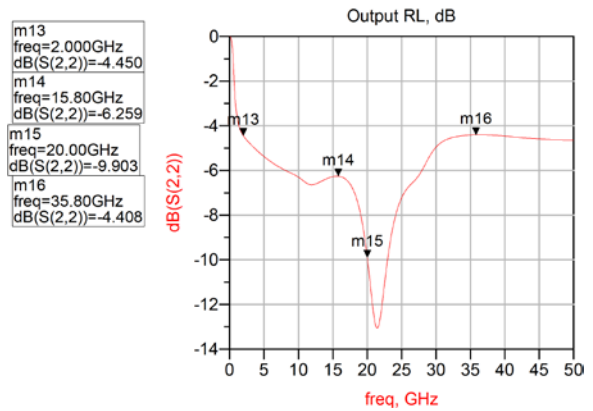
Figure 5 - Amplifier Output Return Loss

The amplifier's stability parameter, μ, is >1 over the simulated frequency range of 0.5 GHz – 50 GHz; the amplifier should be unconditionally stable between those frequencies.
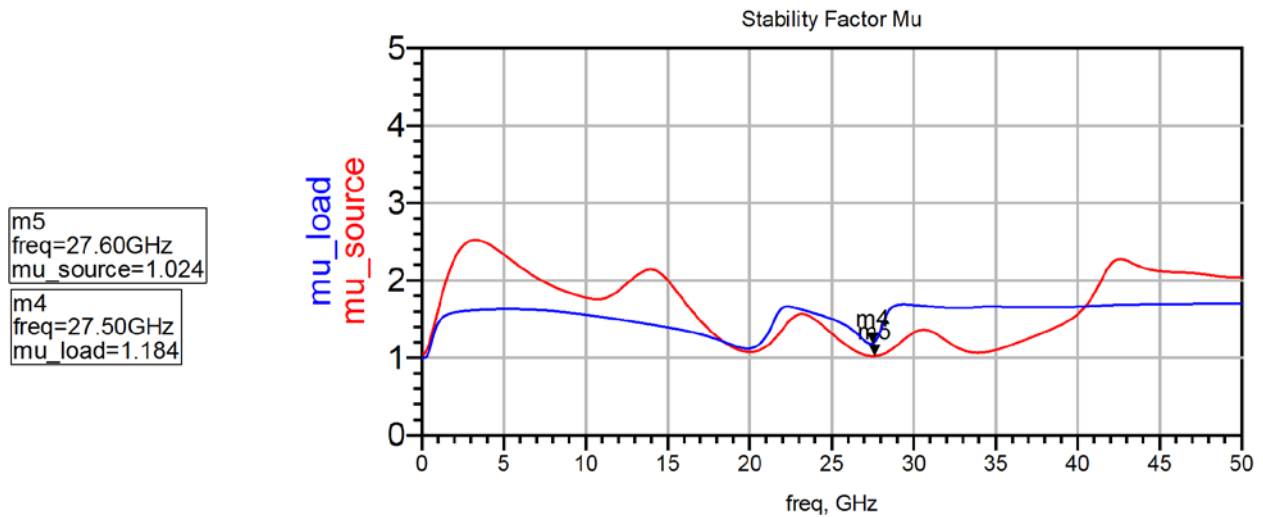
Figure 6 - Amplifier Stability Factor

Linear DC simulation predicts a drain current draw of 292 mA and a gate current draw of 57 nA in linear operation.

P1dB is greater than +23 dBm over the frequency band, and greater than +26 dBm from 500 MHz – 7 GHz, according to harmonic balance nonlinear simulation. Drain current in compression should be around 240 mA over most of the frequency band, exceeding 250 mA above 18 GHz.
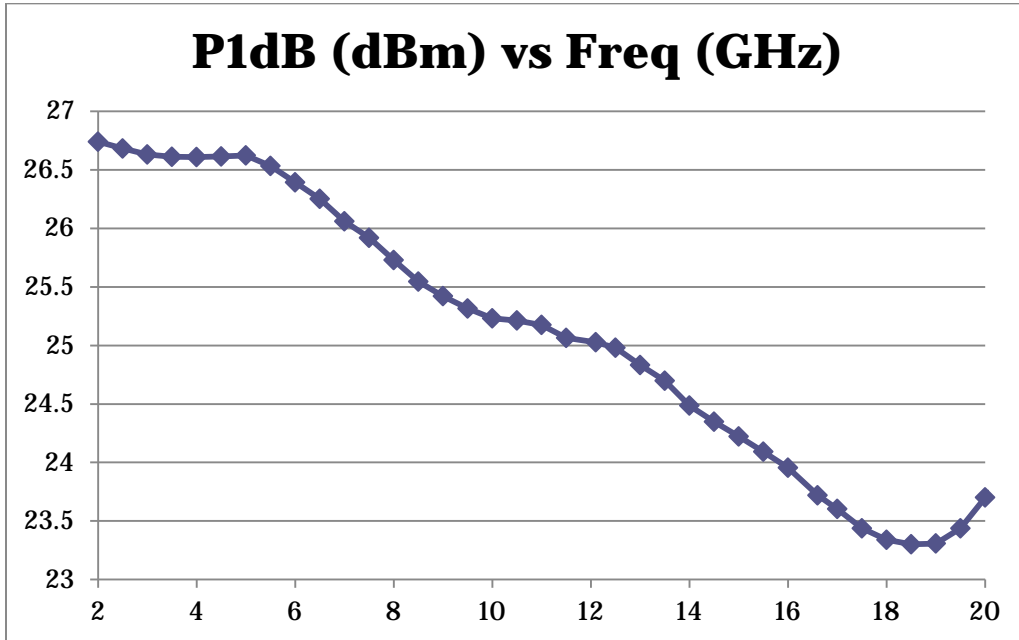
Figure 7 - Amplifier Output Power at 1 dB Compression
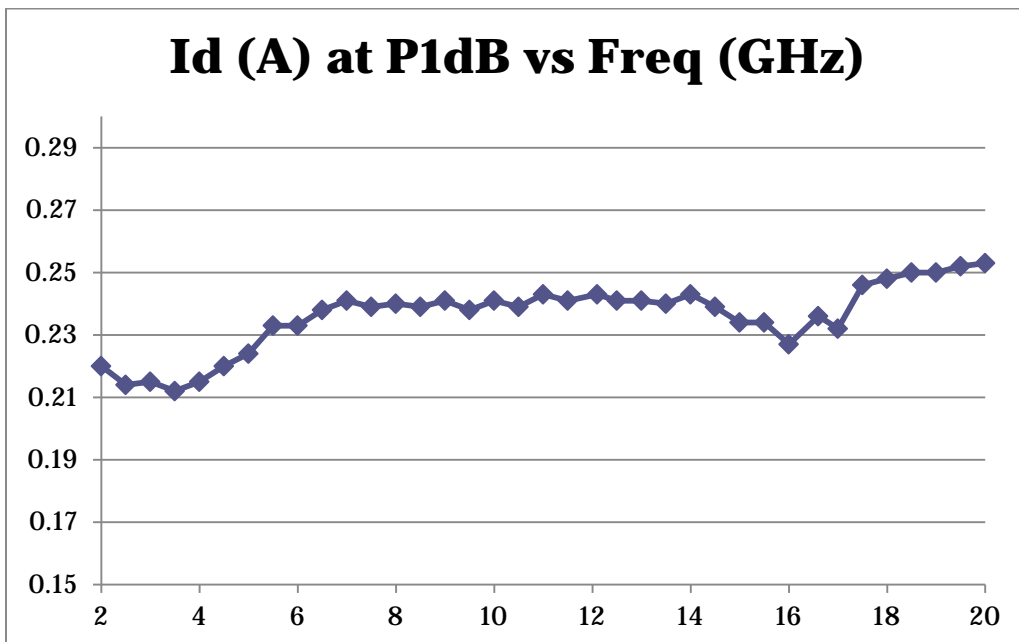
Figure 8 - Amplifier Drain Current at 1 dB Compression

Schematic

A simplified RF schematic of the final distributed amplifier design is presented in Figure 9 - Simplified Amplifier RF Schematic. Drain and gate inductors were realized on-chip with TQP13 MLIN elements. The first two stages have two coupling capacitors because the capacitance required for stability was too low to be realized with a single standard capacitor element. The fourth and fifth transistors (next-rightmost and rightmost on the below schematic) have four 50-μm gate elements; the first, second, and third have two 50-μm gate elements.
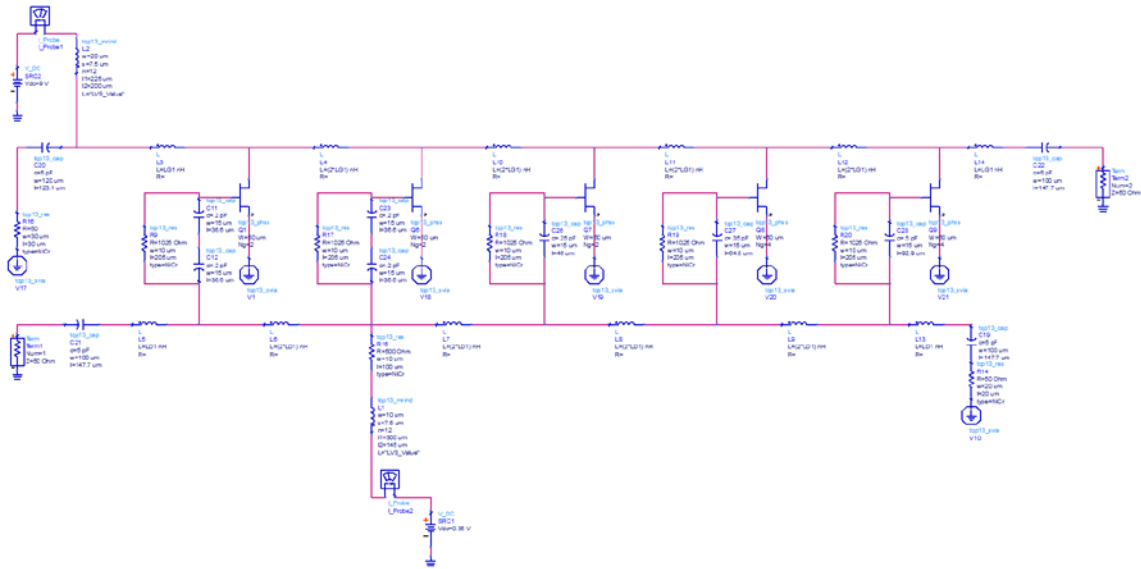
Figure 9 - **Simplified Amplifier RF Schematic**
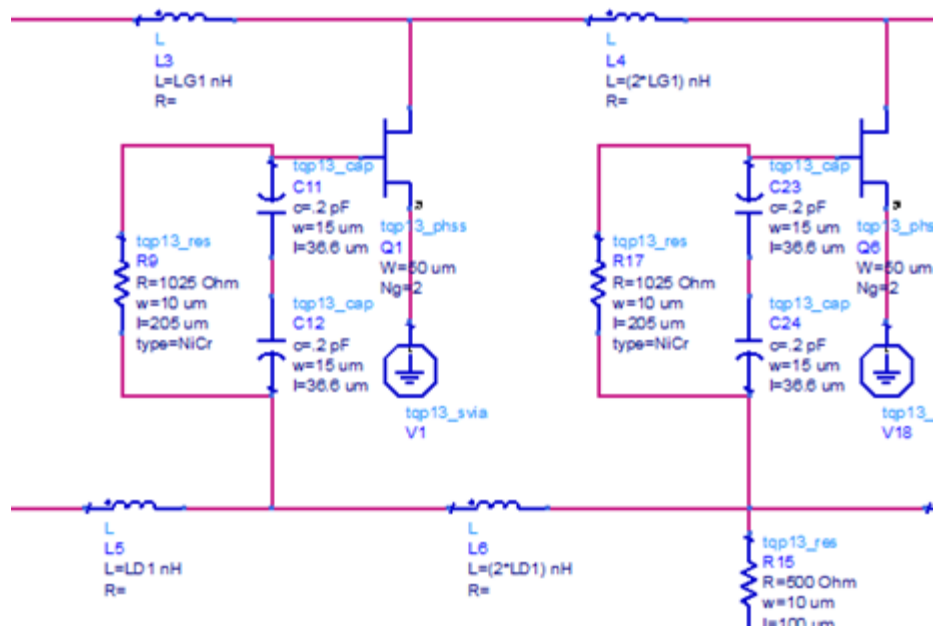
Figure 10 - Amplifier RF Schematic Detail

The DC circuit is shown in Figure 11 - Amplifier DC Schematic. The circuit runs at a 9V drain bias and a +0.35V gate bias.
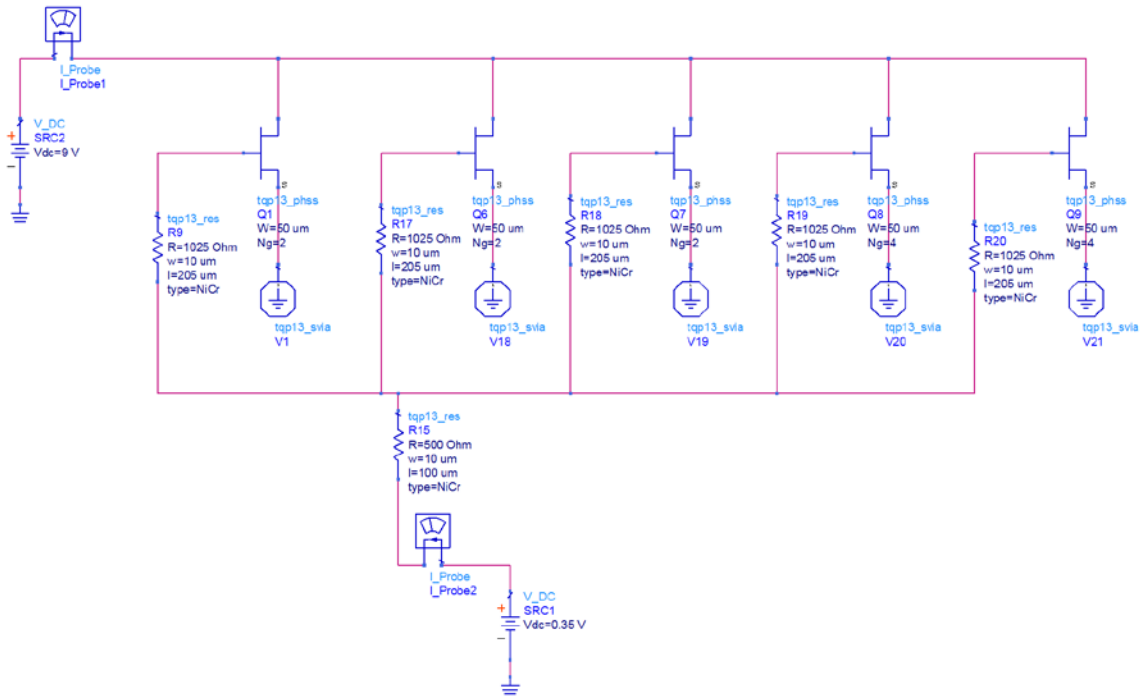
Figure 11 - **Amplifier DC Schematic**

Layout

The final layout of the MMIC appears in Figure 12 - Amplifier Layout. The 50Ω drain termination resistor is on the chip (whereas the TGA8334-SCC required an off-chip termination resistor). Gate and Drain decoupling capacitors and inductors are likewise on the MMIC.
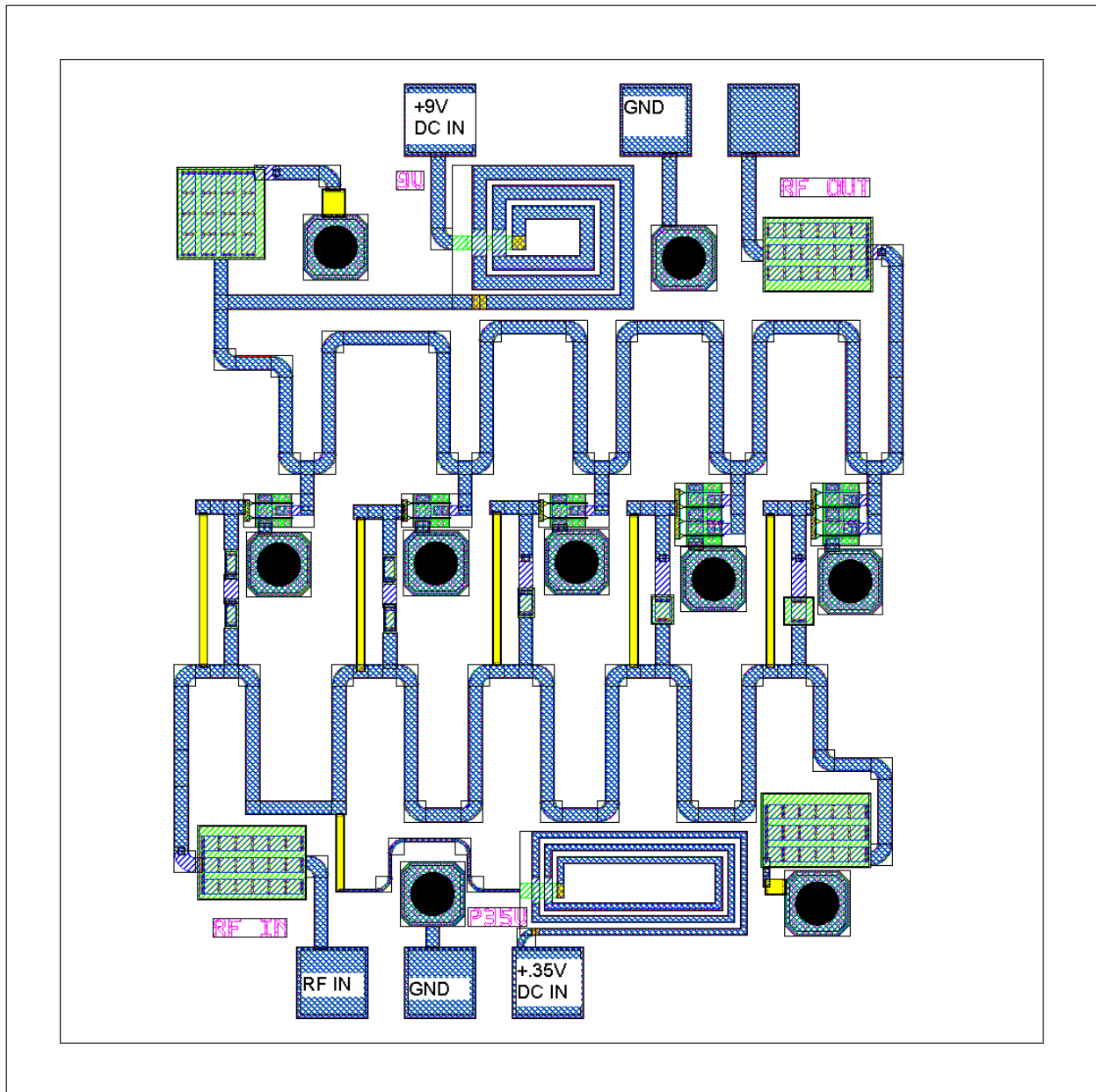
Figure 12 - **Amplifier Layout**

Test Plan

DC & S Parameters

S parameter measurement will be performed using a VNA and a pair of RF signal probes calibrated over the operating band of 2 GHz – 20 GHz.

1. Calibrate VNA from at least 2 GHz – 20 GHz, with at least 181 points (to measure every 100 MHz).
2. Apply -0.5V to the gate DC input through a needle probe to hold the amplifier in pinch-off.
3. Apply +9V to the drain through a second needle probe, ramping up from 0V. Watch for excessive current draw.
4. Slowly increase gate DC input to +0.35V. Amplifier should be drawing < 300 mA. Record gate and drain currents.
5. Measure s parameters.

Power and Current at 1 dB Compression

Compressed power will be measured at frequencies of interest: 2 GHz, 11 GHz, 18.5 GHz, and 20 GHz. This measurement requires a signal generator, an attenuator (since the maximum output power is higher than the "Do Not Exceed" power on most power heads), and a power meter.

1. Connect signal generator to RF IN port; make sure RF output of signal generator is OFF.
2. Connect device output to power meter through a suitable attenuator. 10 dB probably allows a good safety margin.
3. Apply DC per steps 2-4 of the DC & S Parameters section of the test plan.
4. Set signal generator and power meter to the frequency of interest.
5. Take a linear measurement at -20 dBm input power, and increase in large (3 - 6 dB) steps until Pout is around +10 dBm. Increase in smaller steps (1 dB or 0.5 dB) until gain is 1 dB compressed relative to linear gain measurement.
6. Record all Pin and Pout measurements, along with gate and drain current at linear measurement point and at compressed measurement point.

Summary and Conclusions

Amplifier performance is compared to design goals in Table 2 - Amplifier Performance vs. Goals. The design falls short of its performance parameters, but still produces respectable output power and flat gain over the entire operating band. Once the amplifier is fabricated, performance can be compared to simulated results and evaluated against specifications.

Metric	Units	Goal	Performance	Notes
Small Signal Gain	dB	> 8	7.8	Worst case performance at 15.8 GHz
Gain Flatness	dB	+/- 1	+/- 0.6	
Input Return Loss at midband	dB	>10.8	9	6.7 dB worst case at 20 GHz
Output Return Loss at midband	dB	>17.8	6.5	4.5 dB worst case at 2 GHz
Output P1dB at midband	dBm	> 26	25.2	26.75 at 2 GHz; 23.3 at 18.5 GHz
DC Power	W		2.28	253 mA @ 9V + 0.292 mA @ 0.35V
Drain Current	A		0.253	At 1 dB compression, worst case at 20 GHz
Efficiency	%		10.3	At 20 GHz. Range from 9.5% to 24.2%

Table 2 - **Amplifier Performance vs. Goals**

References

Mikemoral. (2012, December 10). *Distributed amplifier.* Retrieved December 2012, 2012, from Wikipedia: http://upload.wikimedia.org/wikipedia/commons/thumb/a/ab/N-stage_traveling-wave_amplifier.svg/500px-N-stage_traveling-wave_amplifier.svg.png

Robertson, I. D. (2001). 5.10.4: High Power Distributed Amplifiers. In I. D. Robertson (Ed.), *RFIC and MMIC design and technology* (p. 234). London, United Kingdom: Institute of Electronics Engineers.

Robertson, I. D. (2001). 5.8: Distributed amplifier. In I. D. Robertson (Ed.), *RFIC and MMIC design and technology* (pp. 213-225). London, United Kingdom: The Institution of Electrical Engineers.

TriQuint Semiconductor. (2003, April 25). TGA8334-SCC Datasheet. Richardson, Texas, United States of America.

[i] Figure by Wikipedia user Mikemoral, and used under terms of Creative Commons Attribution 3.0 Unported license.

2-20 GHz LNA

EN.525.787 – MMIC Design

Brian Billman

12/13/2012

Abstract

This paper describes a 2-20 GHz LNA designed on the Triquint GaAs TQP13 process. The goal was to achieve greater than 10dB gain and less than 3dB noise figure across the entire band. The design meets these goals in simulation.

Design Approach

In order to meet the wideband requirements a distributed amplifier topology was implemented for this design. Distributed amplifiers are able to obtain large gain-bandwidth products relative to other topologies. For this design I implemented the distributed topology by connecting the gates and drains of multiple stages of transistors using transmission lines. The inductance of the transmission line is to tune out the capacitance of the transistors. You could also use inductor coils between transistors.

Specifications:
Frequency: 2-20GHz
Gain: 10dB
Noise Figure: 3dB
Stability: Unconditional

My first step was to determine the necessary transistor size and the required number of stages to meet the gain and noise figure requirements. My initial design had 4 stages with 2x20 transistors. The noise figure was well below the spec but I was unable to meet the gain requirement. The performance of my initial design is shown in Figure 1 and Figure 2.
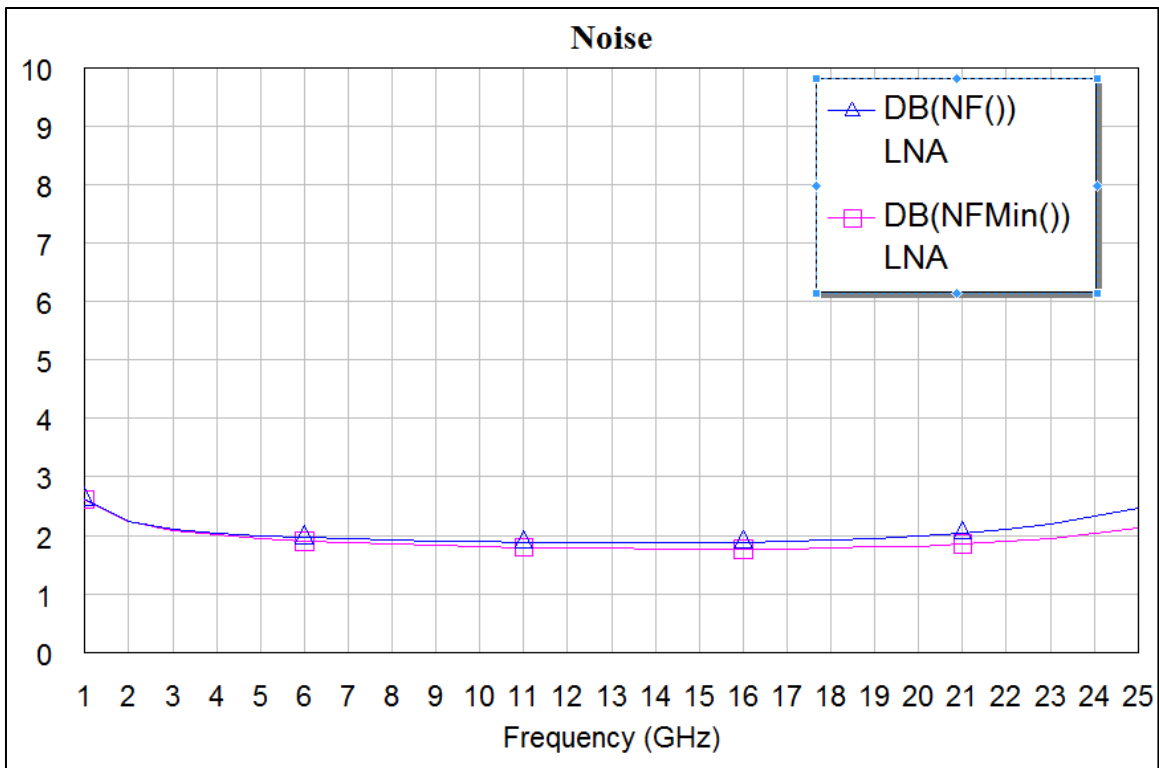
Figure 1. The noise figure of the initial design is well below requirements
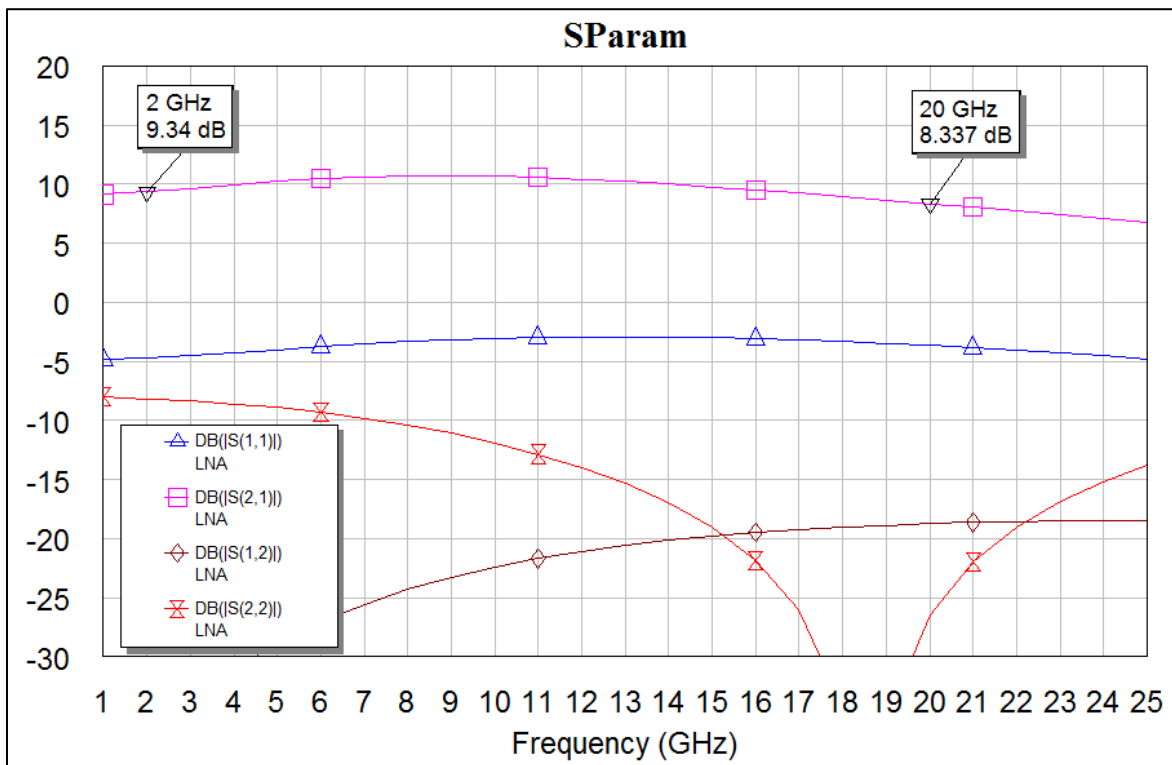
Figure 2. The gain of initial design does not meet the requirements

In order to meet the gain requirement I increased the transistor sizes to 4x40. This increased the noise figure slightly however it still met the spec. With the transistor and stages determined, I moved on to tuning the gate and drain lines. It was a challenge to keep the design unconditionally stable while meeting all the requirements. To resolve this I treated the gate and drain resistors as stabilizing components and tuned their values from the original 50 ohms. I ended up with a 25 ohm drain resistor and an 80 ohm gate resistor.

The final step was to add the bias circuit and complete the layout. In order to simplify the design I decided to use a gate voltage of 0V. A 3V drain bias provided the best performance. As shown in Figure 7, this biases each transistor at ~7mA. I added the drain bias pad behind the largest inductor that fit on the layout. This slightly degraded performance.

Simulations
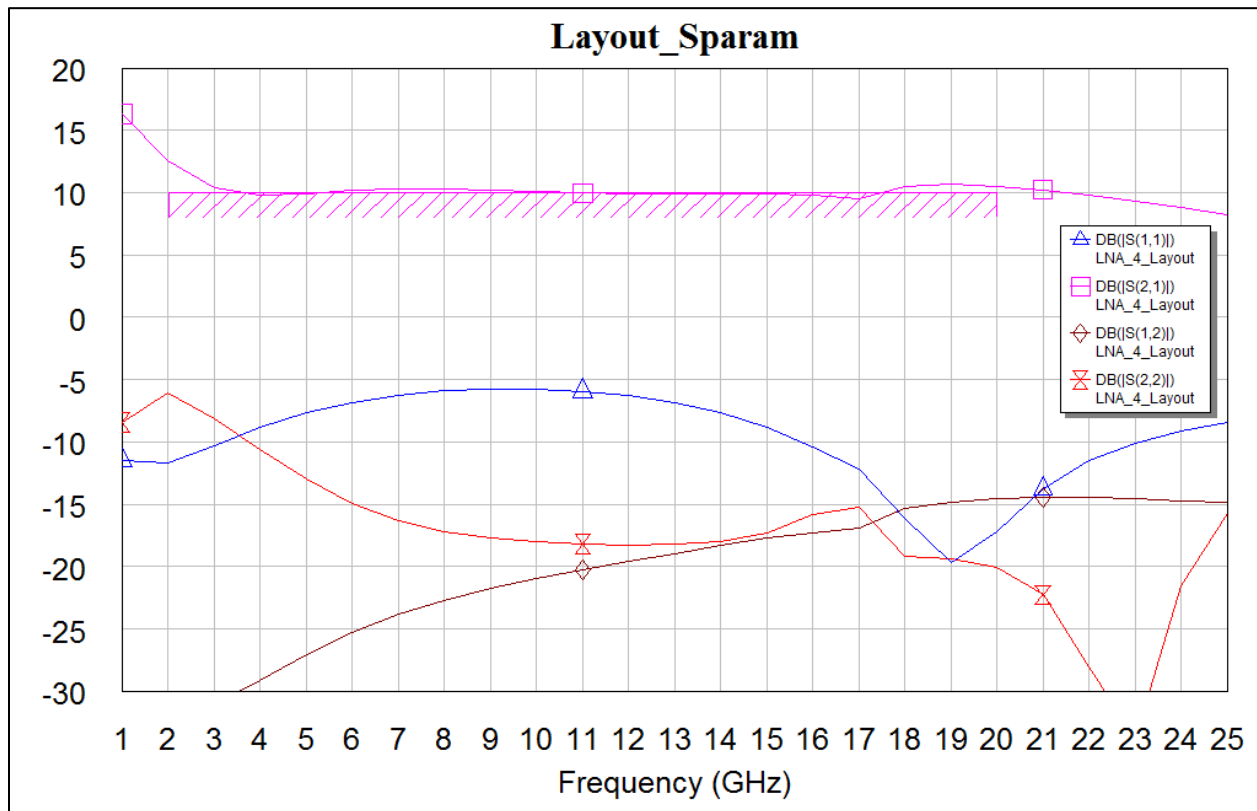
Figure 3. Linear simulation of final design.

The addition of the bias circuit and changes during final layout slightly affected the gain. At 17GHz the gain dips below the spec to 9.5dB. The gain flatness was 3dB with the highest gain being 12.5dB at 2GHz. The gain roll off at the high end of the band is rather gradual which should help reduce any performance degradation from modeled to measured. The input return loss is below -5dB across the band while the output return loss is mostly below 10dB across the band.
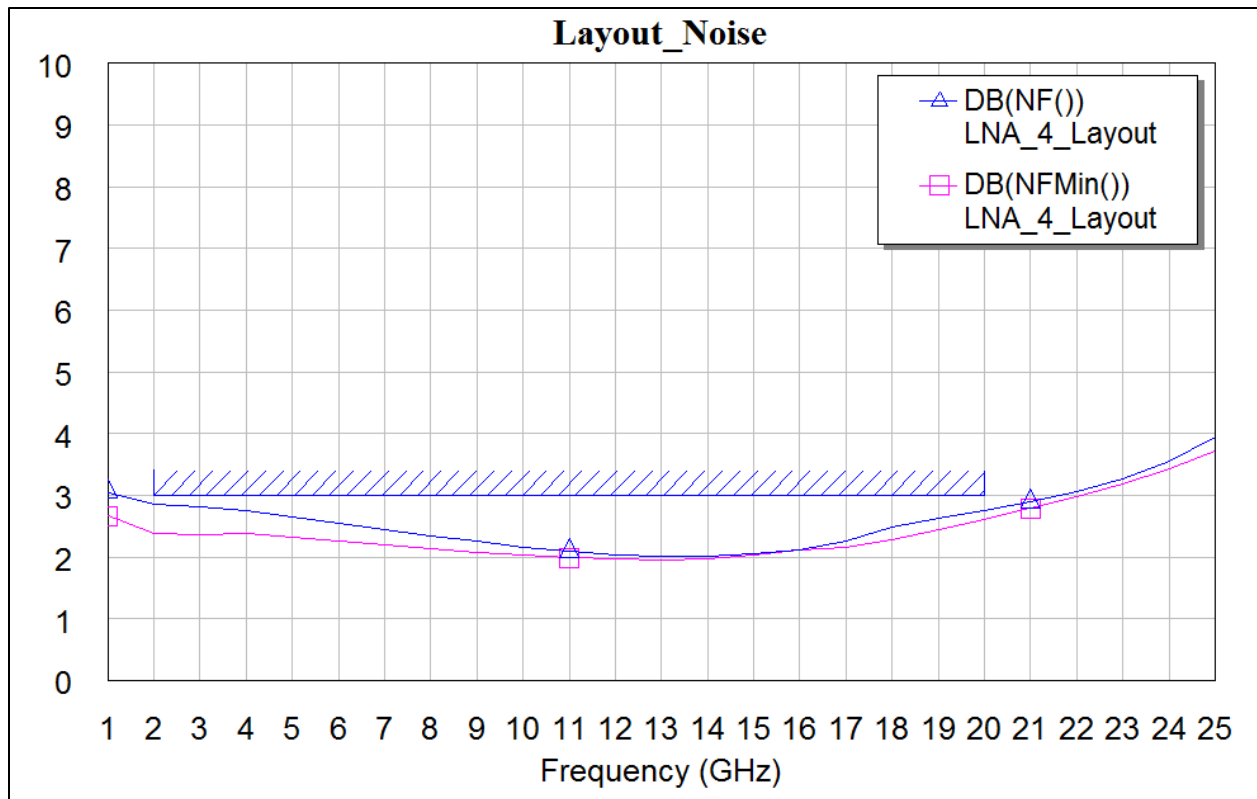
Figure 4. Noise figure simulation of final design.

With the smaller transistors the noise figure was flat around 2dB across the band. With the larger transistors the noise figure pulled up on the ends of the band but was still below the spec. The lowest noise figure is 2dB at 13GHz. The highest noise figure is 2.85dB at 2GHz.
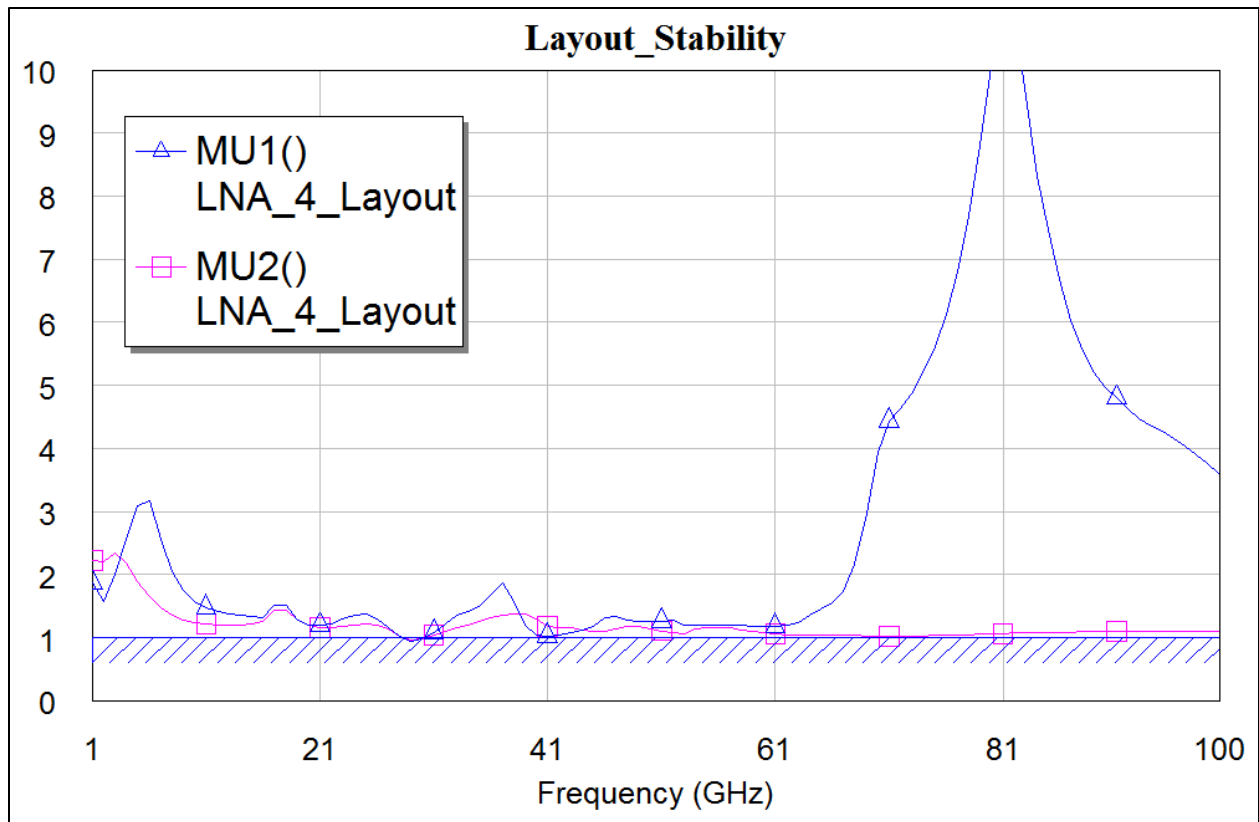
Figure 5. Stability simulation of final design.

The design is unconditionally stable up to 100GHz. This was achieved by tuning the resistors as well as the length and characteristic impedance of the transmission lines.
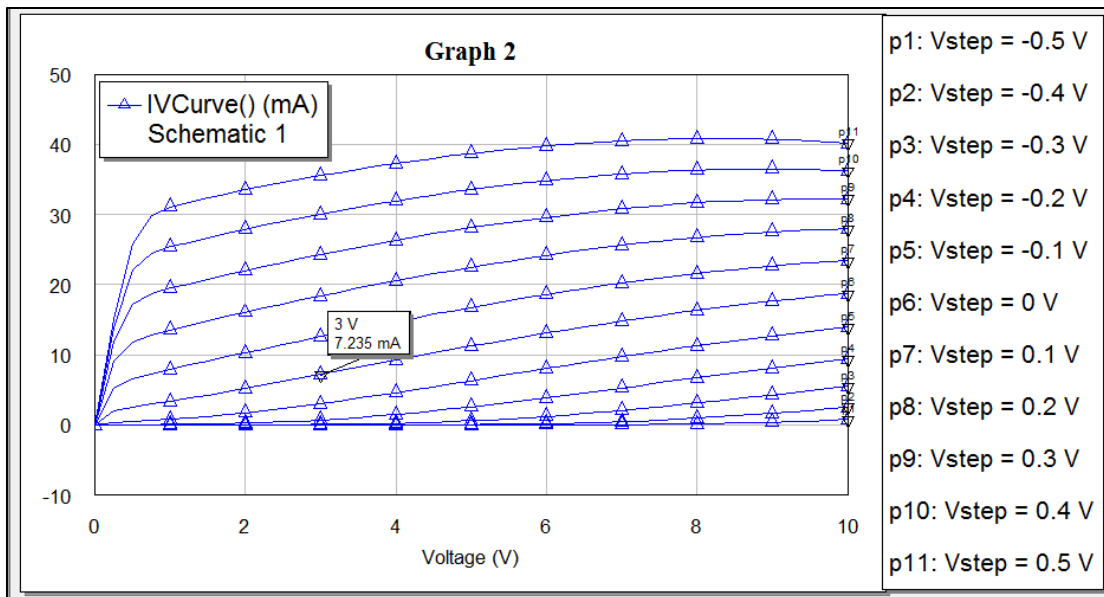
Figure 6. The DC operating point
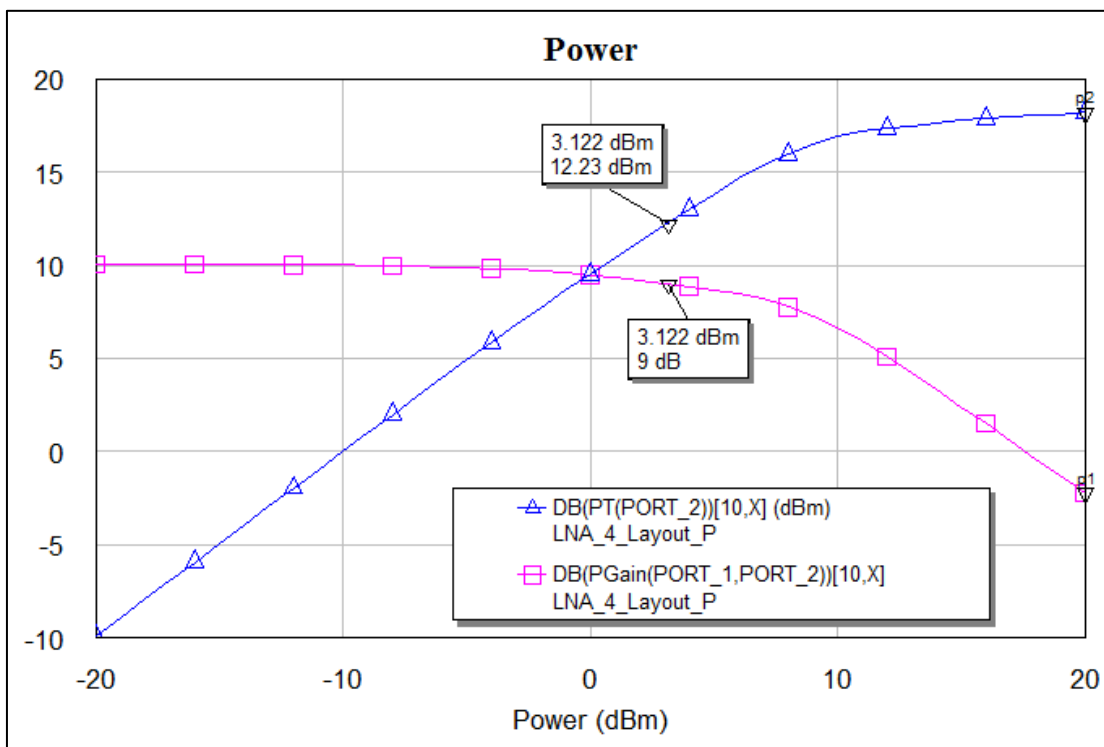
Figure 7. Power with P1dB highlighted

The bias and power simulations are shown in Figure 7 and Figure 8 above. I chose to bias the LNA with 0V on the gate and 3V on the drain. This means that each transistor draws ~7mA of current. The 1dB compression point of the LNA is at 12.2 dBm.

Schematic
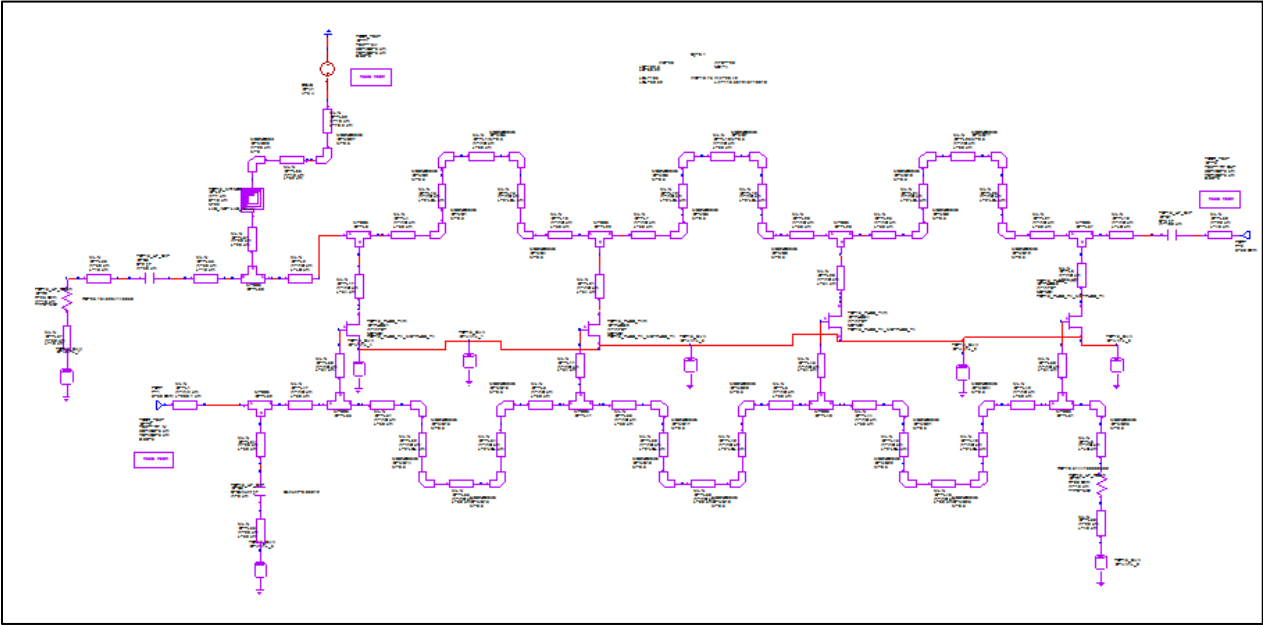
Figure 8. Final schematic with interconnects
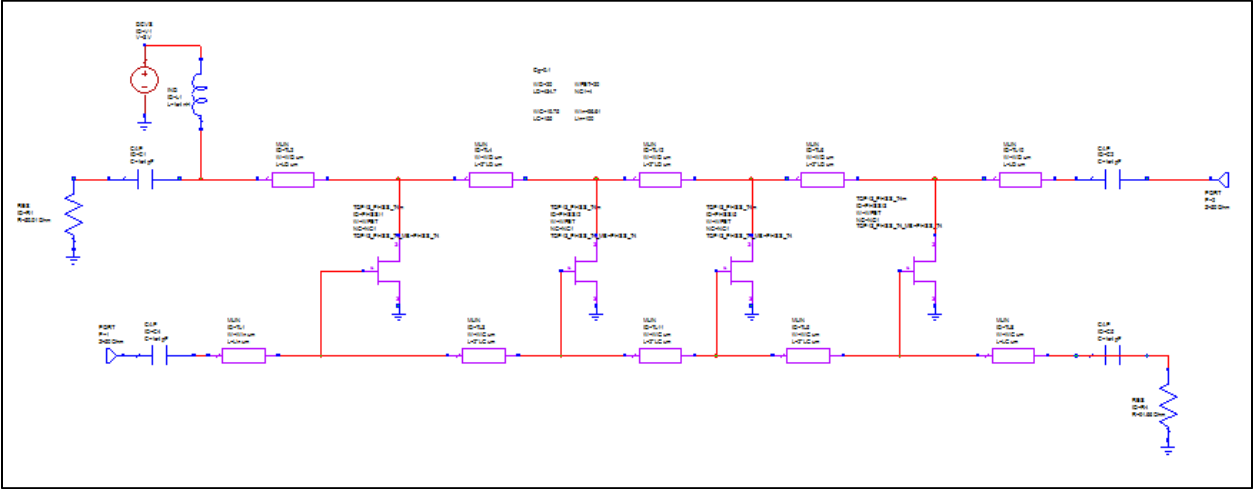
Figure 9. Final schematic without interconnects
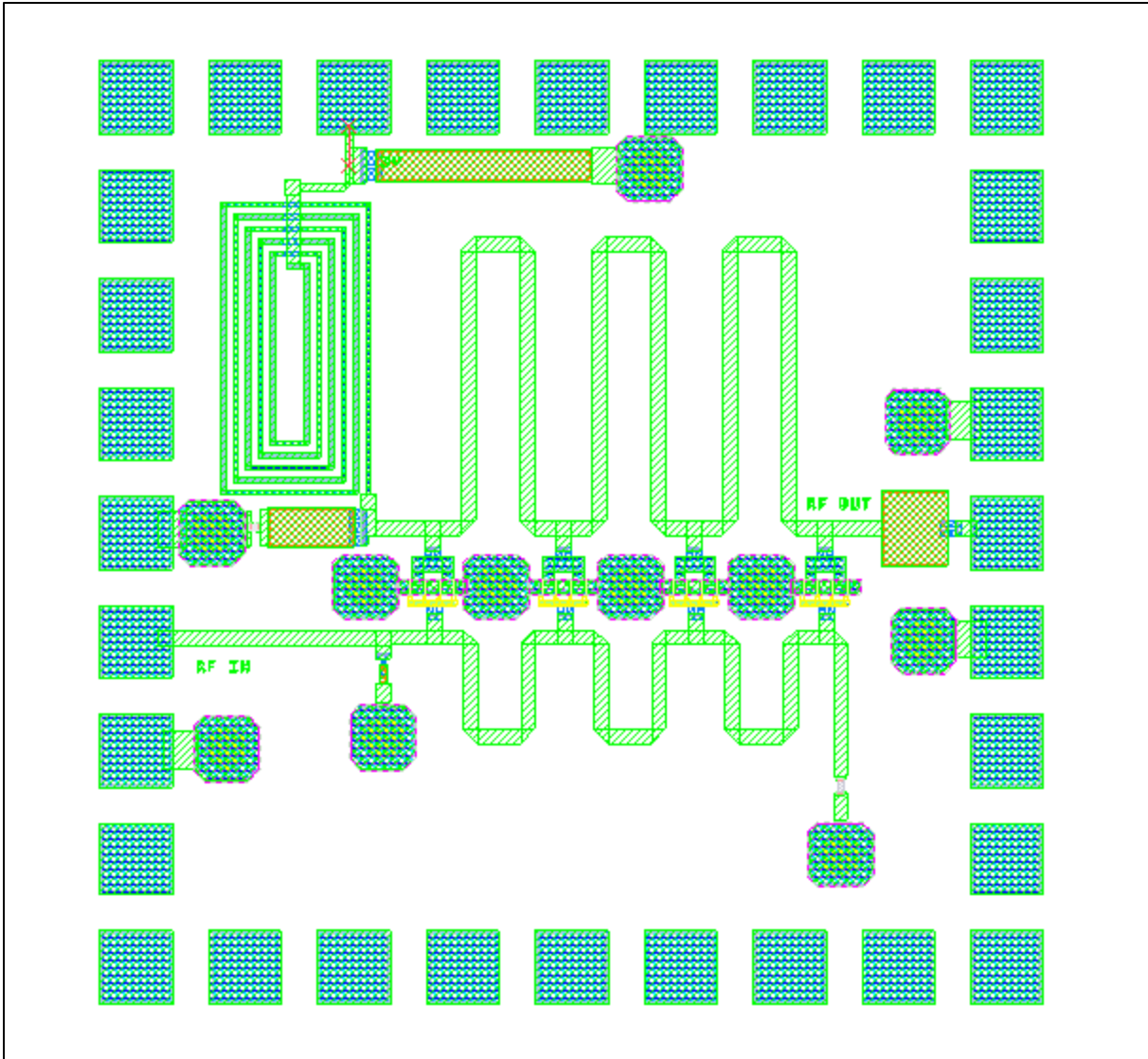
Figure 10. Layout

The design fit well on the given chip size. Given more room, I would be able to increase the bias circuit inductor which would bring the gain back up above 10dB. Adding a second ground via to each transistor helped performance significantly.

Test Plan

1) Connect power supply to DC pad
   a) Set current limit to 50mA
   b) Set voltage to 3V
2) Connect network analyzer to the RF input and output ground-signal-ground pads
3) Measure s-parameters of LNA and compare to simulated results
4) Connect noise figure source to input probe and noise figure meter to output probe
5) Measure NF and compare to simulated results

Conclusion

The distributed amplifier topology was the natural selection for this LNA design. With this topology I was able to achieve good performance over the required band of 2-20GHz. By adjusting the transistor size I was able to balance the gain and noise figure performance of the circuit. This design meets the noise figure specification of 3dB. It meets the gain requirement of 10dB across most of the band but dips down to 9.5dB at the lowest point. The design is also unconditionally stable.

Low Noise Amplifier 2-20 GHz

EN.525.787 MMIC Design

Robert Reyes

12/13/2012

1 Contents

2   Abstract

The design is a wideband low noise amplifier using the TriQuint 0.13um pHEMT process, fitting on a 60x60mil GaAs chip. The low noise amplifier operates over a 2-20 GHz bandwidth, providing roughly 10dB of gain across the entire band with a low noise figure less than 3dB. The return loss is less than -10dB over the majority of the band.

3   Introduction

The low noise amplifier (LNA) is used to amplify weak signals while adding minimal noise to the system. The LNA in this paper was designed to operate over a wide bandwidth (2-20 GHz) with modest gain (~10dB) and a reasonably low noise figure (<3 dB) using the TriQuint 0.13um pHEMT process (TQP-13N). This particular LNA design uses a distributed amplifier approach to achieve the required RF performance over the entire frequency band.

4   Design Approach

4.1   Specifications vs. Goals

TriQuint provided the following suggested specifications for a wideband low noise amplifier: 2-20GHz, NF < 3dB, P1dB > 17.5, and variable gain. From these, the following specifications for this design were generated: the low noise amplifier shall operate from 2 to 20 GHz with a gain of approximately 10dB and noise figure less than 3dB. The design shall also use the TriQuint 0.13um pHEMT process. The 1dB compression point of 17.5dBm is considered to be a goal, although the design focus was mainly on achieving the gain and noise figure specifications. Another goal was to make the design stable when looking into a 50-ohm match.

4.2   Trade-offs

Distributed amplifiers are known for providing relatively flat gain over a large bandwidth. Because this low noise amplifier design had to operate over a wide frequency band, the distributed amplifier architecture was selected as a baseline versus a multi-stage amplifier design. The distributed amplifier template was also selected due to the uniform inductor structure between stages, making it simpler to add or remove stages during the initial design process. The designer started the design with a three-stage distributed amplifier architecture and three stages proved to be sufficient to provide the necessary RF performance.

Initially, the design used FETs with a 6x50um periphery. This was due to the availability of an S2P file for the 6x50um FET biased at 3V and 30mA; however, it was difficult to stabilize the circuit and achieve gain flatness. Reducing the number of fingers and finger length to a 4x20um periphery, while maintaining a gate voltage of 0V, resulted in a vast improvement in the RF performance of the LNA circuit. Flatter wideband gain was achieved and the circuit became unconditionally stable. Reducing the periphery also reduced the current draw of the device, thereby improving the noise figure of the LNA. The DCIV curve of the 4x20um FET is seen below. At a gate bias of 0V, the device drew a drain current of ~7mA at a drain voltage of 3V.

Figure A: DCIV Curve for 4x20um pHEMT
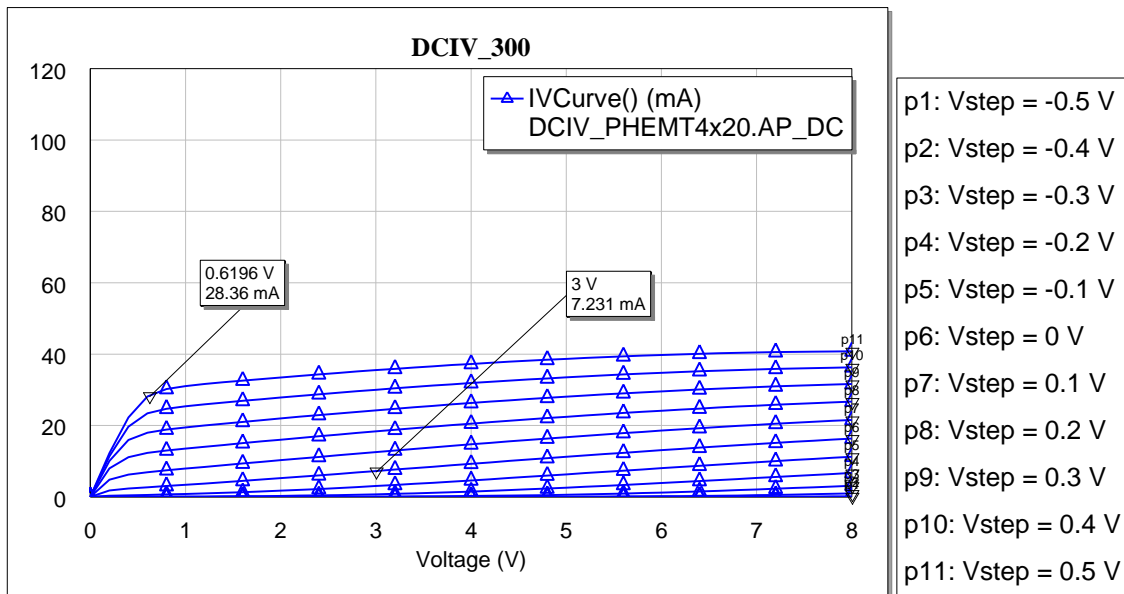
Another trade-off is the use of microstrip transmission lines for tuning instead of inductors. In the initial design, ideal inductors were used as a baseline but this gave way to microstrip transmission line. The reason for this switch is that the inductor values proved to be relatively small and microstrip lines would be easier to size/tune to the needed inductance, using the rule of thumb of 1pH/1um of inductance, instead of trying to adjust the spacing and number of turns to size the inductors appropriately. Also, space was not an issue when switching to a microstrip realization of the circuit. If the LNA design had tighter chip size constraints, then using inductors instead would significantly reduce the amount of space used.

5 Simulations

5.1 Linear

As seen in Figure B, the gain is approximately 10dB across the entire band. The return loss is decent across the majority of the band but it does roll up to roughly -6.5dB at the lower band edge. Figure C shows that the noise figure is well below the specification of less than 3dB. It is much better at the high end of the band than the low end though. Both figures indicate that the design meets both gain and noise figure specifications.

Figure B: S-Parameters for LNA
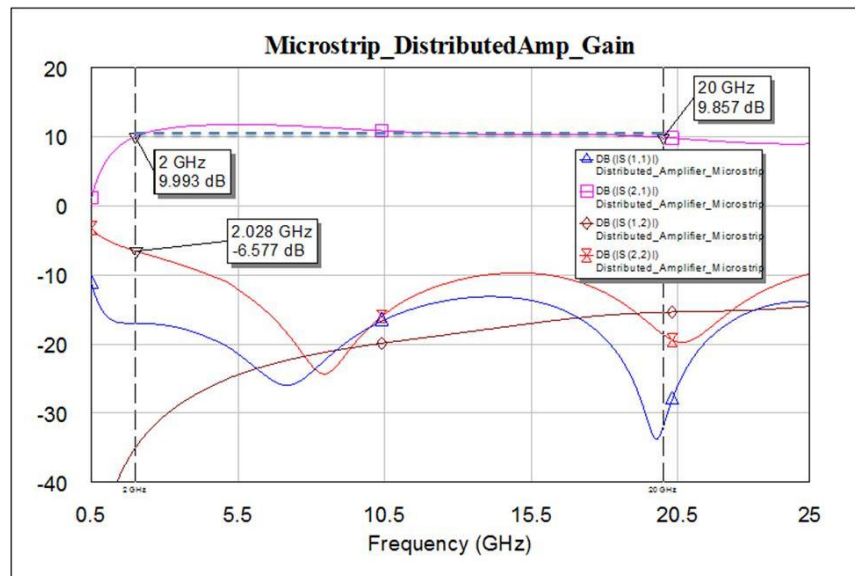
Figure C: Noise Figure for LNA
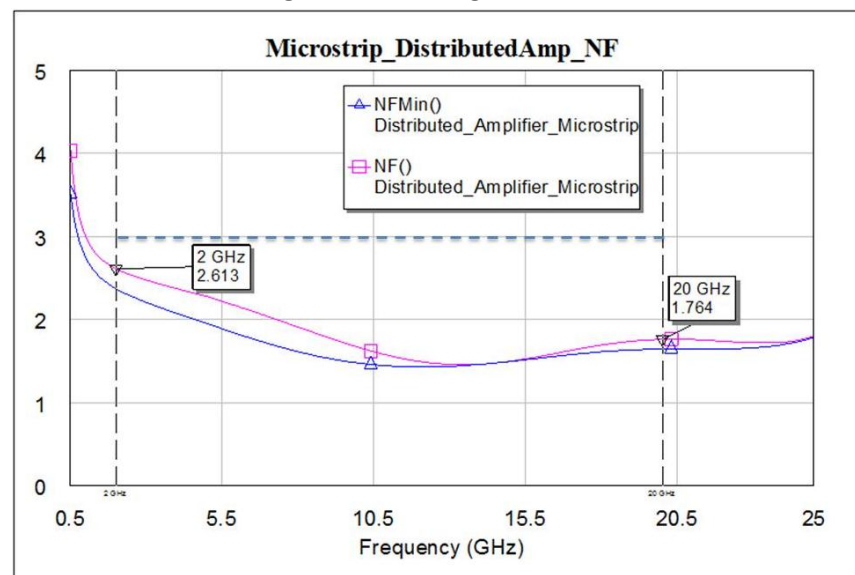
One goal for the design was to make the LNA circuit unconditionally stable. There were issues achieving this when initially designing with the 6x50um FET sizes, but after switching to the 4x20um periphery, the design became unconditionally stable. The design's stability is seen in Figure D, where the stability factor is shown to be greater than 1 up to 100GHz.

Figure D: Stability up to 100GHz for LNA
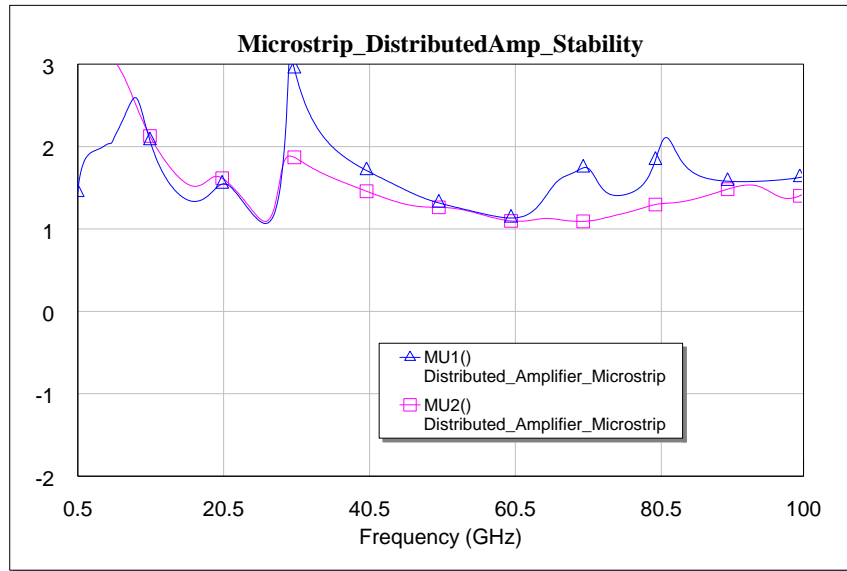
5.2 Nonlinear

One of the goals listed by TriQuint was to achieve a P1dB of 17.5dBm; however, this particular goal was not worked towards. As seen in Figure E, the 1dB compression point, at 10GHz, was found to be 10.87dBm at 1.056dBm in. Figure G shows the family of compression and gain curves from 2 to 20GHz at 1GHz steps. The saturated power appears to be around 18dBm, as seen in Figure G.

Figure E: Compression Curve for LNA at 10GHz
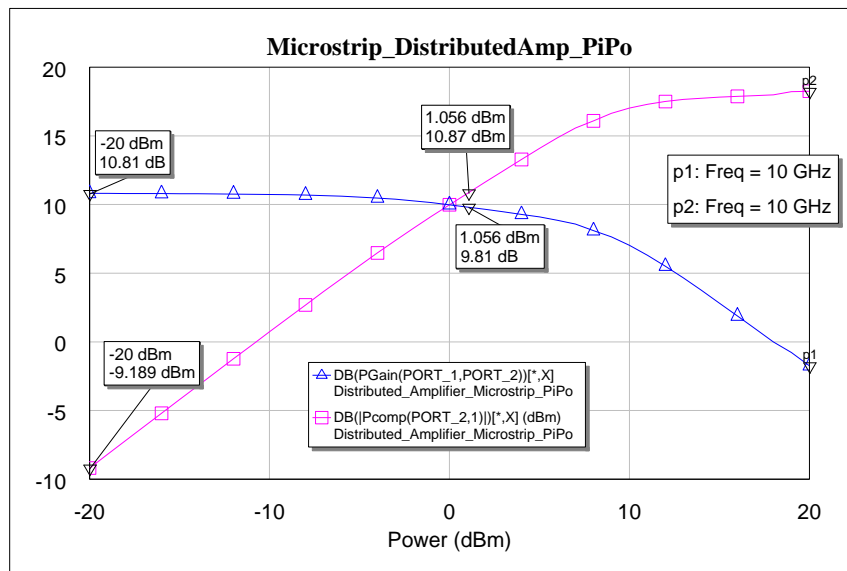
Figure F: Output Power versus Input Power for LNA
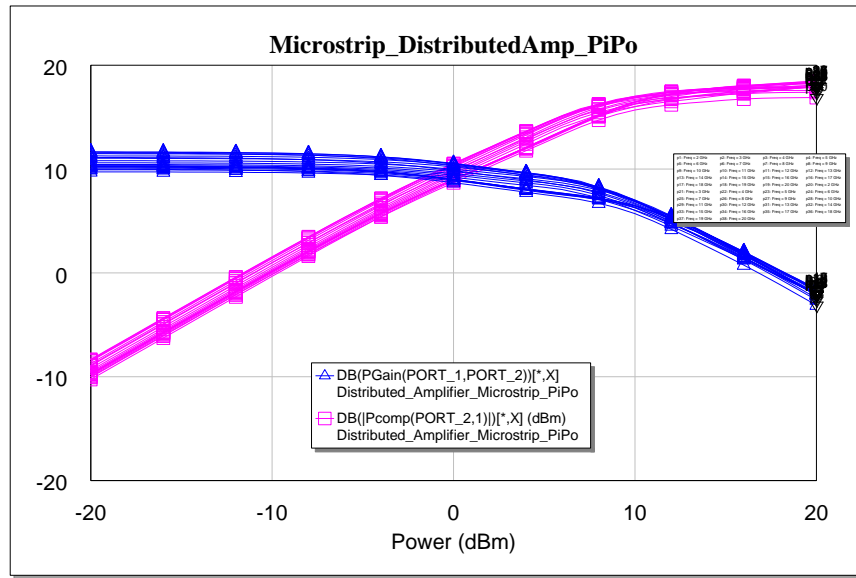
Figure G: Output Power versus Frequency for LNA
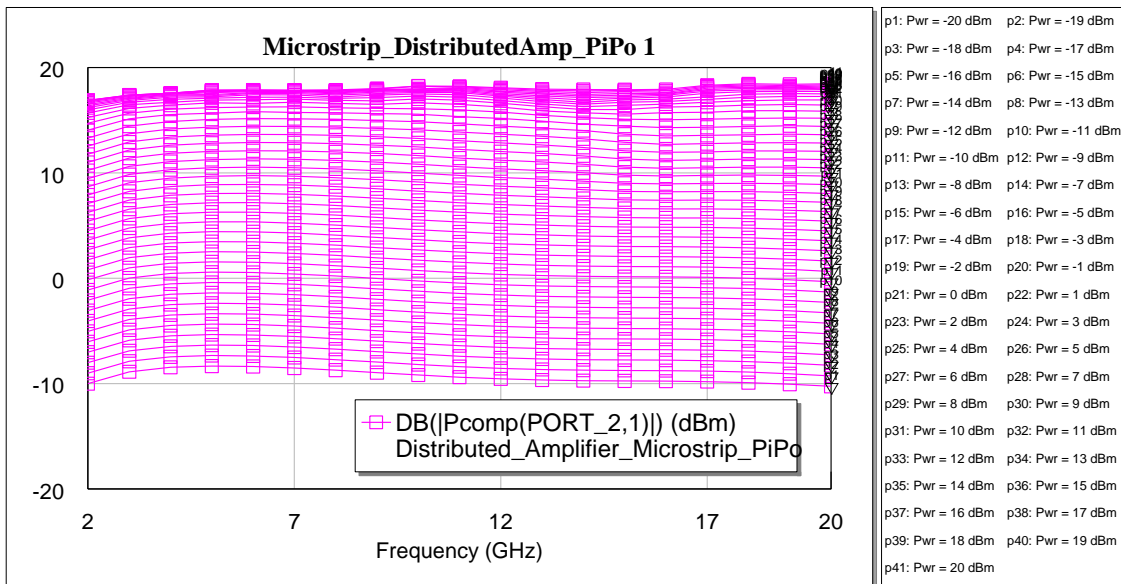
5.3 Bias (DC Analysis)

The DCIV curves for the TOM4 pHEMT model for the 4x20um FET size indicated that a 3V drain voltage with a 0V gate bias would draw approximately 7mA of current. Figure H below shows the DC simulation results at each stage in the distributed amplifier circuit. The simulated current draw corresponds to the DCIV curve seen in Figure A. The total drain current is, as such, expected to be roughly 21mA.

Figure H: Drain Current and Voltage Draw Per Stage
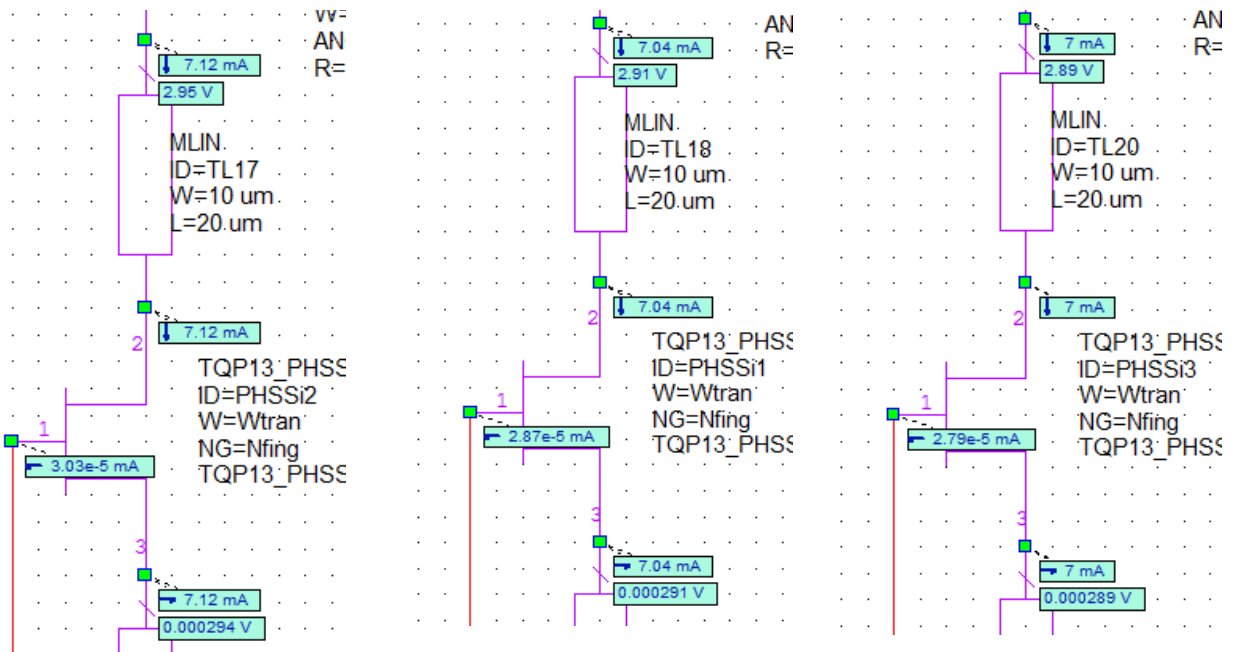
6   Schematic

6.1   Figure I: RF Schematic (without Interconnects)

6.2 Figure J: RF Schematic (with Interconnects)
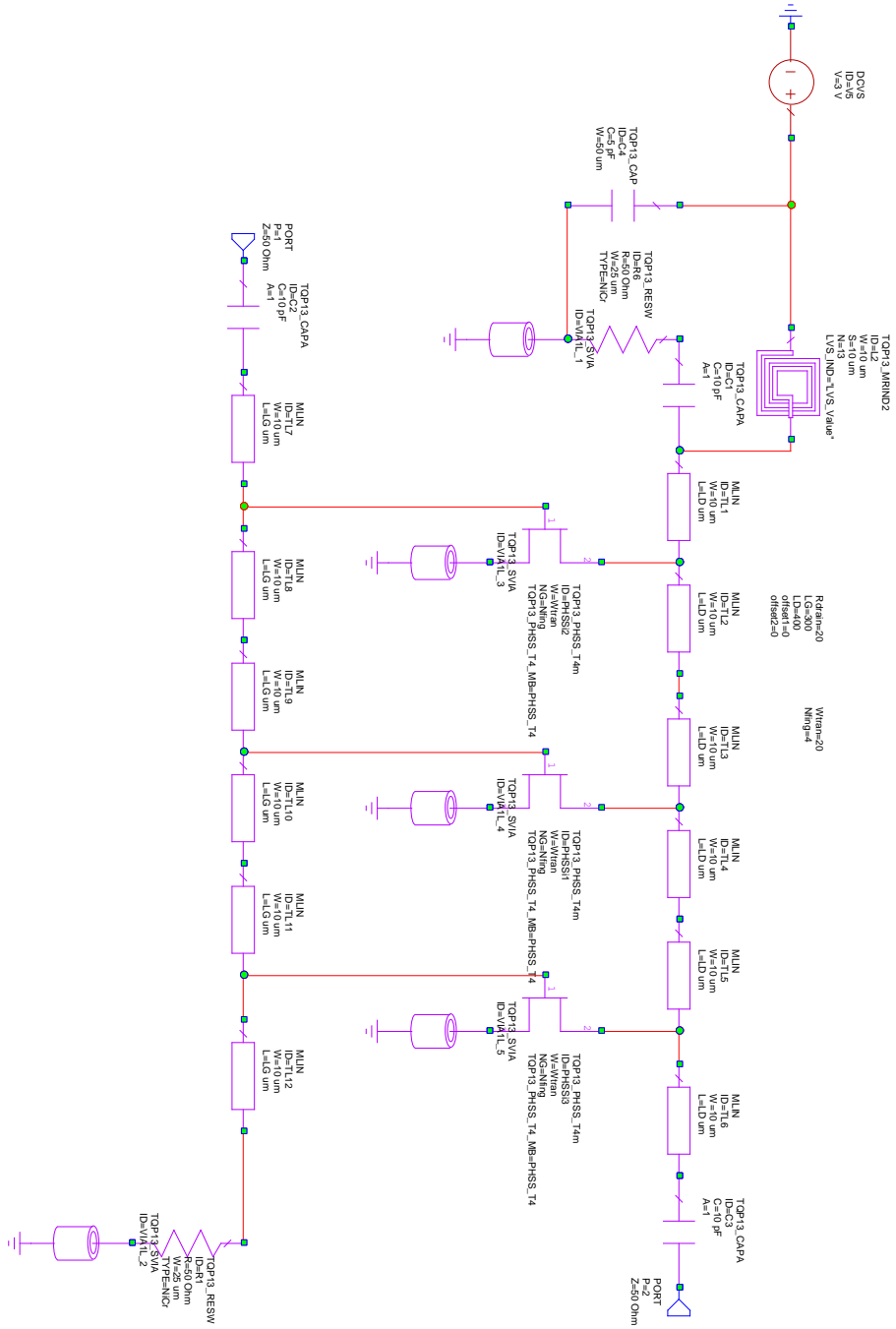
7 Layout

Figure K: 2D Layout of LNA
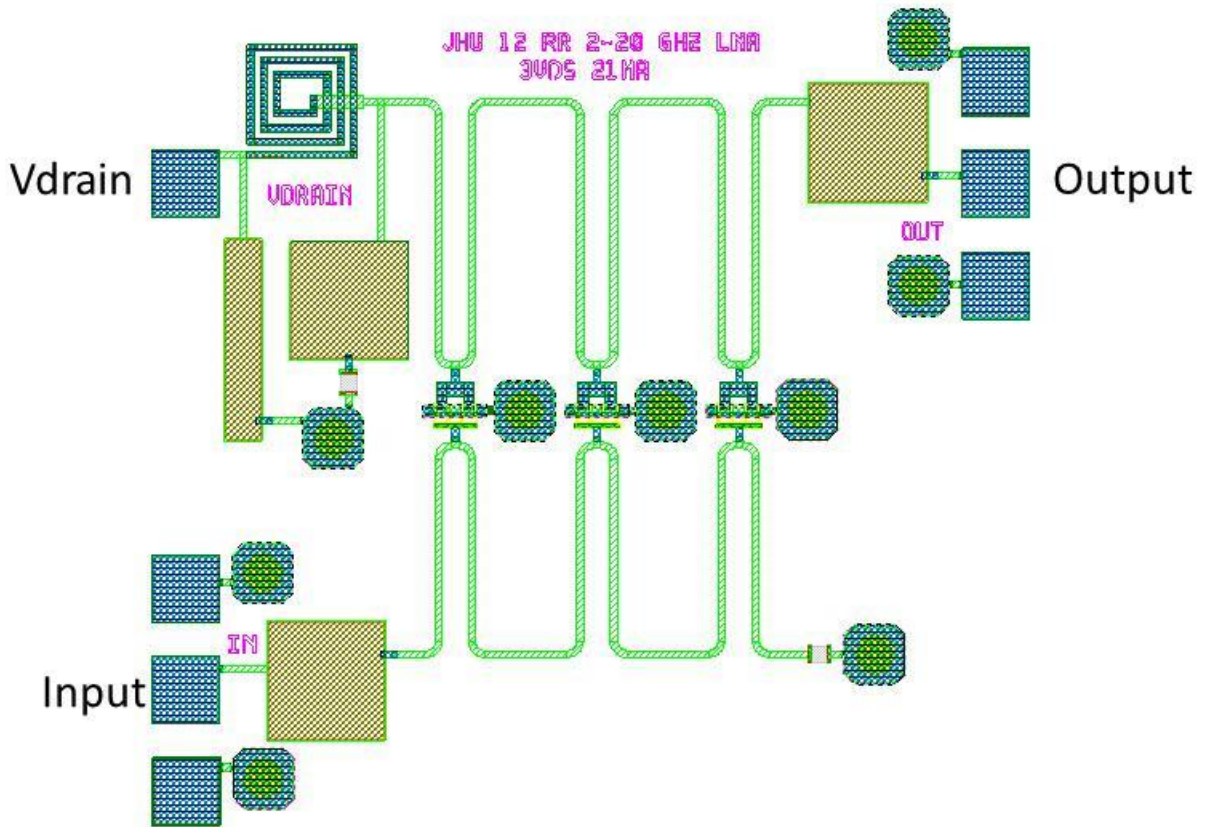
Figure L: 3D Layout of LNA
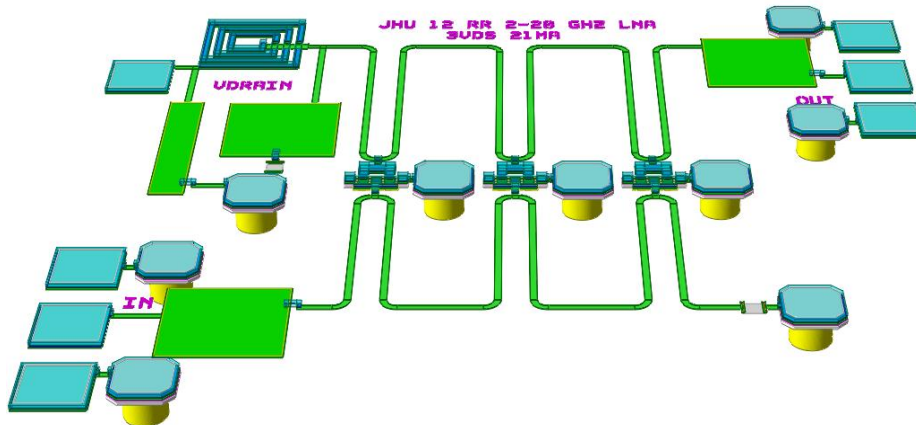
8   Test Plan

8.1   Equipment

For measuring the RF performance of the LNA, the following equipment is needed:

- DC power supply
- network analyzer, such as the Agilent 8510 or PNA
- RF signal generator
- spectrum analyzer or power meter
- noise figure analyzer

8.2   Measurements

8.2.1   DC Bias
1. Connect power supply to drain voltage pad.
2. Set power supply current limit to 30mA. According to the DC simulation, 21mA should be the expected current draw.
3. Set voltage to 3V. Turn power supply on to turn on low noise amplifier circuit.

8.2.2   S-Parameters
1. Connect Port 1 of Network Analyzer to pad labeled "In" and Port 2 to pad labeled "Out".
2. Set frequency range from 1 to 21 GHz and input power level to -20dBm.
3. Measure S11, S12, S21, and S22 of the device. The expected gain (S21) is 10dB across 2 to 20 GHz with a return loss of roughly -10dB across the majority of the band.

8.2.3   Noise Figure
1. Connect circuit to a noise figure analyzer.
2. Measure noise figure from 1 to 21 GHz.

8.2.4   Output Power/Compression
1. Connect output of RF signal generator to the input of the LNA. Connect power meter or spectrum analyzer to the output of the LNA.
2. Beginning at -10dBm, measure the output power at 1dBm steps up to 10dBm, from 2-20GHz in 4GHz steps. Expected P1dB point at 10GHz is 10.8dBm out at 1dBm in.

9   Conclusion

For this design, it was shown that a low noise figure and modest gain is achievable for a wideband low noise amplifier. This was obtained by using a distributed amplifier architecture, which is known for its wideband applications. With a three-stage distributed amplifier circuit using 4x20um transistors, the design was able to meet the specifications of 10dB gain and less than 3dB noise figure from 2 to 20GHz. The gain was also decently flat across the band of interest. In simulation, the circuit was shown to be unconditionally stable up to 100GHz. The P1dB point was found to be approximately 11dBm and the saturated power was roughly 18dBm, according to the nonlinear simulation. One improvement for the design would be to convert the microstrip lines, which were used for tuning, to inductors in order to save space. Overall, however, the low noise amplifier design was successful in meetings the specifications.

Wideband LNA 5-15 GHz

Designed by Michael Coon

For JHU EP class EN525.787 MMIC Design

ABSTRACT:

The purpose of this design was to see just how wideband one could make an LNA using TriQuint's MMIC fabrication process and more traditional amplifier design, rather than a distributed amplifier design. The requirements used to guide the design were those of one of TriQuint's old wideband LNA designs. While the design did not meet the bandwidth requirement of 2-20 GHz, it did get fairly close, while maintaining more than enough gain and noise figure performance.

INTRODUCTION:

Low Noise Amplifiers are used as the first component in a receiver chain to set up the noise performance for the rest of the system and provide some gain to the weak signal coming into the system. For this purpose, an older MESFET design by TriQuint had a bandwidth of 2-20 GHz, with a gain of at least 10 dB and a noise figure of less than 3 dB throughout the band. In the pictures of the circuit it appeared that this performance was obtained using a distributed amplifier setup. Since the new pHEMTs have a larger operational bandwidth, I decided to see just how far I could push the bandwidth of a more traditional 2 stage LNA design.

In forgoing the distributed amplifier design, I realized that I would be making several trade offs that would affect performance, both negatively and positively. First, I realized that the bandwidth would probably not be able to match that of a distributed amplifier. My design only has two stages, and each individual stage would not be nearly enough to get the full range of a distributed amplifier, however I was hoping that the next trade off would make up for that. The second trade off being gain. It was my hope that by doing a design in which I am directly matching one stage to get gain, that I would be able to exceed the overall gain of a distributed amplifier. The only thing I was not aware of is how much my noise figure would be affected by going with a two stage amplifier design. Though it was my hope that I would be able to get a slightly better noise figure than with the distributed amplifier.

DESIGN PROCESS:

For the design process, I designed each of the two stages differently. The first stage was designed at 11 GHz to be a textbook LNA with some noise figure traded off to get more gain. This lead to the following linear S-parameter simulation shown on the next page. It is worthwhile to note that the gain is not at a maximum at 11 GHz due to the trade off between gain and noise figure. The noise figure of the circuit (not shown) was about 1.335 at 11 GHz and stays below 3 dB from 3.5 GHz up to at least 30 GHz which was a fairly promising start.

S Parameters

7.732 GHz
9.795 dB

DB(|S(1,1)|)
LNA 11 GHz

DB(|S(2,1)|)
LNA 11 GHz

DB(|S(1,2)|)
LNA 11 GHz

DB(|S(2,2)|)
LNA 11 GHz

Frequency (GHz)
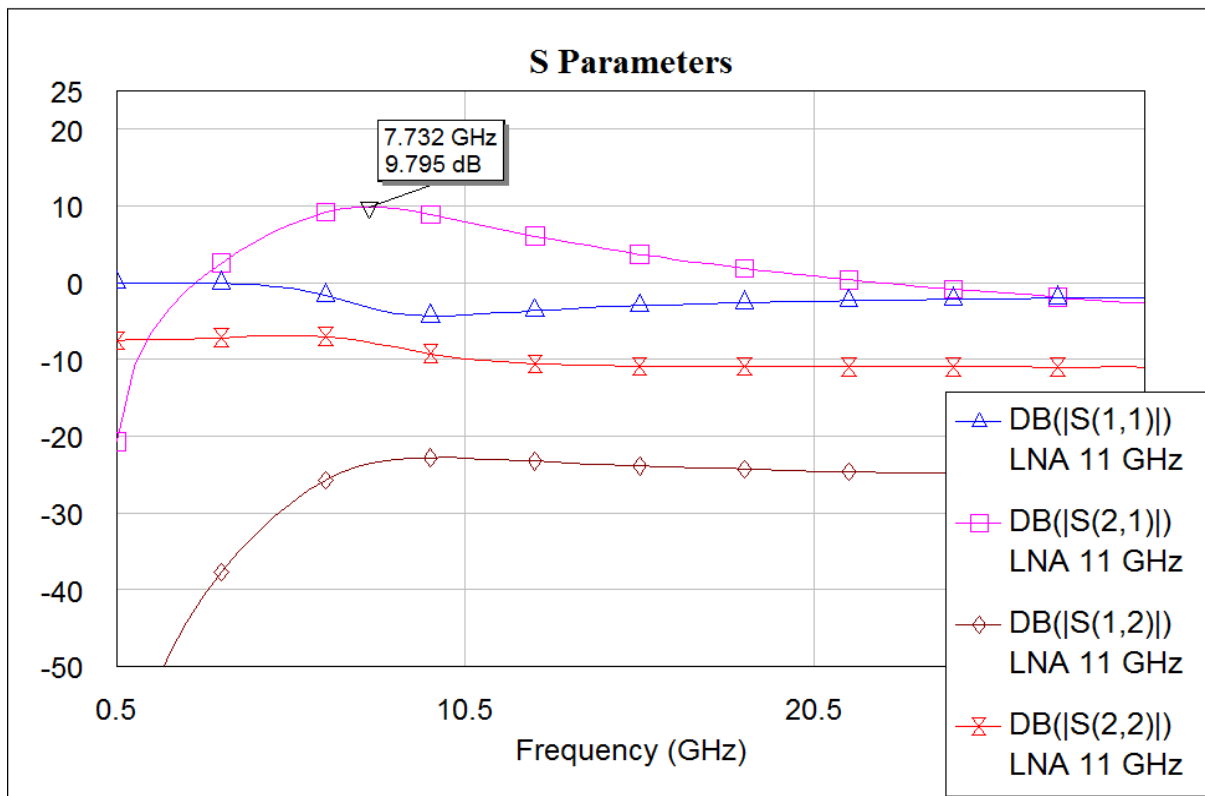
Next, in order to bring up the gain throughout the band of interest, I designed a conjugate matched amplifier at 14 GHz. The goal here was to take the gain that is already present and close to what is required, and boost the areas that were not high enough. Fourteen gigahertz seemed like a fairly good point to do this between the first stage was designed at 11 GHz and had a gain maximum at 7.7 GHz, so for the most part the lower frequencies were fairly well off. From there, the circuit was combined into a two stage amplifier and some work was done to keep the amplifier stable. The following page shows the resulting S-parameters and noise figure.
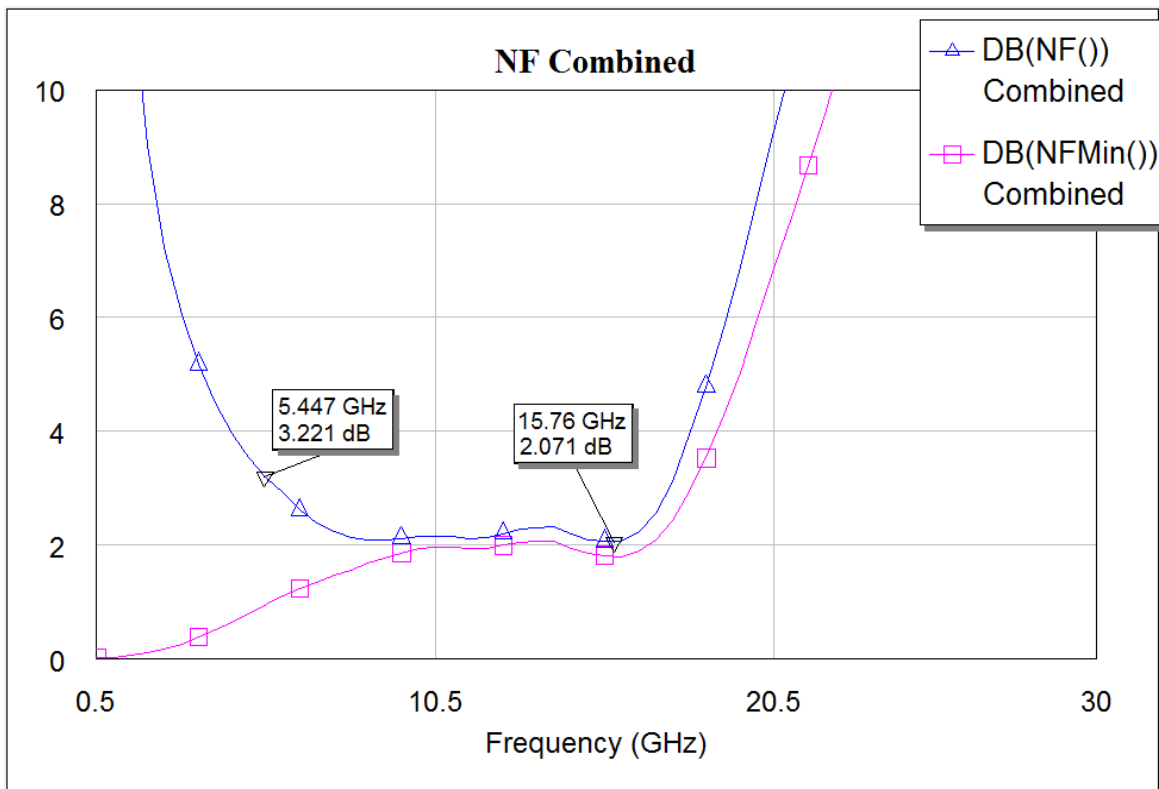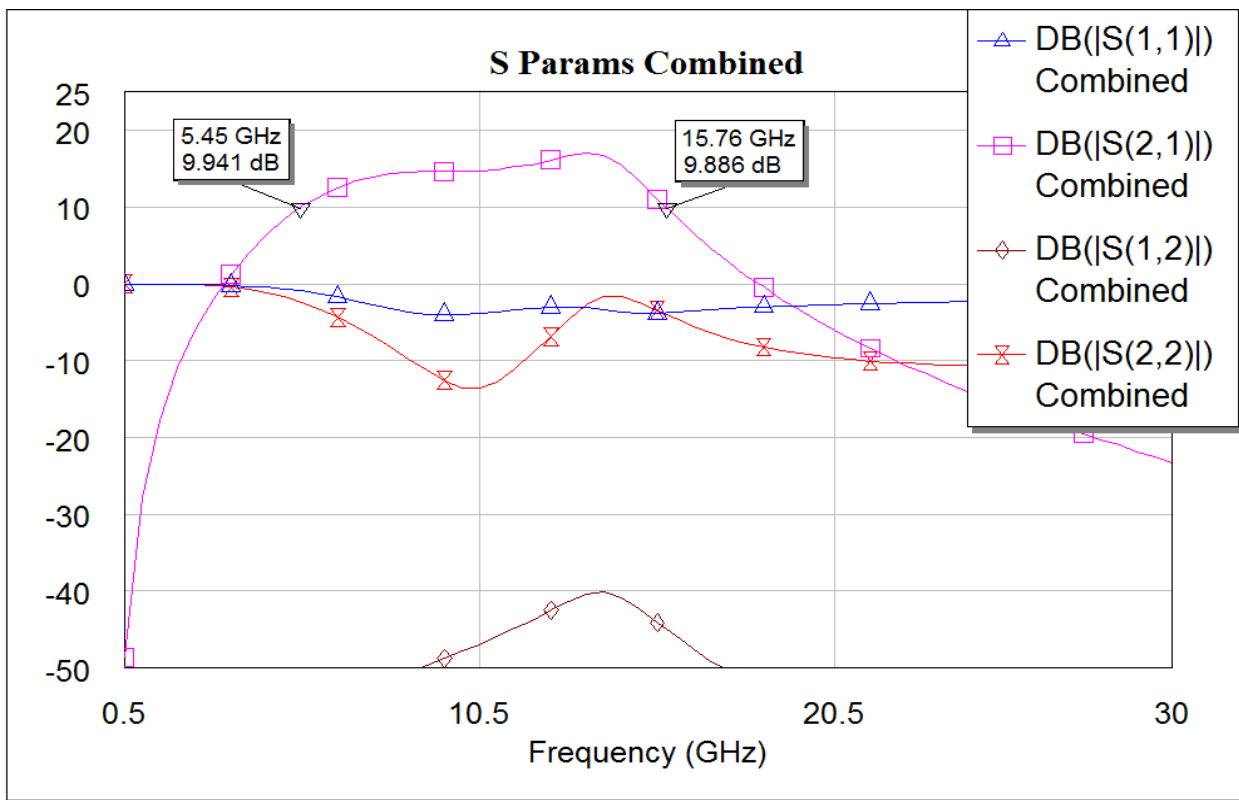
As can be seen, the gain was above the requirement from 5.45 GHz and 15.76 GHz however the noise figure was a bit high. These simulations were done with an S-parameter file instead of a pHEMT model, so I assumed that performance would change with the non-linear model and proceeded.

In order to choose a bias point for the design, I tried to mimic that of the S-parameter file for the LNA portion of the design which lead to a voltage of about 5.2 V due to my stabilizing resistor being in series. This is a happy coincidence since it is fairly close to TTL voltage levels meaning it could be used near or in conjunction with digital circuitry with a small performance hit. The results of non-linear simulation are shown below.
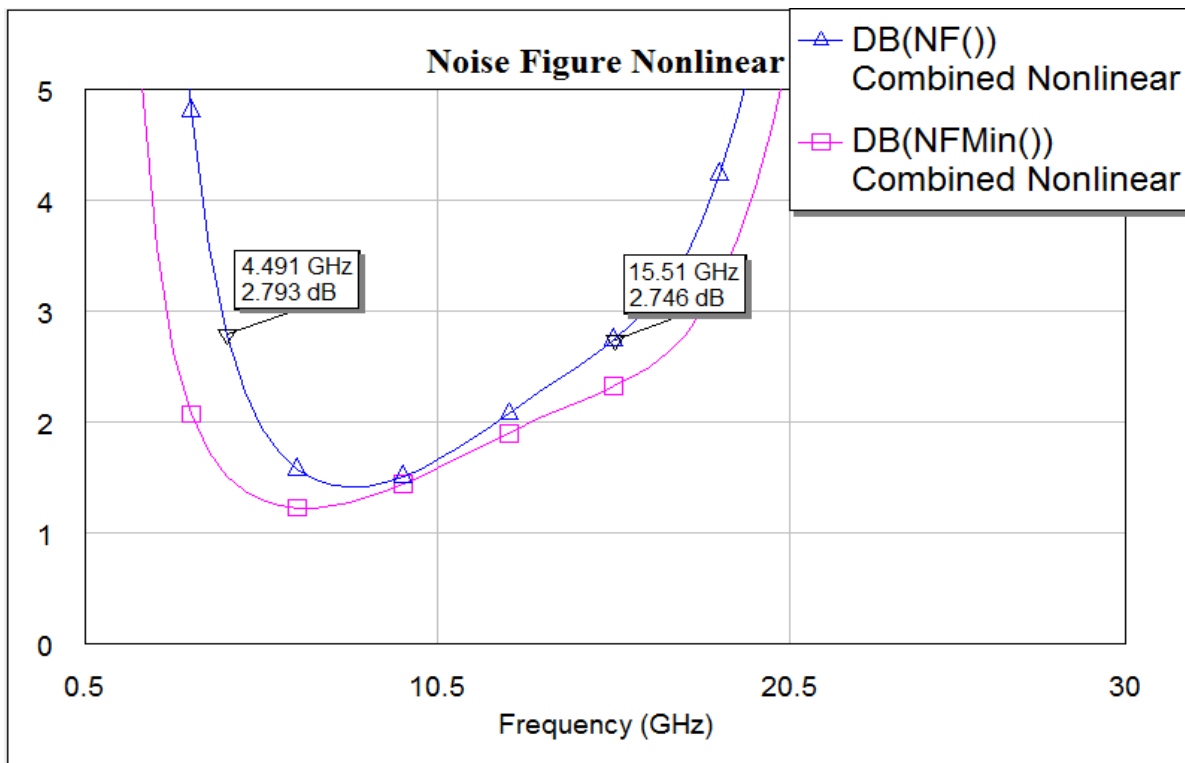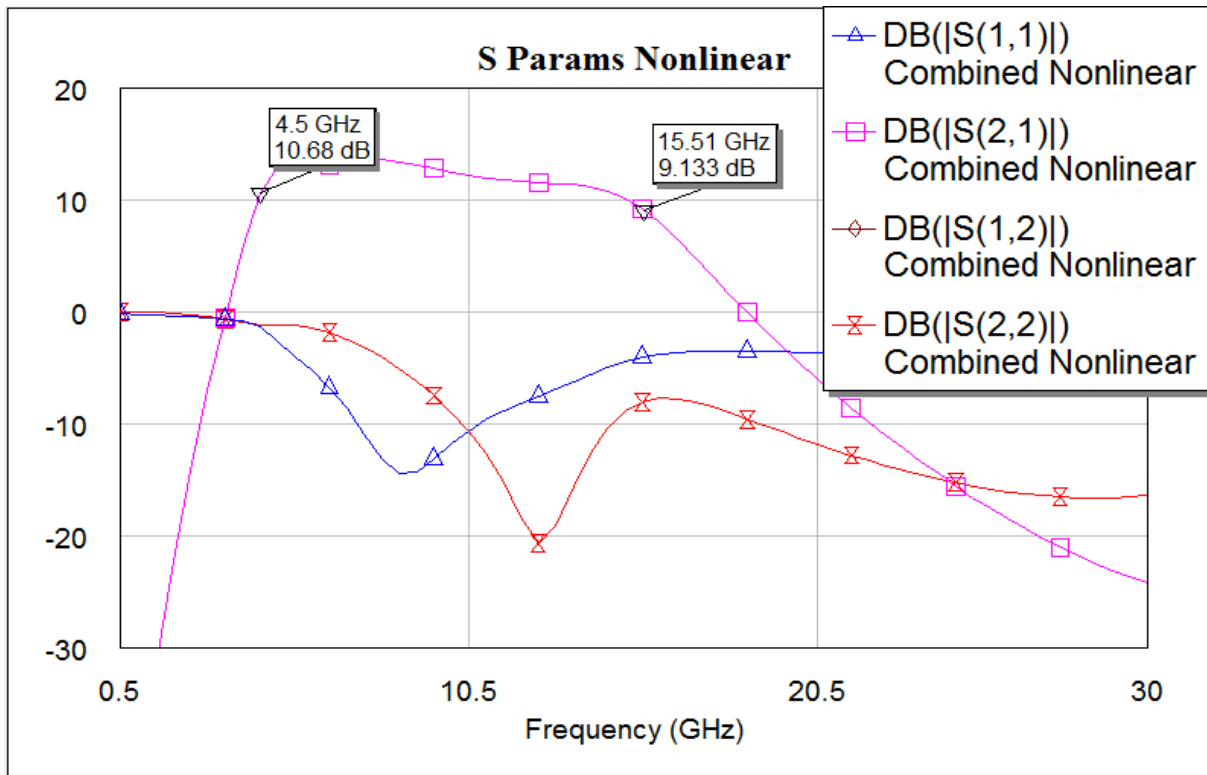
The change in the shape of S21 is due to the addition of interconnects to the circuit. As can be seen, over a reasonable range from 4.5 GHz to 15 GHz, the gain is above 10 dB and the noise figure is less than 3 dB. Return loss is also fairly good in place with S22 measuring -20 dB at 12.5 GHz and S11 measuring -14.5 at 8.5 GHz. The following is a schematic level view of the amplifier without connections between the parts.
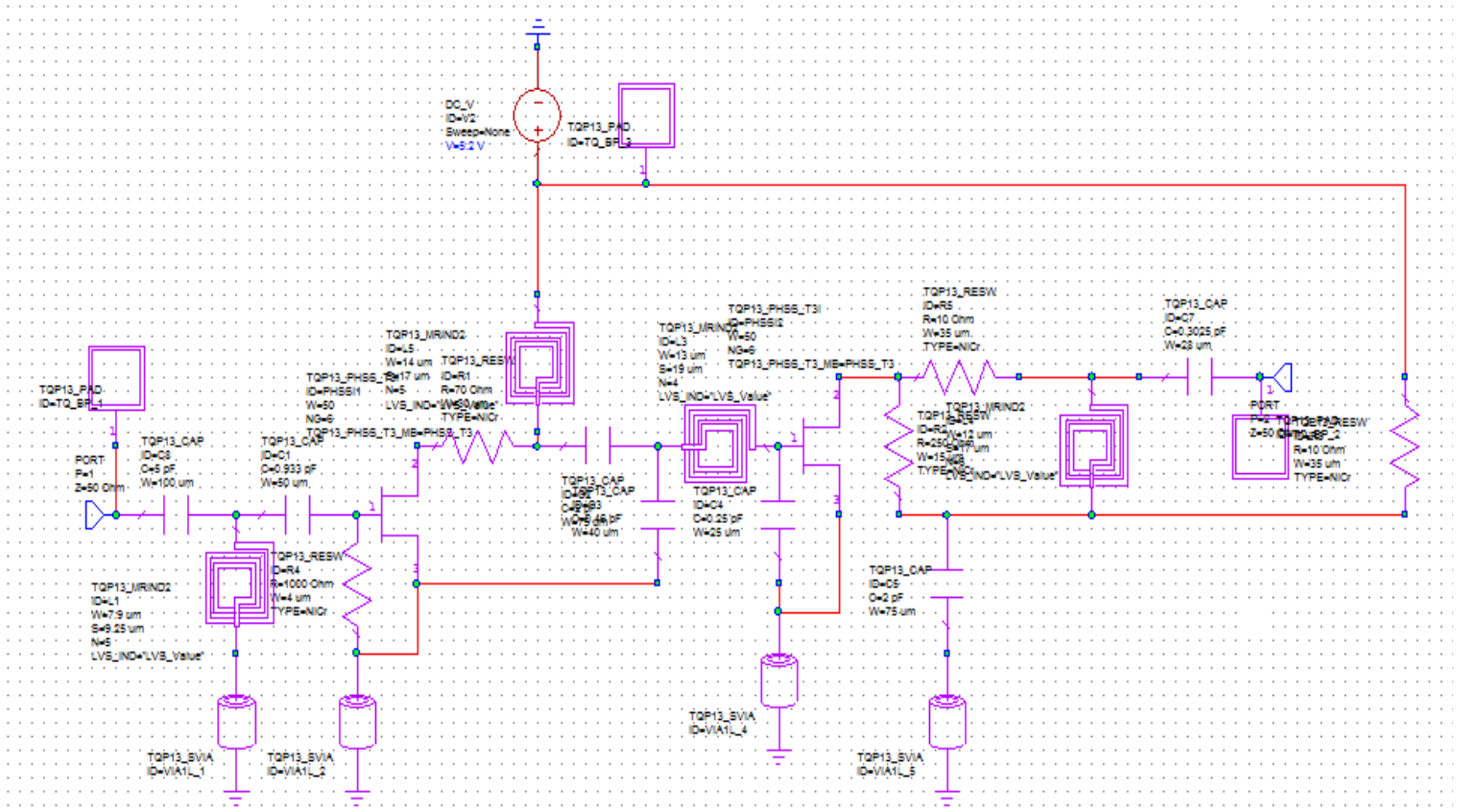
The finished layout is shown below:
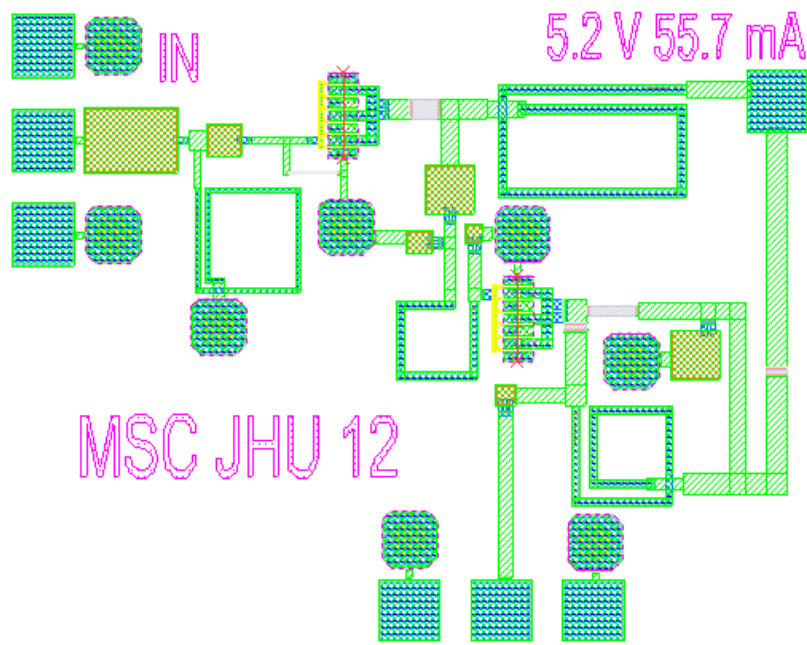
For probing purposes, this circuit has ground signal ground connections, however in a packaged design, it would not. The lettering is not the finished labeling as the font used would not pass design rule checking.

TEST PLAN:

1) Hook up ground signal ground probes to the proper terminals as shown in the design.

2) Attach DC probe to the labeled test point.

3) Apply 5.2 V to LNA

4) Check current. If current is much greater or much less than 55.7 mA cease testing.

5) Use Network analyzer to gather S-parameters over entire frequency range

6) Use noise figure measurement equipment to gather noise figure data for entire frequency range.

7) Write down results and compare.

CONCLUSIONS:

I conclude that it is possible to make a fairly wideband LNA using traditional amplifier design techniques as opposed to doing a distributed amplifier design. That being said, the bandwidth will never be as large as a distributed amplifier, but the gain and noise figure can be comparable over a range of frequencies at less current draw. Therefore, such a design would be more appropriate for a battery powered or space flight project over a distributed amplifier design that would have several more transistors.

DESIGN OF A LOW-NOISE AMPLIFIER FOR
THE FREQUENCY RANGE 20 GHz to 30 GHz
By JOHN NOVAK

ABSTRACT

The purpose of the design project was to develop a stable low-noise amplifier with a gain in excess of 20 dB and a noise figure below 2.5 dB for the 20 GHz to 30 GHz frequency range. Low-noise amplifiers are required in receiver systems to increase the amplitude of low-level signals from the antenna with minimal addition of noise to the received signal. The low-noise amplifier designed is comprised of 4 stages, each of which has a transistor, input and output matching networks and bias feed lines. The amplifier of each stage is a pseudomorphic high-electron-mobility transistor (pHEMT). Each transistor is comprised of 6 fingers that are each 50 microns in width. The drain bias voltage of each transistor is three volts and the gate bias voltage is zero volts. The source of each transistor is connected ground and hence, is also at zero volts. Blocking capacitors are present in between the stages to DC isolate the stages from one another (in other words, to prevent the bias voltages of one transistor from influencing the bias voltages of another transistor). Blocking capacitors are also present at the input and output of the LNA circuit to prevent loading of the LNA circuit by external impedances. The bias point of the transistor along with the IMNs, OMNs and the physical dimensions of the connecting microstrip lines between components were used to tune the LNA circuit to obtain the desired performance. All gain and noise figure performance goals were achieved (the gain was greater than 20 dB and the noise figure was less than 2.5 dB across the entire bandwidth). In addition, unconditional stability was achieved as well as an excellent P_{1dB} output power compression point of 18.23 dB. The latter parametric value (of 18.23 dB) results in an excellent dynamic range for each transistor and, hence, for the entire LNA circuit.

INTRODUCTION

A low-noise amplifier (LNA) has been designed to operate across the 10 GHz bandwidth from 20 GHz to 30 GHz. It is comprised of 4 stages, each of which is composed of a six-finger, fifty-micron-width transistor, input and output matching networks, bias feed lines for the drain voltage and the gate voltage and a grounding line connected to a via for the source terminal of the transistor. The LNA circuit was configured for mounting on a 54 mil by 54 mil anachip. The type of transistor (i.e.,

transistor technology) of each stage is a pseudomorphic high-electron-mobility transistor (pHEMT). High-electron mobility transistors (HEMTs) are the best technology choice for making low-noise amplifiers because the electrons are held within a quantum well, away from the lattice atoms, which reduces their shot noise contribution. A pseudomorphic HEMT is utilized because it allows for enhanced transport properties as well as MMIC fabrication on GaAs. (Specifically, a pseudomorphic HEMT is utilized because it uses an extremely thin layer of a different semiconductor material (in this case InGaAs) that is strained to the lattice constant of the surrounding semiconductor material (in this case AlGaAs), making a pseudomorphic layer of InGaAs with the lattice dimensions of AlGaAs. This results in a transistor that has the enhanced transport properties of InGaAs but still allows the MMIC to be fabricated on a GaAs substrate.) Each transistor has a drain bias voltage of three volts and a gate bias voltage of zero volts, with the source port of the transistors at zero volts as well. The drain bias voltage is achieved with a voltage source (of three volts). The gate bias voltage is achieved with a 2000 ohm resistor connected to ground. The gate resistor is divided into two resistors to allow for the appropriate distribution of physical length of the 2000 ohm gate resistor in the vertical and horizontal direction to aid in the fitting and orienting of the LNA circuit on the chip. The source voltage is obtained by direct connection to a via. The bias voltages $V_{DD} = 3$ V and $V_{GG} = 0$ V results in an $I_{DS} = 21.3$ mA, which, hence, is equal to I_{DSS} due to the fact that $V_{GS} = V_{GG} - V_S = 0$ V. This bias point for the transistors was chosen because it offered the best tradeoff between noise and gain performance. Blocking capacitors are present in between the stages to DC isolate the stages from one another (in other words, to prevent the bias voltages of one transistor from influencing the bias voltages of another transistor). Blocking capacitors are also present at the input and output of the LNA circuit to prevent loading of the LNA circuit by external impedances. These blocking capacitors at the input and output of the LNA circuit were combined with the capacitors associated with the matching networks at the input and output of the LNA to economize the design.

The input matching network and output matching network of each stage are comprised of inductors and capacitors. Initial design of the IMNs and OMNs was achieved using the Smith chart. First design iteration of the IMNs was for a Γ_S that provided a gain for the individual transistors of 8.5 dB and a noise figure of 1.0997 dB, and first initial design of the OMNs was for a $\Gamma_L = \Gamma_{OUT}^*$ that matched to a 50 ohm impedance load. The inductance of the inductors and the capacitance of the capacitors of the IMNs and OMNs were then used, along with the bias point of the transistor and the physical dimensions of the connecting microstrip lines between the components, to tune the LNA circuit to obtain the desired performance for gain (S_{21}), the scattering parameters S_{11}, S_{22}, and S_{12}, the Noise Figure and the stability parameters mu1 and mu2.

Plots of the gain of the LNA show that its magnitude is in excess of 20 dB for the 20 GHz to 30 GHz range. Specifically, from 20GHz to 25.16 GHz, its magnitude is predominantly 24.4 dB with a few vacillations of +/- 0.1 dB over a small amount of the bandwidth in this range. From 25.16 GHz to 27.15 GHz the gain monotonically decreases by 1 dB to a value of 23.4 dB at 27.15 GHZ. For the bandwidth from 27.15 GHz to 28.97 GHz, the gain monotonically decreases from 23.4 dB to 21 dB, and for the last 1.03 GHz of bandwidth, monotonically decreases to a value of 20.1 dB at 30 GHz. Thus, for the entire frequency range of 20 GHz to 30 GHz, the gain (S_{21}) always exceeds the lower design value goal of 20 dB.

The other scattering parameters, S_{11}, S_{22} and S_{12}, of the designed LNA also have, like S_{21}, desired magnitudes across the entire 10 GHz bandwidth from 20 GHz to 30 GHz. For the S_{11} parameter, its magnitude value ranges from a minimum magnitude of -31.4 dB to a maximum value of -11.1 dB. This translates into a maximum voltage transmission coefficient of $(1 - 10^{-31.4/10}) = 0.999$ to a minimum voltage transmission coefficient of $(1 - 10^{-11.6/10}) = 0.922$. So, at any time, for voltage signals with frequencies of oscillation between 20 GHz to 30 GHz entering port 1 of the LNA, 92.2 percent to 99.9 percent of the voltage signal is being transmitted and amplified by the LNA. Similar to S_{11}, the S_{22} scattering parameter also has minimal values across the 10 GHz bandwidth. From 22.84 GHz to 30 GHz (77.16 percent of the bandwidth), S_{22} has a magnitude less than or equal to -10.7 dB, with a minimum of -50.3 dB occurring at the design frequency of 25 GHz. For the frequency range 22.64 GHz to 22.84 GHz, the magnitude of S_{22} ranges from -10 dB to -10.7 dB, and from 20 GHz to 22.64 GHz it varies from -6.15 dB to -10 dB. The S_{12} parameter has even lower magnitude values than the S_{11} and S_{22} parameters with a minimum value of -59.7 dB at 20 GHz to a maximum value of -41.8 dB at 30 GHz. These values of S_{12} indicate that there is excellent signal isolation from port 2 to port 1, with only approximately 0.0001 percent to 0.0066 percent of any voltage signal with a frequency between 20 GHz to 30 GHz entering port 2 being transmitted to port 1. Thus the LNA can be modeled and optimized as a unilateral device.

The resulting noise figure of the low-noise amplifier also is of superior value in comparison to that of the design value (of 2.5 dB). From 20 GHz to 23.56 GHz the noise figure monotonically decreases from 1.94 dB to 1.5 dB. Over the next 54.2 percent of the bandwidth, from 23.56 GHz to 28.98 GHz, the noise figure is below a value of 1.5 dB, reaching a minimum of 1.372 dB at 27.03 GHz. For the latter part of the bandwidth, from 28.98 GHz to 30 GHz, the noise figure is at or below 1.648 dB. Hence, at all frequencies the noise figure is at least 0.56 dB below the design value goal of 2.5 dB, and for 54.2 percent of the 10 GHz bandwidth is greater than 1 dB below this value.

The LNA designed also is unconditionally stable across the entire frequency range from 0.5 GHz to 50 GHz. Plots of the mu1 (load side) and mu2 (source side) parameters across the entire bandwidth from 0.5 GHz to 50 GHz for each stage (of the LNA circuit) independently and for all four stages combined (which comprised the complete LNA circuit) show that both parameters are always greater that one. Indeed, stability of the LNA circuit is so solid that neither parameter for the complete LNA circuit ever has a value less than two for the 20 GHz to 30 GHz frequency range. The stability results for each amplifier and stage alone indicated that no resistors, capacitors or inductors were needed to be added specifically for stabilization of any aspect of the LNA circuit.

Excellent linearity is also provided by the LNA. Plots of P_{OUT} versus P_{IN} of the LNA circuit utilizing the TOM3 nonlinear transistor model for each of the four amplifiers in the LNA circuit show that the P_{1dB} output power compression point at the design frequency of 25 GHz is in excess of 18 dBm with a value of 18.22 dBm. The corresponding input power at this 1 dB compression point is -4.943 dBm and the gain is 23.13 dB. (Hence, the gain in the linear region is approximately 24.13 dB when utilizing the TOM3 nonlinear transistor model.)

The noise floor, N_o, associated with the designed LNA, is also of excellent value. Assuming the LNA is utilized in a receiver that is fed with an antenna having a noise temperature of $T_A = 150K$ and has a bandwidth of 100 MHz, and using the gain and noise figure values of the LNA at 25 GHz (G at 25 GHz = 24.4 dB and NF at 25 GHz = 1.431 dB), the resulting calculated noise floor, N_o, associated with the LNA is:

$N_o = GkB[T_A + (F - 1)T_0] = (10^{24.4/10})*(1.38X10^{-23}$ J/K$)*(10^8$ Hz$)*[150K + (10^{1.431/10} - 1)]$
$= 5.71609 \ X \ 10^{-11} = -102.429$ dB $= -72.428$ dBm

For this value of N_o and using the P_{1dB} value of the LNA, the resulting linear dynamic range of the LNA is P_{1dB} - N_o = 18.22 dBm - -72.428 = 90.648 dB, which, like the other LNA parameters, is an excellent value as well.

DESIGN APPROACH, SCHEMATICS AND LAYOUT

For the design of the wideband LNA for the 20 GHz to 30 GHz range, two design approaches were contemplated. The first design algorithm considered focused on creating a single stage LNA that was designed with tradeoff between gain, noise figure, stability and linearity, and then replicating this stage three times to create a four-stage LNA. The process first would be performed using ideal inductors, capacitors, resistors and ideal interconnections (between the parts), and then the parts and

interconnections would be supplanted by TriQuint inductors, capacitors, resistors and microstrip interconnections. TriQuint vias would be utilized for both the ideal and real circuits to provide a ground. Components comprising the input matching and output matching networks as well as the widths and lengths of the microstrip lines providing connection between the inductors, capacitors, resistors and transistors would be varied. Optimization would begin by performing impedance matching between the stages when viewing towards the output of the four-stage LNA starting at the last stage and working towards the first stage. This would then allow for transmission of the power from the input to the output of the LNA without any reflection occurring back to the input of the LNA. Several more iterations on variation of the physical parameters would then be performed to identify key sensitivity points of the circuit and to converge to the desired performance for the LNA.

The second design algorithm contemplated involved designing the first stage of the four-stage LNA for low noise, the second stage with comparable tradeoff between gain and noise, and the latter two stages for gain (since the latter stages contribution to the noise figure of the four-stage LNA is negligible). Like the first design algorithm, components such as inductors and capacitors as well as the widths and lengths of the microstrip lines providing connection between the inductors, capacitors, resistors and transistors would be varied to obtain the desired scattering parameters, noise figure, linearity and stability for the four-stage LNA. Of these two design approaches, the former was utilized since it was perceived that it would provide a good overall averaging between the scattering parameters (including gain), noise figure, stability and linearity for the four-stage LNA.

To begin, the following circuit below was constructed that included a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS)**,** a gate biasing network providing a gate biasing voltage of zero volts, a drain biasing network providing a drain biasing voltage of three volts, input and out put blocking capacitors to prevent loading by external impedances, and a grounding via for the source terminal of the transistor. The TriQuint transistor model utilized was linear and ideal inductors and ideal capacitors as well as TriQuint vias were used for the components of the circuit surrounding the transistor.

Single-Stage LNA using Ideal Elements Without IMN or OMN
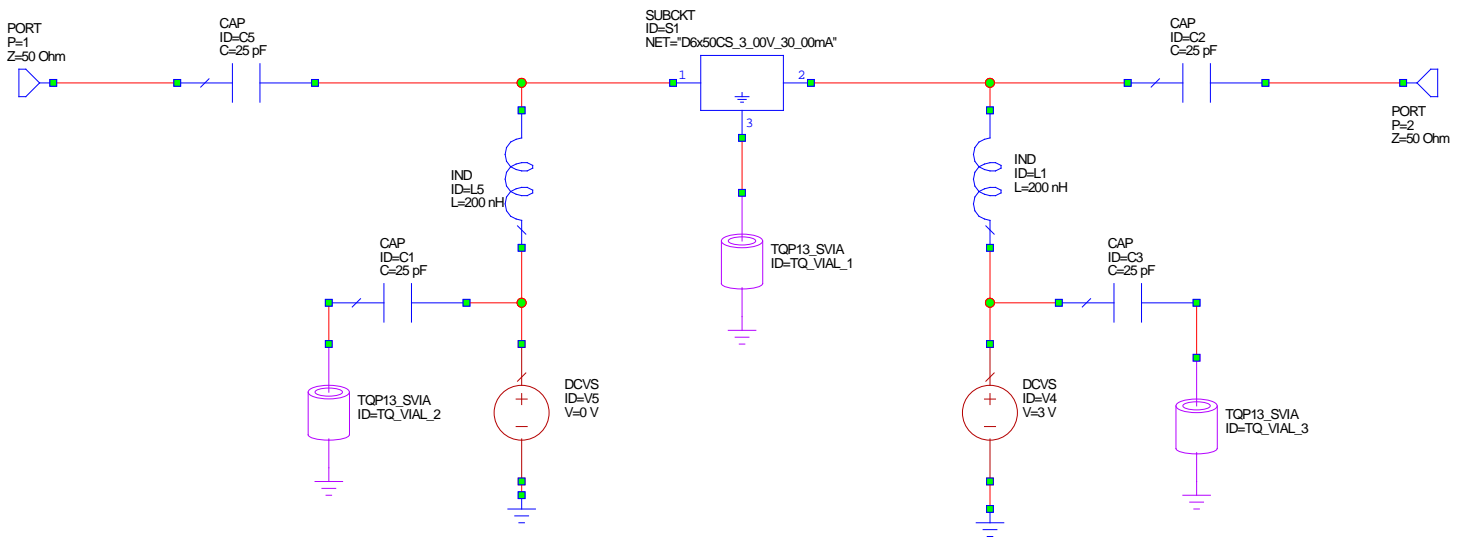
Low Noise Amplifier (LNA) using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at $V_{DS} = 3.0$ Volts and $V_{GS} = 0.0$ Volts. Blocking capacitors are present but no stabilization of the LNA is included and no Input Matching Network (IMN) and no Output Matching Network (OMN) are present. Inductors, capacitors and interconnections are ideal.

The Stability plot of the above circuit is shown below.
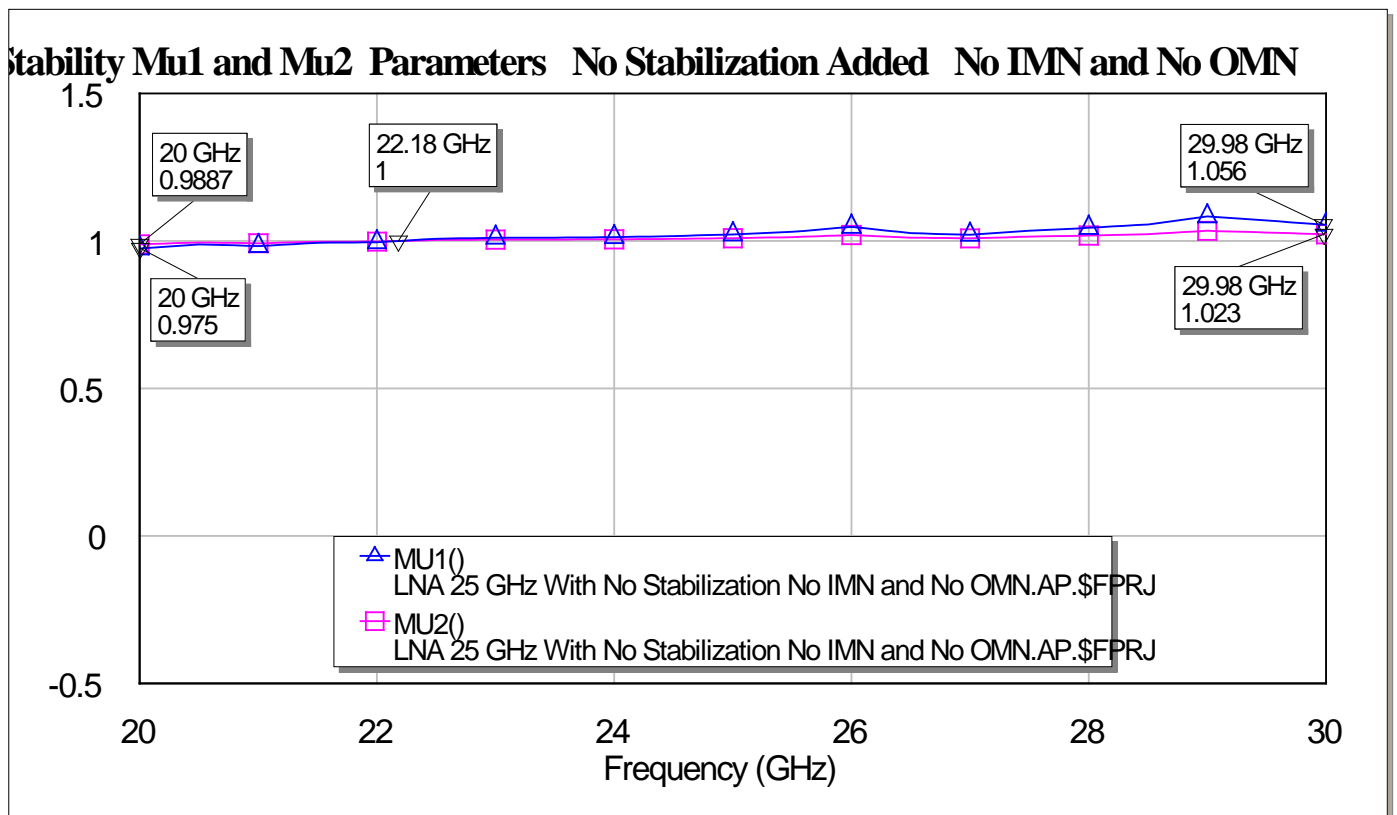
The above stability plot shows that for the 10 GHz frequency bandwidth from 20 GHz to 30 GHz, the LNA without stabilization and without an IMN and OMN is conditionally stable from 20 GHz to 22.18 GHz and is unconditionally stable from 22.18 GHz to out beyond 30 GHz.   Since utilization of real elements from TriQuint will add stability due to attenuation by these parts, it was concluded that no resistors, capacitors or inductors had to be added to this single-stage circuit for stabilization. Note that, if needed, stabilization of the LNA can be achieved by adding a parallel RC circuit on the input of the transistor, inductance on the source port of the transistor, and a series and parallel resistor on the output of the transistor. For the input RC stabilization circuit, the resistor will help stabilize the amplifier at low frequency (the capacitor has a large impedance at low frequency), and the capacitor will help stabilize the circuit at high frequency (the capacitor has a small impedance at high frequency). The inductance on the source port of the transistor will help with stability as well and help provide a compromise (tradeoff) between match (input return loss) and noise figure. The series and parallel resistor on the output (drain) will provide the dominant stability of the LNA circuit. These resistors are located on the output side of the LNA to avoid magnification of thermal noise, since the purpose of the LNA is to provide low-noise amplification. Of these two resistors, the series resistor will provide the main stabilizing affect. However, although small, the parallel resistor will make a stabilizing contribution as well.

The noise and available gain circles of the above single-stage LNA circuit are:
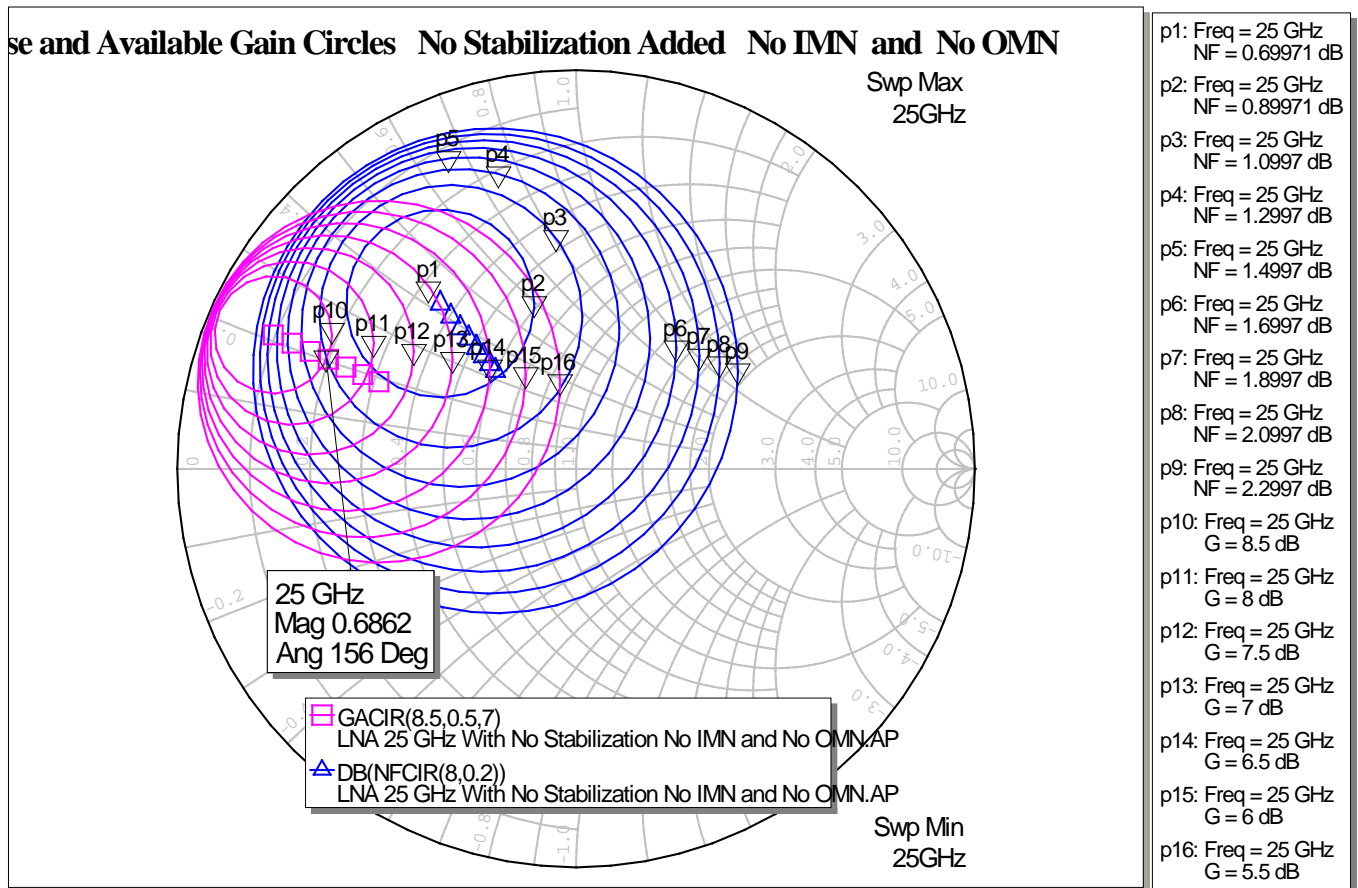
The Γs chosen to match to (via an Input Matching Network of the single-stage LNA) is shown above. It has a magnitude of 0.6862 and a phase angle of 156 degrees. This yields a design point of Noise Figure = 1.0997 dB and Available Gain = 8.5 dB. Utilizing the Smith Chart, one finds that to obtain this design point requires an IMN comprised of a series ideal capacitor of capacitance 0.6775 picofarads and a parallel ideal inductor of inductance 0.1547 nanohenries. Incorporation of this IMN into the LNA above with no stabilization added and no IMN or OMN yields the following circuit:
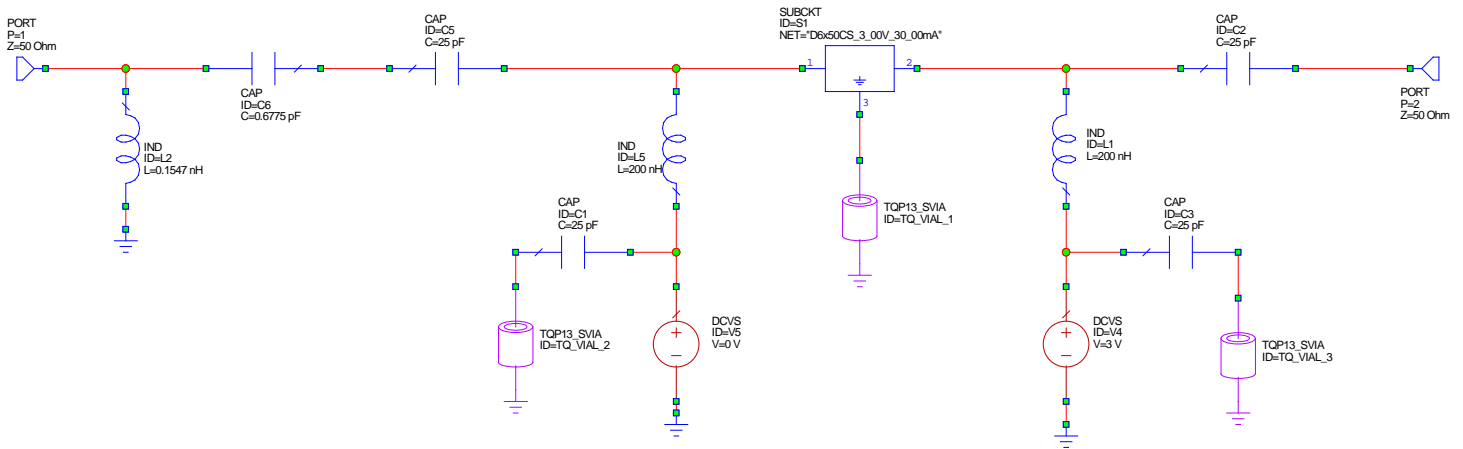
The Stability plot of the above circuit is:
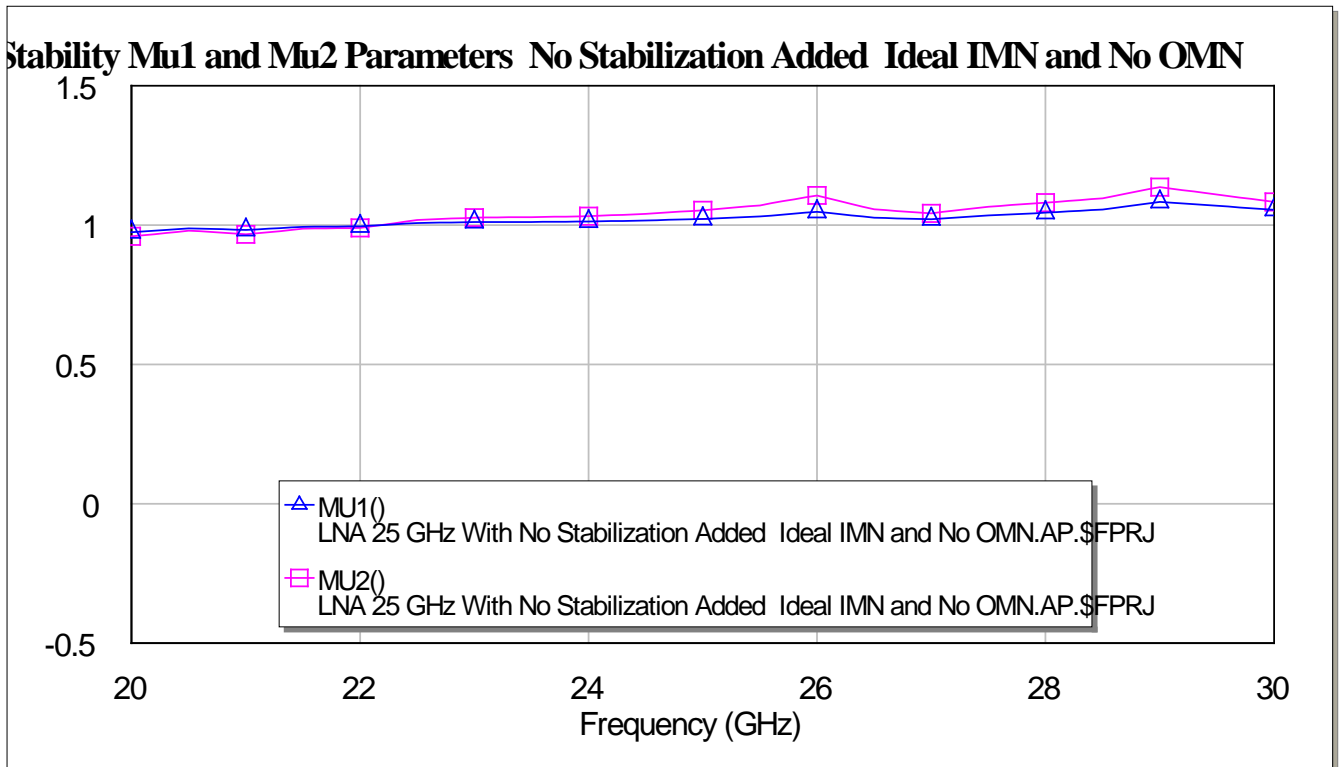
The Noise Figure Circles, Available Gain Circles and the Γ_{OUT} (labeled as S_{22} below) parameter of the above circuit are:

SE AND AVAILABLE GAIN CIRCLES NO STABILIZATION ADDED IDEAL IMN NO OMN

Swp Max
25GHz

25 GHz
Mag 0.01787
Ang -172.4 Deg

25 GHz
Mag 0.5483
Ang -117.4 Deg

GACIR(8.5,0.5,7)
LNA 25 GHz With No Stabilization Added Ideal IMN and No OMN.AP
DB(NFCIR(8,0.2))
LNA 25 GHz With No Stabilization Added Ideal IMN and No OMN.AP
S(2,2)
LNA 25 GHz With No Stabilization Added Ideal IMN and No OMN.AP

p1: Freq = 25 GHz
NF = 0.69971 dB
p2: Freq = 25 GHz
NF = 0.89971 dB
p3: Freq = 25 GHz
NF = 1.0997 dB
p4: Freq = 25 GHz
NF = 1.2997 dB
p5: Freq = 25 GHz
NF = 1.4997 dB
p6: Freq = 25 GHz
NF = 1.6997 dB
p7: Freq = 25 GHz
NF = 1.8997 dB
p8: Freq = 25 GHz
NF = 2.0997 dB
p9: Freq = 25 GHz
NF = 2.2997 dB
p10: Freq = 25 GHz
G = 8.5 dB
p11: Freq = 25 GHz
G = 8 dB
p12: Freq = 25 GHz
G = 7.5 dB
p13: Freq = 25 GHz
G = 7 dB
p14: Freq = 25 GHz
G = 6.5 dB
p15: Freq = 25 GHz
G = 6 dB
p16: Freq = 25 GHz
G = 5.5 dB

Note that the design point of a Noise Figure of 1.0997 dB and a Gain of 8.5 dB is located at the center of the Smith Chart indicating successful design of the ideal-element IMN. The Γ_{OUT} (labeled as S_{22} in the plot) calculated (via simulation) for the LNA circuit with no stabilization added and with the IMN but without the OMN is shown above. It is found to have a magnitude of 0.2417 and a phase angle of -30.32 degrees. Thus, for an LNA, the Γ_L chosen to match to is equal to the conjugate of Γ_{OUT}. Hence, the OMN is designed to match to a reflection coefficient with a magnitude of 0.2417 and a phase angle of +30.32 degrees. Utilizing the Smith Chart, one finds that to obtain this design point requires an OMN comprised of a series inductor of inductance 0.0166 nanohenries and a parallel inductor of inductance 0.2534 nanohenries. Incorporation of this OMN into the single-stage LNA yields the following final design ideal-element single-stage LNA circuit:
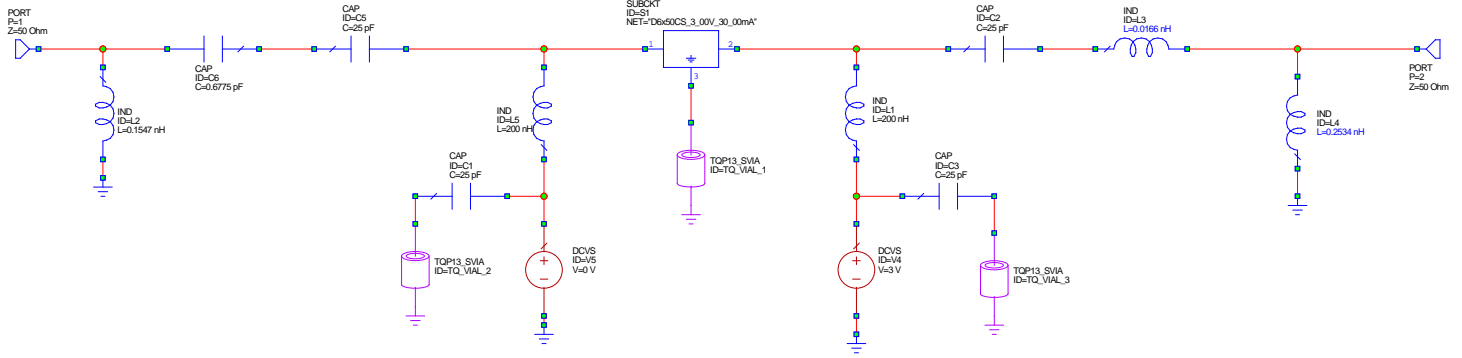
Single-Stage Ideal-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at $V_{DS} = 3.0$ Volts and $V_{GS} = 0.0$ Volts

The Noise Figure Circles, Available Gain Circles and the S_{22} parameter of the above final design of the single-stage LNA comprised of ideal lumped elements for the IMN, OMN and blocking capacitors are:
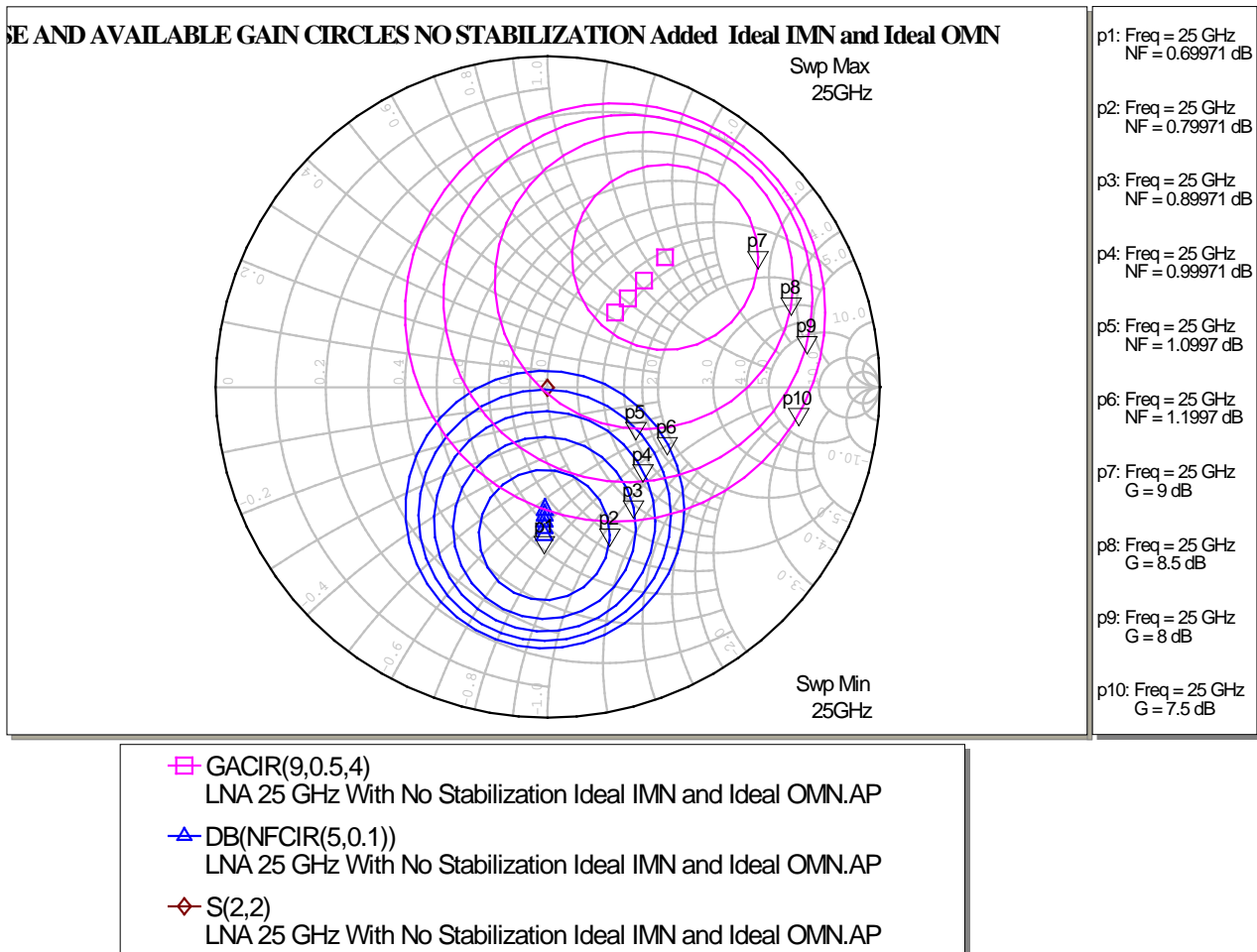
Single-Stage Ideal-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts Noise Figure Circles, Available Gain Circles and S_{22} Parameter Point

Note that the design point of a Noise Figure of 1.0997 dB and a Gain of 8.5 dB as well as the S_{22} parameter of the single-stage LNA circuit are located at the center of the Smith Chart indicating successful design. The scattering parameter plot of the above ideal-element single-stage LNA is shown below as well as the Minimum Noise Figure/Noise Figure and the Stability (Mu1 and Mu2) plot.
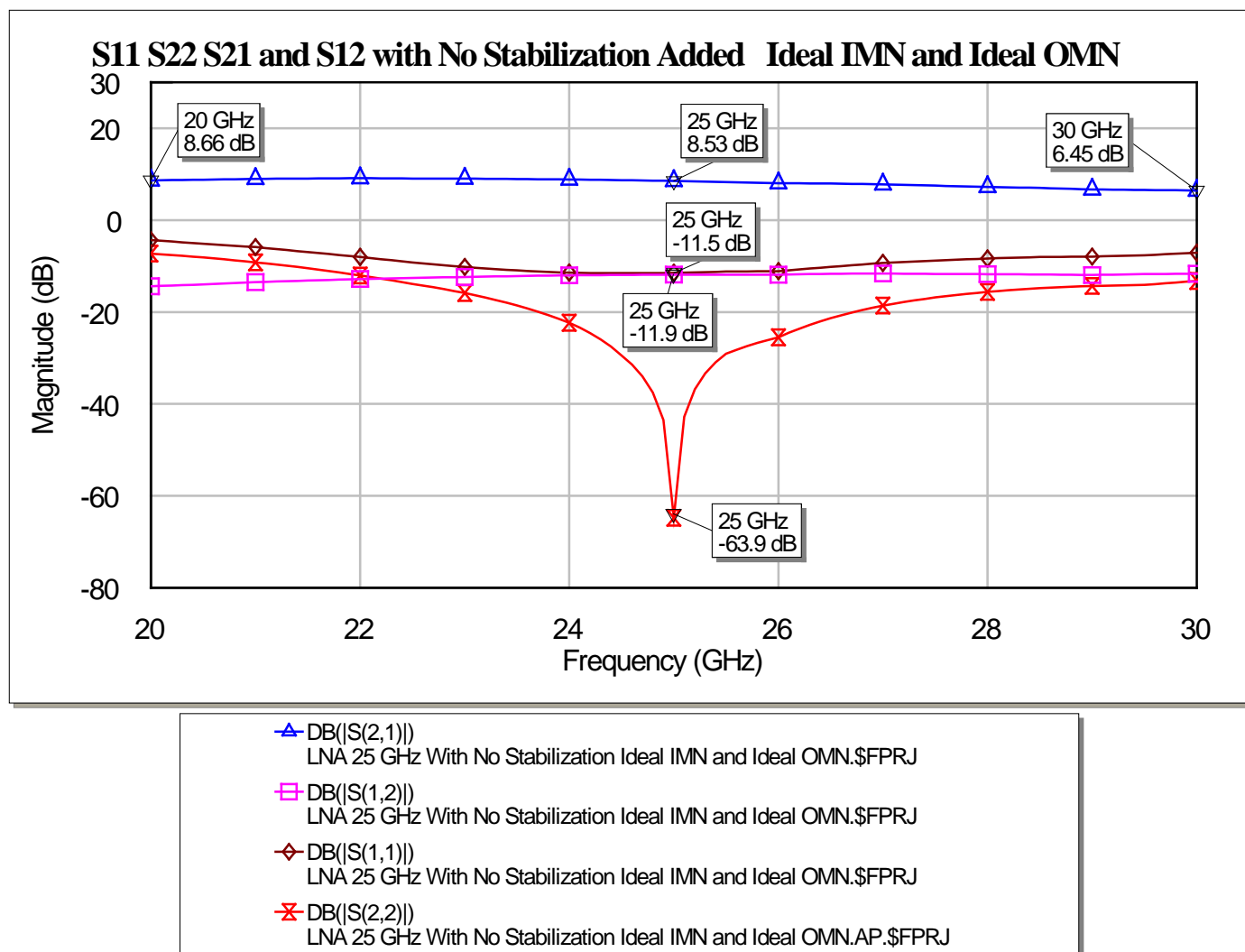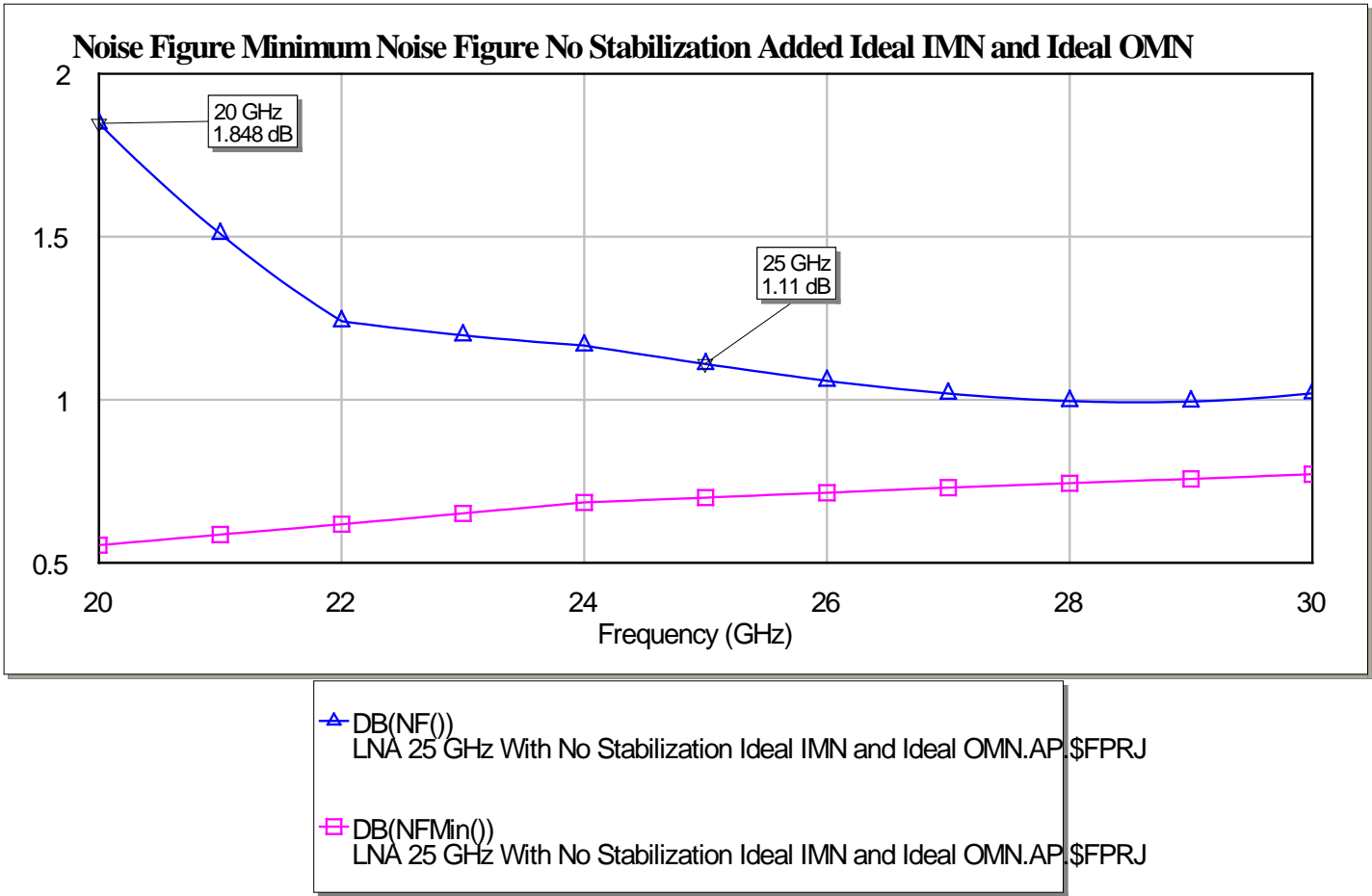

Single-Stage Ideal-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts S-Parameters. Note that the S_{21} parameter (Gain) indicates that the LNA system needs to be multi-stage to meet the design requirement of Gain > 20 dB.

Noise Figure Minimum Noise Figure No Stabilization Added Ideal IMN and Ideal OMN

20 GHz
1.848 dB

25 GHz
1.11 dB

Frequency (GHz)

△ DB(NF())
LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ

□ DB(NFMin())
LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ

Minimum Noise Figure and Noise Figure Plots for the Single-Stage Ideal-Element LNA that utilizes a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts. Note that the design goal of maximum Noise Figure of 2.5 dB is being satisfied by the single-stage LNA.

Stability Mu Parameters No Stabilization Added Ideal IMN and Ideal OMN

Legend:
- MU1() — LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ
- MU2() — LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ

Annotations on plot:
- 20 GHz 0.9601
- 20 GHz 0.9169
- 22.18 GHz 1
- 30 GHz 1.166
- 30 GHz 1.084
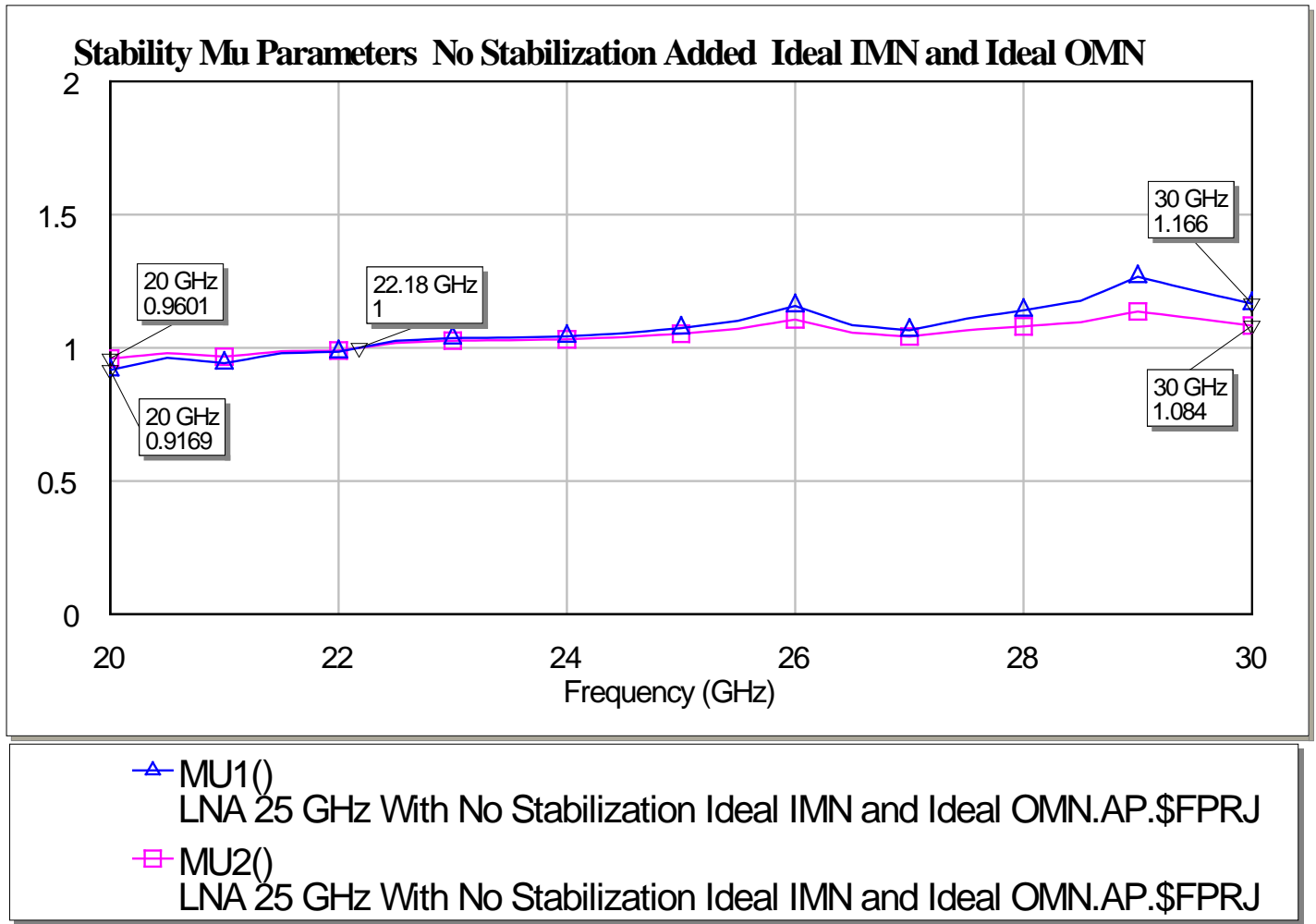
Mu1 and Mu2 Stability Parameters for the Single-Stage Ideal-Element LNA that utilizes a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and $V_{GS}$ = 0.0 Volts. Note that the single-stage LNA is conditionally stable from 20 GHZ to 22.18 GHz and is unconditionally stable from 22.18 GHz to 30 GHz and beyond.

This single-stage LNA was then replicated for a two-stage, three-stage and four-stage ideal-element LNA using (as for the single-stage LNA) a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts. Optimization of the ideal components was performed for each design step.
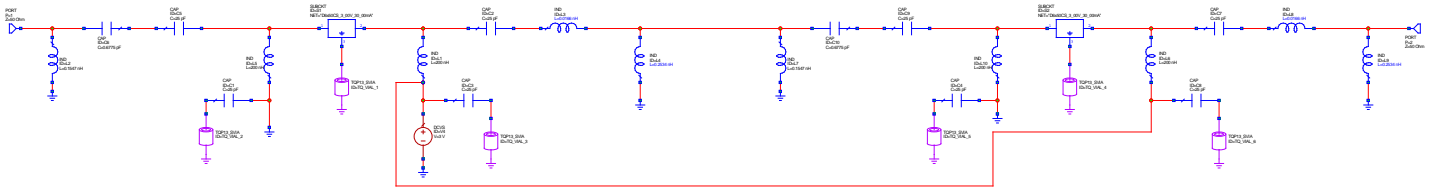
Double-Stage Ideal-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts
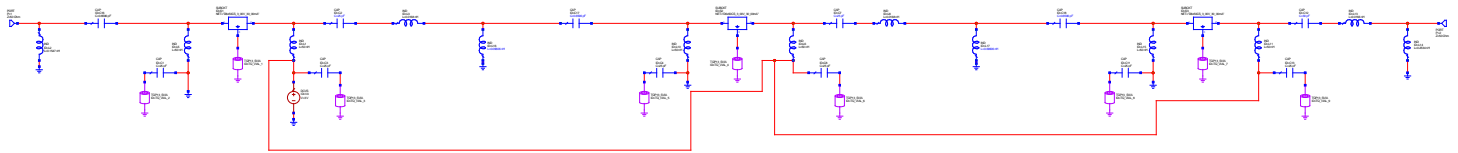
Triple-Stage Ideal-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts
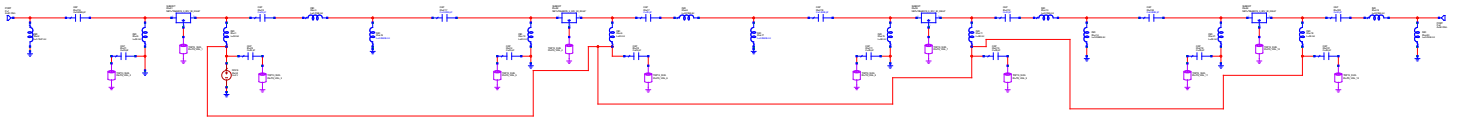
Quadruple-Stage Ideal-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts

For the Quadruple-stage ideal-element LNA above, the following S-parameter, Noise Figure/Minimum Noise Figure and Stability Plots were obtained for the optimized circuit.

S11 S22 S21 and S12   Quad   No Stabilization Added   Ideal IMN and Ideal OMN

Legend:
- DB(|S(2,1)|)
  Quad LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.$FPRJ
- DB(|S(1,2)|)
  Quad LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.$FPRJ
- DB(|S(1,1)|)
  Quad LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.$FPRJ
- DB(|S(2,2)|)
  Quad LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ

S-Parameter plot of the Quadruple-Stage Ideal-Element LNA that uses a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) b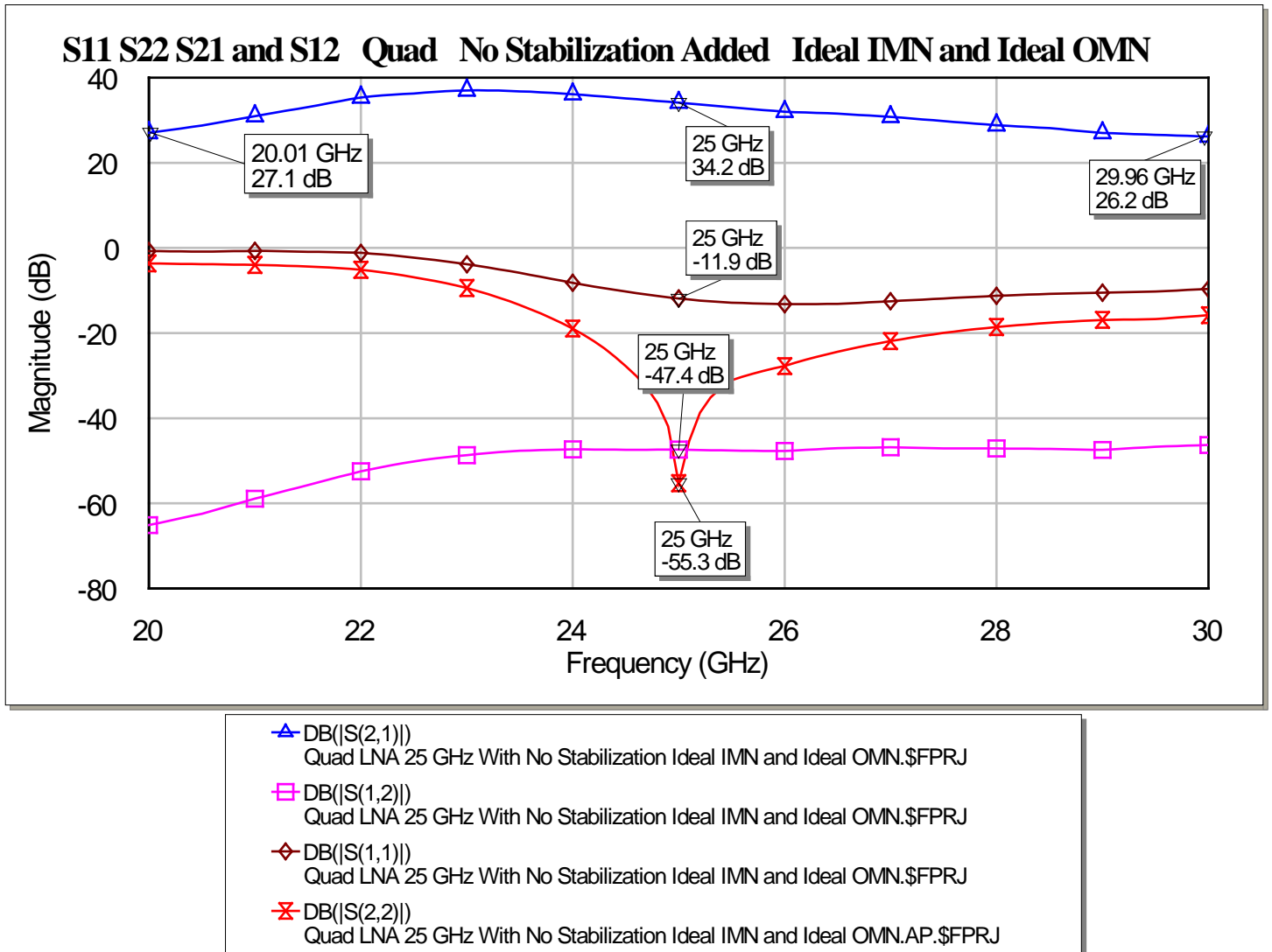iased at $V_{DS} = 3.0$ Volts and $V_{GS} = 0.0$ Volts for each stage. Note that the S_{21} parameter (Gain) indicates that the four-stage LNA system comprised of ideal elements does meet the design requirement of Gain > 20 dB.

Noise Figure Minimum Noise Figure Quad No Stab Added Ideal IMN Ideal OMN

20 GHz
2.357 dB

25 GHz
1.268 dB

Frequency (GHz)

DB(NF())
Quad LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ
DB(NFMin())
Quad LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ
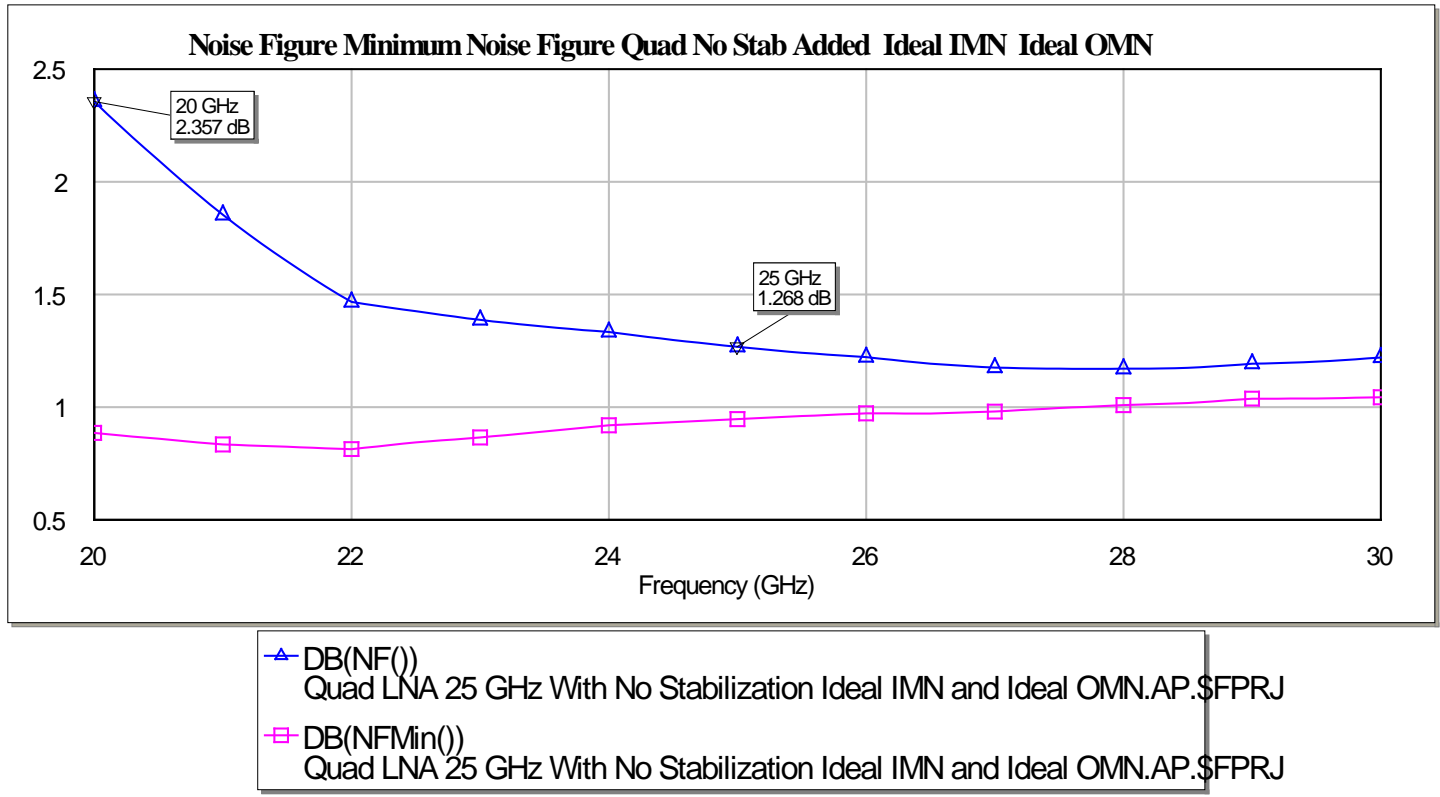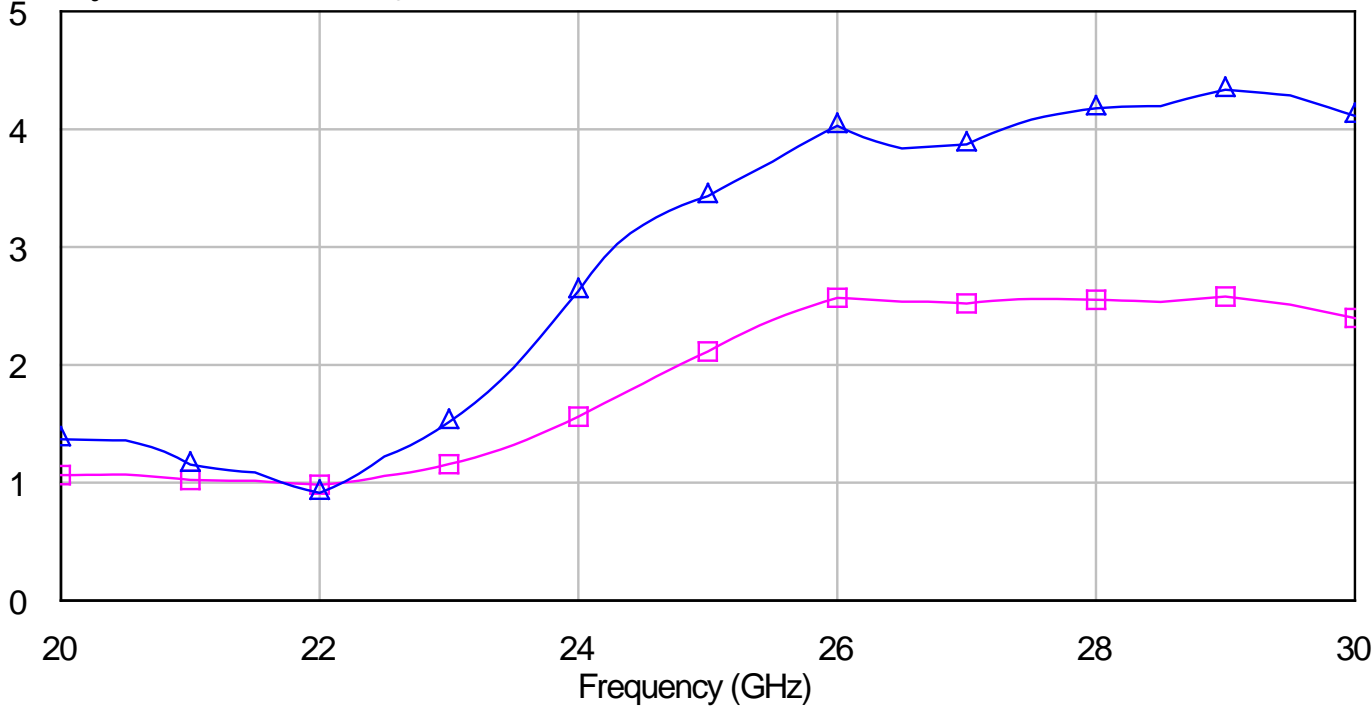
Minimum Noise Figure and Noise Figure Plots for the Quadruple-Stage Ideal-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts. Note that the design goal of a maximum Noise Figure of 2.5 dB is being satisfied by the Quadruple-stage LNA comprised of ideal elements.

Stability Mu Parameters Quad No Stabilization Added Ideal IMN and Ideal OMN

Legend:

— MU1()
Quad LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ

— MU2()
Quad LNA 25 GHz With No Stabilization Ideal IMN and Ideal OMN.AP.$FPRJ

Stability parameters Mu1 and Mu2 for the Quadruple-Stage Ideal-Element LNA that utilizes a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at $V_{DS} = 3.0$ Volts and $V_{GS} = 0.0$ Volts for each stage. Note that the Quadruple-stage LNA comprised of ideal elements is unconditionally stable for the entire 10 GHz bandwidth, except for around 22 GHz (where it is conditionally stable). Note, also, that substitution of real elements and connections will make this circuit unconditionally stable for the entire 10 GHz bandwidth and beyond.

The next step in the design process was the replacement of the ideal elements with TriQuint elements in the Quadruple-stage LNA circuit. This resulted in the circuit shown below.
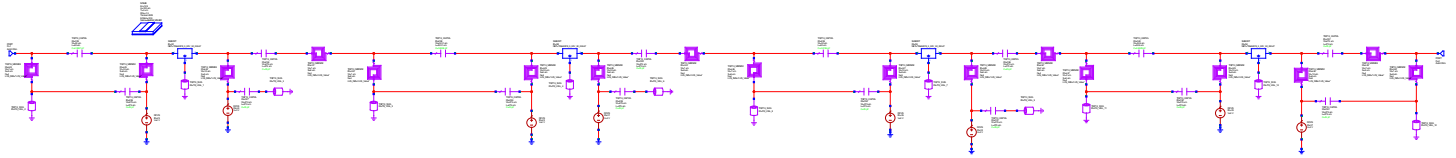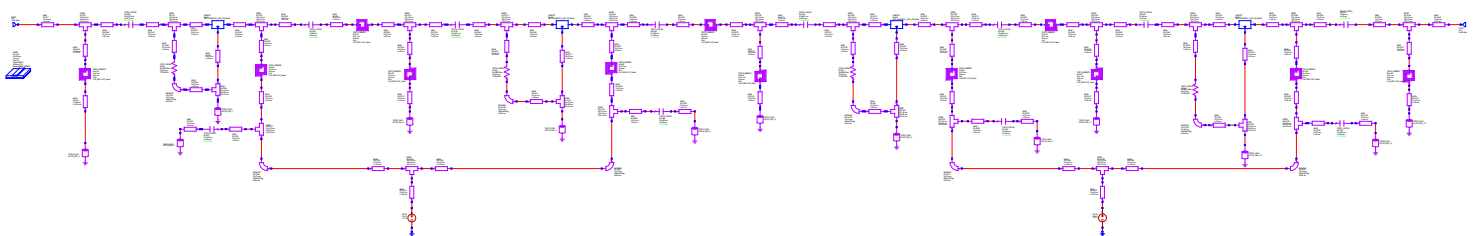
Quadruple-Stage Real-Element (Ideal interconnections) LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at $V_{DS} = 3.0$ Volts and $V_{GS} = 0.0$ Volts.

The inductors and capacitors were all re-optimized to meet and/or exceed the design goals of the project. The re-optimization of the Quadruple-stage LNA was necessary due to the parasitic capacitance and resistance associated with each inductor, and the parasitic inductance and resistance associated with each capacitor. Once this was accomplished, microstrip line connections replaced the ideal interconnections between the components. The value of the substrate parameters utilized was:

Substrate Characteristics

ε_r = Relative Dielectric Constant = 12.9
H = Substrate Thickness = 100 microns
T = Conductor Thickness = 4 microns
ρ = Metal Bulk Resistivity Normalized to Gold
Tand = Loss Tangent of Dielectric = 0.0005

With TriQuint microstrip line connections, the above Quadrple-stage LNA circuit became:

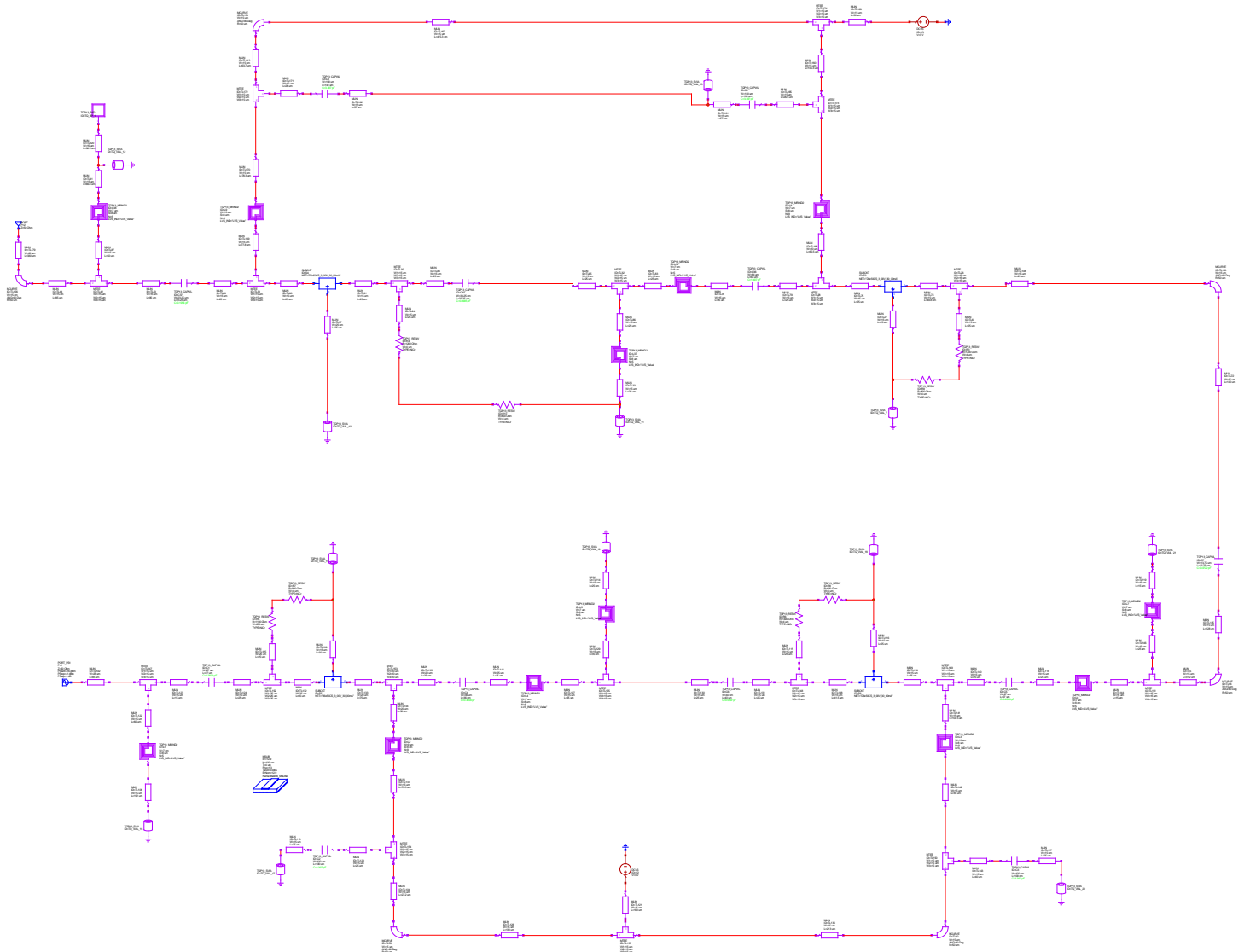## Quadruple-Stage TriQuint-Element LNA laid out linearly that utilizes a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at $V_{DS} = 3.0$ Volts and $V_{GS} = 0.0$ Volts

Note that bias gate voltage source of 0.0 volts was replaced with a 2000 ohm resistor connected to ground, and the first- and second-stage drain bias voltage source of 3.0 volts is shared as well as the third- and fourth-

stage drain bias voltage source. Again, the circuit was re-optimized to meet and/or exceed the design goals of the project.

The final step in the design process was to reshape the circuit such that it would fit onto a 54-mil by 54-mil anachip. To that end, the above circuit was reshaped to the circuit below.

Quadruple-Stage TriQuint-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts

Note that the above circuit did have to be re-optimized due to the reshaping, resizing and the addition of extra microstrip connection line between stages two and three. Also, a smaller HEMT device that has a lower noise figure could have been utilized (particularly for the first and second stage of the LNA since theory shows that the first few stages are dominant in determining the noise figure of the device), but data available indicated that the smaller devices had a larger input impedance requiring a larger magnitude Γ over the entire

bandwidth. Using a slightly larger device size of 50µm allowed for successfully achieving a matching circuit for minimum noise figure over the entire bandwidth from 20 GHz to 30 GHz.

The nonlinear version of the circuit above, with the TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS) linear model supplanted by the TOM3 nonlinear model, is shown below. For this circuit, $V_{GS} = 0.0$ Volts, $V_{DS} = 2.98$ Volts and $I_{DS} = 21.3$ milliamps for each amplifier.
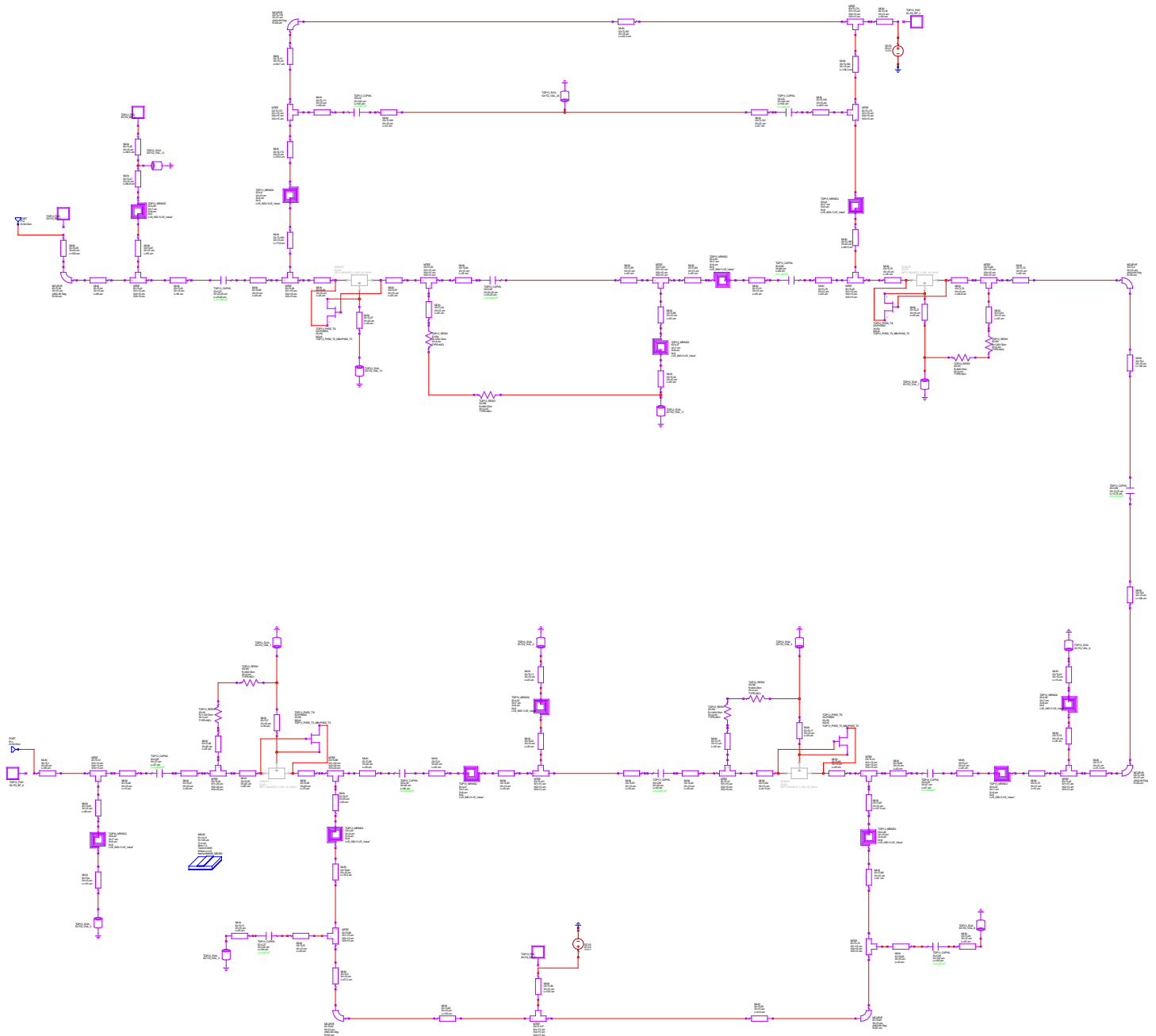
Quadruple-Stage TriQuint-Element LNA using the TOM3 nonlinear model biased at

$V_{DS} = 3.0$ Volts, $V_{GS} = 0.0$ Volts and $I_{DS} = 21.3$ milliamps
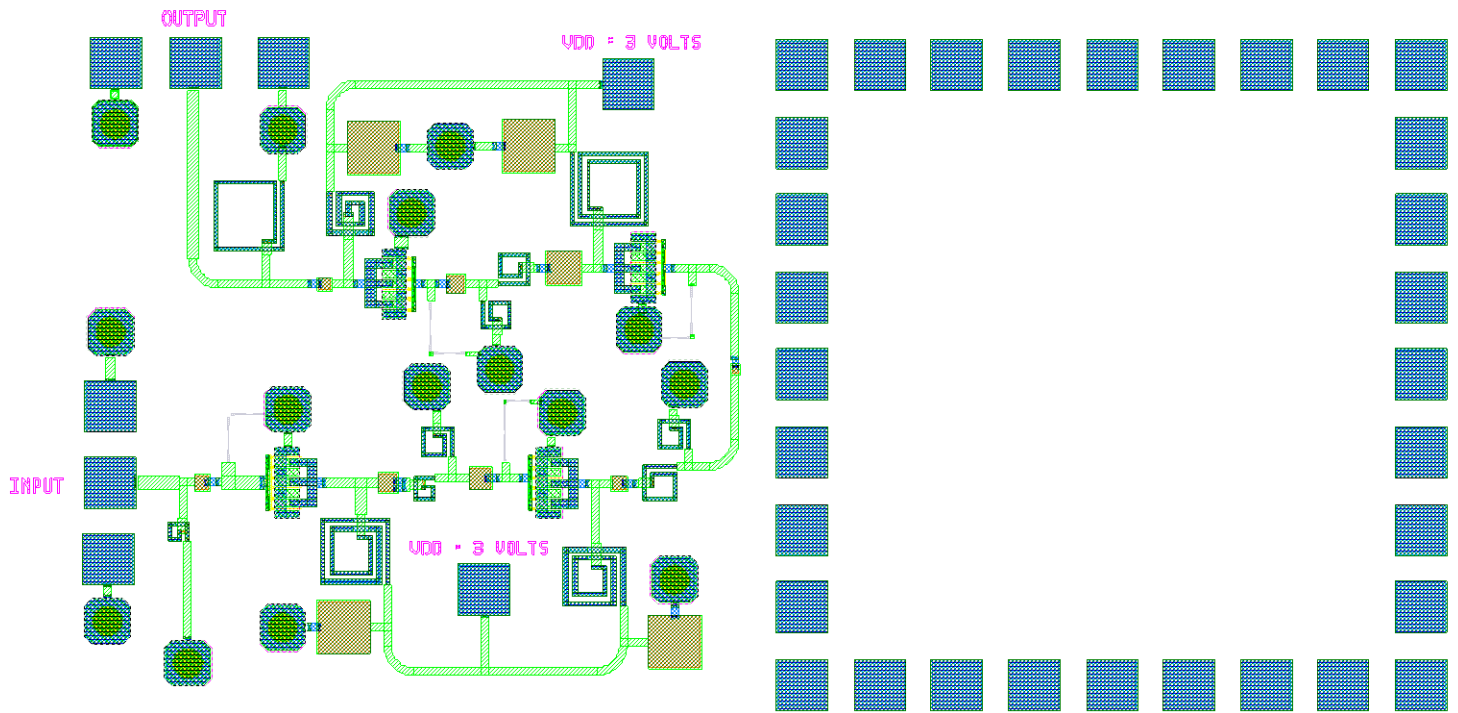
2-D Layout View of the Quadruple-Stage TriQuint-Element LNA in which the TOM3 nonlinear model is used biased at V_{DS} = 2.98 Volts, V_{GS} = 0.0 Volts and I_{DS} = 21.3 milliamps
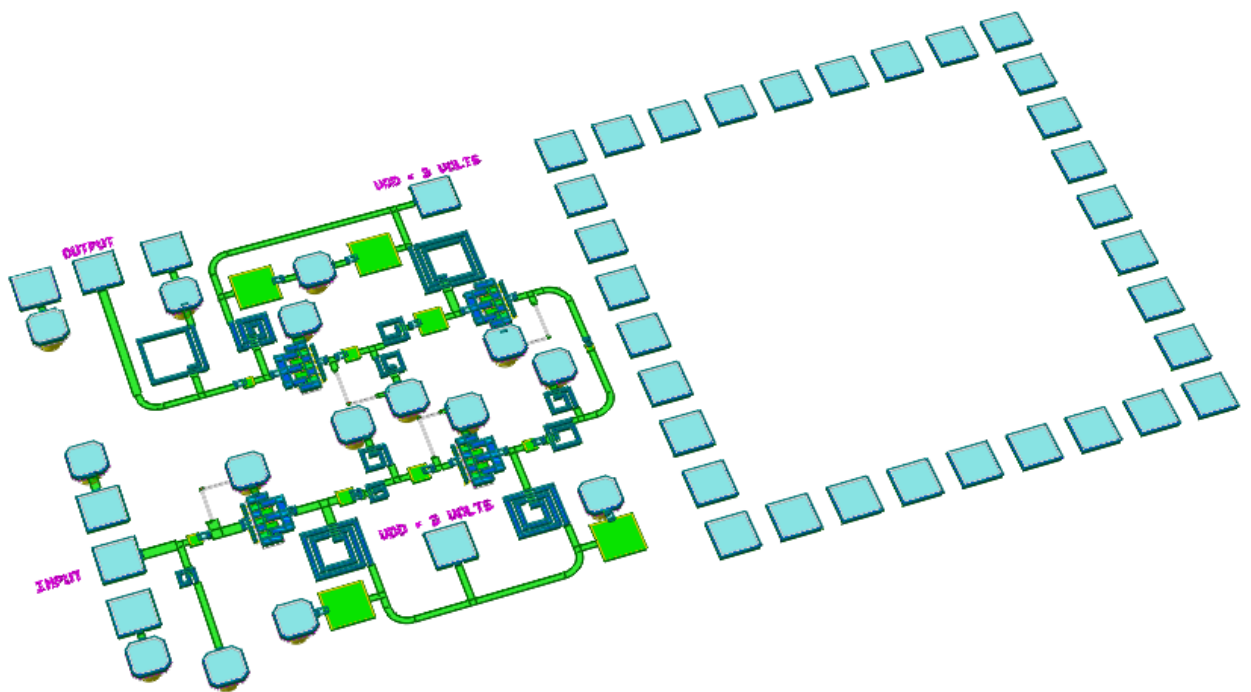
3-D Layout View of the Quadruple-Stage TriQuint-Element LNA in which the TOM3 nonlinear model is used biased at V_{DS} = 2.98 Volts, V_{GS} = 0.0 Volts and I_{DS} = 21.3 milliamps

SIMULATIONS

The S-Parameter simulation of the final quadruple-stage LNA circuit (using TriQuint's Linear Transistor model) is:
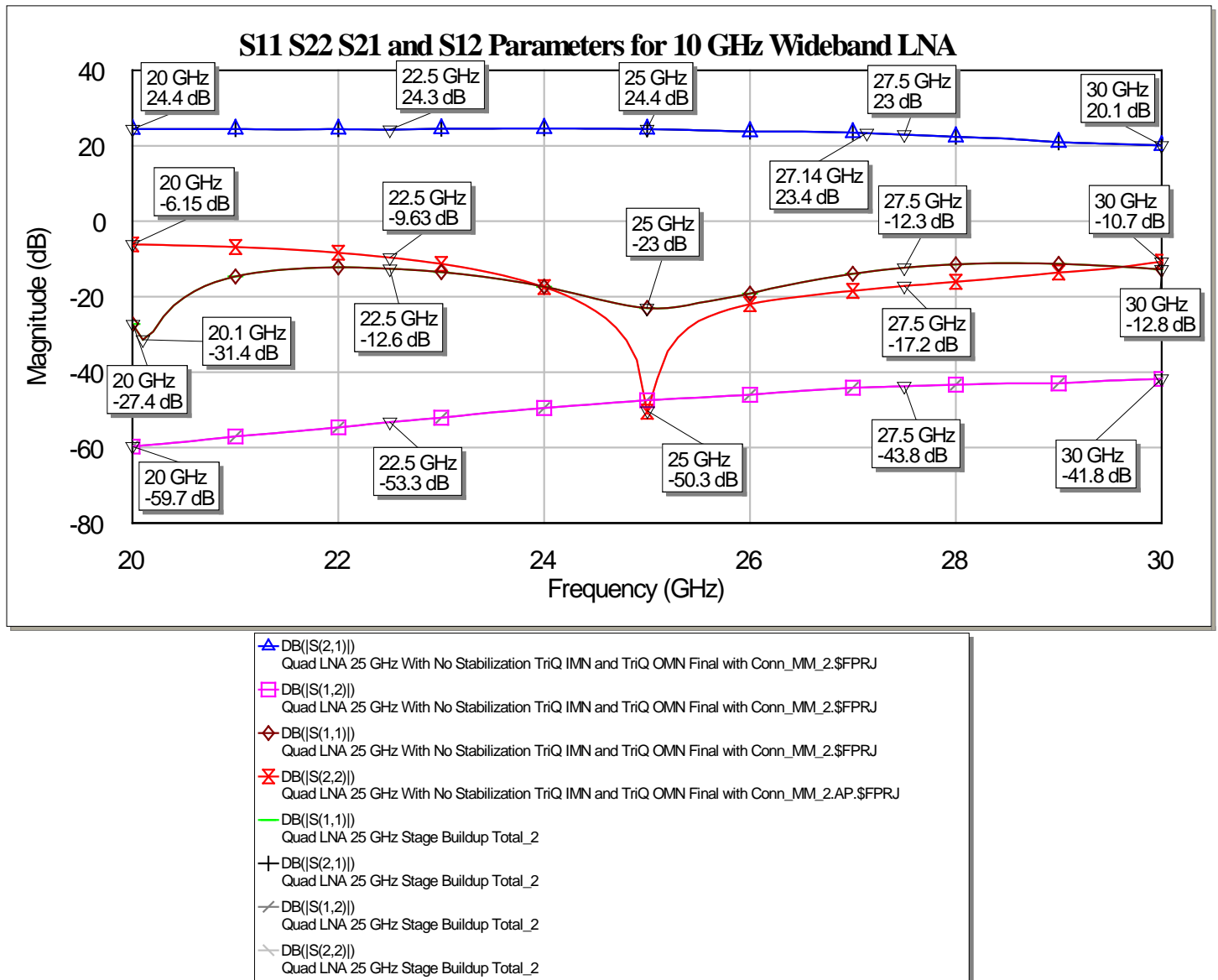
S-Parameters from 20 GHz to 30 GHz of the Quadruple-Stage TriQuint-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts

S11 S22 S21 and S12 Parameters for 10 GHz Wideband LNA 05 GHz to 50 GHz
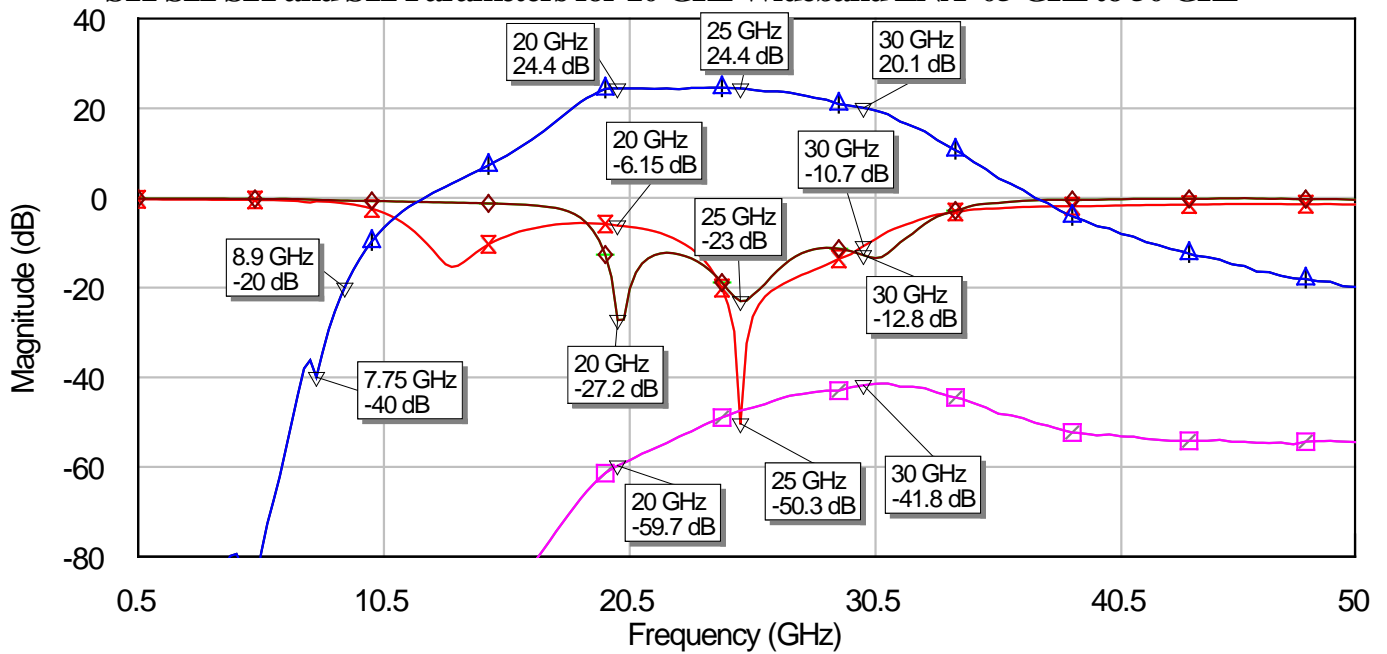
Legend:
- DB(|S(2,1)|) — Quad LNA 25 GHz With No Stabilization TriQ IMN and TriQ OMN Final with Conn_MM_2.$FPRJ
- DB(|S(1,2)|) — Quad LNA 25 GHz With No Stabilization TriQ IMN and TriQ OMN Final with Conn_MM_2.$FPRJ
- DB(|S(1,1)|) — Quad LNA 25 GHz With No Stabilization TriQ IMN and TriQ OMN Final with Conn_MM_2.$FPRJ
- DB(|S(2,2)|) — Quad LNA 25 GHz With No Stabilization TriQ IMN and TriQ OMN Final with Conn_MM_2.AP.$FPRJ
- DB(|S(1,1)|) — Quad LNA 25 GHz Stage Buildup Total_2
- DB(|S(2,1)|) — Quad LNA 25 GHz Stage Buildup Total_2
- DB(|S(1,2)|) — Quad LNA 25 GHz Stage Buildup Total_2
- DB(|S(2,2)|) — Quad LNA 25 GHz Stage Buildup Total_2

S-Parameters from 0.5 GHz to 50 GHz of the Quadruple-Stage TriQuint-Element LNA using a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at $V_{DS} = 3.0$ Volts and $V_{GS} = 0.0$ Volts

Noise Figure and Minimum Noise Figure from 20 GHz to 30 GHz of the Quadruple-Stage TriQuint-Element LNA utilizing a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts

Stability Mu Parameters for 10 GHz Wideband LNA
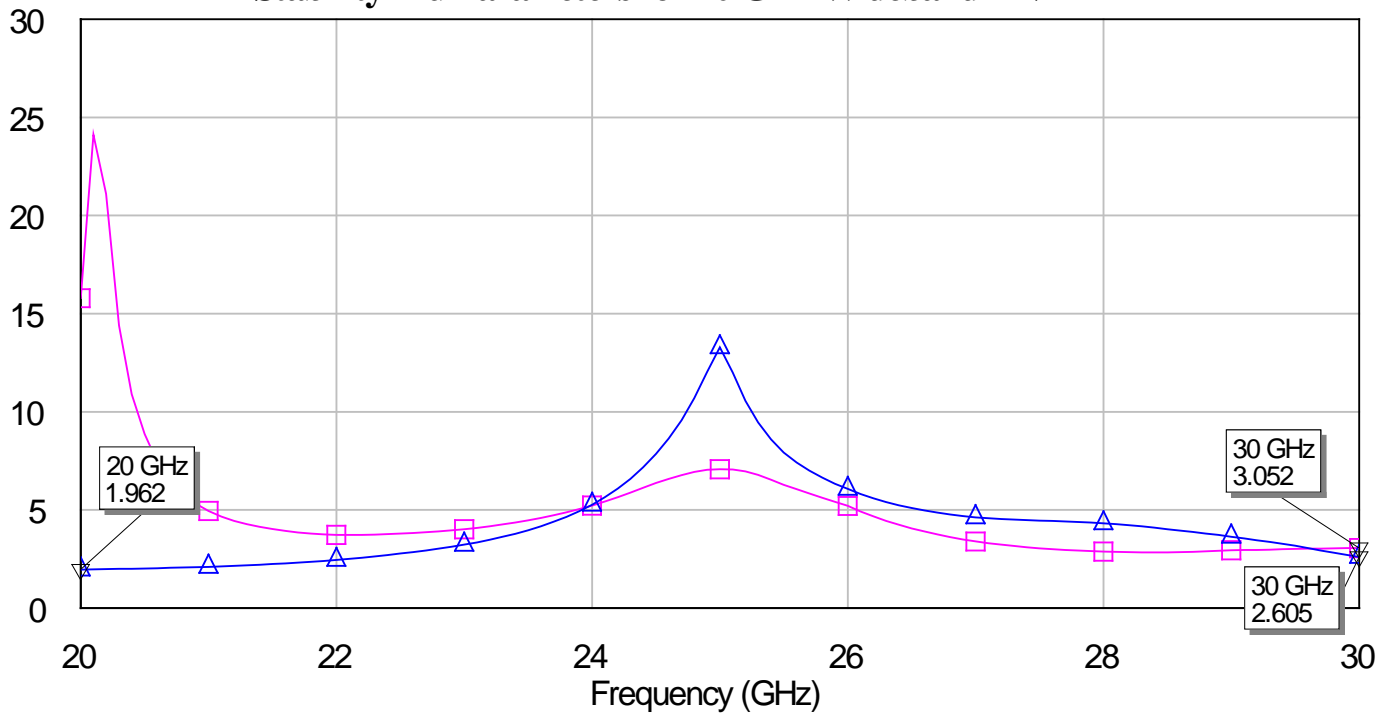
Legend:
- MU1() — Quad LNA 25 GHz Stage Buildup Total_2.AP.$FPRJ
- MU2() — Quad LNA 25 GHz Stage Buildup Total_2.AP.$FPRJ

Data callouts:
- 20 GHz 1.962
- 30 GHz 3.052
- 30 GHz 2.605

X-axis: Frequency (GHz)

Stability Parameters Mu1 and Mu2 from 20 GHz to 30 GHz of the Quadruple-Stage TriQuint-Element LNA utilizing a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) biased at $V_{DS} = 3.0$ Volts and $V_{GS} = 0.0$ Volts
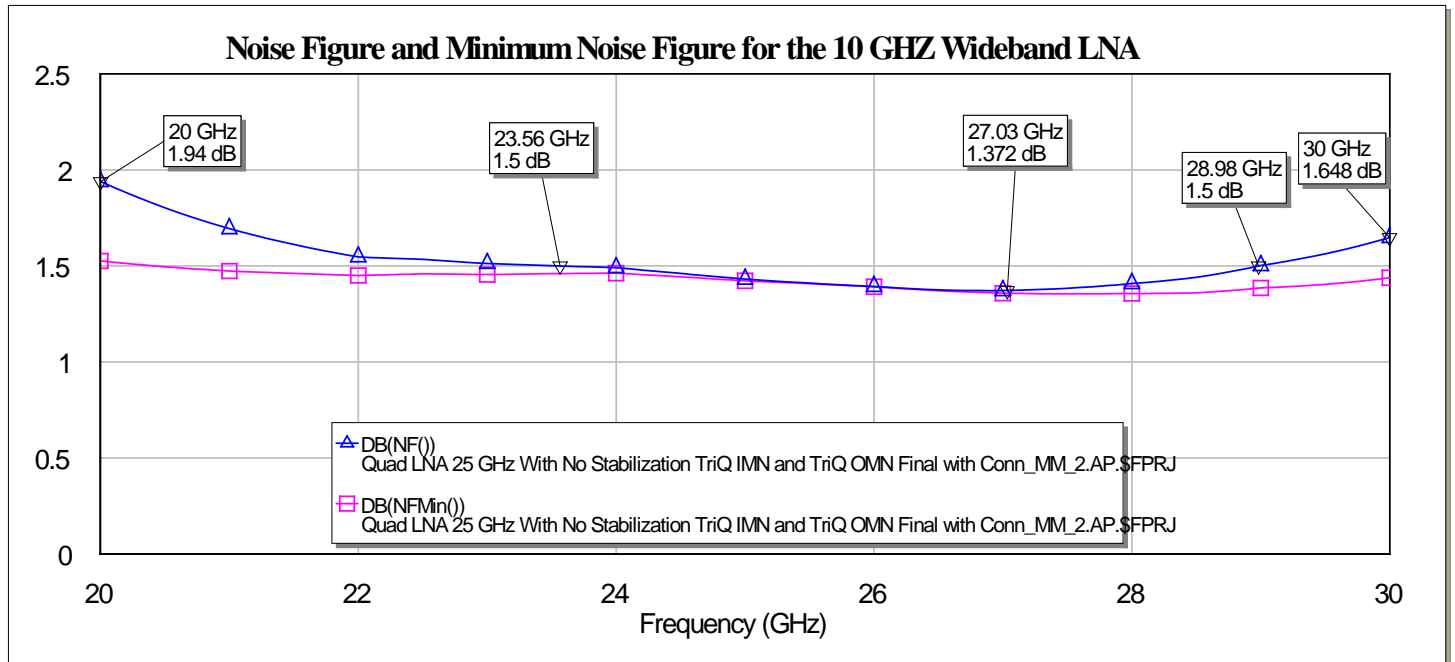
Stability Parameters Mu1 and Mu2 from 0.5 GHz to 50 GHz of the Quadruple-Stage TriQuint-Element LNAusing a TriQuint 6X50 0.13 micron PHEMT

(TPQ13 PHSS linear model) biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts
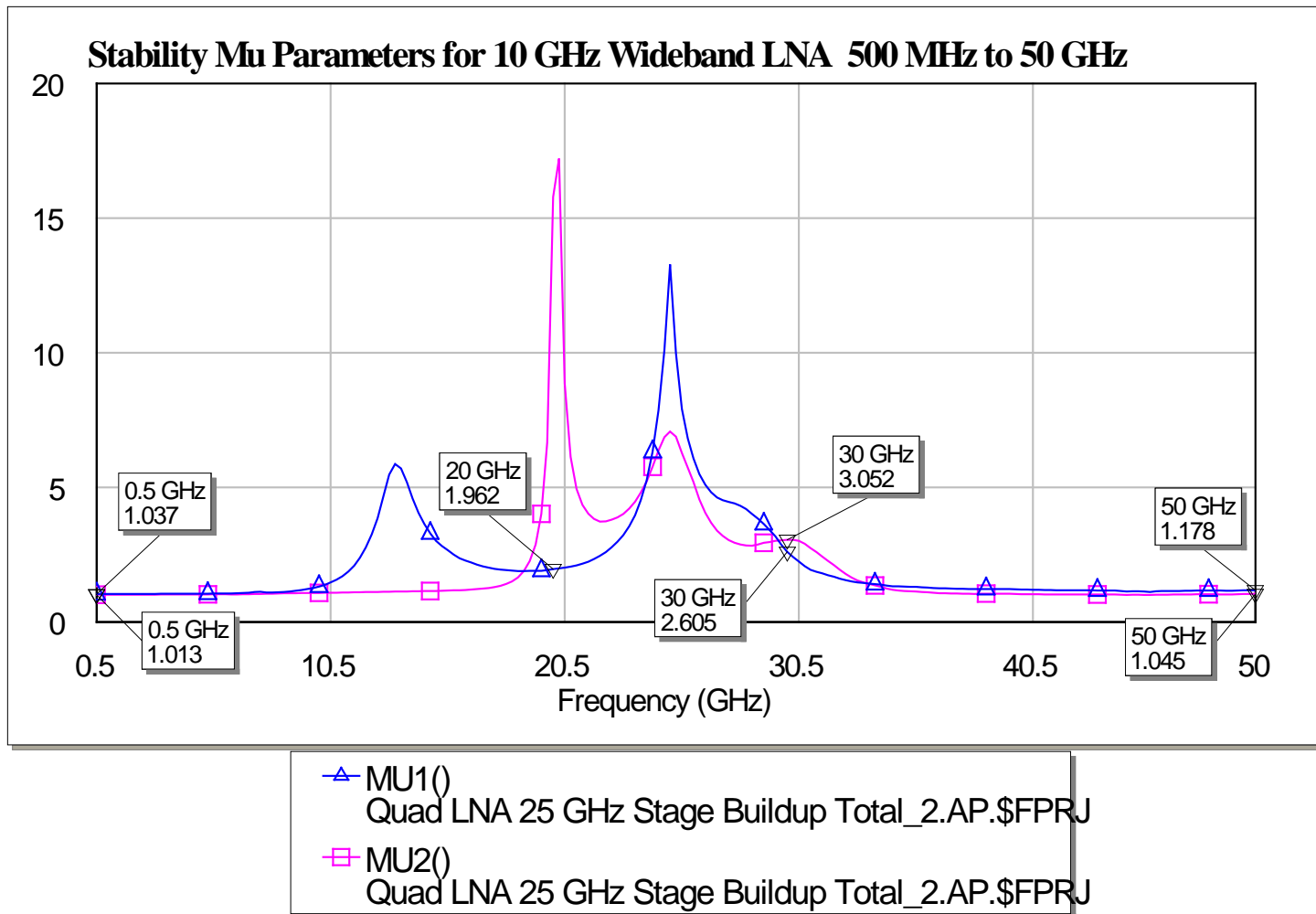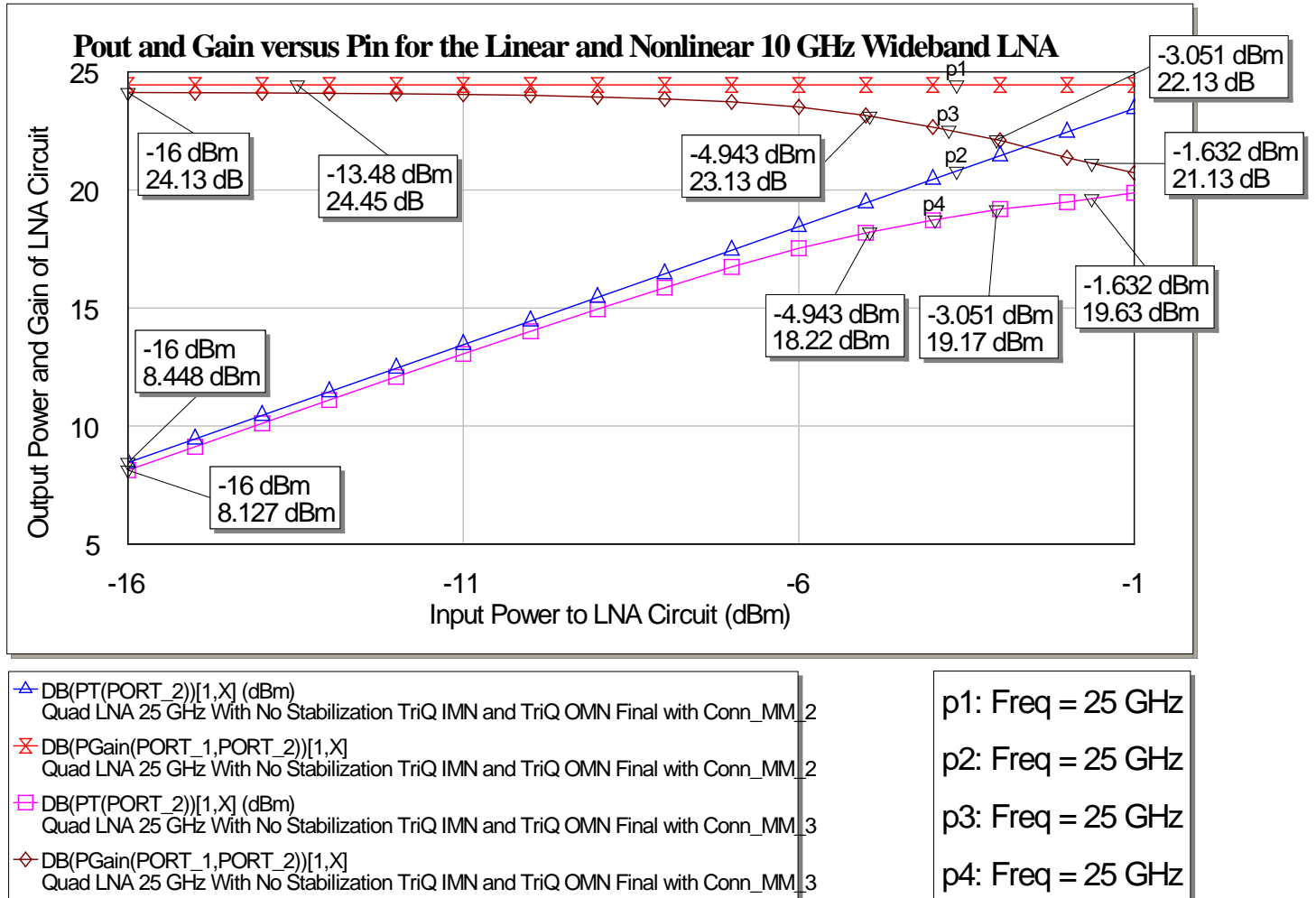
P_OUT and Gain versus P_IN for the Quadruple-Stage TriQuint-Element LNA utilizing a TriQuint 6X50 0.13 micron PHEMT (TPQ13 PHSS linear model) and the TOM3 nonlinear model biased at V_{DS} = 3.0 Volts and V_{GS} = 0.0 Volts

TEST PLAN

The LNA circuit designed will be experimentally tested after fabrication. The scattering parameters will be measured using a network analyzer and the noise figure will be obtained using a noise figure analyzer. (If the lab lacks a noise figure analyzer, a spectrum analyzer can be utilized with the appropriate software and controller, or the network analyzer can be used with a tuner and appropriate software.) The scattering parameters and the noise figure will be measured over the frequency range 20 GHz to 30 GHz. In addition, a plot of P_{OUT} versus P_{IN} will be obtained using a spectrum analyzer as the input power is varied from -16 dBm to -1 dBm in increments of 1 dB for an input signal of 25 GHz.

SUMMARY AND CONCLUSIONS

A successful design was conceived for a low-noise amplifier operating in the frequency range from 20 GHz to 30 GHz. The LNA circuit designed was comprised of four transistors with accompanying inductors, capacitors and resistors. The entire circuit had a length and width that were each less than 54 mils allowing it to be mounted on a 54 mil by 54 mil anachip. The total DC power required of the LNA circuit was a minimal value of 253.9 milliwatts. In addition to achieving small size, low weight and low DC input power requirements, the gain goal of a magnitude greater than 20 dB and the noise figure goal of less than 2.5 dB were both definitively achieved, with the gain nearly constant for the majority of the 10 GHz operating frequency bandwidth. The gain of the LNA was a constant 24.4 +/- 0.1 dB from 20 GHz to 25.16 GHz before slightly reducing at the higher frequencies. From 25.16 GHz to 27.14 GHz the gain smoothly decreased by 1 dB from 24.4 dB to 23.4 dB, and then slightly decreased further by 0.4 dB to 23 dB at 27.5 GHz, ending at a value of 20.1 dB at the upper boundary of the operating frequency range (30 GHz). Thus, for over 51 percent of the bandwidth the gain was within a constant value of 24.4 dB by 0.1 dB, and for over 71 percent of the bandwidth the gain was within 1dB ranging from 24.4 dB to 23.4 dB.

The noise figure of the conceived LNA design, like the gain, also had excellent values across the entire 10 GHz operating bandwidth from 20 GHz to 30 GHz. The maximum value of the noise figure, which occurred at a frequency of 20 GHz, was 1.94 dB, well below the maximum allowable value of 2.5 dB. From 20 GHz to 27.03 GHz, where the minimum noise figure occurred (having a value of 1.372 dB), the noise figure steadily decreased. Beyond 27.03 GHz, the noise figure monotonically increased, but only slightly (less than 0.3 dB), ending with an excellent value of 1.648 dB at 30 GHz. Thus, at all frequency points along the bandwidth from 20 GHz to 30 GHz, the noise figure was well below the upper bound noise figure value of 2.5 dB.

In addition to excellent gain and noise figure values, the LNA circuit was also found to have excellent stability. For the 10 GHz bandwidth from 20 GHz to 30 GHz, both mu1 and mu2 stability parameters were found to always have a value greater than 1.96. Indeed, even for the larger frequency range from 0.5 GHz to 50.0 GHz, both mu1 and mu2 never went below 1.02, indicating unconditional stability for the entire 49.5 GHz bandwidth investigated. Note that for frequencies below 8.9 GHz, the value of the stability parameters was of minimal concern since the gain dropped off precipitously to values well below -20 dB.

Excellent linearity of the LNA circuit was also successfully achieved. Plots of P_{OUT} versus P_{IN} of the LNA circuit utilizing the TOM3 nonlinear transistor model for each of the four amplifiers in the LNA circuit show that the P_{1dB} output power compression point at the design frequency of 25 GHz was in excess of 18 dBm with a value of

18.22 dBm. The corresponding input power at this 1 dB compression point was -4.943 dBm and the gain is 23.13 dB. (Hence, the gain in the linear region was approximately 24.13 dB when utilizing the TOM3 nonlinear transistor model for simulation.)

In designing this LNA circuit, the fundamental algorithm to which the design process converged to involved designing the IMN and OMN to obtain the desired gain and noise figure for each stage independently, interfacing the stages, and then adjusting the lengths of the interconnections to allow for the circuit to be mounted on the 54 mil by 54 mil anachip, and varying the inductor and capacitor values and the widths of some of the interconnections to obtain the desired performance. As predicted by theory, the components closest to the input port had the largest affect on the noise figure, while those located near the output port had virtually no affect on the LNA noise figure, with strength of affect of the in-between components tapering off from input location to output location. The gain of the LNA circuit was equally affected at all power flow locations in the LNA circuit, with local variation occurring depending on whether the component was located along the power flow path or on a circuit branch connected to this path. Hence, optimization to obtain the desired noise figure and gain for the complete LNA circuit involved (primarily) adjusting component values of the first two stages to obtain the desired noise figure value and adjustment of the component values of the final two stages to obtain the desired gain values.

MMIC EE787 Final Project

VCO

C. Reese Jones

12/13/2012

Abstract

This paper describes the design of a voltage controlled oscillator (VCO) for use in the Ka-band. It has been designed to operate at a nominal center frequency of 30 GHz and will be built using Triquint's TQP13 Gallium Arsenide process.

During simulation, it has been shown to oscillate at 30 GHz with a tuning range of 100 MHz.

Introduction

At its most fundamental level, oscillators convert DC power to AC power. For this reason, they are commonly utilized as a source of RF and microwave signals in radar and communication systems. Frequently oscillators are designed as voltage controlled oscillators (VCO's), which allow the oscillation frequency to be tuned by an external voltage.

High frequency VCO's are often designed using MMIC transistors. They tend to be limited to lower output powers and are dominated by the type of resonator used. In practice, MMIC oscillator design consists of three parts: resonator, gain section, and load.

For this project, a voltage controlled oscillator has been designed to operate at a nominal center frequency of 30 GHz

The VCO was designed and simulated using elements from Triquint's TQP13 Library. A layout was then created for Triquint's TQP13 GaAs process and submitted for fabrication.

Design Approach

Specifications vs. Goals

The most difficult part about this design is getting the circuit to oscillate at 30 GHz. Previous designs used in this course utilized a source-connected feedback resistor on a common-source transistor; this design, however, reaches it's theoretical limits around 24 GHz. To achieve oscillation at 30 GHz, a different design approach was implemented using a source-connected feedback capacitor. Based on this topology, higher frequencies are attainable; thus, the primary goal of this project was to achieve oscillation at 30 GHz using the capacitor feedback topology.

In addition, a tuning range of +/- 100 MHz is desired. MMIC oscillators tend to be limited to low output powers, so a design that achieves greater than 0 dBm power would also be considered a success

Tradeoffs

As mentioned above, MMIC oscillators tend to be limited to low output powers. So, to achieve an oscillation frequency of 30 GHz, the output power level will be sacrificed. Typically, a buffer amplifier or power amplifier would be used at the output of the VCO to compensate; however, adding additional gain stages is beyond the scope of this project.
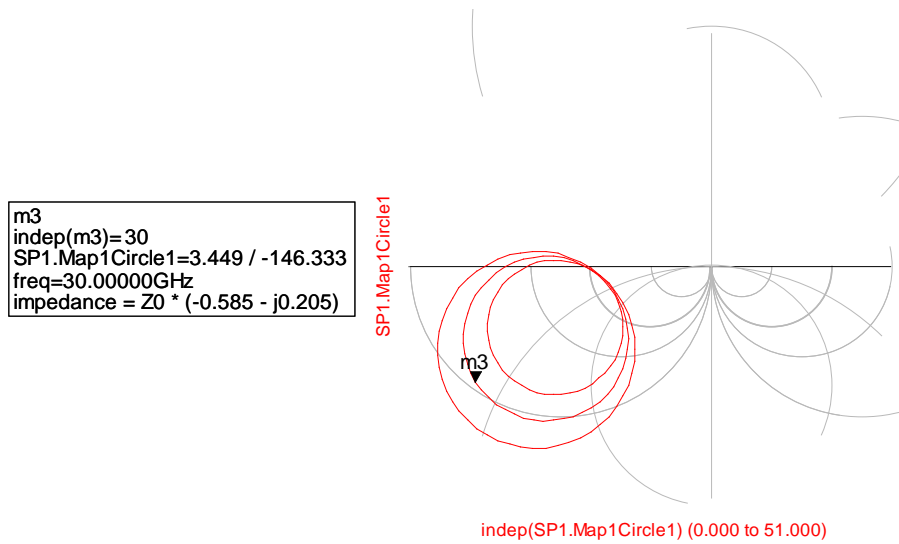
Design

In practice, MMIC oscillator design consists of three parts: a resonator, a gain section, and a load. Furthermore, when utilizing a transistor in the oscillator, the properties of negative resistance must also be taken into account. This design will effectively create a one-port negative-resistance network (resonator and gain section) by terminating an unstable transistor with an impedance (load) designed to drive the device in an unstable region.
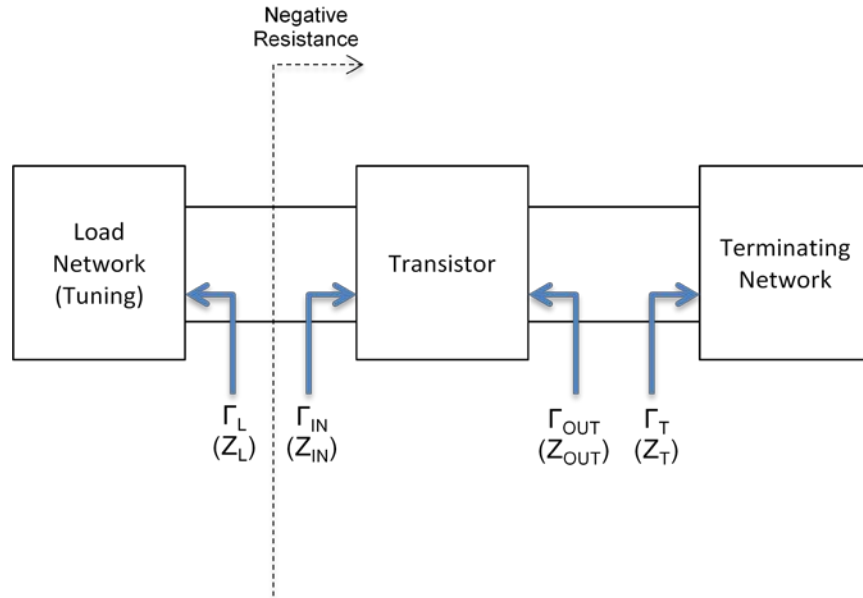
Figure 1. Transistor circuit for a two-port oscillator circuit.

A common-source FET topology was chosen for use in this design. To enhance the instability of the device a feedback capacitor was connected to the source terminal of the transistor. The value of the capacitor was chosen to maximize the input reflection coefficient as seen at the gate

Using a feature of ADS's simulation package - called Map1Circle - the available terminations at port 2 of the transistor were mapped onto port 1. This allows for the designer to maximize the input reflection coefficient (as seen at the gate) based on available impedance terminations at the load of the transistor. It is also important to be mindful that you are not only trying to maximize the magnitude of the input reflection coefficient, but that you are also trying to maximize the negative resistance of the input – in order to aid in startup and steady state oscillation requirements. Figure 2 below illustrates the results of a Map1Circle plot; here you can see the maximum input reflection coefficient magnitude (based on available terminating networks) is ~3.5.

m3
indep(m3)= 30
SP1.Map1Circle1=3.449 / -146.333
freq=30.00000GHz
impedance = Z0 * (-0.585 - j0.205)

SP1.Map1Circle1

m3

indep(SP1.Map1Circle1) (0.000 to 51.000)

Figure 2. Map1Circle plot illustrating maximum input reflecion coefficient based on available terminating networks on port 2.

Once the feedback capacitor value has been set to maximize the input reflection coefficient, the load termination required to achieve this input impedance can be determined.

$$\Gamma_T = \frac{\Gamma_{IN} - s_{11}}{s_{12} * s_{21} + (s_{22} * \Gamma_{IN} - s_{11} * s_{22})}$$

Now that the input impedance has been set (based on the terminating network of the transistor), the load impedance can be chosen to match the input impedance.

$$Z_L = \frac{-R_{IN}}{3} - jX_{IN}$$

It is important to remember, the negative resistance of the transistor will become less negative as the power builds up, so typically the load resistance is chosen to be 1/3 of the input resistance. In addition the reactive part of the load impedance is chosen to resonate the circuit, so it is chosen as the negative of the input reactance.

Simulations

Linear

The complete VCO design using the Triquint TQP13 elements was simulated using Agilent's ADS software. Figure 3, below, shows the output reflection (s_{11}) magnitude and phase; these plots illustrate the output is significantly greater than unity and the phase response crosses zero at the operating frequency of 30 GHz. Figure 4 shows the same output reflection plots across a much wider band.
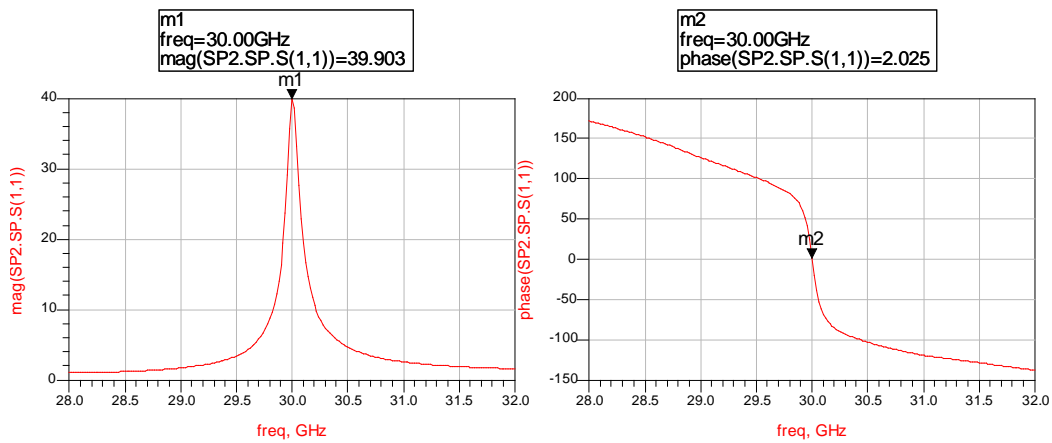

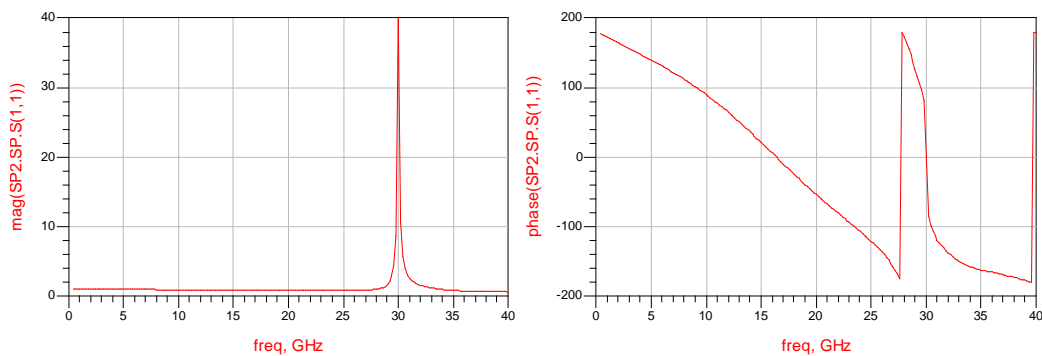**Figure 3.** Output reflection magnitude and phase

Figure 4. Output reflection magnitude and phase across entire frequency spectrum

Now that we have shown the design works at the nominal frequency of 30 GHz, the design was simulated while sweeping the tune voltage from -0.4 V to +0.4 V. Figure 5 below illustrates the results of sweepin the tune voltage.
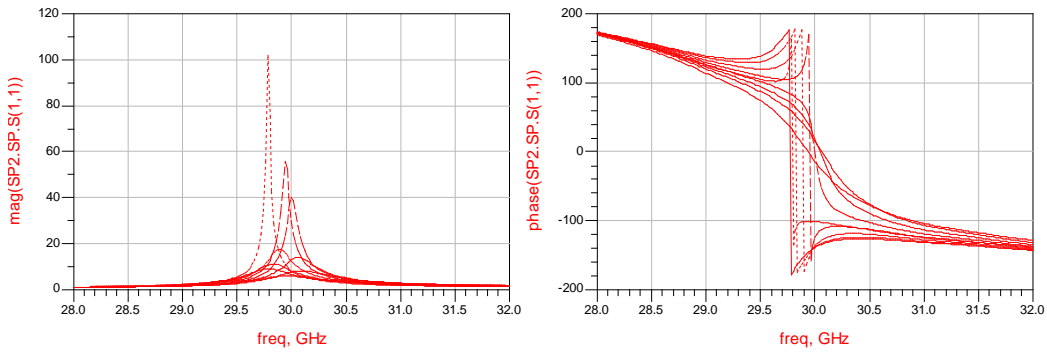

Figure 5. Output reflection magnitude and phase while sweeping tune voltage from -0.4 V to +0.4 V

Bias (DC Analysis)

A plot of I_D vs. V_{DS} for various values of V_{GS} is shown in Figure 6 below. The transistor bias conditions were chosed to provide ~30 mA of drain current during operation. This value was chosen based on the linear simulation file being used – which was biased at 3V and 30 mA.

m4
indep(m4)=3.500
plot_vs(I_Probe2.i, Vdd)=0.029
Vgg=0.050000

Vgg=0.100
Vgg=0.075
Vgg=0.050
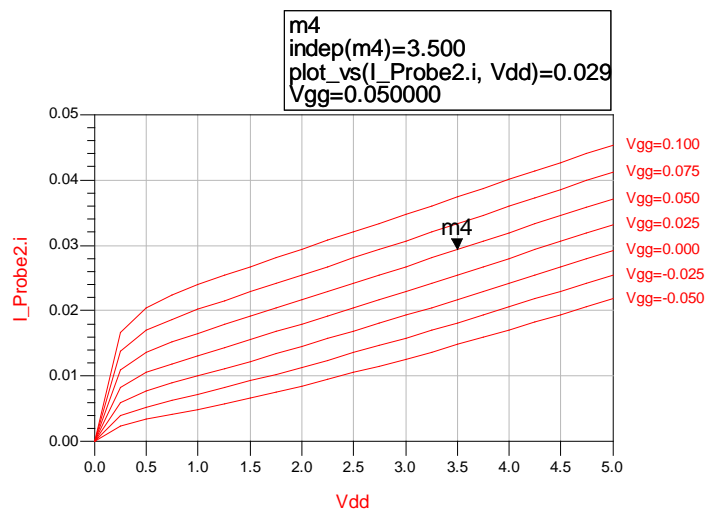Vgg=0.025
Vgg=0.000
Vgg=-0.025
Vgg=-0.050

Figure 6. I_D vs. V_{DS} for various values of V_{GS}

Schematic

RF Schematic

A simplified lumped element model of the complete VCO circuit is shown below in Figure 7. Enclosed within the green block is the resonator portion of the VCO; this represents the loading network used to tune the oscillator. Enclosed within the purple block is the single transistor stage with capacitive feedback on the source terminal; during the design of the oscillator, this portion was treated as the negative resistance element. Enclosed within the orange block is the terminating network; this portion represents terminating network used to maximize the input impedance of the transistor. Enclosed within the yellow block, is the bandpass filter used to filter the output signal.
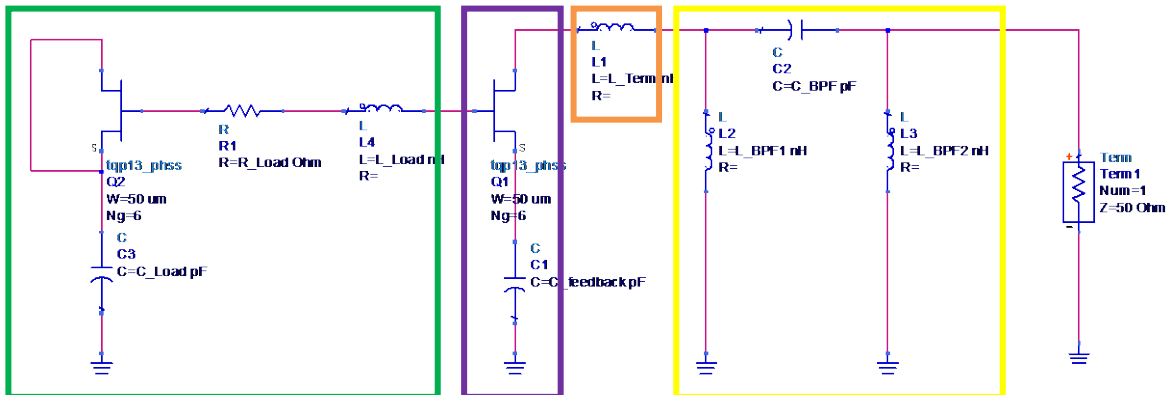

Figure 7. Simplified RF lumped element model of VCO

In the actual design of the VCO, many of the component values were very small, approaching the design limits of the process. To overcome these limitations, distributed elements were utilized in some places. Figure 8 illustrates the simplified RF schematic of the VCO with the distributed elements shown.
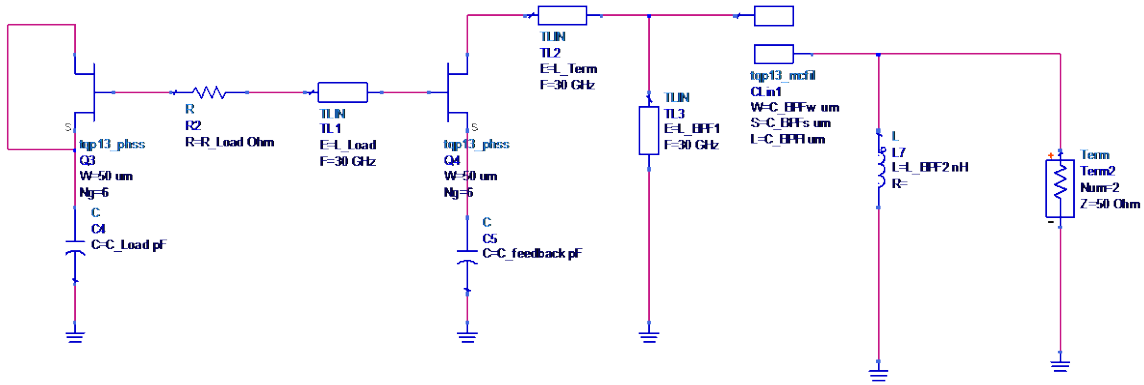
Figure 8. Simplified RF distributed/lumped element hybrid model of VCO

DC Schematic

A simplified lumped element model of the complete VCO circuit with the DC elements also included is shown below in Figure 9. A resistive divider network was utilized to set the gate voltage from the drain voltage supply.
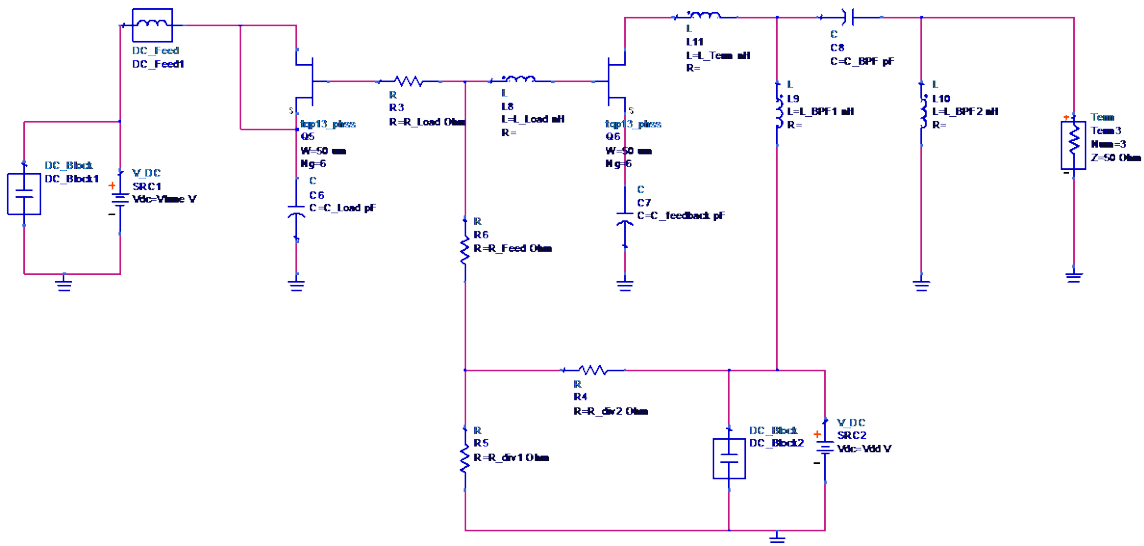

Figure 9. Simplified lumped element model of VCO with DC elements included

Layout

The final layout to be submitted to Triquint for fabrication is shown below. The drain supply voltage is labeled "3.5V" and the varactor tuning voltage is labeled "V TUNE".
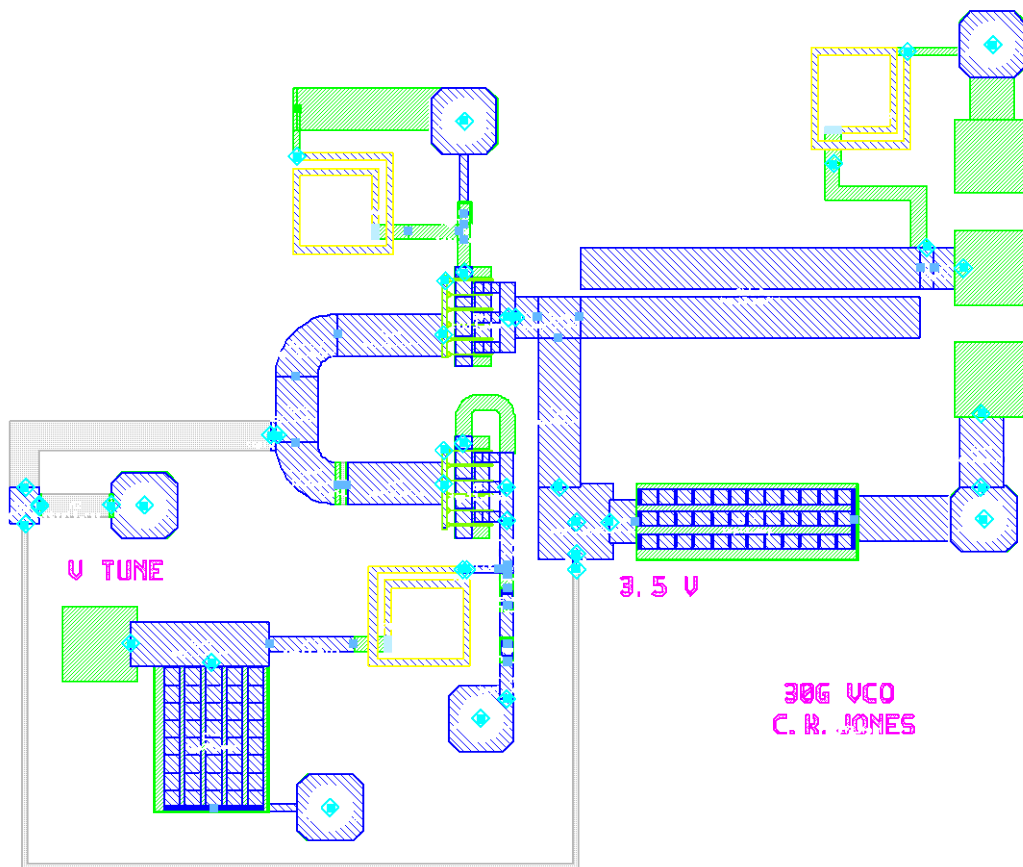

Figure 10. Final layout design of VCO

Test Plan

Upon fabrication of the VCO design, test time will be provided to test the resultant VCO design.

The following equipment will be required for testing the VCO design:

- DC power supplies (x2)
- Spectrum Analyzer
- Probes
    - DC (x2)
    - RF (x1)

The following test plan will be utilized once all materials for testing have been gathered.

- Connect power supplies to DC pads of die with DC probes
- Connect spectrum analyzer to RF pad of die with RF probe
- Apply DC power to DC pads of die with DC probes (connected to power supplies)
- Vdd should be set to 3.5 V
- V_tune should be set to 0.0 V
- Circuit should oscillate at 30 GHz once proper power has been supplied to DC pads; verify frequency of oscillation on spectrum analyzer
- If circuit is oscillating, set V_tune to 1V and measure power and frequency of resultant signal
- Proceed to adjust V_tune in 0.5 V steps making sure to record measured power and frequency of signal

Summary and Conclusions

This report describes the design of a 30 GHz VCO to be fabricated using Triquint's TQP13 GaAs process. Because the VCO is to be operated at 30 GHz, microwave design techniques were utilized. According to the ADS simulation, it appears the design will work. The output reflection coefficient was well above unity at 30 GHz and the phase crossed the zero line at 30 GHz as well. Further investigation into the phase noise and harmonic index of the design needs to be carried out.

Because the design operates at such a high frequency, it was found that the line lengths played a critical role in setting the final frequency of the oscillator. Coincidentally, because some of the lumped element components were replaced by distributed element equivalents, the Q-factor of the overall design increased. This occurred because the lumped elements were replaced with wide transmission lines that introduced less loss into the system.

In the future, a design that is based around a gate voltage of 0 V is suggested. Laying out the resistive divider network was dificult and it's hard to say how accurate the voltage will be once implemented. The final output frequency seemed to fluctate if the gate voltage was not exactly as designed for.
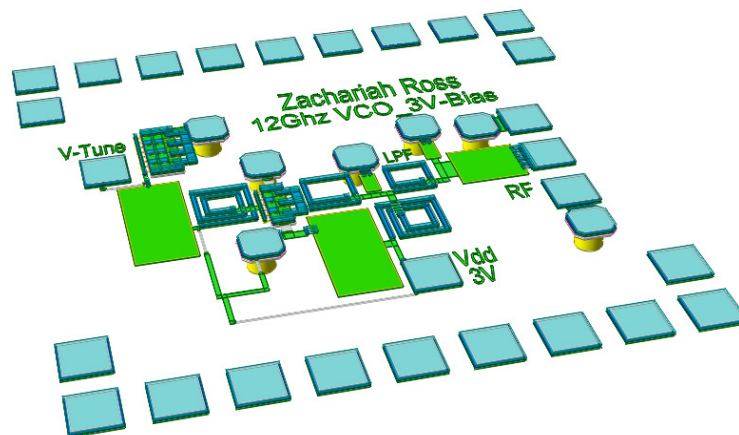
12 GHZ VOLTAGE CONTROLLED OSCILLATOR

by

Zachariah Ross

Final Design Project
Fall 2012

MMIC Design – 525.787
Johns Hopkins University

ABSTRACT

This paper describes and details the design of a 12GHz Voltage Controlled Oscillator Monolithic Microwave Integrated Circuit. This MMIC is designed using TriQuint elements with AWR's Microwave Office for fabrication through the 0.13um TPQ13 process. The design includes lumped element components with a low pass filter transformer, varactor tuning network, and encompassed on a 60mil x 60mil anachip area.
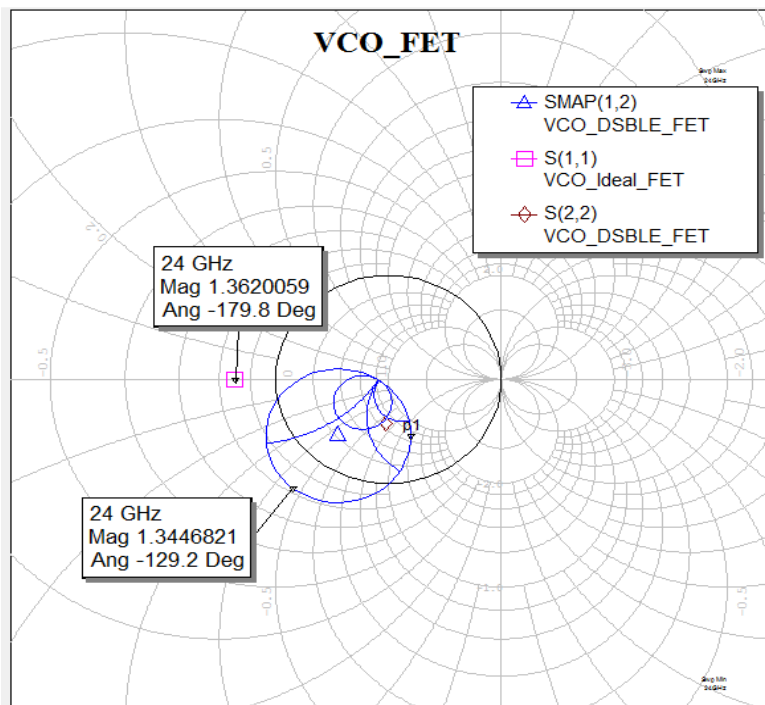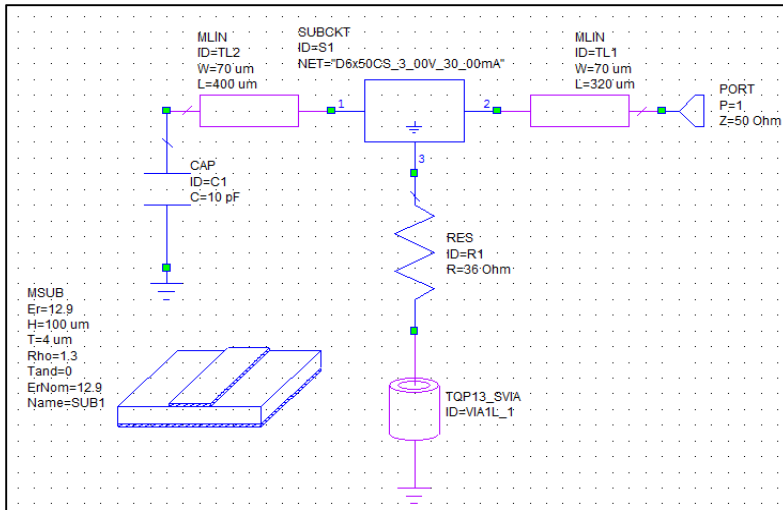
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INTRODUCTION

The Voltage Controlled Oscillator (VCO) described in this paper is a one-port device for use in a microwave receiver for use as a local oscillator for up/down conversion of RF signals. The target frequency is 12GHz with a 3V bias and Varactor tuning range -0.4V to +0.4V. This design includes a low pass filter for the quarter-wave transformer to limit higher order harmonic signals. The ouput signal will be around 12dBm depending on tuning, and will be matched to a 50Ohm input. The design uses TQP13 library with the TOM-4 6x50 um PHEMT.

DESIGN APPROACH & SIMULATIONS

The overall design approach is to use the negative impedance method for determining destabilizing resistance, gate and drain inductance to achieve $R_D > 3(R_L)$, and creating a lumped element π-design low pass filter as the quarter-wave transformer. The varactor tuning network was then designed to vary the capacitance and enable frequency tuning.

Initial attempt with 24GHz design target using the above approach proved incapable of giving the necessary controlled oscillation. With the most optimal destabilizing resistance at 24GHz (36Ohms), $R_D > 3(R_L)$ was not even close to being achievable with a maximum R_D of 1.36(R_L). Simulation of 24GHz attempt is shown below. Gate and Drain inductors/microstrip lines barely improved on outcome.

VCO_FET

Legend:
- SMAP(1,2) VCO_DSBLE_FET
- S(1,1) VCO_Ideal_FET
- S(2,2) VCO_DSBLE_FET

24 GHz
Mag 1.3620059
Ang -179.8 Deg
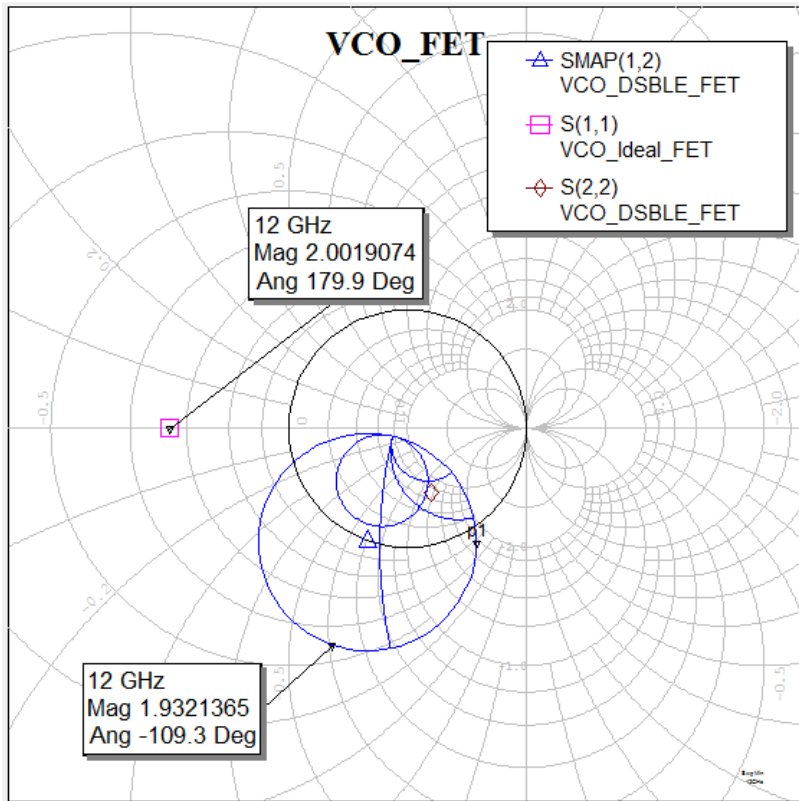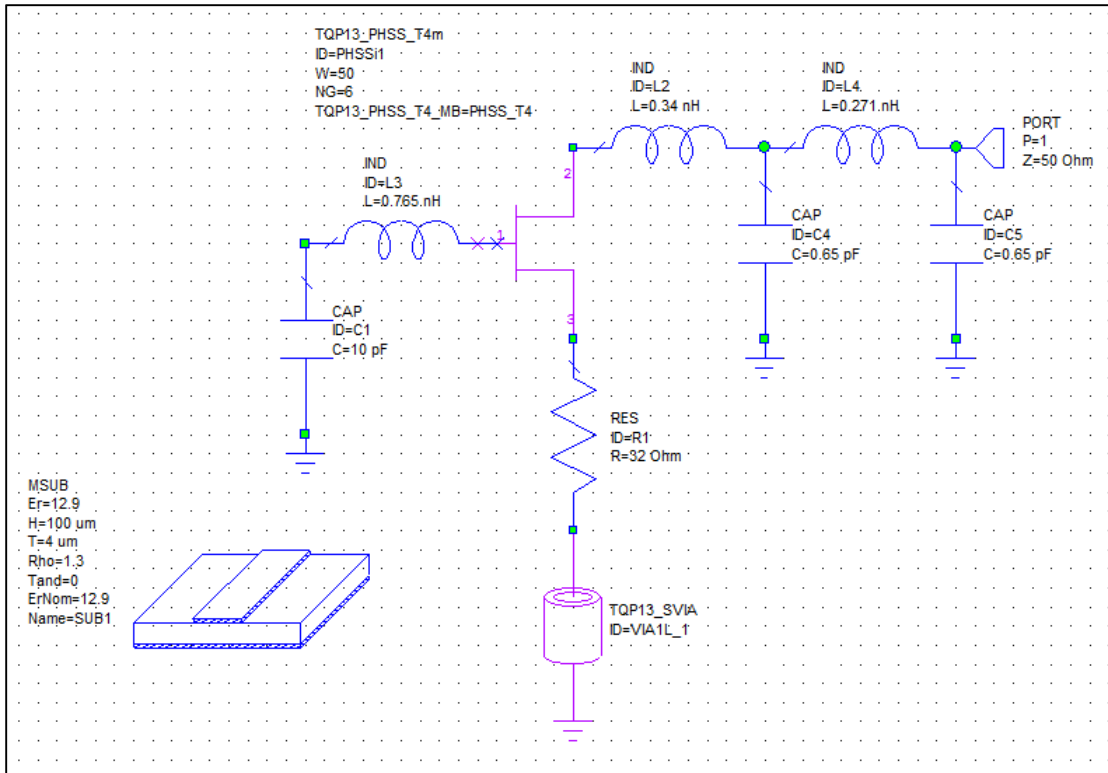
24 GHz
Mag 1.3446821
Ang -129.2 Deg

After it was determined that 24GHz was not feasible with the negative resistance approach, target frequency was switched to 12GHz with potential for combining it with a frequency doubler to obtain 12GHz.

Destablizing Resistor, Gate and Drain elements, Quarter-wave Transform:

The 12GHz was easily achievable with the negative resistance approach in which the $R_D > 3(R_L)$ requirement was obtained. Optimal destabilizing resistance was found to be 32Ohms for 6x50um PHEMT at 12GHz. The Γ_s mapping circle only had a max magnitude of 1.93, but the gate and drain inductors were able to considerably improve S11 to $R_D > 3.5(R_L)$. A π-designed low pass filter was added to the circuit as the quarter-wave transformer: 20.4Ohms needed to transform 8.5 to 50 Ohms.

TQP13_PHSS_T4m
ID=PHSSi1
W=50
NG=6
TQP13_PHSS_T4_MB=PHSS_T4

IND
ID=L2
L=0.34 nH

IND
ID=L4
L=0.271 nH

PORT
P=1
Z=50 Ohm

IND
ID=L3
L=0.765 nH

CAP
ID=C4
C=0.65 pF

CAP
ID=C5
C=0.65 pF

CAP
ID=C1
C=10 pF

RES
ID=R1
R=32 Ohm

MSUB
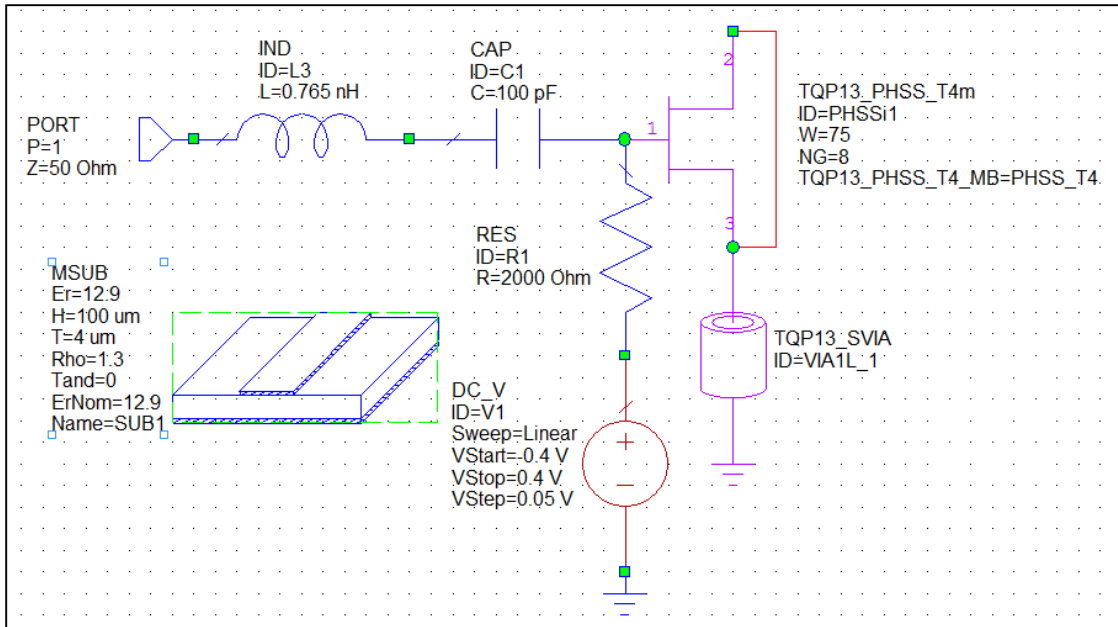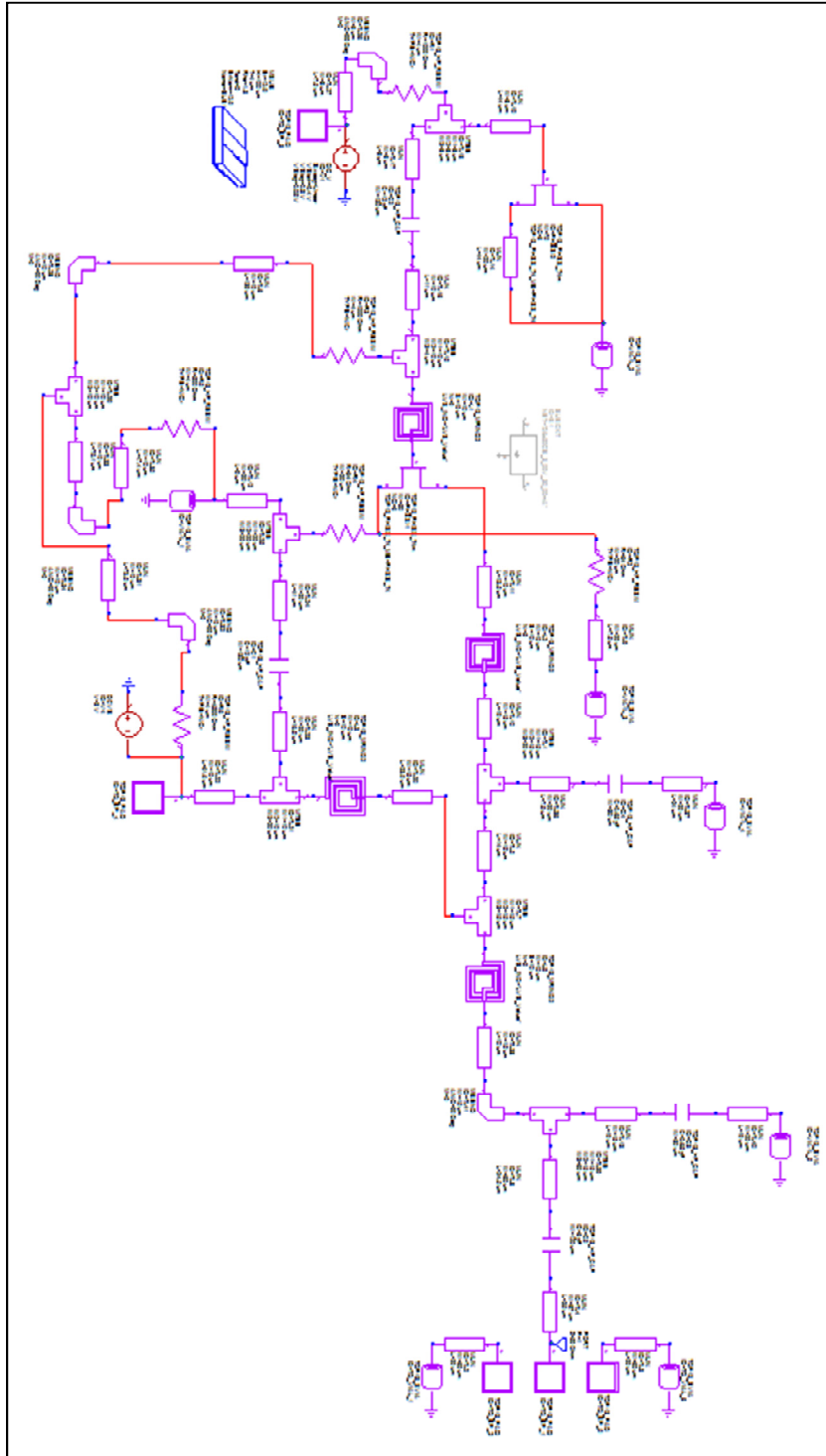Er=12.9
H=100 um
T=4 um
Rho=1.3
Tand=0
ErNom=12.9
Name=SUB1

TQP13_SVIA
ID=VIA1L_1

Varactor Design:

The varactor design encompasses a TOM-4 PHEMT and a DC Tuning power supply of -0.4V to +0.4V.

Label	Value
p1:	Vdc = -0.4 V
p2:	Vdc = -0.35 V
p3:	Vdc = -0.3 V
p4:	Vdc = -0.25 V
p5:	Vdc = -0.2 V
p6:	Vdc = -0.15 V
p7:	Vdc = -0.1 V
p8:	Vdc = -0.05 V
p9:	Vdc = 0 V
p10:	Vdc = 0.05 V
p11:	Vdc = 0.1 V
p12:	Vdc = 0.15 V
p13:	Vdc = 0.2 V
p14:	Vdc = 0.25 V
p15:	Vdc = 0.3 V
p16:	Vdc = 0.35 V
p17:	Vdc = 0.4 V

Varactor

Swp Max
12GHz

12 GHz
Mag 0.9629
Ang 120.3 Deg

S(1,1)
Varactor

Swp Min
12GHz

IND
ID=L3
L=0.765 nH

CAP
ID=C1
C=100 pF

PORT
P=1
Z=50 Ohm

TQP13_PHSS_T4m
ID=PHSSi1
W=75
NG=8
TQP13_PHSS_T4_MB=PHSS_T4

RES
ID=R1
R=2000 Ohm

MSUB
Er=12.9
H=100 um
T=4 um
Rho=1.3
Tand=0
ErNom=12.9
Name=SUB1

DC_V
ID=V1
Sweep=Linear
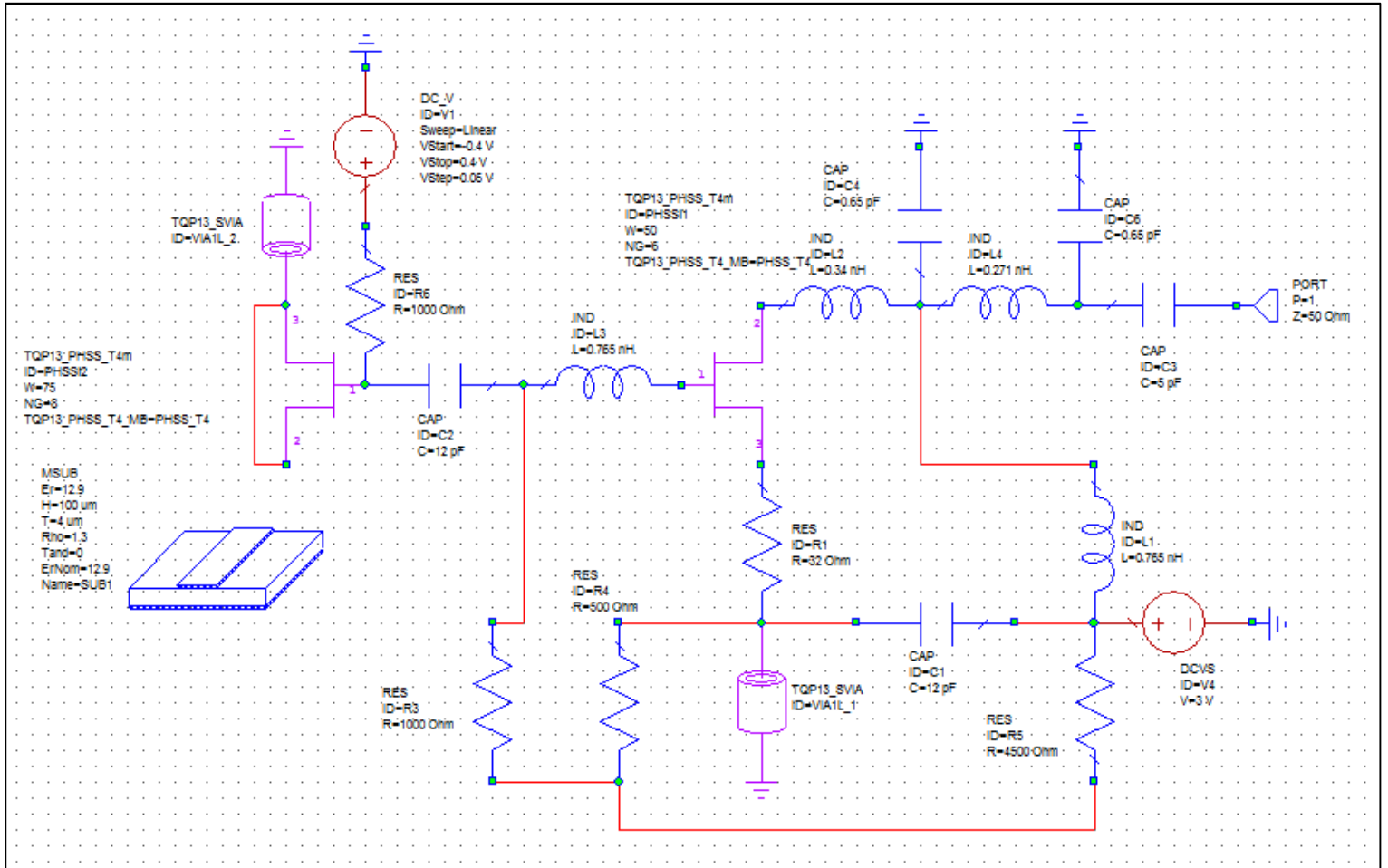VStart=-0.4 V
VStop=0.4 V
VStep=0.05 V

TQP13_SVIA
ID=VIA1L_1

SCHEMATIC: INTERCONNECTS INCLUDED

SCHEMATIC: SIMPLIFIED DC WITHOUT INTERCONNECTS

LAYOUT

The following layout is from AWR's Microwave Office and shows the circuit inside the border of the anachip library. The RF Input, 3V Vdd bias pad, and varactor tuning pad are all properly labeled. The location of the low pass filter is also designated. The three broken connections on the 2 large capacitors are only symbolic, as the element connections are correctly implemented in the layout. This is due to the element requirement that connection be made at the opposite ends of the capacitors in the library which is not actually necessary.
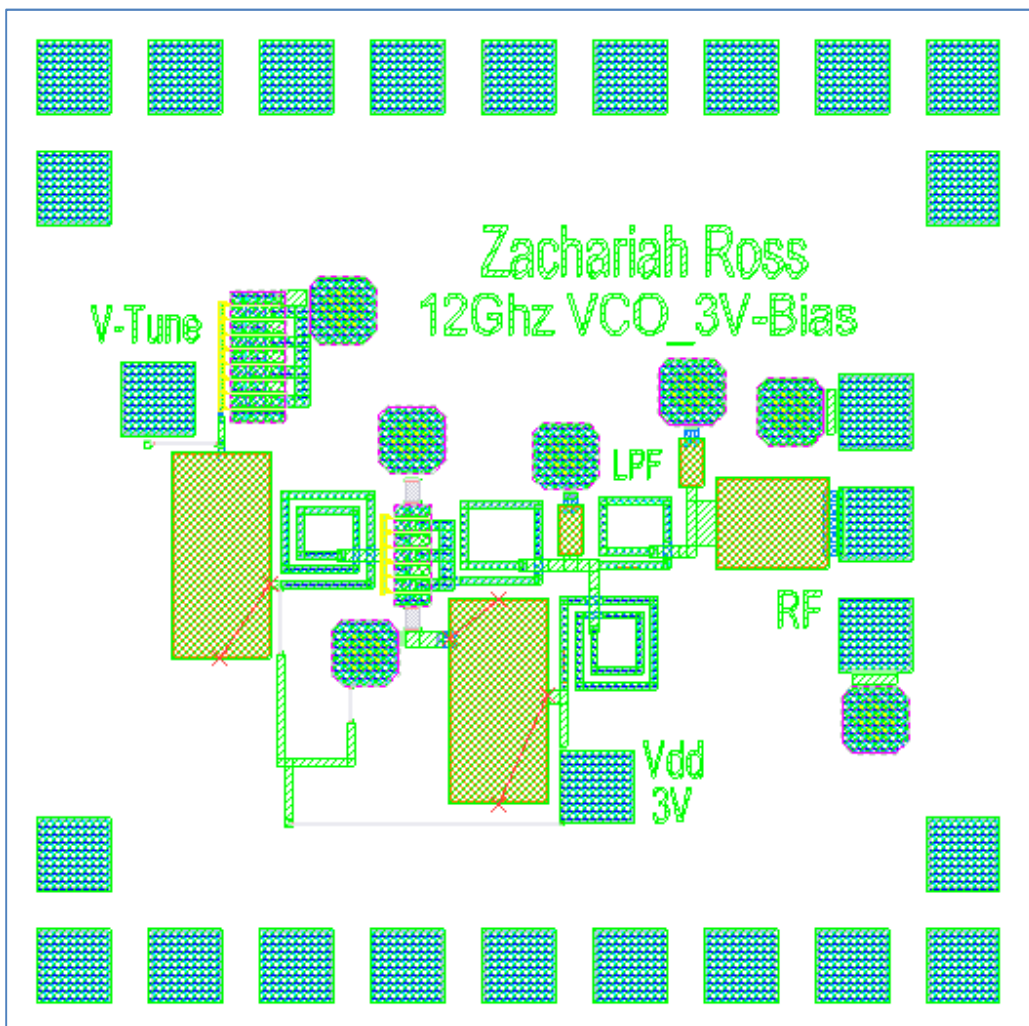
LAYOUT

Here is the 3-D layout:
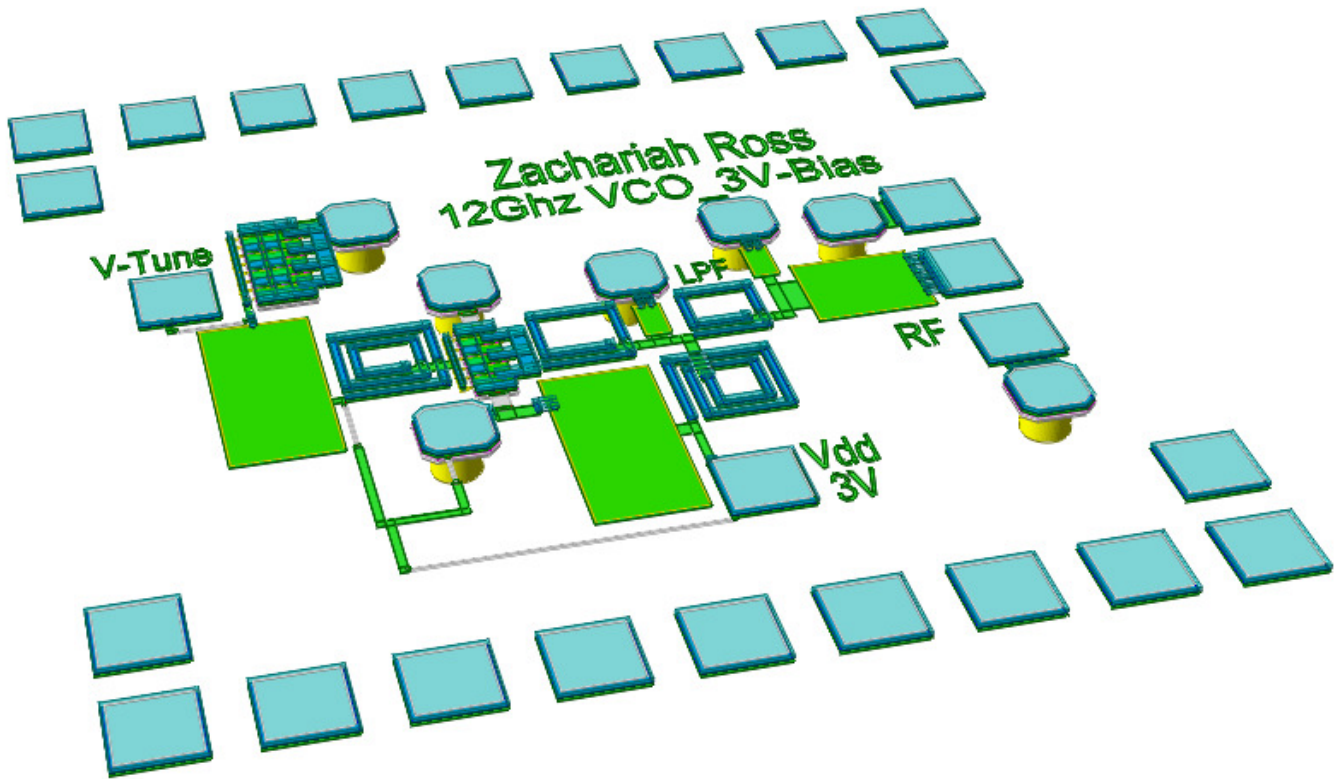
TEST PLAN

Once the MMIC has been fabricated the following requirements and procedures can be used to test the chip in the lab:

Requirements:
1. DC Power supply and probe for 3V Vdd
2. DC Power supply and probe for Varactor Tuning
3. Network Analyzer and RF probe for signal

Procedures:
1. Connect a 3V power supply to the Vdd pad with a probe
2. Connect the other DC power supply to the VTune pad and set it to -0.4V with a probe.
3. Connect the network analyzer to the ground signal ground and measure the signal being generated.
4. Also measure the Low Pass Filter effectiveness by checking the 2nd and 3rd higher order harmonics.
5. Adjust V-Tune to optimize the frequency by increasing the voltage in 0.1V increments. Check the frequency range and set it to the design frequency. Again check for the suppression of the 2nd and 3rd higher order harmonics.

SUMMARY & CONCLUSIONS

The 12GHZ VCO device outlined in this report will be able to act as a local oscillator for any receiver design and can be couple with a frequency multiplier to obtain higher frequencies. Using the TriQuint elements and traditional negative impedance VCO design method, creating a VCO below 20GHz was fairly straight forward compared to the initial effort of creating a 24GHz VCO which proved difficult to obtain the necessary resonance with a destabilizing resistance. The use of the low pass filter should aid in quenching high order signals and leave only the fundamental 12GHz signal.

As far as the TPQ13 process, there should not be any issues with fabrication of the MMIC supplemental to passing the design rule check and Layout vs. Schematic check. Possibilities in using this design can include combining it with a frequency multiplier, and/or with a mixer in as a up/down conversion matching it to the 50Ohm port.