THE JOHNS HOPKINS UNIVERSITY
G. W. C. WHITING SCHOOL of ENGINEERING
ELECTRICAL ENGINEERING PROGRAM

MICROWAVE ENGINEERING
MMIC DESIGN 525.787
PROJECT REPORTS

MMIC DOUBLE BALANCED MIXER
E Adler and E Viveiros

ACTIVE CIRCULATOR
G Polacek and R Meissner

MEDIUM POWER AMPLIFIER
J Roussos and D Boulanger

2 db - 4 dB SWITCHED ATTENUATOR
LJ Moskowitz and SR Turnquist

8 dB - 16 Db SWITCHED ATTENUATOR
M Pacek and K Faison

MMIC ELLIPTIC FILTERS
Charles Cook

INSTRUCTORS:

CRAIG MOORE AND JOHN PENN

DECEMBER 20, 1989

MMIC DOUBLE BALANCED MIXER

ERIC ADLER and ED VIVEIROS

DECEMBER 11,1989

MMIC DESIGN 525.787

PROFESSORS CRAIG MOORE and JOHN PENN

Conclusions and Recommendations

Computer simulations performed on the mixer, which included a FET ring and active baluns, revealed that the design met or exceeded all the required specifications. A maximum conversion loss 10 dB is achieved for RF and LO frequencies from 2 to 4 GHz with an IF from .2 to .6 GHz. The limitations in the IF bandwidth is mainly caused by roll off of the DC blocking capacitor. A larger value capacitor would extend the usable range closer to DC. The RF and LO baluns are more lossy at higher frequencies and the amplitude and phase matching also degrades as the frequency increases. This causes more loss in the mixer for higher RF and LO frequencies. The yield analysis indicated the mixer conversion loss would remain under 10 dBm over the process variation.

LO - RF isolation was observed to be -49 dB at an LO of 2.6 GHz. The actual isolation is expected to be worse due to coupling and parasitics in the circuit which could not be accounted for since the circuit layout could not be simulated. Compression simulations of the RF input didn't show the 1 dB compression point as the RF was swept from -60 to 0 dBm. The linear analysis of the RF, LO, and IF balun circuits indicate the RF compression point would be above the -20 dB goal. The actual compression point is expected to be lower than that shown in the linear analysis of the baluns since the ring FETs are only 48 μm which is much smaller then the 150 μm FETs used in the baluns. VSWR simulations were unattainable for the final mixer design due to the inability to characterize the ring FET for linear analysis. Return loss (VSWR) simulations performed on the RF/LO and IF baluns, which were modeled in a 50 Ω environment, are the only indications of the expected results. The return loss for the RF/LO balun was 11 dB min. and 8 dB min. for the IF balun.

The conversion loss could be improved by adding a bias to the ring FETs to select the desired operating condition. A circuit was simulated with the ring biased which showed a conversion gain of around 5 dB. This bias was not included in the final design due to space limitations. Circuit performance could have been improved if the input impedance of the ring FETs could have been determined. A better match between the ring and the balun circuits could then be achieved.

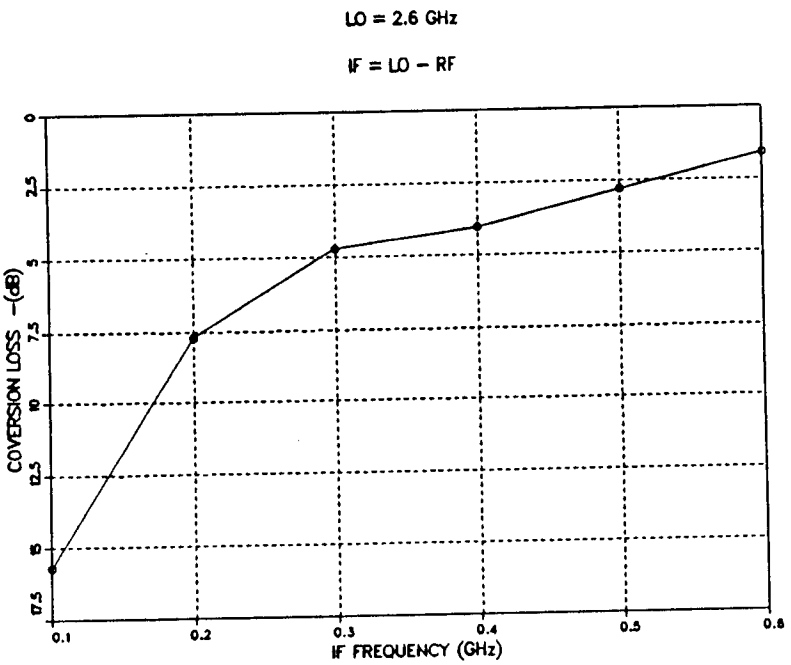


Figure 11: Narrowband Conversion Loss

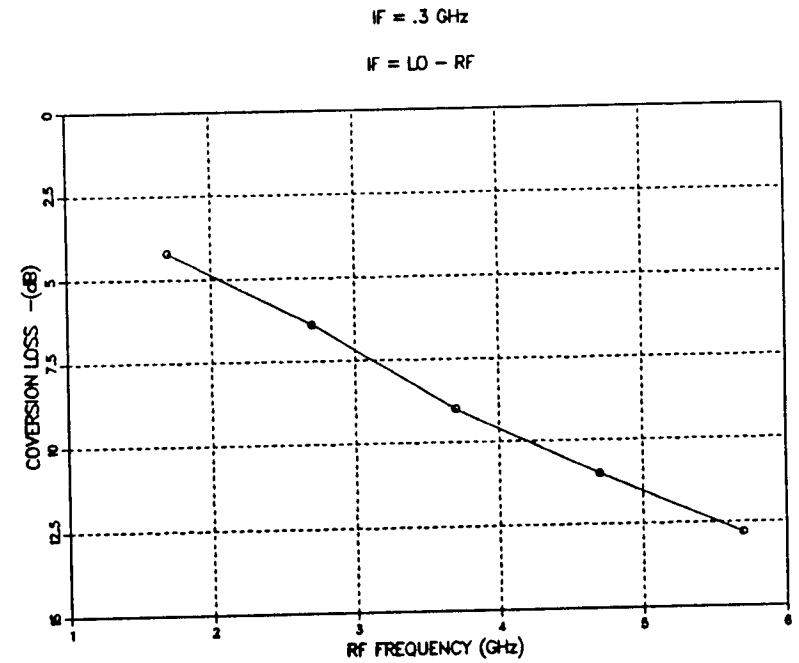


Figure 12: Wideband Conversion Loss

JHU MICROWAVE ENGINEERING

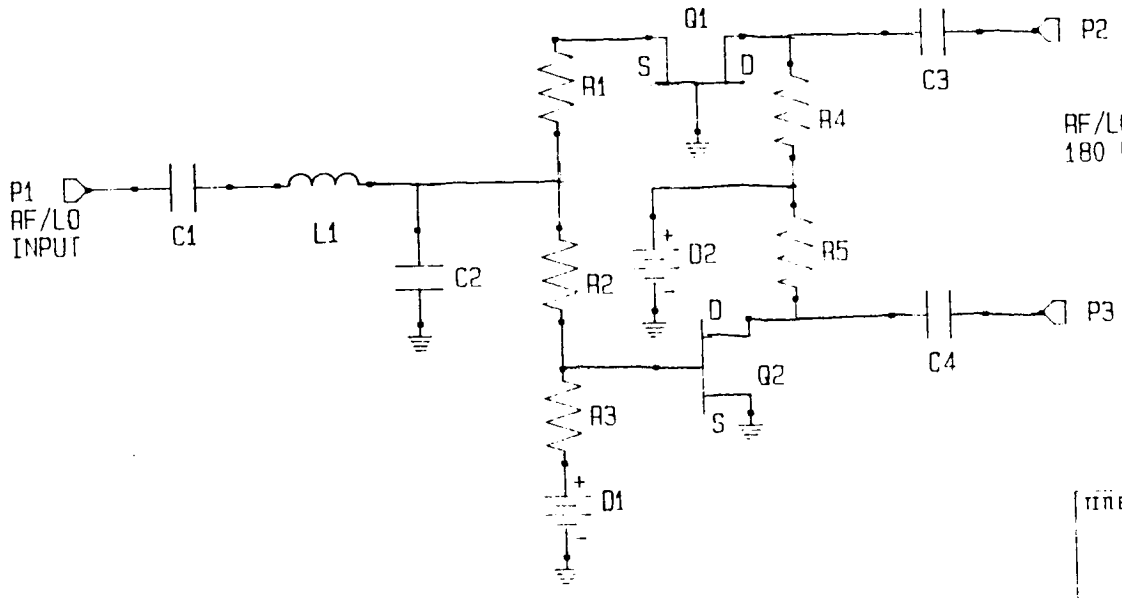
PARASITIC ELEMENTS

BOND WIRE L1 300 pH
PAD CAPACITANCE C2 45 fF

EXTERNAL DC BLOCKING CAP
C1 10000 fF

ELEMENT VALUES

D1	-5 VDC
D2	10 VDC
Q1	300um FET
Q2	300um FET
R1	25 OHMS
R2	75 OHMS
R3	280 OHMS
R4	446 OHMS
R5	500 OHMS
C3	3500 fF
C4	650 fF

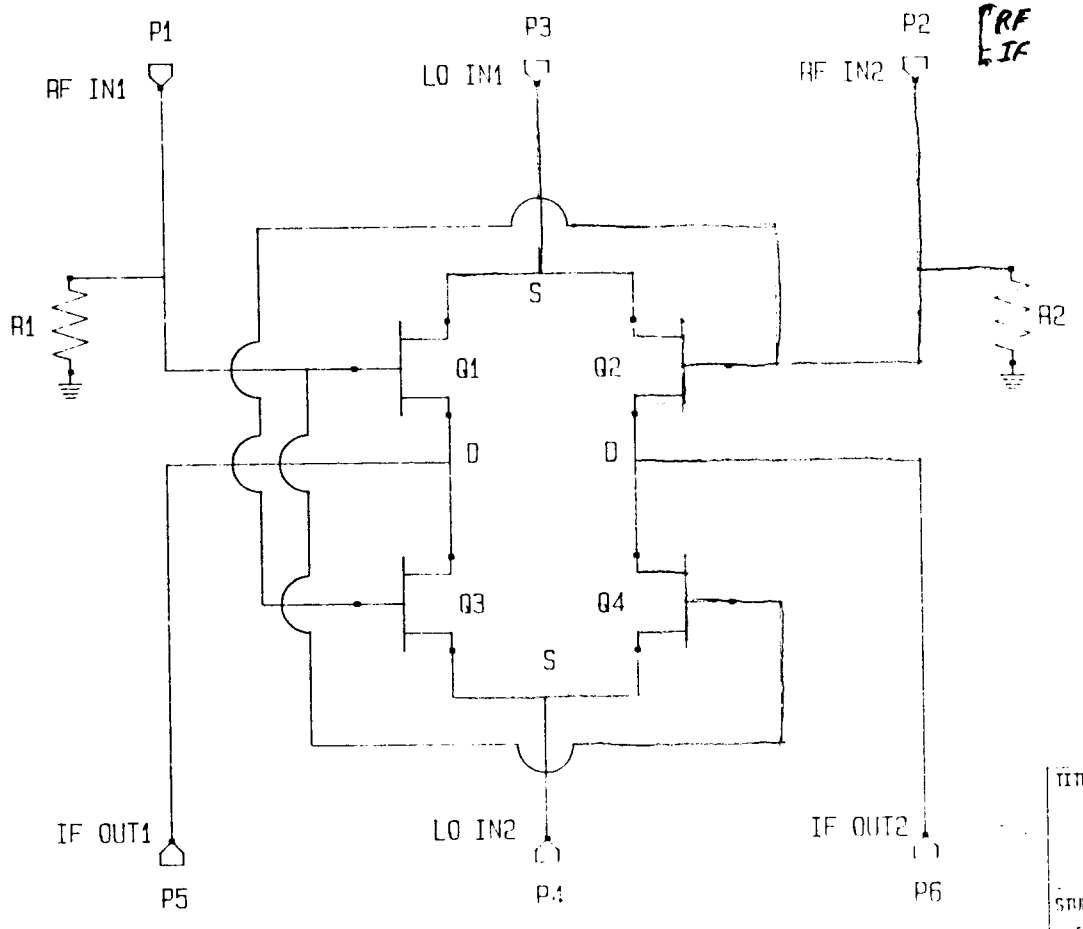


RF/LO OUTPUTS
180 DEGREES OUT OF PHASE

TITLE: MMIC DOUBLE BALANCED MIXER RF/LO BALUN			
STUDENT'S NAME: ERIC ADLER/ ED VIVEIROS			
SCALE	COURSE: 525.787	INSTRUCTOR: CRAIG MOORE/ JOHN PENN	
	DATE: 12/10/89	SHEET: 1 OF 3	

Figure 3.

JHU MICROWAVE ENGINEERING



This LO on gates
RF
IF

ELEMENT VALUES

Q1	48um FET
Q2	48um FET
Q3	48um FET
Q4	48um FET
R1	500 OHMS
R2	500 OHMS

TITLE
MMIC DOUBLE BALANCED MIXER
FET RING CIRCUIT

STUDENT'S NAME
ERIC ADLER/ ED VIVEIROS

SCALE | COURSE 525.787 | INSTRUCTOR CRAIG MOORE/ JOHN PENN

DATE 12/10/89 | SHEET 2 OF 3

JHU MICROWAVE ENGINEERING

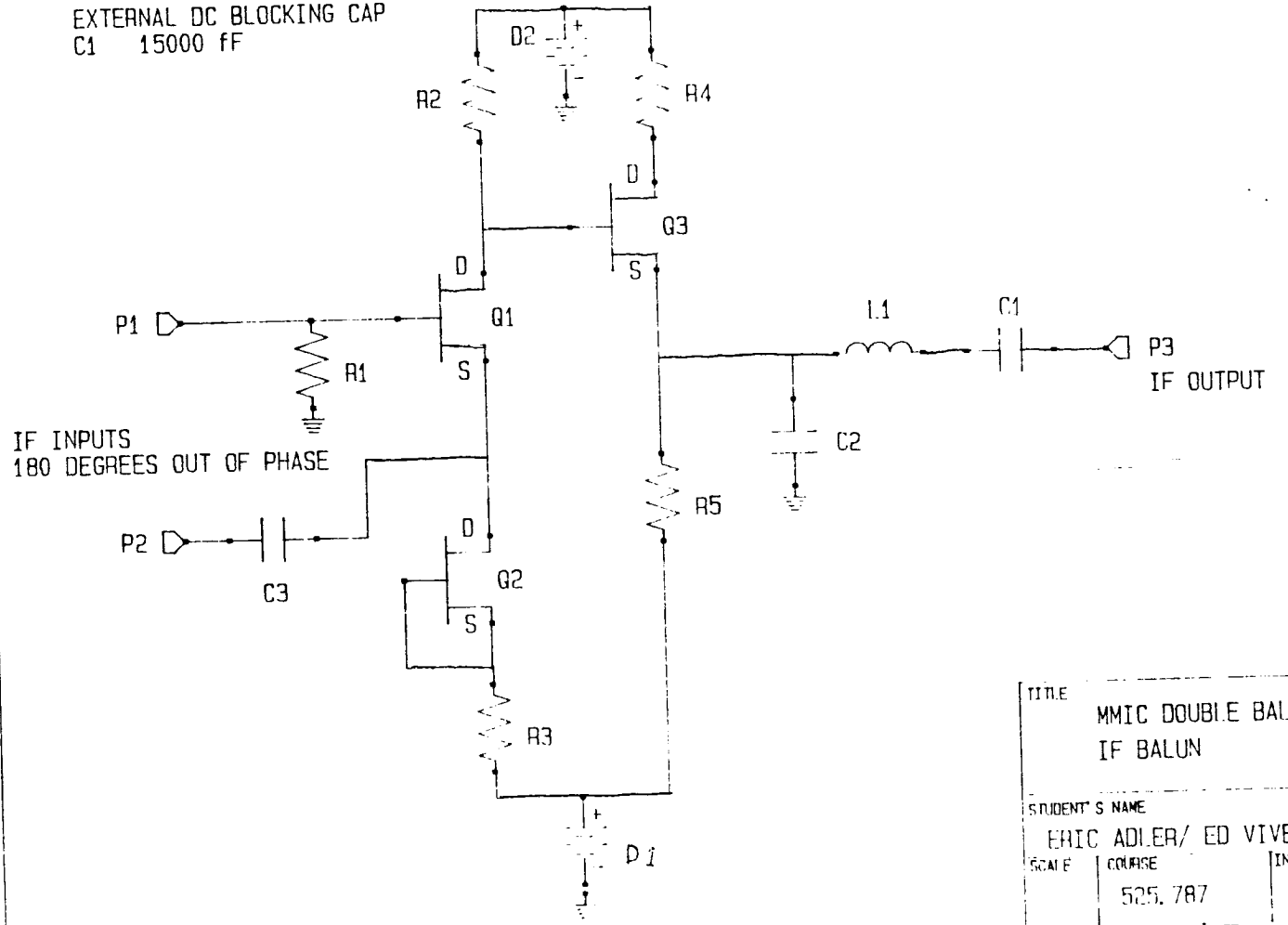
PARASITIC ELEMENTS

BOND WIRE L1 300 pH
PAD CAPACITANCE C2 45 fF

EXTERNAL DC BLOCKING CAP
C1 15000 fF

ELEMENT VALUES

D1	-5 VDC
D2	10 VDC
Q1	300um FET
Q2	100um FET
Q3	300um FET
R1	500 OHMS
R2	446 OHMS
R3	200 OHMS
R4	220 OHMS
R5	600 OHMS
C3	3500 fF



TITLE
MMIC DOUBLE BALANCED MIXER
IF BALUN

STUDENT'S NAME
ERIC ADLER/ ED VIVEIROS

SCALE	COURSE	INSTRUCTOR
	525.787	CRAIG MOORE/ JOHN PENN

DATE 12/10/89 SHEET 3 OF 3

Figure 5:

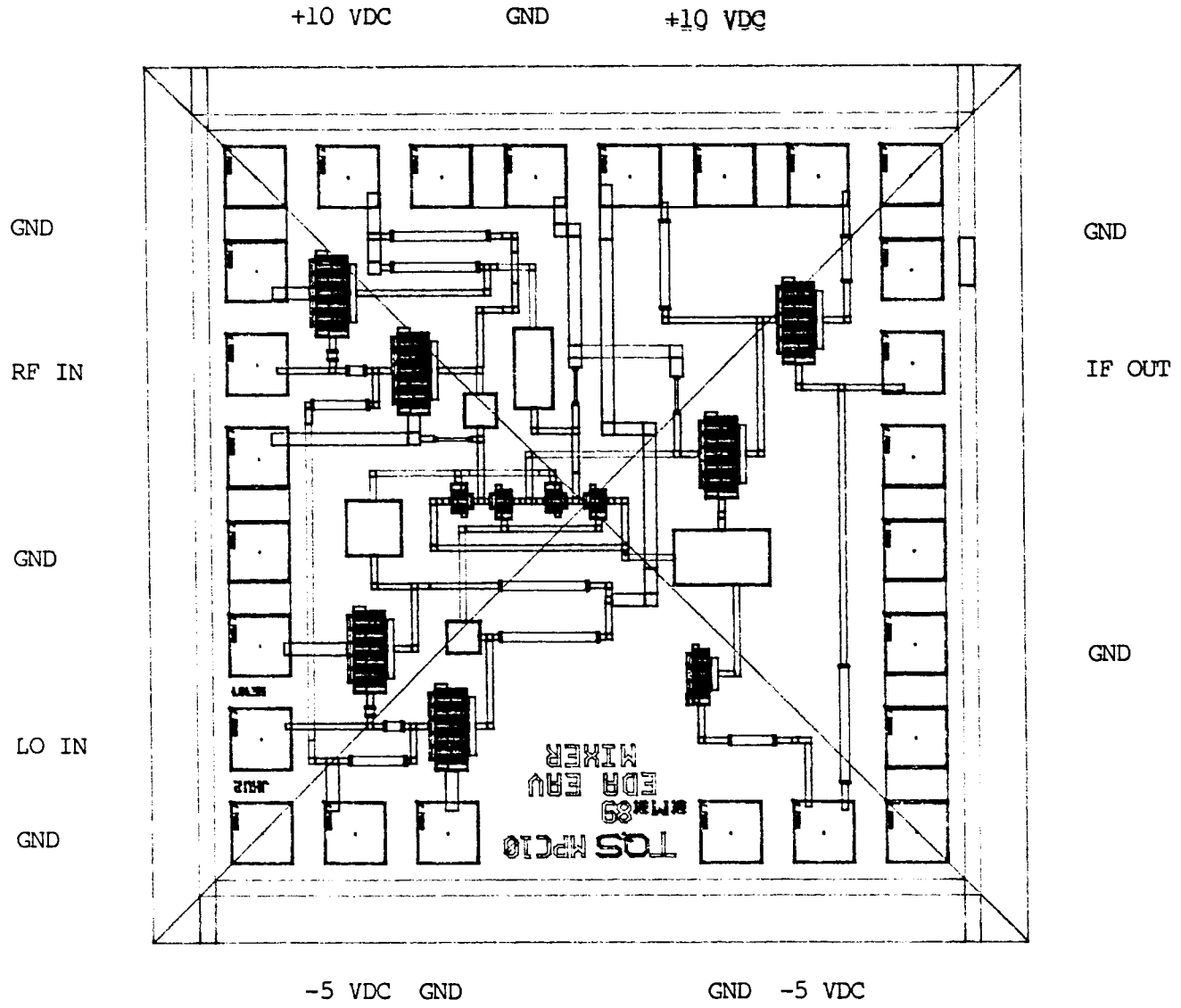


Figure 14: Final Circuit Layout

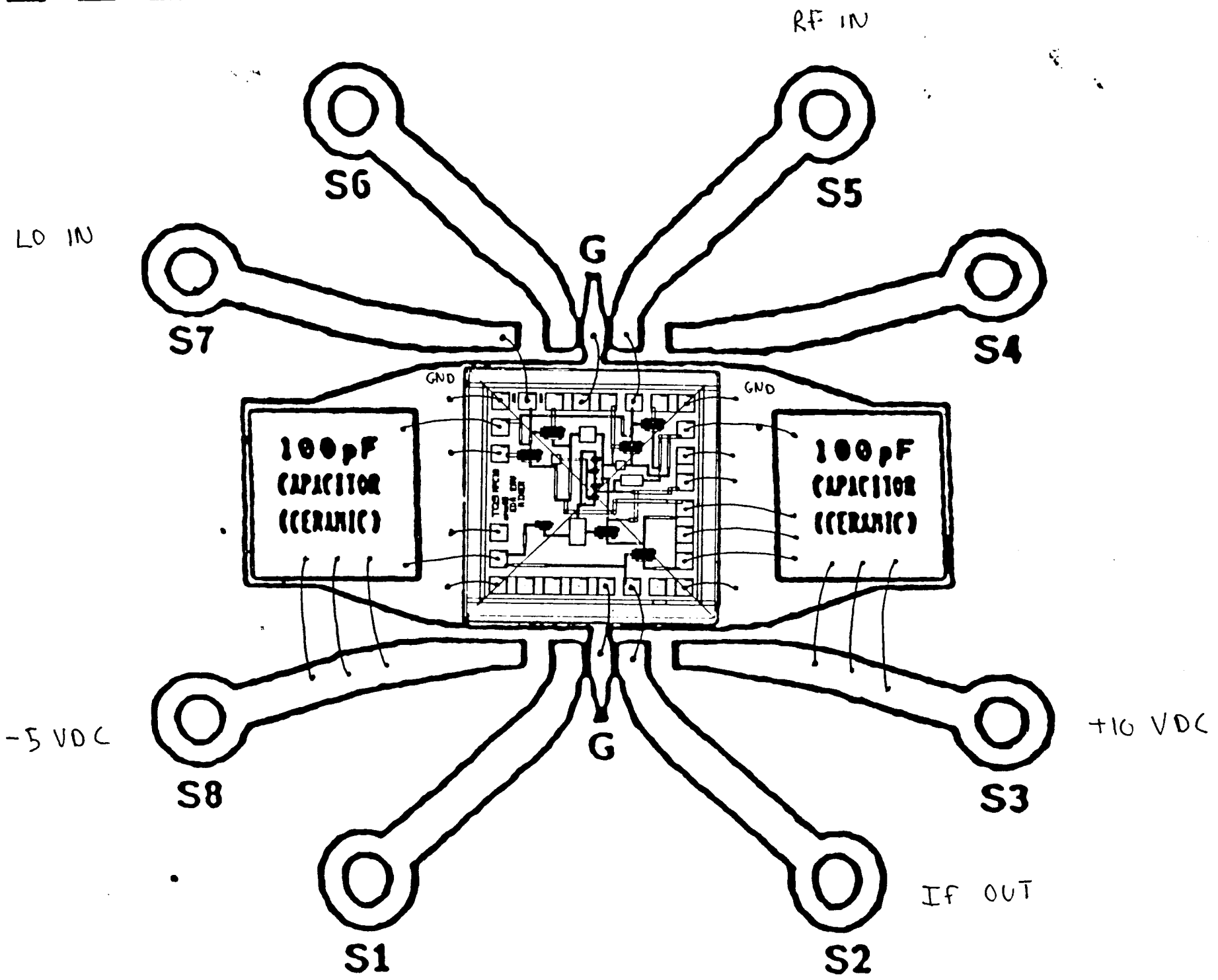
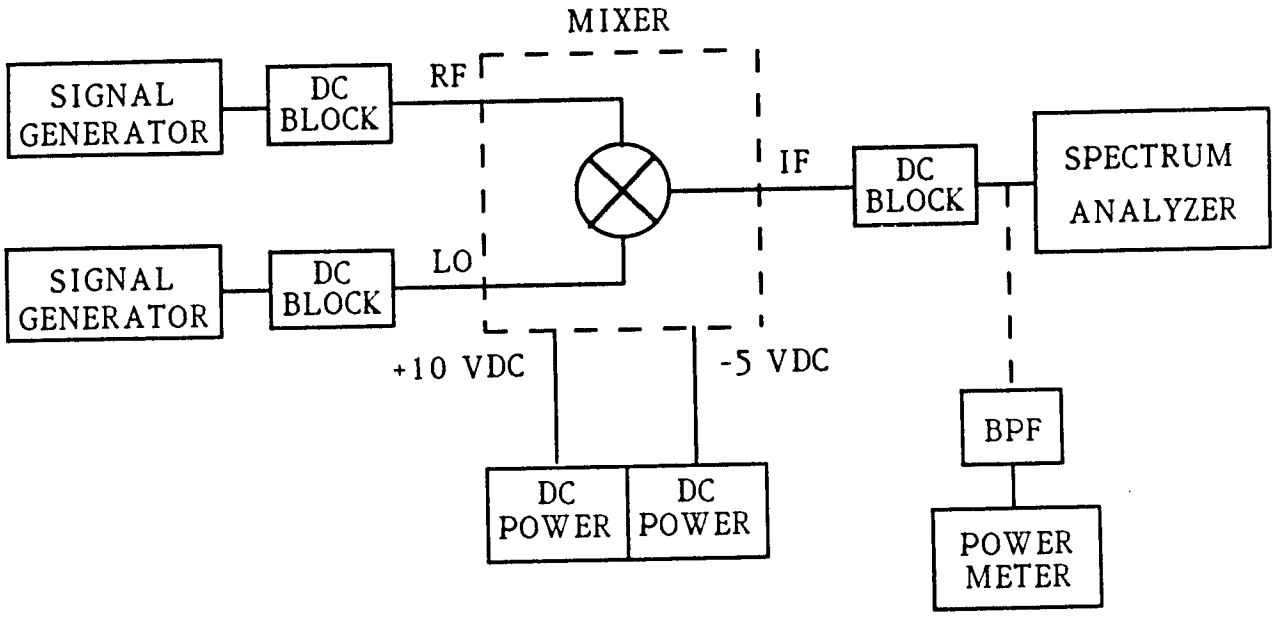


Figure 15: Expanded Bond Wire Diagram



Equipment List:

2 Signal Generators - 1-6 GHz, -20 to 0 dBm
1 Spectrum Analyzer - .1-6 GHz
2 DC Power Supplies - -5 to +10 Volts
3 DC Blocking Capacitors - 15 pF min.
1 Bandpass Filter (fixed or tunable) - pass 100-600 MHz
1 Power Meter - -40 to 0 dBm

Figure 17: Test Equipment Configuration

Active Circulator Final Report

Prepared for:
525.787 MMIC Design
December 11, 1989

Submitted by:
George Polacek
and
Robert Meissner

Specification Compliance Matrix

	SPECIFICATION	GOAL	MODELED PERFORMANCE[1]
FREQUENCY	2 - 6 GHZ	1 - 10 GHZ	1 - 10 GHZ
ISOLATION	10 dB min.	16 dB	18 dB
INSERTION LOSS	5 dB[2]	1 dB	4 dB
VSWR	2.5:1 max.	1.5:1	1.35:1
POWER @ 1 dB COMPRESSION		+10 dBm	+12 dBm

[1] - The limits of the operating frequency are taken to be the points where modeled performance fails to achieve any of the specifications. All of the other modeled performances listed are the worst case performance over the frequency range 2 to 6 GHz.

[2] - There was no specified limit on the insertion loss, but we have accepted the 5 dB goal that the author in reference 1 chose for insertion loss.

7. CONCLUSIONS AND RECOMMENDATIONS

Conclusions

The proposed circulator meets all of the specified performance measurements and even exceed most of the goals. The yield analysis predicts that 93% of the units produced will meet the requirements.

Therefore, because most of the known parasitics have been included in the modeling and because the predicted performance greatly exceeds the specifications; there is high confidence that the chip when it is actually tested will achieve the specifications from 2 to 6 GHz.

Furthermore, should the circulator achieve the predicted 1 to 10 GHz bandwidth, this design would be a marked improvement over the design in Reference 1.

Recommendations

The design of a MMIC chip is an iterative process and while we are pleased with the predicted results, we are not satisfied. Given more time, there are several areas in which further analysis/relayout could yield improved performance.

1. Convert as much of the MLINs as possible to Metal 2. This should reduce the losses in the circuit.

2. Because of physical constraints, each leg of the circulator are not identical. More could be done to improve this.

3. Because performance improved with the addition of the bond wires, perhaps series inductance could be added to the input of each port.

4. The common source greatly affects overall performance and thus a final look at optimizing the component values may improve the results.

REFERENCES

1. Dougherty; **Microwaves & RF Magazine**; June 1989; pp 85-89

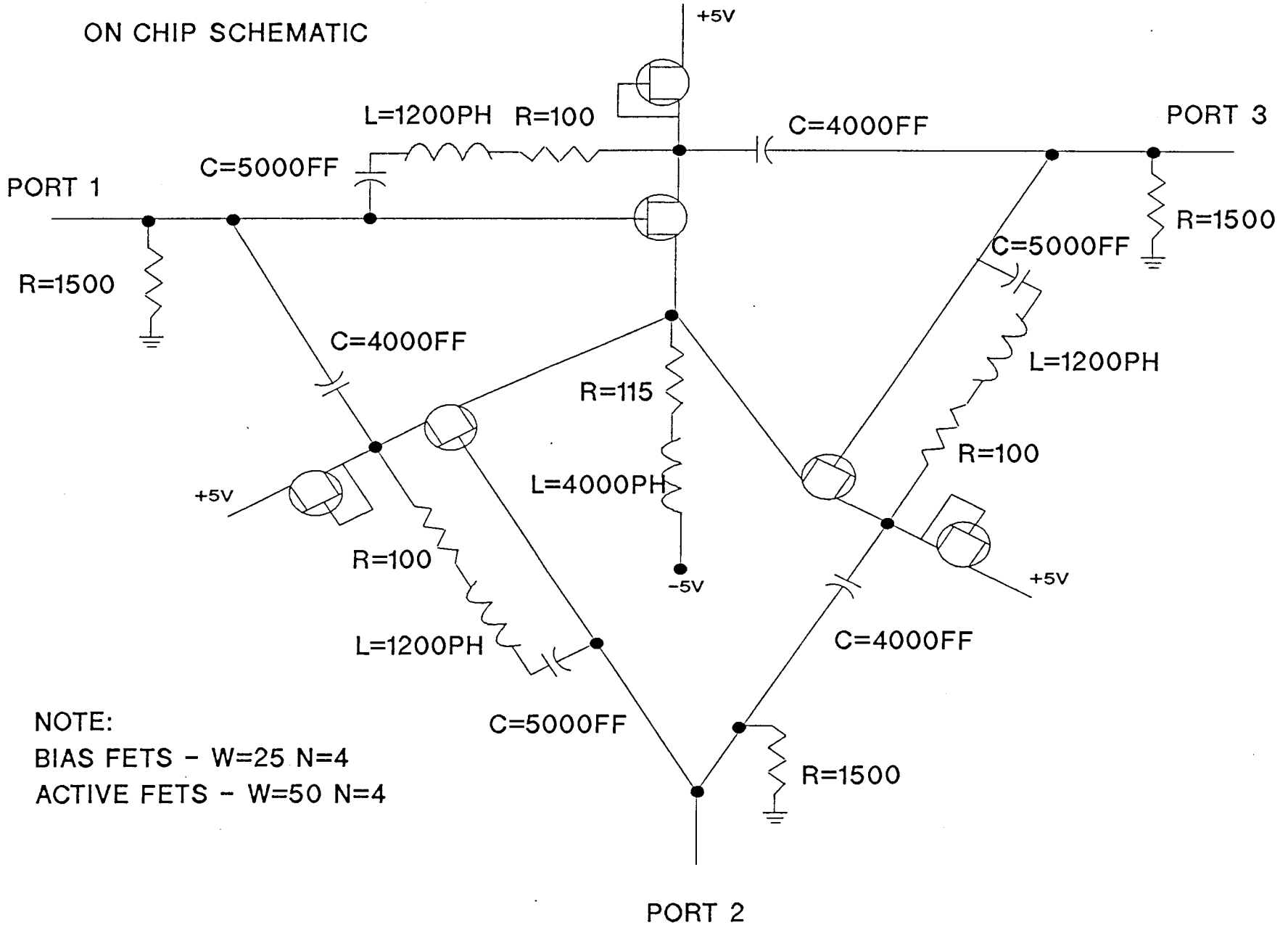


Figure 4-1. On Chip Schematic Diagram

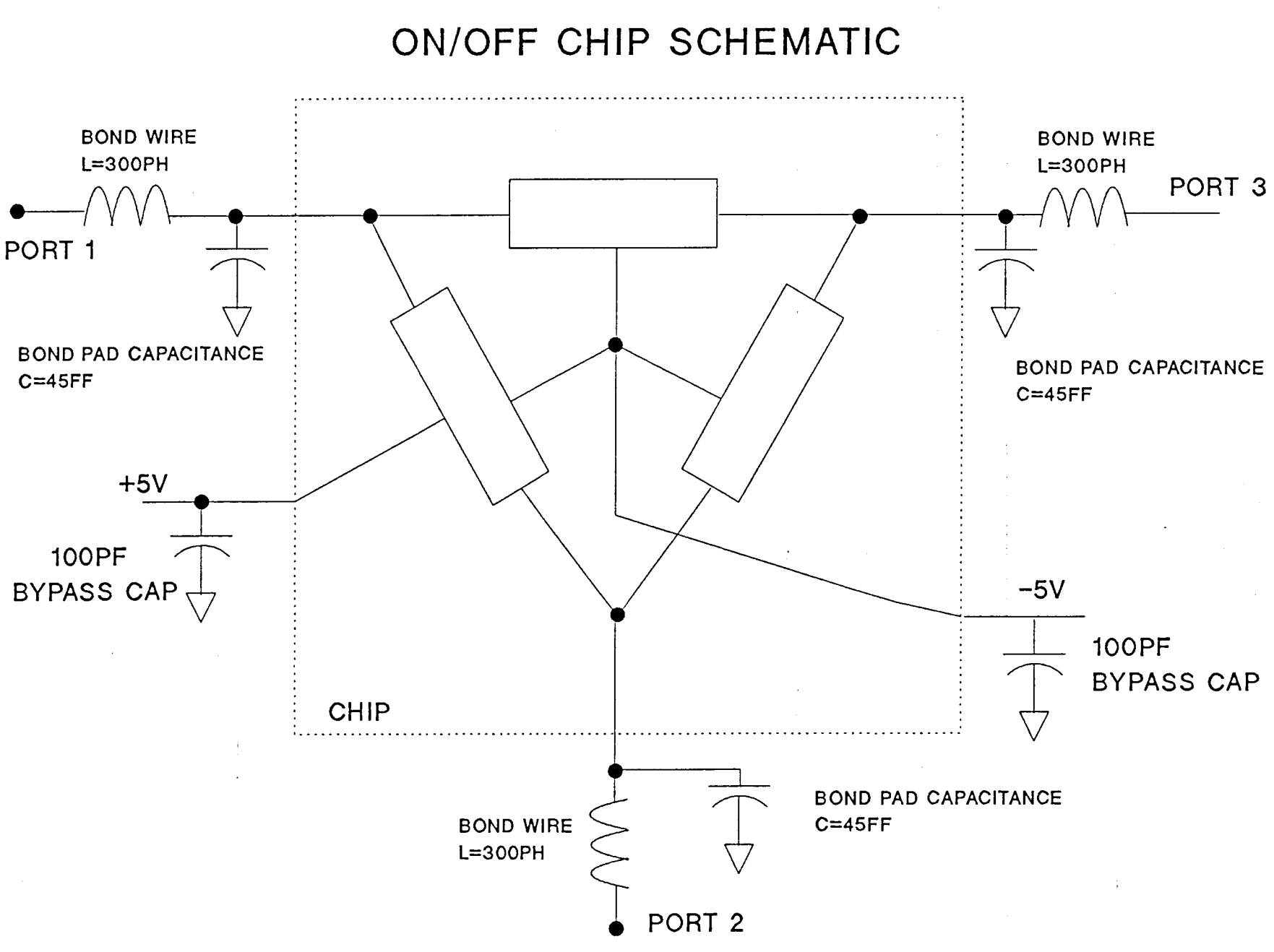


Figure 4-2. On and Off Chip Schematic Diagram

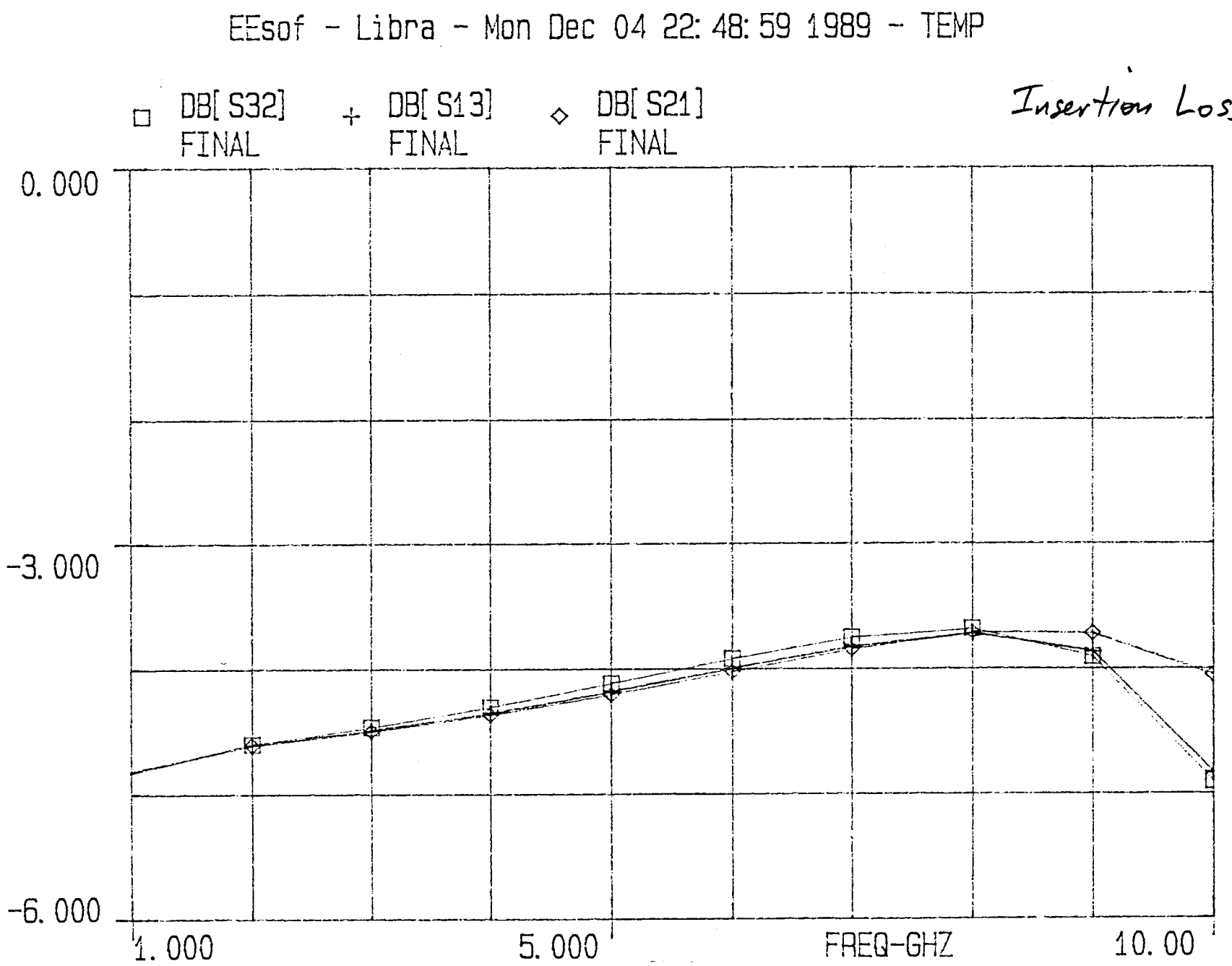


Figure 3-12. Post-Layout Linear Simulation for Insertion Loss

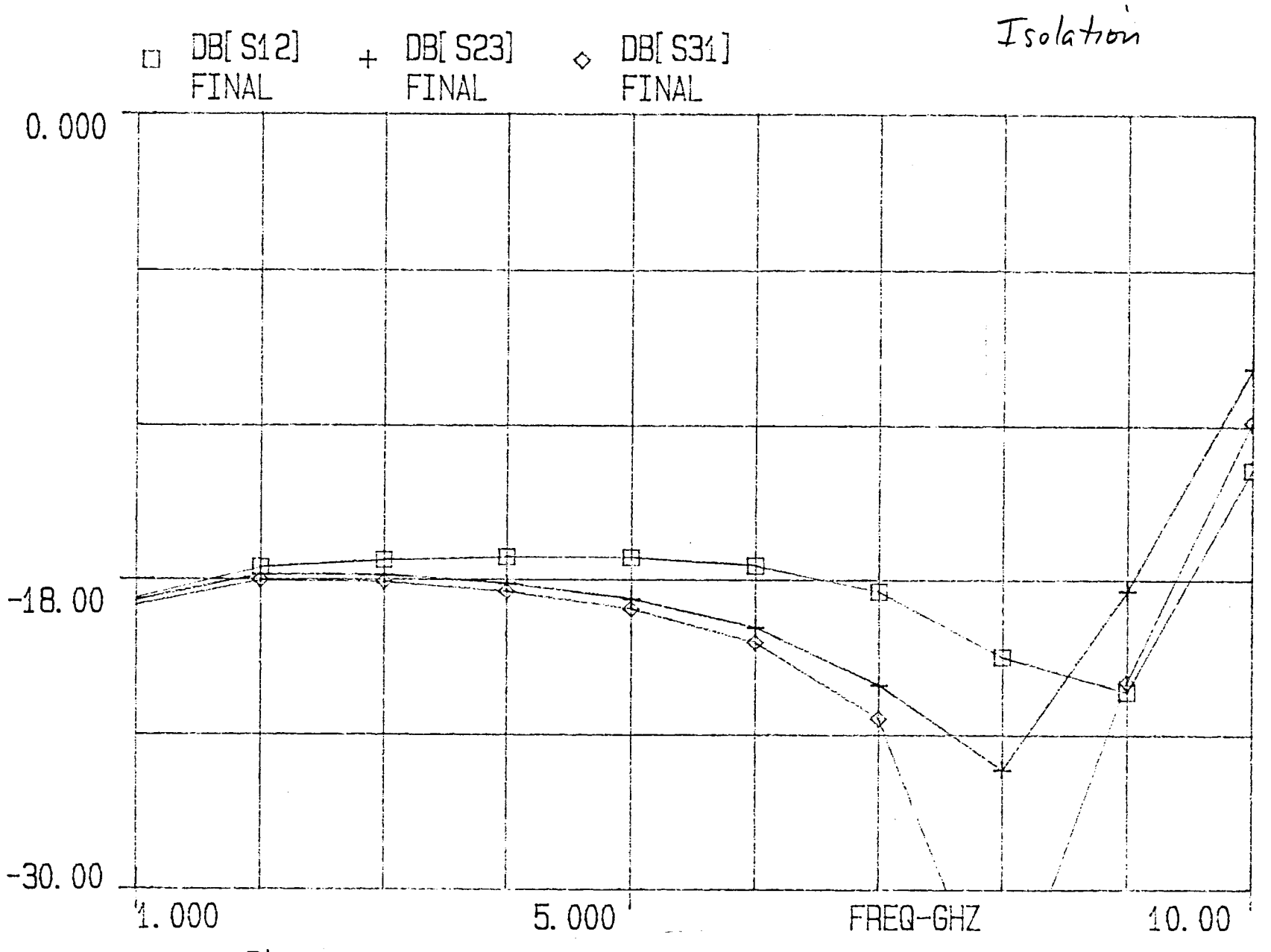


Figure 3-10. Post-Layout Linear Simulation for Isolation

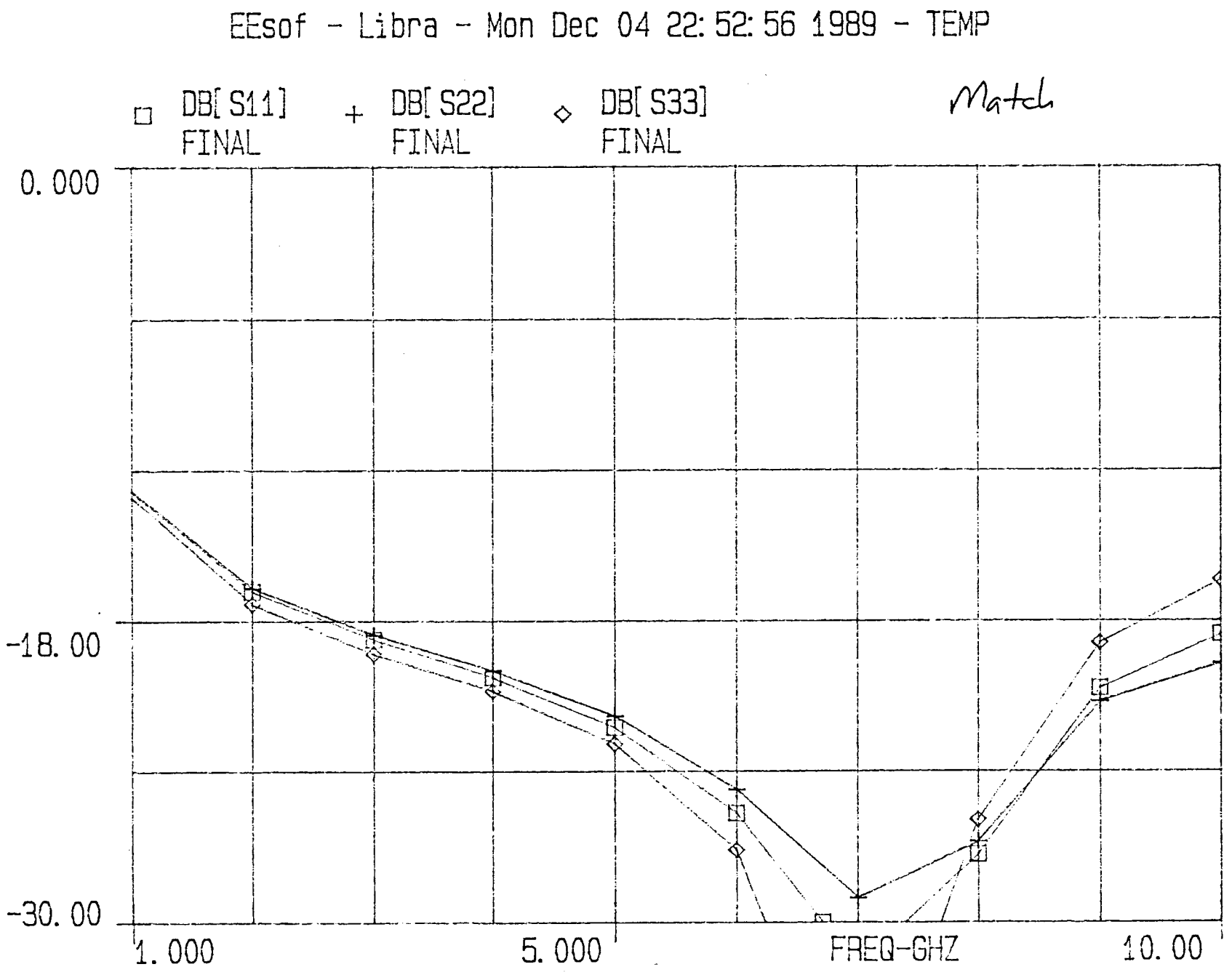


Figure 3-11. Post-Layout Linear Simulation for VSWR

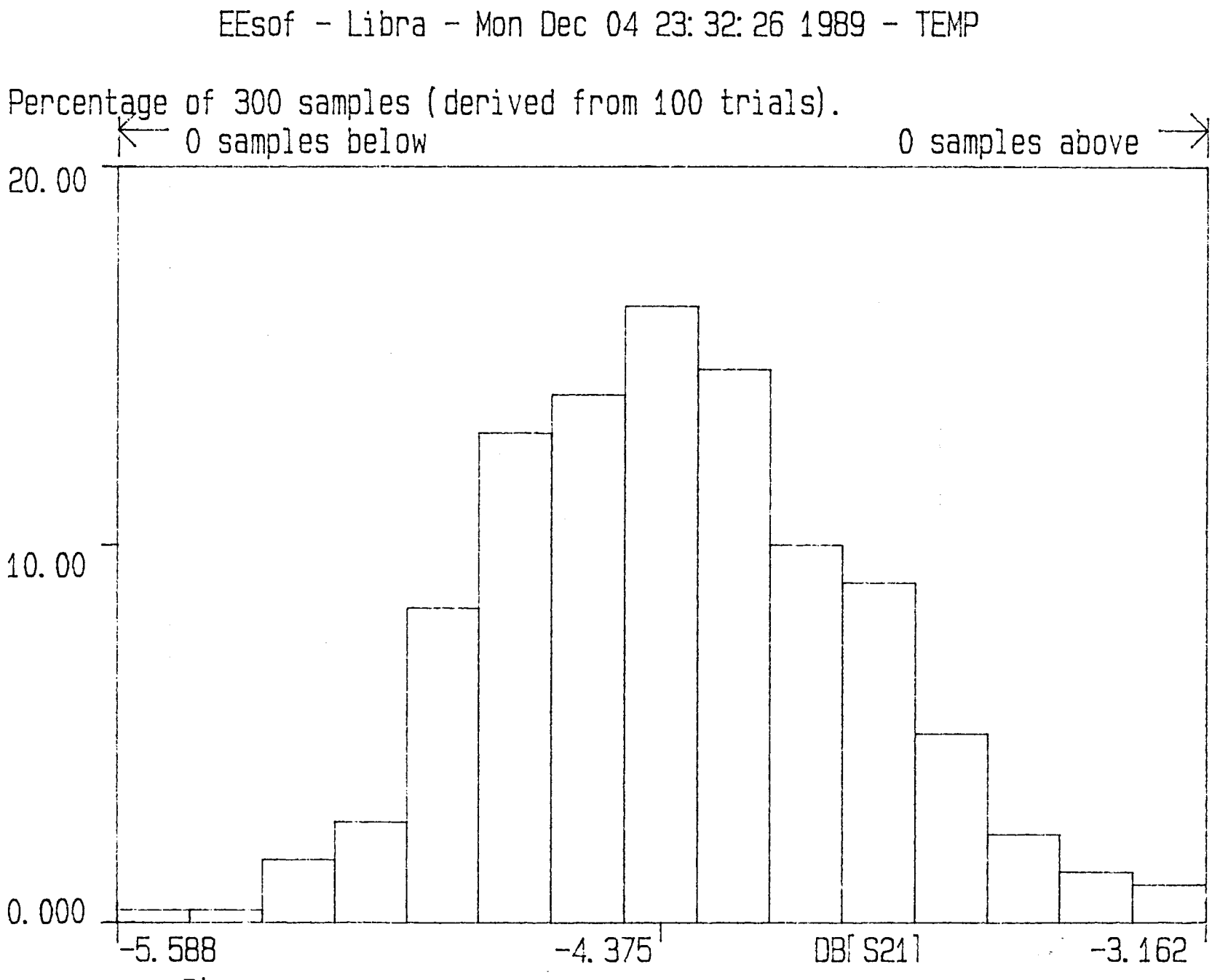


Figure 3-17. Yield based on Insertion Loss Specification @ 2-6 GHz

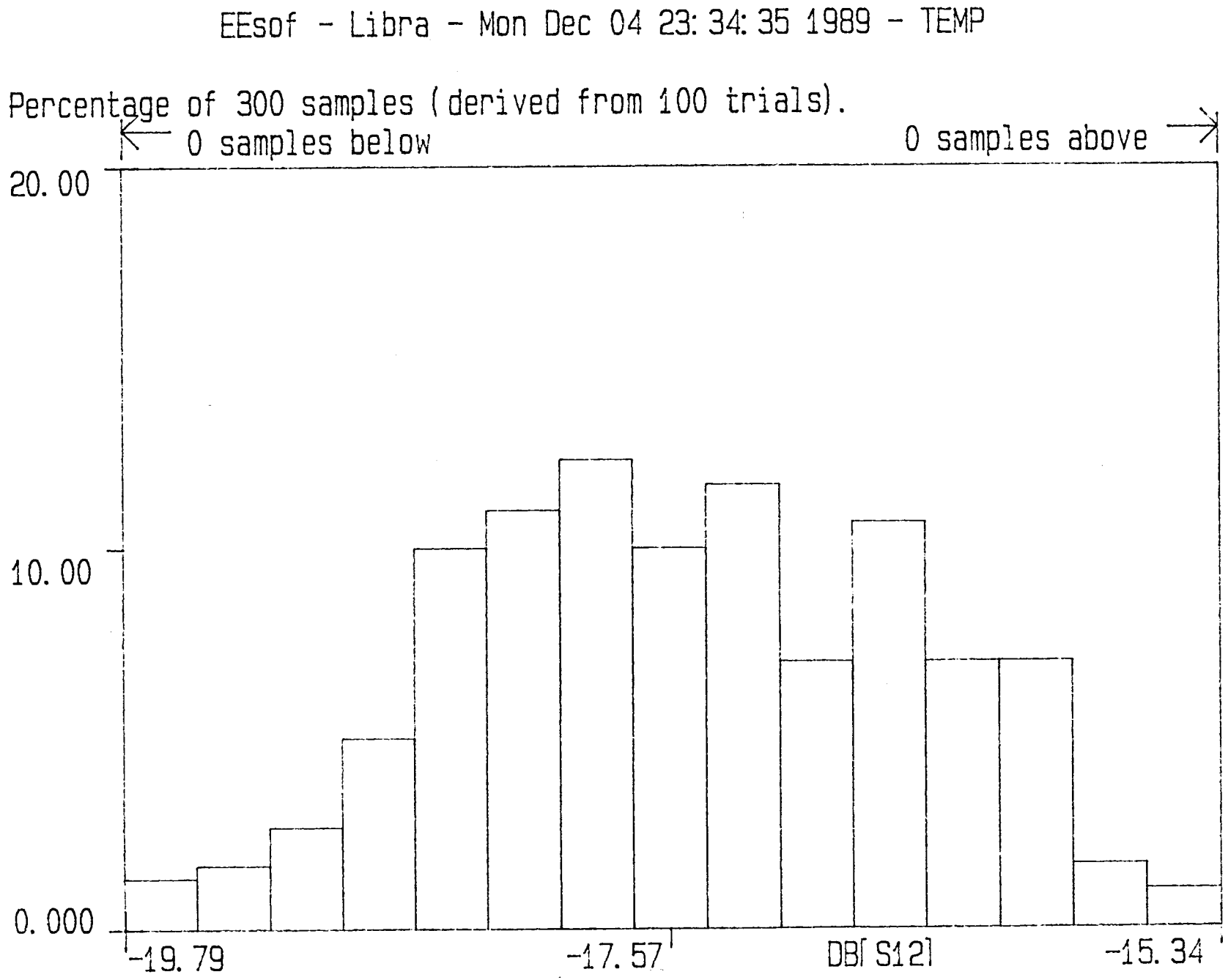


Figure 3-18. Yield based on Isolation Specification @ 2-6 GHz

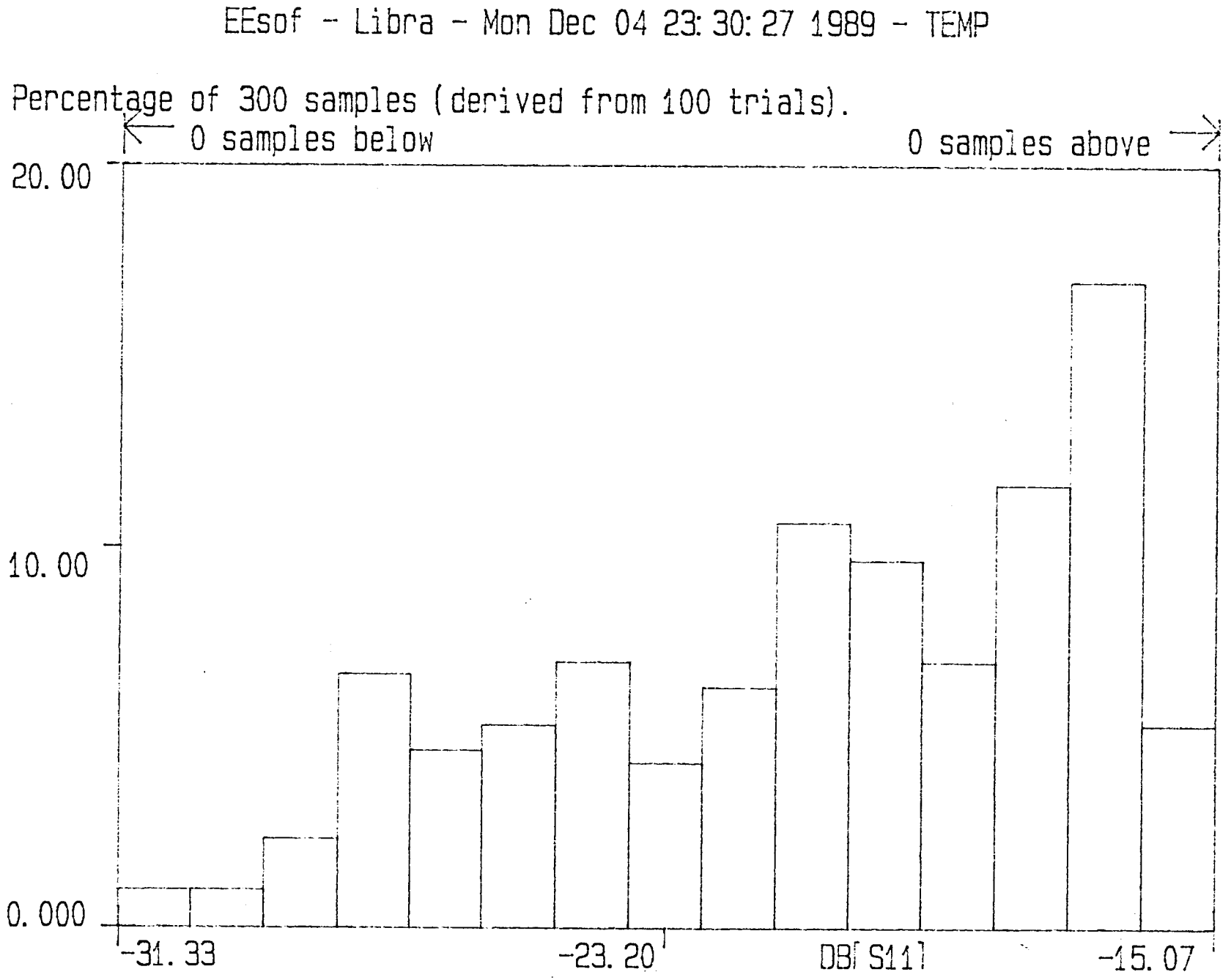


Figure 3-16. Yield based on VSWR Specification @ 2-6 GHz

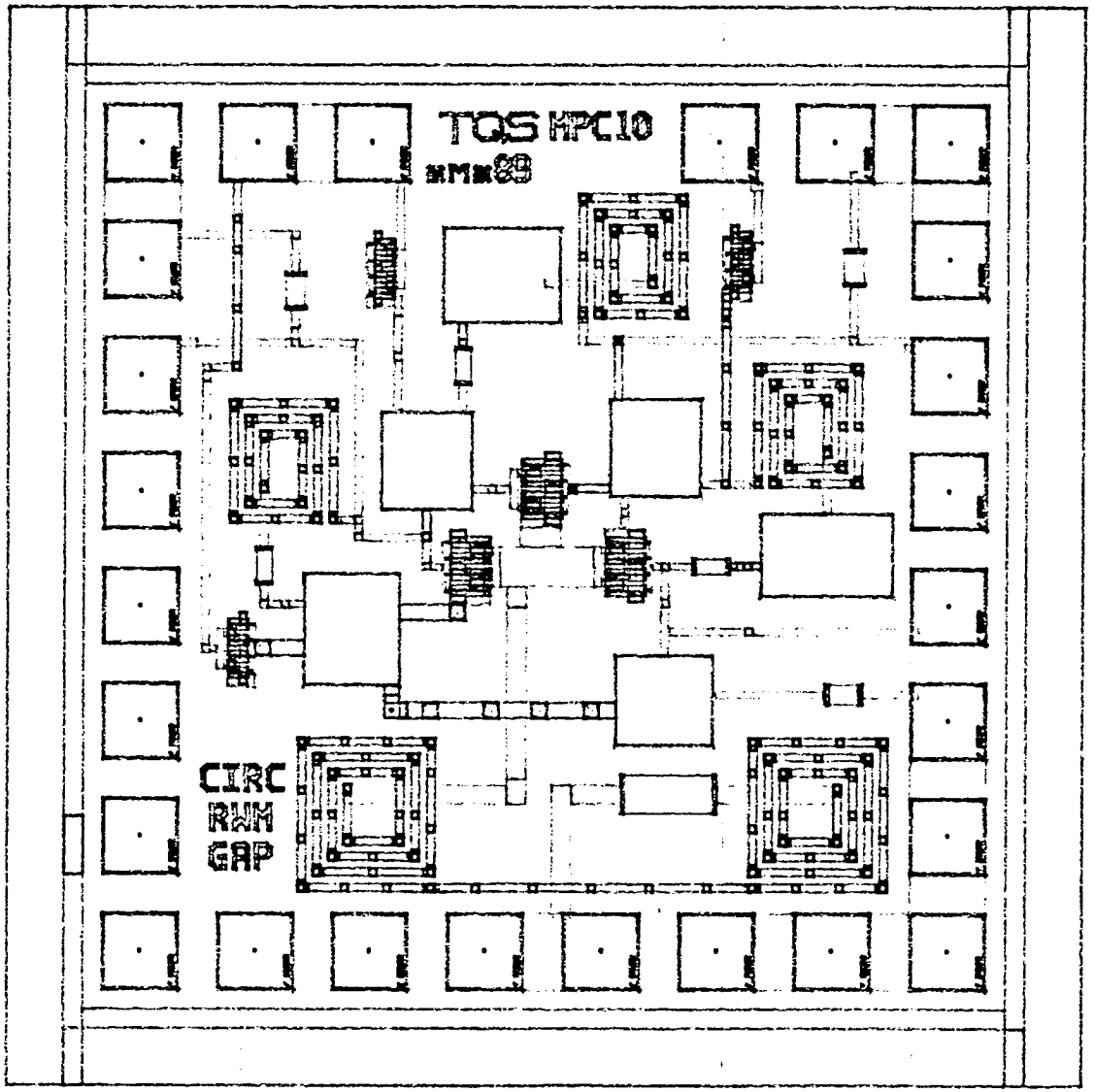


Figure 5-3. Active Circulator Layout

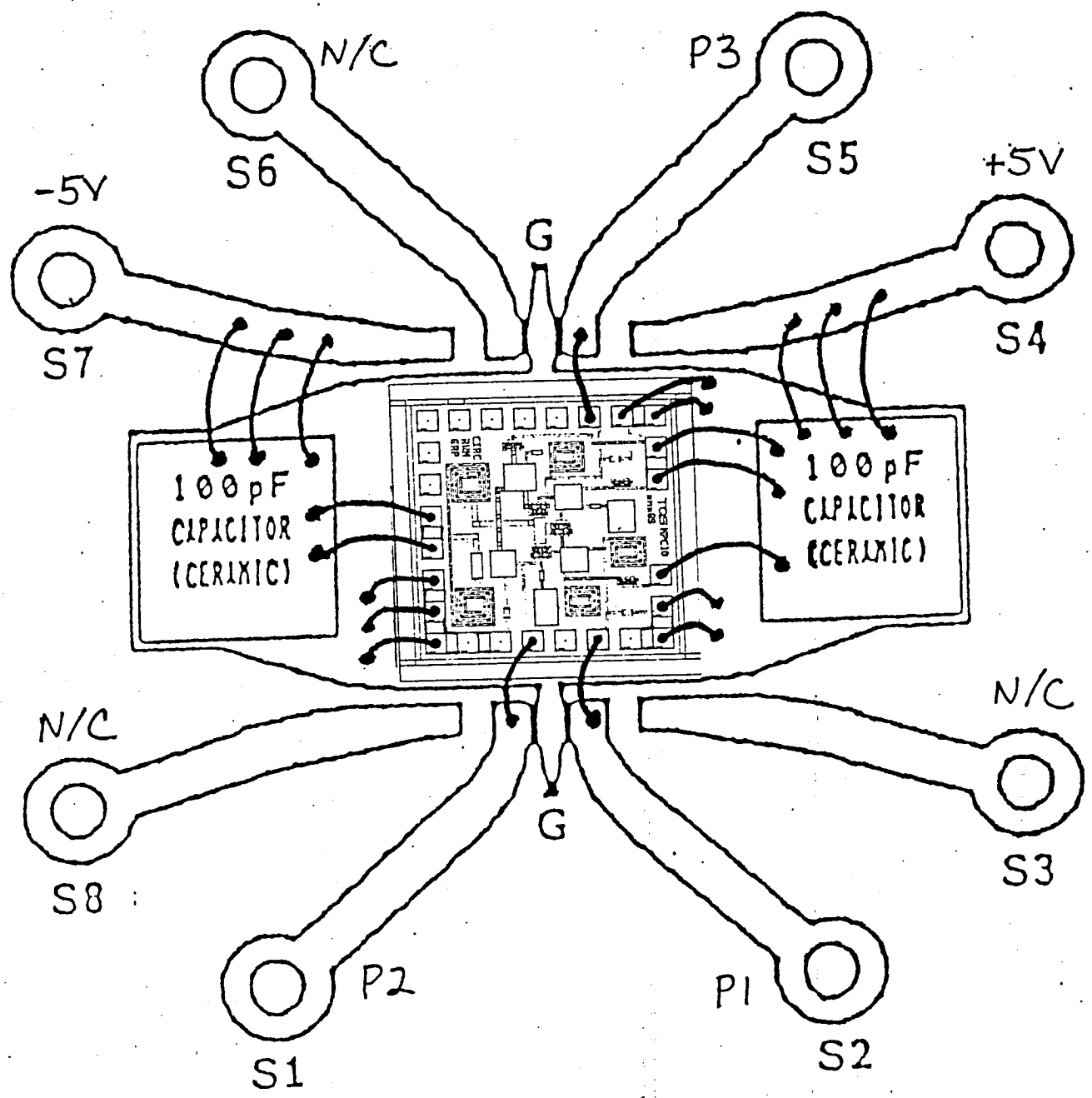


Figure 5-1. Bonding Diagram - Micro View

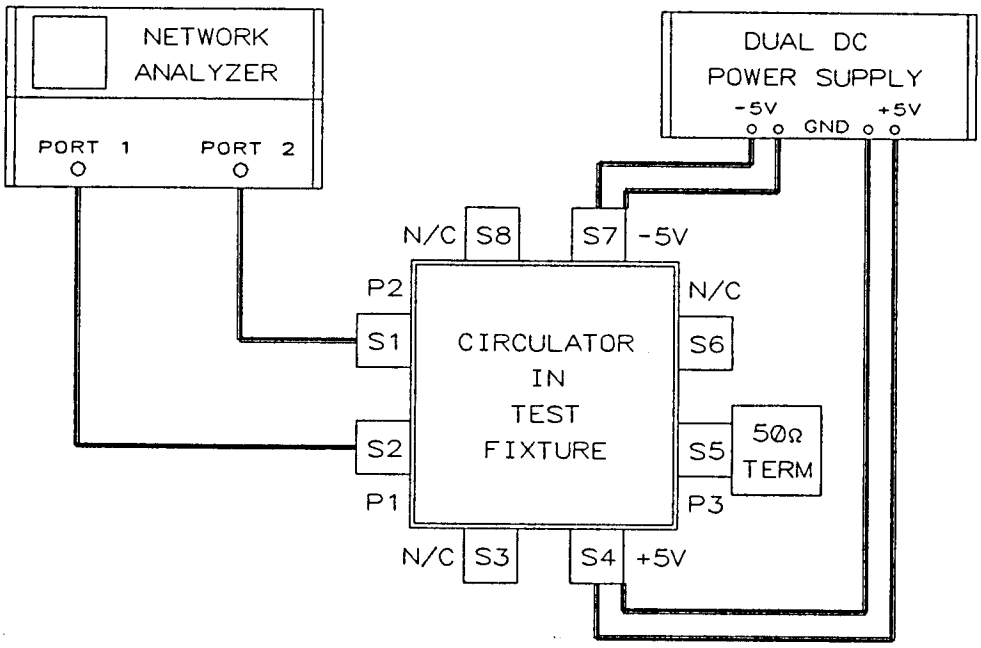


Figure 6-1. Network Analyzer Measurement Setup

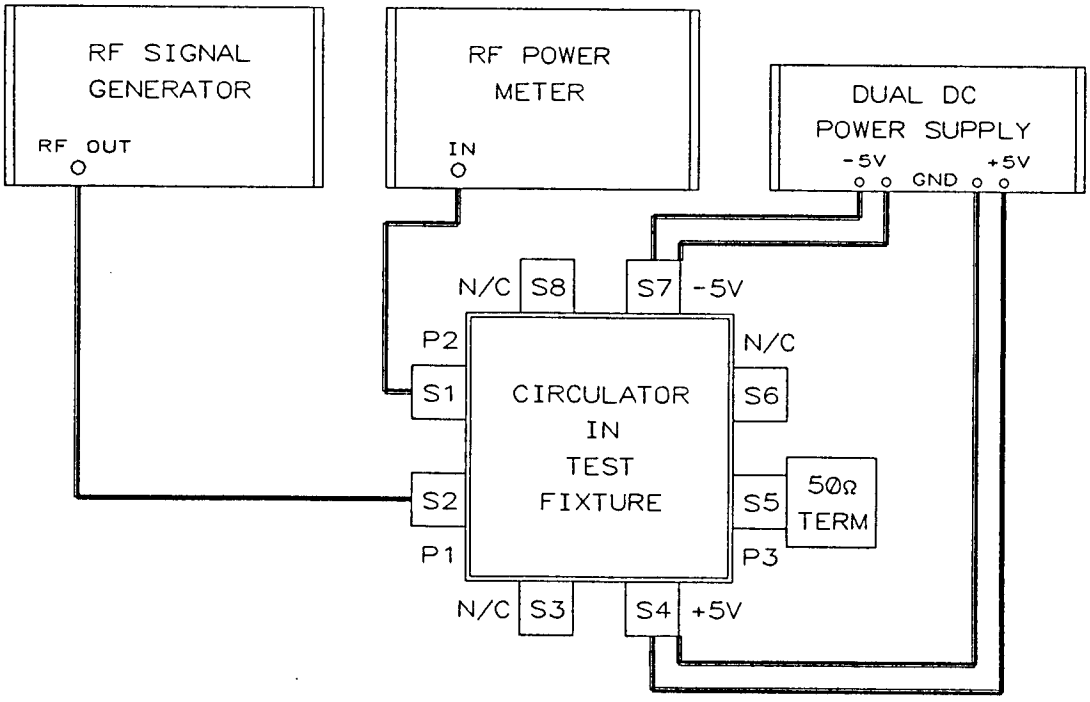


Figure 6-2. Power Meter Measurement Setup

Dec 11th, 1989

MMIC DESIGN

525.787

FINAL PROJECT : MEDIUM POWER AMPLIFIER

By : JASON ROUSSOS
DAVID BOULANGER

APL

INTRODUCTION

CIRCUIT DESCRIPTION :

the medium power amplifier is a two-stage amplifier using a 300u FET at the input and a 1200u FET at the output. the matching circuits are the input, interstage and the output. Active bias are used for each FET to permit the use of external inductor which will block the rest of the package to fit properly.

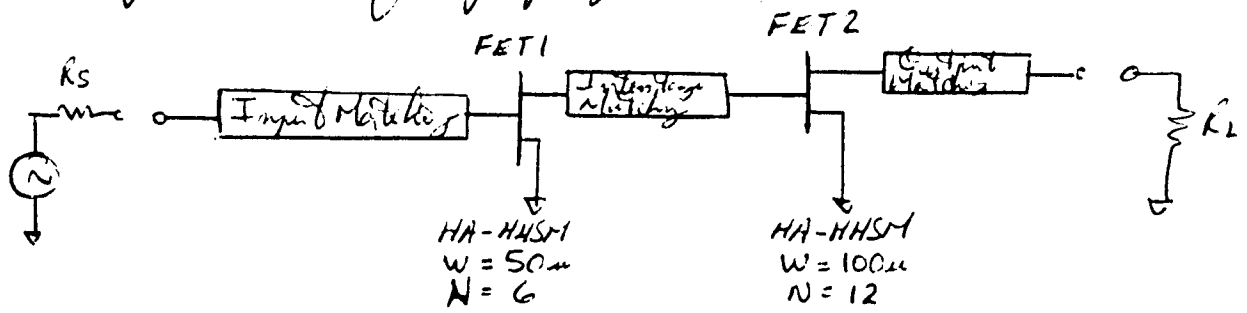


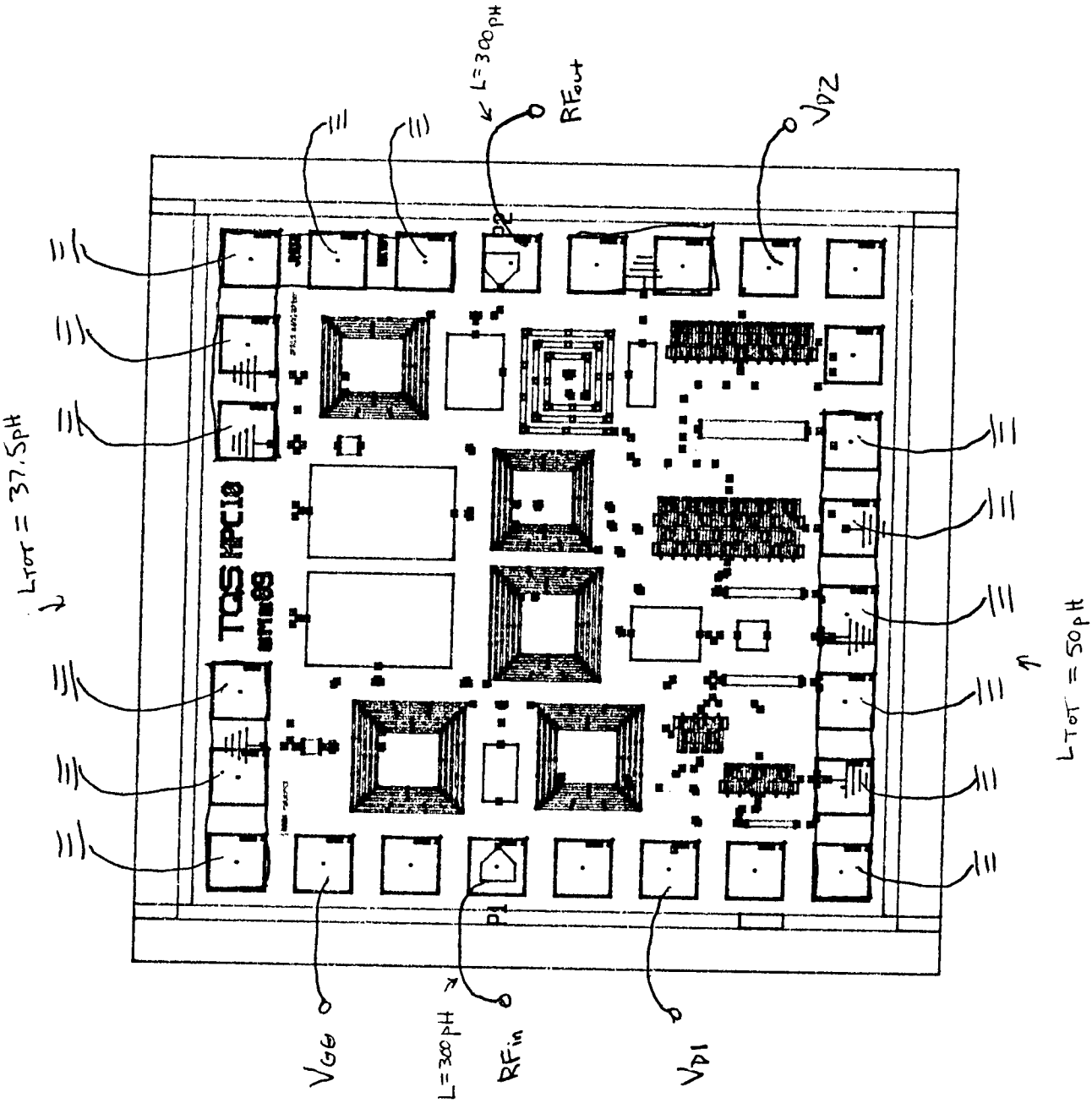
Figure 2.1 MPA RF schematic

the input matching circuit is design to provide good return loss over the band of interest and provide matching to achieve the target gain with an excellent flatness over the band. the output matching circuit is design to provide the required P1dB and reasonable return loss.

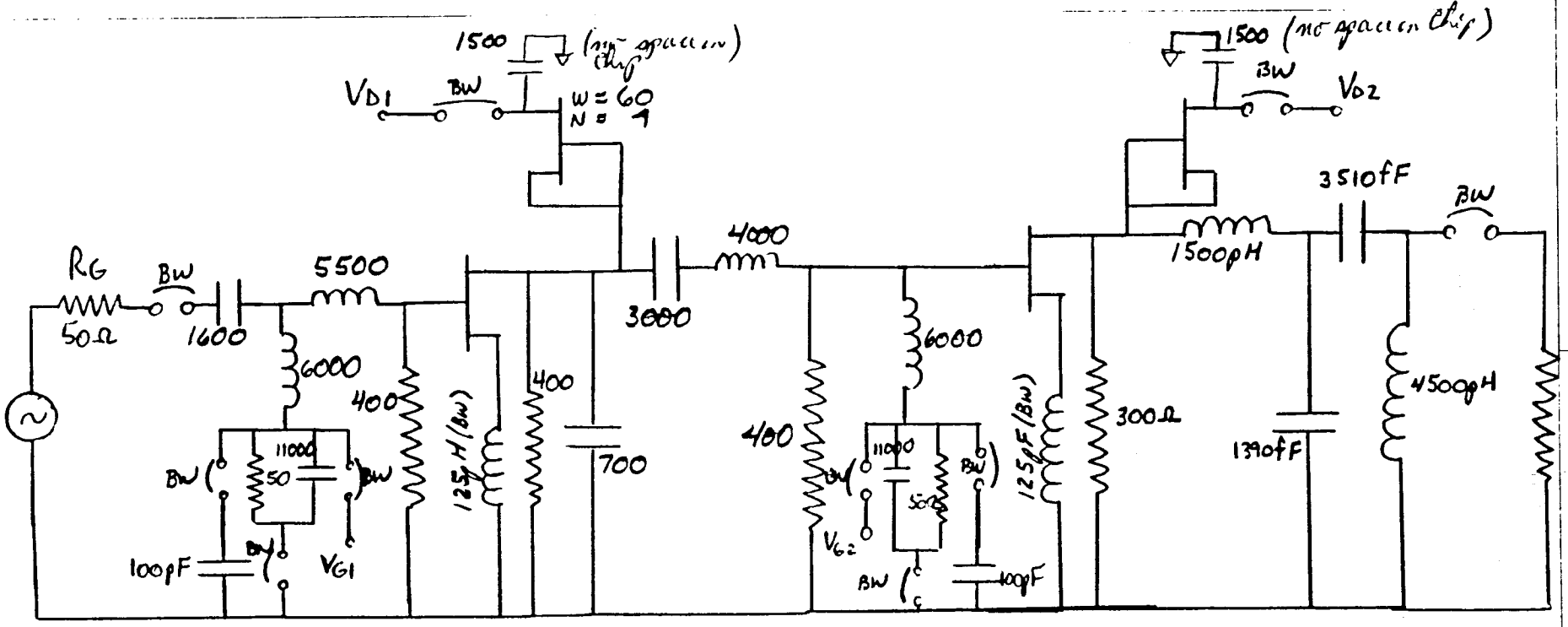
the bias point are selected to provide the output power with reasonably efficiency. But the use of active bias is degrading the efficiency by 33%.

Section 4 – Schematic Diagrams

A schematic diagram is included in the main report for the pre layout circuit. Note the inclusion of bondwire parasitics. A schematic of the post layout circuit is not shown, but the layout and necessary connections (and parasitics resulting from these connections) is shown below



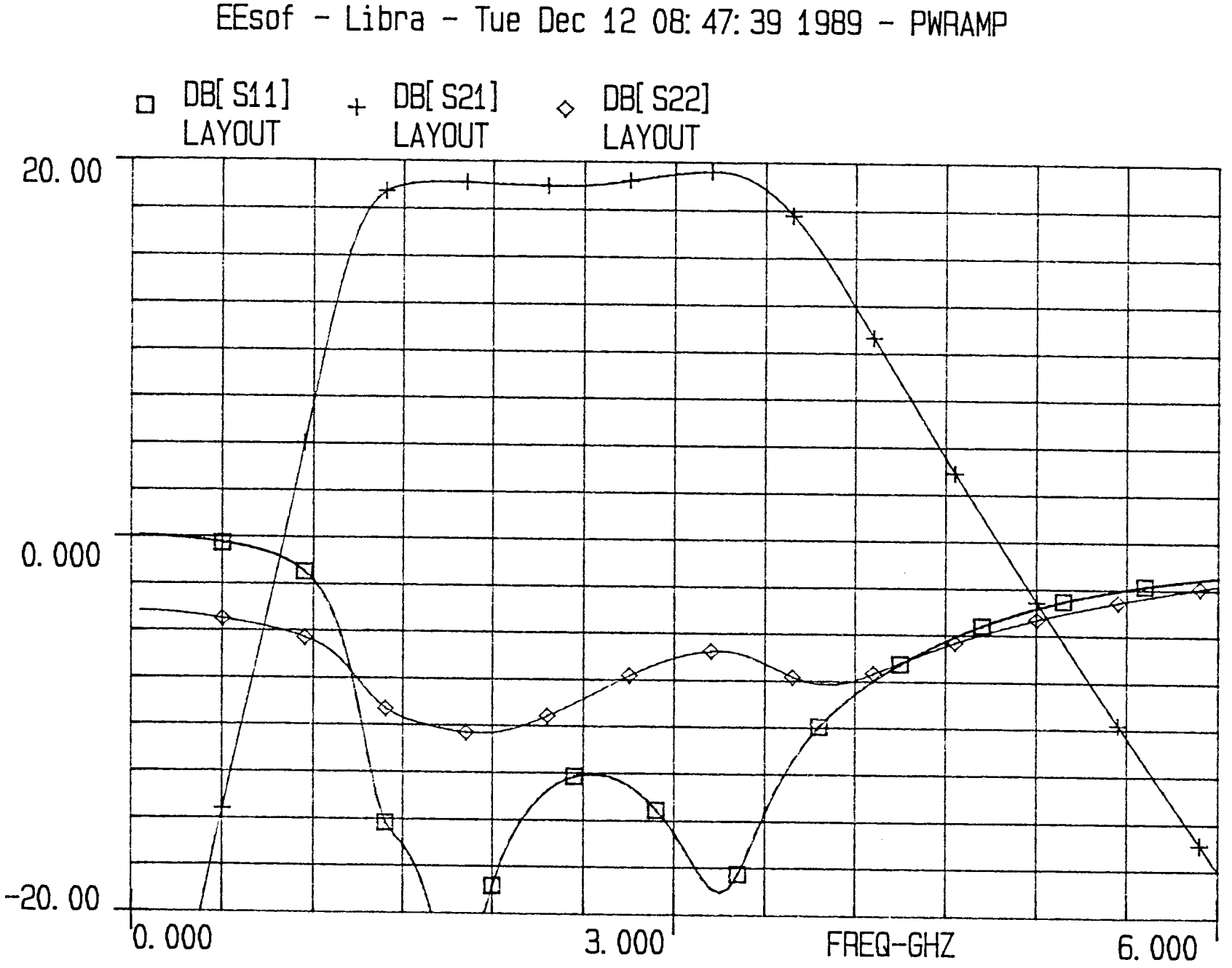
Note that parasitic bondpad capacitances were not included in the simulations due to their minimum effect at 2.5 GHz (as determined in the LNA designs in HW # 5). Each bondwire was assumed to have 300 pH inductance (300 μm length).

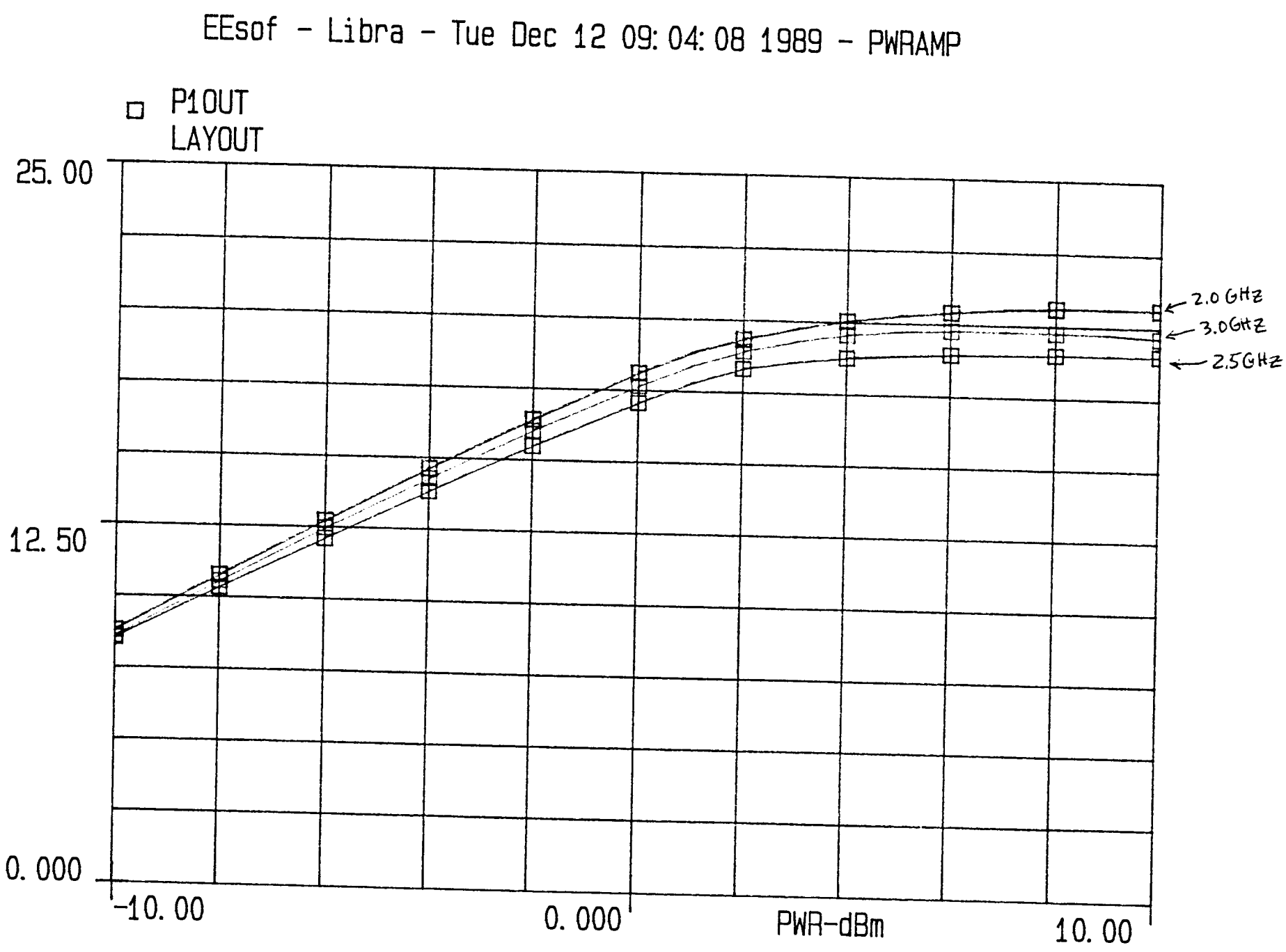


A. SHEMATIC DIAGRAMS

3.- SPECIFICATION COMPLIANCE MATRIX

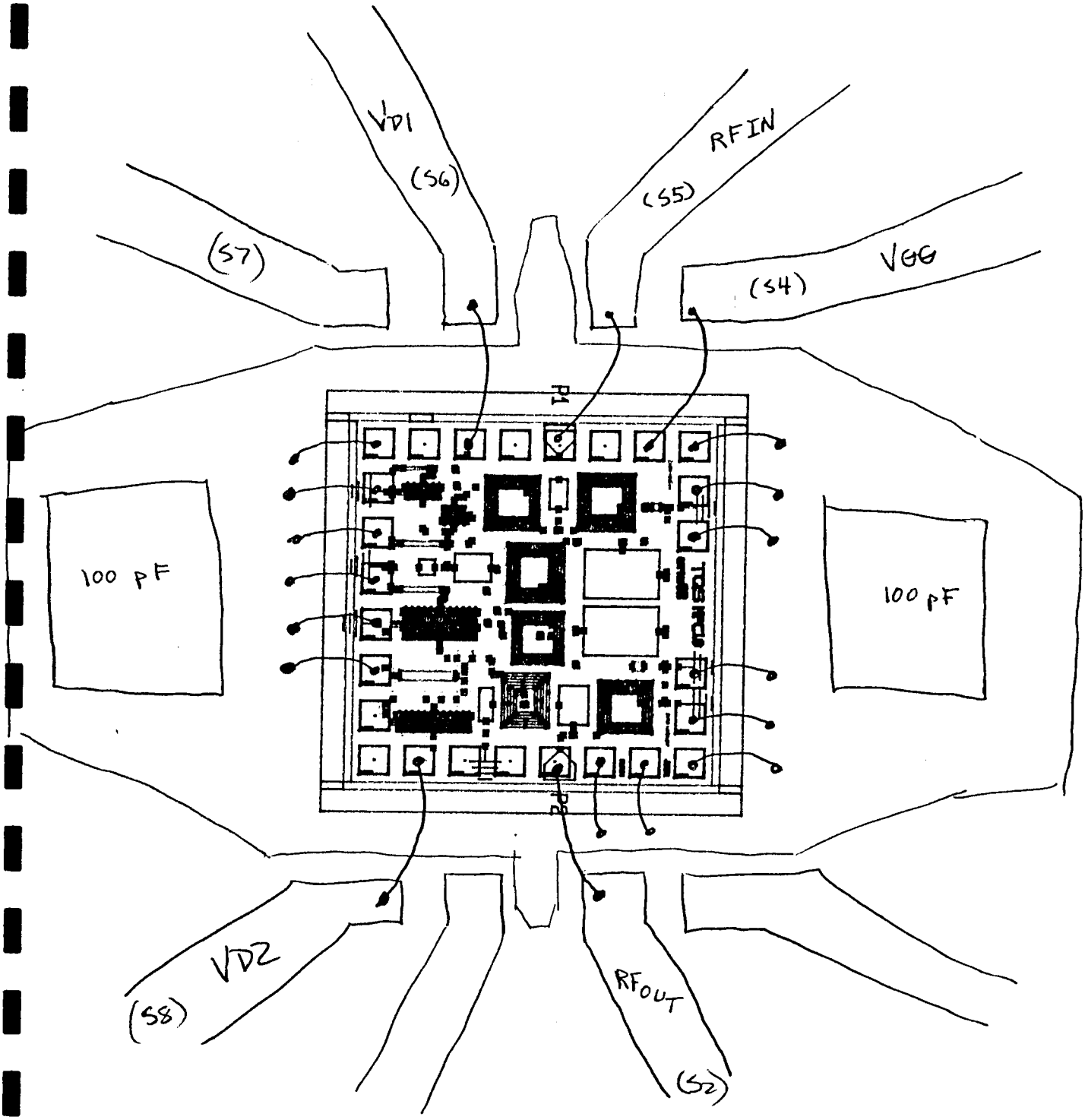
PARAMETER	SPECIFICATION	SIMULATED RESULTS
FREQUENCY	2-3 GHz	1.8-3.2 GHz
GAIN	15 dB MIN	18.5 dB MIN
GAIN RIPPLE	+/- 1dB	± .25 dB
P_{1dB}	+20 dBm MIN	+19dBm ? (using Raytheon model)
I/P R/L	7.5 dB	>12.5 dB
o/p R/L	7.5 dB	> 6.0 dB
η(%) at P_{1dB}	—	9.8 % WITH ACTIVE BIAS 14.7 % WITHOUT ACTIVE BIAS


EEsof - Libra - Tue Dec 12 08:47:39 1989 - PWRAMP
DB[S11]
LAYOUT
DB[S21]
LAYOUT
DB[S22]
LAYOUT
20.00
0.000
-20.00
0.000
3.000
6.000
FREQ-GHZ


EEsof - Libra - Tue Dec 12 09:04:08 1989 - PWRAMP
P1OUT
LAYOUT
25.00
12.50
0.000
-10.00
0.000
10.00
PWR-dBm
2.0 GHz
3.0GHz
2.5GHz

Section 5 - Bonding Diagram

The bonding diagram for the TRI QUINT package is shown below.



The chip will be placed in the TRI QUINT package according to TRI QUINT layout and parasitics manual. The numbers of the traces above must line up with the appropriate SMA connectors on the package.

MMIC DESIGN COURSE

FINAL PROJECT

THE 2db AND 4db STAGES OF A SWITCHED ATTENUATOR

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December 11, 1989

Section 2: INTRODUCTION

The goal of this project was to develop and simulate a switched four stage attenuator. The attenuator stage value requirements were 2, 4, 8, and 16 db which originally were to be cascaded together for varying levels of attenuation between 0db and 30 db. Two teams of two people were working this problem. There were 8 leads available for input and output to the attenuator because of the mounting structure used for the final chip. Because of this, the 2/4 db stages and 8/16d db stages were not cascaded and share voltage control signals. The following write-up details the efforts of the team responsible for the 2db and 4db stages of this attenuator.

Sections 3 and 4: Modeled Performance and Schematic Diagrams

Several possible circuit designs were developed and simulated for this project. Figure 1 provides the three basic circuit types which were simulated and varied in order to achieve the design used in this project. Ultimately Figure 1c was the best performer; Figure 2 provides a detailed circuit diagram of the ideal elements used to form the attenuator stages. The same FETs were used in both stages and only the pad resistors needed to be varied to provide the needed attenuation levels. Figure 3 provides the circuit schematic representing the same circuit using Triquint NiCr resistors. Since the minimum value for these resistors was 25 Ohms, several resistors had to be placed in parallel to form the proper resistive values for each pad.

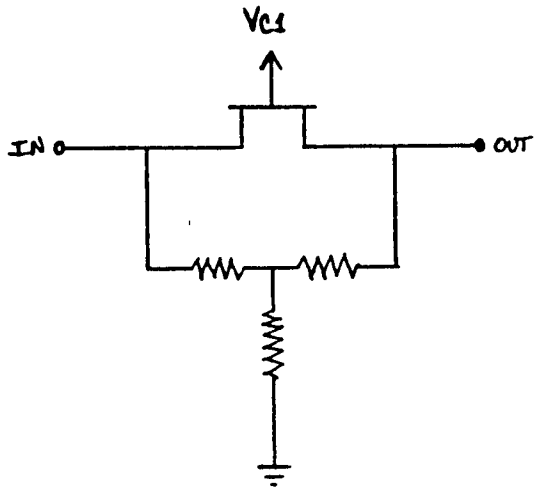
In all simulations except the intermodulation performance analysis, a linear model made up of scaled ideal lumped components was used to provide the characteristics of the 300 and 150 micron FETs used in these circuits. This was done since the FETs are being used as switches with the input on the drain and the output on the source. For both FETs two linear models were used. One model represents the FET characteristics when it is on and the other is used for the off condition. Figure 4 provides the schematic diagram of the linear FET model used in these analyses as well as the baseline values which are scaled in order to model the 150 micron FET.

To assess the 3rd order intermodulation intercept point of the circuit The Raytheon-Statz model of each FET was used and only the 0 db attenuator configuration was evaluated. This is because it is assumed that the characteristics of the attenuator stage bypass FETs will drive the worst-case intermodulation intercept.

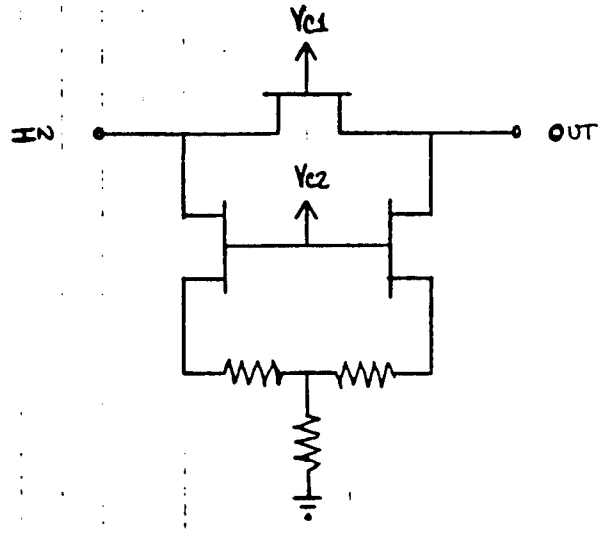
Table 1 provides a summary of the various pertinent design simulation results. Table 2 provides the yield analysis results of the final circuit simulation.

FIGURE 1

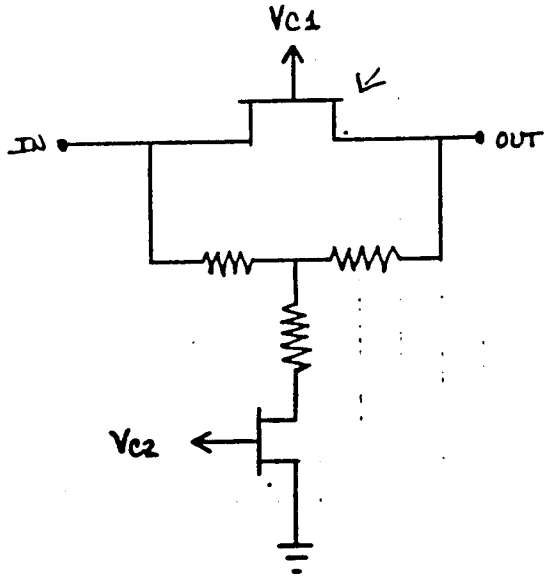
BASIC ATTENUATOR TYPES EVALUATED FOR 2/4 db ATTENUATOR STAGES



(a)



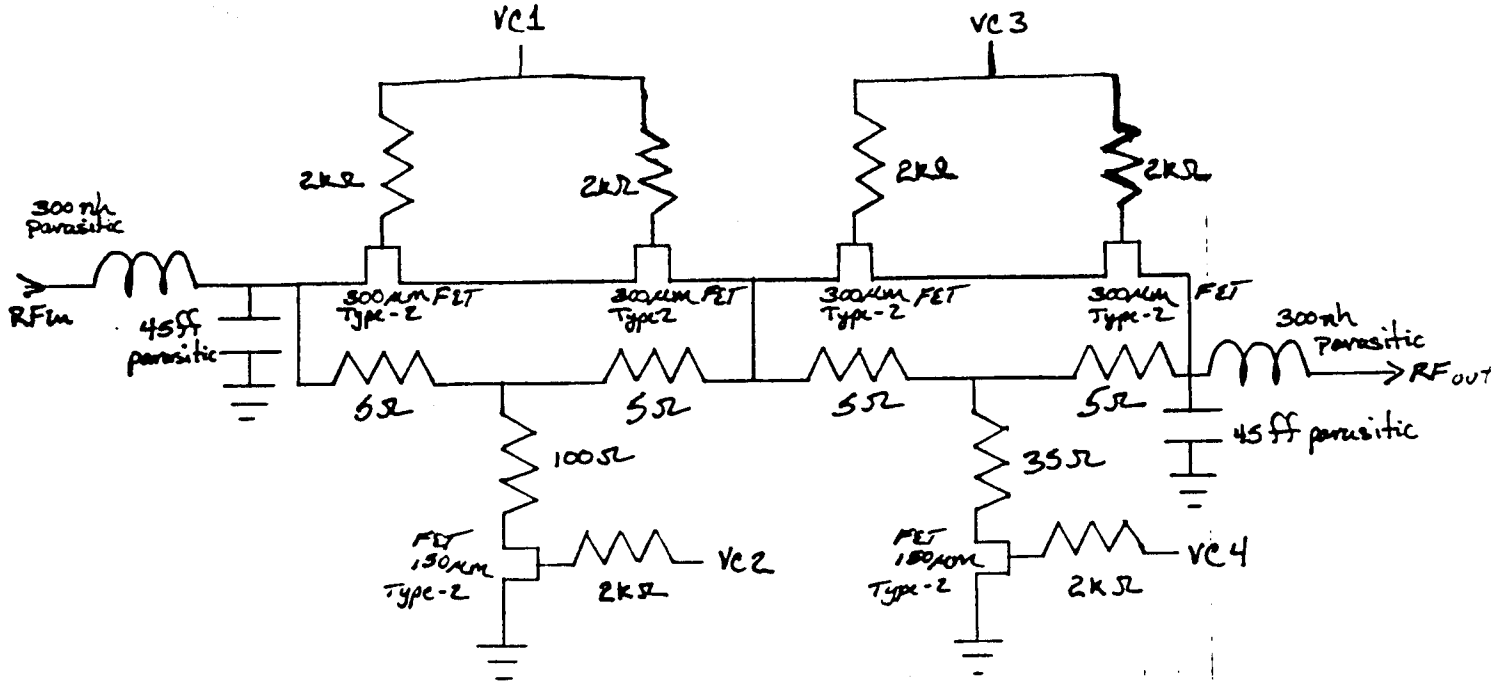
(b)



(c)

FIGURE 2

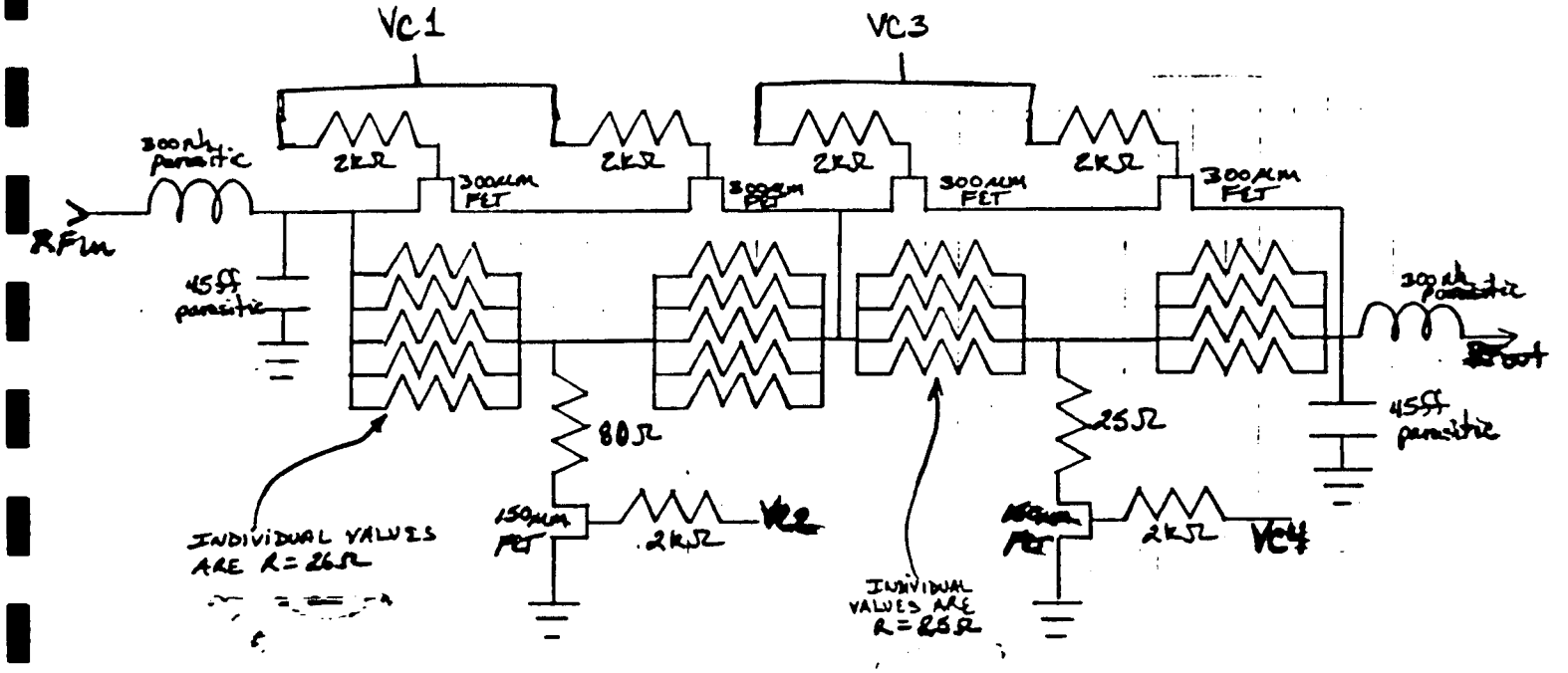
DETAILED SCEMATIC OF SIMULTED 2/4 db ATTENUATOR STAGES



USING IDEAL ELEMENTS

FIGURE 3

DETAILED SCHEMATIC OF 2/4 db ATTENUATOR STAGES USING TQ NiCr RESISTOR



USING TRIQUINT NiCr RESISTORS

Attenuator Values Normalized to Insertion Loss
Using Process Block

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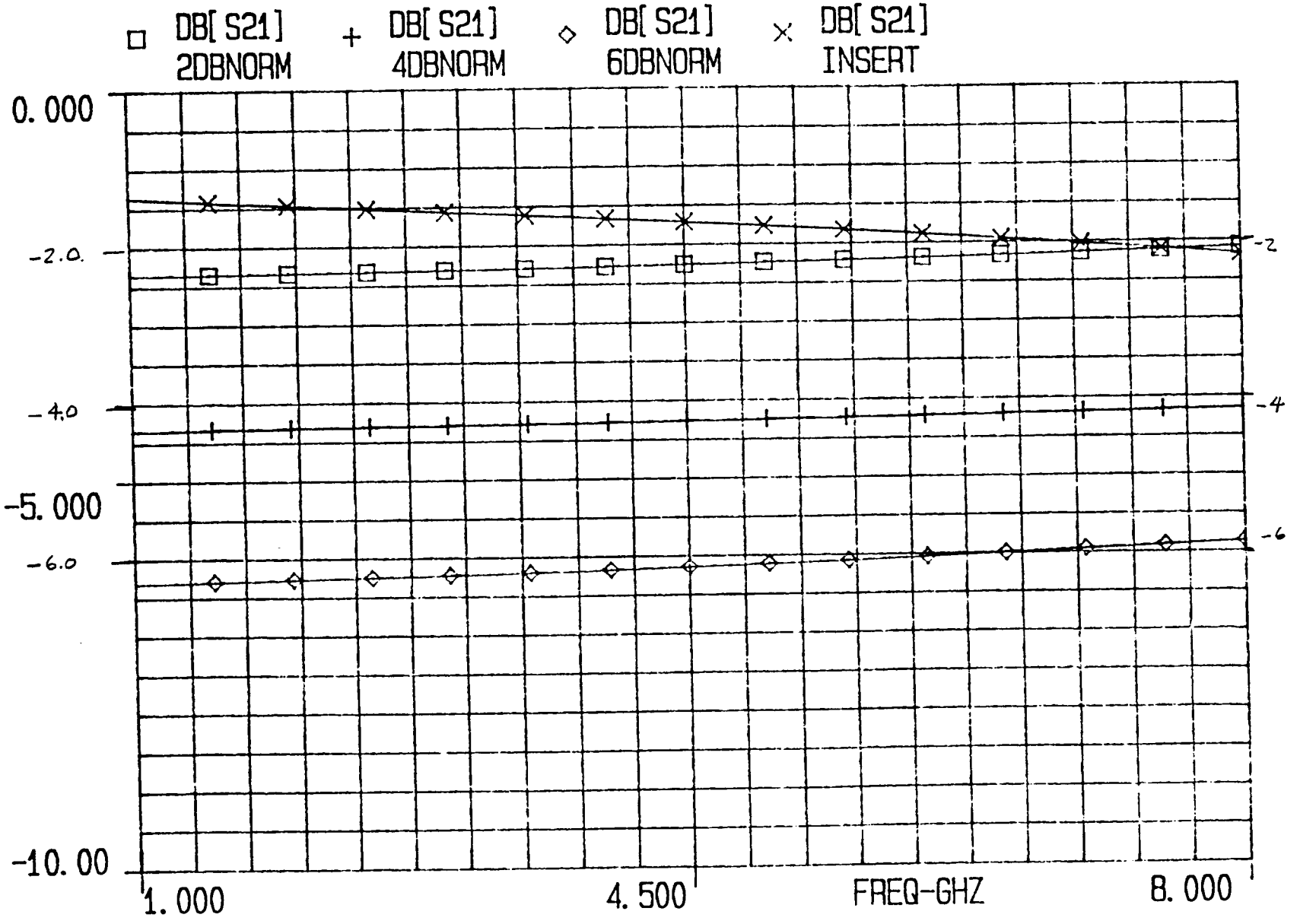
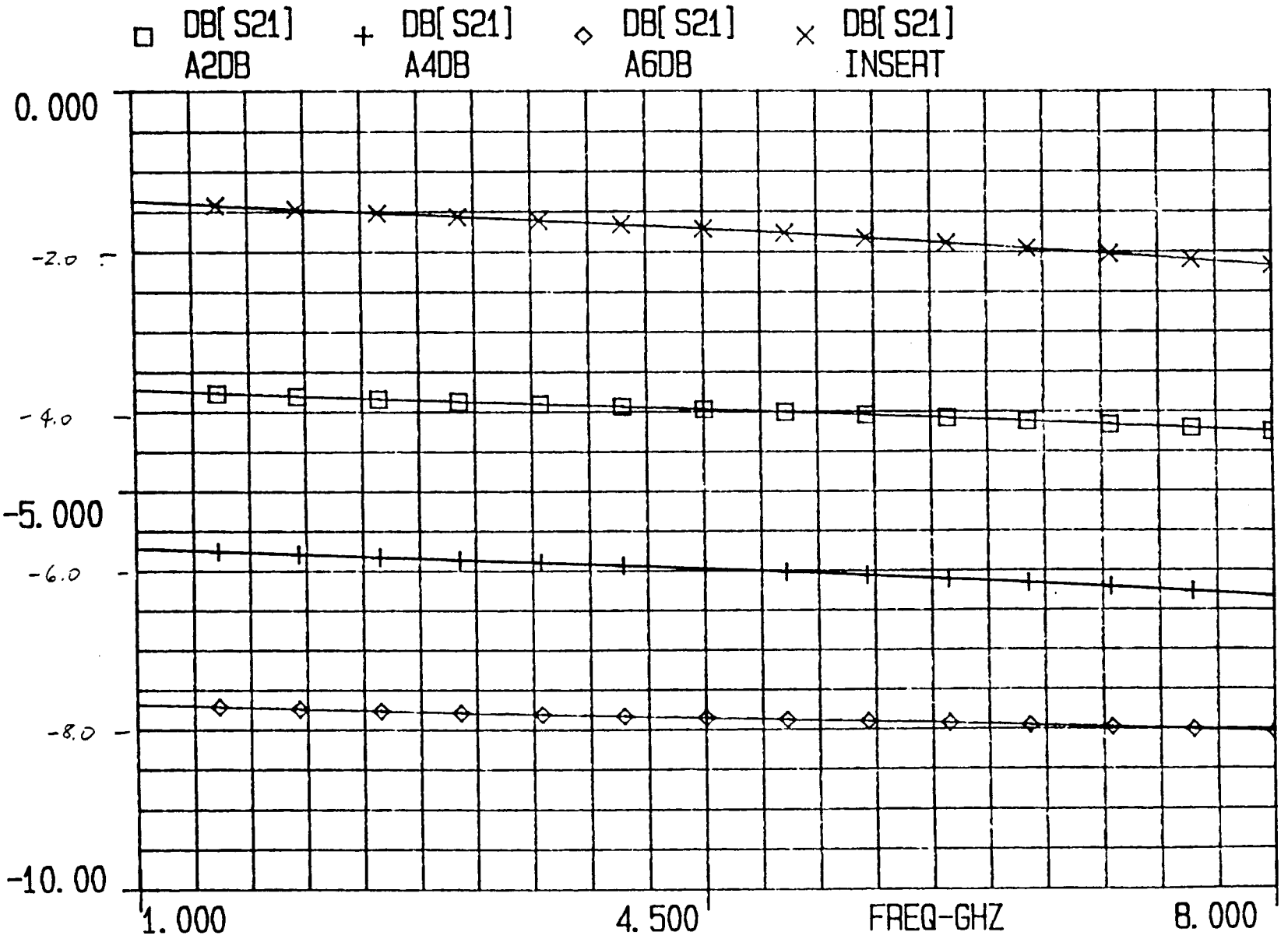
Relative Ins. Loss

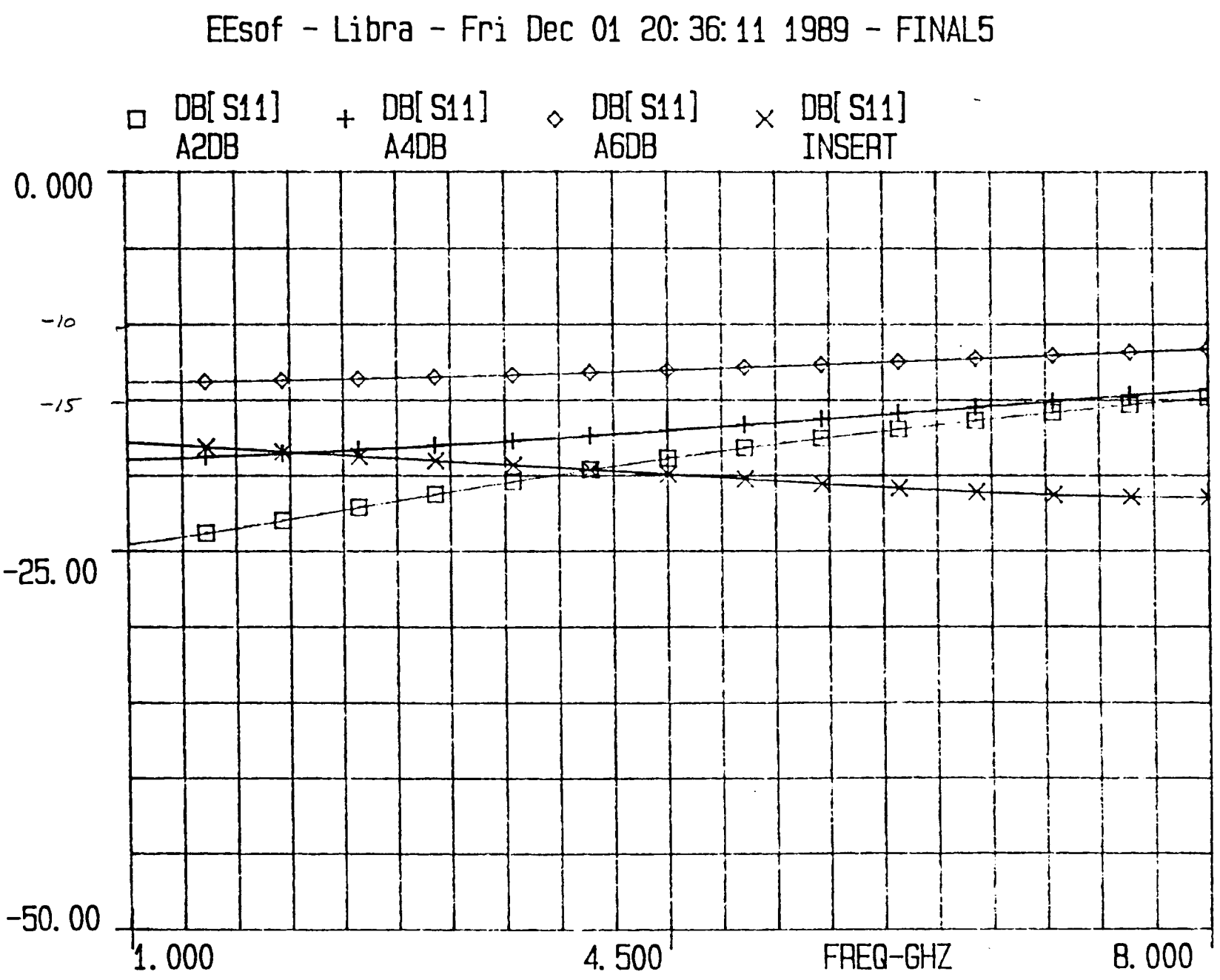


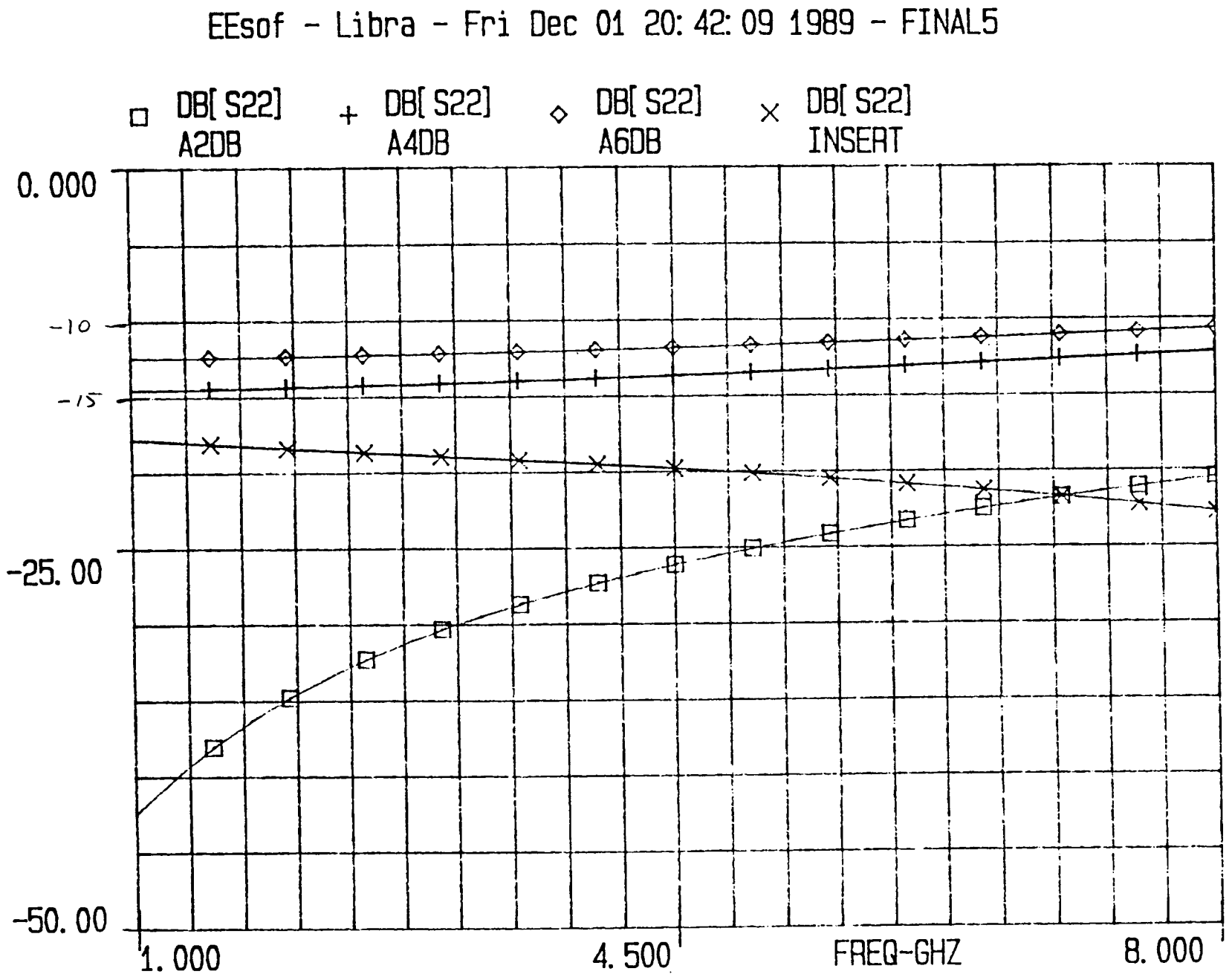
Non-Normalized Attenuator Results

Absolute Ins. Loss

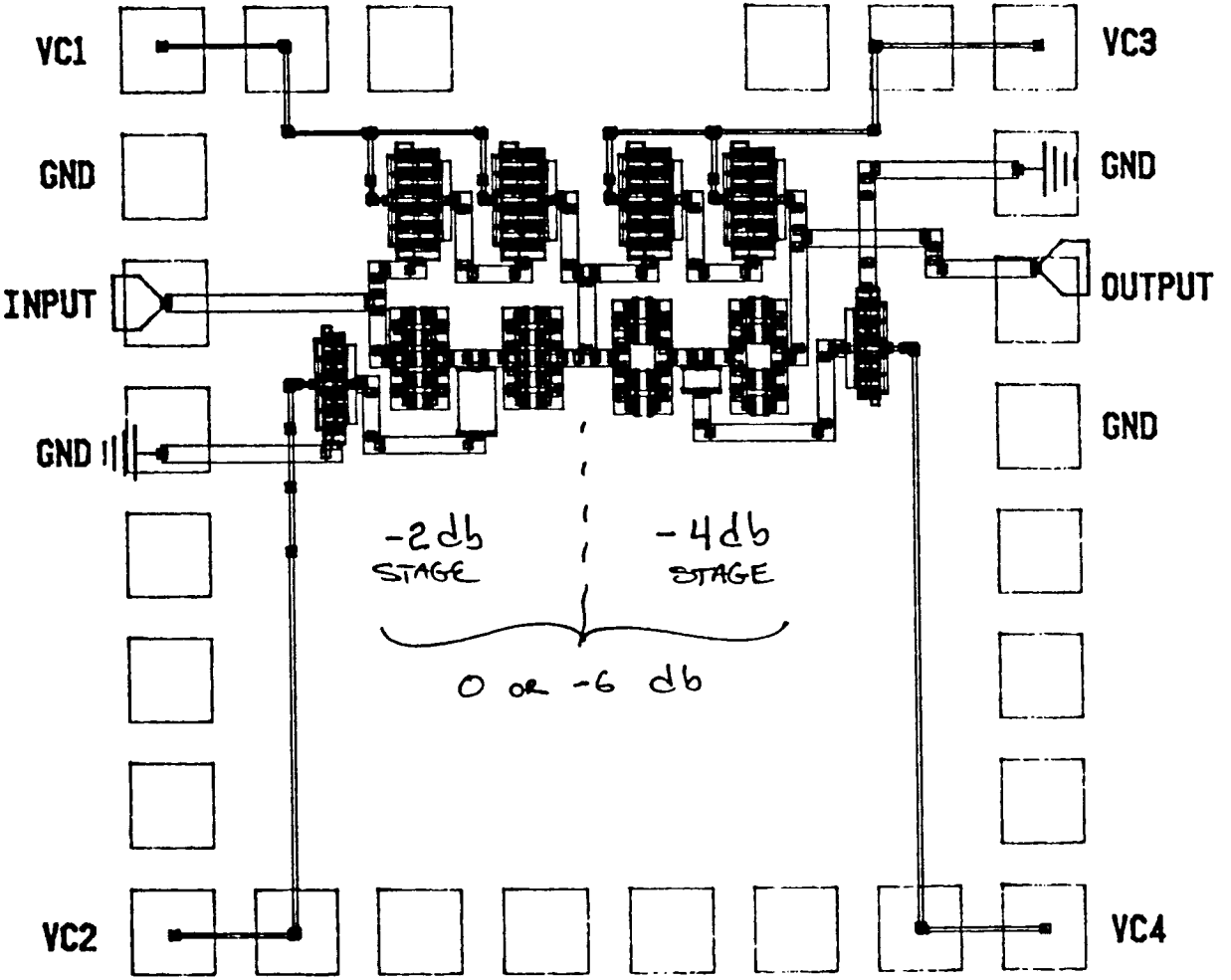
EEsof - Libra - Fri Dec 01 20:58:46 1989 - FINAL5




EEsof - Libra - Fri Dec 01 20:36:11 1989 - FINAL5
DB[S11] A2DB
DB[S11] A4DB
DB[S11] A6DB
DB[S11] INSERT
0.000
-10
-15
-25.00
-50.00
1.000
4.500
8.000
FREQ-GHZ


EEsof - Libra - Fri Dec 01 20:42:09 1989 - FINAL5
DB[S22] A2DB
DB[S22] A4DB
DB[S22] A6DB
DB[S22] INSERT
0.000
-10
-15
-25.00
-50.00
1.000
4.500
8.000
FREQ-GHZ

— CIRCUIT SIMULATED IN LAOUT —

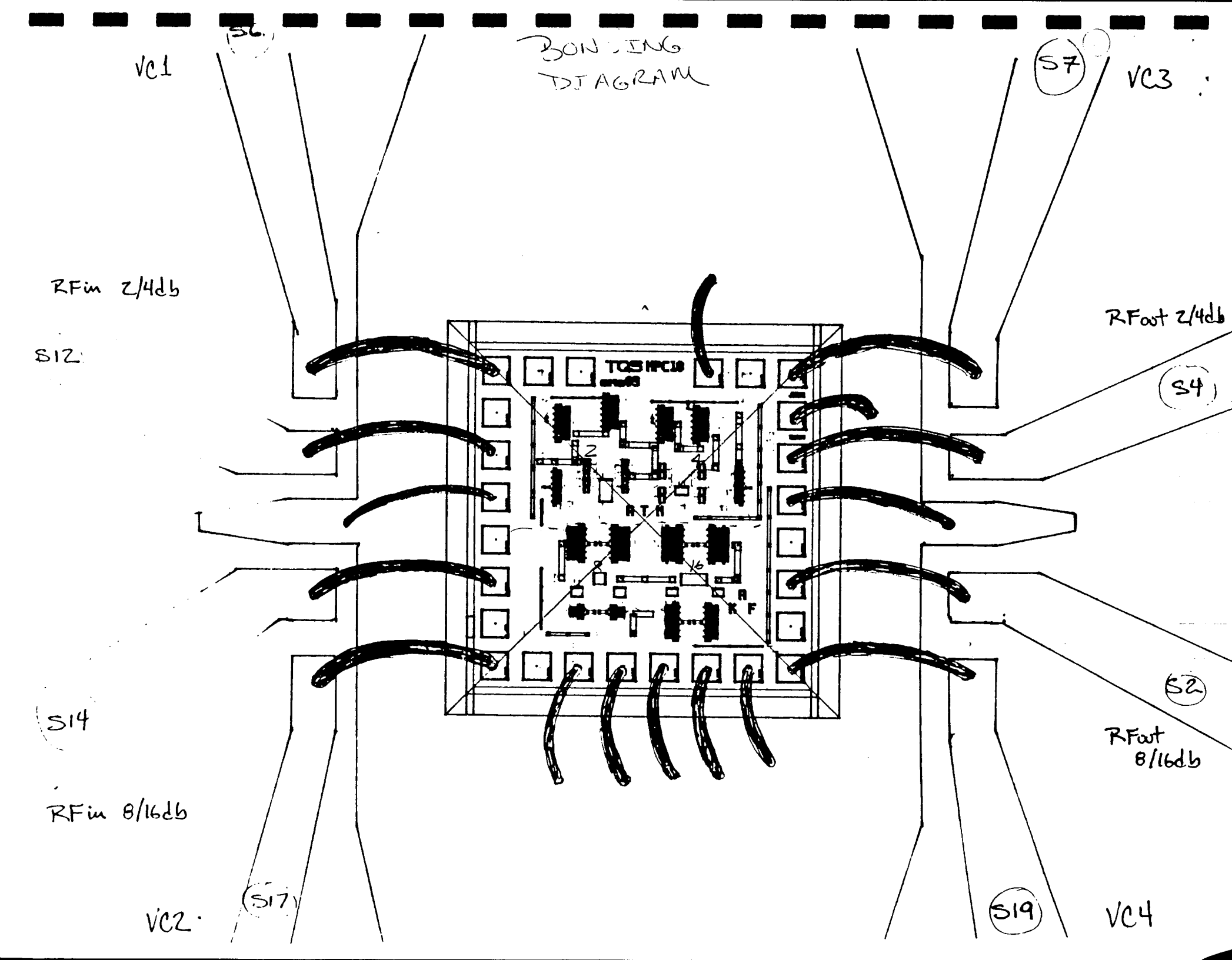


0 db : VC1 = 0Vdc, VC2 = -4Vdc, VC3 = 0Vdc, VC4 = -4Vdc

2 db : VC1 = -4Vdc, VC2 = 0Vdc, VC3 = 0Vdc, VC4 = -4Vdc

4 db : VC1 = 0Vdc, VC2 = -4Vdc, VC3 = -4Vdc, VC4 = 0Vdc

6 db : VC1 = -4Vdc, VC2 = 0Vdc, VC3 = 0Vdc, VC4 = 0Vdc


BONDING DIAGRAM
VC1
S6
S7
VC3
RFin 2/4db
S12
RFout 2/4db
S4
S14
S2
RFout 8/16db
RFin 8/16db
VC2
S17
S19
VC4

8 AND 16 DB

SWITCHED ATTENUATOR

MARK PACEK

KEVIN FAISON

12/11/89

Circuit Description

The 8 and 16 dB attenuator circuit is made up of two switched resistive PI networks connected in series (figure 1). Each attenuator section requires two control voltages. The thru path (no attenuation) is selected by turning the series FETs on (V+=0V) and the shunt FETs off(V-=-4V). The PI's are switched in when the shunt FETs are on (V1-=0V) and the series FETs are off (V1+=-4V). The shunt resistors have been adjusted to account for the drain to source resistance of shunt FETs. FET widths were selected on the basis of the output the intercept point requirement (OP3) and then optimized for RF performance. The circuit was designed using the latest in CAD software including TOUCHSTN for linear analysis, LIBRA for non-linear harmonic balance analysis and PSPICE for initial ouput compression point estimates. The circuit meets all performance goals, consumes minimal chip area and is process tolerant.

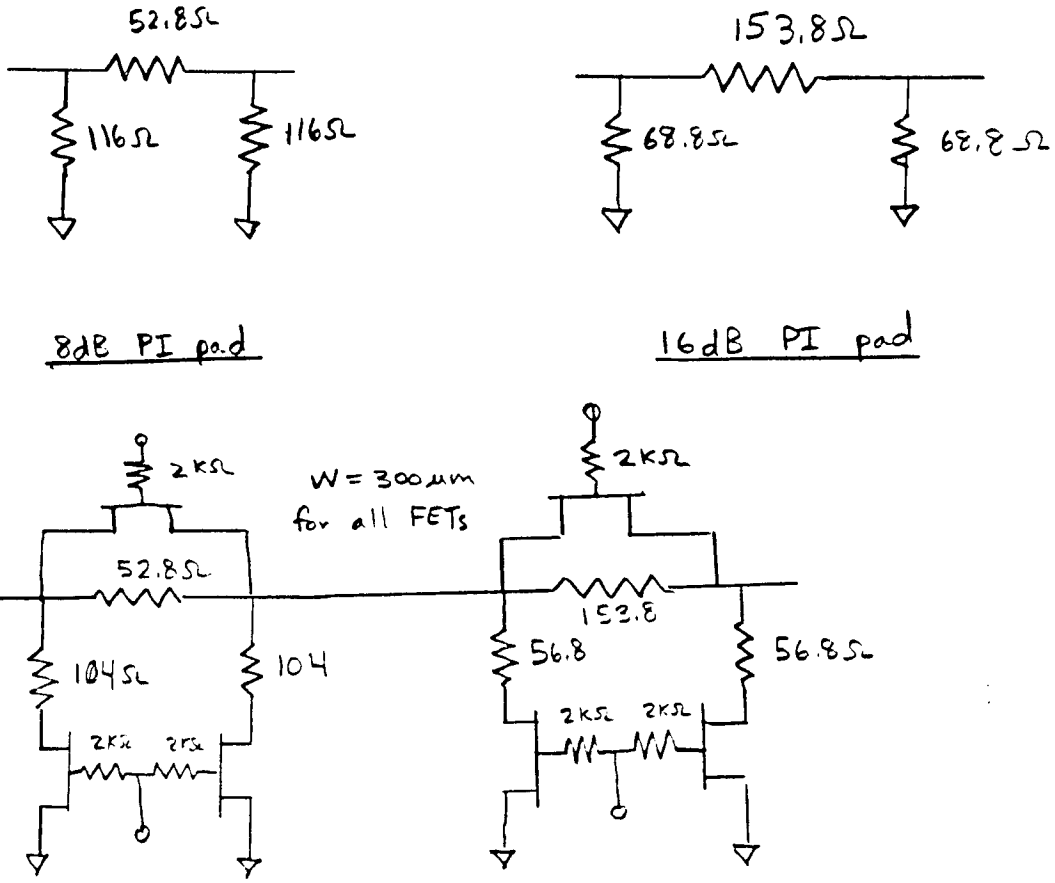
Design Philosophy and trade-offs

The PI topology was one of three considered for the MMIC attenuator design. The others were the switched TEE and the switched path attenuators. The switched TEE network (figure 2) is the dual to the switched PI. It has a slight advantage in requiring one less resistor. It's main disadvantage for this application is the small size of the shunt resistor since the shunt FET resistance becomes the dominant resistance in the branch. Because Rds of the TQFET has a 3 sigma process variation of 14% vs. 3% for a NICR resistor, the accuracy of the TEE attenuator (for the 8 and 16dB case) is less process tolerant than the PI attenuator.

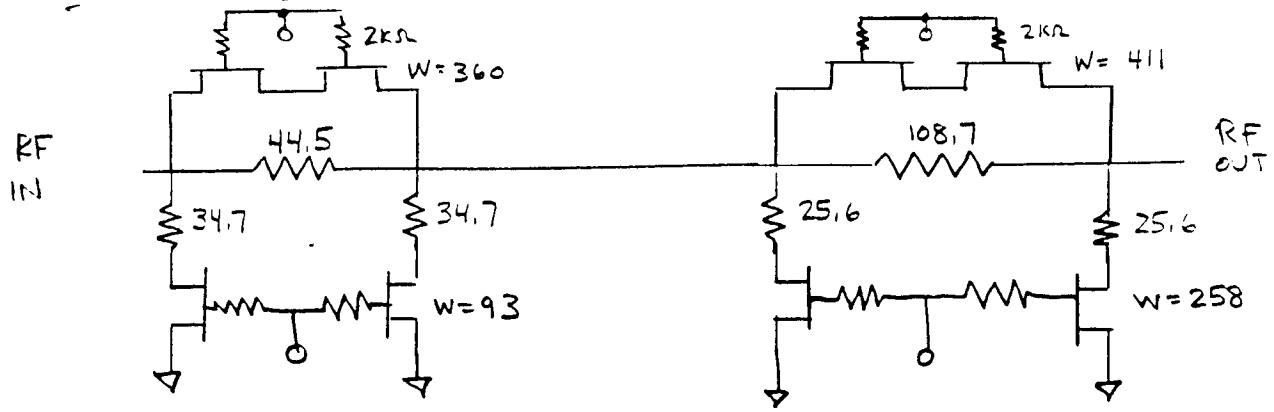
The switched path attenuator (figure 3) is made up of two back to back SPDT switches and a resistive pad. The two RF paths are identical with the exception of the the resistive TEE which is used to give the desired attenuation step. The number of FETs in the thru and attenuation path are the same. Since any variation in the FET switch parameters will be seen by both paths the attenuation step accuracy will be mostly dependent on control of the NICR resistors. Thus this circuit is excellent in terms of being process tolerant. This symetry also offers advantages in phase response. This attenuator showed very little phase shift between attenuation states whereas the PI attenuator had 40 degrees of shift between the 0 dB and 24 dB attenuation states at 8 GHz. Disadvantages between the switched path attenuator and the PI attenuator include increased complexity and area (16 FETS total vs. 8 for the PI), higher insertion loss, and a slightly lower output intercept point (OP3). This circuit could not be made to fit on the chip.

Process Sensitivity

The prime contributor to variation in attenuation accuracy in the switched PI attenuator is variation in the on resistance of the FETs. Simulations were performed in which the FET gate widths were allowed to vary +/-10 percent. The worst case variation from the simulation with nominal components was found to be +/- 0.4 dB.



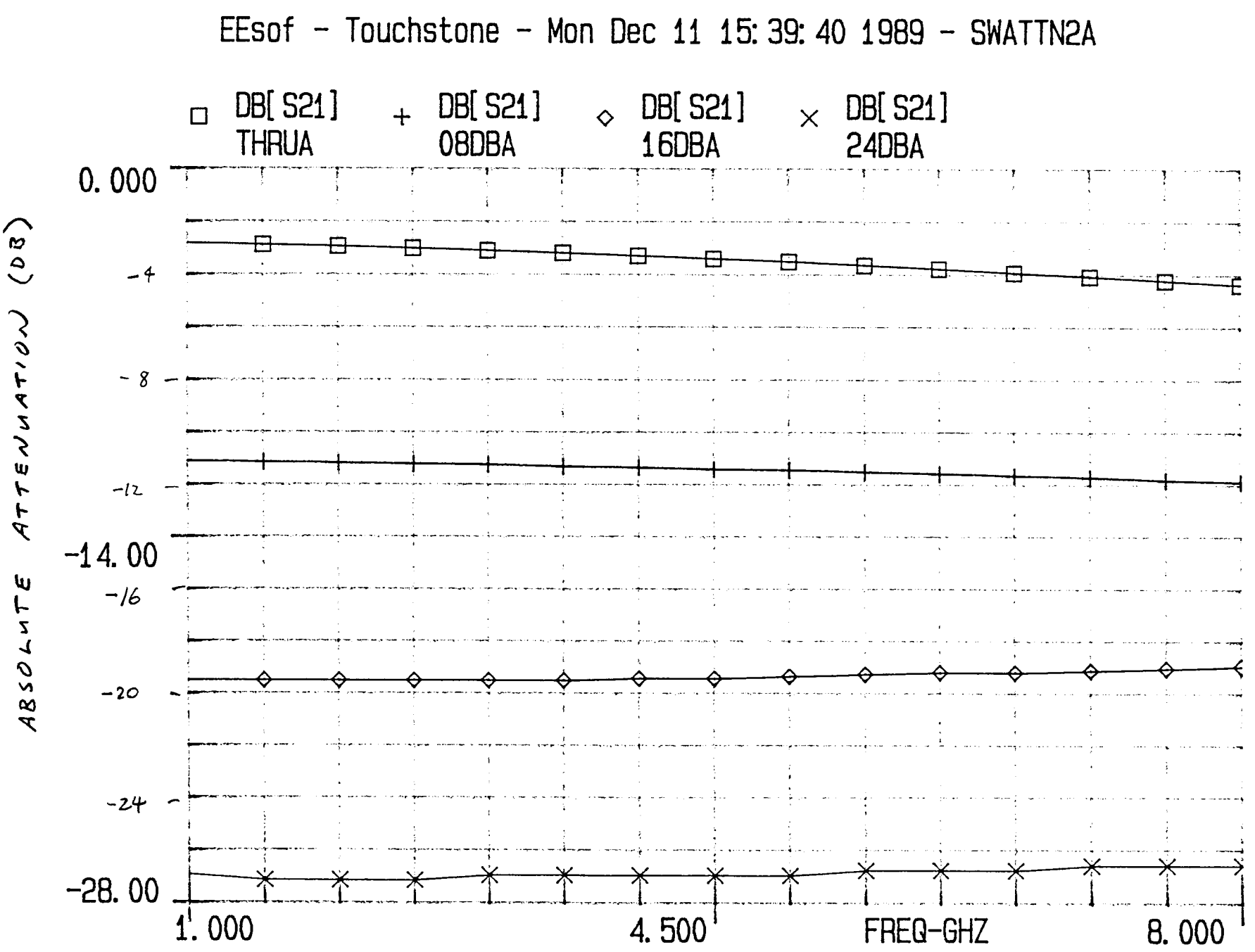
8/16 dB Switched Pi Attenuator (Initial circuit)

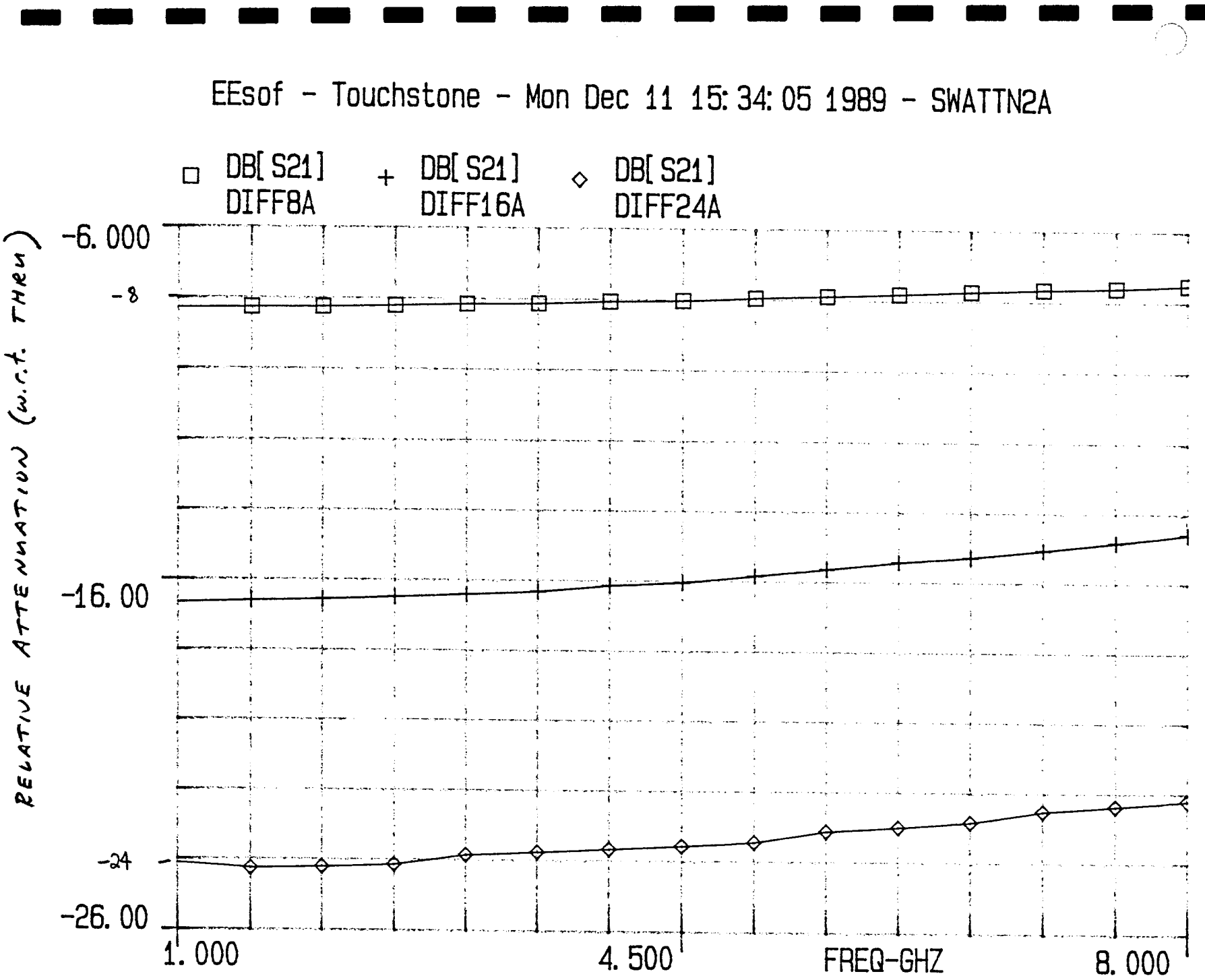


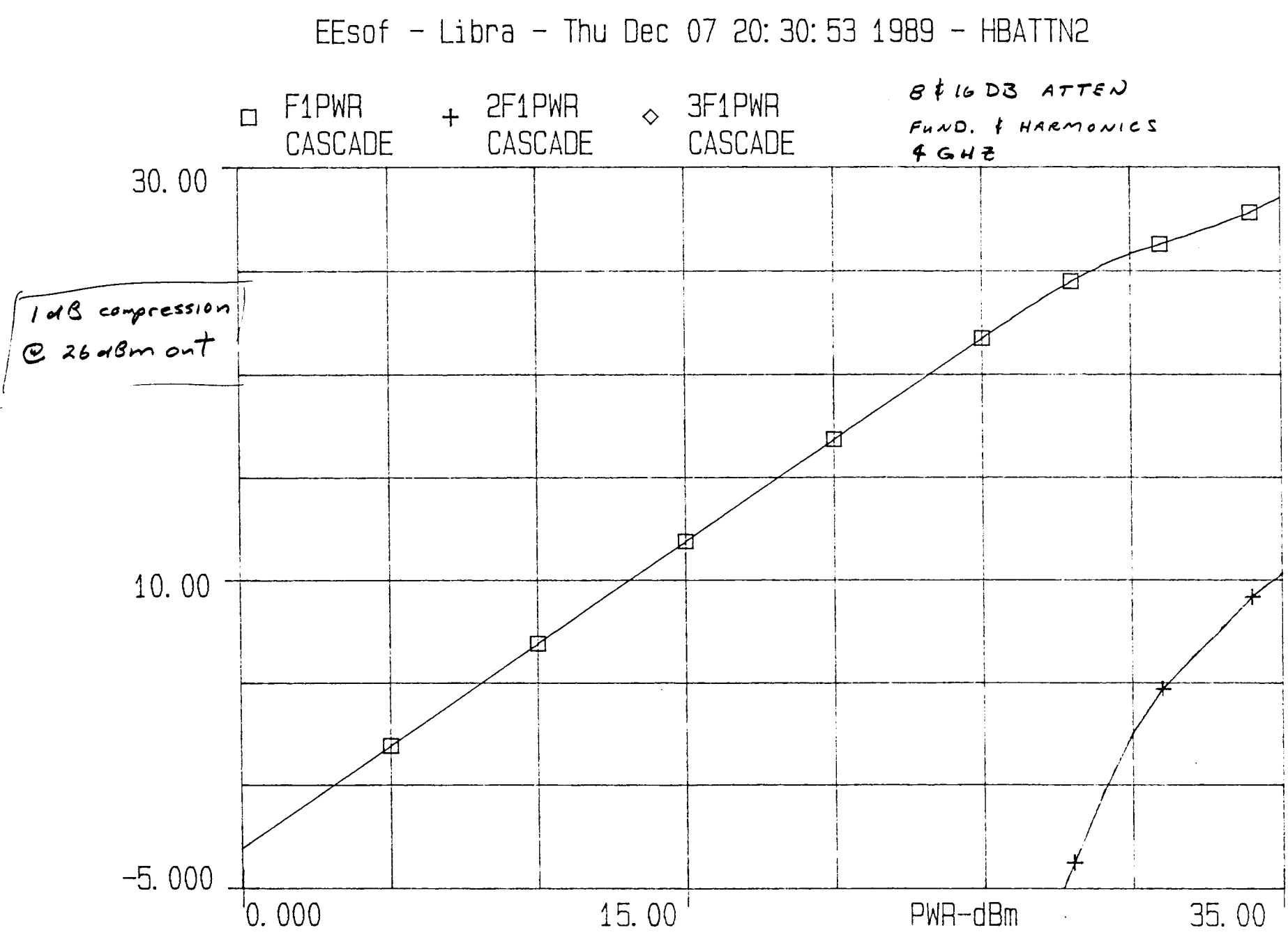
8/16 dB Switched Pi Attenuator (Final Circuit)

Figure 1

FINAL LAYOUT INCLUD. G BONDING L & C




EEsof - Touchstone - Mon Dec 11 15:34:05 1989 - SWATTN2A
DB[S21] DIFF8A
DB[S21] DIFF16A
DB[S21] DIFF24A
-6.000
-8
-16.00
-24
-26.00
RELATIVE ATTENUATION (w.r.t. THRU)
1.000
4.500
8.000
FREQ-GHZ


EEsof - Libra - Thu Dec 07 20:30:53 1989 - HBATTN2
F1PWR CASCADE
2F1PWR CASCADE
3F1PWR CASCADE
8 & 16 DB ATTEN
FUND. & HARMONICS
4 GHz
30.00
10.00
-5.000
0.000
15.00
PWR-dBm
35.00
1 dB compression
@ 26 dBm out

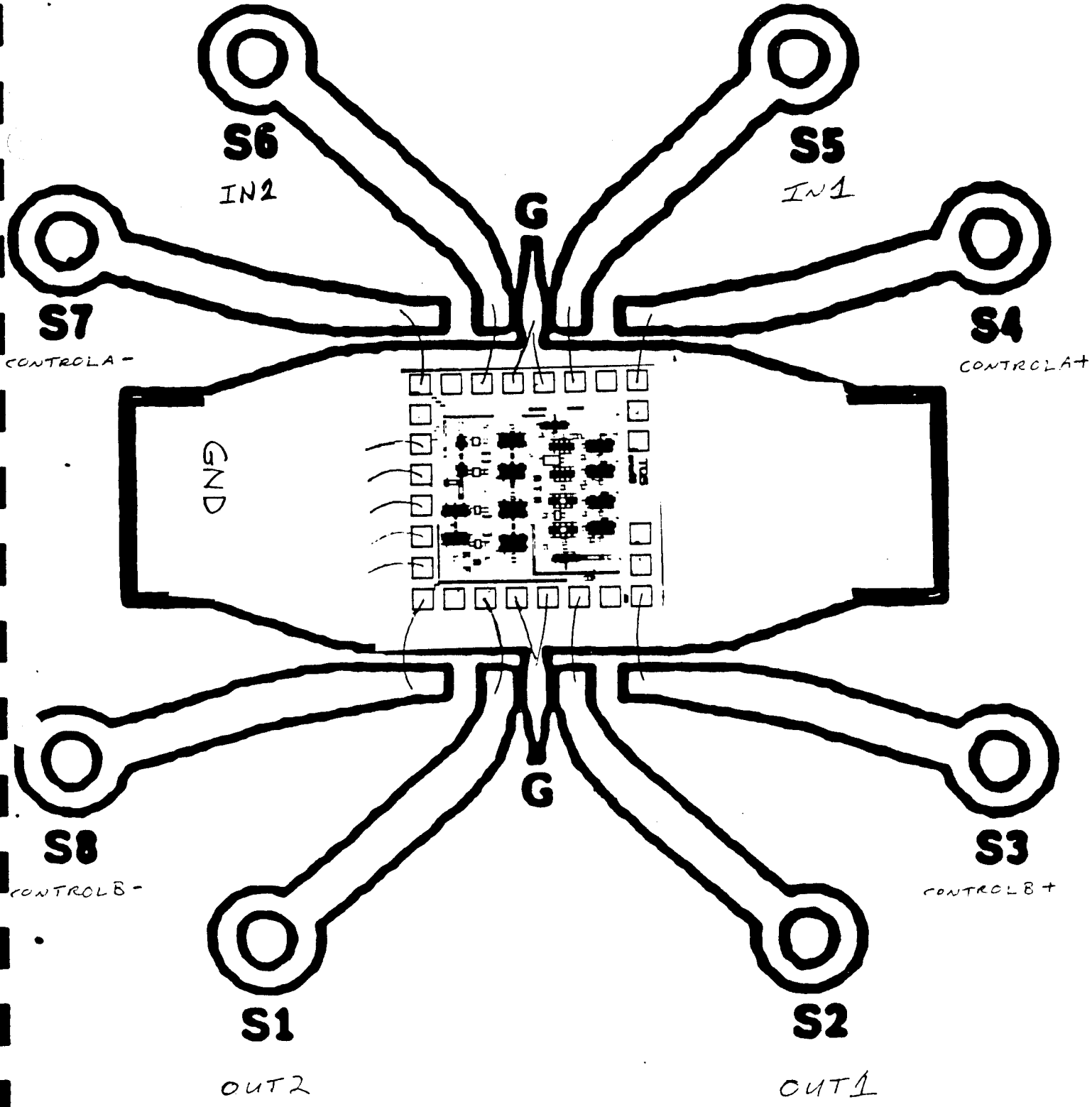


Figure . Bonding Diagram
switched Attenuator

ABSTRACT

This paper describes the design of a MMIC elliptic filter using active FET resonators. Resonators composed of passive MMIC components typically have Qs of less than twenty. Active resonators were designed with Qs of several hundred. High Q resonators enable the synthesis of high performance filter networks. This paper discusses the design of a 4 GHZ active elliptic filter.

MMIC ELLIPTIC FILTERS

INTRODUCTION

Gallium Arsenide Monolithic Integrated Circuit Technology is currently being applied to military sensors, survielance and communications systems to reduce size and weight. A typical receiver in any of these systems combines active components with filters. The filters reject unwanted signals and spurious products, increasing the system dynamic range.

At the present time most MMIC receiver designs use off-chip resonators and filters in the frequency conversion process. MMIC resonators have low Q and cannot be tuned during the manufacturing process. A smaller more reliable product would result if the filters were integrated into the chip with the other components.

This paper investigates the problems associated with the design of a 100% monolithic elliptic filter. The problem of low component Q is solved by introduciing FETs to create active resonators. Some of the problems associated with active filter design are identified and solved.

CURRENT STATE OF THE ART

A review of MMIC designs in recent literature has revealed examples of monolithic filters. A MMIC mixer-lowpass filter combination was reported by Yang[1] for use in a 6 GHZ to 10 GHZ receiver. Esfandiari[2] developed a two pole Chebyschev filter with 5% bandwidth. The best example of MMIC filter designs is reported by Halladay[3]. He developed a set of four wideband elliptic filters centered between 1.5 GHZ and 9.2 GHZ. These filters form the preselector for a electronic warfare system.

The filter networks discussed in these papers are implemented with passive MMIC components. Performance is limited by the low Q of passive resonators. The problem of low resonator Q has been solved by using active components. At video and HF frequencies operational amplifiers are used to create active filters. At this time no microwave Opamps are available. In the VHF/UHF range active resonators based on BJTs and lumped elements have been constructed (ref. 4-7,1969-83). The filter described in this paper operates in the microwave range using FETs and 100% monolithic construction.

ELLIPTIC FILTER SYNTHESIS

The elliptic filter examined in this report is a 7 pole ladder network. The component values for the passive lumped element network are obtained from tables[8]. The resulting network consisted of ten parallel LC resonators. Other topologies were not considered due to time constraints. This network provides a excellent example of the problems encountered in active MMIC filter design.

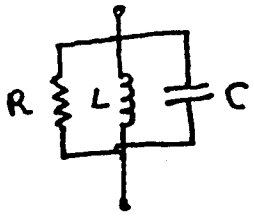
The response of this filter using ideal components and passive MMIC components is shown in figure 1.The "IDEAL" curve was generated using perfect inductors and capacitors. The "MMIC" curve was generated by substituting passive MMIC components into the network. The low Q of the MMIC resonators has clearly degraded the filter performance. This filter requires resonator Q > 140. The following Qs for 4 GHZ MMIC resonators were estimated by computer simulation.

L (ph)	C (pf)	Q
2000	0.792	7.5
1000	1.583	7.5
500	3.160	8.0

The Q of the MMIC resonators must be increased by a factor of at least 20 to implement the desired filter.

HIGH Q RESONATOR SYNTHESIS

Parallel RLC resonators are described by the following set of equations.



$$Y_r = 1/R + j(wC - 1/wL)$$

$$w_0^2 = 1/LC$$

$$Q_0 = w_0 CR = R/w_0 L = R\sqrt{C/L}$$

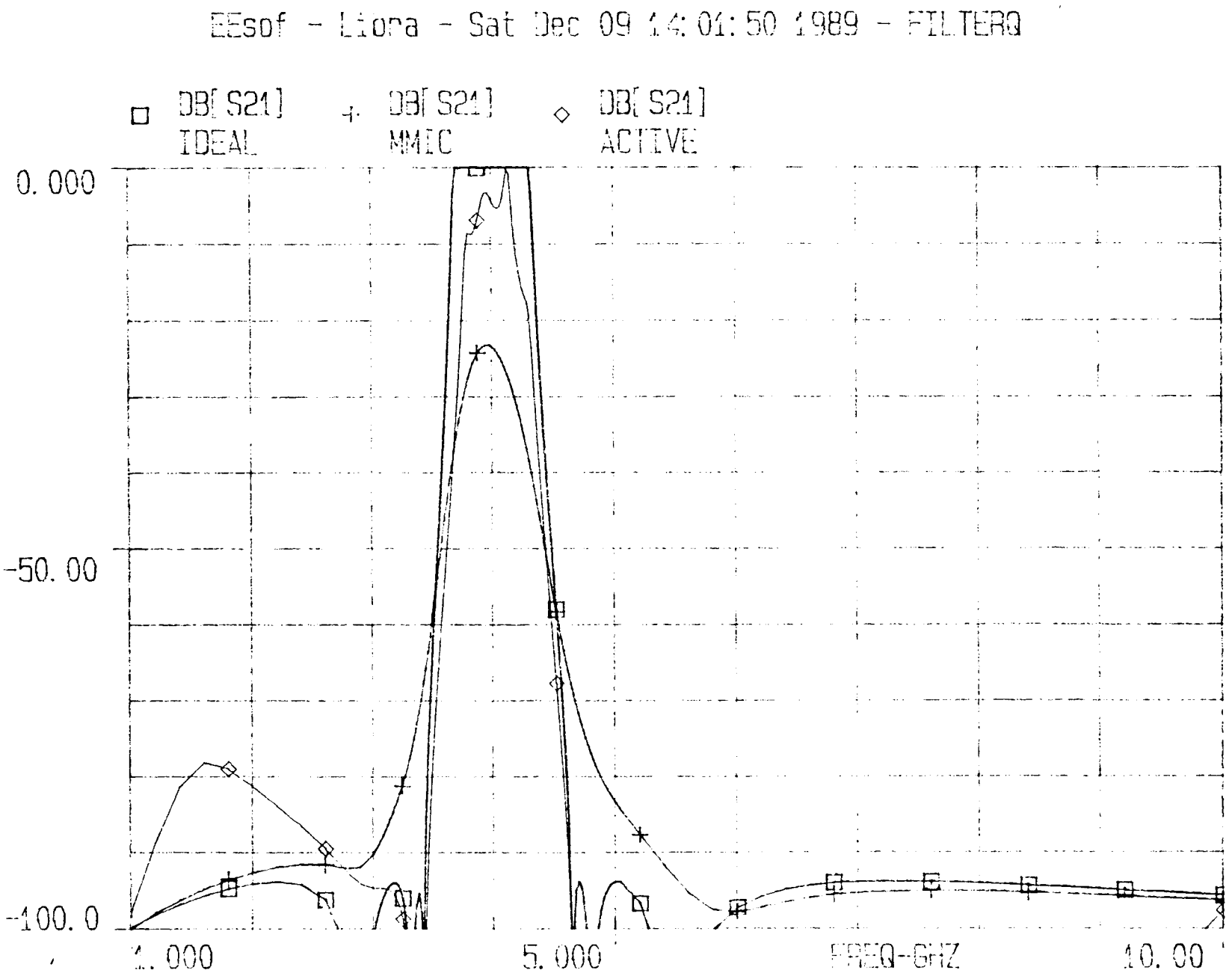
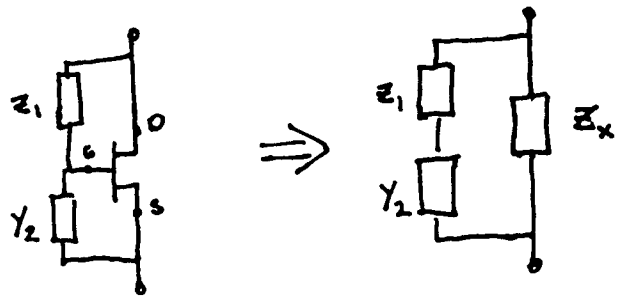


FIGURE 1: FILTER RESPONSE

FETs may be used to synthesize high Q resonators by using the following technique.



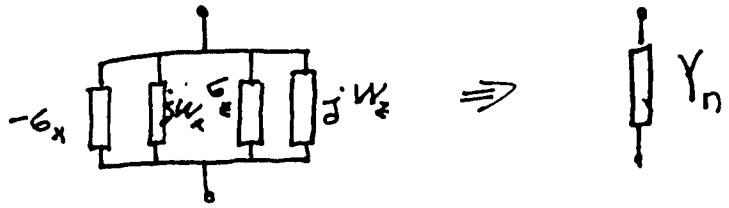
$$Z_1=R_1+jX_1$$

$$Y_2=G_2+jW_2$$

$$Z_x=(Z_1*Y_2+1)/g_m$$

$$Z_x=(1/g_m)[\ (R_1G_2-X_1W_2+1)\ +j(G_2X_1+R_1W_2)\ ]$$

Selection of suitable impedance values make it possible to drive the real part of Z_x negative. Shunting Z_x with a lossy conductance yields the following network conductance.



$$Y_n=(G_z-G_x)+j(W_z+W_x)$$

The real part of the resulting network can be zeroed yielding a reactive network with infinite Q.

Actual synthesis of MMIC resonators is not as easy as the math leads one to believe. As the network Q is increased the network becomes sensitive to parasitic effects, particularly stray capacitance. The possibility of negative resistance also creates the possibility of oscillation.

Approximately thirty different single and dual FET active resonator networks were investigated. Analysis was based on ideal components with finite Q. Simulations were performed using the available MMIC component library. Synthesizing a resonator with the required Q, $w_\emptyset$ and L/C ratio is difficult. The optimizers used by Libra tend to optimize only one or two of the

three required parameters yielding a useless network. Resonators 2 and 3 could not be accuratlly synthesized. Optimization is a problem that will have to be resolved in future investigations. The following results were obtained for the ten filter resonators.

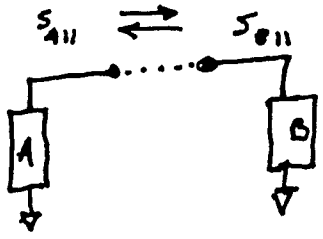
L (ph)	C (pf)	^{w}Ø (ghz)	Q (MMIC)	Q (active)
261	6.ØØØ	3.989	15.9	885
27Ø4	Ø.3Ø9	5.Ø35	1.7	
5149	Ø.588	2.891	5.4	
156	1Ø.17Ø	3.987	17.5	281
719	1.628	4.649	7.1	952
977	2.212	3.423	7.Ø	238
161	9.837	3.988	16.5	717
965	1.137	4.8Ø5	7.9	199
14ØØ	1.65Ø	3.311	6.8	343
282	5.647	3.989	16.4	92Ø

Replacing the passive resonators with the active resonators yielded the network response labeled "ACTIVE" in figure 1. The circuit file containing the actual active resonator circuits is attached to this report.

The active resonator filter response approaches the ideal response. The deviation from ideal is caused by the active resonators not quite having the correct resonant frequencies and L/C ratio. Those two problems cause the filter poles to shift and the sections to mismatch. Yielding a distorted network response. This problem should be solvable if the optimizer can be made to work correctly. The active filter response has removed some of the passband loss and restored the narrow transition bands. Hence this design technique may yield usable filter networks after further research.

STABILITY ANALYSIS

Introducing active components into the filter network creates the possibility of oscillation. The resonators themselves may oscillate or they may oscillate when connected to the network. The oscillation condition for a network node may be expressed as follows.



$|S_{a11}S_{b11}|>1$ possible oscillation

It is interesting to note that even though a resonator may have gain the network may still remain stable if the correct feedback is not present at that node.

The following method of testing for oscillation using actual component models was developed.

```
CKT
  ...            network a definition
  DEF1P    NetA
  ...            network b definition
  DEF1P    NetB
PROC
  STABILITY= NetA * NetB
OUT
  STABILITY  DB[S11]
```

Using this technique the stability of active resonators 1,4,5 and 6 were tested. The results shown in figure 2 indicate that resonators 4 and 6 are unstable and that resonators 1 and 5 are stable. This technique allows the network to be tested with actual component performance data and suitable layout parasitics. The circuit file used to generate this test is attached to this report.

BIASING

Active components require DC bias to operate. The DC needs to enter and exit the circuit at low impedance points, preferably AC grounds. The ladder filter topology does not provide a ground for every resonator. To solve this problem the following approach was going to be used. The active resonators would all use identical FETs (1um x 600um) connected in series. The DC would enter and exit the circuit on the ground side of the shunt resonators. Gate biasing would be accomplished using a ladder of large value resistors. The expected schematic for this technique is developed in figure 3.

This design never progressed to the point of actually constructing this network and simulating the bias network effects on the filter response. However the active resonators selected were designed with this biasing technique envisioned.

Some of the dual FET resonators offered desirable performance if two types of FETs were used. However the biasing for multiple FETs some of which were floating would have been much more complicated and beyond the scope of this project. A more integrated approach would have been to use the dual FET resonators and balance the impedance transformations in each filter section to match biasing requirements.

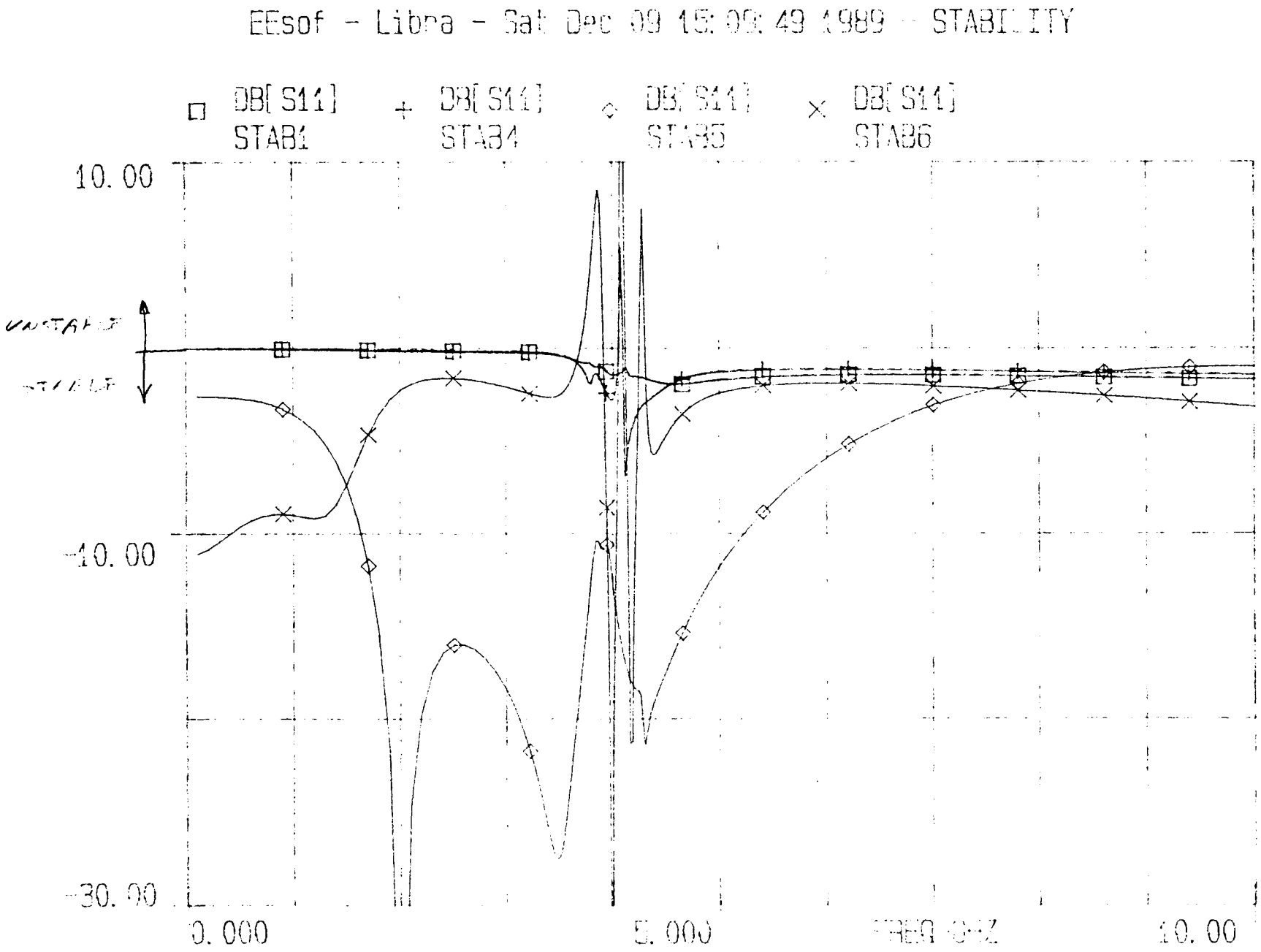


FIGURE 2: STABILITY ANALYSIS

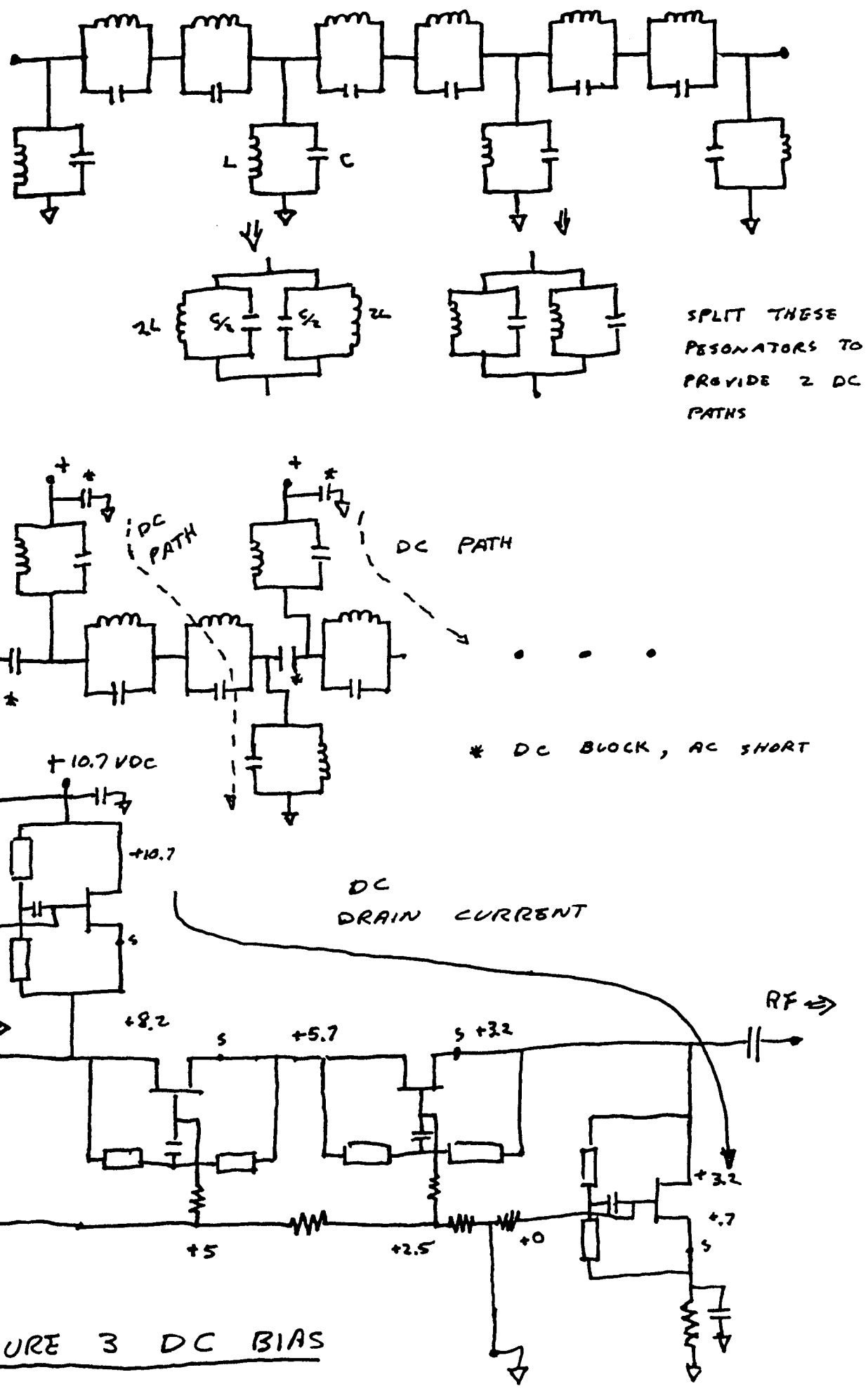


FIGURE 3 DC BIAS

SUMMARY

The filter design attempted in this paper was not successful. Analysis showed that the resulting network was not a high performance filter, but a poorly designed oscillator. However several successes were made. High Q resonators were synthesized and analysis techniques were developed. It appears that active MMIC filters are possible to design using single FETs and monolithic components. Further research is required to optimize resonator design and filter topology. MMIC filters will enable the design of a new generation of monolithic receivers.

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