THE JOHNS HOPKINS UNIVERSITY
G. W. C. WHITING SCHOOL OF ENGINEERING
ELECTRICAL ENGINEERING PROGRAM

MICROWAVE ENGINEERING
MMIC DESIGN 525.787
PROJECT REPORTS FALL 1993

ENHANCED C-BAND MMIC MIXER
M. Dye

ACTIVE INDUCTOR
D. Coghlan

A 5.654 GHz LNA
K. Bontzos

MILLIMETERWAVE ABSORPTIVE SPST SWITCH
A. DeWitt

A WIDE BAND DIRECTIONAL COUPLER
D. LaBarbera

PUSH-PUSH CLASS B 24 GHz TO 48 GHz DOUBLER
K. Ditzler

THE JOHNS HOPKINS UNIVERSITY
PART-TIME PROGRAMS IN
ENGINEERING AND APPLIED SCIENCES

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ENHANCED C-BAND MMIC MIXER

Final Project
MMIC Design 525.787
Fall 1993

Michael Dye

1. Abstract

A MMIC single-balanced diode mixer with 50 ohm input and output coplanar ports has been designed with the Tri-Quint HA process for use in the AMSAT C-Band receiver. This work is a follow-up to the original design of Ferrell and McReynolds. The new design uses a 180 degree lumped element coupler that achieves a 33% fractional bandwidth, <0.5 dB amplitude imbalance, <10 degree phase imbalance, <1.5:1 VSWR (all ports) and >27dB isolation between inputs, around the design frequency of 6000 MHz. Following the direction of an idealized mixer analysis, the matching elements of the previous circuit have been adjusted to provide an RF embedding impedance near the desired 50 +j50 ohms. Nonlinear simulation of the layout predicts a conversion loss <10dB, almost 4dB better than the previous mixer. Finally, the output IF circuit has been adjusted to boost series dc-blocking capacitance and maintain at least a 2.5:1 VSWR at the IF port, while maintaining proper impedances near the diodes at the input and output frequencies. This correction may have had a more beneficial effect than the RF matching, because previously the diodes were highly mismatched, perhaps 4:1 VSWR. Since the dc-blocking capacitance has been identified as a problem limiting bandwidth, an auxiliary output (coplanar probe compatible) has been provided.

2. Introduction

The performance specifications and goals for the original MMIC single-balanced diode mixer designed by Ferrell and McReynolds [1] are shown in Table 2.1 along with the measured results [2]. The measured results were achieved when a short at the RF input was identified and removed. A simplified schematic is shown in Figure 2.1.

Research was conducted using Maas [3] as the primary reference to identify better mixer circuits for MMICs. Of particular interst were the FET mixers, which can provide conversion gain with moderate noise figure. Standard single balanced FET mixer circuits were rejected because of the large area the input and output hybrids would require [3, p.333]. FET resistive mixers [3, p.362] and active load FET switching mixers [3, p.359] were investigated, with mediocre results. In any event, good nonlinear models for the linear FET region were lacking.

Due to time constraints it was decided to stay with a diode mixer design, but with the goal of improving the conversion loss and bandwidth.

3. Modeled Performance

Improved bandwidth for the mixer is possible by replacing the lumped element 90 degree coupler with a lumped element 180 degree coupler. [3, p.254] The coupler was designed by converting the three 1/4 wave branches and the one 3/4 wave branch of the distributed model with lumped element equivalent lowpass and highpass circuits (see Figure 3.1). A symmetrical layout was tried at first, but chip size and via placement forced a non-symmetrical format (see layout in Figure 4.2). Performance is still good, as seen in Figures 3.2 (a), (b), and (c).

Limited chip size ruled out including a FET amplifier in the input or output to reduce conversion loss, but non-optimal diode matching was identified. Using a simplified form of the Held and Kerr mixer analysis procedure [4] described in [5], the optimum source (RF) and load (IF) impedances as well as the conversion loss were estimated, based on the given frequencies, diode parameters (Tri-Quint 1um X 2 X 80um device), and biasing (.55V per diode). The results:

Zrf_opt	=	50 + j50 ohms
Zif_opt	=	150 + j50 ohms per diode in parallel
Conv loss	=	5 dB min

The desired source impedance was easily obtained by reducing the series capacitance and shunt inductance of the original matching circuit in both coupler outputs (see Figure 3.3). More significant was the modification of the output LPF (see Figure 3.4(a)), which mismatches the real part of the diode IF impedance. The new circuit (see Figure 3.4(b) and Figure 3.5) improves the match while maintaining an effective RF short for the diodes. An auxiliary port has been included to permit off-chip dc blocking to improve output bandwidth.

The new compliance matrix is shown in Table 3.1 for the full Tri-Quint MMIC mixer layout. All specifications are met by the new mixer. With at least 2 dB of loss inherent in the Tri-Quint coupler and matching circuit, the 9.7dB conversion loss is within 3dB of the analysis minimum.

In Figure 3.6, the input return losses and the conversion loss are shown as functions of the LO drive. Clearly the mixer desires a +10dBm LO, but it can be run at lower drive levels with moderate increases in conversion loss and input VSWR.

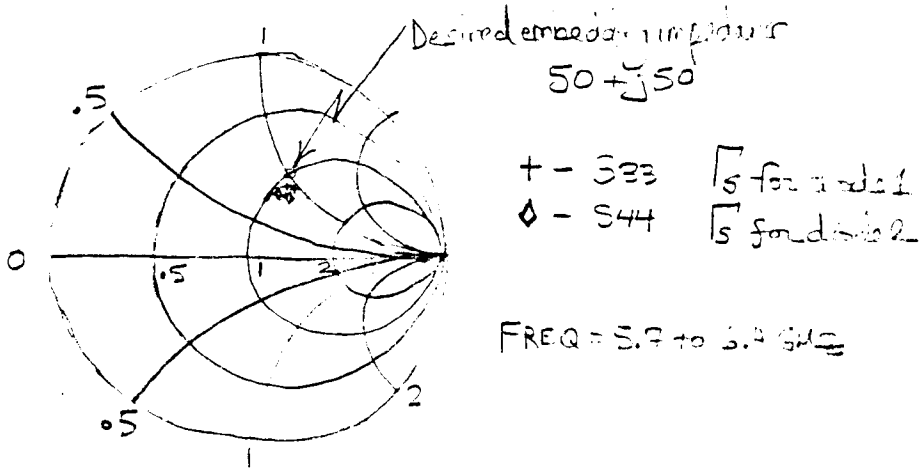
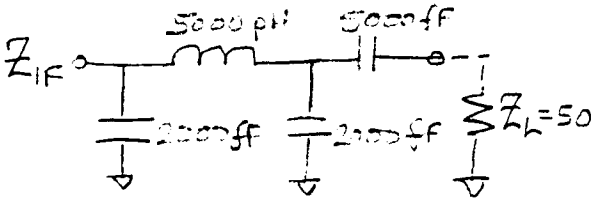
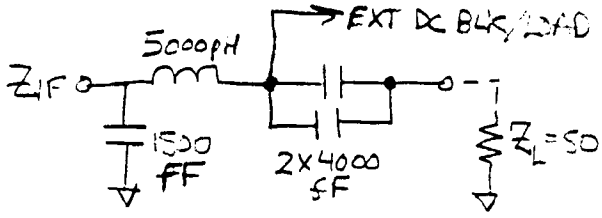


Figure 3.3 Source Impedance at diode ports



$Z_{IF} = .03 - j15\ \Omega$ @ RF
$= 17 - j16\ \Omega$ @ IF

(a) ORIGINAL IF OUTPUT CKT



$Z_{IF} = .3 - j14\ \Omega$ @ RF
$= 1.7 - j20\ \Omega$ @ IF

(b) MODIFIED IF OUTPUT CKT

Figure 3.4 IF output circuits

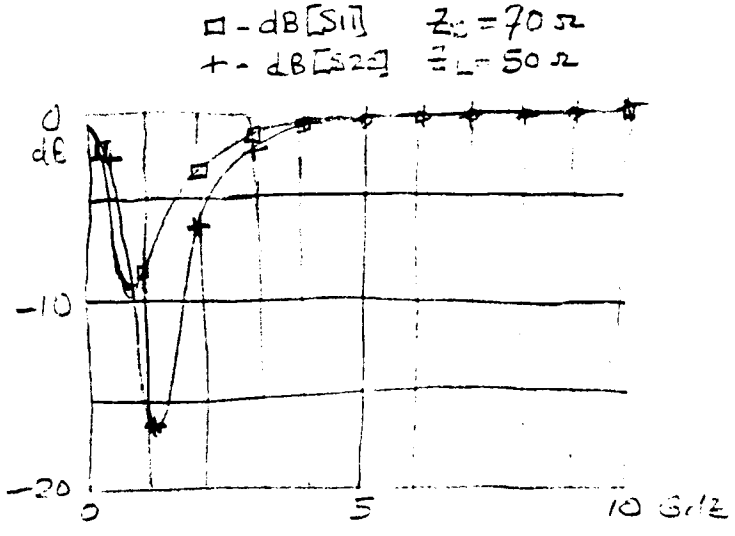


Figure 3.5 RETURN LOSS OF IF CKT GIVEN $Z_{IN} = 70\ \Omega$, $Z_{OUT} = 50\ \Omega$

Table 3.1 New MMIC Mixer Compliance Matrix

Parameter	Specification	Goal	Predicted
RF FREQ	5654 MHZ	-	5654 MHZ
LO FREQ	6400 MHZ	-	6400 MHZ
IF FREQ	746 MHZ	-	746 MHZ
BANDWTH	>100 MHZ	-	yes
L TO R	10 DB	16 DB	33 DB
R TO L	10 DB	16 DB	25 DB
CONV L	15 DB	6 DB	9.5 DB
SUPPLY	+-5 V	+5 V	+5 V
RF VSWR	2.5:1	1.5:1	1.3:1
LO VSWR	2.5:1	1.5:1	1.3:1
IF VSWR	?	?	<2.5:1
L TO I	?	?	46 DB
R TO I	?	?	23 DB
LO PWR	?	?	+10 DBM

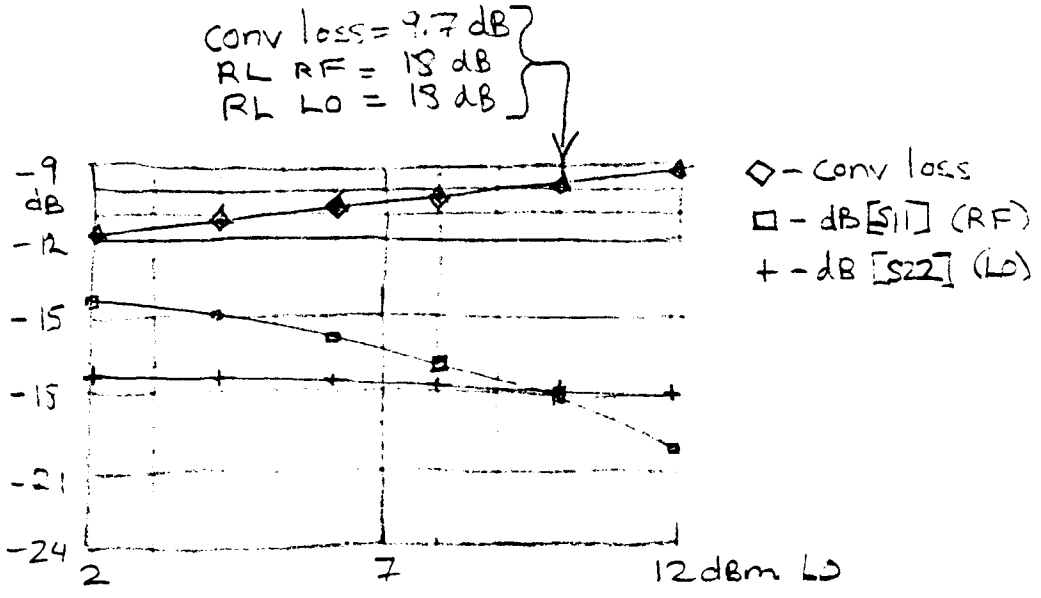


Figure 3.6 Conversion [illegible] vs LO Drive
Return [illegible] vs "
Return [illegible] RF "

4. Schematic, DC Analysis and Layout

Figure 4.1 (a) is a simplified schematic of the mixer MMIC. A DC bias check on the final circuit is superimposed on the schematic in Figure 4.1 (b). The resistors, capacitors, inductors, diodes and interconnects are all rated to handle the predicted current, as seen by the first mixer.

Figure 4.2 shows the final chip layout. The ports have been labelled for easy identification.

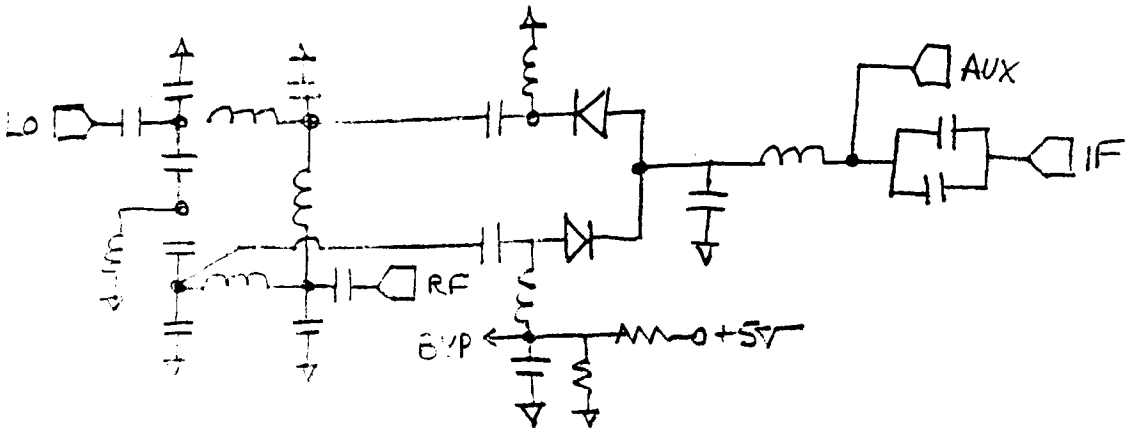


Figure 4.1 (a) Mixer Schematic

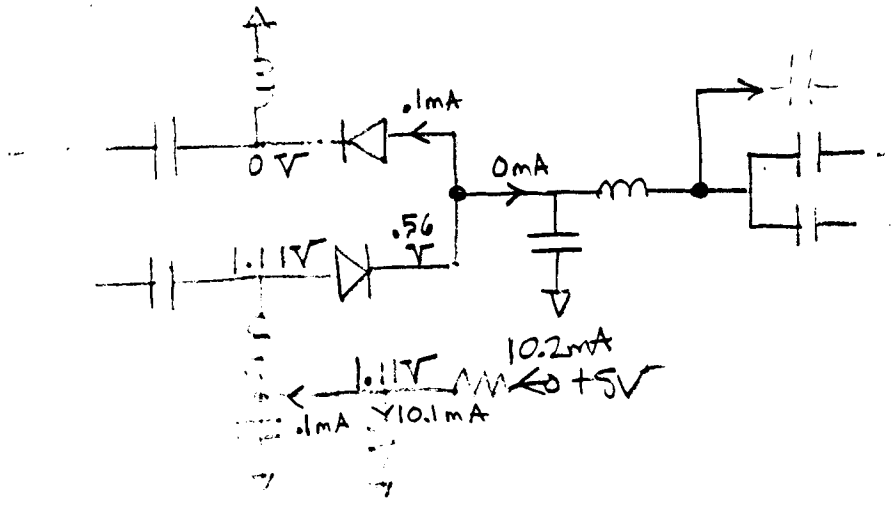
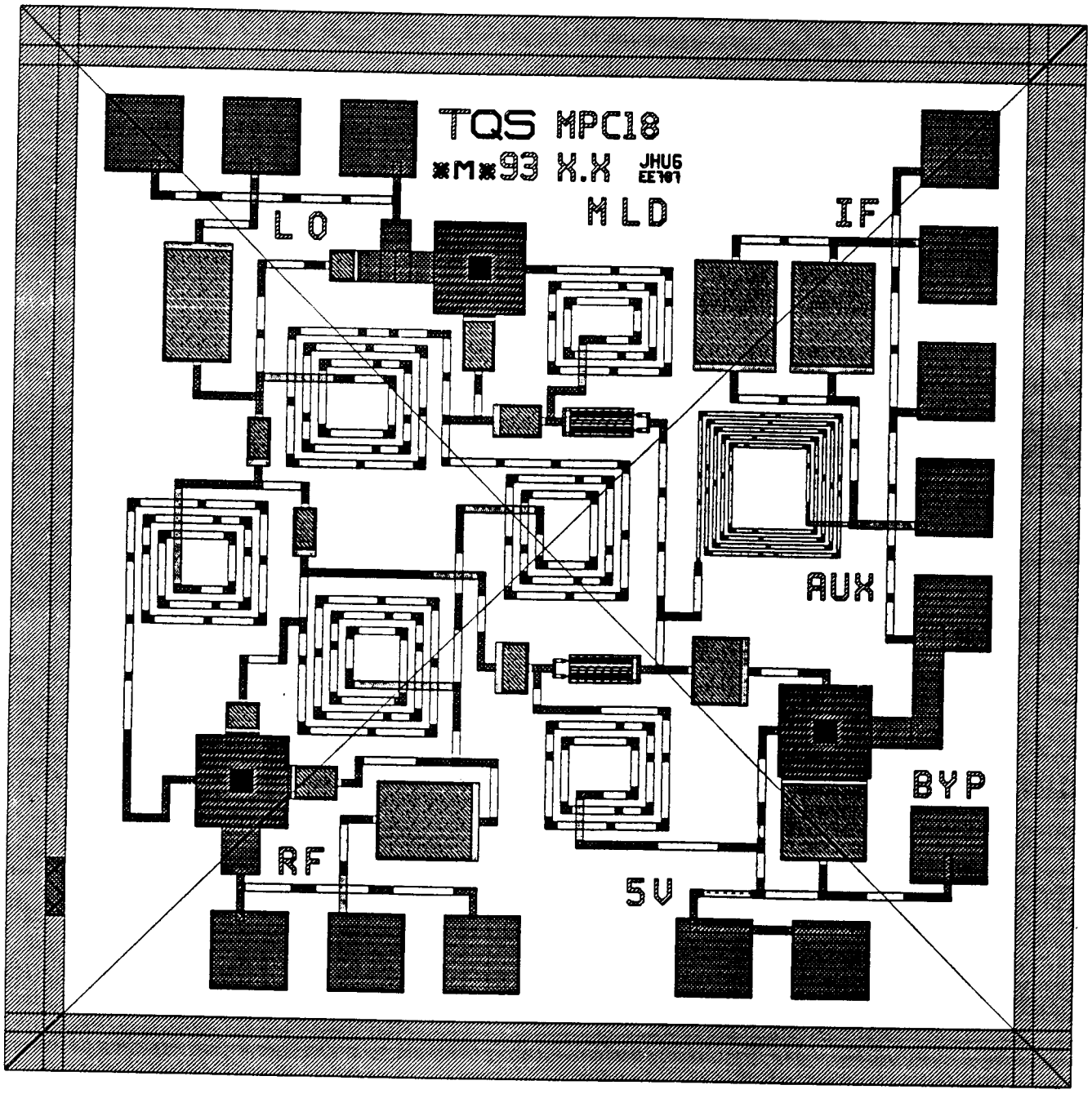


Figure 4.1 (b) DC Analysis


TQS MPC18
*M*93 X.X JHU6 EE701
MLD
LO
IF
AUX
BYP
RF
5V

5. Design Robustness

A study of the effect of process tolerance on mixer performance was done to indicate sensitive parameters and for design centering. Diode, inductor and trace width variations were assumed negligible compared with capacitor and resistor variations that can reach 20% and 10% up and down, respectively. The results are shown in Table 5.1. The most sensitive capacitor was found to be the shunt element at the coupler LO input, which was adjusted upwards for design centering of the LO return loss.

Table 5.1 Design Sensitivity

Parameter	Nom	C_up	C_dwn	R_u/d	
L TO R	33	29	30	NC	(DB)
R TO L	25	28	21	NC	(DB)
CONV L	9.5	9.3	10.6	NC	(DB)
RF VSWR	1.3:1	1.5:1	<1.1:1	NC	
LO VSWR	1.3:1	1.5:1	1.5:1	NC	
L TO I	46	NC	NC	NC	(DB)
R TO I	23	NC	NC	NC	(DB)

NC = Negligible change

6. Test Plan

Please refer to [1] for this section.

7. Conclusions and Recommendation

The new mixer should lower conversion loss and increase bandwidth due to better diode matching and the use of a 180 degree coupler. Unfortunately, despite the careful layout of the coupler, uneven placement of the diodes (forced by chip geometry) added a 10 degree phase offset between the pair, but port isolation remained better than 20dB regardless. Also, improving the diode match at the RF and the decoupling of the bias at the IF could have been investigated further, but the mixer should meet spec even with process variation.

Although the new mixer may show better performance than the previous, the original goal of conversion gain was not met due to inadequate time and resources. Further study of FET mixers should include better linear-region models, nonlinear FET analysis (like the diode program) and practical feedback compensation "tricks" to lower the output impedance of FET mixers, which apparently tends to be unreasonably high. Reference [3] was very helpful and is highly recommended for additional MMIC mixer work.

8. Disk Files

tqmix2.cal ---------- Calma file of final layout
tqmix2.ckt ---------- Libra circuit file of mixer
mixemb.mcd ---------- Mathcad file used for mixer analysis

REFERENCES

[1] G. Ferrell and K. McReynolds, C-Band MMIC Mixer, Final Rpt. EN525.787, Fall 1992, Johns Hopkins U.

[2] M. Dye, Nov. 8, 1993, Dorsey Ctr., JHU.

[3] S. Maas, Microwave Mixers, 2nd ed.

[4] D. Held and A. Kerr, "Conversion Loss and Noise of Microwave and Millimeter Wave Mixers: Part I - Theory and Part II - Experiment", IEEE Trans Microw Theory Tech, v. MTT-26, Feb. 1978, pp. 49-61.

[5] M. Dye, Design of a 75-110 GHz MMIC Mixer, Master's Thesis, UVa, May 1993.

MMIC REPORT

ACTIVE INDUCTOR

DES F COGHLAN

FALL '93

525.787

2.0 Theory

The first attempt was based on the paper " Broad-Band, Lossless Monolithic Microwave Floating Inductor" by Guang Fei Zhang, and J.L Gautier in IEEE Microwave and Guided Letters, Vol 3, No4, April 1993. See fig 1.

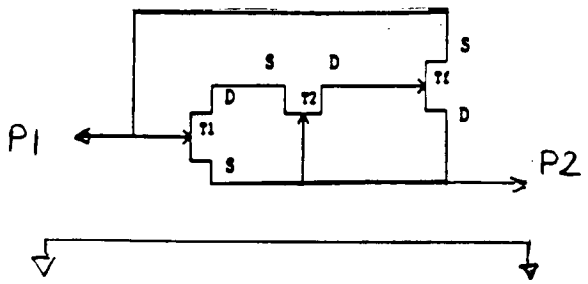


FIG 1

FETS T1 and T2 are connected in cascode, and FET Tf is feedback. Assuming that each FET may be ideally modelled as input capacitor, Cgs and current source gm, the input admittance is represented by eq (1), where the suffixes 1,2, and f refer to the T1,T2 and Tf. This presumes that the FETs are identical.

$$[Y] = \left[j\omega C_{gs1} + \frac{1}{j\omega \frac{C_{gf}}{g_{m1} g_{m2}}} \right] \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \cdot - - - (1)$$

This is equivalent to a parallel LC circuit : see fig 2.

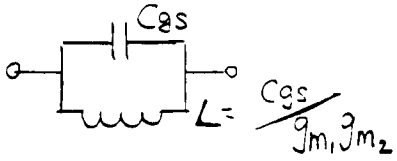


FIG 2

Modelling fig 1 by replacing the ideal FETs with the Triquint model TQSLFET for linear analysis, it became apparent that for L> 10 nH, the FETs had to be quite small:
eg for L= 30 nH

Gate length = 1micon FET,
Gate Width < 10 microns
Number of fingers < 2

Including DC biasing resulted in the circuit in fig 3. T4 and T5 act as DC current sources with minimum loading at RF. The gates are connected to DC voltage sources with high resistances.

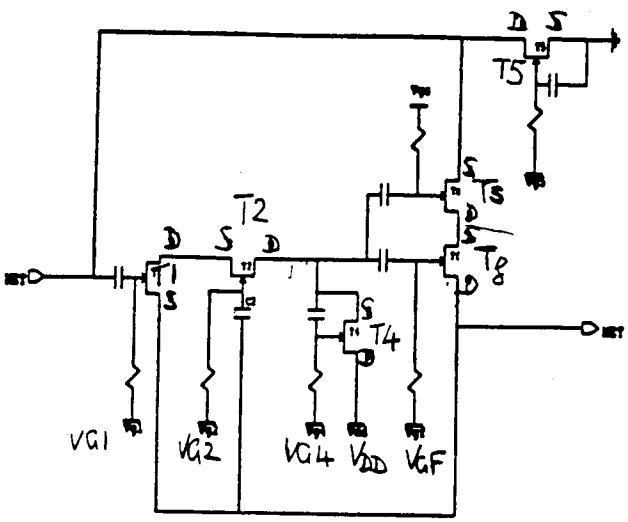


Fig. 3. Configuration of the floating active inductor.

A realistic maximum value is 20 kOhm, based on a 5 micron wide resitor on Tech 11 N-material - 1kOhm per square. However, adding this resistance caused the inductor quality factor Q to degrade to a maximum of less than 1.5. The reason is that the small FETs have a small Cgs. To equate to the energy stored in a large inductor, requires a high RF voltage swing. Connecting resistors to these "hot" RF points, the circuit Q is severely degraded.

2.1 Second Approach

This is based on "Lossless Broad-Band Monolithic Microwave Active Inductors" by Shinji Hara etc in IEE MTT, Vol 37, Dec 1989, pps 1979 to 1984. See fig 4.

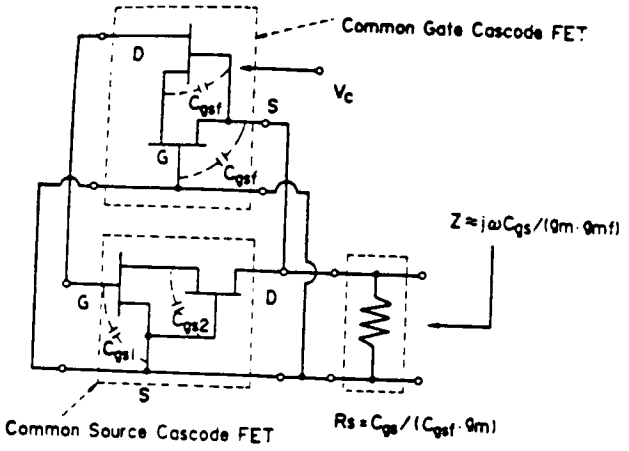


Fig 4

Again assuming the simple FET model of capacitance Cgs and current source gm, the input admittance is given by

$$Y = -g_m \frac{C_{gsf}}{C_{gs}} + \frac{1}{j\omega\left(\frac{C_{gs}}{g_m g_{mf}}\right)} \quad ---(2)$$

The negative real term suggests the possibility of cancelling the real losses from the bias network and FET parasitics. This was proved with the linear circuit model in fig 5 and test results in figs 6 to 9. The FET parameters are:

Gate Width = 20 micron	Length = 1 micron
Drain Current = 0.2*IDss	VDS = 2 V

The impedance from P1 to P2 is equivalent to 20 nH. Note that S11 is not equal to S22 and that S11 is equivalent to a resistor less than 50 Ohms. Since P2 is terminated in 50 Ohms, the circuit from P1 to P2 has negative real resistance.

The FETs are arranged drain-source-drain etc for ease of DC basing. The gates are connected with resistors > 20 kOhm. The drain of the top FET will be connected to the DC supply and so is shown grounded. The source resistors = 1200 Ohm are added to ensure a drain current = 0.2*IDss - see DC Biasing below.

To complete the RF path requires feedback capacitor. 300 fF (0.3pF) is large enough in capacity not to change the RF performance and small enough in area to meet layout requiremnts.

3) Layout

FIg 10 shows the final layout. Except for the grounded gate on F15 , all gates are connected to a large resistor. Each gate resistor is brought out to a discrete test point to permit adjusting the DC bias during test for it's impact on tunability, Q etc. Breakable air-bridges allow settiing the bias resistors to one of 4 values - 0, 6.6k, 13.3k and 20k.

The input, output ports are connected to 10,000 fF. The DC supply is de-coupled by 9000 fF.

Figs 11 to 14 show the test results for the layout of fig 10. Note S11 lies on the constant 50 Ohm line of the Smith Chart until 0.8 GHz. At 1.0 GHz , the Q is approx 10, and the inductance equivalent to 20 nH.

4) Test Plan

Fig 15 shows the test fixture required: the potentiometers are adjusted for the nominal voltages shown.

The network anayser is calibrated for return loss measurements including the probes. Port P2 is terminated in 50 Ohms and S11 is measured looking into P1. The analyser display is set to Smith Chart, impedance. The real and imaginery impedance values,R +jI, are recorded from 0.25 ro 3.0 GHz in steps of 0.25 GHz.

The inductance is calculated as $L = Im(Z/2*pi*f)$

The circuit impedance is $Rc = (\text{Measured Real Value} - 50)$

$Q = Im(Z)/Rc$

Adjust the DC bias to determine the tunability of the inductance.
Im(Z), R and Q are plotted and compared to calculated values.

Included is a plot of the stability factor mu, that is based on the more well known Stability Circle.

mu =(mag - rad) *par

where mag = distance from the center of the Smith Chart to the center of the Stability Circle
rad = radius of the Stability Circle
par =-1 or +1 depending on whether the stability circle intersects the Smith Chart.

mu >=1 implies unconditional stability. Note that mu < 1 at low frequencies, indicating potential instability. A real resistor may be connected across the ports P1 and P2 to assure stability.

At low frequencies (< .7 GHz) the impedance is capacitive due to the 10 pF coupling capacitors that are the largest size that may be accomadated in the layout.

2.2 DC Biasing

The inductance and Q are very sensitive to bias conditions. The test results in figs 6 to 9 are based on drain-source votlge = 2V,and drain current = 0.2*IDss. Using the non-linear model TQSNFET, IDss for a 2 finger, 20 micron width ,1 micron length FET = 4.5 mA. For 0.2 IDss, , the gate-source voltage = -1.2 V. This may be realised by a grounded FET with 1200 Ohms in the source.In fig 6, all six FETs are the same, including the bias FETs F15 and F1, with the same DC bias of VDS = 2V, VGS = -1.2V and drain current = 0.95 mA.

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The circuit impedance is $Rc = (\text{Measured Real Value} - 50)$

$Q = Im(Z)/Rc$

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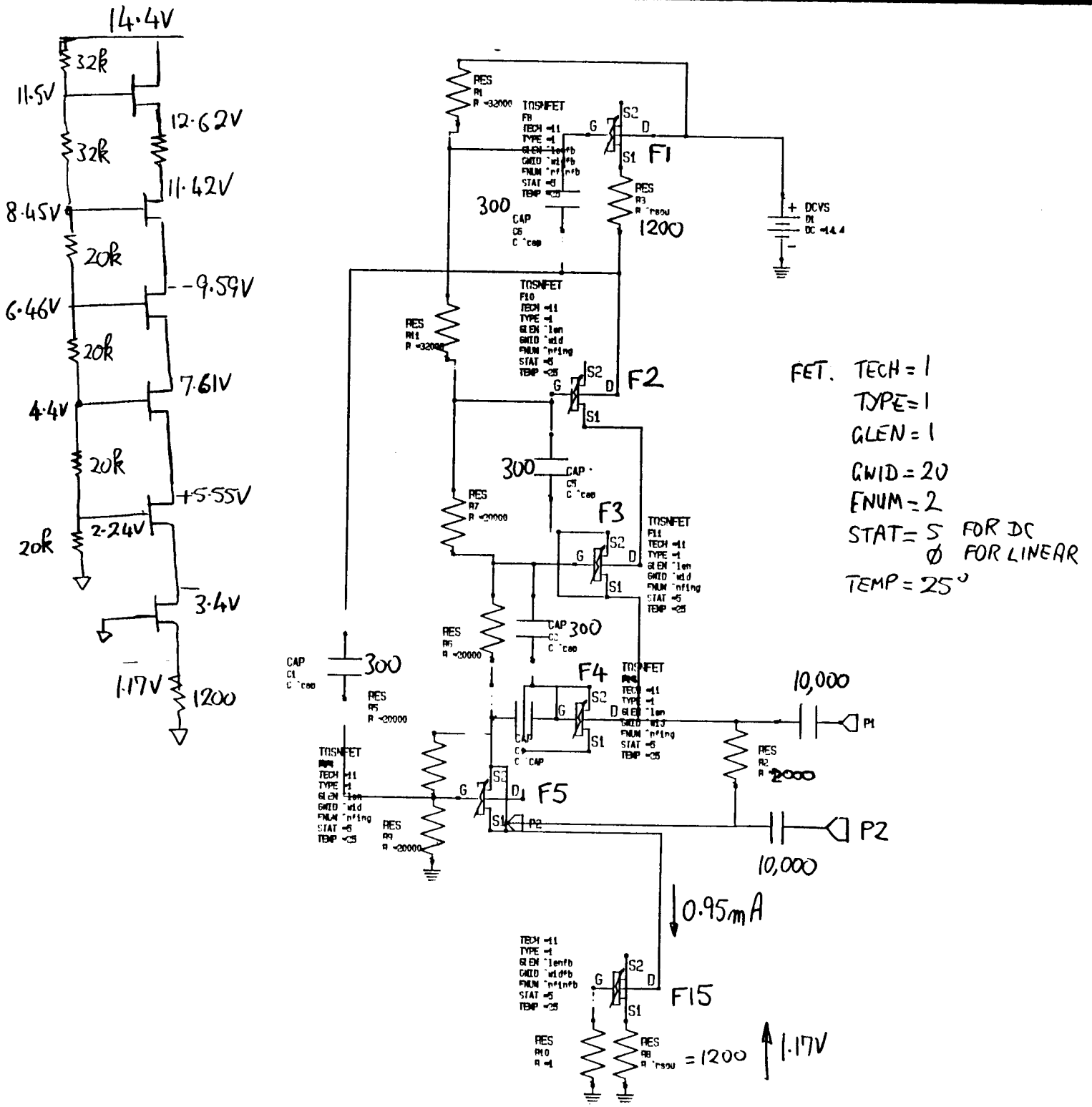
Im(Z), R and Q are plotted and compared to calculated values.


14.4V
32k
11.5V
12.62V
32k
11.42V
8.45V
20k
-9.59V
6.46V
20k
7.61V
4.4V
20k
+5.55V
2.24V
20k
3.4V
1.17V
1200
F1
F2
F3
F4
F5
F15
300
CAP
RES
TOSNFET
DCVS
10,000
P1
P2
2000
0.95mA
1.17V
= 1200
FET. TECH = 1
TYPE = 1
GLEN = 1
GWID = 20
ENUM = 2
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0 FOR LINEAR
TEMP = 25°

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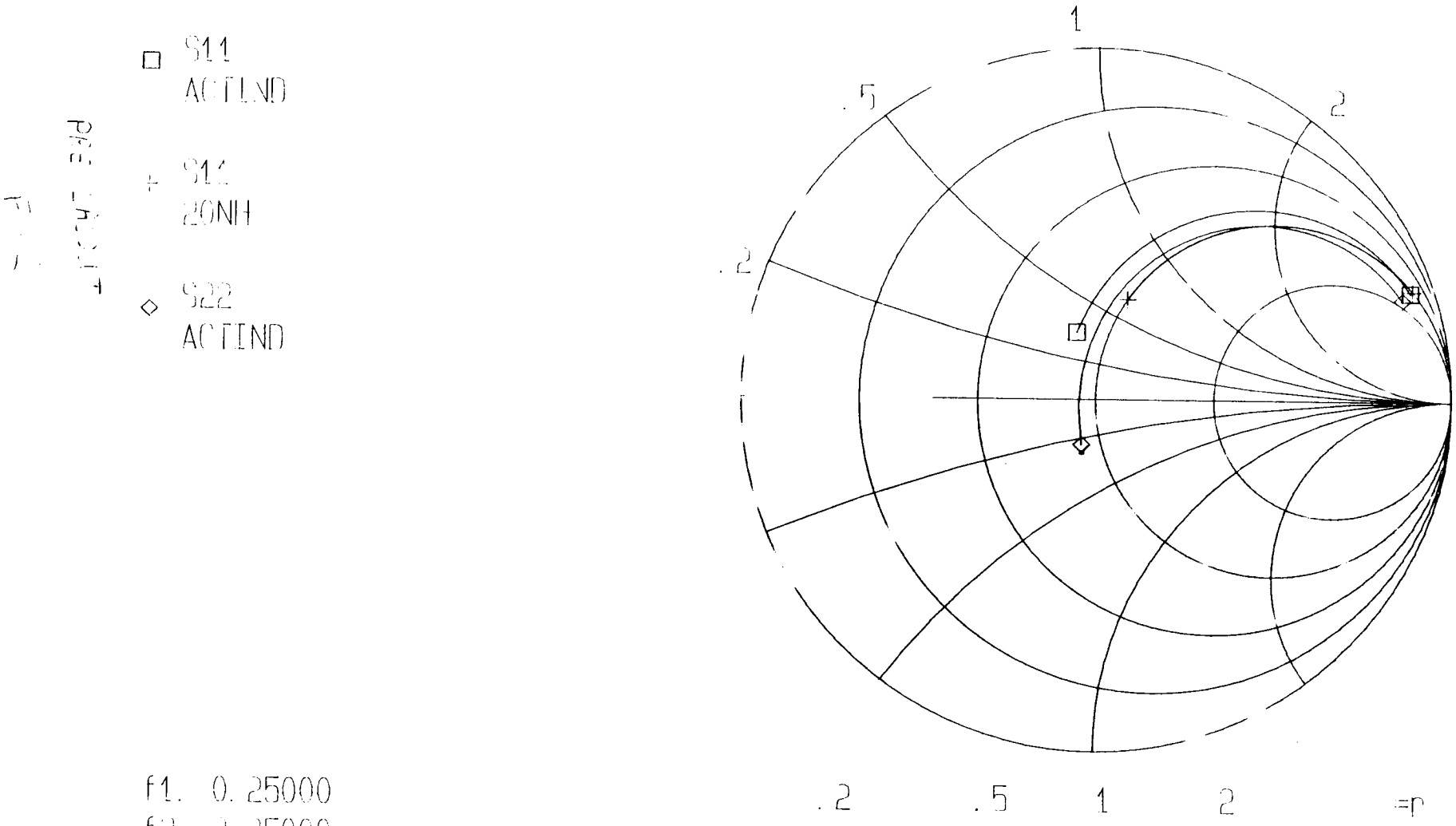
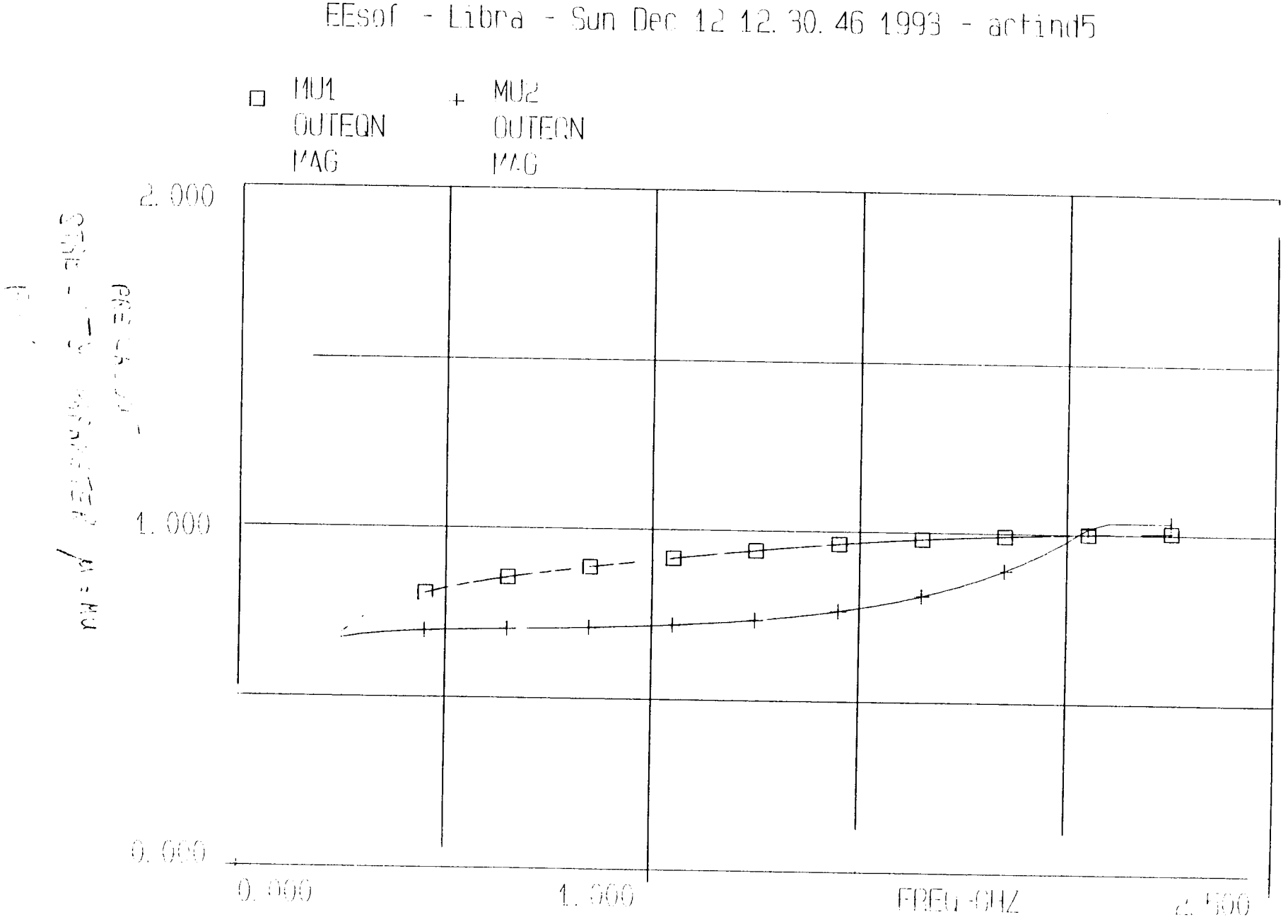


f1. 0.25000
f2. 2.25000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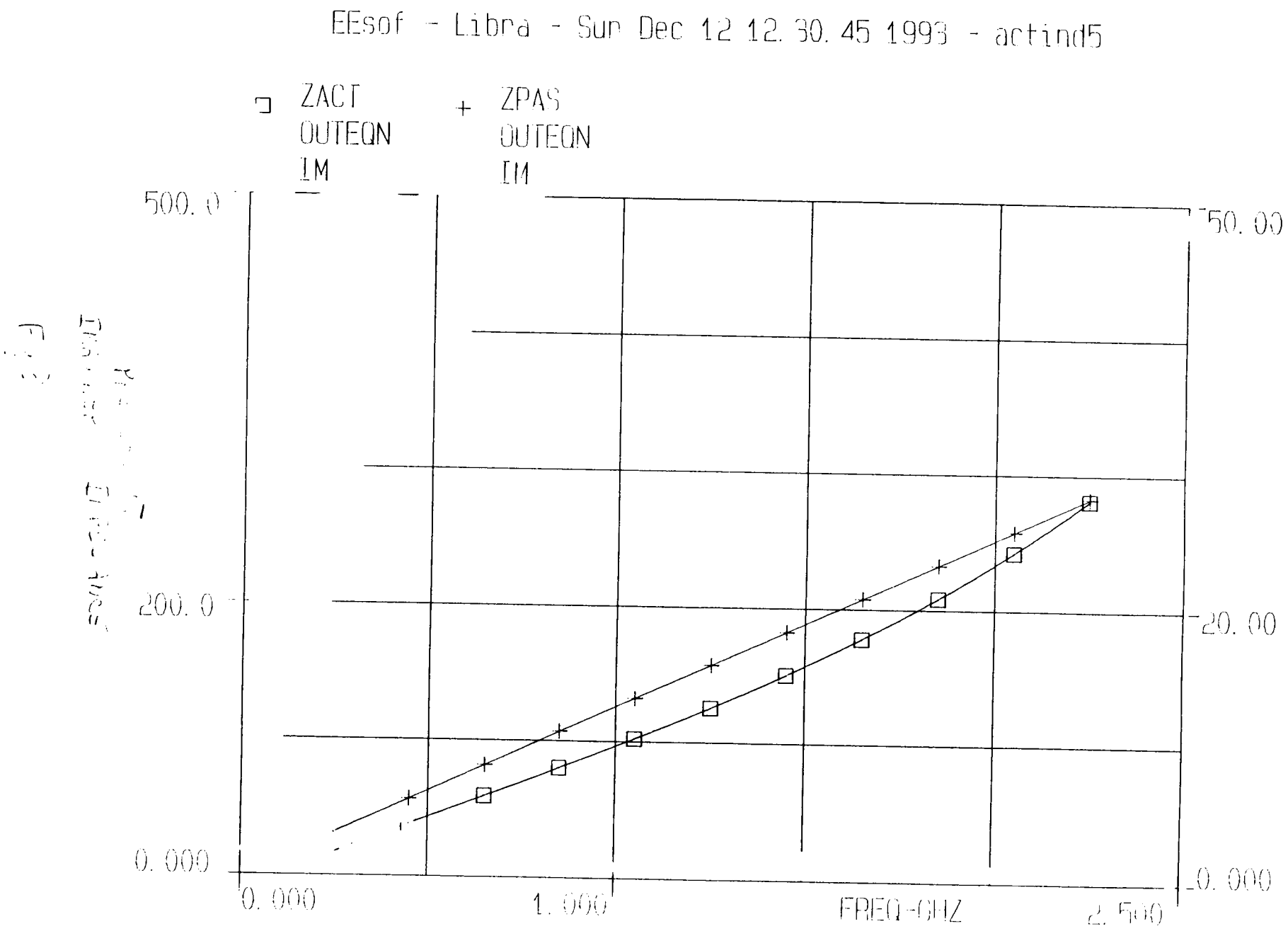
MAG
MU2
OUTEQN
MAG
2.000
1.000
0.000
0.000
1.000
FREQ-GHZ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IM
ZPAS
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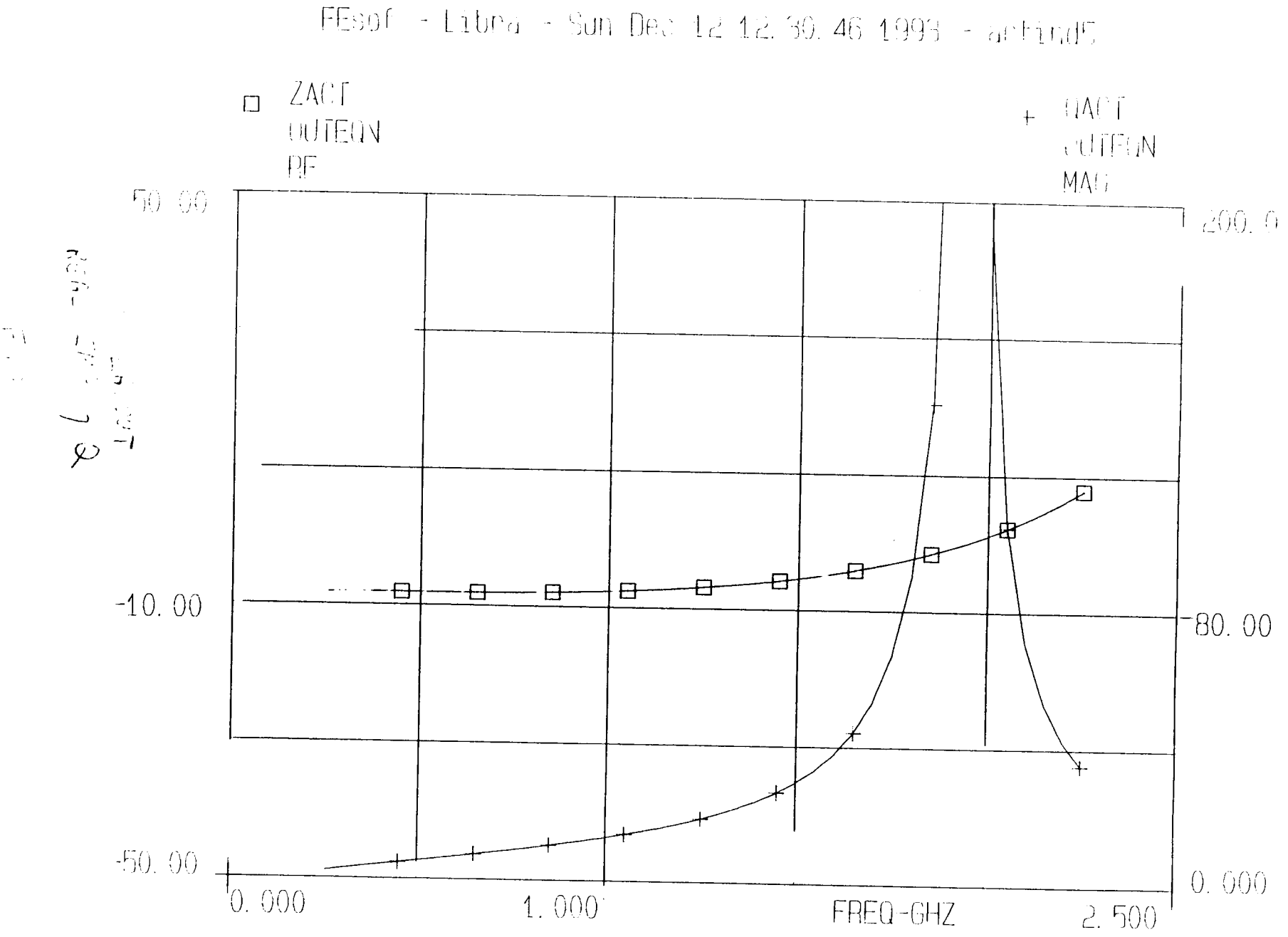
-20.00
-0.000
0.000
1.000
FREQ-GHZ
2.500


FEsof - Libra - Sun Dec 12 12:30:46 1993 - ar
ZACT
OUTEQN
RF
ZACT
OUTEQN
MAG
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200.0
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0.000
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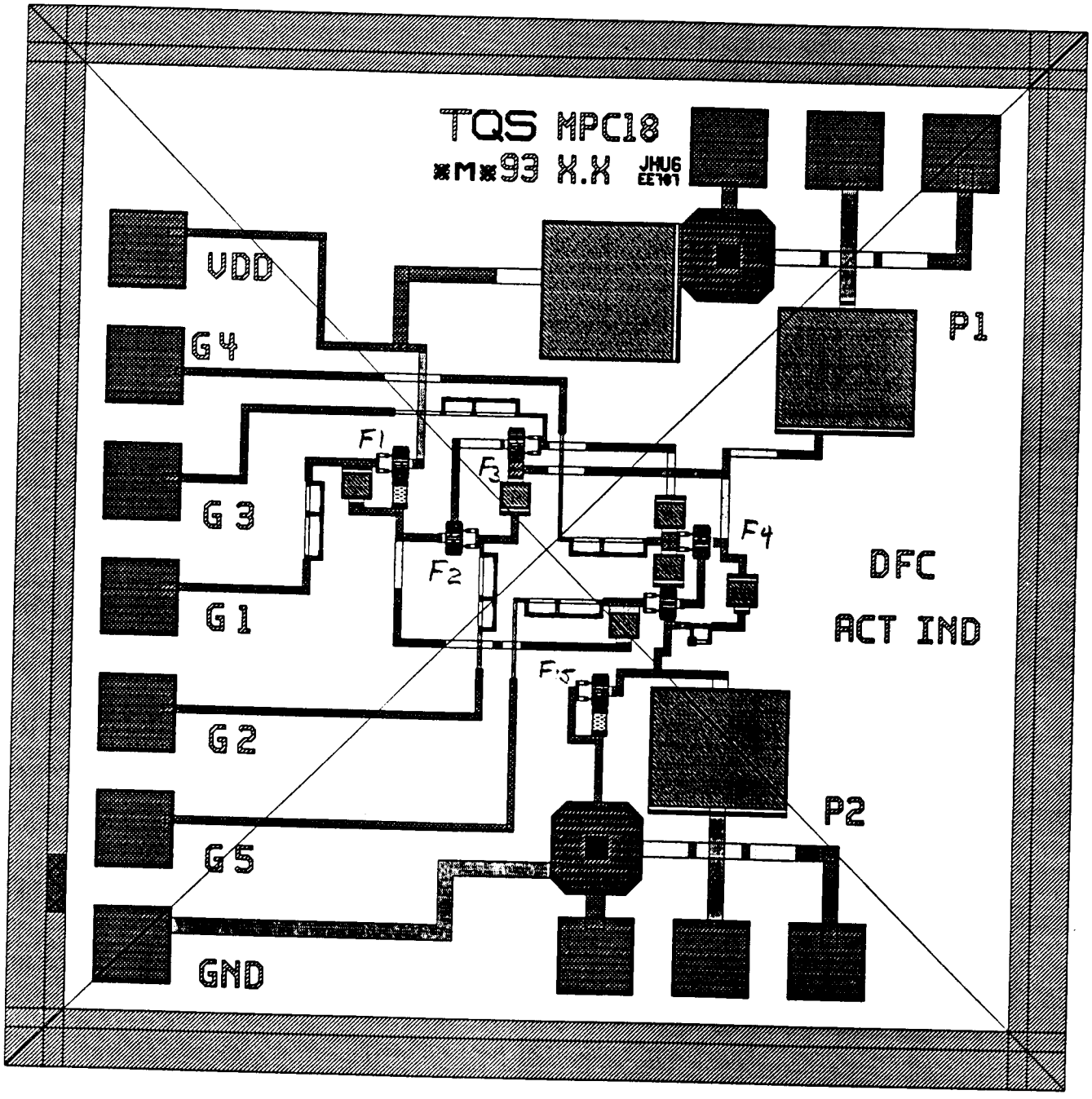
FREQ-GHZ
2.500



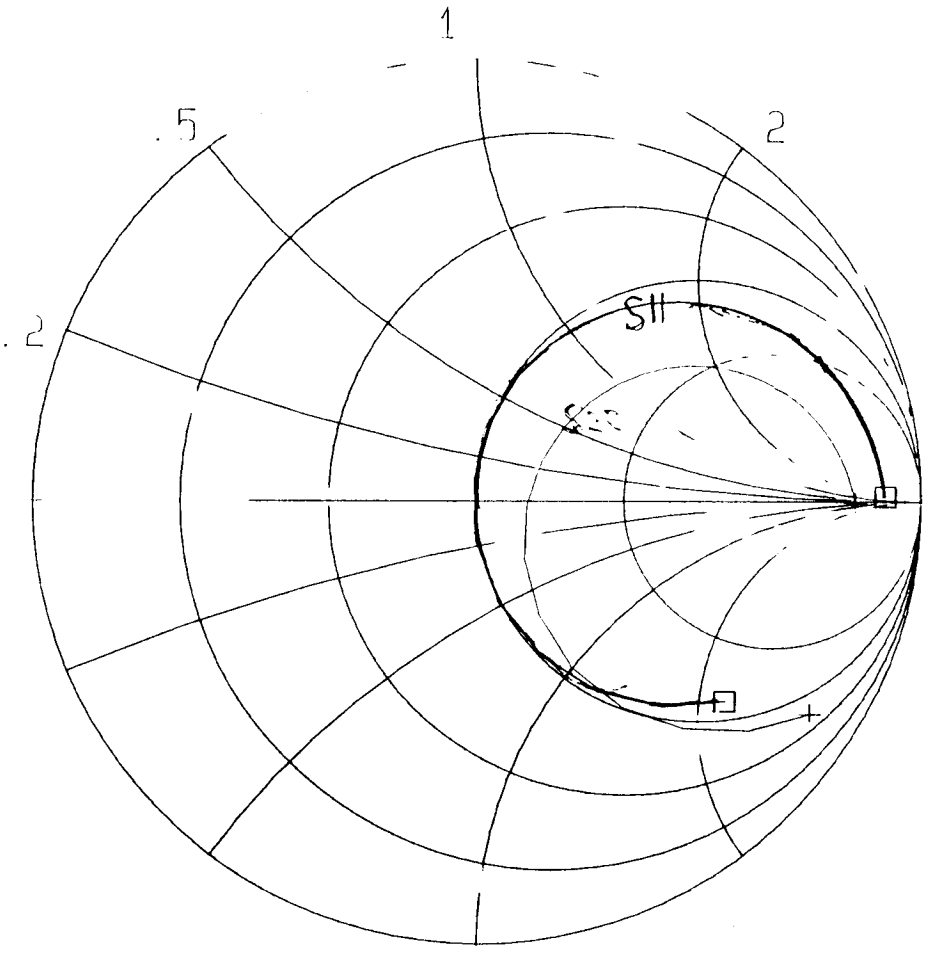
FINAL LAYOUT

FIG 10

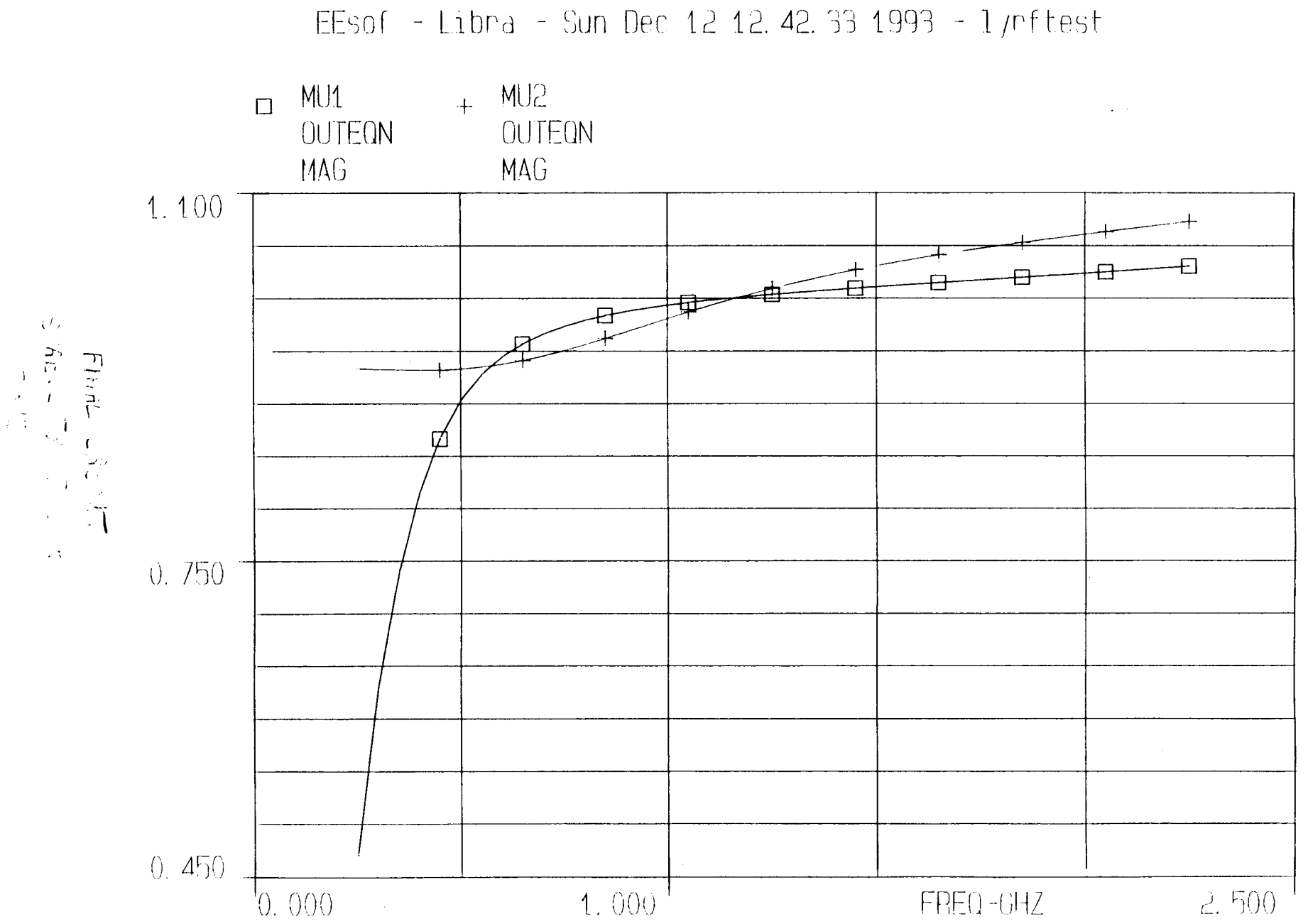
EEsof - Libra - Sun Dec 12 12:42:34 1993 - lynftest

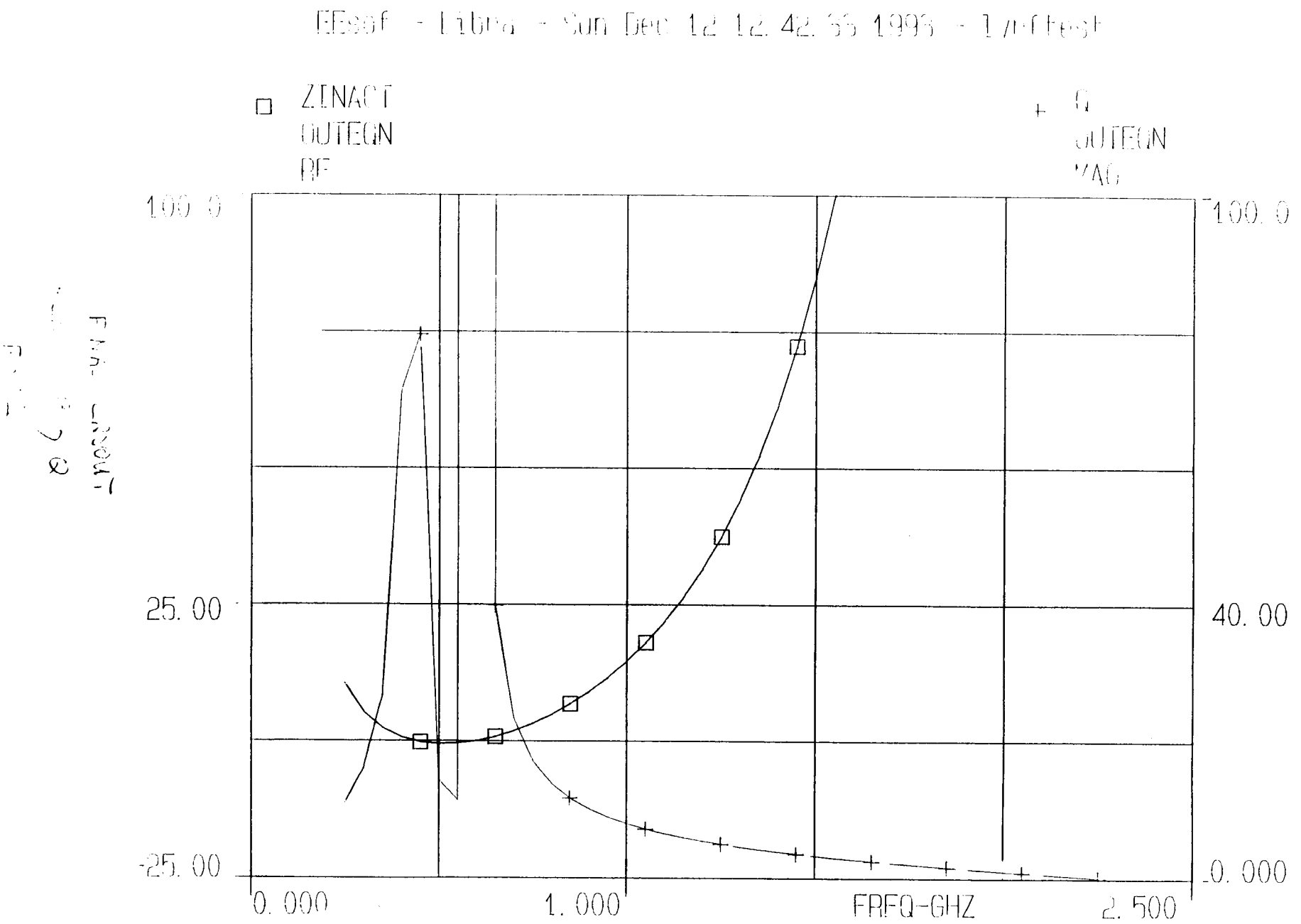
□ S11
ACTIND

+ S22
ACTIND



F1 0.25000
F2 4.25000


EEsof - Libra - Sun Dec 12 12.42.33 1993 - 1/rftest
MU1
OUTEQN
MAG
MU2
OUTEQN
MAG
1.100
0.750
0.450
0.000
1.000
FREQ-GHZ
2.500


EEsof - Libra - Sun Dec 12 12:42:55 1993 - Untitled
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RF
OUTEQN
MAG
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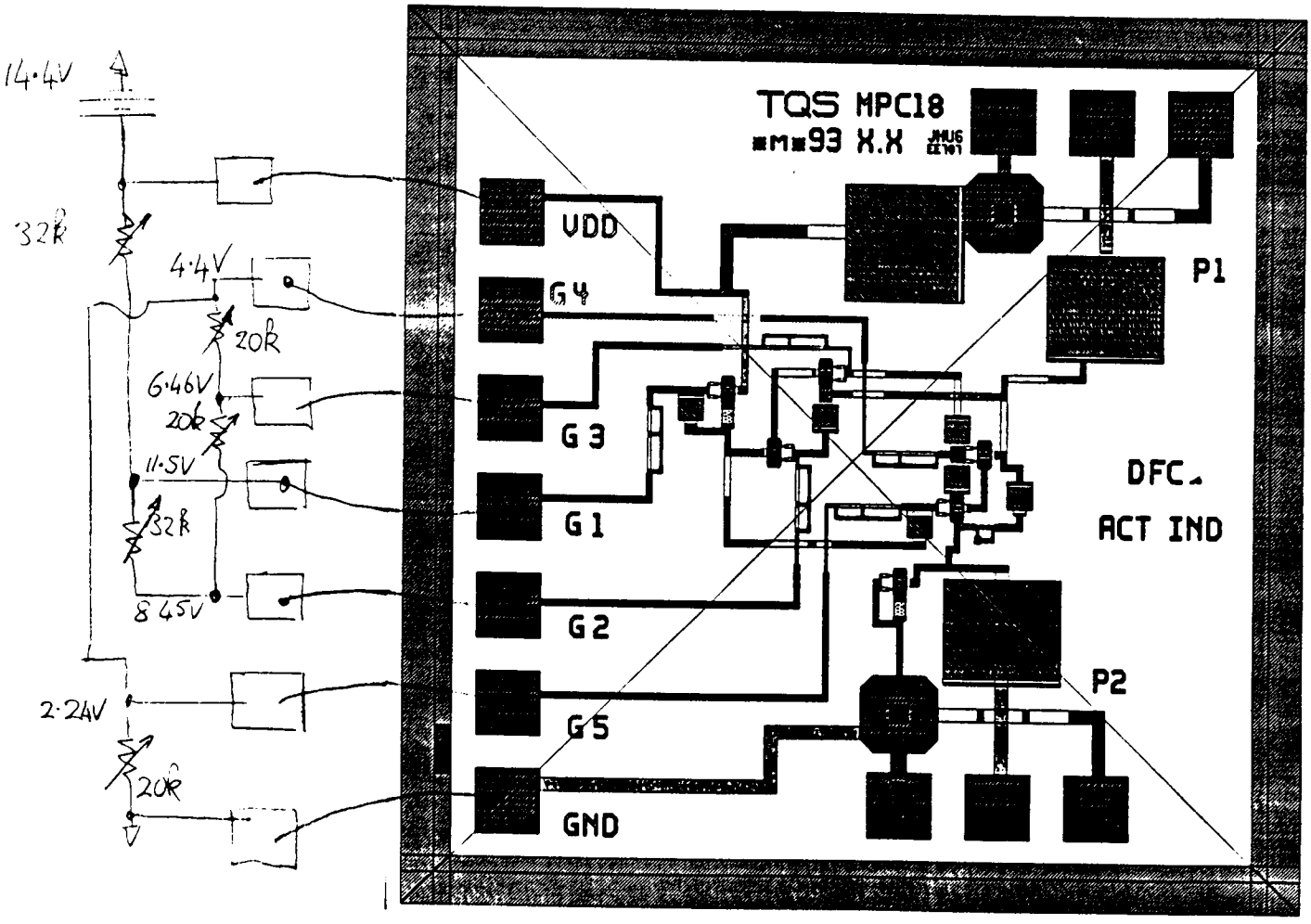
-25.00
100.0
40.00
0.000
0.000
1.000
FREQ-GHZ
2.500



TEST FIXTURE

Fig 15

A 5.654 GHz LNA

Design By:

Konstantinos S. Bantzis

12-13-93

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I. Summary

This team project consisted of designing an MMIC low noise amplifier with on-chip matching and provisions for an off-chip matching network. The primary specifications were ~3.5 dB NF with 20 dB of gain and good input and output VSWR. The required center frequency was 5.654 GHz with 100 MHz bandwidth. The foundry used for this design was Triquint and the devices chosen were 300 μm GASFETs.

The design consists of two GASFETs with input, interstage and output matching networks. Two FETs were required to meet the gain requirements. The matching networks were first designed using lumped elements and then transfered to standard Triquint elements. Due to the chip size restrictions it was necessary to try and simplify the matching networks. The final matching networks consisted of a shunt capacitor and a series inductor at the input a series inductance between the devices and a series inductance at the output. Both devices were self biased to approximately 20% Idss. Inorder to reduce the size of the bias network, each device is biased using a 60 μm GASFET operating at Idss.

Overall, the design was successful. The final computer simulations predict a 4dB NF with 18dB of Gain, very good VSWR at both the input and output and excellent stability.

II. Introduction

The circuit primarily consists of two GASFETs self biased to 20% Idss, with on-chip matching networks and provisions for off-chip input and output matching networks. In order to reduce the required chip size the matching networks have been reduced to lumped basic elements and the bias is supplied through active devices sized to provide the proper operating current.

The input matching network is entirely contained on the chip but provisions have been made to accomadate an off-chip matching network. The pad labeled, "RF IN", is the 50 Ω input to the chip. The pads on either side of the input are connected to ground vias and are spaced to provide the proper transition from a coplanar probe station. A small piece of 50Ω line connects the input pad to a shunt 700 FF capacitor. The shunt capacitor along with the 2000 pH series inductor and interconnecting lines that follow make up the input matching network. A 5000 FF capacitor has been added for input dc blocking. The circuit has a small piece of airbridge between the blocking cap and the gate of the first 300 µm GASFET. This airbridge can be broken so that an off-chip matching network can be used. An off-chip input matching circuit can be connected to the pad labeled, "FET IN". This pad is connected to the gate

of the first FET by a 10 μm microstrip line and a small piece of airbridge. When the on-chip matching network is used this airbridge must be broken.

The interstage matching network consists of only a 2500 pH series spiral inductor. A 5000 FF blocking capacitor and some 10μm microstrip line connect the spiral inductor to the gate of the second FET.

The output matching network again consists of only a series 2500 pH spiral inductor. A 5000 FF blocking capacitor and some 10μm microstrip line connect the spiral inductor to the 50Ω output pad. This pad is labeled "RF OUT". The 100μm pads on either side are both connected to a ground via and have been appropriately spaced to provide the coplanar transition for the probe station. Another pad labeled, "FET OUT" has also been added to provide a connection to an off-chip matching network. A small piece of airbridge has been added just before the input to the spiral inductor. This airbridge must be broken when the off-chip output matching network is used, otherwise the airbridge that connects this pad must be broken. Although even if this connection is not broken it will not hurt the on-chip matching network.

Both FETs are self biased to 20% Idss through one or two 5V supplies. The bias is connected to the chip at the two pads labeled 5V. Each pad is connected to the drain of a 50 μm FET who's source is then connected

to the drain of the 300 μm FET. The gate of each 60 μm FET is connected to its source, therefore operating at Idss and providing approximately a 20% Idss and 2.5V bias to the 300 μm FET. A 5000 pF capacitor in parallel with a 100 Ω NiCr resistor is connected between the source and ground. The resistor provides the proper bias for the transistor while the capacitor provides a good RF short. Each gate of the 300 μm FET is connected to ground through a 1000 Ω NiCr resistor.

Standard amplifier design techniques were used for this project although several iterations were required in order to simplify the matching circuit and meet the size constraints. A lumped element matching circuit was first designed to meet the amplifier performance requirements. This circuit was optimized to reduce the number of elements and then implemented using Triquint elements. The design was again optimized to meet performance and size requirements. Self biasing of the FETs was preferred for this design since it eliminates the need for a negative supply. The active bias eliminates the need for large bias inductors. The same bias circuit is used for both on and off-chip matching.

As with all low noise amplifier designs there is a trade-off between NF, gain and input match. In this design NF and gain were slightly compromised in order to produce a good input match. An amplifier without a good input match can be a problem in any system.

III Specification compliance matrix.

	Specification	Modeled performance
Frequency:	5654 MHz	5654 MHz
Bandwidth:	100 MHz	300 MHz
Gain:	>30dB	18dB
Gain Ripple	± 0.5dB max	± 0.33dB max
Noise Figure	<3.5 dB goal	4.1 dB
Input VSWR	< 2.0:1	< 2.0:1
Ouput VSWR	< 1.5:1	< 1.5:1
Supply Voltage	±5V, single +5V goal	+5V

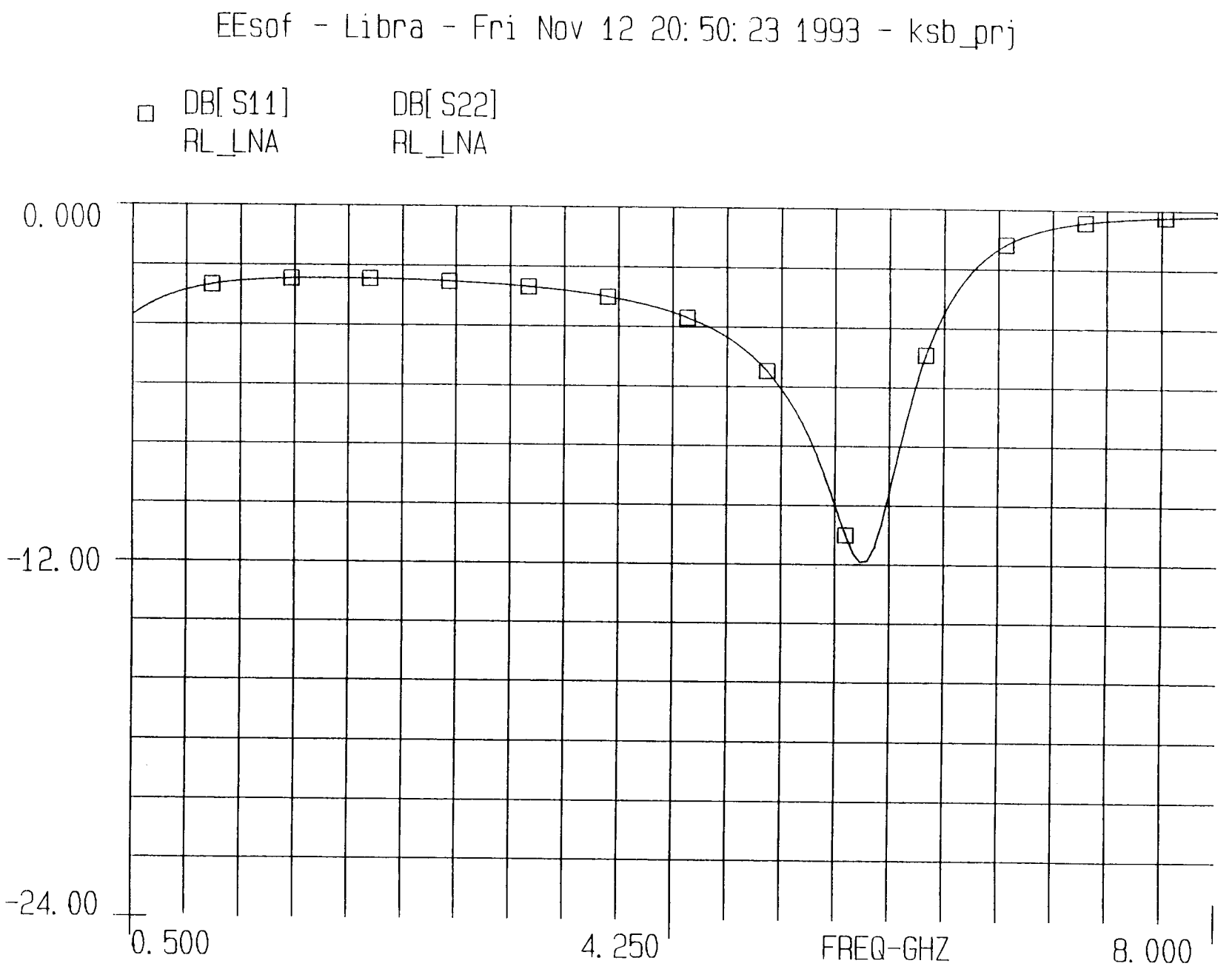


Fig 4B Performance results of optimized [illegible]

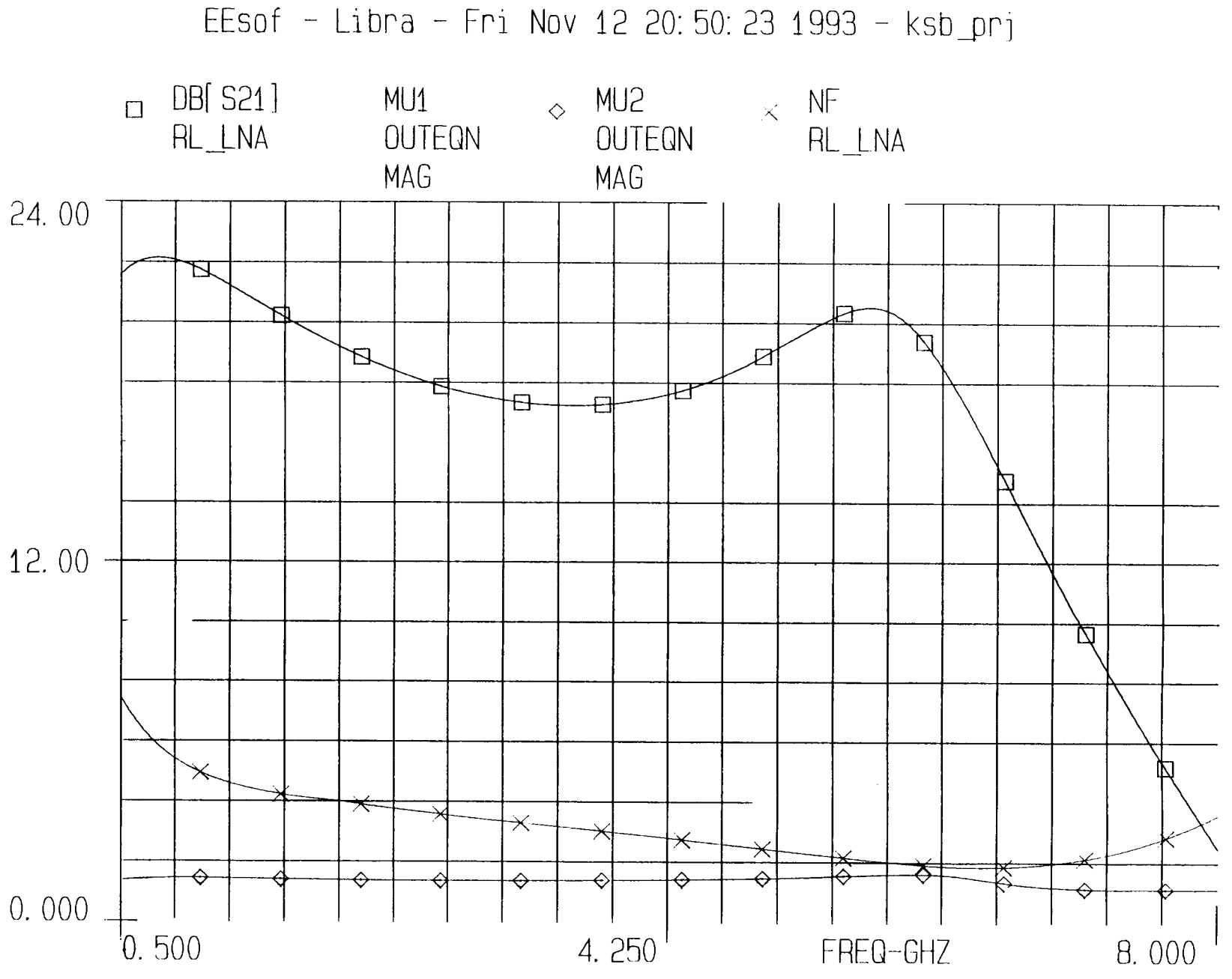
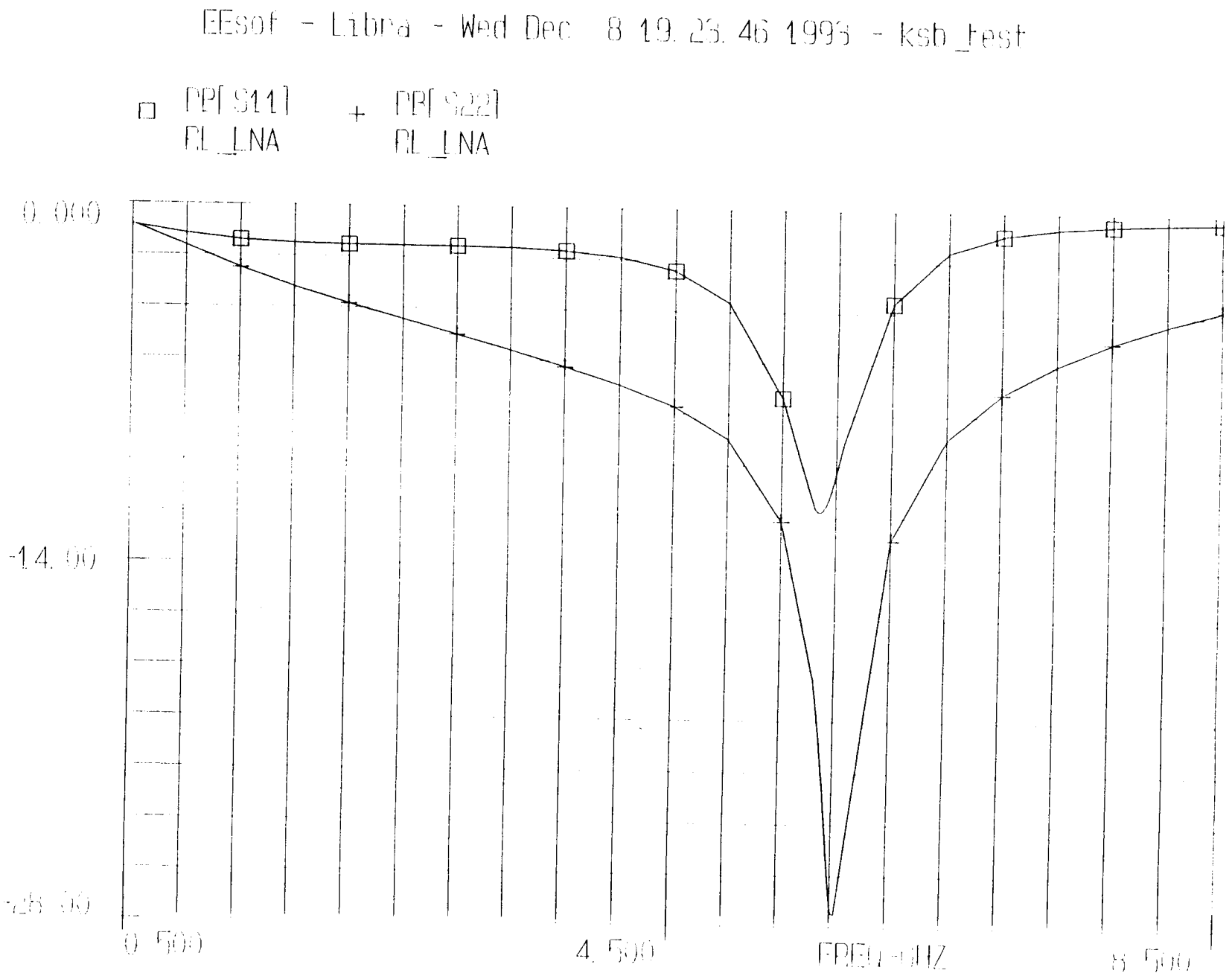


Fig. 4A Performance results of optimized lumped element LNA


EEsof - Libra - Wed Dec 8 19:23:46 1993 - ksh_test
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DL_LNA
PP[S22]
DL_LNA
0.000
-14.00
0.500
4.500
FREQ,GHz
8.500

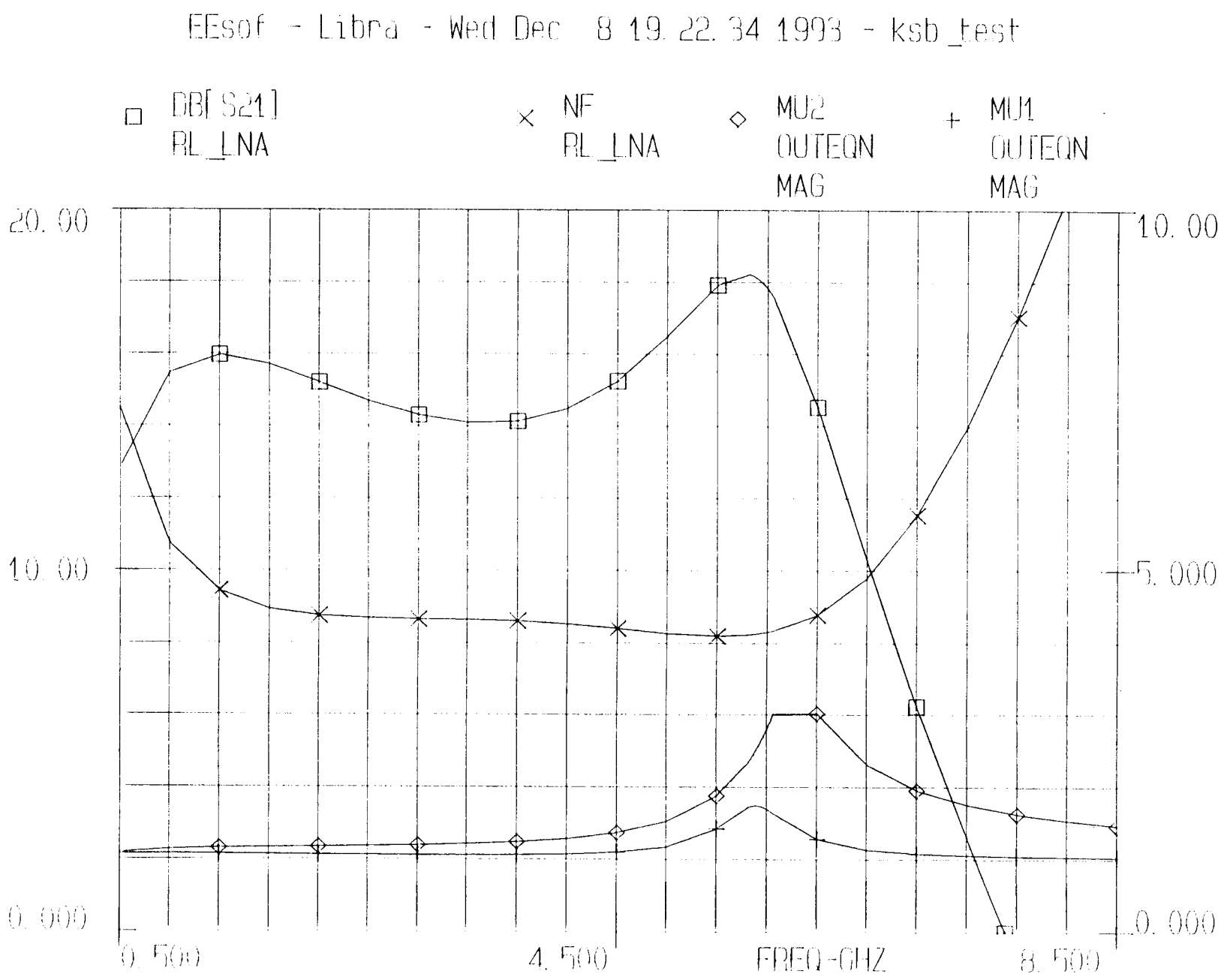


Fig 5B - Performance results for final design.

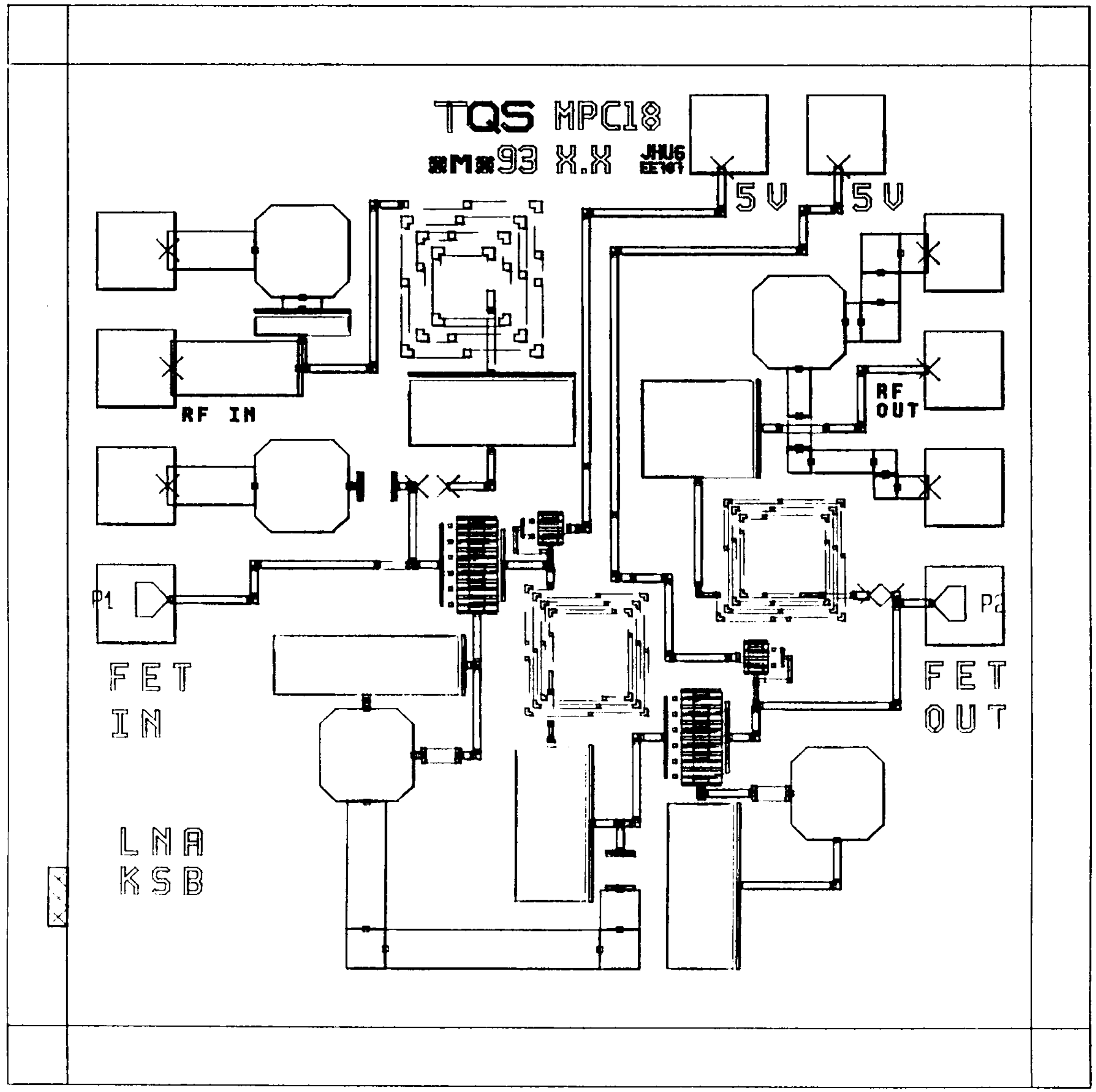
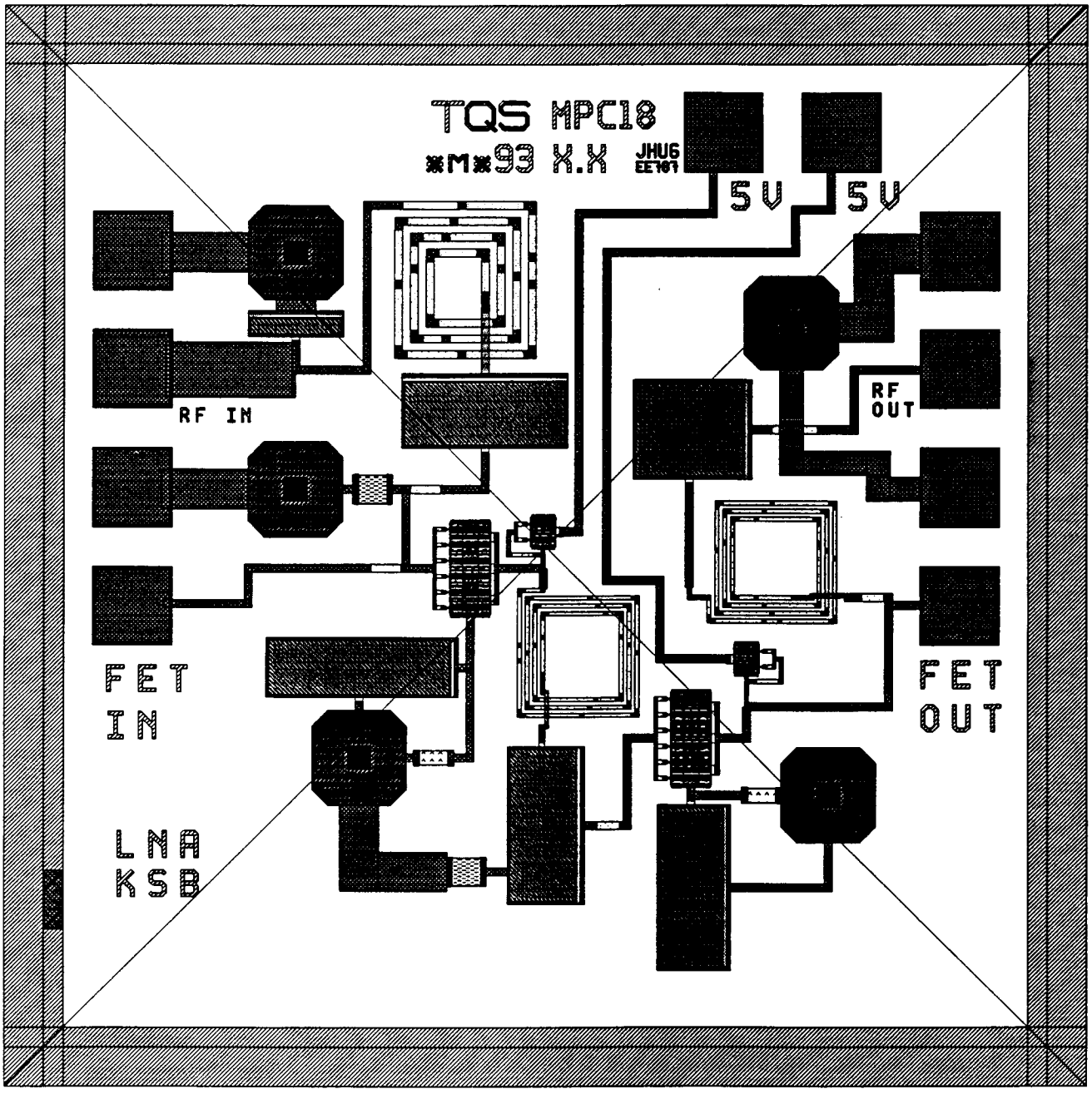


Fig 2 - Final layout showing ports and broken airbridge locations for off-chip matching.


TQS MPC18
*M*93 X.X
JHUG
EE101
5V
5V
RF IN
RF OUT
FET IN
FET OUT
LNA KSB

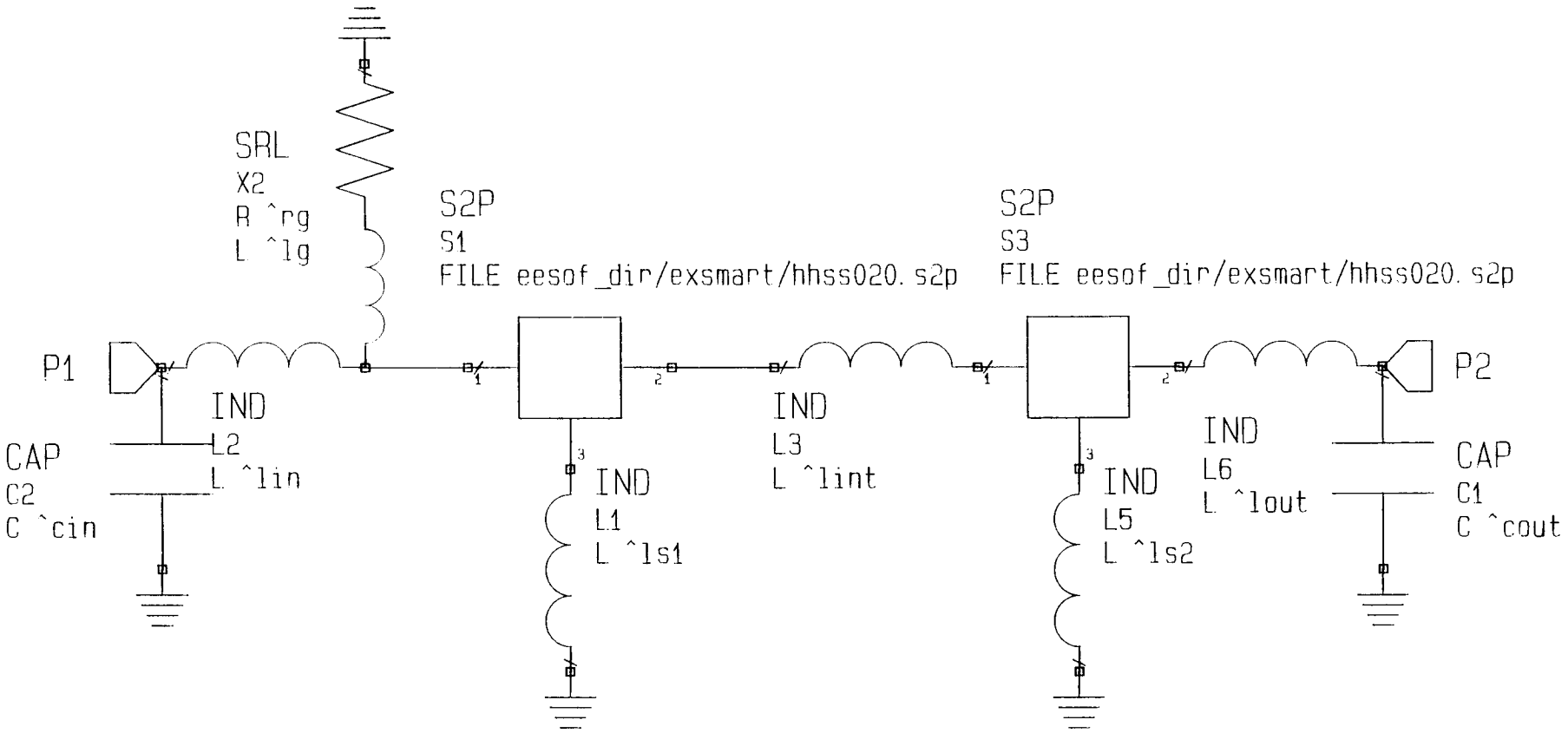


Fig. 3 schematic of lumped element amplifier

V. DC Analysis

A dc analysis was conducted before and after the final layout. Each 300 μm FET is biased at 2.5V and 4 mA. These devices have an I_{DSS} of approximately 44 mA. At 20% I_{DSS} the devices are properly biased for low noise operation. The active bias will help maintain the device bias given the tolerances involved with the processing.

All of the necessary components have been checked for current steals. The interconnect lines are primarily 10 μm wide and the source resistors are 18 μm wide N+. The gate resistors are 1000 Ω at 36 μm wide.

II Design Robustness

The simplicity of this design helps eliminate many of the problems involved with component tolerances. All interconnecting lines were kept 10μm wide. The small tolerance involved with obtaining this linewidth will not effect the performance. A 5% change in the series inductors was found to not effect the performance of the amplifier. The most sensitive component is the shunt capacitor at the input. This component also has the largest tolerance. The value of the capacitor was changed by ±10% and the results are shown in the attached figures. As the plots illustrate, even a ±10% change in the capacitance will not seriously compromise overall performance. The amplifier has been tuned over twice the required bandwidth and will therefore be more tolerable to component tolerances.

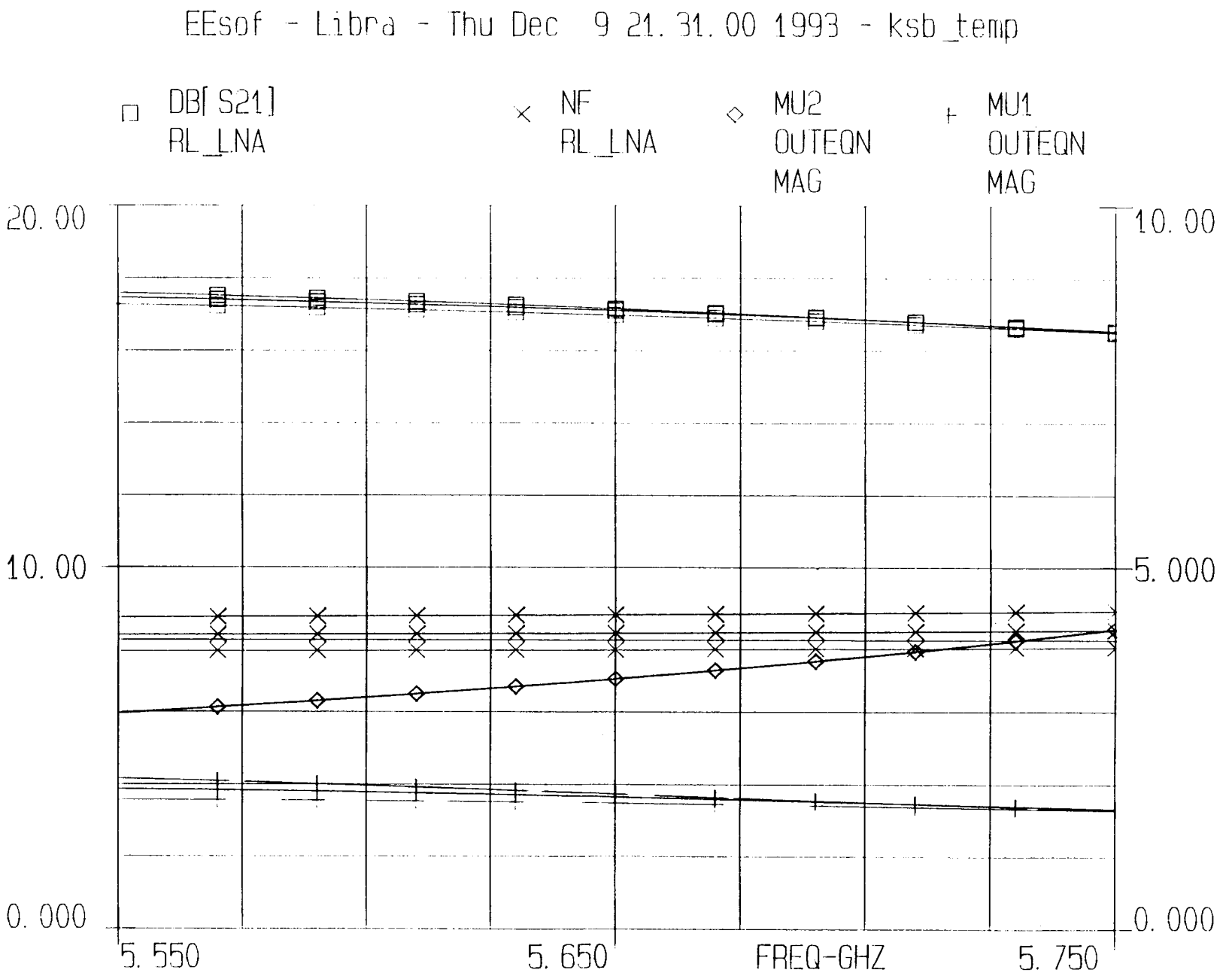


Fig. 6A Effect on circuit performance ± 10% change

EEsof - Libra - Thu Dec 9 21:30:59 1993 - ksb_temp

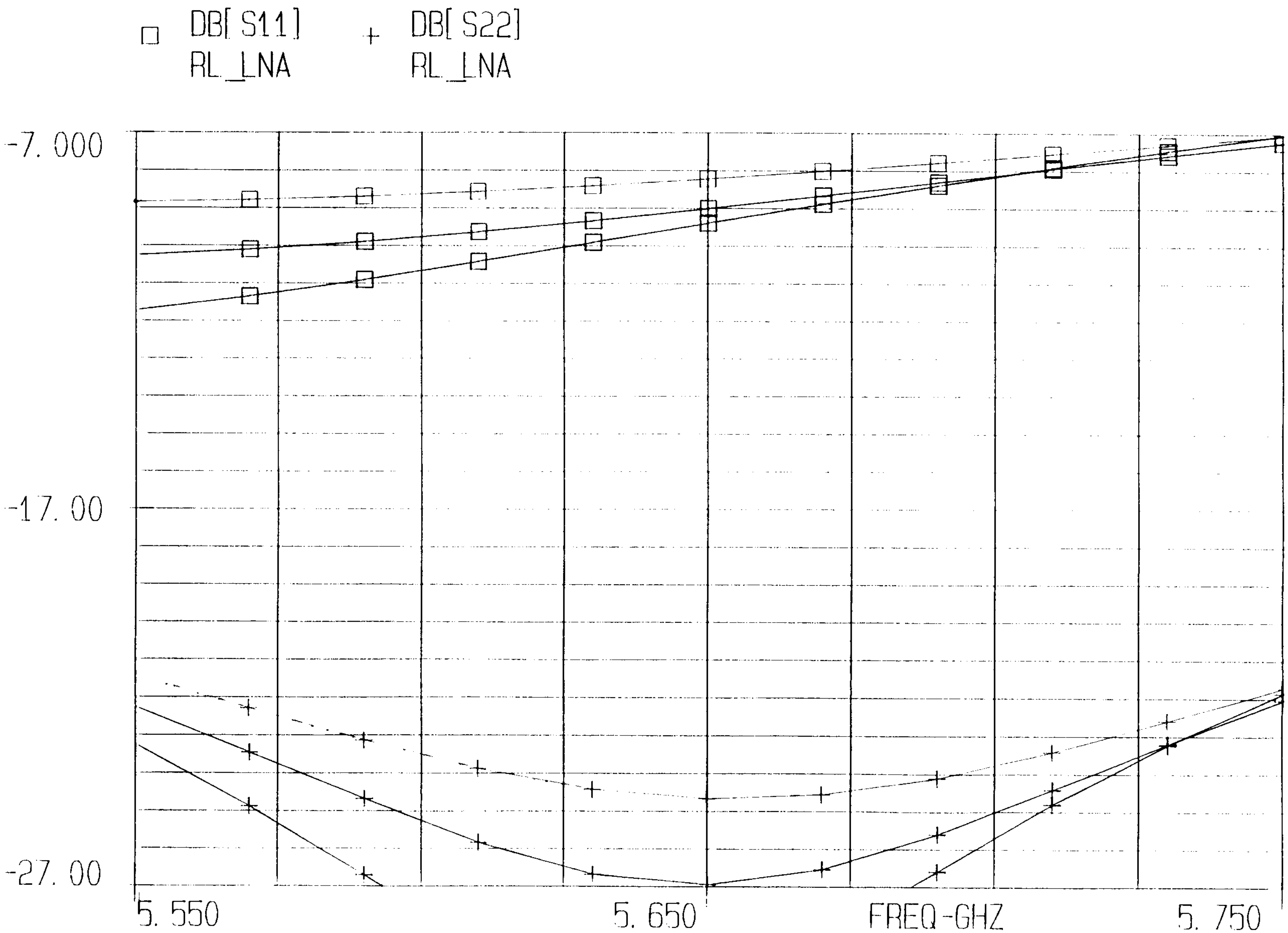


Fig 6B Affect on circuit performance at ± 10% change

VII Test Plan

The equipment required for testing are a network analyzer, a probestation and a noise figure meter or a spectrum analyzer and calibrated noise source.

The network analyzer and probe station can be used to measure gain and input and output VSWR. The noise figure meter is required to measure noise figure. If one is not available, a noise source can be connected to the input with a spectrum analyzer connected to the output. The NF of the amp can be calculated from the difference in the noise floor when the noise source is switched on and off.

VIII Conclusions and recommendations

Overall the design task was very successful. The final simulations show very good performance over more than twice the required bandwidth. Since the amplifier has been tuned over a much broader bandwidth component tolerances will have a much smaller affect on its performance. A seperate 5V pad has been provided for each transistor. These pads can either be directly connected or isolated through seperate supplies. The use of seperate supplies will help reduce the risk of possible oscillations and provide flexibility in the biasing of each device.

Provisions have been made to accommodate off-chip matching networks. The airbridges that must be broken have been identified in Fig. 2. If an off-chip matching network is desired then S-parameters must be measured at the input and/or output to the chip after the transition has been made to a carrier. The actual S-parameters can then be compared to the simulation and the differences explained. Using this corrected data an off-chip input and/or output matching network can be developed. A good off-chip input matching network may reduce the noise figure by .5 dB and increase gain by 1 dB. An off-chip output matching network may increase gain by .5dB. An off-chip input matching network can be used alone. Depending upon the overall chip response this may be the prefered method.

```
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RES            OH
COND          /OH
IND            PH
CAP            FF
LNG            UM
TIME           PS
ANG           DEG
VOL             V
CUR            MA
PWR           DBM
VAR

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lint =72.0000000000
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wl2 =59.4110700000
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INDOUT %2500.00000000 1.00000000000
EQN

CKT

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RGH=0.50000000000
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GWID=30.0000000000 FNUM=2.00000000000 STAT=0.00000000000 TEMP=25.0000000000 &
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MCORN_T17 4 5 W=5.00000000000
MLIN_T20 3 6 W=5.00000000000 L=5.00000000000
MLIN_T21 2 7 W=10.0000000000 L=10.0000000000
MTEE_T53 6 10 11 W1=5.00000000000 W2=5.00000000000 W3=5.00000000000
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MLIN_T72 12 11 W=5.00000000000 L=9.00000000000
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DEF2P 7 10 BIAS
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RGH=0.50000000000
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TQSIND_L2 66 4 L^INDINT AIN=90.0000000000 AOUT=-90.0000000000 MIR=1.00000000000
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OCT=1.00000000000
TQSRESL_R3 82 70 TECH=30.0000000000 L=50.0000000000 R=100.000000000
MLIN_T54 81 73 W=10.0000000000 L=100.000000000
MCORN_T55 74 73 W=10.0000000000
MLIN_T56 74 75 W=10.0000000000 L=30.0000000000
MLIN_T57 44 46 W=50.0000000000 L=110.000000000
MLIN_T58 41 76 W=50.0000000000 L=110.000000000
MTEE_T59 72 6 78 W1=10.0000000000 W2=10.0000000000 W3=10.0000000000
MLIN_T60 6 79 W=10.0000000000 L=10.0000000000
MLIN_T61 78 80 W=10.0000000000 L=30.0000000000
MCORN_T62 79 81 W=10.0000000000
TQSRESL_R4 71 80 TECH=11.0000000000 L=50.0000000000 R=1000.00000000
MLIN_T63 69 82 W=10.0000000000 L=60.0000000000
MLIN_T64 7 68 W=10.0000000000 L=53.0000000000
MBEND_T65 83 68 W=10.0000000000 ANG=90.0000000000 M=0.00000000000
MLIN_T67 84 85 W=10.0000000000 L=30.0000000000
MLIN_T69 97 87 W=10.0000000000 L=170.000000000
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MTEE_T74 85 96 97 W1=10.0000000000 W2=5.00000000000 W3=10.0000000000
MLIN_T75 92 93 W=5.00000000000 L=10.0000000000
BIAS_X3 91 93
BIAS_X4 98 86
MLIN_T76 96 86 W=5.00000000000 L=25.0000000000
MLIN_T77 23 83 W=10.0000000000 L=119.500000000
MLIN_T78 64 29 W=10.0000000000 L=16.0000000000
MCORN_T79 87 88 W=10.0000000000
TQSMLIN1_T80 54 89 W=5.00000000000 L=40.0000000000
MSTEP_T81 89 90 W1=5.00000000000 W2=10.0000000000
MLIN_T82 90 100 W=10.0000000000 L=20.0000000000
MCORN_T83 95 99 W=10.0000000000
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MLIN_T85 98 94 W=10.0000000000 L=70.0000000000
MCORN_T86 101 94 W=10.0000000000
MLIN_T87 101 102 W=10.0000000000 L=90.0000000000
MBEND_T88 102 103 W=10.0000000000 ANG=90.0000000000 M=0.00000000000
MLIN_T89 103 104 W=10.0000000000 L=39.2500000000
MLIN_T93 21 105 W=5.00000000000 L=20.0000000000
MCORN_T94 106 105 W=5.00000000000
MLIN_T95 106 107 W=5.00000000000 L=10.0000000000
MSTEP_T96 107 108 W1=5.00000000000 W2=10.0000000000
MLIN_T97 108 109 W=10.0000000000 L=130.000000000
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OCT=1.00000000000
MLIN_T98 56 2 W=50.0000000000 L=20.0000000000
MCORN_T99 2 58 W=50.0000000000
MLIN_T100 58 111 W=50.0000000000 L=38.0000000000
MCORN_T101 112 111 W=50.0000000000
MLIN_T102 112 113 W=50.0000000000 L=35.0000000000
MLIN_T103 110 114 W=10.0000000000 L=25.0000000000
MLIN_T104 19 115 W=30.0000000000 L=60.0000000000
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TQSMLIN2_T106 114 117 W=10.0000000000 L=60.0000000000
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MCORN_T110 121 120 W=30.0000000000
MLIN_T111 121 122 W=30.0000000000 L=3.00000000000
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MLIN_T113 123 124 W=30.0000000000 L=40.0000000000
MLIN_T114 117 125 W=10.0000000000 L=40.0000000000
MCORN_T115 125 126 W=10.0000000000
MLIN_T116 126 127 W=10.0000000000 L=65.0000000000
MCORN_T117 128 127 W=10.0000000000
MLIN_T118 128 129 W=10.0000000000 L=80.0000000000
TQSVIA3_V8 57 32 13 W1=50.0000000000 W2=10.0000000000 W3=10.0000000000 &
OCT=1.00000000000
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MCORN_T121 60 59 W=50.0000000000
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MLIN_T125 132 60 W=50.0000000000 L=270.750000000
MLIN_T126 131 57 W=50.0000000000 L=161.500000000
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MLIN_T7 45 9 W=50.0000000000 L=15.0000000000
MLIN_T8 91 133 W=10.0000000000 L=5.00000000000
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PROC
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MODEL

SOURCE

DCTR

FREQ

SWEEP 5.55 5.75 .02
POWER

FILEOUT

OUTVAR

mag1 = rl_lna MAG[sb1]
mag2 = rl_lna MAG[sb2]
rad1 = rl_lna RAD[sb1]
rad2 = rl_lna RAD[sb2]
par1 = rl_lna PAR[sb1]
par2 = rl_lna PAR[sb2]

OUTEQN

mu1 = (mag1-rad1)*par1
mu2 = (mag2-rad2)*par2

OUT

!l_lna SB1 sc2
!l_lna NPAR sc2
rl_lna DB[s11] gr1
rl_lna DB[s21] gr2
rl_lna DB[s22] gr1
OUTEQN MAG[mu1] GR2A
OUTEQN MAG[mu2] GR2A
!l_lna S11 sc2
rl_lna NF GR2A
GRID

FREQ 5.55 5.75 .025
GR2 0 20 2
GR2A 0 10

HBCNTL

OPT
OUTEQN MAG[mu1]>1.5 10
OUTEQN MAG[mu2]>1.5  10
rl_lna db[s11]<0  10000
rl_lna db[s22]<0  10000
freq 5.55 5.75
rl_lna db[s11]<-10 10
rl_lna db[s22]<-12
rl_lna db[s21]>19  10
```

```
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rl_lna NF <3.5   100

YIELD
FREQ 5.55 5.75

YIELD  SENS    15

TRACE  ALL

rl_lna DB[S21]<20
rl_lna DB[S21]>16
rl_lna NF <5
rl_lna DB[S11]<-8
rl_lna DB[S22]<-10

rl_lna DB[S21] PH1
rl_lna NF      PH2
TOL
```

MMIC Design 525.787

Millimeterwave Absorptive SPST Switch

by

Adam DeWitt

December, 1993

The Johns Hopkins University

Abstract:

The objective of this project was to design an absorptive SPST MMIC switch operating at 37 GHz. The physical layout of the circuit was created to be compatible with the Martin Marrietta foundry process. Libra version 3.5 was utilized to perform the electrical simulation of the circuit. The following pages discuss the specific goals of the project and the design philosophy used to create the final circuit.

Introduction:

The fundamental switching component used in this project was a PHEMT transistor with the gate to source bias voltage varied. When the transistor is on, Vgs ≈ 0 Volts, the drain to source impedance should be very low. While a large negative bias , Vgs ≈ -3.5 Volts, should pinch of the path from drain to source. This characteristic was the foundation used to complete to create a switch for this project.

Before the switch could be designed, an accurate model of the transistor at the necessary frequency and bias operating points was required. This model was created by fitting the simple model shown in Figure 1 to VNA measurements taken on sample transistors. Component values derived for the two transistors tested are listed in the table below Figure 1. Once an accurate model was available, the design of the switch circuit could begin.

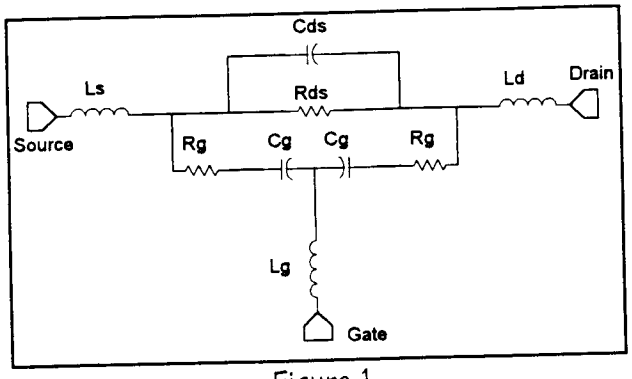


Figure 1

FET Size (μm)	Vgs (Volts)	Ls (pH)	Rds (Ω)	Cds (fF)	Ld (pH)	Lg (pH)	Rg (Ω)	Cg (fF)
50	0.25	20	32	15	20	20	18	33
50	-3.5	20	20K	15	20	20	18	20
200	0.5	20	6	250	20	20	6	100
200	-3.5	20	20K	45	20	20	6	55

The design of this circuit was broken into sections to make optimization more manageable. There were three types of single FET switches used to create the total circuit. Figure 1 illustrates how the three types of circuits were assembled to create the total switch. The first type was the matched shunt switch (SH1), which provides the match when the circuit is in the off state. An ideal circuit of this type would be an open circuit when off and a perfect match when on. The second type was the resonant series switch (SE1), which provides the forward on/off isolation. An ideal circuit of this type would be an open circuit when off and a short when on. The final type was the shorted shunt switch (SH2), which increased the loss in the off state. An ideal circuit of this

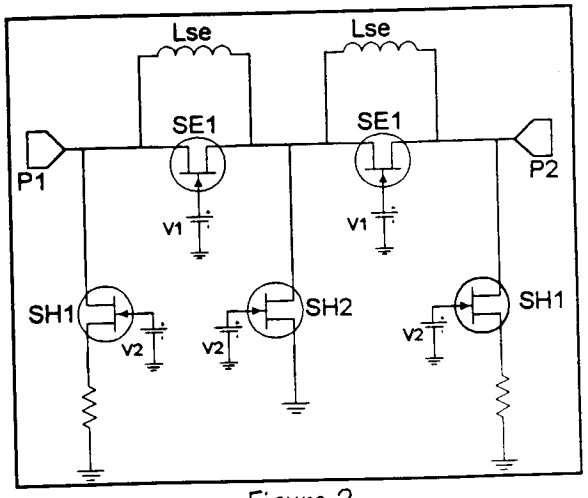


Figure 2

type would be an open circuit when off and a short when on. There were some other circuits used to ensure proper operation of the main circuits. This included the bias circuitry for the series switches, and also the quarter wave stub used for a ground reference. To better illustrate the operation of the total switch circuit a table showing the state of the single FET switches relative to the total switch state is shown below.

Total Switch	Matched Shunt(SH1)	Resonant Series(SE1)	Shorted Shunt(SH2)
On	Open	Short	Open
Off	50 Ω	Open	Short

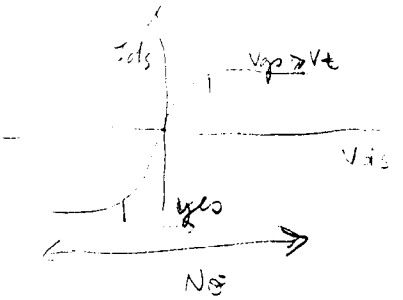
To try to minimize the on state insertion loss it was desirable to use the largest transistors available as the switching component of the series switches. The largest transistors available for model extraction were 8 X 25 μm (200 μm) PHEMTs. These transistors were also used for the shorted shunt switch, to produce the lowest impedance. For the matched shunt switch a smaller transistor would be better since it would produce a larger off impedance. The smallest transistors available were 4 X 12.5 μm (50 μm) PHEMTs. The high on state resistance of these transistors was easily compensated for with external circuitry. An important fact about the transistor operation for this circuit was that electrically the drain and source were interchangeable. But for the FET to operate as modelled, the DC gate to source voltage had to be correct. This required that there be a DC ground reference for each of the transistor sources.

Once the transistor models were available and the basic building block functions were defined, the realistic realization of this circuit could begin. The most difficult section to design was the series switch. The difficulty arose due to the high parasitic capacitances of the 200 μm PHEMTs. The gate capacitance made the circuit very susceptible to the impedance of the bias circuitry driving the transistor. It was decided to drive the gate of the series switches with a small pinched off transistor to eliminate this problem . The combination of the parasitic capacitances made the off state insertion loss of the series switch very low. To compensate for this situation a high impedance microstrip line was used to resonate the off state transistor capacitance. Designing the matched shunt switch was considerably easier. The circuit was implemented by placing a small resistance between ground and the source of a 50 μm transistor. The value of the resistor was adjusted until the circuit looked like a good match at 37 GHz. The shorted shunt switch was the easiest circuit of the three to implement. To ground the source as well as possible all lines were made as short as possible. The shorted stub present in the circuit is a DC ground reference for the transistor used in the matched shunt and series switches.

In the process of designing this circuit some very important trade-offs became apparent. It was decided that this switch would be absorptive rather than reflective in the off state. It quickly became obvious that a reflective circuit could be created with higher on/off isolation. The next trade-off encountered was between bandwidth and isolation. By resonating the series switches the bandwidth of the circuit has been lowered. It was determined that this sacrifice was necessary to get sufficient isolation at 37 GHz. Since the transistors of this circuit are driven by varying the gate voltage, additional transistors cause very little additional DC current. This fact may lead one to conclude that a switch

with many sections would be desirable to maximize the on/off isolation. The fault with this logic lies in the fact that every additional section will definitely increase the total circuits insertion loss while possibly increasing isolation. For this reason, it was decided to use the minimum number of sections necessary to achieve the required isolation. This decision was solidified by the fact that the amount of area available to implement the circuit was finite. Obviously more sections would make the circuit larger thus making the smallest number of sections the most desirable from a size point of view. As was mentioned above, if properly operated this circuit should require very little DC current. Because of this, it was safe to use thin resistors in the bias networks. It would have been desirable to use very large resistance values in some of the bias circuits. This was not an option, since there is not a layer with high sheet resistance available. One of the facts of life was that the size of the circuit interconnections were an appreciable portion of a wavelength at 37 GHz. This fact dictated that the line lengths and widths were important to the performance of the total circuit. Therefore it was crucial to include the interconnections in the design of the circuit. All of these effects were weighted against one another to arrive at the final design.

I have spent some effort to point out the difficulties and limitations of this design process. I would like to end this section by mentioning some of its advantages and capabilities. The largest advantage was the large amount of space available for the design. Since the frequency of operation was high and the die size was large no concessions had to be made on performance because something wouldn't fit. Also, the high operating frequency made the use of 50Ω lines possible. The choice of varying the drain to source resistance by varying the gate to source voltage creates a circuit with very low current consumption expected. Using the drain to source path of the transistor as the through path should yield a circuit with high power cut off. This is due to the fact that the transistor will not go into saturation until the microwave signal is large enough to swing over the entire operating range of the transistor. Because of the inherent advantages of this circuit the only difficult portion of the design was interconnecting the components without degrading the circuits performance.



Modeled Performance:

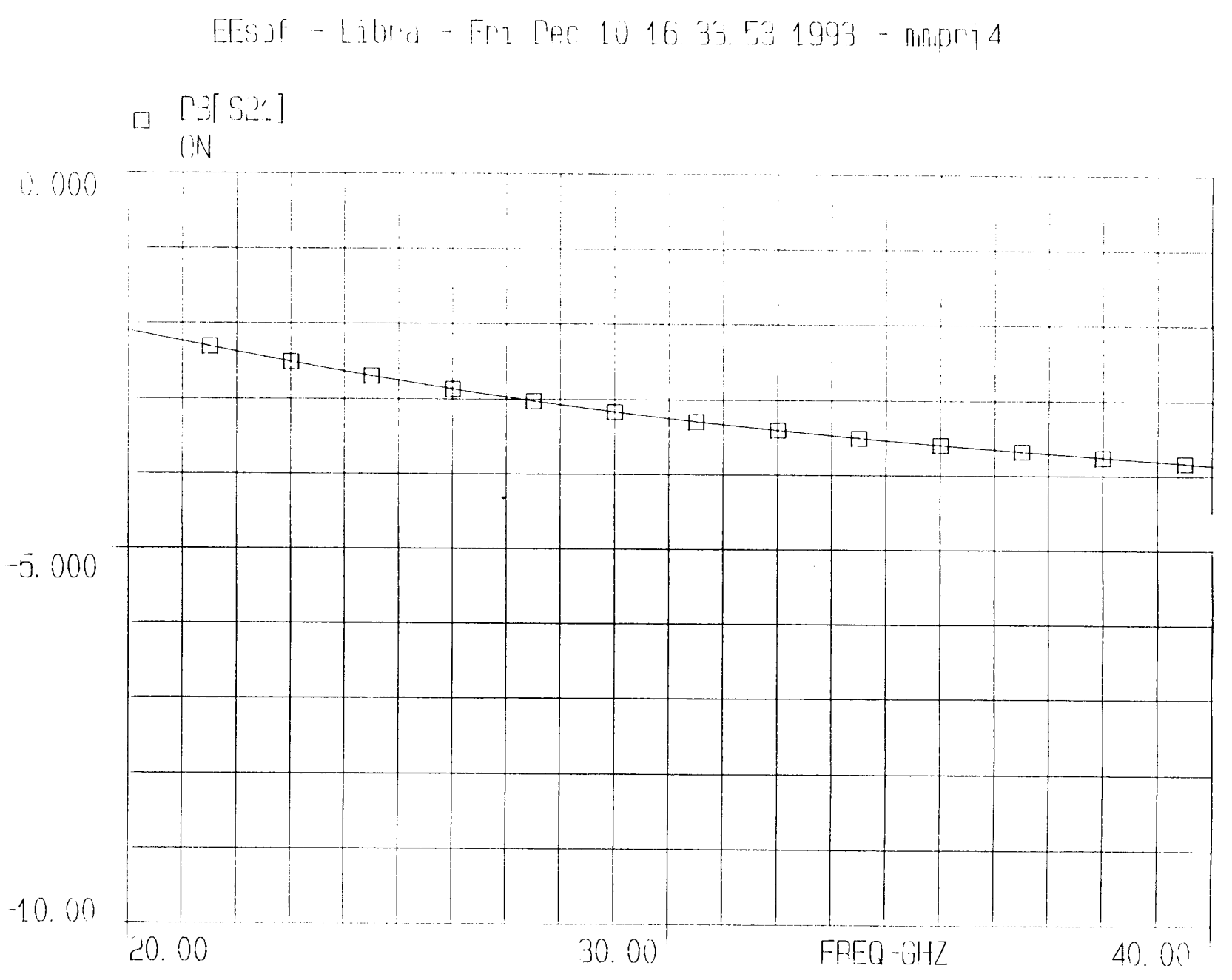
Following is a copy of the specifications as they were given. These guidelines were used to guide the optimization of the circuit during design.

SPECIFICATIONS FOR SPST CONSTANT IMPEDANCE SWITCH
p-HEMT switches internally terminated in 50 ohms

FREQUENCY:	37 GHz; 20 - 40 GHz, goal
INSERTION LOSS:	< 2 dB; 1 dB, goal
ISOLATION:	> 30 dB, goal
VSWR:	< 1.25:1 on.off, goal
CONTROL VOLTAGE:	TBD

It was found to be difficult to meet all of these specifications. During the design process it was decided which parameters could be flexed to allow realization of the others. In particular it was difficult to meet the VSWR and the isolation requirements simultaneously. It was instead to try to get good isolation with a decent VSWR. This came at the cost of making the circuit narrowband, as was mentioned previously. Because of the importance of the interconnections to the performance of this circuit I have included simulation plots of only the final layout. The plots included are of insertion loss (dB[S21]), input and output VSWR (VSWR1 and VSWR2) for the total switch on and off states, and the on/off isolation (dB[ISO]) versus frequency. The plots are on the following three pages in the order listed above. Below is the specification compliance matrix all predicted performance numbers are specified at 37 GHz. Since this report is being created before the circuit is fabricated, it can't have the results of the probed chip. As for the control voltage of the circuit, a shematic diagram and a truth table type of chart is included later in the report for that purpose.

Parameter	Specification	Goal	Modeled
Insertion Loss	< 2 dB	1 dB	4 dB
On/Off Isolation	> 30 dB	> 30 dB	40 dB
On State Input VSWR	< 1.25 : 1	< 1.25 : 1	< 2.65 : 1
On State Output VSWR	< 1.25 : 1	< 1.25 : 1	< 2.65 : 1
Off State Input VSWR	< 1.25 : 1	< 1.25 : 1	< 1.35 : 1
Off State Output VSWR	< 1.25 : 1	< 1.25 : 1	< 1.35 : 1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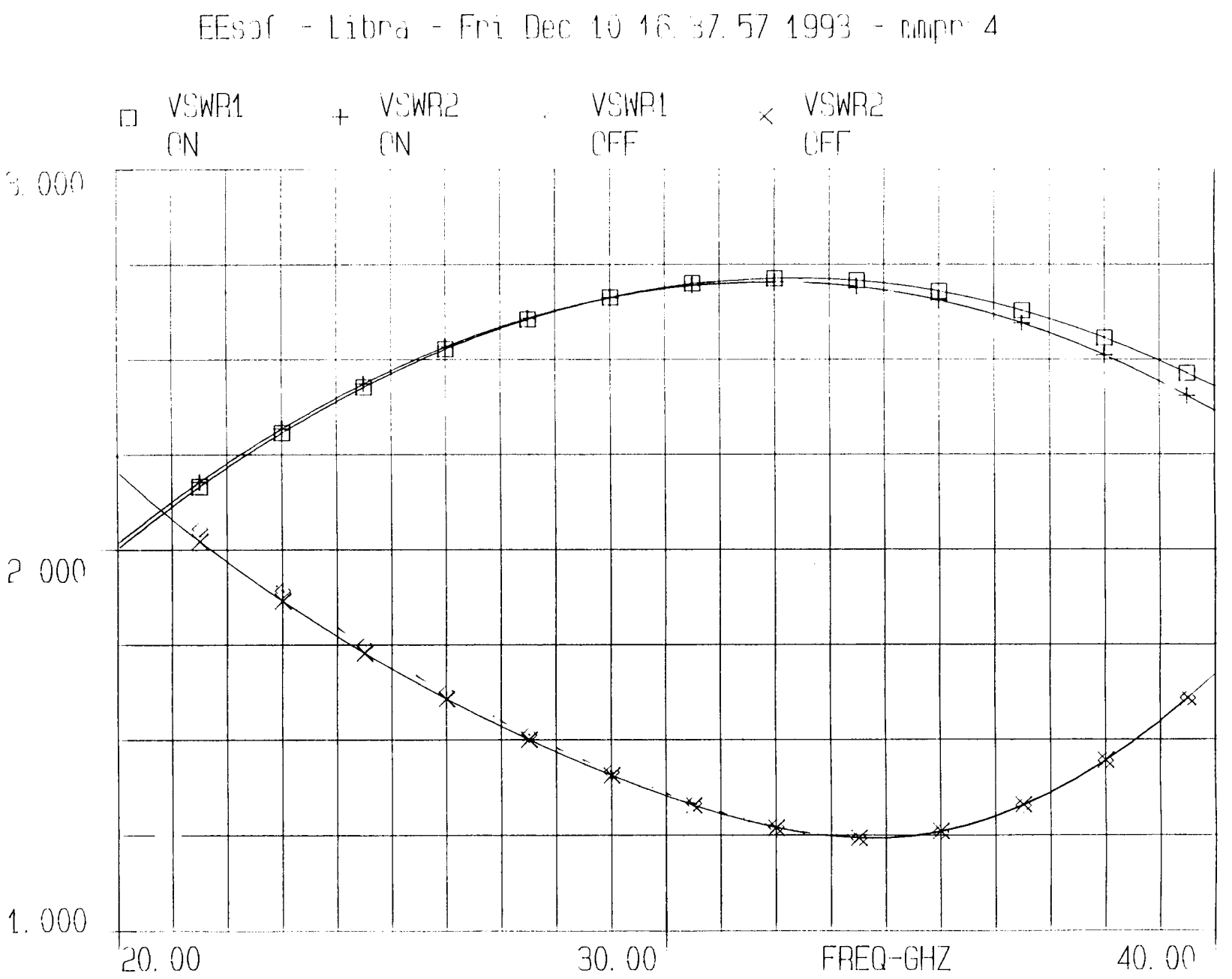
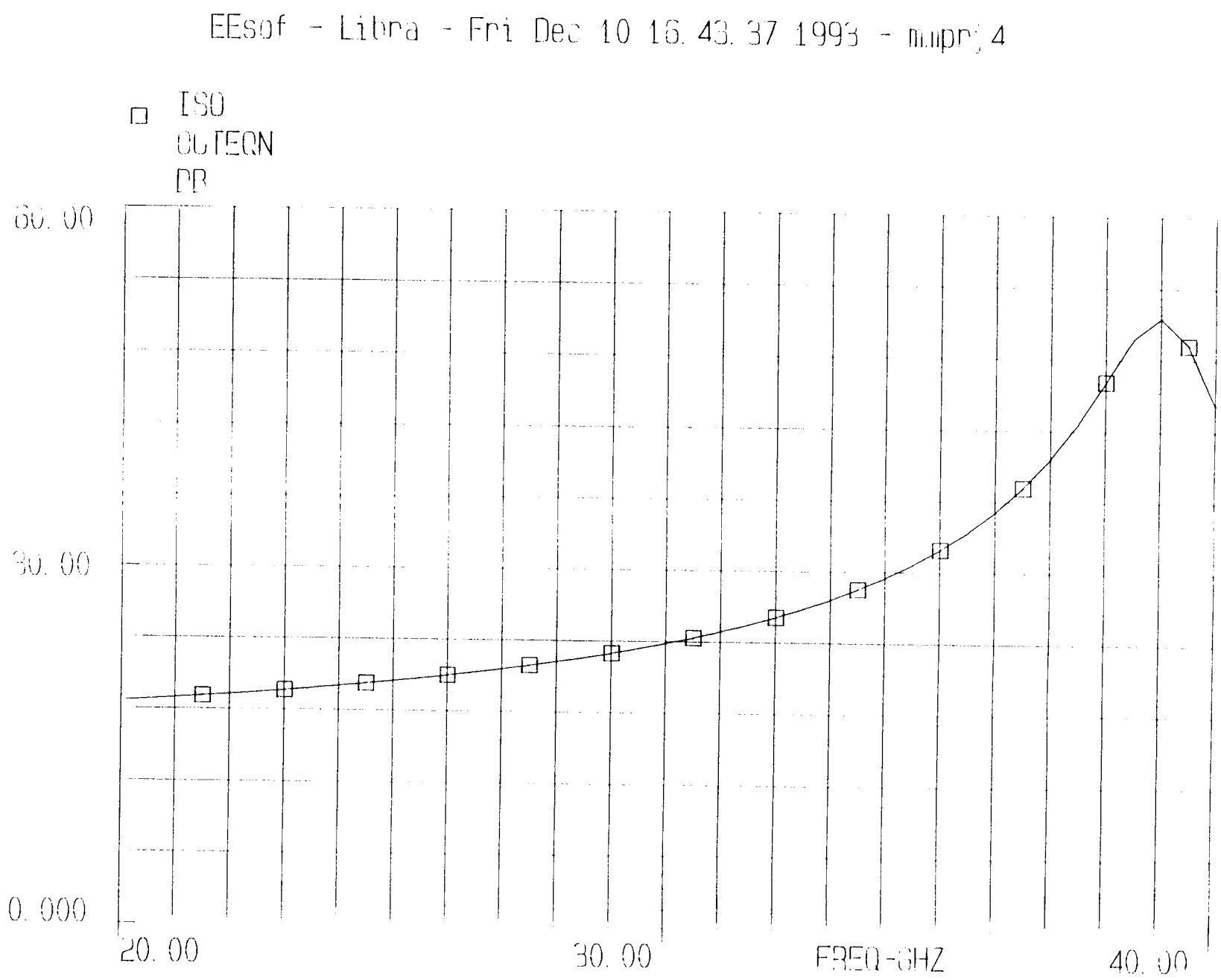
-5.000
-10.00
20.00
30.00
FREQ-GHZ
40.00


EEsof - Libra - Fri Dec 10 16:37:57 1993 - mmpr 4
VSWR1 ON
VSWR2 ON
VSWR1 OFF
VSWR2 OFF
3.000
2.000
1.000
20.00
30.00
FREQ-GHZ
40.00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ISO
OUTEQN
DB
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30.00
0.000
20.00
30.00
FREQ-GHZ
40.00

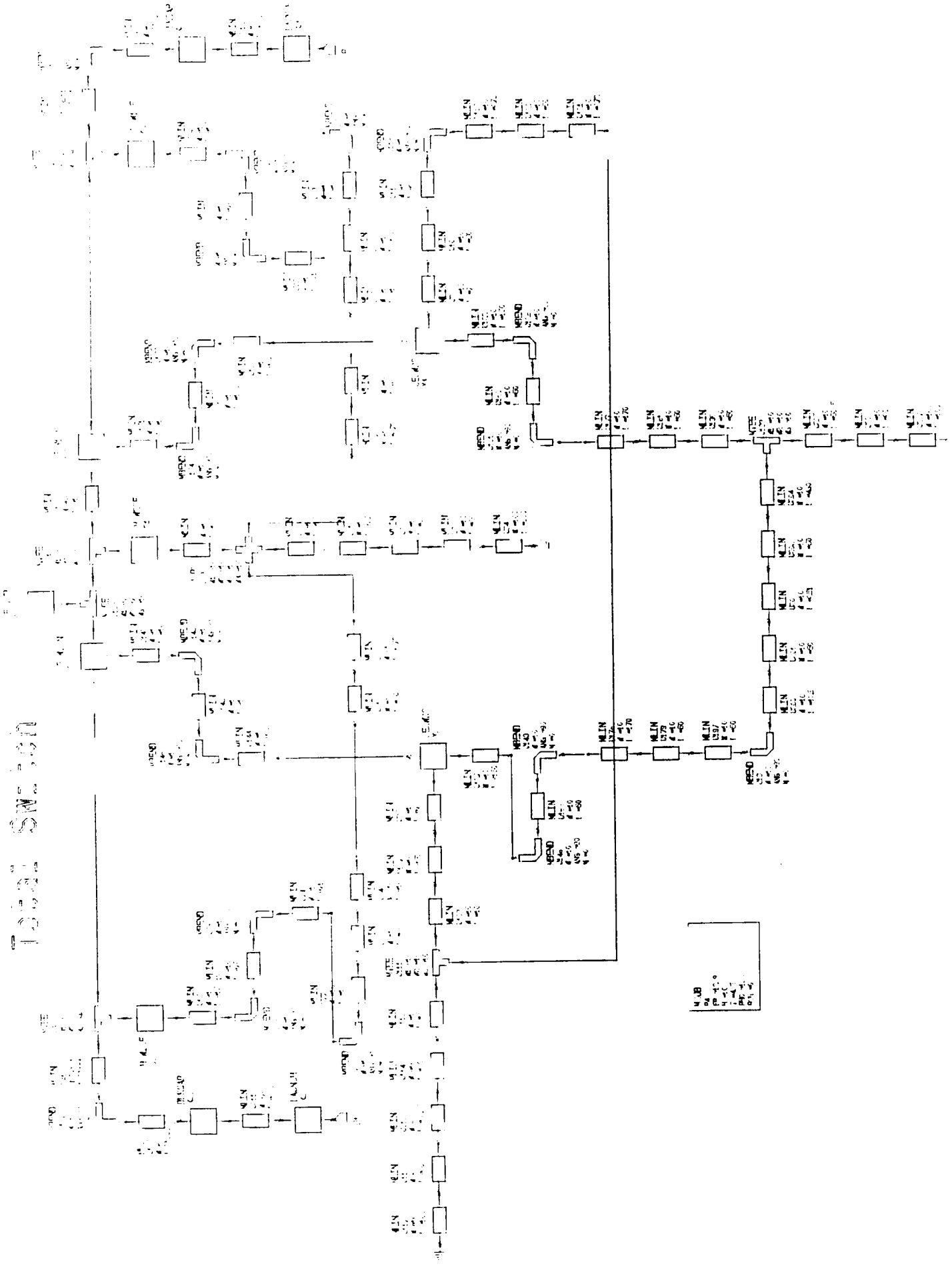
Schematics:

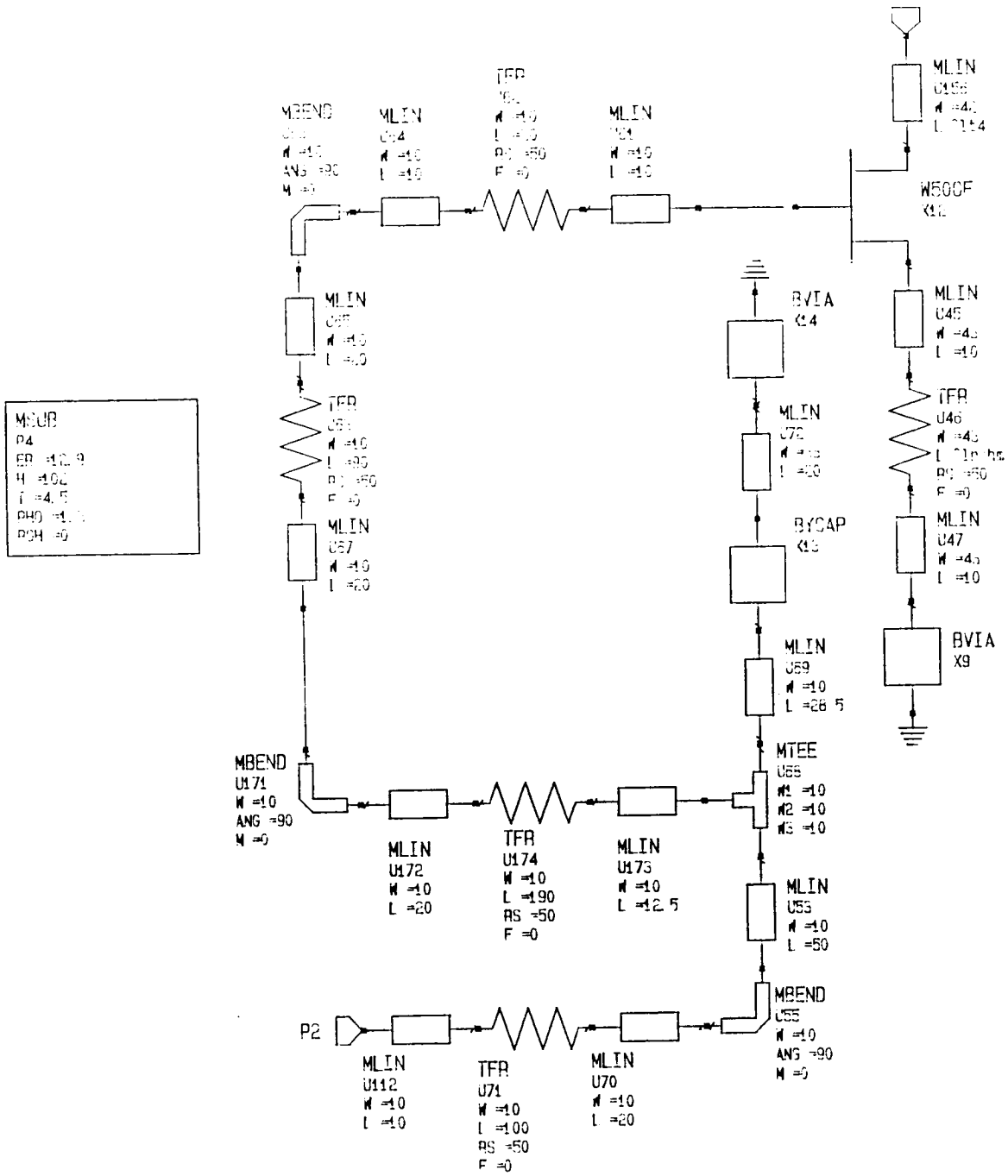
Before I discuss the schematic diagrams following this page, I would like to remind the reader of the two in the introduction section. Figure 2 is the theoretical block diagram describing this circuit. The Total Switch schematic on the next page is the ACADEMY realization of Figure 2. Figure 1 is the schematic used to model the transistors in this circuit. The transistors in the other schematics are actually modeled using Figure 1 and the table below it. To make the schematics easier to understand, there is a short list of terms used in ACADEMY below. It should also be mentioned that the schematics included are the total switch in its on state and the subcircuits in the states required for this. Including the circuits associated with both states of the total switch would not have been informative, so I decided against it. Refer to the table below Figure 2 for information on subcircuit condition relative to total switch state.

Term	Definition
W500F	50 μm FET with Vgs = -3.5 volts
W500N	50 μm FET with Vgs = 0.25 volts
W2000F	200 μm FET with Vgs = -3.5 volts
W200N	200 μm FET with Vgs = 0.5 volts
SHSW1OF	Matched shunt switch in its off state
SHSW1ON	Matched shunt switch in its on state
SHSW2OF	Shorted shunt switch in its off state
SHSW2ON	Shorted shunt switch in its on state
SESW1OF	Series switch in its off state
SESW1ON	Series switch in its on state
SESWDC	Series switch bias subcircuit
BLKCAP	Blocking capacitor
BYCAP	Bypass capacitor
BVIA	Bottom ground via
LAUNCH	Coplaner waveguide to microstrip launch
SESTUB	λ/4 DC ground reference

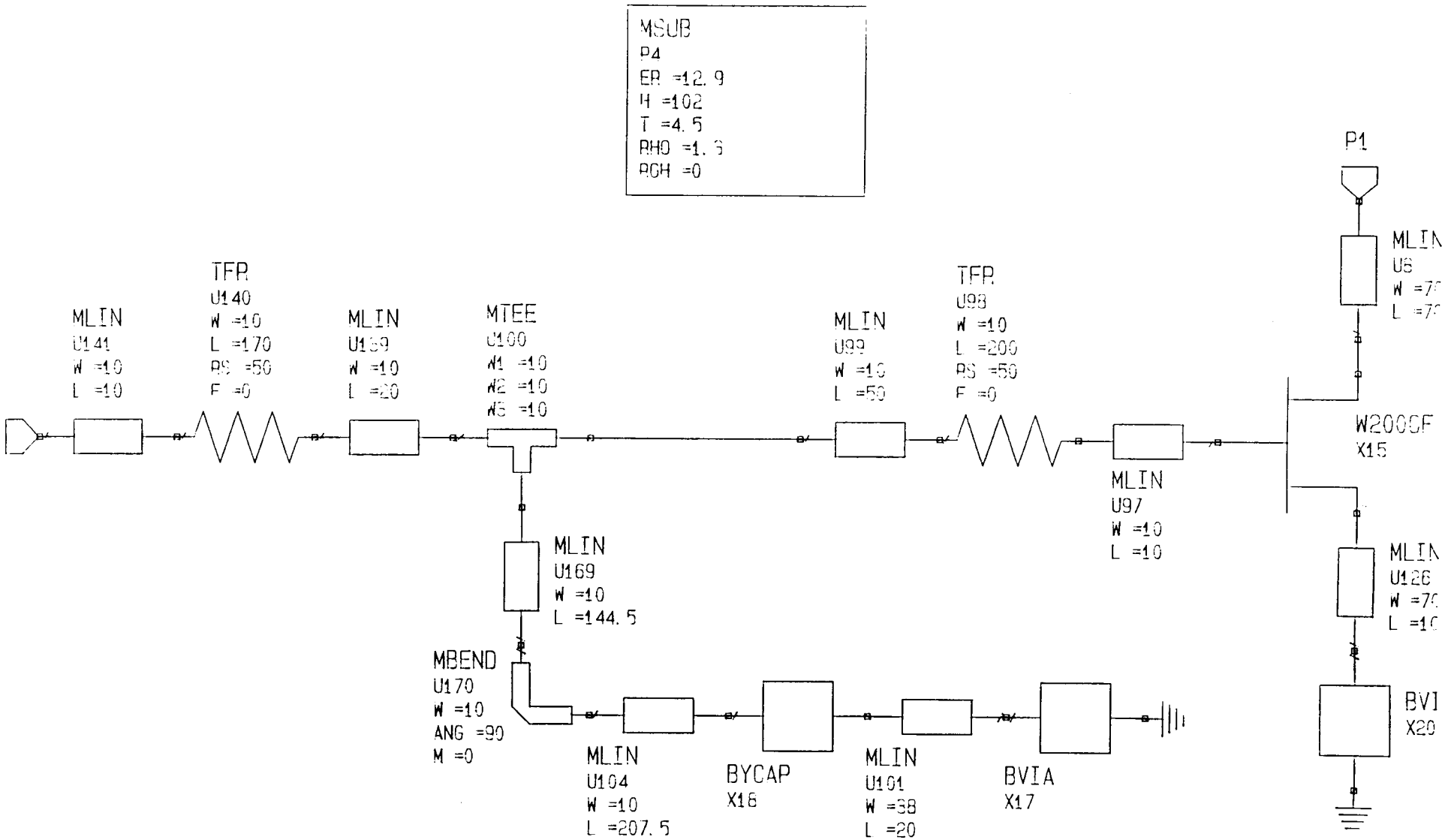
Below is a list of the schematics following this page in the order that they appear.

Title	Description
Total Switch	The final switch circuit in the on state
Matched Shunt Switch	The matched shunt switch in its off state
Shorted Shunt Switch	The shorted shunt switch in its off state
Series Switch	The series switch in its on state
Series Switch Bias	The bias subcircuit required for the series switch

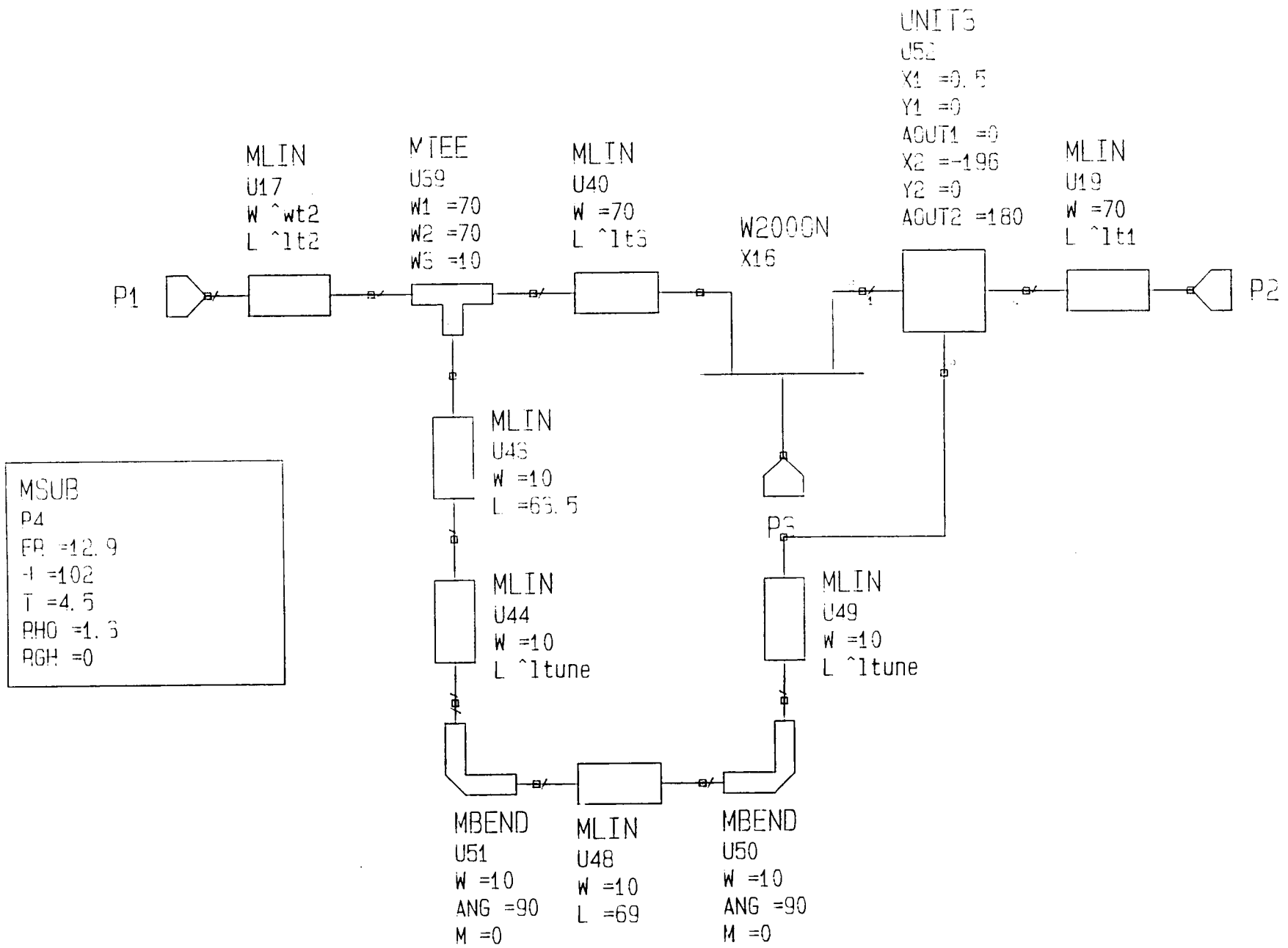




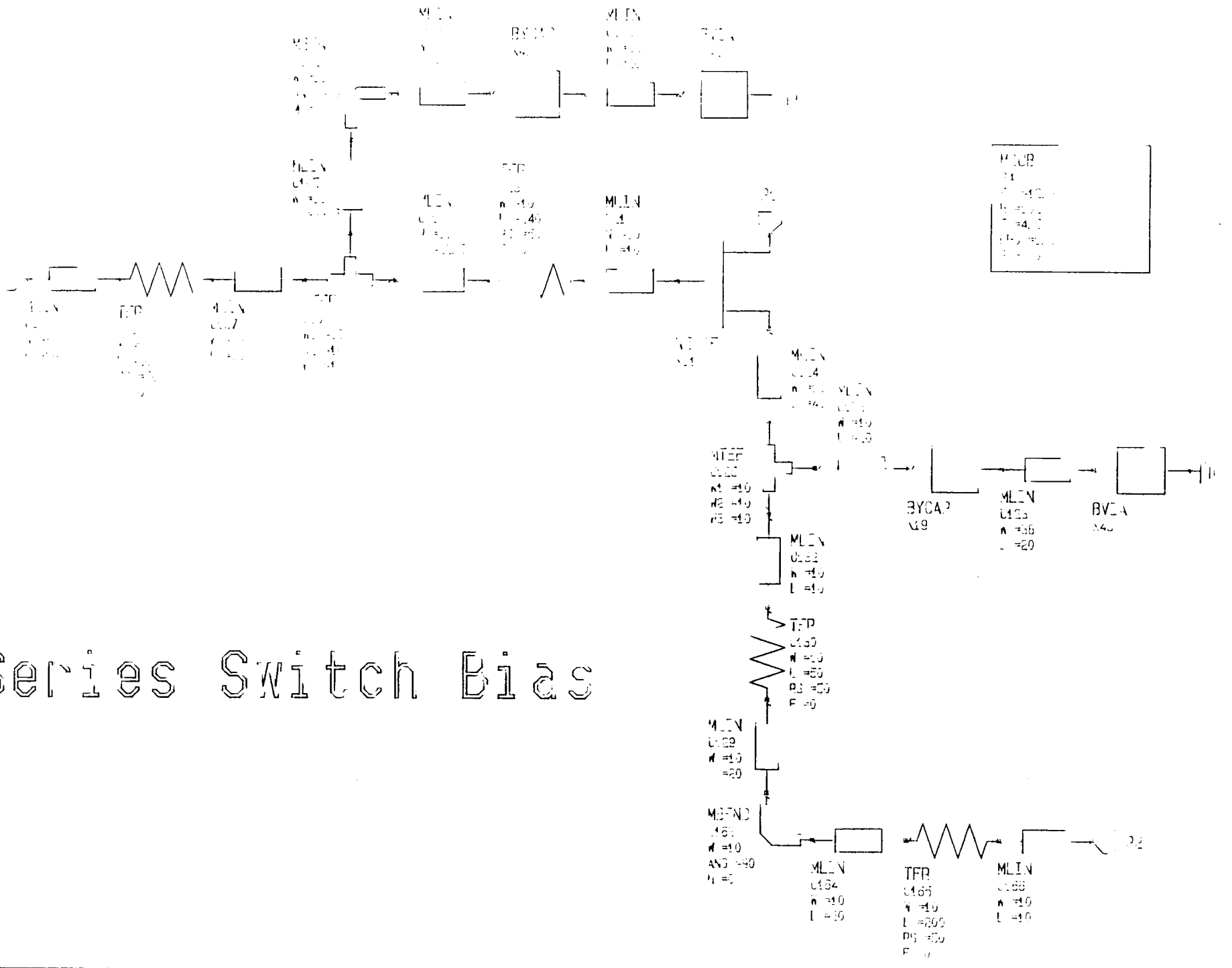
Matched Shunt Switch



Shorted Shunt Switch



Series Switch



Series Switch Bias

DC Analysis:

As was mentioned in the introduction, this circuit should require very low DC current. The DC response was not simulated with EESOF due to the lack of an appropriate nonlinear model of the transistors in this circuit. Considering that the transistor models utilized ideal capacitors to create an appropriate linear response, It was also true that the model used for the Martin Marrietta capacitors was an ideal capacitor. EESOF will think that there will be no DC current flow into the gate of the transistors. Of course, there will be some DC current flow; but, this current flow should be very low since the DC bias is connected to only transistor gates. Taking these facts into account, I thought it would be sufficient to use thin resistors in the bias network. The reader should refer to the test plan section to see how to bias the circuit correctly.

Design Robustness:

Once again, I felt that without a better transistor model any statistical analysis of the circuit would of suspect consequence. For this reason I did not perform large scale statistical analysis of the switch using EESOF. My thinking was that the value of the various components in the transistor models could be different in the final circuit. It was assumed that the components could vary in any direction and possibly independent of one another. From this foundation I began my probing of the circuit. Instead, I manually changed parameters while observing the response of the circuit. Therefore this portion of the report is a discussion of that process and the subsequent trends observed.

For simplicity, I will discuss only the 200 μm transistors used in the series switches in this paragraph. It comes as no great surprise that the insertion loss will increase if Rds increases. It was mildly pleasing to find that the value of Cds and Cg did not have a large effect on insertion loss. These components did have an effect on the isolation and VSWR of the circuit. This was also expected since the parallel inductance resonates these capacitors. As it turns out the effect was not that large and the circuit should perform well if the values are different.

For simplicity, I will discuss only the 200 μm transistors used in the shorted shunt switch in this paragraph. This subcircuit was designed to improve the total switch isolation. Due to its location in the circuit it has an effect on VSWR and insertion loss as well. My analysis led me to the conclusions I expected in this case. If the off state Cds was increased the VSWR and insertion loss improved slightly. This is because the shorted shunt switch appears more like an open circuit as the capacitance decreases. If the on state Rds was increased the isolation decreased. This is because the shorted shunt switch appears less like a short circuit as the resistance increases.

For simplicity, I will discuss only the 50 μm transistors used in the matched shunt switch in this paragraph. This subcircuit was designed to create a matched circuit in the off state of the total switch. The circuit does not have much effect on the other parameters of the total switch. The most important component of this transistor is therefore its on state Rds. If the value of Rds varies, it raises the entire VSWR curve for the total switch off state. The on state of the total switch is relatively unaffected by small changes in this transistor.

For simplicity, I will discuss only the 50 μm transistors used in the series switch bias in this paragraph. This subcircuit was designed to create a large impedance at the gate of the series switch transistors. The need for this circuit arose from the fact that the bias network on the series switches was having a negative effect on the insertion loss of the total switch. Through trial and error it was found that any impedance above 10 kΩ on the gate of the transistors eliminated the negative effect on insertion loss. The most important component of this transistor is therefore its off state Rds. As expected, the circuit response is immune to variations in this component as long as Rds is above 10 kΩ.

In general the circuit is designed to be fairly immune to any variation in the components of the bias network. In other words, the actual values of the resistors and capacitors in this circuit are not critical. To ensure that this is true I varied the impedance seen by the switches looking into their respective bias networks. Essentially the various subcircuits and subsequently the total circuit could tolerate large variations in these impedances. This is of course excluding the transistor in the series switch bias that was

discussed previously. Variations in the value of the DC blocking capacitors had very little effect on the circuit performance. I think that the circuit will perform well if there are variations in the capacitors and resistors.

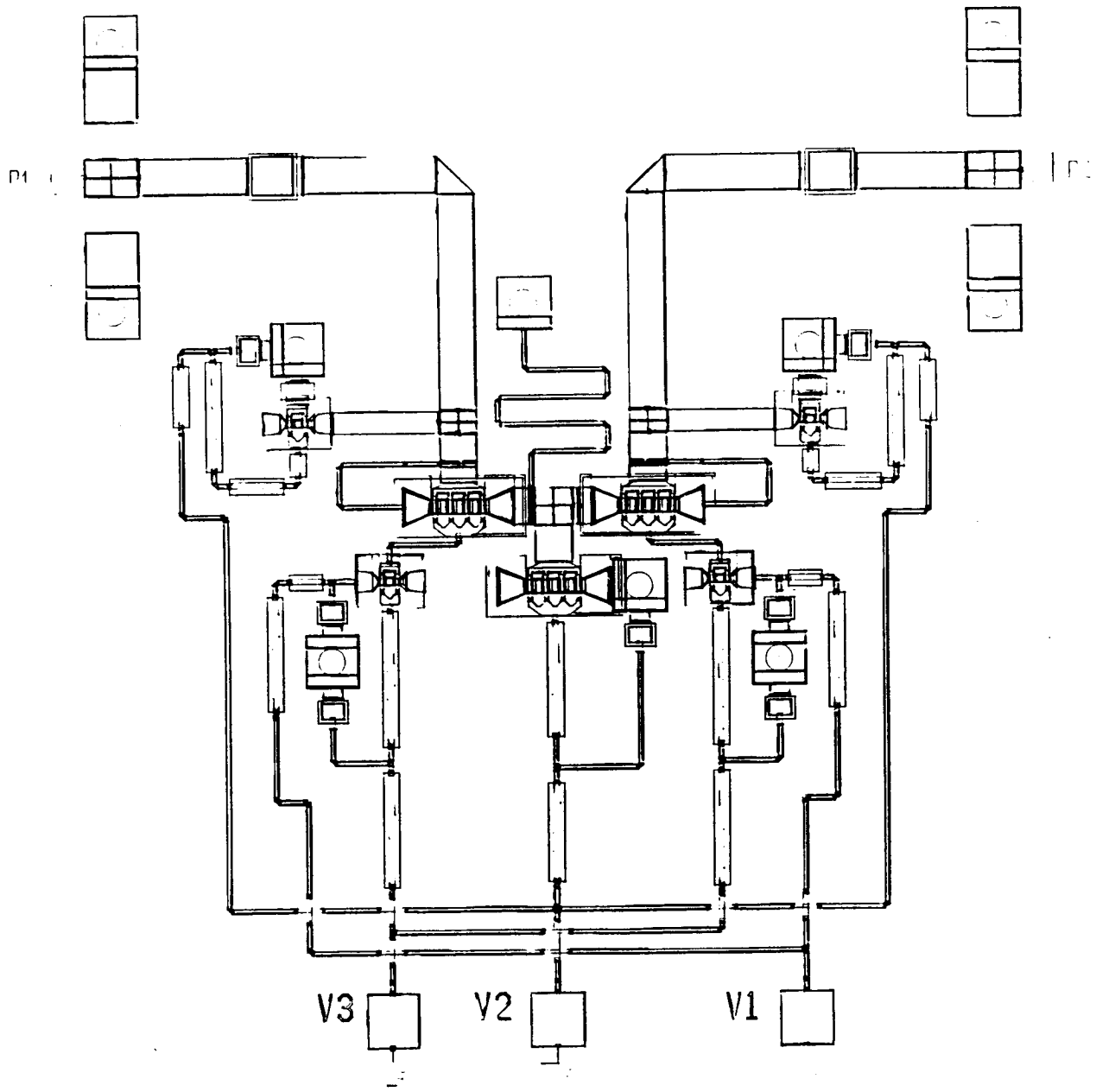
The pitfall of this circuit is its dependence on the component values in the various transistor models. If the models derived for this project are correct in the fabricated circuit the total circuit should perform well. If the models are off by a considerable amount the circuit will suffer the consequences listed above.

Test Plan:

All of the parameters that have been discussed in this report can be measured using a VNA and a probe station. It would be interesting to make a couple of other measurements. The total amount of DC current required to run the circuit would be an useful specification to know. If the circuit operates like expected, the low magnitude of the current may make this a difficult measurement. It would also useful to know at what microwave power level the switch compresses. This could be measured using a synthesizer and a spectrum analyzer. The input power to the switch could be increased until the insertion loss through the switch increases by one dB. The input power at this point would be considered the input one dB compression point. As mentioned in the introduction, the compression may be a high number and therefore may require a power amp following the synthesizer to make the measurement possible. There may be other measurements of importance for a specific application. It is my opinion that these two and the three specified for the circuit are the most common ones of concern.

The three parameters specified for this circuit were insertion loss, on/off isolation, and input and output VSWR when the switch is in both its on and off states. All these measurements can be performed by measuring the two port S parameters of the circuit using a VNA. It will be necessary to measure the S parameters in the off state and the on state. The following page is a picture of the physical layout of this circuit. The circuit is symmetric and can be operated in either direction. Therefore either of the coplaner waveguide launches can be used for the input while the other is the output. Below is a table describing the bias operating conditions.

Switch State	V1 (Volts)	V2 (Volts)	V3 (Volts)
On	0.5	-3.5	-4.0
Off	-3.5	0.25	-4.0


V3
V2
V1

Microwave Monolithic Integrated Circuit (MMIC) Design
525.787
The Johns Hopkins University
December 13, 1993
A Wide Band Directional Coupler
Dean M. LaBarbera

Abstract

A symmetrical quasi-TEM mode coupled transmission line 10 dB directional coupler was designed and a layout created for implementation using MMIC technology on gallium arsenide. Wide bandwidth was achieved with the use of a multi section equal ripple design. The coupler was produced on a substrate measuring 80 by 120 mils which is far larger than actually required to accommodate this design. The high dielectric constant of gallium arsenide facilitates distributed element designs above approximately 20 GHz, the frequency at which wavelengths are short enough to be accommodated by commercially available chip sizes. With this limitation in mind, the coupler was designed to operate over the frequency range of 20 to 150 GHz. With the following analysis, it will be shown that the performance of the quasi-TEM microstrip coupler is not comparable to the TEM coupler. Microstrip couplers are not capable of providing adequate isolation over a wide bandwidth.

Introduction

Directional couplers are often used for microwave and millimeter wave network analysis. The directional behavior makes possible return loss measurements and measurements with respect to a reference level. For a directional coupler to be useful, the power level at the isolated port must be at least 10 dB below the power level at the coupled port, i.e. -20 dB for a 10 dB coupler. A MMIC directional coupler would be small enough to be installed in the probe head of a probe station. Down conversion of the microwave or millimeter wave test signals could then be performed at the probe head, eliminating the cable losses now incurred in measurement systems of this type. This would greatly improve measurement accuracy of MMIC devices. This design analysis explores the possibility of implementing a wide band directional coupler using MMIC techniques for the application stated above.

Design Procedure

Design procedures for symmetrical TEM mode transmission line directional couplers are well documented in the literature. Much work was done during the 1960's on these devices. Tables of designs for symmetrical couplers of various numbers of sections and

coupling coefficients were presented by E. G. Cristal and L. Young*. The tables tabulate the even mode impedances for various bandwidth couplers normalized to a Z_0 of 1 Ohm. To design a TEM coupler the even mode impedance for each coupler section is read from the tables corresponding to the bandwidth and coupling desired.

Once the even mode impedances for each section have been obtained from the tables the odd mode impedances can then be determined. The product of the even and odd impedance for a given section is equal to 1; therefore, the odd mode impedance is the reciprocal of the even mode impedance. The even and odd impedances are then scaled by multiplying each normalized impedance by 50.

The TEM coupler was then converted to quasi-TEM (microstrip) with the assistance of Line-Calc. by EEsof. Line-Calc has a coupled line mode which yields line widths and spacing when given the even and odd mode impedances for each coupled line section. The physical coupled sections can then be analyzed with computer aided techniques.

Design Philosophy

The even and odd mode impedances obtained using the previously described procedure were first verified with Libra. Ideal coupled lines were created using the CLIN elements. The cascade of these elements was then simulated. This ideal coupler indicated that the impedances were correct. The performance matched the expected theoretical result exactly.

The physical quasi-TEM design was then simulated with Libra using the MCLIN elements. This design did not include any connecting lines as Libra cannot model the coupling effects of these lines. The resulting performance was degraded relative to the TEM coupler. This was expected due to the difference in the even and odd mode phase velocity for quasi-TEM propagation. The greatest discrepancy was in isolation. Isolation in a parallel line directional coupler is achieved when the even and odd mode signals arrive at the isolated port 180 degrees out of phase, canceling each other. For quasi-TEM,

* E. G. Cristal and L. Young, "Theory and tables of optimum symmetrical TEM-mode coupled transmission line directional couplers," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-13, no. 5, pp. 544-558, September 1965.

isolation degrades with increasing frequency due to the increasing phase error of the even and odd mode signals.

The physical design was then analyzed with Sonnet, an electromagnetic simulator. This simulation included all connecting lines and bends. The connecting lines and bends further degraded performance from the ideal case.

From the above mentioned tables it was determined that a five section coupler would be needed to achieve the desired performance over the specified bandwidth of 20 to 150 GHz. After analysis of the five section coupler it was apparent that the dispersive effects of microstrip were limiting the high frequency performance of the coupler. The insertion loss rapidly increased with increasing frequency and the isolation rapidly decreased. In general, the results were departing from the ideal case by a large margin.

A three section coupler was then designed with the hopes that the decreased length of this coupler would have less degradation due to microstrip dispersion. The results of the analysis proved this to be true. The coupler was still hindered by the effects of dispersion but to a lessor degree. The results more closely agreed with the ideal coupler.

Modeled Performance

Specification Compliance

	Frequency Range	Coupling	Coupling Ripple	Directivity	Insertion Loss	VSWR
Specification	20-150 GHz	10 dB	$\pm$ 2 dB	20 dB	1 dB	1.5 : 1
Prediction	20-115 GHz	12 dB	$\pm$ 1.5 dB	1 dB	1.6 dB	3 : 1

Predicted performance

The performance of the ideal three section TEM coupler is shown in Figure 1. These results indicate near perfect performance, thus validating the even and odd impedances used for this design. Unfortunately, this performance cannot be achieved in quasi-TEM mode. The performance of the physical microstrip sections without connecting lines as

predicted by Libra is shown in Figure 2. The effects of dispersion are clearly evident in the results for isolation (S31) and insertion loss (S41). VSWR (S11) was still respectable, -16 dB at 150 GHz. The coupling response (S31) maintained a shape similar to the ideal coupler response. The complete coupler was then analyzed with the Sonnet electromagnetic simulator. This simulation included all connecting lines and bends. The results of this simulation are shown in Figure 3. The results are reasonably close to the performance predicted by Libra. The predicted coupling for the coupler is closer to 12 dB. This increased loss is probably due to the loss inherent in the gallium arsenide MMIC process. The predicted isolation performance indicates that the desired directivity is never achieved anywhere in the operating band. It appears that the specified level of directivity cannot be achieved for a 10 dB coupler over such a wide bandwidth in microstrip. The insertion loss exceeds specification at 115 GHz but is still respectable, 1.6 dB at 150 GHz. VSWR exceeds specification at 125 GHz, degrading to -7 dB at 150 GHz. From these results it is difficult to determine the actual operating bandwidth due to the poor isolation performance. With respect to the remaining specifications, this coupler appears to operate form 20 to 115 GHz.

Schematic Diagram

The schematic diagram for the coupler is shown in Figure 4. (Only one half of the coupler is shown as the other half is identical.) The schematic represents the elements which were used to construct the coupler in Academy layout. This schematic was not used for simulations. The final layout is shown in Figure 5. Two versions of the coupler were created to facilitate testing. A single section coupler for the same frequency range was created to utilize the remaining chip area.

Test Plan

Due to the limitations of the probe station used for final testing, two versions of the coupler were required for complete testing. The probe station requires that input and output probes must be postitioned on opposite sides of the chip. Three of the four ports on each coupler are internally terminated in 50 Ohms. These terminations are connected with air bridge metal and can be easily disconnected. With all terminations in place, S11 can be measured. With the termination on port 2 removed, S21 can be tested. With the

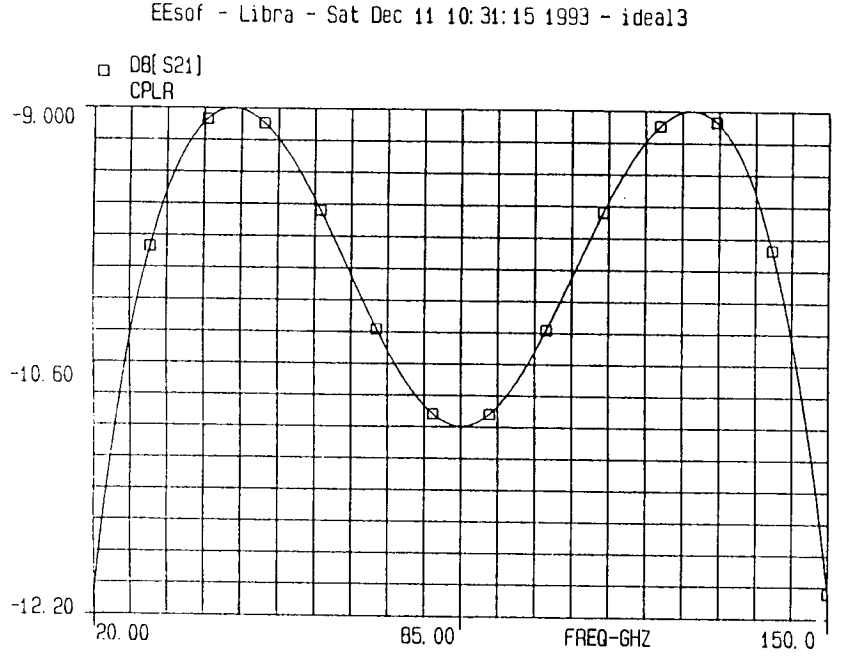
other version of the coupler S31 and S41 can be measured. This measurement sequence is illustrated in Figure 6.

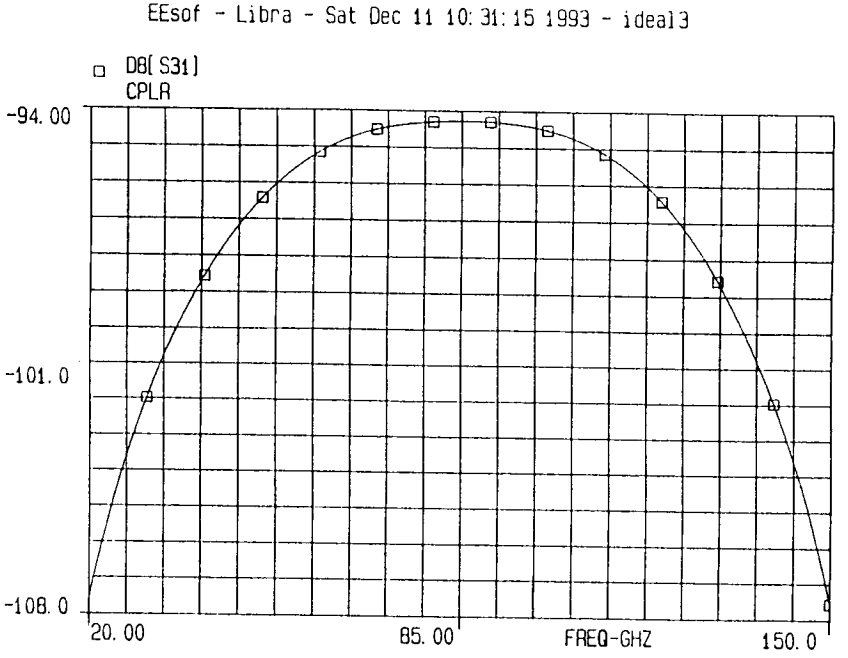
Conclusion

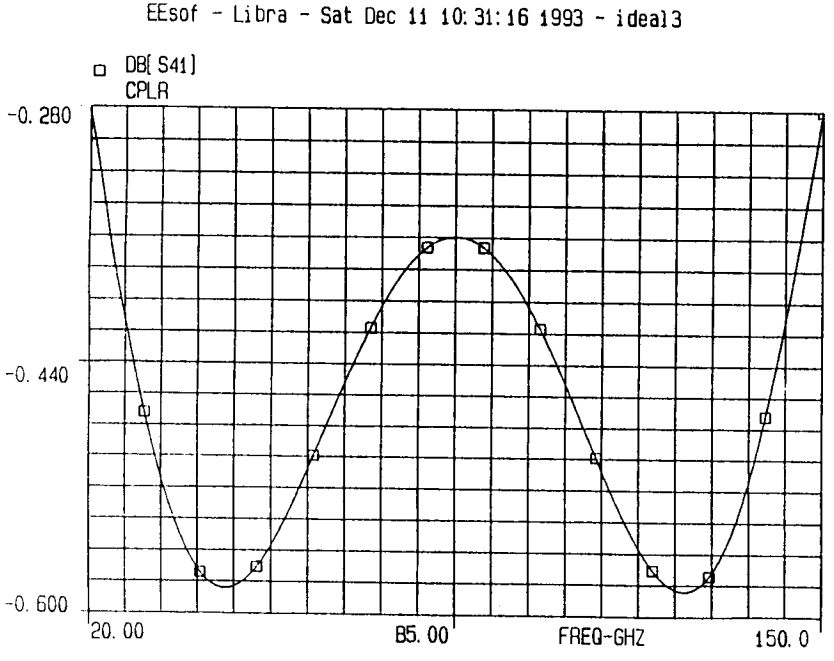
Quasi-TEM couplers are not capable of the level of performance attainable with TEM structures such as stripline. The most notable performance shortfall is in isolation and directivity. This is the primary performance parameter for directional couplers. To sacrifice directivity to achieve small size will render the coupler virtually useless.

Recommendation

The performance of this coupler can be improved slightly by optimizing the connecting lines and bends. The performance will not improve over the level predicted by the Libra simulations without connecting lines. Therefore, investigation of a MMIC stripline approach is suggested. The stripline coupler should yield performance very close to ideal coupler predictions. The only observed differences attributable to the MMIC process would be loss, which would be minimal in a loosely coupled coupler, i.e. greater than 10 dB.







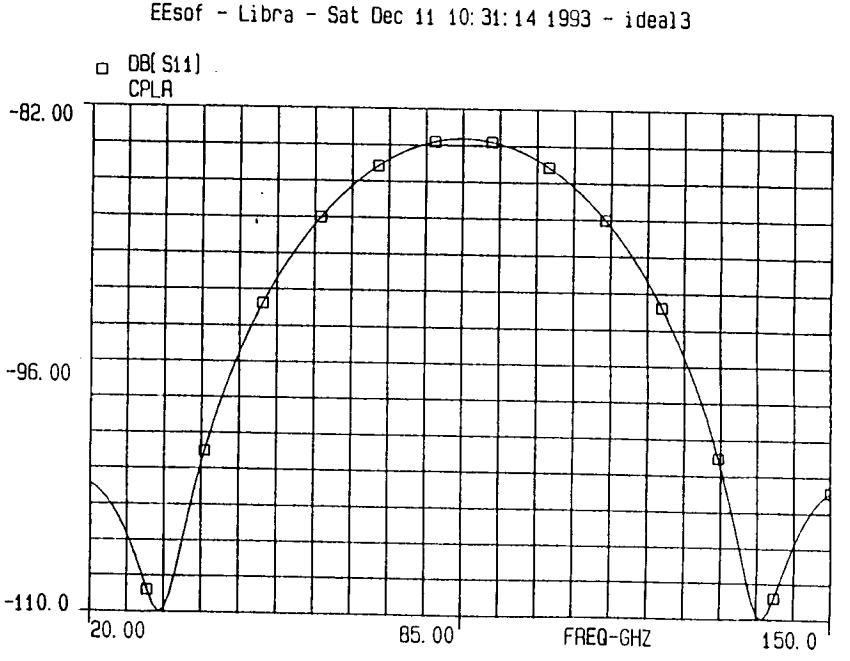
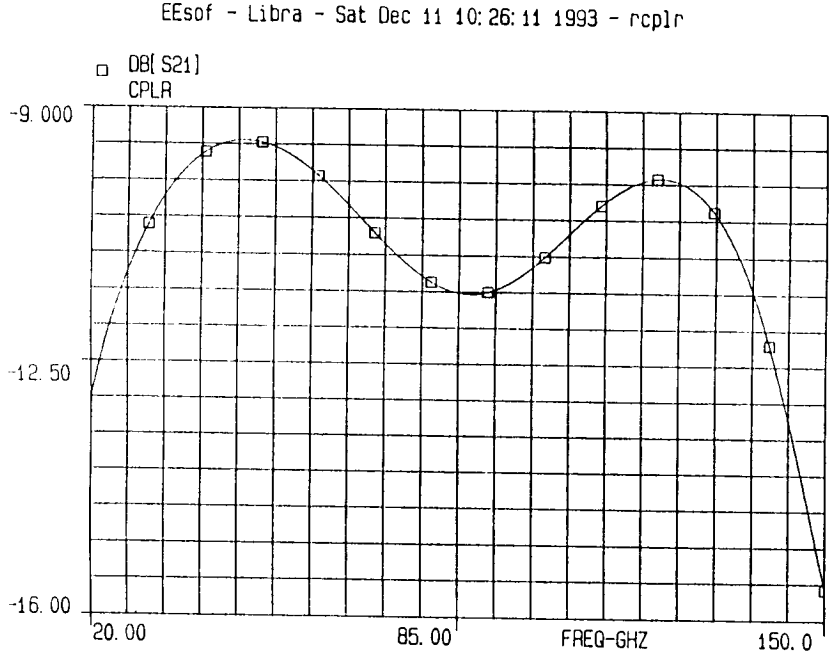
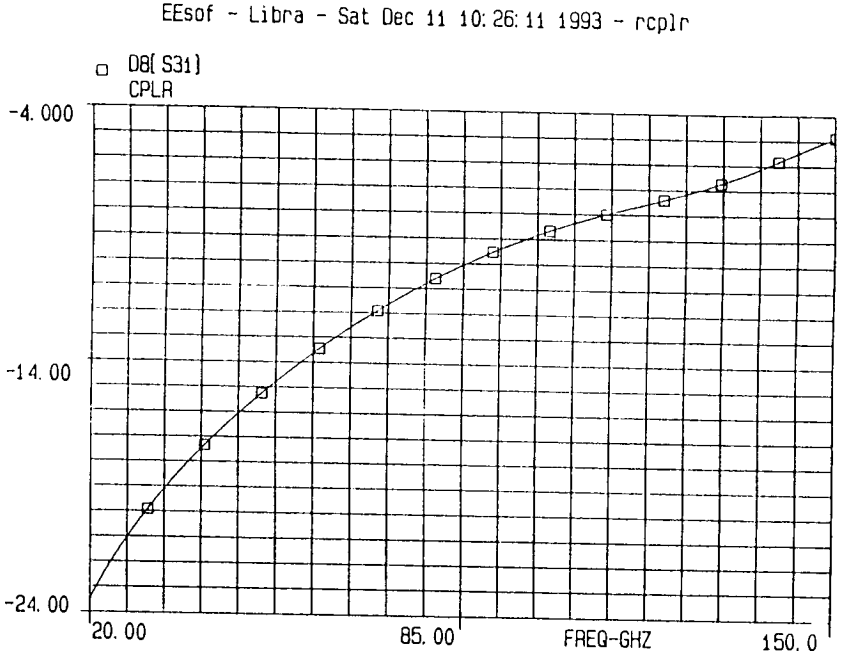
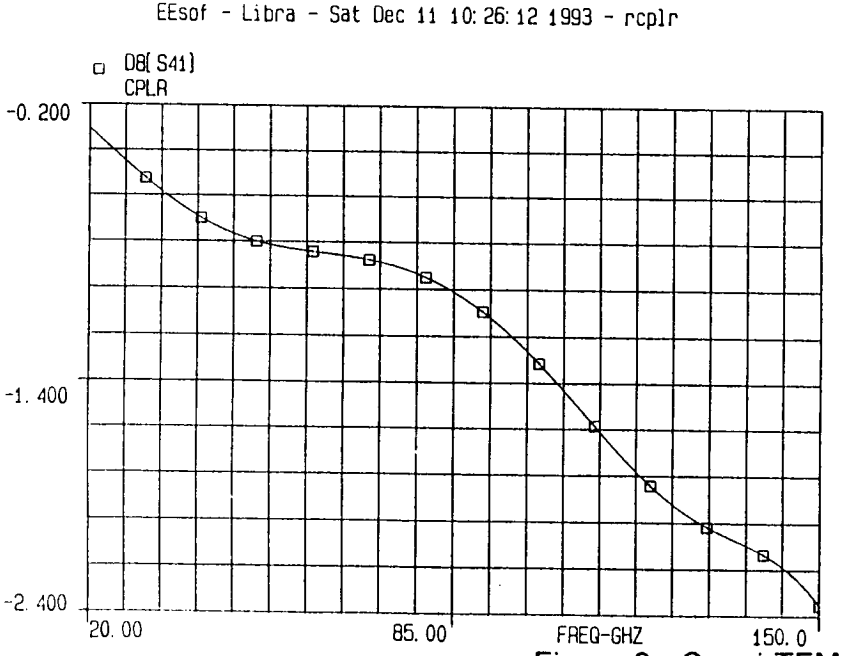


Figure 1. Ideal TEM coupler performance.







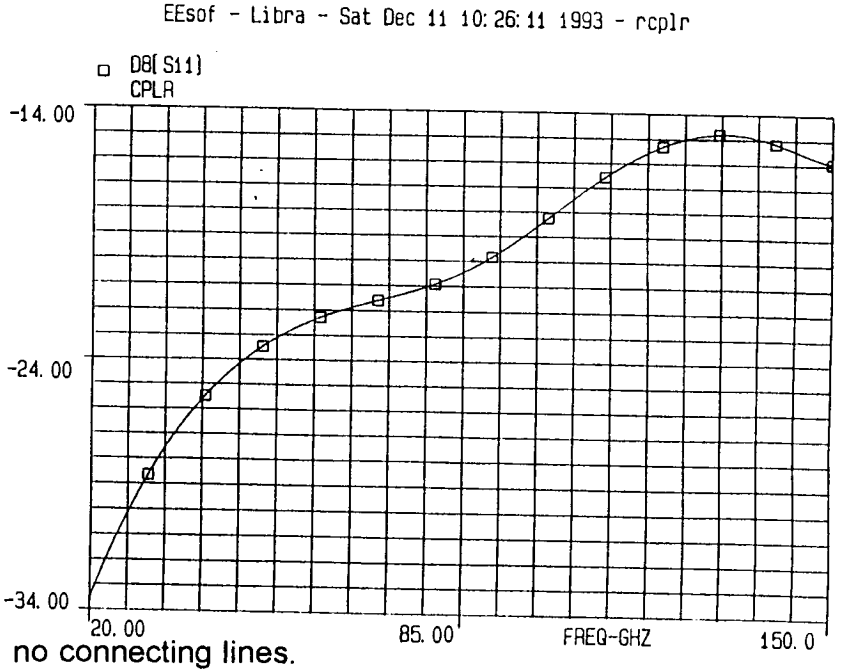
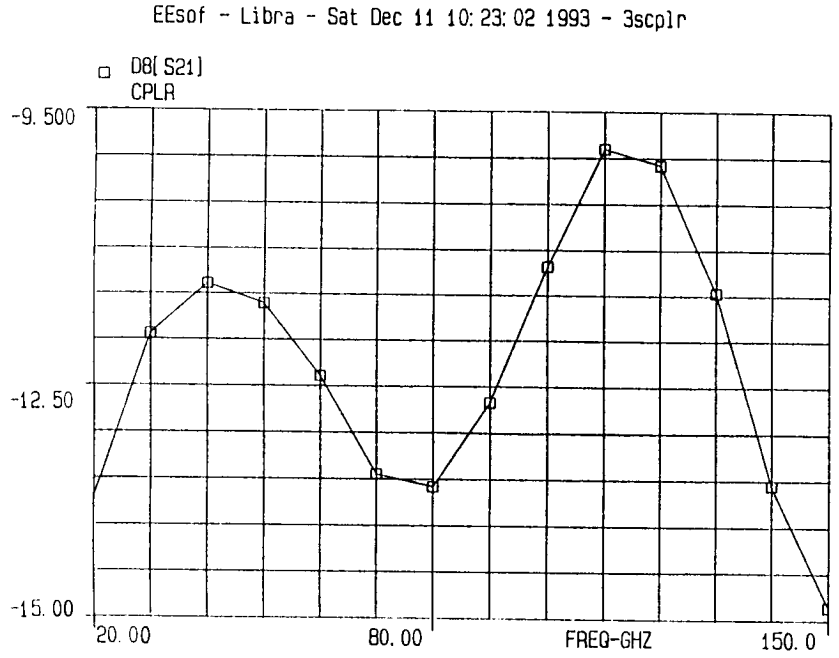
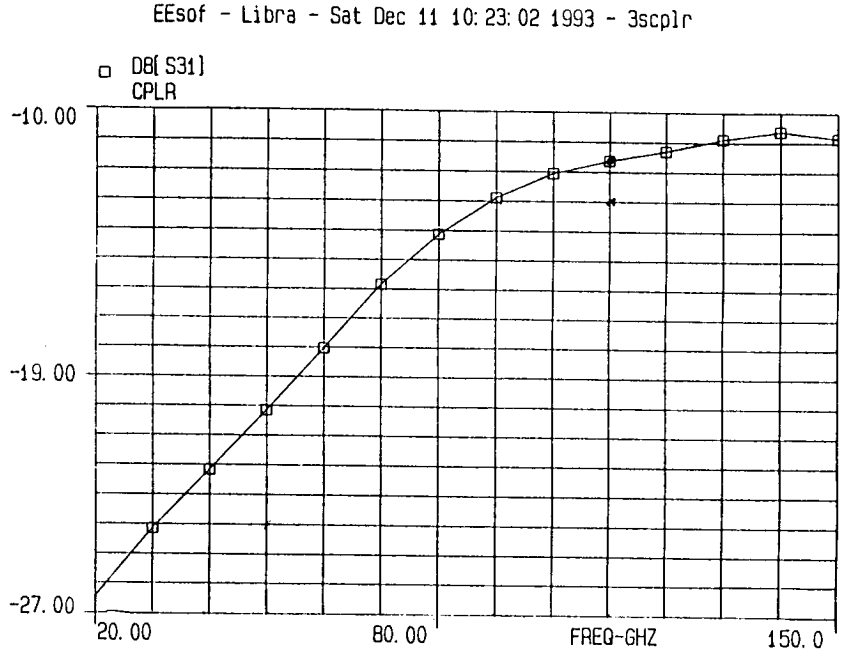
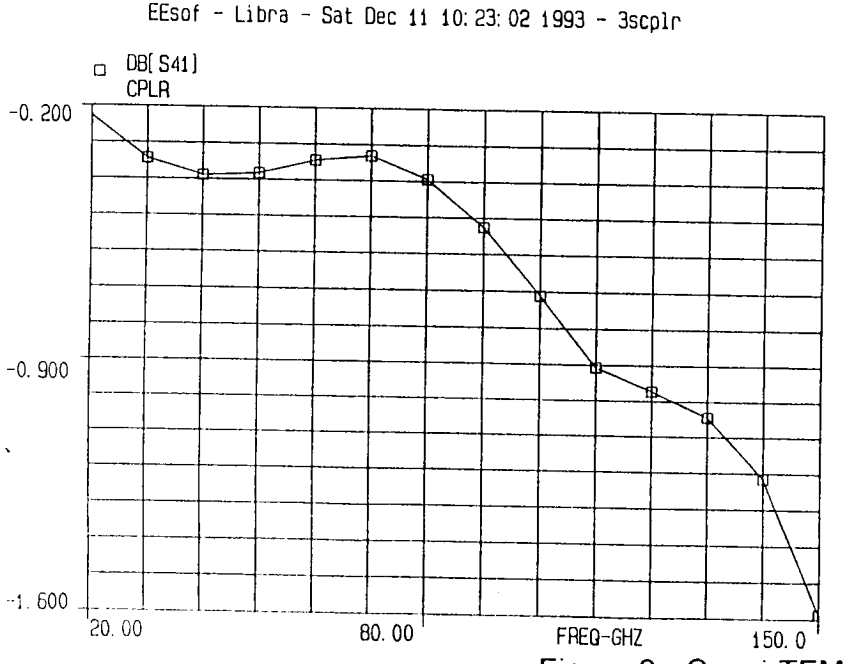


Figure 2. Quasi-TEM performance, no connecting lines.







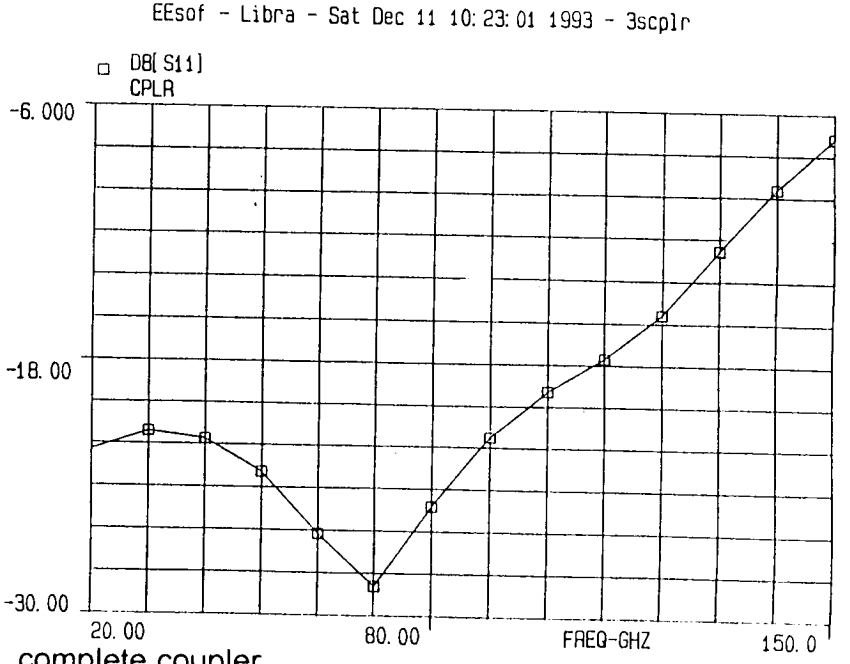


Figure 3. Quasi-TEM performance, complete coupler.

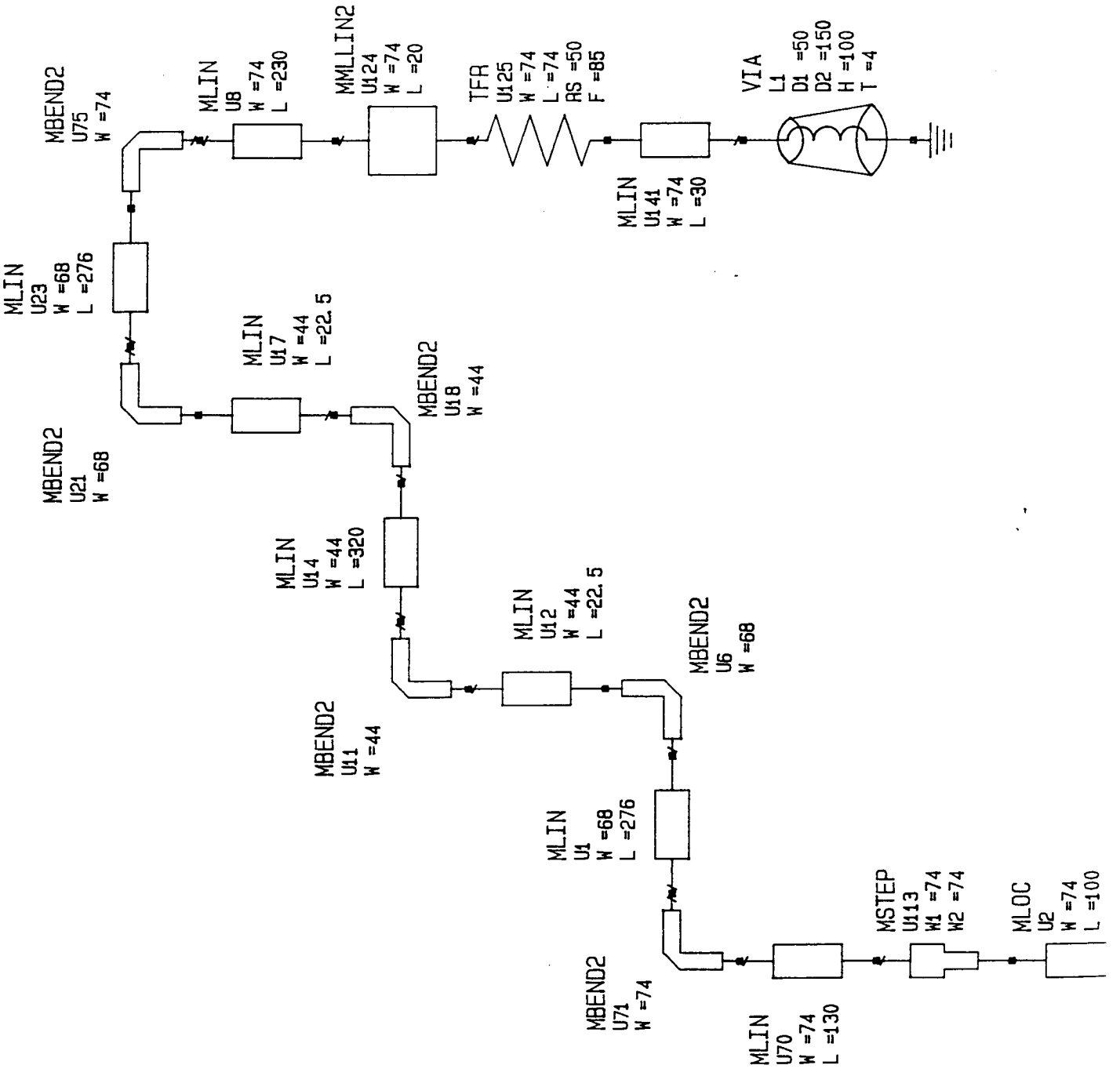


Figure 4. Schematic Diagram.

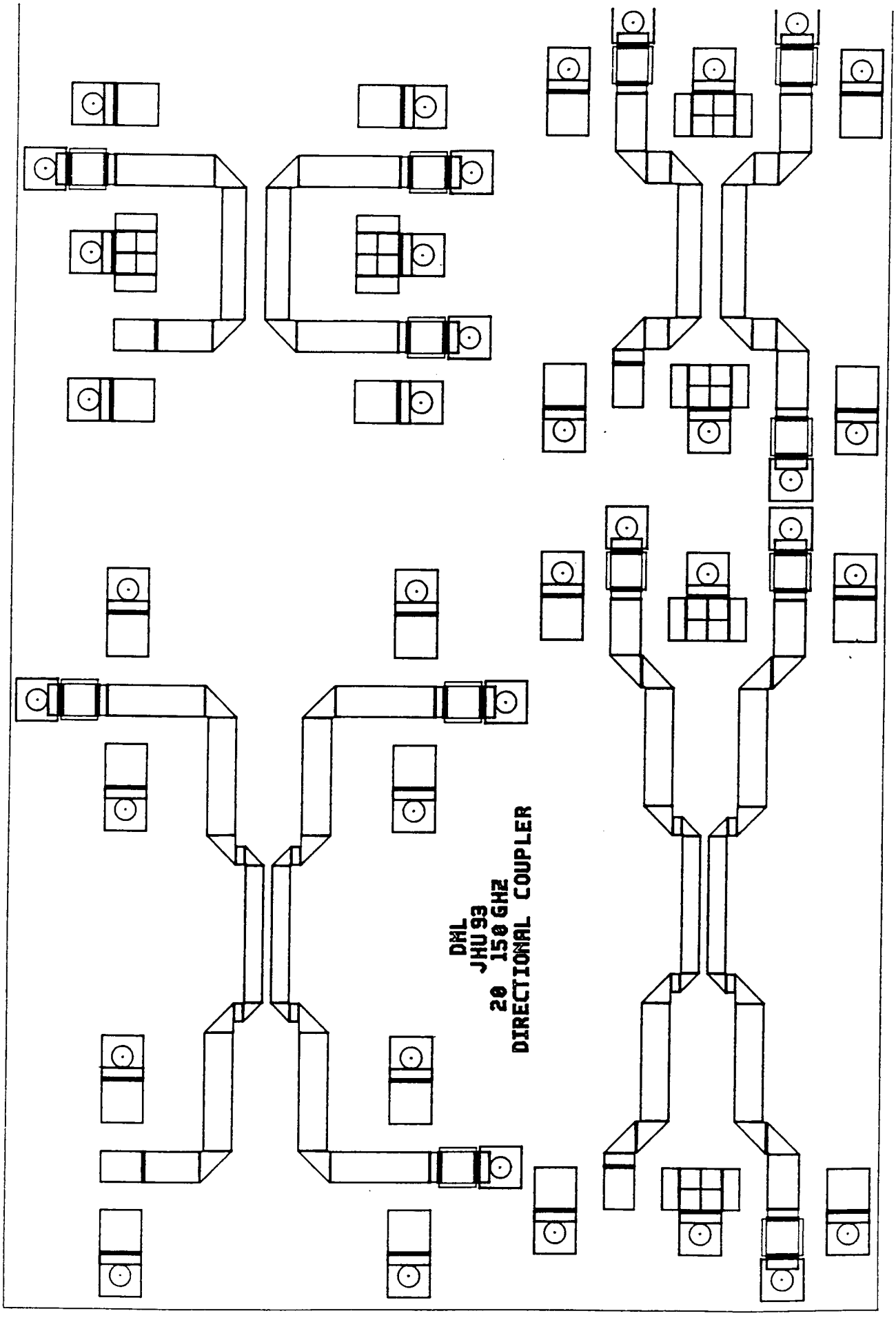


Figure 5. Final Layout.

Test Plan

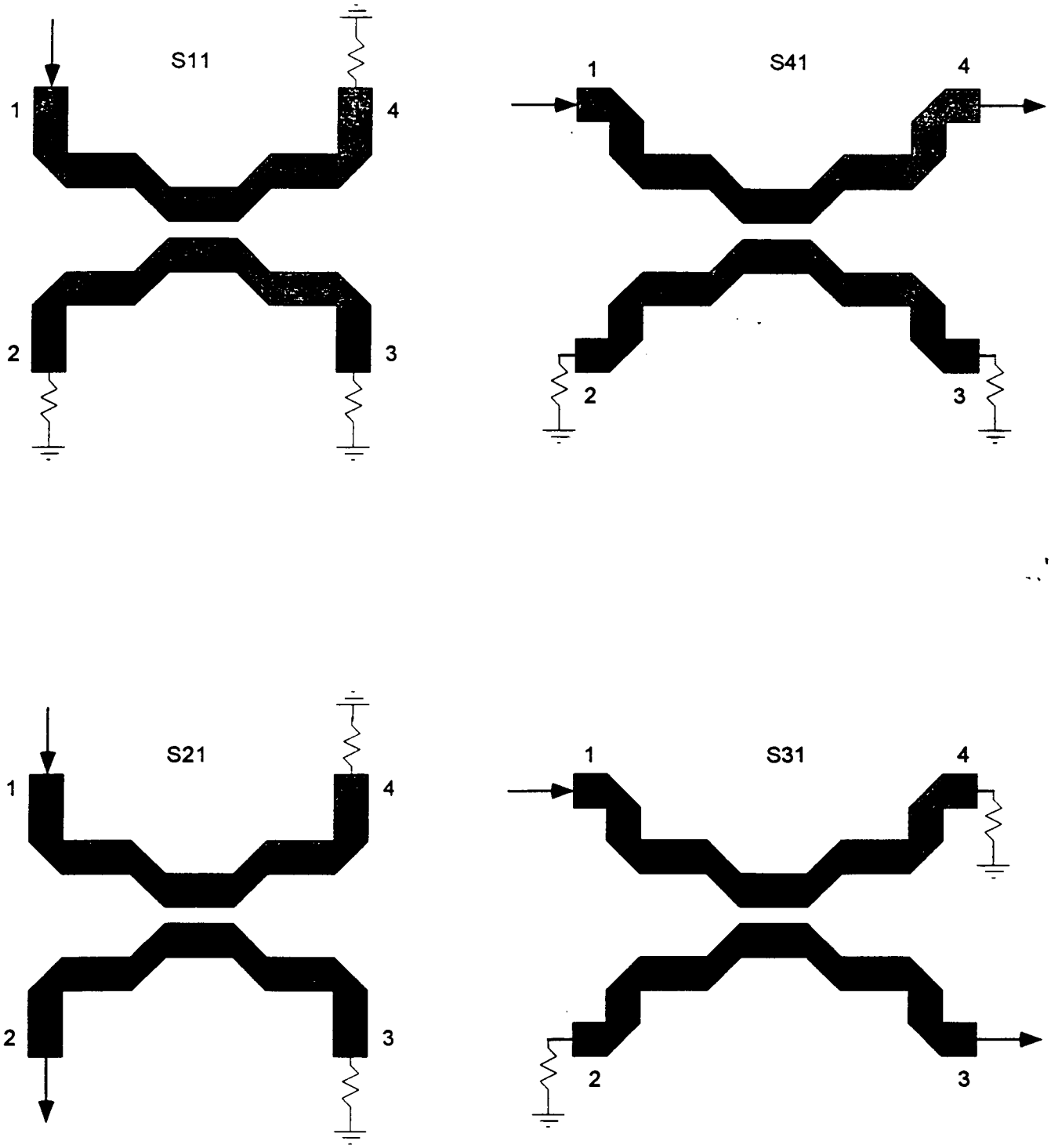


Figure 6.

MMIC Design 525.787

Push-Push Class B
24 GHz to 48 GHz Frequency Doubler

by

Keith D. Ditzler

December 13, 1993

Contents:

Section I: Abstract

Section II: Introduction

Section III: Modeled Performance

Section IV: Schematic Diagrams

Section V: DC Analysis

Section VI: Design Robustness

Section VII: Test Plan

Section VIII: Conclusion

Section I: Summary

The contents of this report will discuss a 24 GHz to 48 GHz Push-Push Class B frequency doubler. This project was part of a MMIC design course offered at Johns Hopkins University in conjuction with the Martin Marietta Laboratories. This circuit will be simulated and artwork generated with the CAD software Academy/Libra provided by EESOF. Topics to be discussed include: design strategies and concepts, circuit specifications, DC and AC circuit analysis, yield analysis. From these results a final conclusion will be drawn. Also included will be schematics, performance plots, and a test plan.

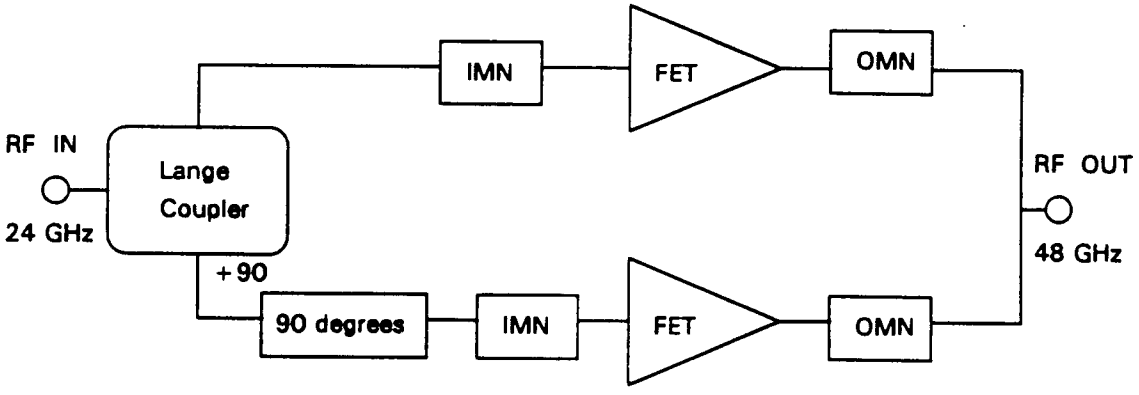
Section II: Introduction

A. Design Philosophy

The frequency doubler has a very simplistic design philosophy. The basic idea is to drive a balanced FET arrangement with a fundamental frequency 180 degrees out phase. Thus canceling the fundamental and its odd order harmonics while generating the desired second harmonic and other even order harmonics. The FET input will be matched at the fundamental while the output will be matched to the second harmonic allowing only the desires frequencies to propagate efficiently. Utilizing two 200 micron FETs the circuit will operate near pinchoff (Vgs = -0.5 V) in order to produce the desired harmonic with Vds = +3.5V.

B. Circuit Description

This circuit will utilize a 3 dB Lange coupler which will provide a balanced output with a 90 degree phase difference. Then with the use of micro strip line an addition 90 degrees will be added. Producing the 180 degree phase difference required for frequency doubling. This concept was practical since a quarter wavelength at 24 GHz is approximately 1100 microns. The input and output were matched using a series capacitor and shunt inductor. This concept made physical implementation of DC bias efficient and provides DC blocking at the RF ports.



Block Diagram Push-Push Class B Frequency Doubler

C. Trade-offs

In this design trade-offs were made choosing a Lange coupler versus using a high pass low pass filter approach. Primarily this was done for increased real estate and improved impedance matching. Also, the drain bias voltage (Vds) was lowered from +5V to +3.5 to insure proper performance. Simulations show that a passive drain bias would degrade the second harmonic output level.

Section III: Modeled Performance

This section will present circuit specifications and performance graphs based on the nonlinear characteristics of this design.

Table 3.1 Specification Compliance Matrix
Figure 3.1 Frequency Spectrum Pre-Layout
Figure 3.2 Frequency Spectrum Chip Layout
Figure 3.3 Harmonic Power Output versus Frequency Chip Layout
Figure 3.4 Input and Output VSWR versus Frequency Chip Layout
Figure 3.5 Input and Output FET Voltages versus Time Chip Layout
Figure 3.6 Output Voltage versus Time Chip Layout

	Specification	**Pre-Layout Design**	**Chip Layout Design**
Frequency : IN / OUT	24 GHz / 48 GHz	24 GHz / 48 GHz	24 GHz / 48 GHZ
Input Level	+7 dBm	+7 dBm	+7 dBm
Output Level	0 dBm	+7 dBm	+3 dBm
VSWR:			
Input	1.5:1	*N/A	9.5:1
Output	1.5:1	*N/A	11.5:1
Spectral Purity			
Fundamental	>-20 dBc	-30 dBc	-33 dBc
3rd Harmonic	>-20 dBc	-29 dBc	-35 dBc
Bandwidth	2 GHz	2 GHz	2 GHz
Supply Voltage	+ / -5V	+3.5V / -0.5V	+3.5V / -5V

Table 3.1 - Specification Compliance Matrix

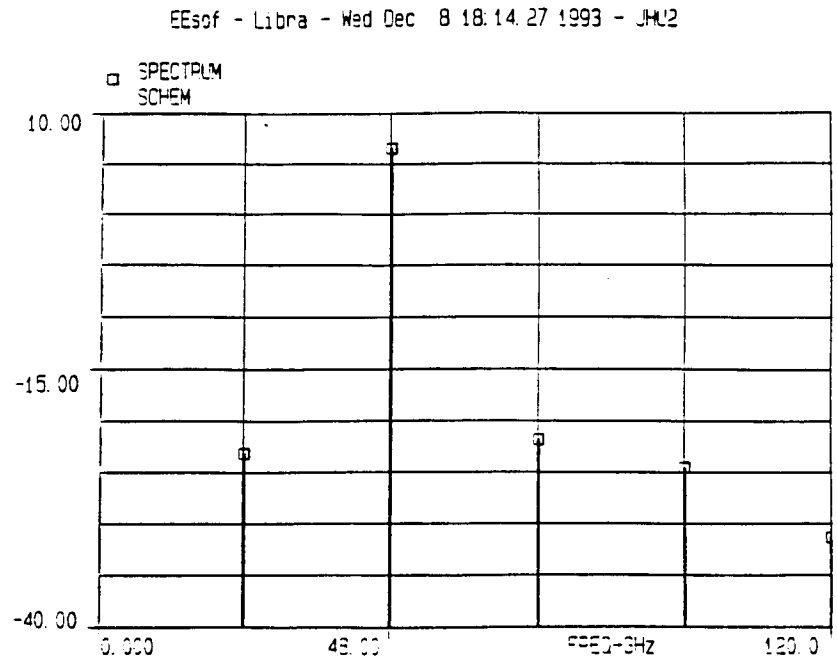


Figure 3.1 - Frequency Spectrum Pre-Layout

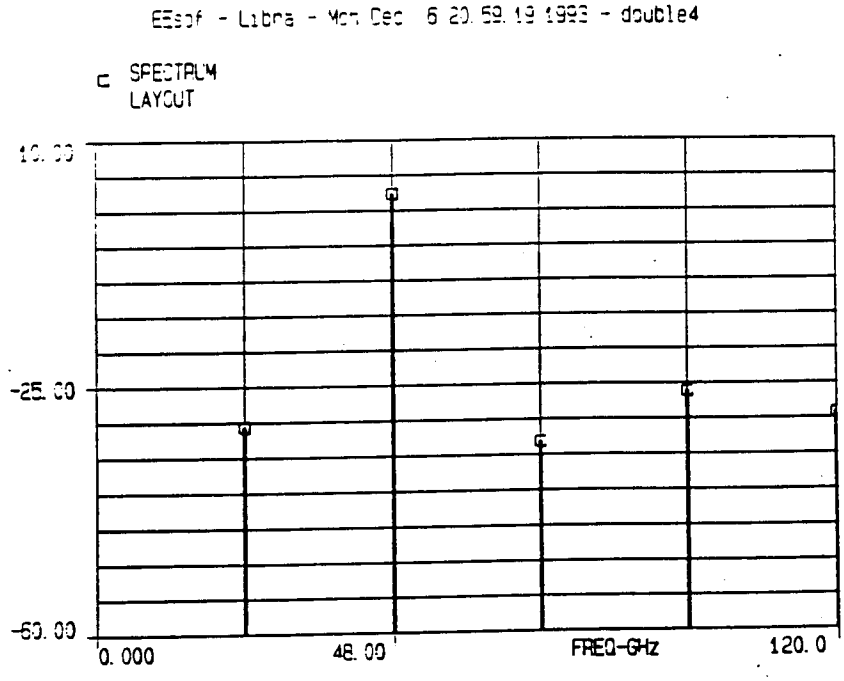


Figure 3.2 - Frequency Spectrum Chip Layout

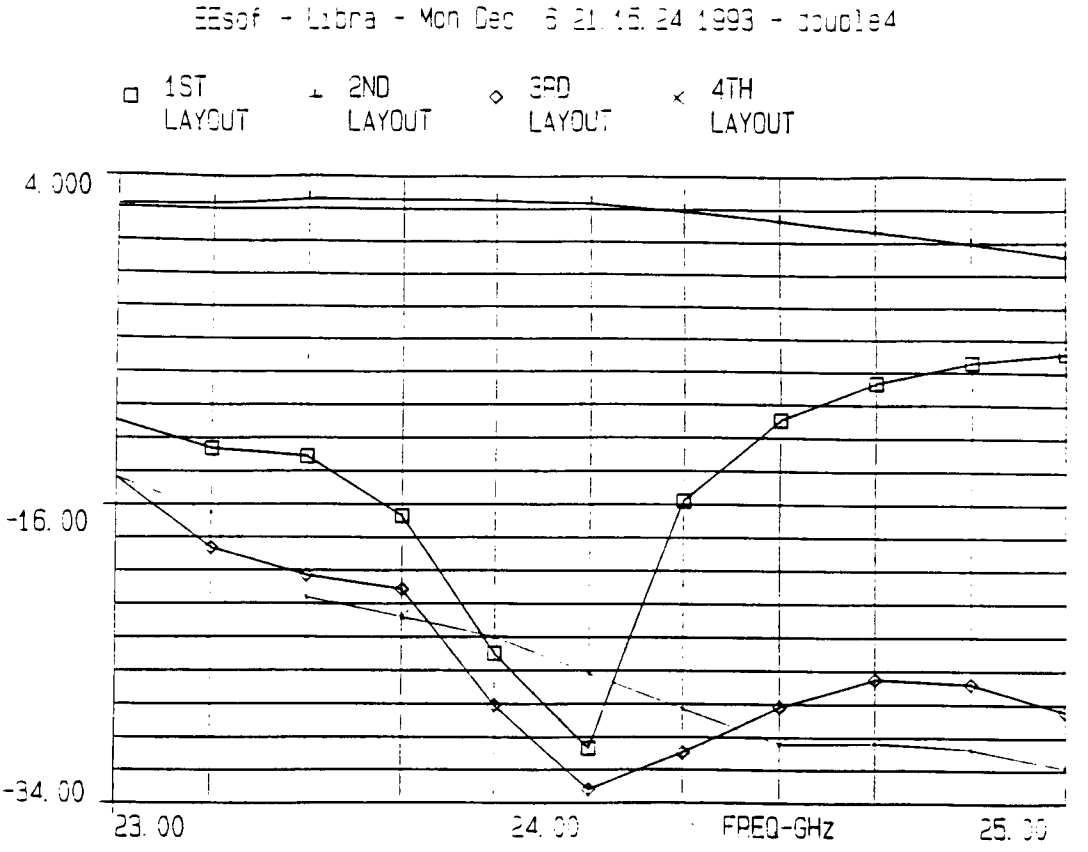


Figure 3.3 - Harmonic Output Power versus Frequency

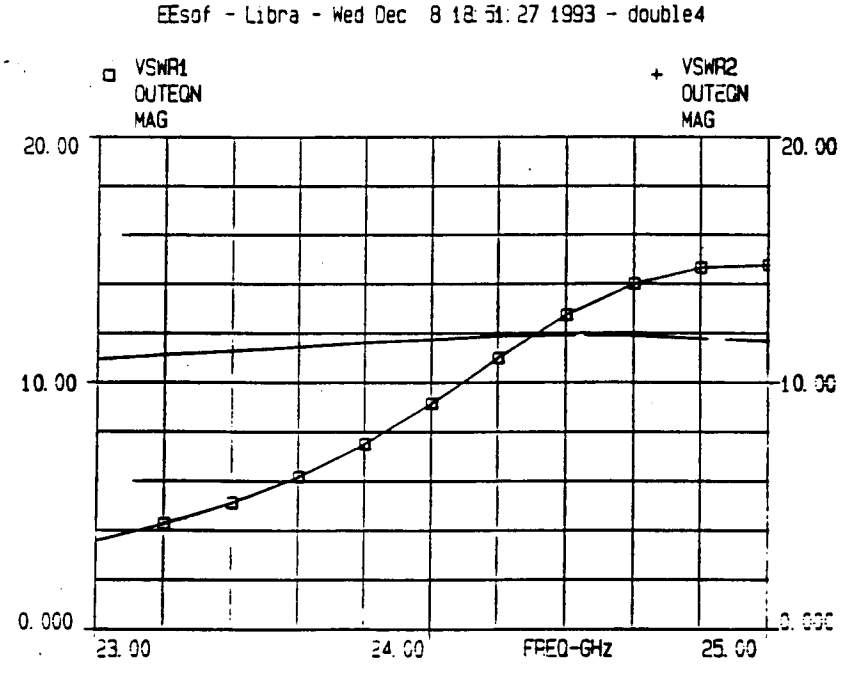


Figure 3.4 - Input and Output VSWR versus Frequency Chip Layout

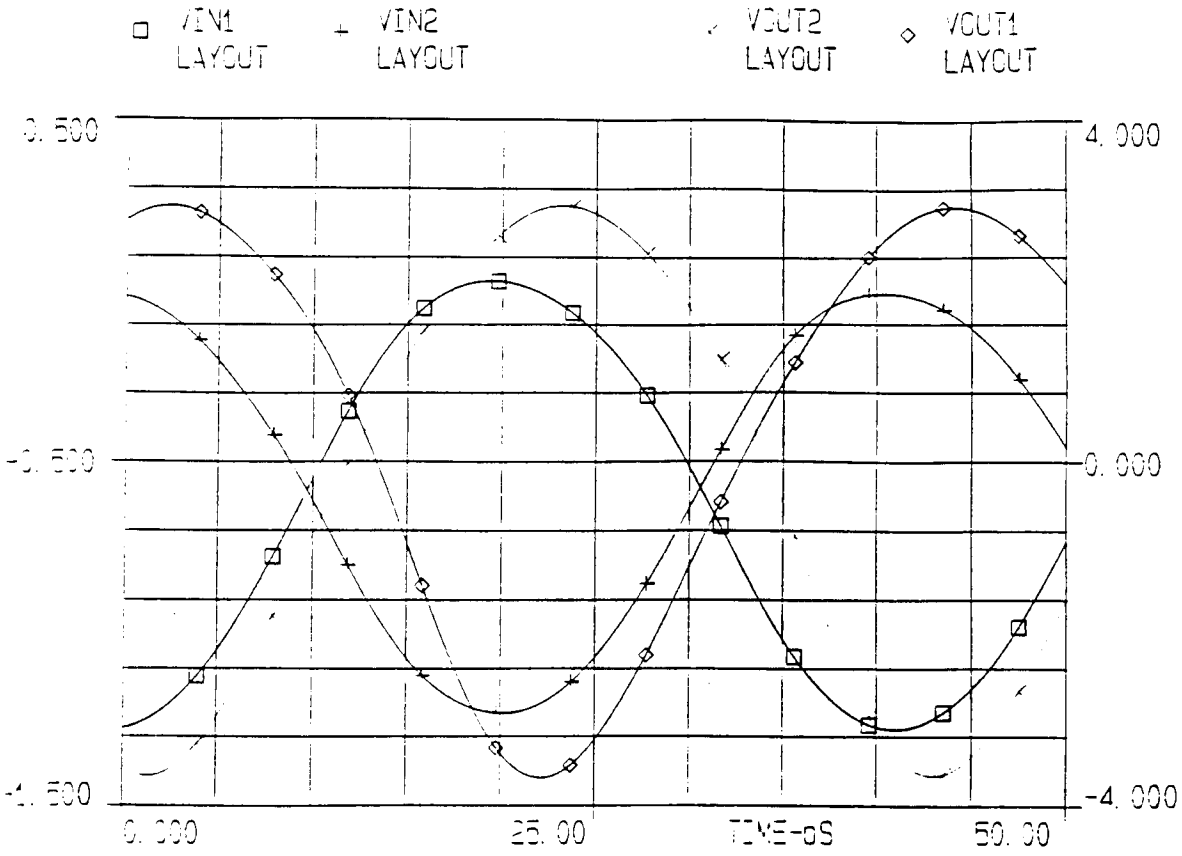


Figure 3.5 - Input and Output FET Voltages versus Time Chip Layout

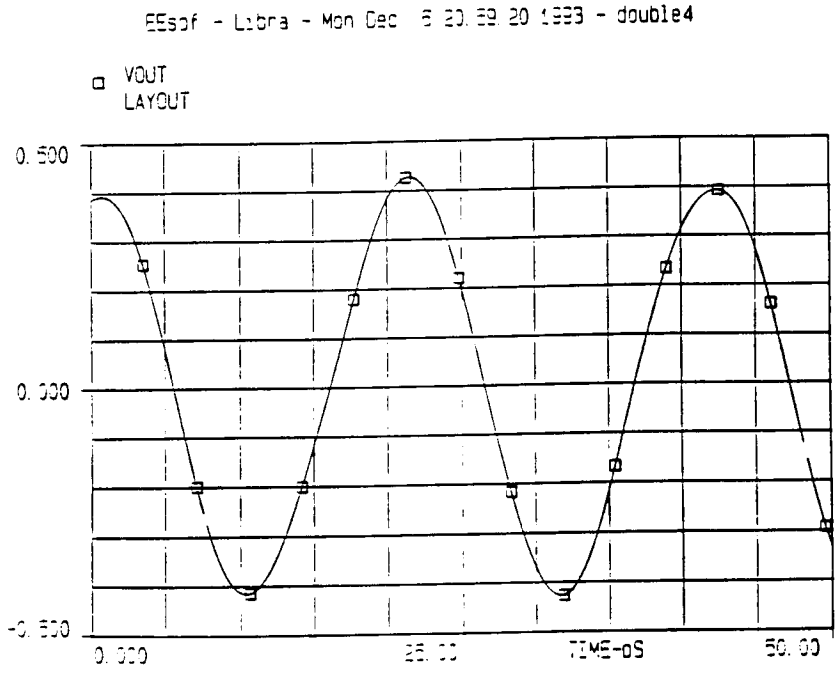


Figure 3.6 - Output Voltage versus Time Chip Layout

Section IV: Schematic Diagrams

Contents in this section include the schematic diagrams for the Pre-Layout and Chip Layout designs.

Figure 4.1 - Pre-Layout Schematic
Figure 4.2 - Chip Layout Schematic
Figure 4.3 - Chip Layout

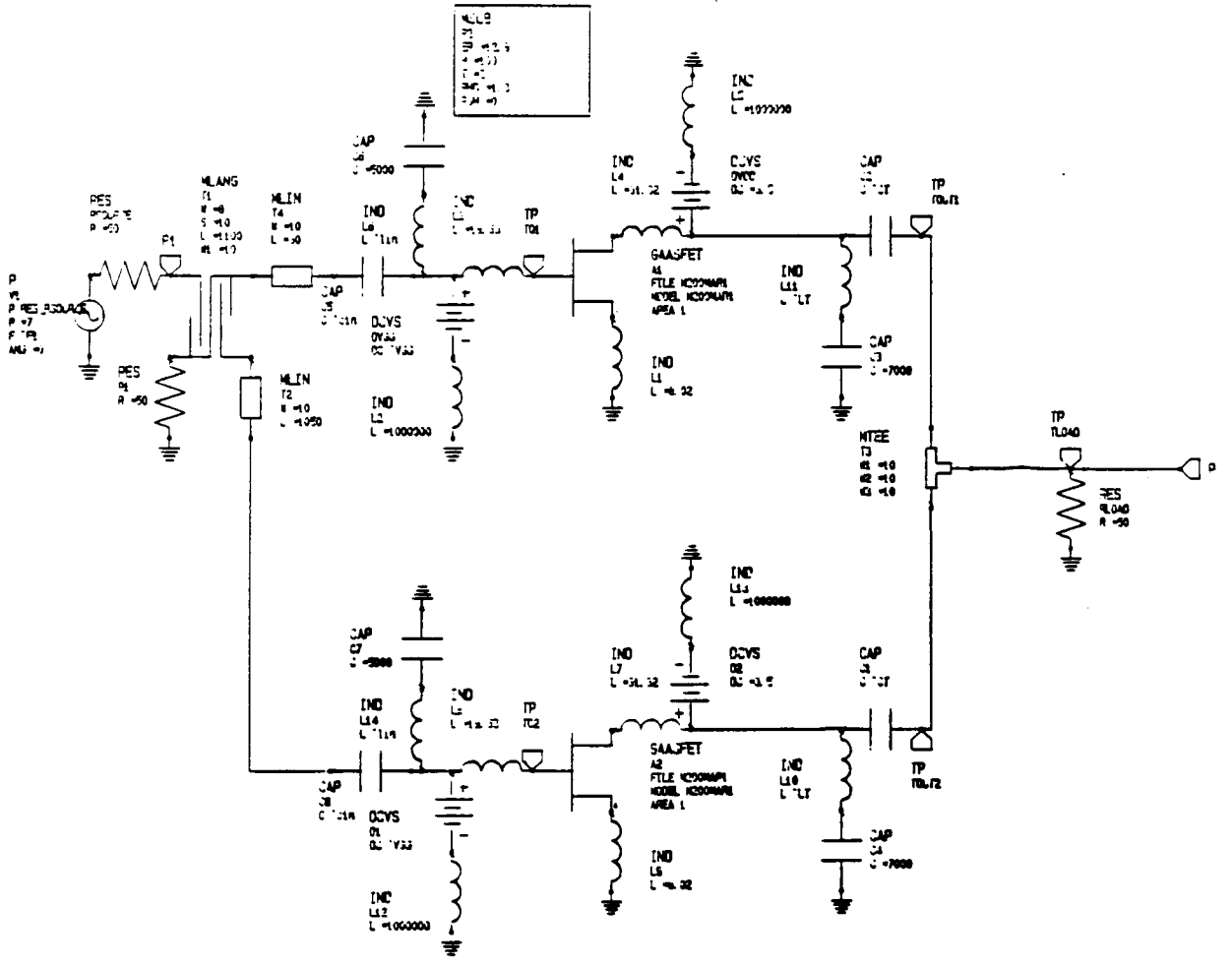


Figure 4.1 - Pre-Layout Schematic

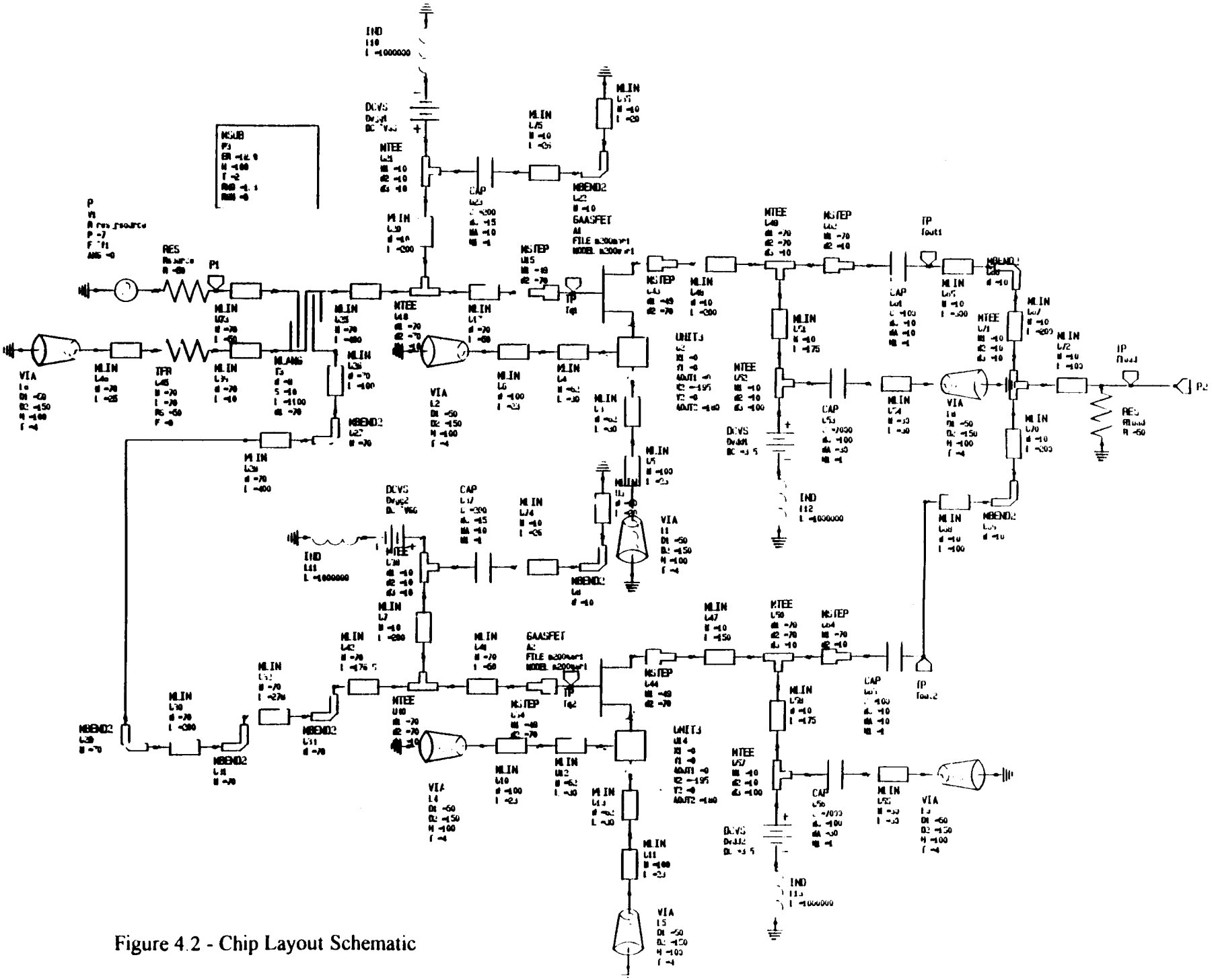


Figure 4.2 - Chip Layout Schematic

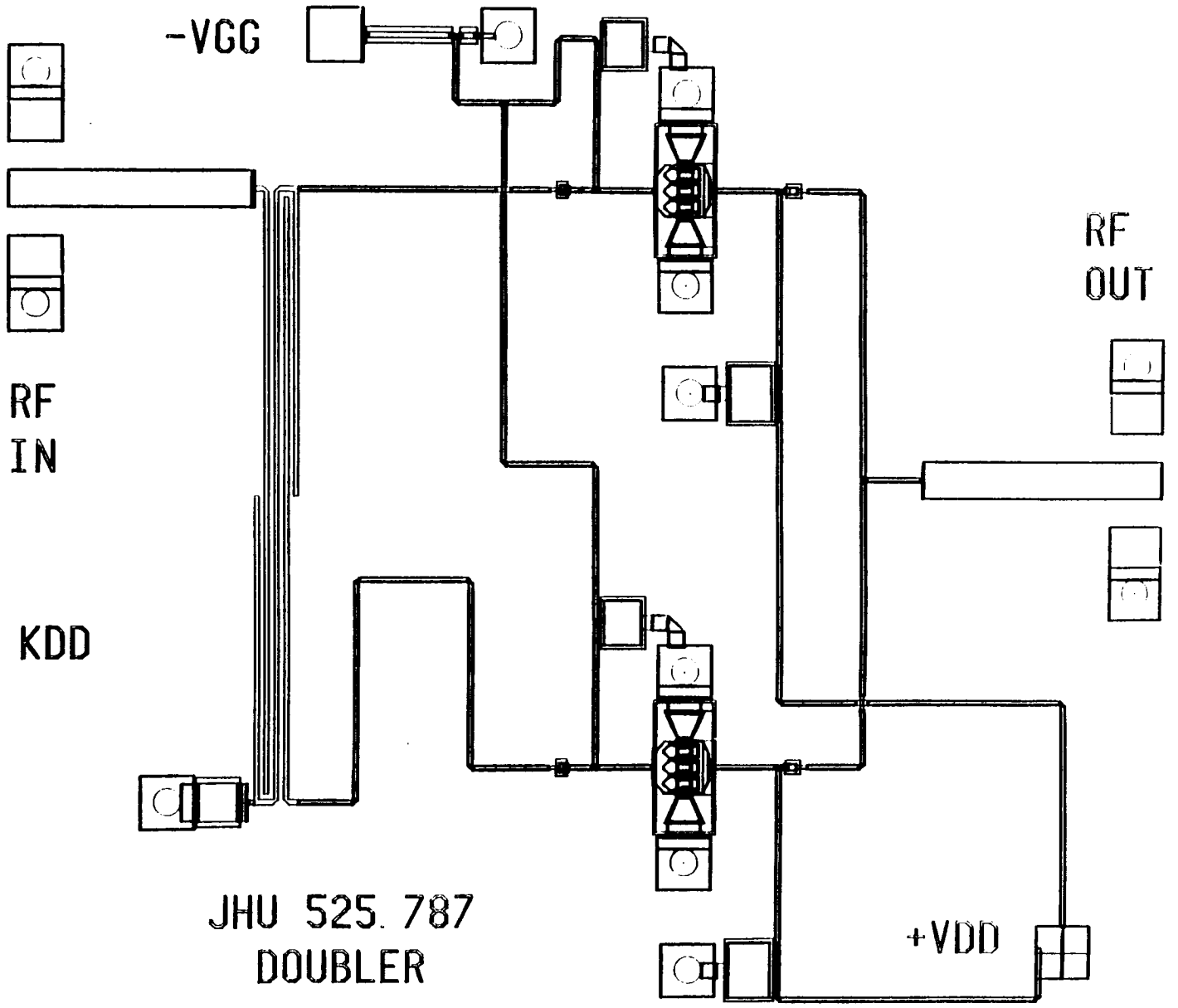


FIGURE 4.3 CHIP LAYOUT

Section V: DC Analysis

This section will show the results of a DC bias analysis. Included our individual node voltages and currents throughout the Chip Layout design. The results of this analysis have been condensed to the two FET nodes which can be viewed in Table 5.1. The Pre-Layout simulations had Vgs = -0.5 V which is very close to the FET pinchoff voltage (Vp) but the Chip Layout used Vgs = -0.6 V. This was chosen to assure nonlinear characteristics with RF applied. The Vgs parameter is very critical in order for optimal circuit performance. Also shown in this section is the I-V curves for the Martin Marietta 200 micron FET (Figure 5.1).

This design uses a passive network consisting of two series resistors supplying the proper gate voltage. Each resistor is 10 microns in width capable of handling 1 mA/micron or 10 mA, well within specifications. Metal1 and metal2 can handle 2 mA/micron and 5 mA/micron, respectively. This poses no deficiency in current handling capabilities for the design, since all line widths are 10 microns or greater.

Network Name	**Device.Terminal**	**Current (mA)**	**Voltage (V)**
Layout	GAASFET_A1.D	0.000066	3.500000
	GAASFET_A1.G	-0.000117	-0.600821
	GAASFET_A1.S	0.000051	-2.9 E-10
	GAASFET_A2.D	0.000066	3.500000
	GAASFET_A2.G	-0.000117	-0.600821
	GAASFET_A2.S	0.000051	-2.9 E-10

Table 5.1 DC Analysis Results

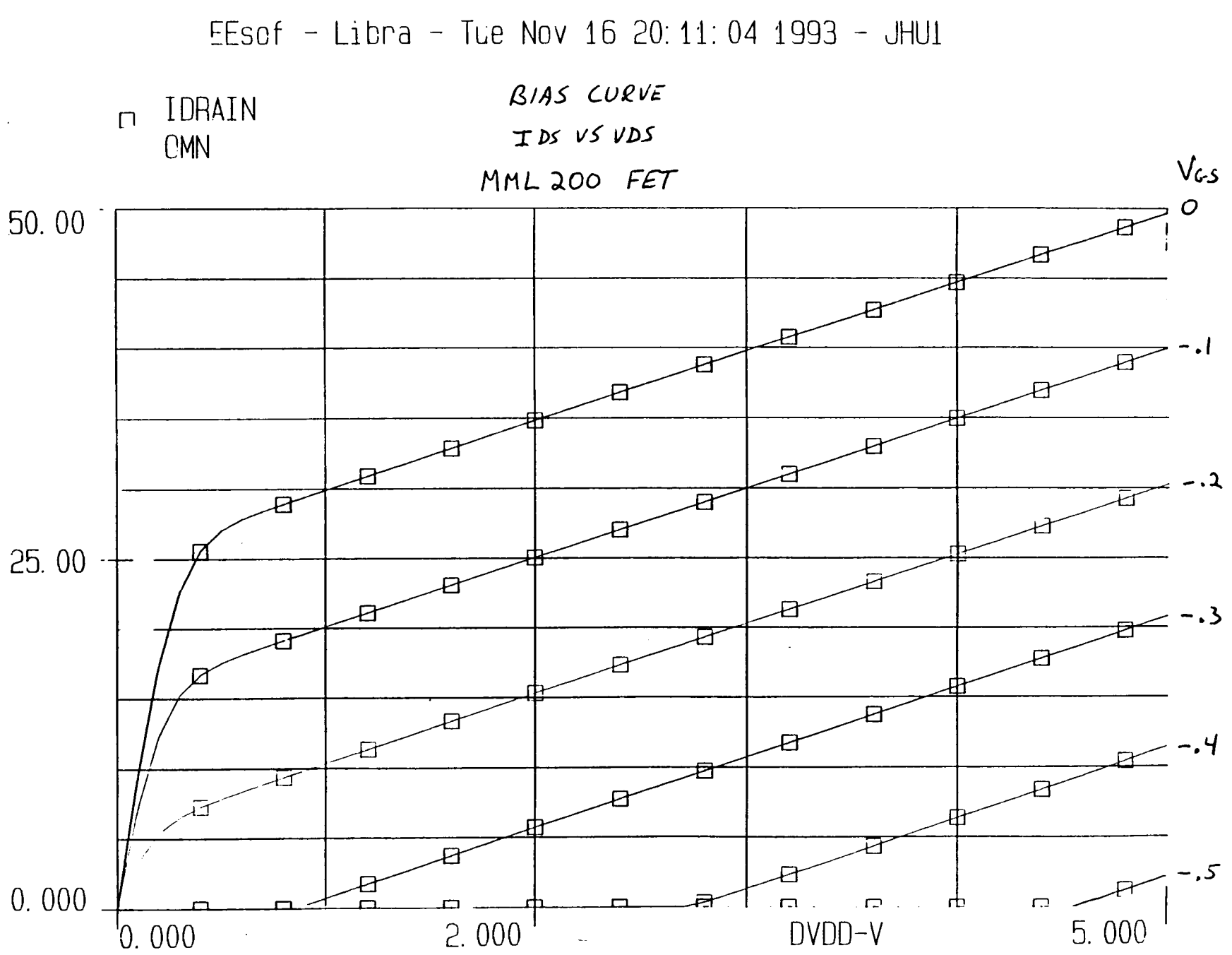

EEsof - Libra - Tue Nov 16 20:11:04 1993 - JHU1
IDRAIN
OMN
BIAS CURVE
IDS VS VDS
MML200 FET
VGS
0
-.1
-.2
-.3
-.4
-.5
50.00
25.00
0.000
0.000
2.000
DVDD-V
5.000

FIGURE 5.1

Section VI: Design Robustness

It is important that a design to be robust in order to maintain high yields. A yield and sensitivity analysis were performed to the Chip Layout. In this analysis certain parameters were varied by a specified percentage and yields produced by establishing performance criteria. The following parameters were varied based on the criteria:

Criteria: Second Harmonic > 0 dBm
Fundamental < -25 dBm
Third Harmonic < -25 dBm

Variables: Input match capacitor (CIN) +/- 10%
Input match inductor (LIN) +/- 5%
Output match capacitor (COUT) +/- 10%
Output match inductor (LOUT) +/- 5%

From this the following histogram plots were produced based on 50 trials.

Figure 6.1 - Second Harmonic Output Power
Figure 6.2 - Fundamental Output Power
Figure 6.3 - Third Harmonic Output Power
Figure 6.4 - CIN Sensitivity
Figure 6.5 - LIN Sensitivity
Figure 6.6 - COUT Sensitivity

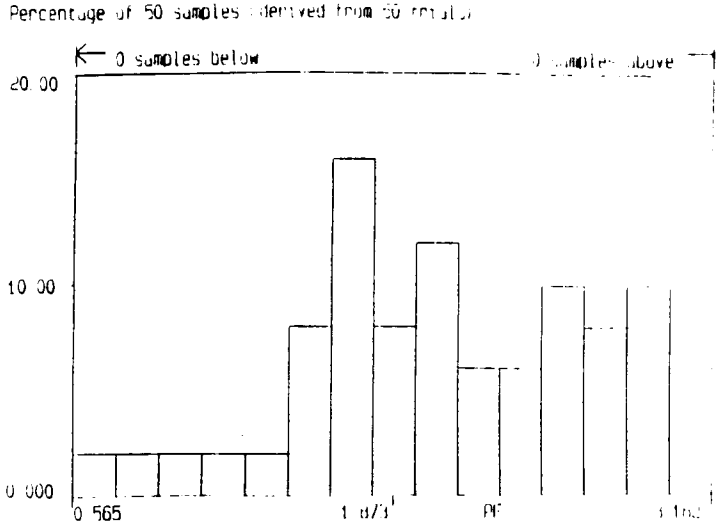


Figure 6.1 - Second Harmonic Output Power

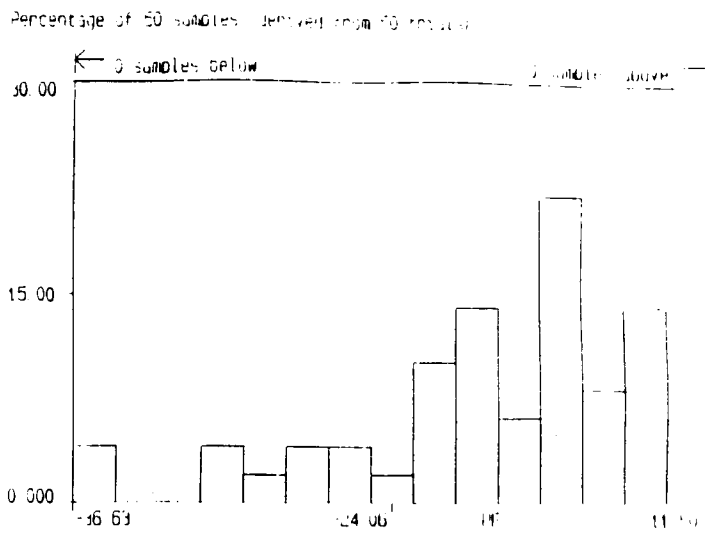


Figure 6.2 - Fundamental Output Power

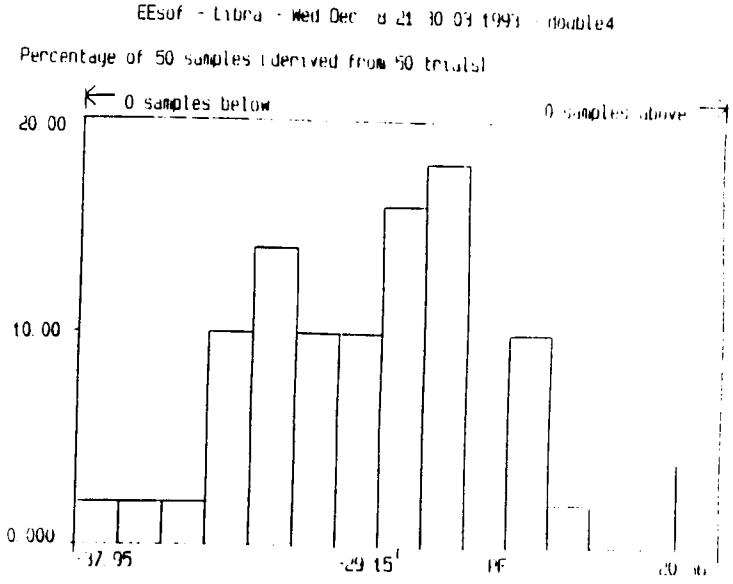


Figure 6.3 - Third Harmonic Output Power

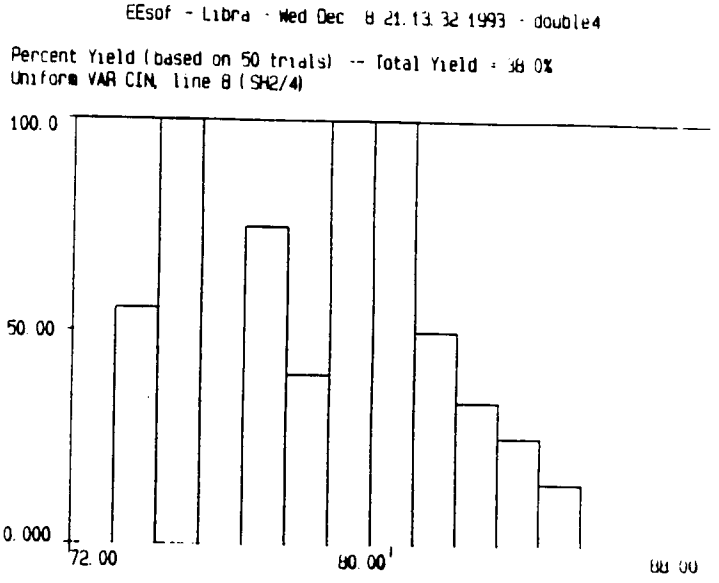


Figure 6.4 - CIN Sensitivity

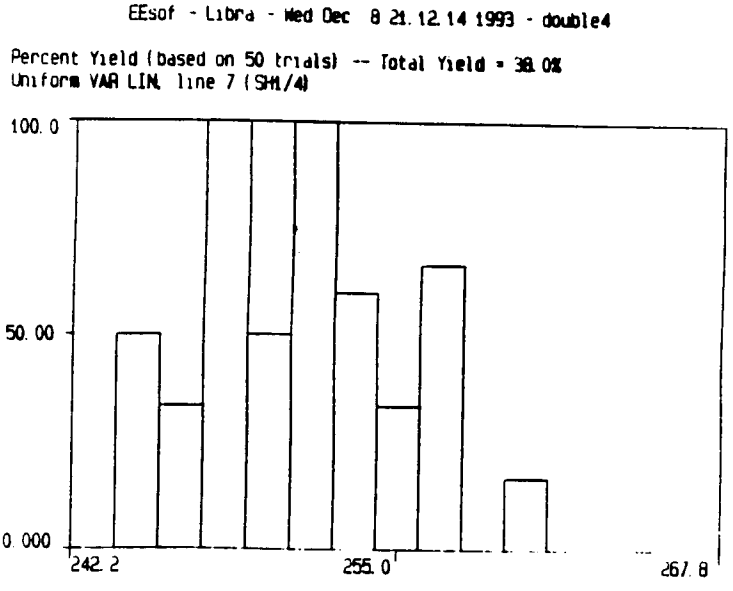


Figure 6.5 - LIN Sensitivity

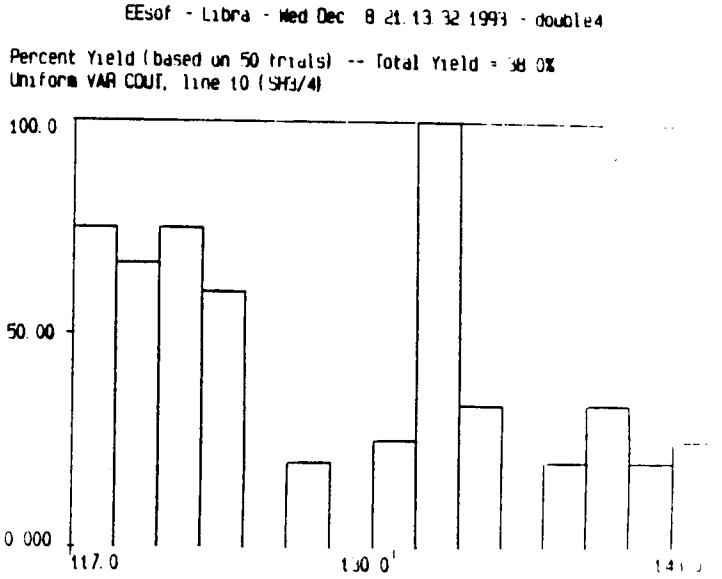
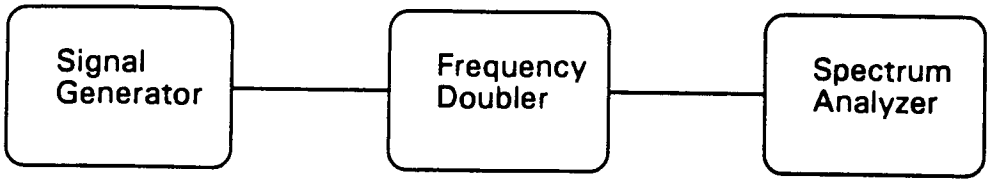


Figure 6.6 - COUT Sensitivity

Section VII: Test Plan

A. Power Output Measurement

Measuring Power out versus Frequency can only be measured to the second harmonic since the third harmonic frequency exceeds the test equipment capabilities. The following test setup may be used as shown in Figure 7.1.



Apply -5V first, then apply +3.5V to the circuit. Set the signal generator frequency to 24 GHz with the output at +7 dBm. Observe output and adjust supply voltages for maximum isolation between the second harmonic and fundamental.

Record: Vgg = Volts
Vdd = Volts

Signal Generator Frequency (GHz)	Fundamental Signal Level (dBm)	Second Harmonic Frequency (GHz)	Second Harmonic Signal Level (dBm)
23.50 GHz		47.00 GHz	
23.75 GHz		47.50 GHz	
24.00 GHz		48.00 GHz	
24.25 GHz		48.50 GHz	
24.50 GHz		49.00 GHz	

B. VSWR Measurements

For the input VSWR calibrate the HP 8510 for a 1-port measurement.
Signal Generator = +7dbm
Center Frequency = 24 GHz
Span = 1 Ghz

For the output VSWR calibrate the HP 8510 for a 1-port measurement.
Signal Generator = +7dbm
Center Frequency = 48 GHz
Span = 2 Ghz

Plot input and output VSWR measurements.

Section VIII: Conclusion

The Pre-Layout circuit would not simulate over a swept frequency range, it could not converge was the error message. In order for the circuit to simulate, the matching networks were altered thus degrading performance. On the other hand, this was not experienced with the Chip Layout circuit. The only change was an increase in Vgs from -0.5V to -0.6V probably due to circuit losses induced by an increase in elements.

Overall, I found this project to be challenging and enriching. For the time allotted this project and the work involved, I feel the project required two people. I wish for more time to further analyze this design in order to assure that the final product will be successful.