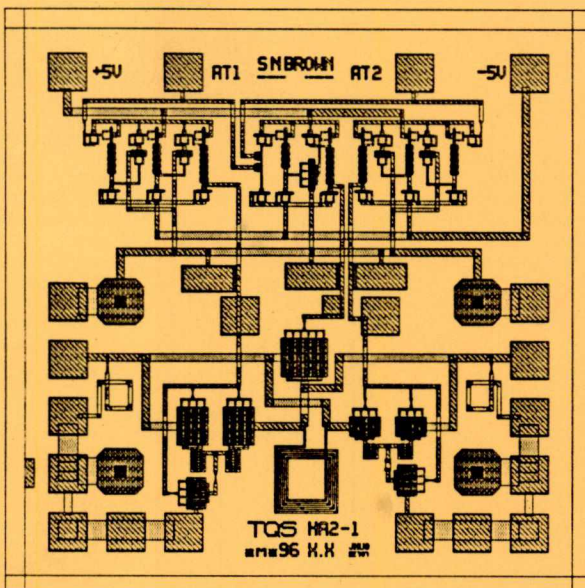
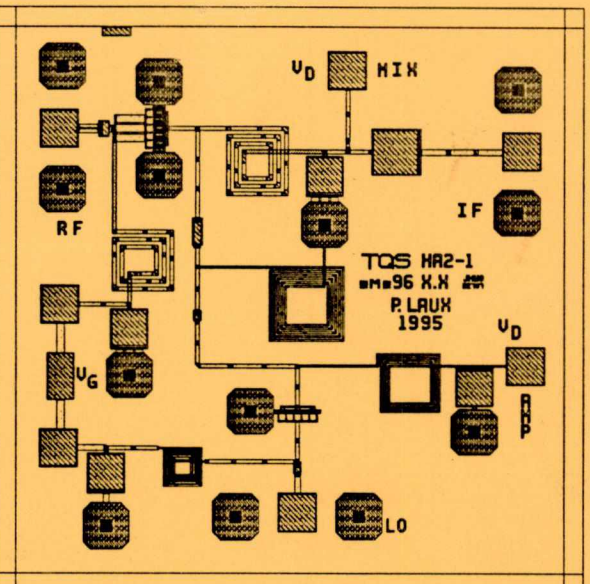
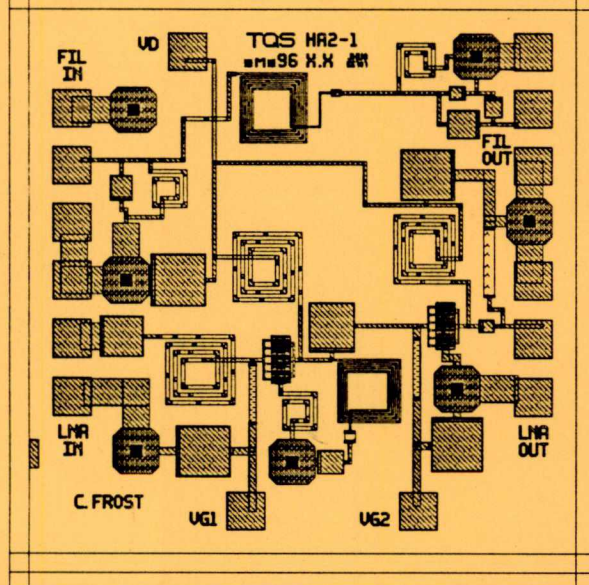
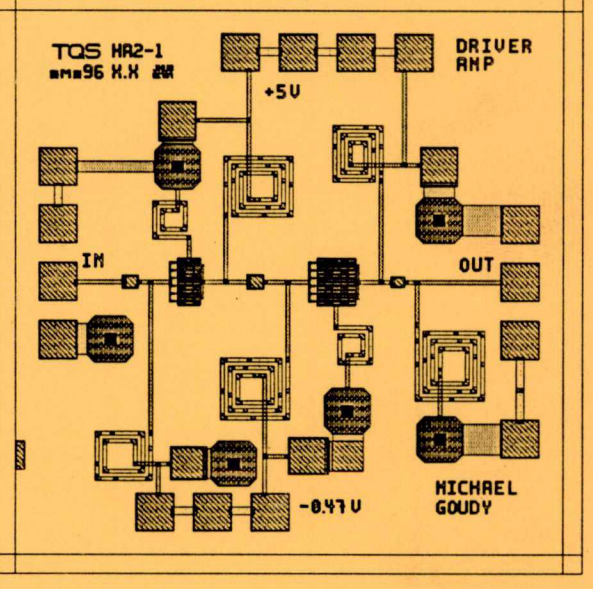
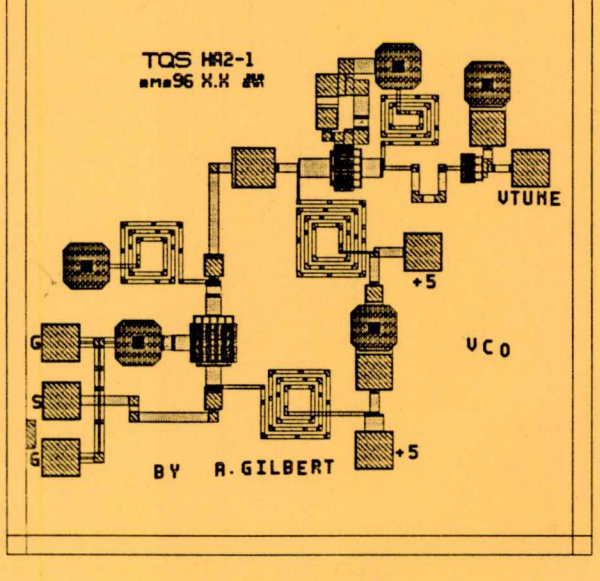










MMIC DESIGN
JHU EE 787
FALL 1995
STUDENT PROJECTS

5.7 GHZ ISM TRANSCEIVER

ATTENUATOR - S. BROWN
LNA - C. FROST
DRIVER AMP. - M. GOUDY
VCO - A. GILBERT
MIXER - P. LAUX

Step Attenuator
MMIC Design
The Johns Hopkins University
EN 525.787

Scott Brown
Fall 1995

Summary

The design outlined in this report is the product of the MMIC Design course taught at The Johns Hopkins University Whiting School of Engineering (EN 525.787). The circuit was designed, simulated and placed for fabrication using the TriQuint Semiconductor HA2 process. An RF Step Attenuator has been developed for C band ISM application.

Introduction

The MMIC step attenuator controls the signal amplitude of the transmit path of an ISM transceiver. Step values of 3 dB and 7 dB are commanded by a two bit digital control. Two primary circuits in the design are the RF attenuator section that has the switches routing RF to different paths having varying attenuation levels, and the digital level translator section that converts TTL inputs into FET gate control signals.

Three circuits were initially considered for this design (see the Design Selection chart). Circuit 3 has TEE attenuators in series with large FET switches to shunt the RF around the section not in use. Design 2 uses FET switches to change the attenuator resistor values that make up a common TEE attenuator. Both these rejected circuits required too many FETs in order to meet the aggressive insertion loss spec. As a result, the control circuitry for these designs become prohibitive. Both rejected circuits suffer from unrealistically low resistor values that make up the TEE attenuators. Design 1 was chosen over the other two since it offers low insertion loss, realistic resistor values, and simple control logic. To design a circuit that has the best chance of fitting on the ANACHIP, the option of having a fourth attenuator state of 10 dB was not realistic.

At the heart of the RF attenuator section are FET switches that switch in one of three parallel RF paths: Thru, 3 dB and 7 dB. The thru path is constructed with a wide, 600 μm, FET chosen for its low insertion loss which is essential to meeting the 1 dB insertion loss spec. Large distributed capacitance of this FET is resonated out with an inductor which greatly increases the isolation state of the switch. The TEE attenuator branches are switched in for the desired attenuator states.

The digital logic control section uses multi-stage level shifting circuits to convert the two TTL control signals into the three gate FET control signals (one FET control signal for each RF path). The translator has been designed to run off $\pm$5V. The two attenuator path FETs are controlled with FET_DRIVER block and the large shunt RF FET must interpret the two control signals with a combinatorial OR logic constructed with diode logic found in the FET_LOGIC block.

Modeled Performance

Design Goal	Units	Design Goal	Modeled Performance
IL	dB	1 (max)	1.2
Step 1	dB	3 ± 0.5	3.2
Step 2	dB	7 ± 0.5	6.9
Freq, Center	MHz	5800	5800
Bandwidth	MHz	150	> 4000
VSWR	dB	-14	< -19.5
Control Voltage	-	TTL	TTL
Supply Voltage	V	± 5	± 5
Size	mil	60 x 60 ANACHIP	60 x 60 ANACHIP

Modeling the attenuator circuit was done in two stages: (1) the RF attenuator block, and (2) the digital logic and control block. Because mature models were not available for both DC and RF simulations, the RF section of the attenuator was modeled with specific RF FET models optimized for the switch configuration and tested in a linear test bench. The digital logic and control circuit was tested in a DC test bench using the non-linear FET model. Unfortunately the two models couldn't be merged to test both circuits working together.

The non-linear FET models developed for RF simulators don't accurately model the RF performance of a FET in the pinched off region where the FET acts like a switch. An inclass handout suggests the model to be used and allows RF simulations when the gate to source voltage is held constant (see the FET Switch RF Model). This model is for a 300 μm FET, other size FETs required the element values to be scaled proportionately. The switch FETs were simulated with a V_{gs} of 0V in "on" state and -4V in the "off" state. A hierarchical model of the FET switch was created to ease simulation and circuit tuning. The circuit was configured to be in the "thru" state where the signal passes through the large bypass FET and the insertion loss is measured for reference. The attenuator is then commanded to be in the 3dB attenuation state, with respect to insertion loss. The resistors that make up the TEE attenuator are tweeked until this path meets spec. Notice in the layout that 4 parallel resistors were required to achieve the series resistance for each attenuator. The smallest NiCr resistor the TQSRESL allows is 25 Ω and a value of about 6 Ω is required. A parallel combination of five resistors would allow the resistances to be optimized to better match the reflection coefficient though the circuit meets spec with substantial margin.

The control circuit was simulated using the TQSNFET non-linear FET model. The two main circuits are based on an input TTL being level shifted with a series of diodes to create a negative bias. The bias then controls the gate of a FET that provides the circuit with gain. In the case of the "driver" circuit, a third state is

required to invert the control voltage again so the sense of the circuit in correct. In the case of the "logic" circuit, the input is designed to be pulled "low" until either, or both, of the input control signals pull the input "high". This is accomplished with diodes that allow a simple diode logic gate to be realized. The input is then level shifted and passed to a single gain/level-shift state similar to the one described above. During simulations, the gate widths were adjusted to set the threshold voltage to 1/2 of the +5V supply so there is margin on either side for process variances that the FET model was not able to reflect. Quite a bit of effort was spent on reducing the current requirement of the driver circuits. The initial circuits required about 15mA each and the final design requires 7 or 8 mA each.

DC Analysis

DC analysis only really applies to the driver circuitry used to generate the FET control voltages. Small FETs were used with no more than 3mA flowing from drain to source in all cases. Though cumbersome to do DC analysis using the Libra software, the graphs of the voltages and currents are shown during a switching event. Notice the drivers have substantial gain to quickly transition the output from one voltage to the other. This is essential to increase the noise immunity of the circuit and is further helped by the driver going from one voltage limit to the other. The driver circuits are designed to operate from 0V to about 1.5V for the "low" level and about 3.5V to 5V for the "high" level. These comply with the levels of all TTL families, however, the CMOS and ACT / HCT families of TTL will ensure a drive of almost 0V to 5V yielding the most best choice for digital control driver for this attenuator.

Stress on the circuit is also limited to the driver circuitry since the RF attenuator circuit only receives gate voltages of 0V or -4V with no current flow and the RF level is in the milliwatt level. As stated above the current in each branch of the driver circuits never exceeds 3mA (or 0.6mA/μm max). Most of the current handling traces are made with all 3 metal layers and can handle a current density of 28mA/μm. The same current density is also present at the N- implant resistors when the TTL input is pulled "low".

Test Plan

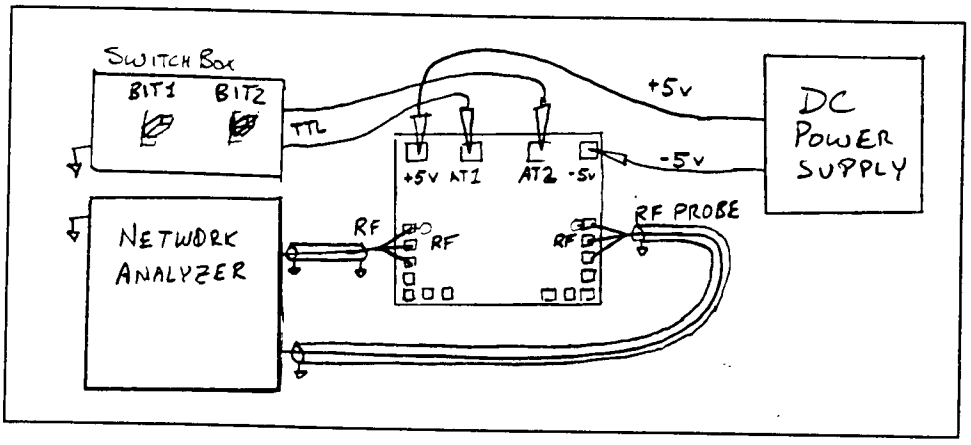
The attenuator chip has been laid out for wafer probing as well as in-package testing. There is an RF input and output for RF wafer probes to contact with the three pad (ground-signal-ground) arrangement. Two DC power and two TTL control signals are provided with DC probes to perimeter pads. RF performance is monitored while changing the TTL control signals.

Required Test Equipment:

1 Network Analyzer (HP 8510 or equiv.)
2 DC power supplies, +5 V and -5 V
1 Switch assembly test box to provide TTL control signals, or

two independent power supplies

1 Wafer probe station with
- 2 RF probes (ground-signal-ground)
- 4 DC probes



Test Procedure:

1) Set the network analyzer to a center freq of 5800 MHz and a span of 500 MHz. Set the power level to 0 dBm.
2) Calibrate the network analyzer and wafer probe station following the vendors calibration procedures.
3) Place attenuator chip to be tested in probe station fixture.
4) Set the two power supplies to + and - 5V. Turn off the supplies and connect them to two DC probes and position probe so they touch the DC pads on the chip (one pad per supply).
5) Connect the two control lines from the switch assembly test box to two DC probes. With switch assembly box off, position the probes to touch the two control signal pads.
6) Move the RF probes to rest on the RF input and output pads.
7) Turn ON the DC power supplies to the chip under test, turn on the switch assembly test box if it does not turn on with the chip's power supplies.
8) Set the test box switches to bit1 = 0, bit2 = 0 logic level. Measure the S parameters for this state.
   $S_{21} = S_{12}$ = IL: 1.2 dB (nom)
   $S_{11} = S_{22}$: < -14 dB
   Bandwidth: >150 MHz
9) Set the test box switches to bit1 = 1, bit2 = 0 logic level. Measure the S parameters for this state.
   $S_{21} = S_{12}$ = IL: IL+3 $\pm$ 0.5 dB
   $S_{11} = S_{22}$ = <-14 dB
   Bandwidth: >150 MHz
10) Set the test box switches to bit1 = 0, bit2 = 1 logic level. Measure the S parameters for this state.

$S_{21} = S_{12}$ = IL: IL+7 $\pm$ 0.5 dB
$S_{11} = S_{22}$ = <-14 dB
Bandwidth: >150 MHz

11) Turn the test box switches to bit1 = 0, bit2 = 0 logic level. Turn off the power supplies. Tests are complete.

Note: In the event the chip does not seem to work and the control circuitry is suspect, airbridges connecting the drivers and the RF attenuator section can be broken. Probe pads have been provided to inject a voltage between 0V for selection of the attenuation path and -4V for turning off path.

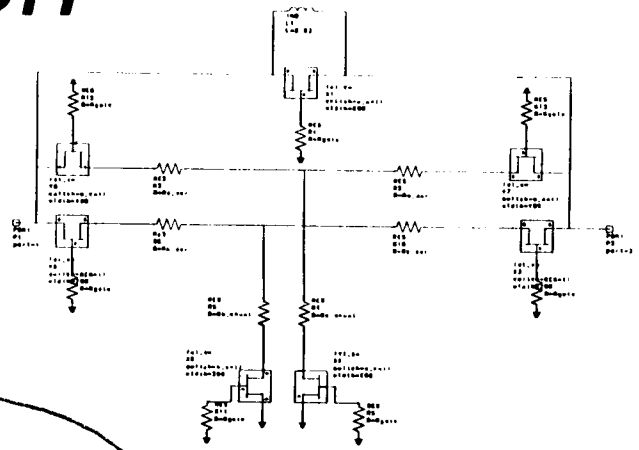
Conclusion and Recommendations

The MMIC design discussed in this paper meets all required specs except insertion loss by 0.2 dB. The circuit just barely fits within the ANACHIP dimensions. Test pads have been provided for chip level RF and DC probing.

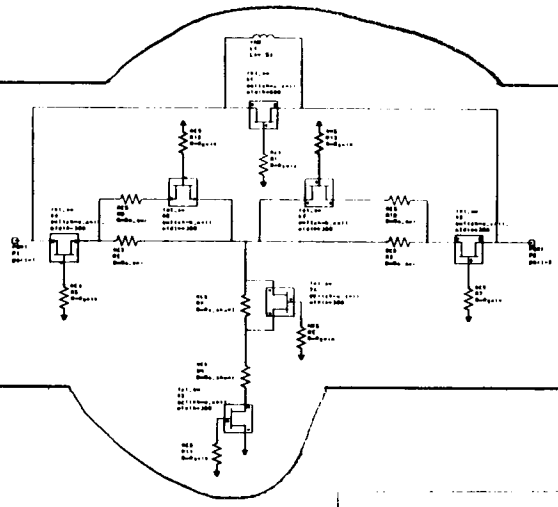
During the layout of this chip a couple of frustrations were experienced with the RF design tool, Libra. The most annoying being the frequent crashes that take about 5 minutes to unfreeze the workstation. A crash always occurred when a hierarchical symbol value was edited in the Layout screen. A SPICE workstation running PROBE postprocessor would allow faster and easier to interpret DC simulations. The Libra simulation of each driver circuit would take over 30 seconds to complete and only the data prearranged to measure was recorded.

Design Selection

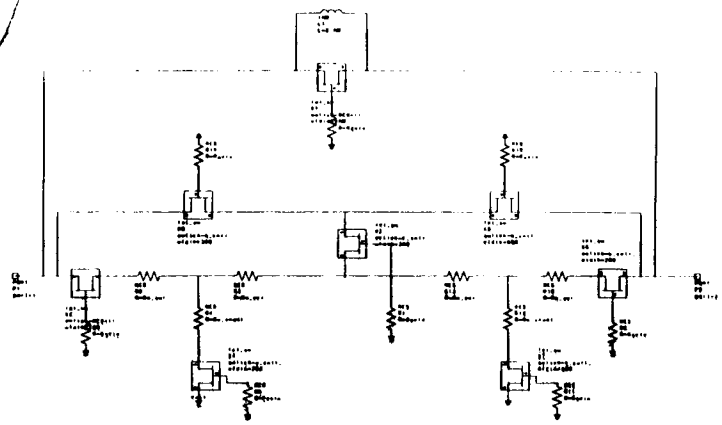
①
- Best Choice
- IL = 0.9 dB
- Uses largest NiCr resistor values
  - 3 dB ~ 6 Ω series / 154 Ω shunt
  - 7 dB ~ 12.9 Ω series / 61 Ω shunt
- Simple control logic



②
- IL = 0.8 dB
- Resistors for 3 dB pad too small
  - 3 dB ~ 1.8 Ω series / 346 Ω shunt
  - 7 dB ~ 16.6 Ω series / 50 Ω shunt

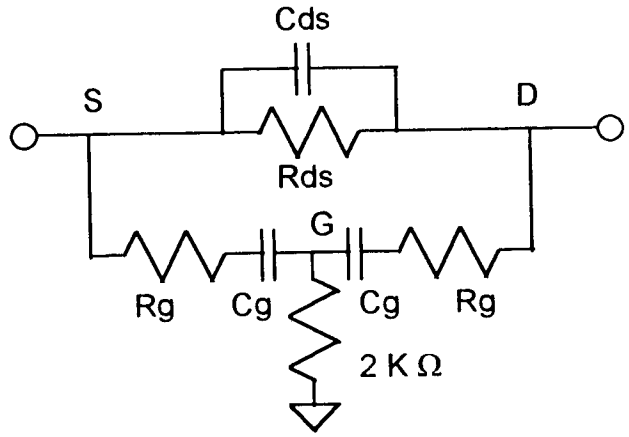


③
- IL = 0.8 dB
- Resistors for 3 dB attn too small
- Control logic very complicated
- Extra FETs required to keep IL low



CIRCUIT DETAILS

- FET Switch RF Model:



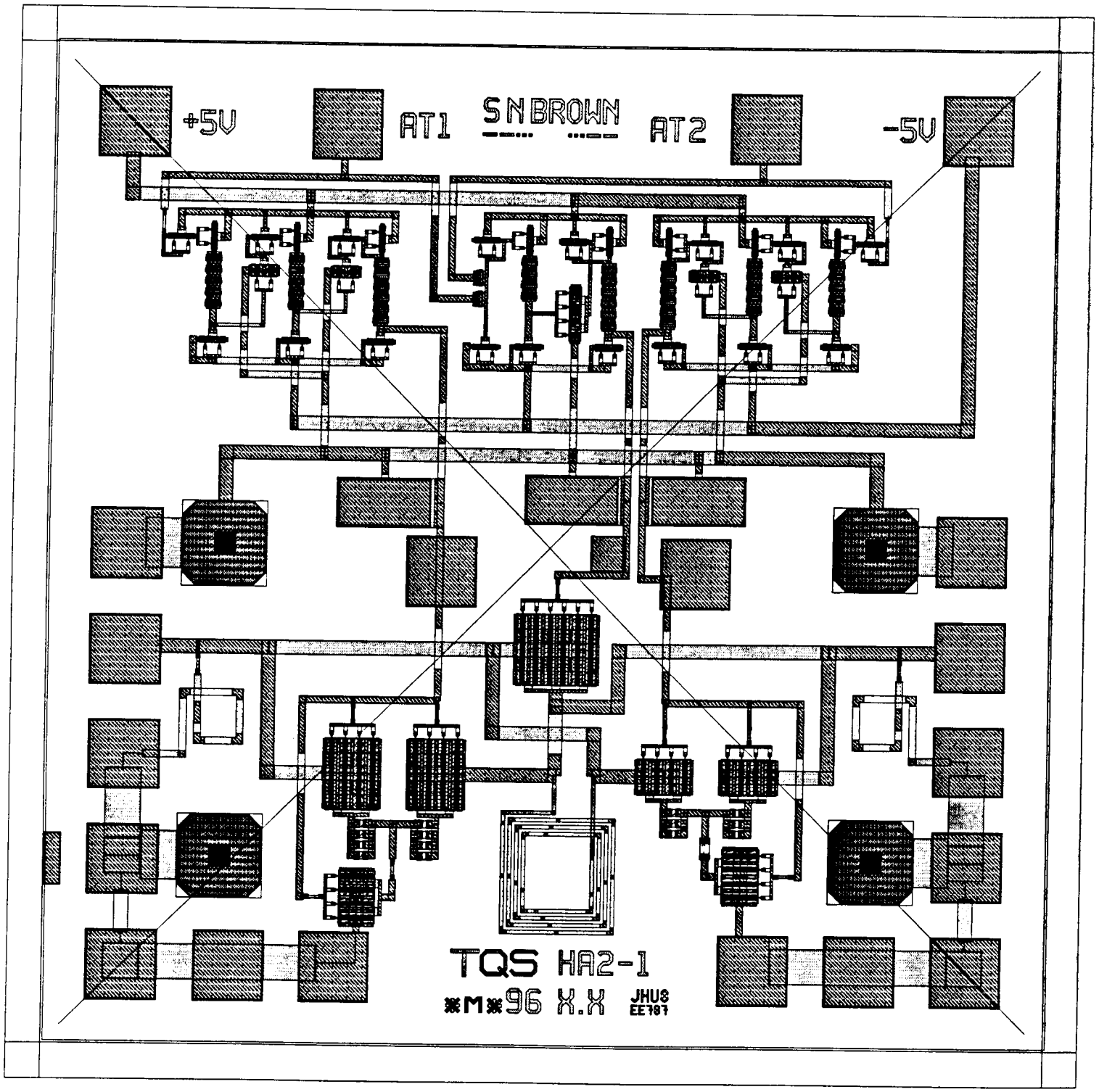
FET Scaling Relationships:
C ~ W*N; R ~ 1/(W*N)

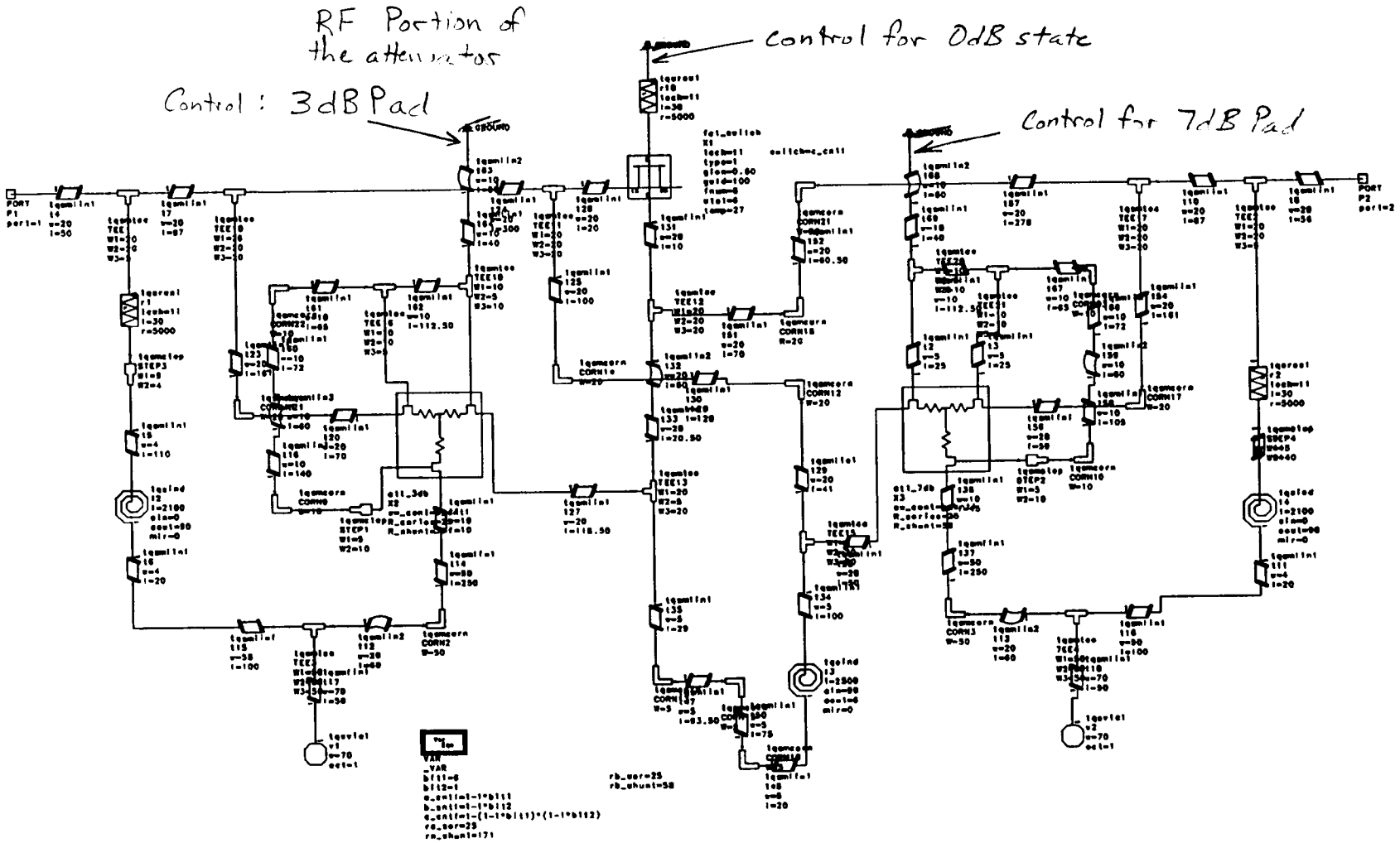
FET Switch Performance vs Size

Total Width (um)	S21 of Fet ON (dB)	S21 of Fet OFF (dB)	S21 w/ Lds ON (dB)	S21 w/ Lds OFF (dB)
100	-2.5	-17.5	-2.5	-44
200	-1.4`	-11.6	-1.4	-44
300	-1.0	-7.1	-1.0	-48
600	-0.6	-4.0	-0.6	-40

Model Values for 300um FET Width

	Vgs (V)	Rds (Ω)	Cds (pF)	Rg (Ω)	Cg (pF)
THRU	0.0	10.51	0.08	1.22	0.1516
ATTN	-4.0	20K	0.08	4.13	0.0711

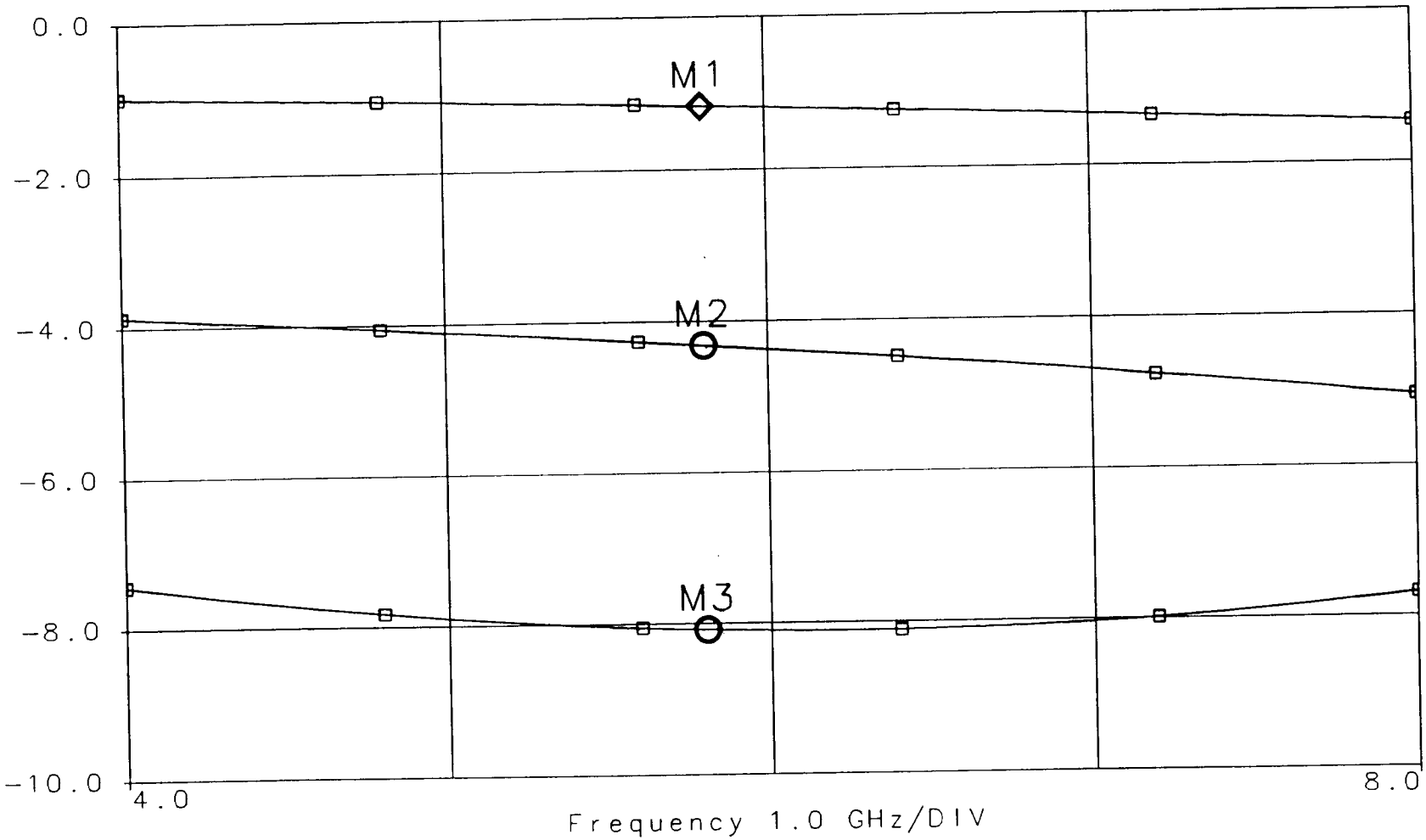

+5V
AT1
S.N.BROWN
AT2
-5V
TQS HA2-1
*M*96 X.X
JHUS
EE781



Control = 0v for selection
-4v for unused path

attn_prj_tb
S21
attn8_prj
S[2,1]
dB

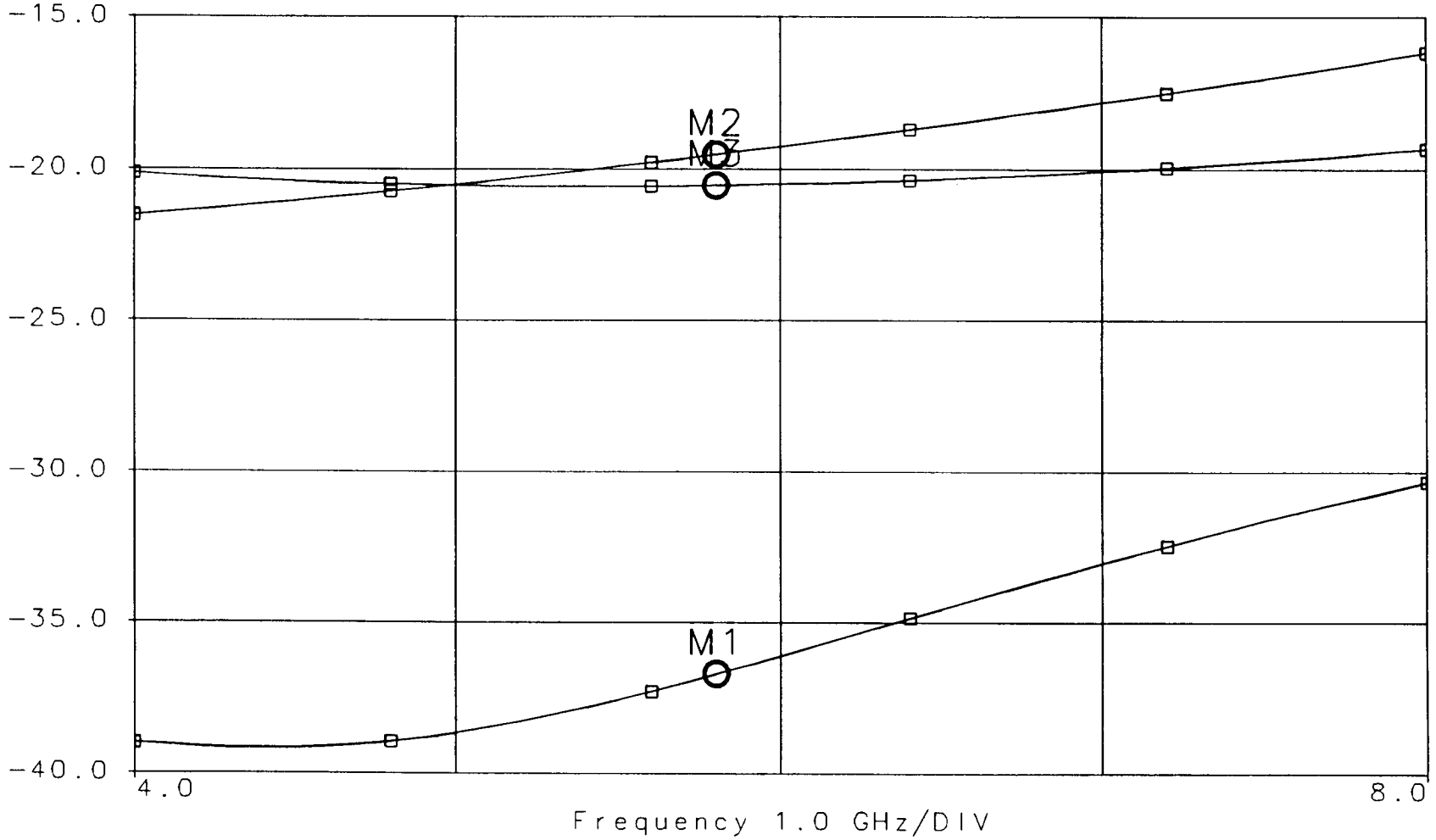
ATTN8_PRJ



Freq = 5.8 GHz
IL = -1.17 dB
3 dB (nom) = 3.15 dB (actual)
7 dB (nom) = 6.92 dB (actual)

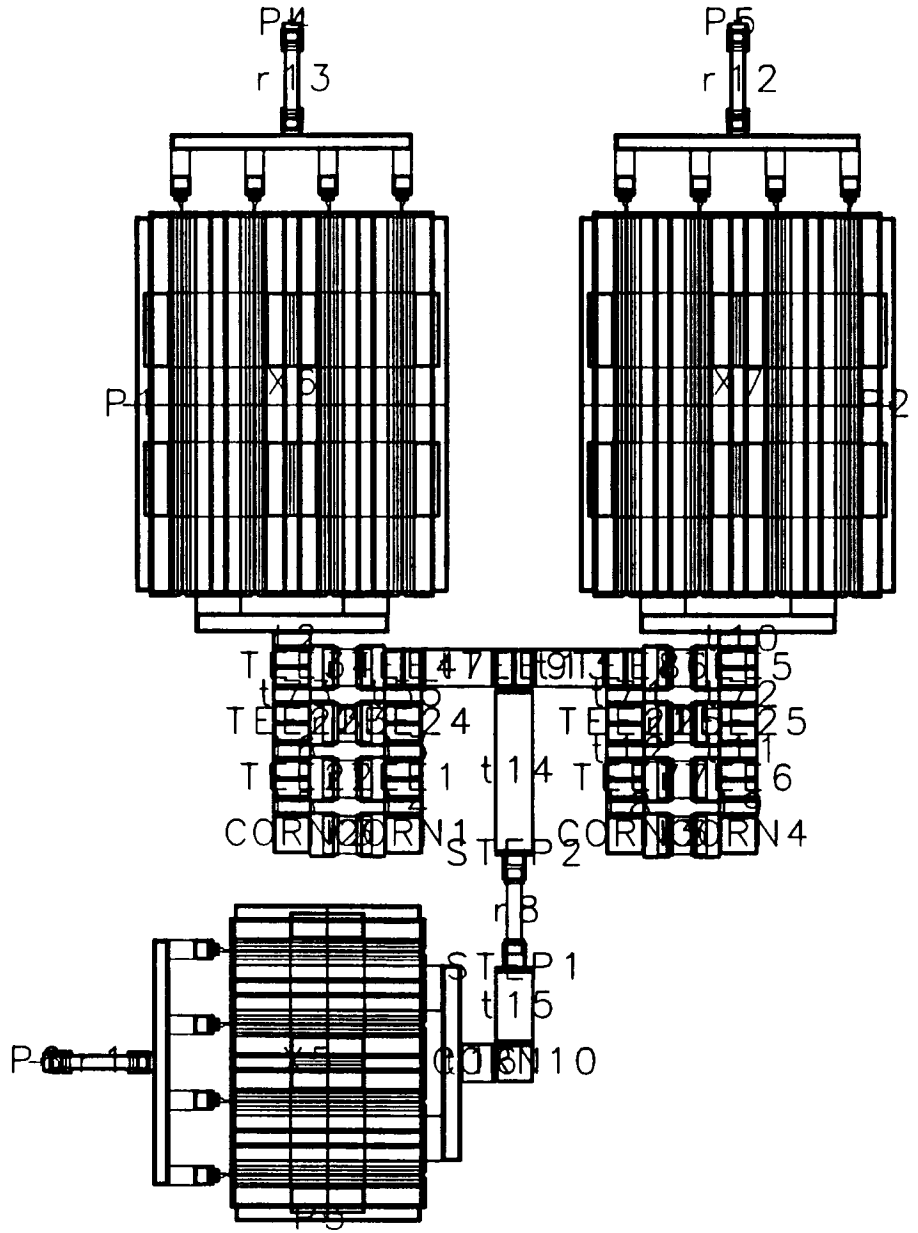
attn_prj_tb
S11
attn8_prj
S[1,1]
dB

ATTN 8_PRJ

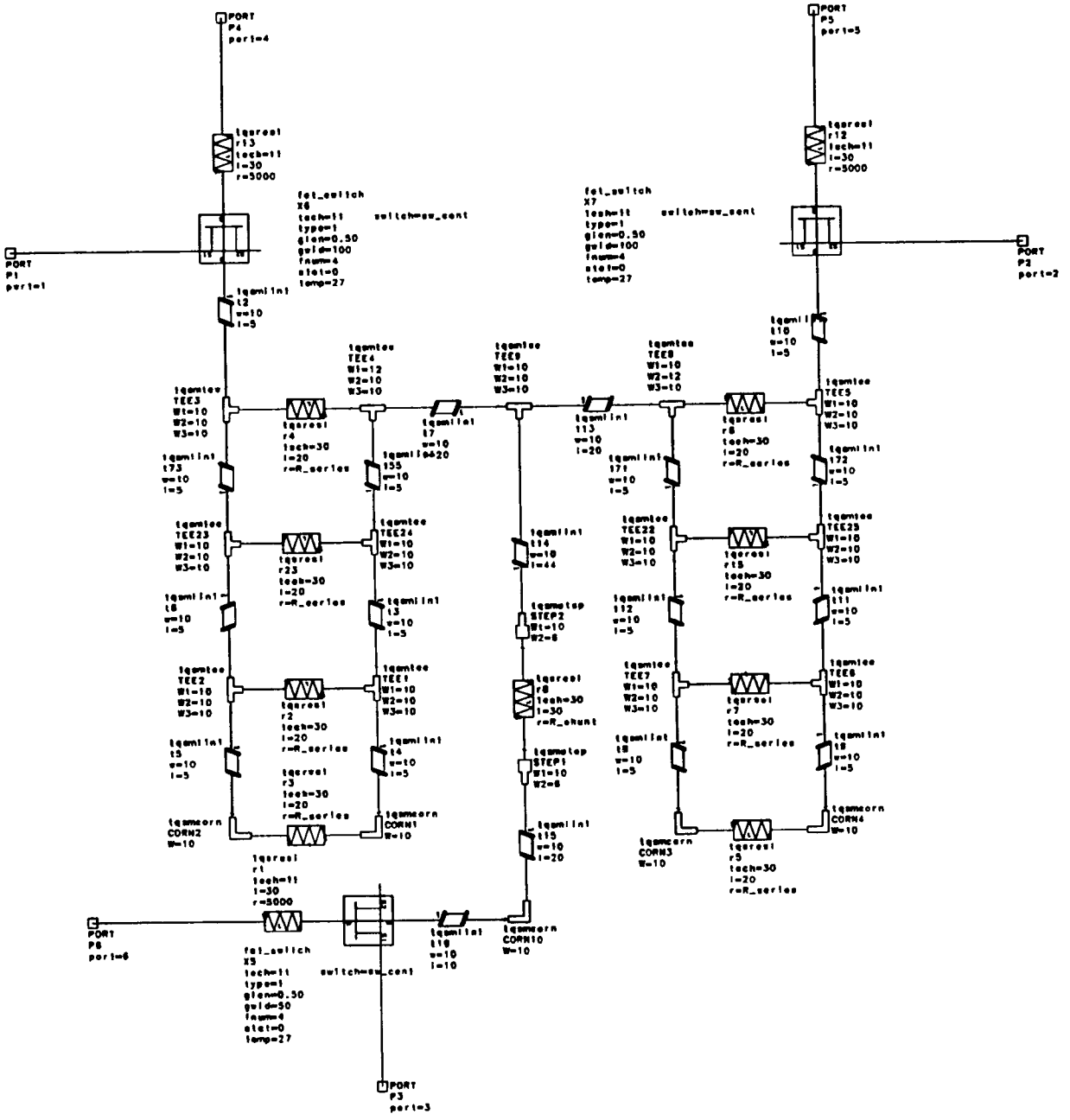


Reflection Coeffecient, Freq = 5.8 GHz
Thru = -36.7 dB
3 dB = -19.5 dB
7 dB = -20.5 dB

attn_3dB


P4
r13
P5
r12
X6
X7
P1
P2
t14
t15
r3
STEP2
STEP1
CORN1
CORN4
CORN10

attn - 3dB


PORT
P4
port=4
tqsreal
r13
tech=11
l=30
r=5000
fet_switch
X6
tech=11
type=1
glen=0.50
gwid=100
fnum=4
state=0
temp=27
switch=sw_cent
PORT
P1
port=1
tqsmlin
t2
w=10
l=5
tqsmtee
TEE4
W1=12
W2=10
W3=10
tqsmtee
TEE3
W1=10
W2=10
W3=10
tqsreal
r4
tech=30
l=20
r=R_series
tqsmlin
t55
w=10
l=5
tqsmlin
t73
w=10
l=5
tqsmlin
t7
w=10
l=20
tqsmtee
TEE9
W1=10
W2=10
W3=10
tqsmlin
t13
w=10
l=20
tqsmtee
TEE8
W1=10
W2=12
W3=10
tqsreal
r8
tech=30
l=20
r=R_series
tqsmtee
TEE5
W1=10
W2=10
W3=10
tqsmlin
t71
w=10
l=5
tqsmlin
t72
w=10
l=5
tqsmlin
t10
w=10
l=5
PORT
P5
port=5
tqsreal
r12
tech=11
l=30
r=5000
fet_switch
X7
tech=11
type=1
glen=0.50
gwid=100
fnum=4
state=0
temp=27
switch=sw_cent
PORT
P2
port=2
tqsmtee
TEE23
W1=10
W2=10
W3=10
tqsreal
r23
tech=30
l=20
r=R_series
tqsmtee
TEE24
W1=10
W2=10
W3=10
tqsmlin
t14
w=10
l=44
tqsmtee
TEE22
W1=10
W2=10
W3=10
tqsreal
r15
tech=30
l=20
r=R_series
tqsmtee
TEE25
W1=10
W2=10
W3=10
tqsmlin
t9
w=10
l=5
tqsmlin
t3
w=10
l=5
tqsmstep
STEP2
W1=10
W2=8
tqsmlin
t12
w=10
l=5
tqsmlin
t11
w=10
l=5
tqsmtee
TEE2
W1=10
W2=10
W3=10
tqsreal
r2
tech=30
l=20
r=R_series
tqsmtee
TEE1
W1=10
W2=10
W3=10
tqsreal
r9
tech=30
l=30
r=R_shunt
tqsmtee
TEE7
W1=10
W2=10
W3=10
tqsreal
r7
tech=30
l=20
r=R_series
tqsmtee
TEE6
W1=10
W2=10
W3=10
tqsmlin
t5
w=10
l=5
tqsmlin
t4
w=10
l=5
tqsmlin
t8
w=10
l=5
tqsmlin
t6
w=10
l=5
tqsreal
r3
tech=30
l=20
r=R_series
tqsmstep
STEP1
W1=10
W2=8
tqsmcorn
CORN2
W=10
tqsmcorn
CORN1
W=10
tqsmlin
t15
w=10
l=20
tqsmcorn
CORN3
W=10
tqsreal
r5
tech=30
l=20
r=R_series
tqsmcorn
CORN4
W=10
tqsreal
r1
tech=11
l=30
r=5000
PORT
P6
port=6
fet_switch
X5
tech=11
type=1
glen=0.50
gwid=50
fnum=4
state=0
temp=27
switch=sw_cent
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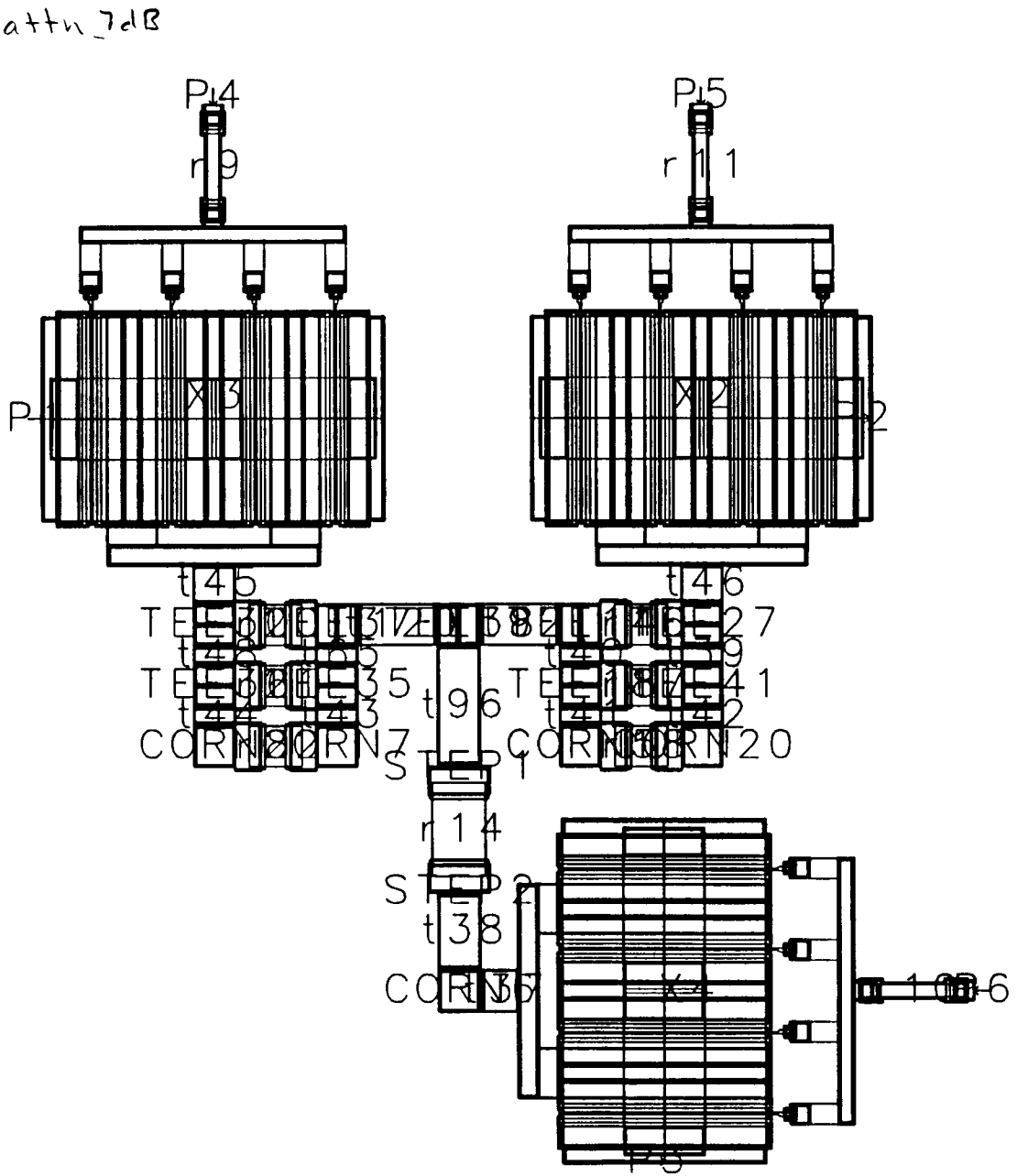
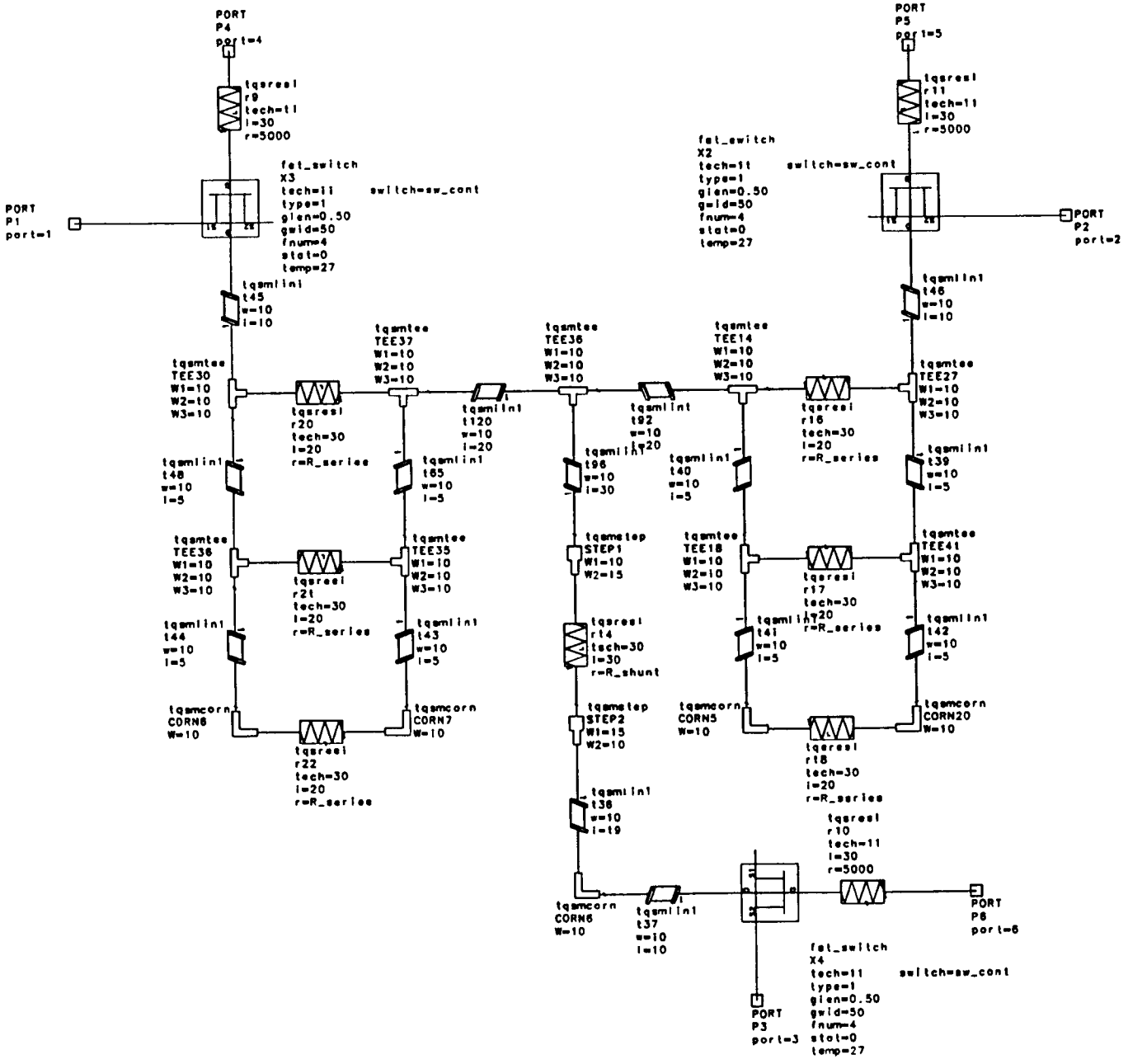
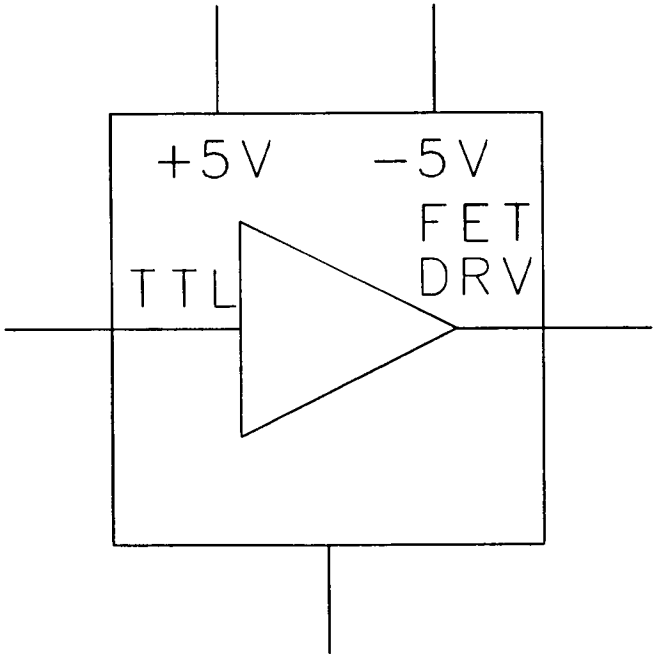
t10
w=10
l=10
tqsmcorn
CORN10
W=10
PORT
P3
port=3

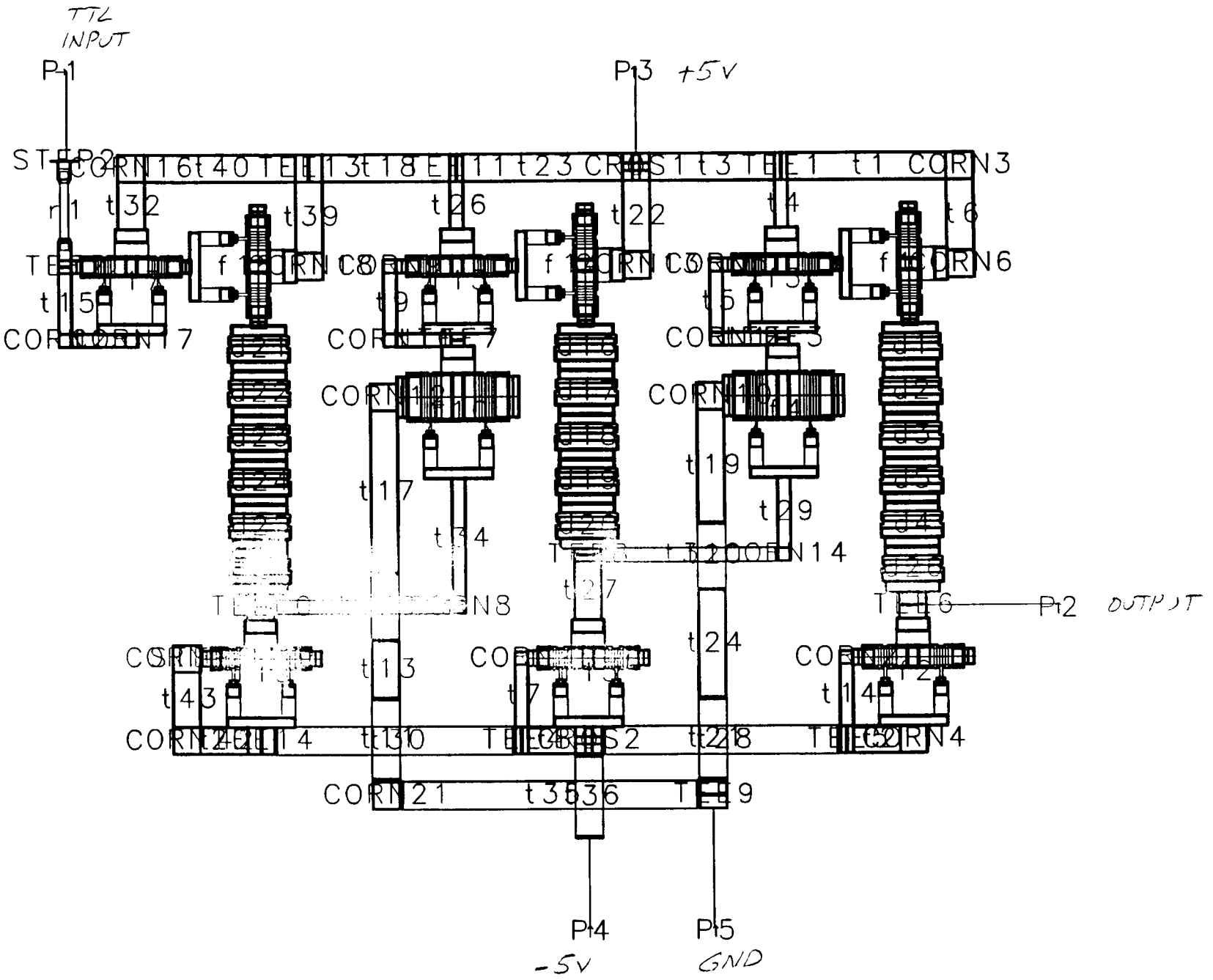

attn_7dB
P14
P15
r9
r11
X3
X2
t45
t46
t96
t38
X4

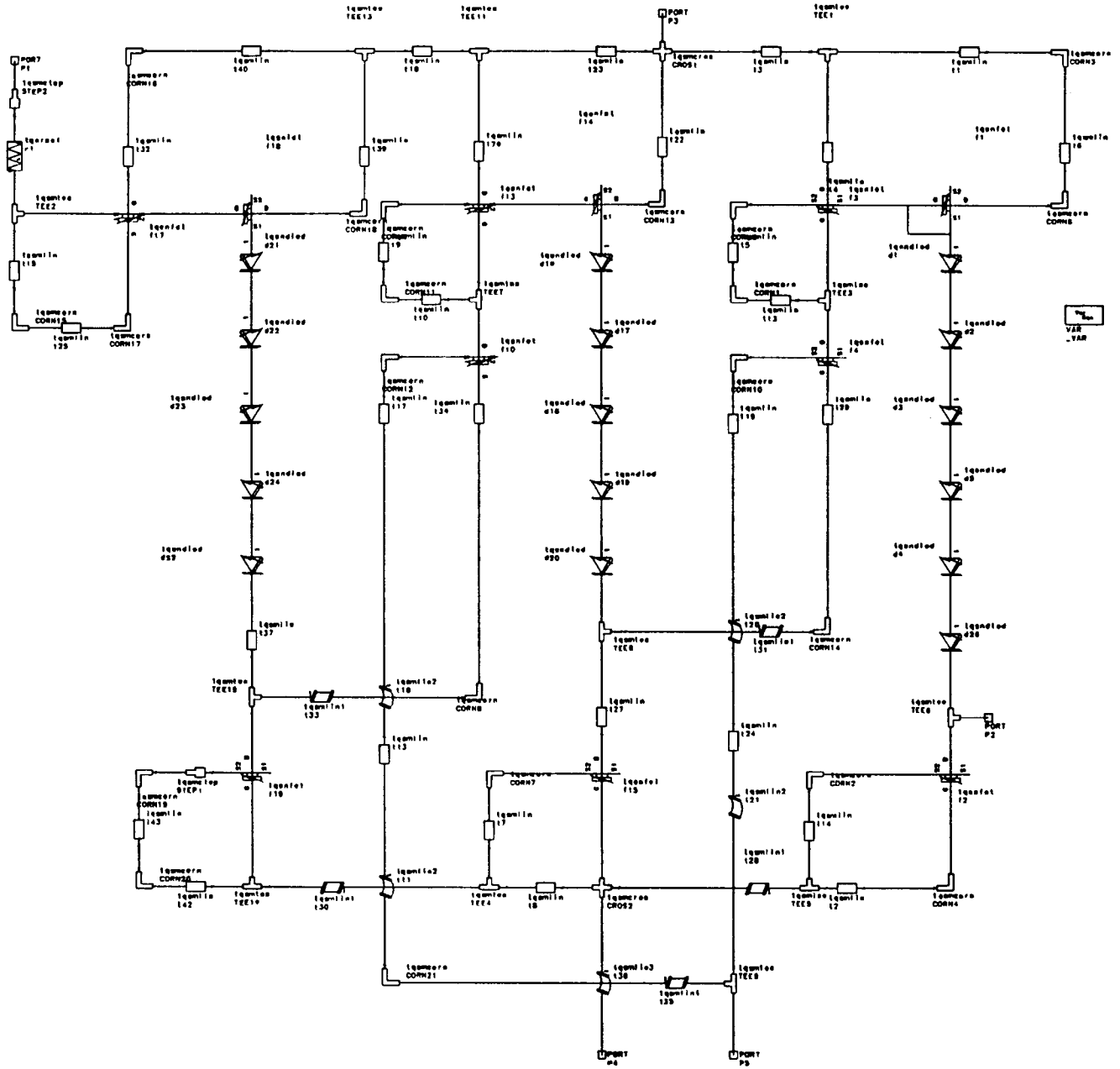
attn_7dB


PORT
P4
port=4
tqsresl
r9
tech=11
l=30
r=5000
fet_switch
X3
tech=11
type=1
glen=0.50
gwid=50
fnum=4
stat=0
temp=27
switch=sw_cont
PORT
P1
port=1
tqsmlinl
t45
w=10
l=10
tqsmtee
TEE30
W1=10
W2=10
W3=10
tqsresl
r20
tech=30
l=20
r=R_series
tqsmtee
TEE37
W1=10
W2=10
W3=10
tqsmlinl
t120
w=10
l=20
tqsmlinl
t48
w=10
l=5
tqsmlinl
t65
w=10
l=5
tqsmtee
TEE36
W1=10
W2=10
W3=10
tqsresl
r21
tech=30
l=20
r=R_series
tqsmtee
TEE35
W1=10
W2=10
W3=10
tqsmlinl
t44
w=10
l=5
tqsmlinl
t43
w=10
l=5
tqsmcorn
CORN8
W=10
tqsmcorn
CORN7
W=10
tqsresl
r22
tech=30
l=20
r=R_series
tqsmtee
TEE36
W1=10
W2=10
W3=10
tqsmlinl
t96
w=10
l=30
tqsmstep
STEP1
W1=10
W2=15
tqsresl
rt4
tech=30
l=30
r=R_shunt
tqsmstep
STEP2
W1=15
W2=10
tqsmlinl
t36
w=10
l=t9
tqsmcorn
CORN6
W=10
tqsmlinl
t37
w=10
l=10
tqsmlinl
t92
w=10
l=t20
tqsmtee
TEE14
W1=10
W2=10
W3=10
tqsmlinl
t40
w=10
l=5
tqsmtee
TEE18
W1=10
W2=10
W3=10
tqsmlinl
t41
w=10
l=5
tqsmcorn
CORN5
W=10
tqsresl
r16
tech=30
l=20
r=R_series
tqsresl
r17
tech=30
l=t20
r=R_series
tqsresl
rt8
tech=30
l=20
r=R_series
PORT
P5
port=5
tqsresl
r11
tech=11
l=30
r=5000
fet_switch
X2
tech=11
type=1
glen=0.50
gwid=50
fnum=4
stat=0
temp=27
switch=sw_cont
PORT
P2
port=2
tqsmlinl
t46
w=10
l=10
tqsmtee
TEE27
W1=10
W2=10
W3=10
tqsmlinl
t39
w=10
l=5
tqsmtee
TEE41
W1=10
W2=10
W3=10
tqsmlinl
t42
w=10
l=5
tqsmcorn
CORN20
W=10
tqsresl
r10
tech=11
l=30
r=5000
PORT
P6
port=6
fet_switch
X4
tech=11
type=1
glen=0.50
gwid=50
fnum=4
stat=0
temp=27
switch=sw_cont
PORT
P3
port=3

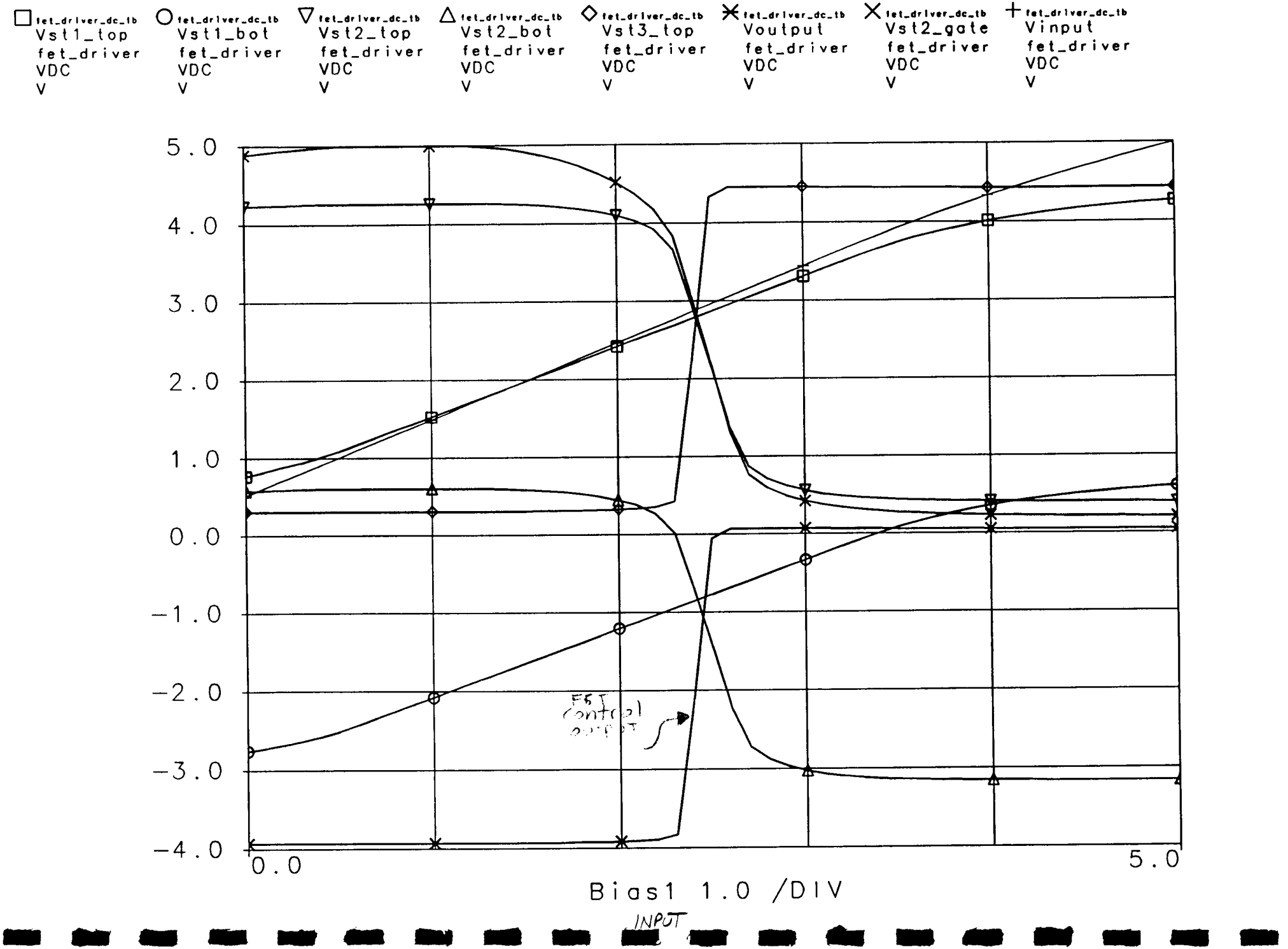


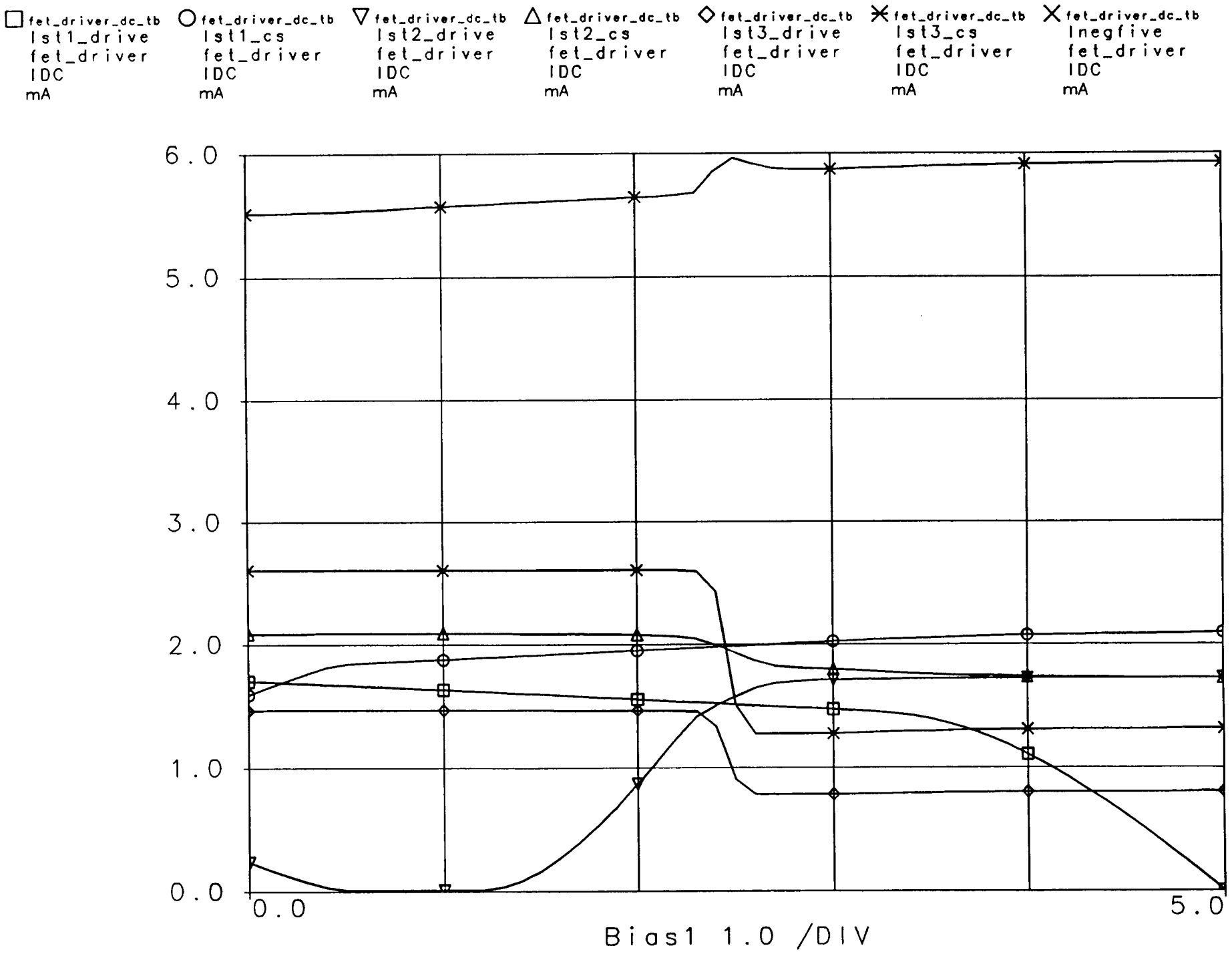
TTL IN	FET OUT
0 V	-4V
5 V	0 V

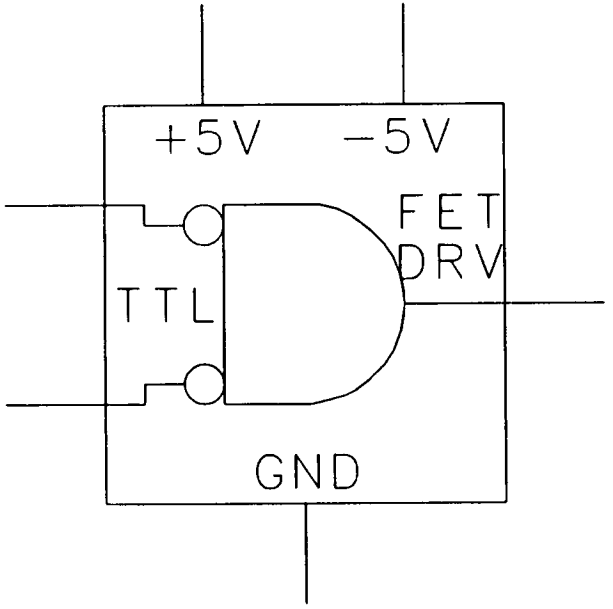

TTL
INPUT
P1
P3 +5V
P2 OUTPUT
P4
-5V
P5
GND



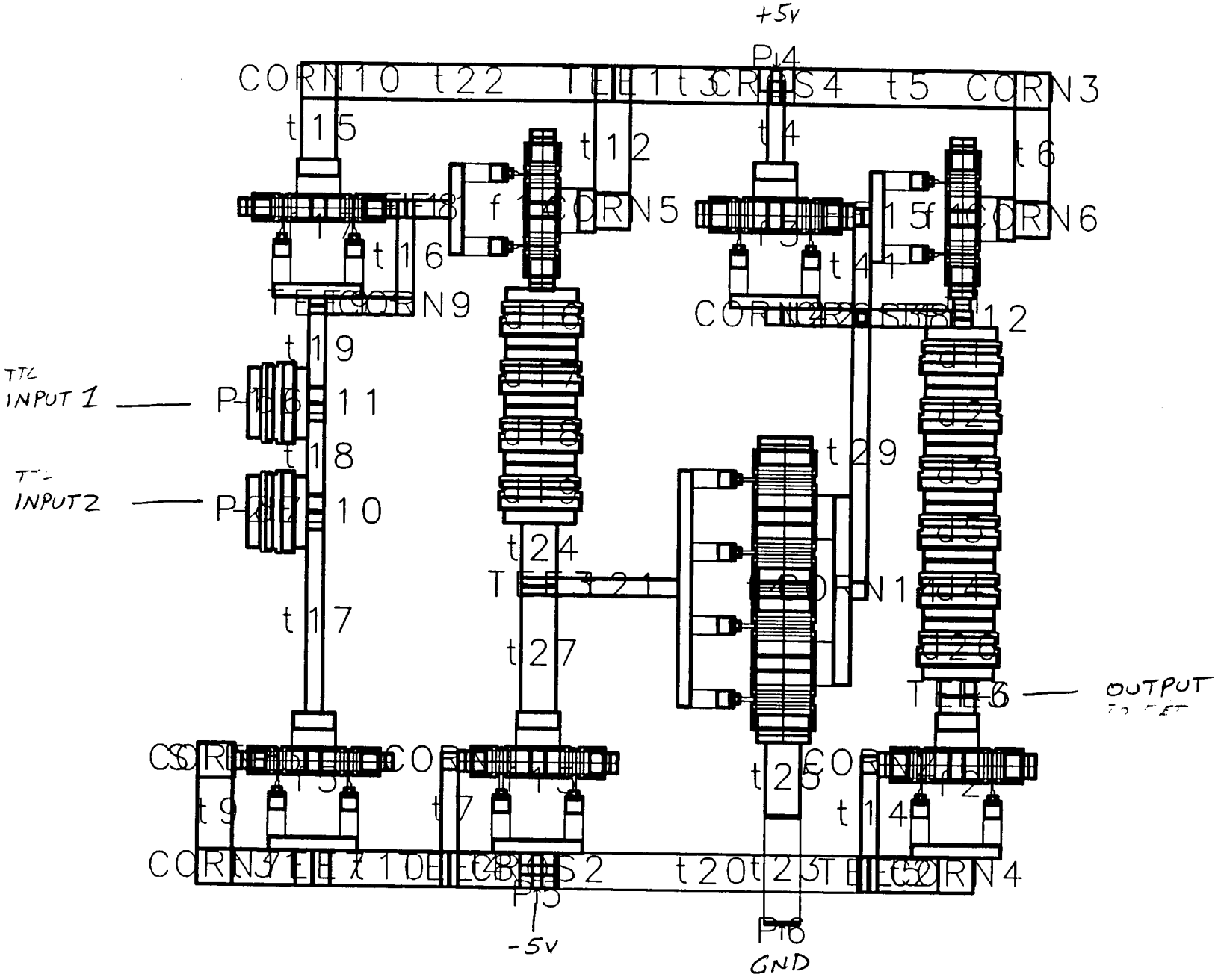
12/7/95

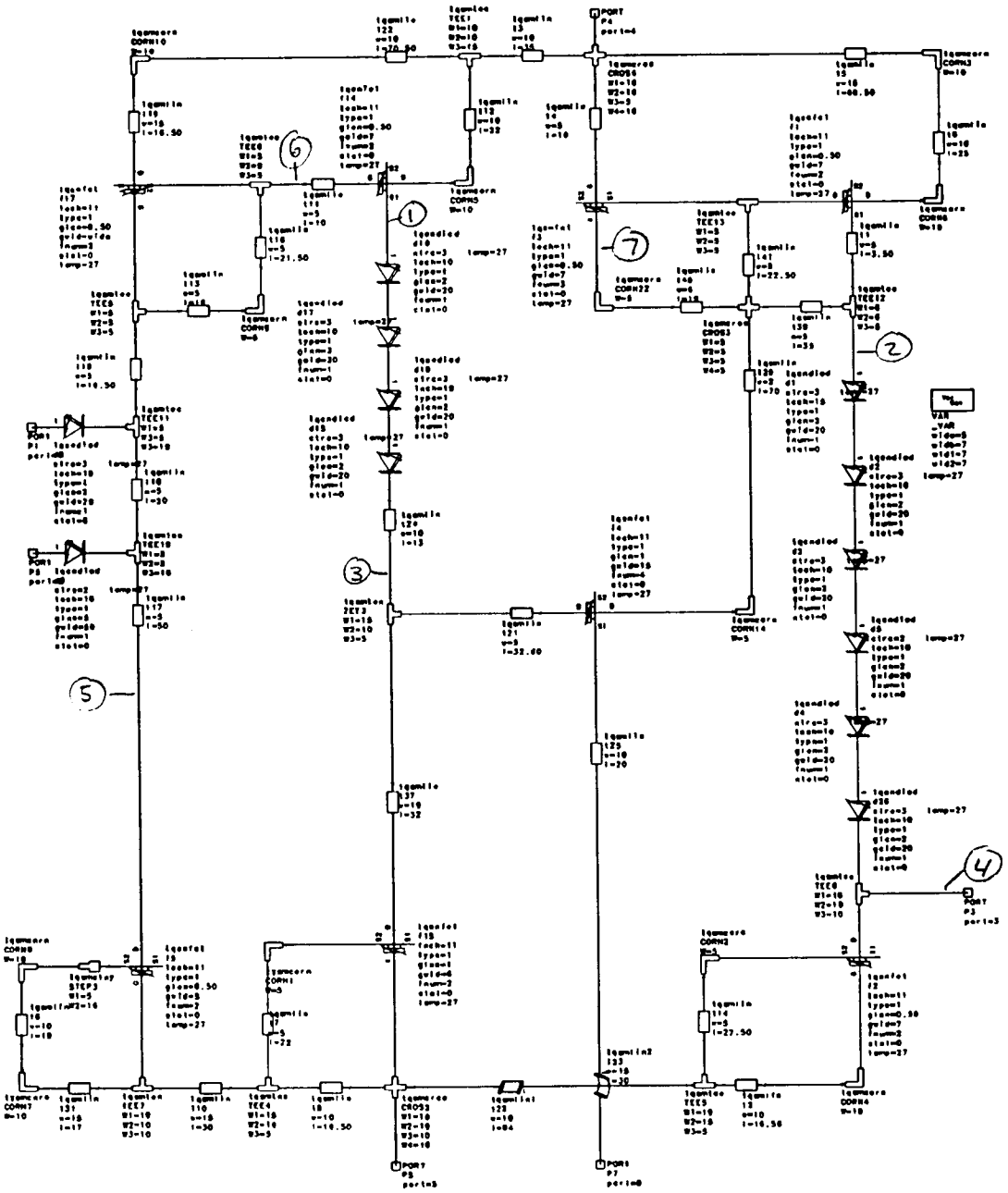

fet_driver_dc_tb Vst1_top fet_driver VDC V
fet_driver_dc_tb Vst1_bot fet_driver VDC V
fet_driver_dc_tb Vst2_top fet_driver VDC V
fet_driver_dc_tb Vst2_bot fet_driver VDC V
fet_driver_dc_tb Vst3_top fet_driver VDC V
fet_driver_dc_tb Voutput fet_driver VDC V
fet_driver_dc_tb Vst2_gate fet_driver VDC V
fet_driver_dc_tb Vinput fet_driver VDC V
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
-4.0
0.0
5.0
Bias1 1.0 /DIV
FSI control output
INPUT

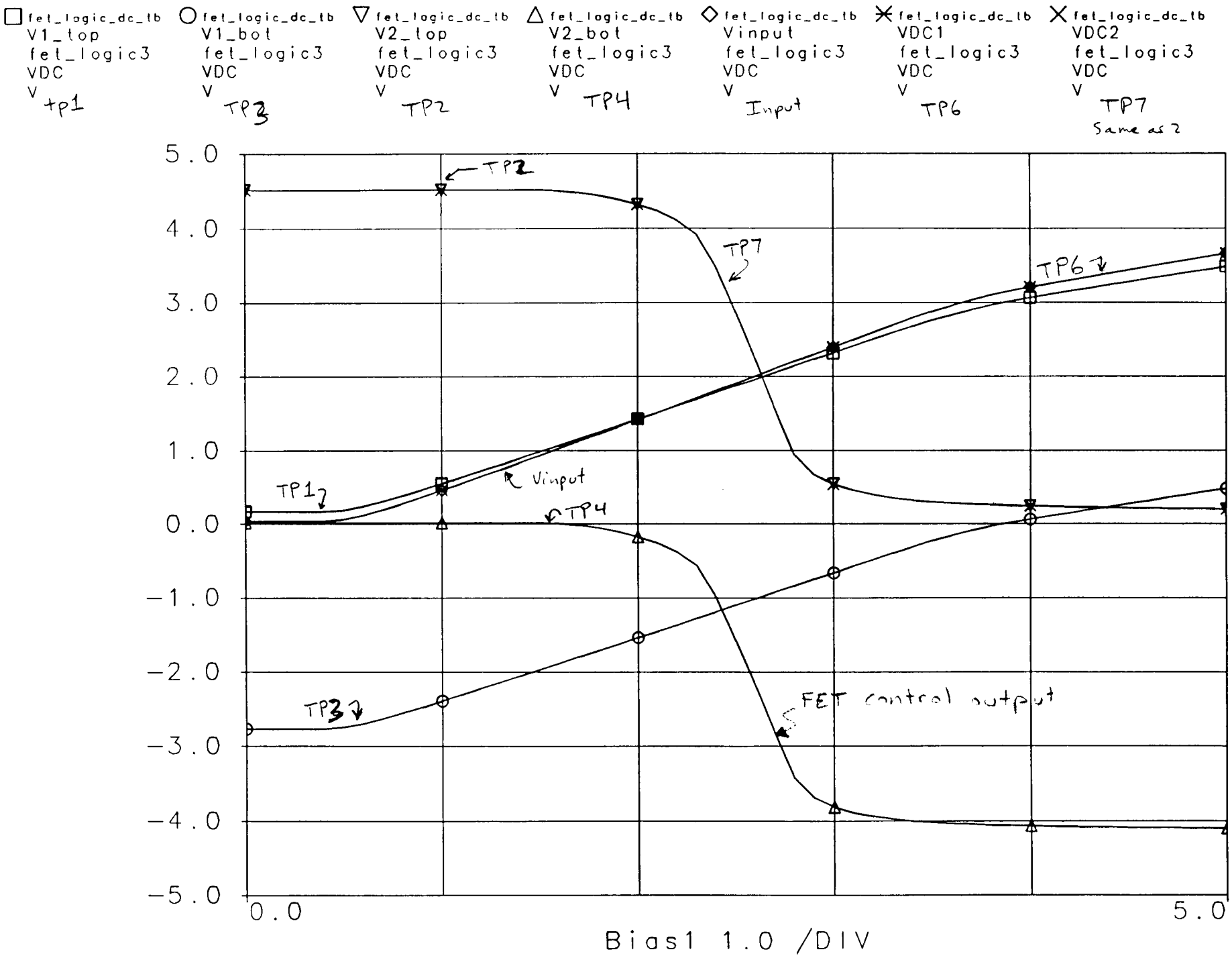

fet_driver_dc_tb
Ist1_drive
fet_driver
IDC
mA
fet_driver_dc_tb
Ist1_cs
fet_driver
IDC
mA
fet_driver_dc_tb
Ist2_drive
fet_driver
IDC
mA
fet_driver_dc_tb
Ist2_cs
fet_driver
IDC
mA
fet_driver_dc_tb
Ist3_drive
fet_driver
IDC
mA
fet_driver_dc_tb
Ist3_cs
fet_driver
IDC
mA
fet_driver_dc_tb
Inegfive
fet_driver
IDC
mA
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0.0
5.0
Bias1 1.0 /DIV

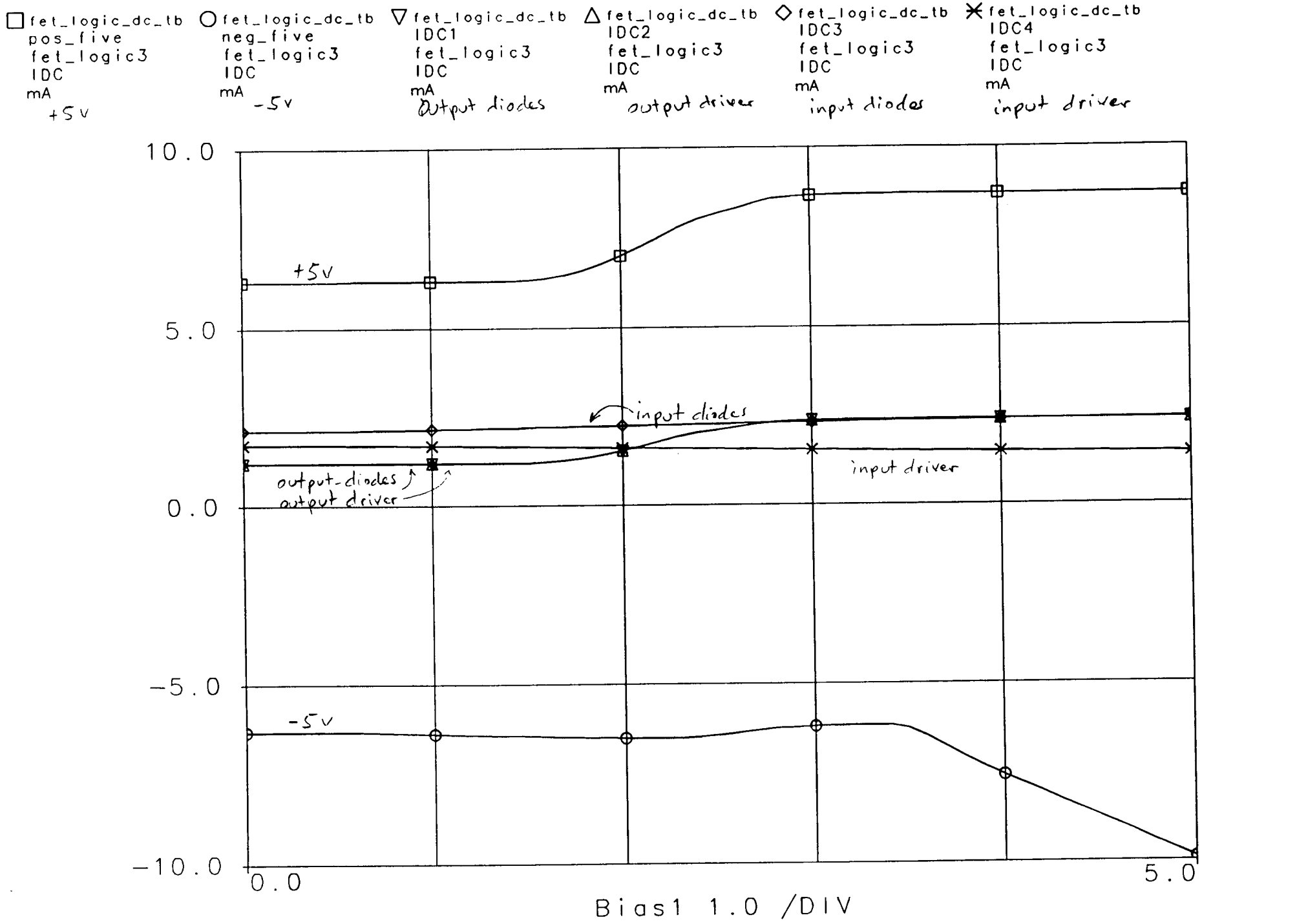


TTL		FET
IN1	IN2	OUT
0	0	0
0	5v	-4v
5v	0	-4v
5v	5v	-4v


+5v
P14
CORN10
t22
TEE1
t3
CRAS4
t5
CORN3
t15
t12
t4
t6
CORN5
CORN6
t16
t11
CORN9
CORN12
t19
TTL
INPUT 1
P16
11
t18
TTL
INPUT2
P15
10
t24
t29
t21
CORN1
t17
t27
OUTPUT
TEE6
CORN7
CORN8
t25
t9
t7
t14
CORN11
CORN4
t10
CRAS2
t20
t23
TEE2
P13
-5v
P16
GND


1
2
3
4
5
6
7


fet_logic_dc_tb V1_top fet_logic3 VDC V
fet_logic_dc_tb V1_bot fet_logic3 VDC V
fet_logic_dc_tb V2_top fet_logic3 VDC V
fet_logic_dc_tb V2_bot fet_logic3 VDC V
fet_logic_dc_tb Vinput fet_logic3 VDC V
fet_logic_dc_tb VDC1 fet_logic3 VDC V
fet_logic_dc_tb VDC2 fet_logic3 VDC V
tp1
TP3
TP2
TP4
Input
TP6
TP7
Same as 2
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
TP2
TP7
TP6
TP1
Vinput
TP4
TP3
FET control output
0.0
5.0
Bias1 1.0 /DIV


fet_logic_dc_tb
pos_five
fet_logic3
IDC
mA
+5v
fet_logic_dc_tb
neg_five
fet_logic3
IDC
mA
-5v
fet_logic_dc_tb
IDC1
fet_logic3
IDC
mA
output diodes
fet_logic_dc_tb
IDC2
fet_logic3
IDC
mA
output driver
fet_logic_dc_tb
IDC3
fet_logic3
IDC
mA
input diodes
fet_logic_dc_tb
IDC4
fet_logic3
IDC
mA
input driver
10.0
5.0
0.0
-5.0
-10.0
+5v
input diodes
output diodes
output driver
input driver
-5v
0.0
5.0
Bias1 1.0 /DIV

A

5.8 GHz ISM-BAND LOW NOISE AMPLIFIER

EE 525.787

MMIC DESIGN

FALL 1995

CRAIG FROST
DECEMBER 11, 1995

5.8 GHz ISM-BAND LOW NOISE AMPLIFIER

I. Abstract

A GaAs MMIC low noise amplifier was designed for the 5.8 GHz ISM band. It consists of two stages, employs on-chip input and output matching networks and series feedback to achieve both a low noise match and conjugate input match. The simulations show a 2.5 dB noise figure, 18 dB gain, and less than 1.2:1 input VSWR over the 5.725-5.875 GHz passband. Also, a 5.8 GHz bandpass filter is included on the chip. It is independent of the amplifier and has its own input and output. The filter is a three-section all-pole design.

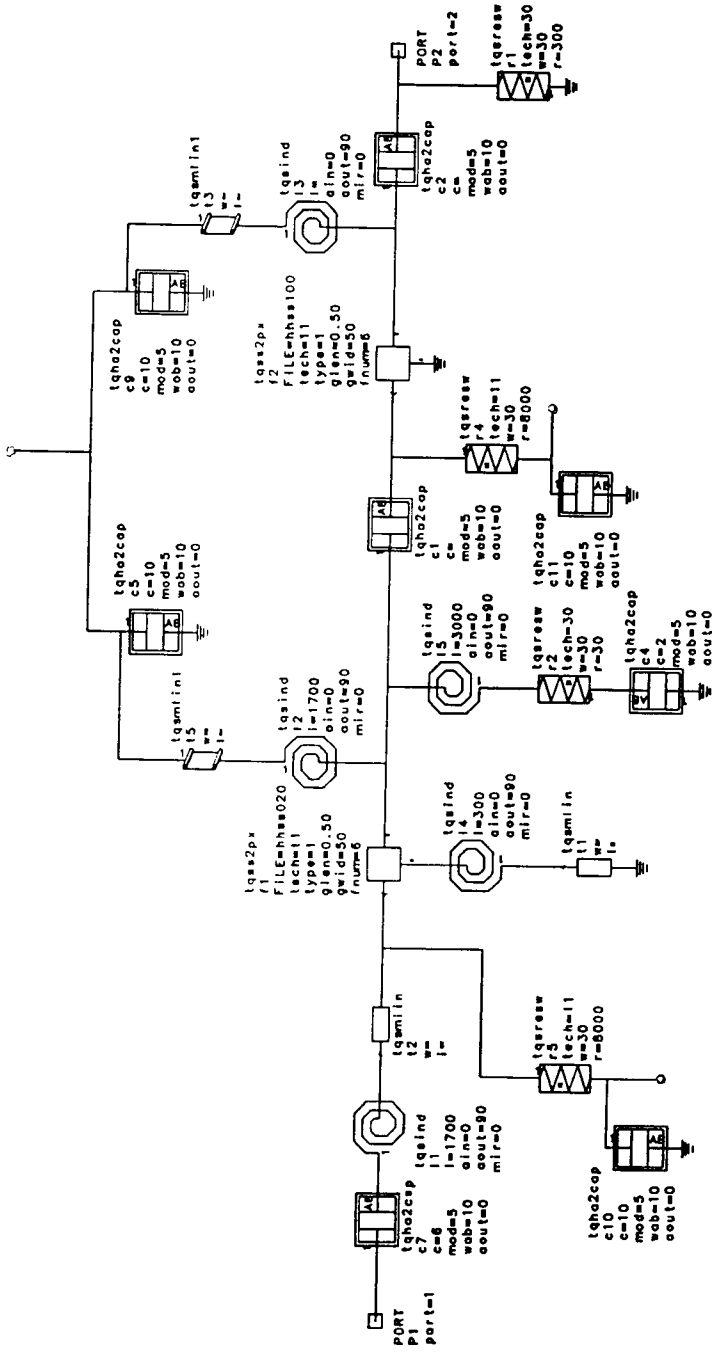
II. Introduction

A. Circuit Description

The MMIC was designed for Triquint's HA2 process using EESof's Series IV, Version 6.0. The amplifier consists of two cascaded FETs. Each is a 50 x 6 μm, 0.5 μm gate length depletion implant MESFET. The second FET is in the common-source configuration and is biased at 100% I_{DSS} for maximum gain. For this device geometry, I_{DSS} is about 45 mA. The first FET is biased at 20% I_{DSS} for lowest noise and has its source connected to ground through approximately 300 pH of inductance. This source inductance creates series feedback which has the effect of moving Z_{opt}, the source impedance for optimum noise match, in a roughly circular counterclockwise direction on the Smith chart [1]. With the right amount of source inductance, Z_{opt} can equal S_{11}*, the conjugate match of the FET's input impedance [2]. Then when the FET is conjugately matched at its input, it is matched for both lowest noise figure and lowest input VSWR. This was done to the first FET in the cascade.

A simplified circuit topology is shown in the schematic on the next page. Following the first stage, an interstage matching network connects the two FETs. It is made of a shunt inductor and a series capacitor. The match is intended to be a compromise between gain and noise figure in the second FET. The final output match consists of shunt inductor and a series capacitor, and is a conjugate match for good output VSWR.

For stability, shunt resistors are used at two locations. At the output (drain) of the first FET, a series RLC network is connected to ground. The reason for the inductor and capacitor is to provide an extra low impedance path to ground at about 3 GHz, since the circuit was more unstable at that frequency. The resistor value is small, 30 Ω, the inductor is large, 3000 pH, and the overall effect is to help stabilize the circuit without greatly affecting the 5.725-5.875 GHz passband. The second shunt resistor is located at the final output, after the series capacitor. This is a 300 Ω resistor. The overall circuit is unconditionally stable, and each individual part of the cascade is also unconditionally stable.


PORT
P2
port=2
tqsresw
r1
tech=30
w=30
r=300
tqsmlin
l3
w=
l=
tqsind
l3
l=
qin=0
qout=90
mir=0
tqsh2cap
c2
c=
mod=5
wob=10
qout=0
tqsh2cap
c9
c=10
mod=5
wob=10
qout=0
tqss2px
f2
FILE=hhss100
tech=11
type=1
glen=0.50
gwid=50
fnum=6
tqsresw
r4
tech=11
w=30
r=8000
tqsh2cap
c1
c=
mod=5
wob=10
qout=0
tqsh2cap
c5
c=10
mod=5
wob=10
qout=0
tqsh2cap
c11
c=10
mod=5
wob=10
qout=0
tqsind
l5
l=3000
qin=0
qout=90
mir=0
tqsresw
r2
tech=30
w=30
r=30
tqsh2cap
c4
c=2
mod=5
wob=10
qout=0
tqsmlin
l5
w=
l=
tqsind
l2
l=1700
qin=0
qout=90
mir=0
tqss2px
f1
FILE=hhss020
tech=11
type=1
glen=0.50
gwid=50
fnum=6
tqsind
l4
l=300
qin=0
qout=90
mir=0
tqsmlin
l1
w=
l=
tqsmlin
l2
w=
l=
tqsresw
r3
tech=11
w=30
r=8000
tqsind
l1
l=1700
qin=0
qout=90
mir=0
tqsh2cap
c7
c=8
mod=5
wob=10
qout=0
tqsh2cap
c10
c=10
mod=5
wob=10
qout=0
PORT
P1
port=1

The biasing scheme is uses a positive and negative supply. The gates require two negative voltages, V_{G1} and V_{G2}. Since FET 2 is to be biased at 100% I_{DSS}, V_{G2} will normally be 0 V. However the signal V_{G2} is brought to a bonding pad so that the value can be changed and experimented with. The gate bias voltage for FET 1, V_{G1}, is also brought to a pad and will normally be about -1.0 V, but it can be varied to check the effect on noise figure. The drains are tied together and brought to a bonding pad. The drain bias voltage, V_D, should normally be about 2.5 V. Ten picofarad power supply bypass capacitors are included on all three bias lines at the node where they enter the chip.

B. Design Philosophy

This MMIC was designed with learning and experimentation in mind. This is why the two or three bias voltages are required rather than using one supply and on-chip bias networks. Thus, experiments can be performed including measuring noise figure and gain versus V_{G1}, V_{G2}, V_D, and I_D. It is expected that noise figure and gain do not vary greatly with V_D. How low can V_D be while still giving adequate performance? Lowering V_D will lower the power consumption by the same percentage. This philosophy is also the reason for adding the bandpass filter. After the LNA was finished, space was left over on the chip. The filter was added to see what the loss will be with the new Triquint HA2 airbridge inductors, and also to see how far off the passband frequency is.

C. Tradeoffs

One LNA topology that was investigated was the cascode amplifier. The first FET would be a common-source stage biased at 20% I_{DSS} and the second FET would be a common-gate stage also biased at 20% I_{DSS}. The advantage over two common-source stages is that the two cascode FETs share the same bias current. Thus the total current draw would be only about 9 mA instead of 54 mA. The drain voltage, though, would have to be 5 V instead of 2.5 V (each FET would have a 2.5 V drop across the channel), making the power consumption 45 mW for the cascode versus 135 mW for the common-source version. Cascode amplifiers are desirable for low-power applications.

The major drawbacks of the cascode LNA were lack of gain and poor output match. The gain achieved after stabilizing the network was about 12 dB. To meet the 15 dB requirement, another stage would have to be added, increasing the complexity and power consumption. Also, the output impedance of the cascode is high. The match to 50 Ω creates a high Q network. The match was not good over the full 150 MHz band. The sharp output return loss null also indicates that it will be susceptible to matching network component value errors. Since the MIM capacitors cannot be produced to precise values, the match would likely be off in frequency. For these reasons the cascode approach was ruled out for this project.

III. Modeled Performance

A. Specification Compliance Matrix

The given specifications for the LNA as well as the predicted performance is shown below. Note that the simulations were performed with the Triquint Smart Library HA1 inductors. The new inductors have thicker airbridge metal and should have lower loss. Thus these predictions can be considered conservative.

Parameter	Requirement	Goal	Predicted
Frequency [GHz]	5.725-5.875	Same	5.725-5.875
Bandwidth	>150 MHz	Same	> 150 MHz
Gain	> 15 dB	20 dB	> 17.6 dB
Gain Variation	< 1 dB	Same	< .9 dB
Noise Figure	< 4 dB	< 3 dB	< 2.52 dB
Input IP3	> -10 dBm	Same	+ 2 dBm *
VSWR, 50 Ω	< 1.5:1, In/Out	Same	<1.18:1 In, 1.3:1 Out
Supply Voltage	± 5 V	+ 5 V only	± 5 V
Size	60 x 60 mil	Same	60 x 60 mil

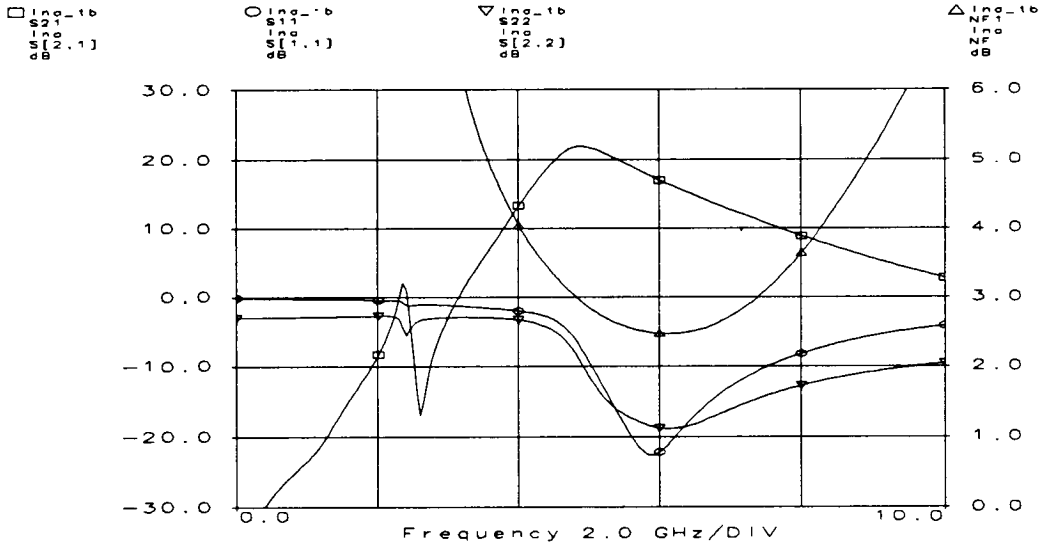
* The input IP3 was estimated from 1 dB compression simulation results at 5.8 GHz. The input power at 1 dB gain compression is -8 dBm, and the third order intercept is typically 10 dB higher the 1 dB compression.

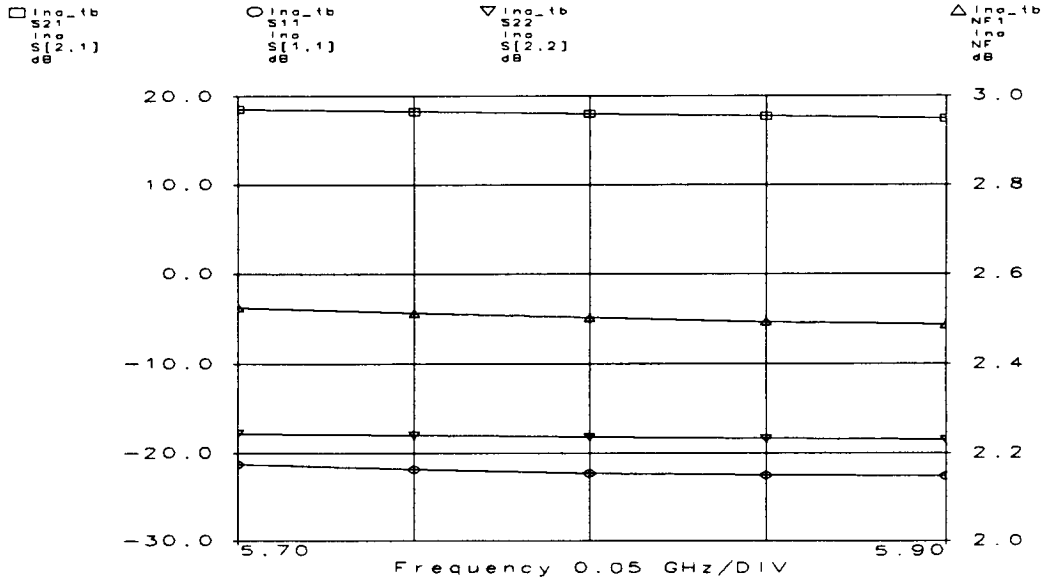
B. Predicted Performance

Additional predicted performance parameters are shown below for the LNA.

LNA Parameters	Predicted
Reverse Isolation	>34 dB (0-12 GHz)
<3 dB Noise Figure Bandwidth	4.81-7.41 GHz (2.6 GHz)
>15 dB Gain Bandwidth	4.16-6.41 GHz (2.25 GHz)
<1.5:1 Input VSWR Bandwidth	5.26-6.86 GHz (1.6 GHz)
<1.5:1 Output VSWR Bandwidth	5.16-7.61 GHz (2.45 GHz)
Voltages, Current	54 mA @ 2.5 V, < 10 μA @ -1 V
Power Consumption	135 mW

The following two plots show the LNA gain, input and output return loss, and noise figure from DC to 10 GHz and from 5.7 to 5.9 GHz.

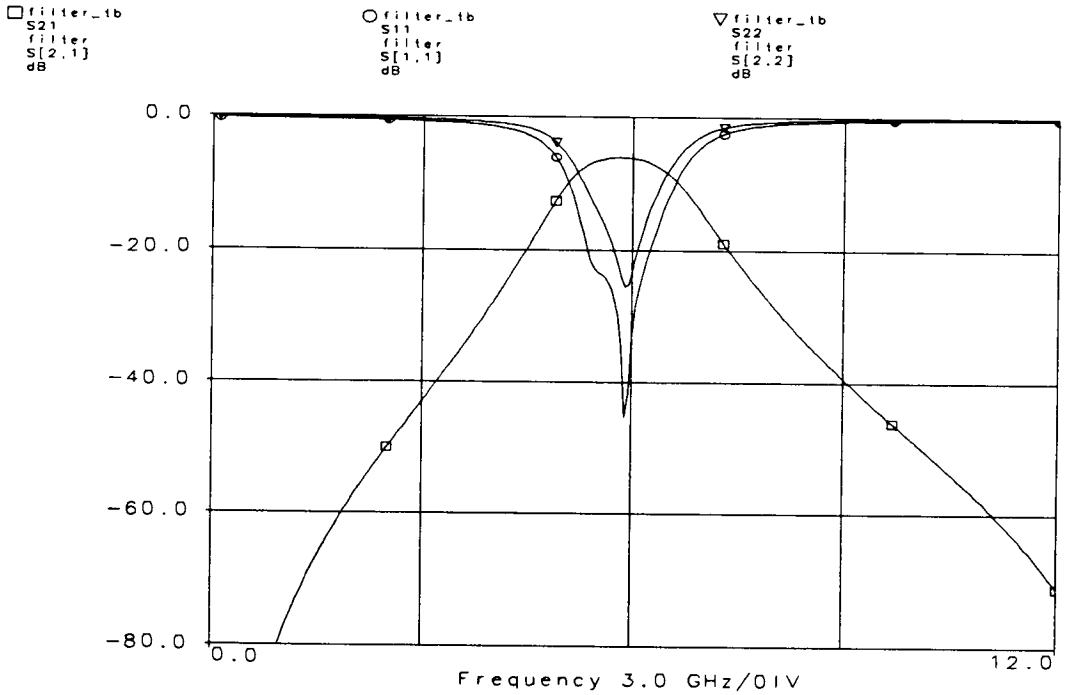


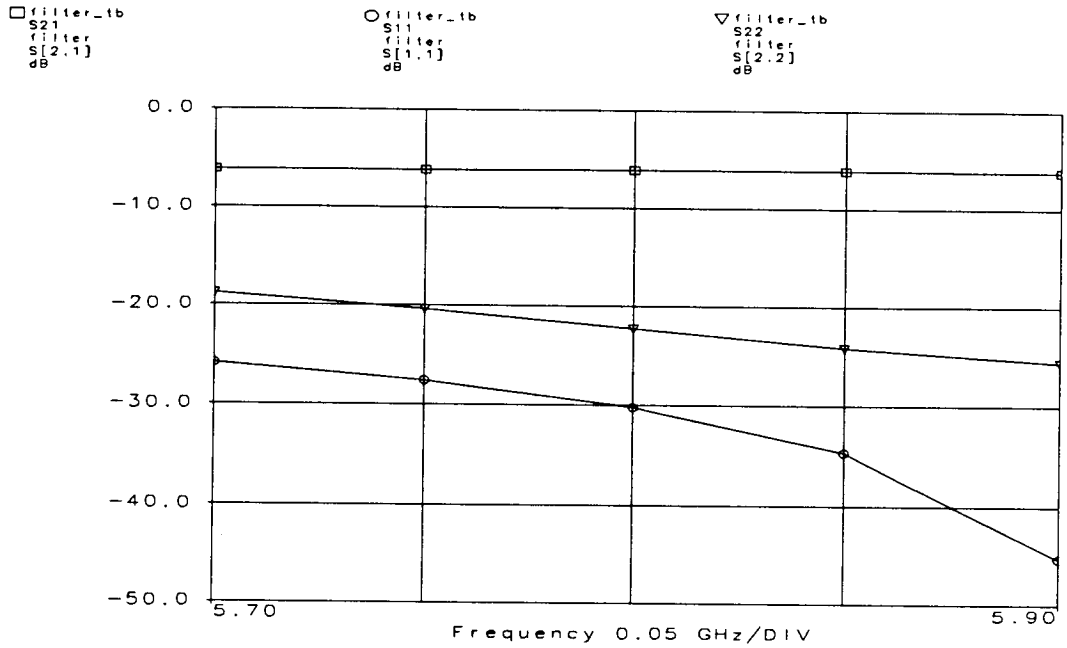


Predicted performance parameters are shown below for the bandpass filter. Note that no specifications were given for the bandpass filter.

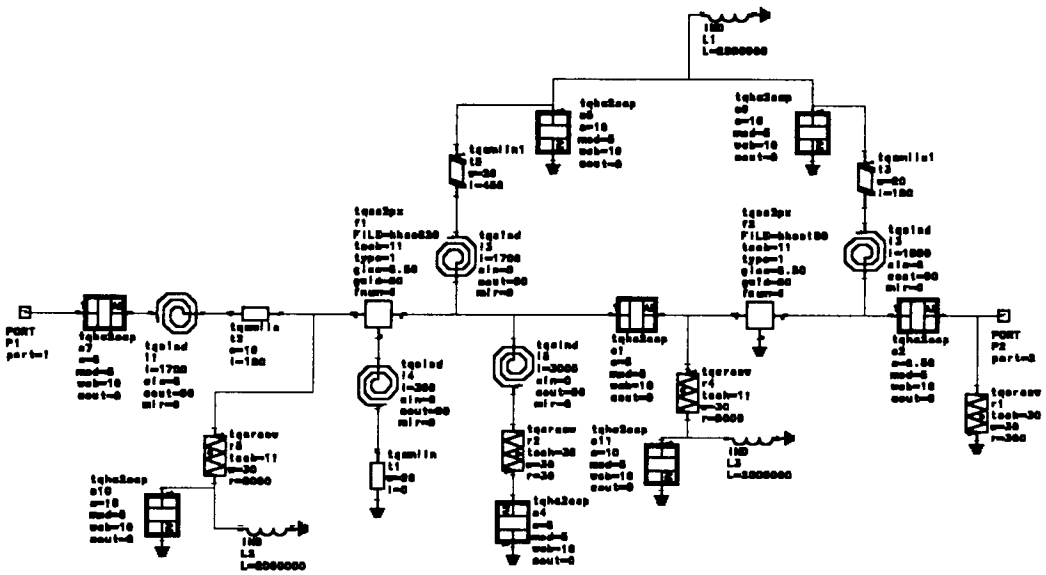
Bandpass Filter Parameters	Predicted
Center Frequency	5.8 GHz
3 dB Bandwidth	1.45 GHz
Midband Insertion Loss	6.2 dB
50 dB Bandwidth	8.65 GHz
Return Loss over 5.7-5.9 GHz	> 25 dB In, > 18 dB Out

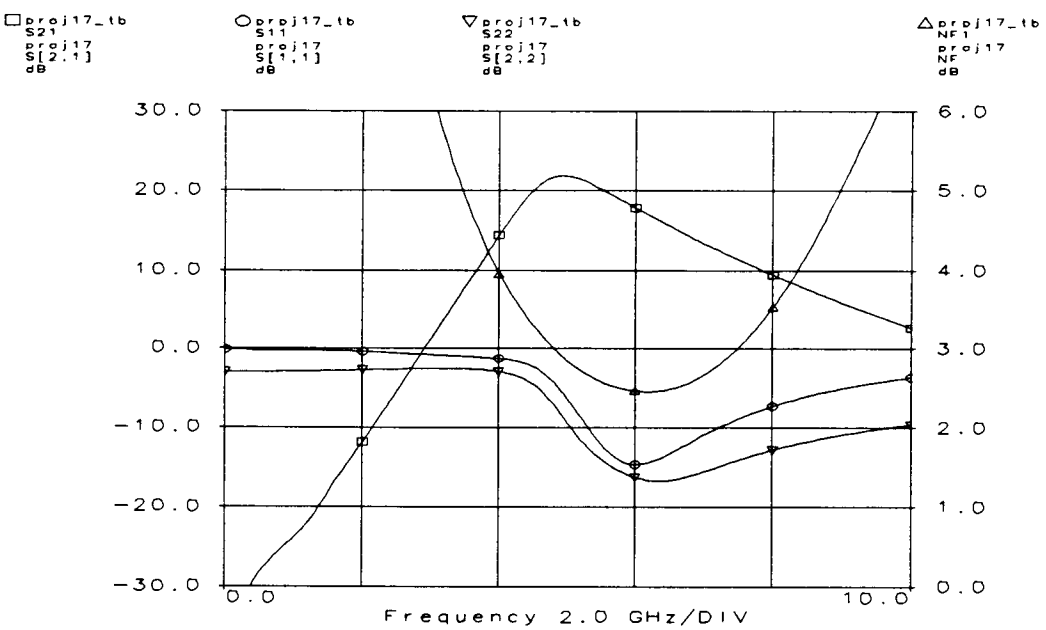
The following two plots show the bandpass filter insertion loss and input and output return loss from DC to 12 GHz and from 5.7 to 5.9 GHz.



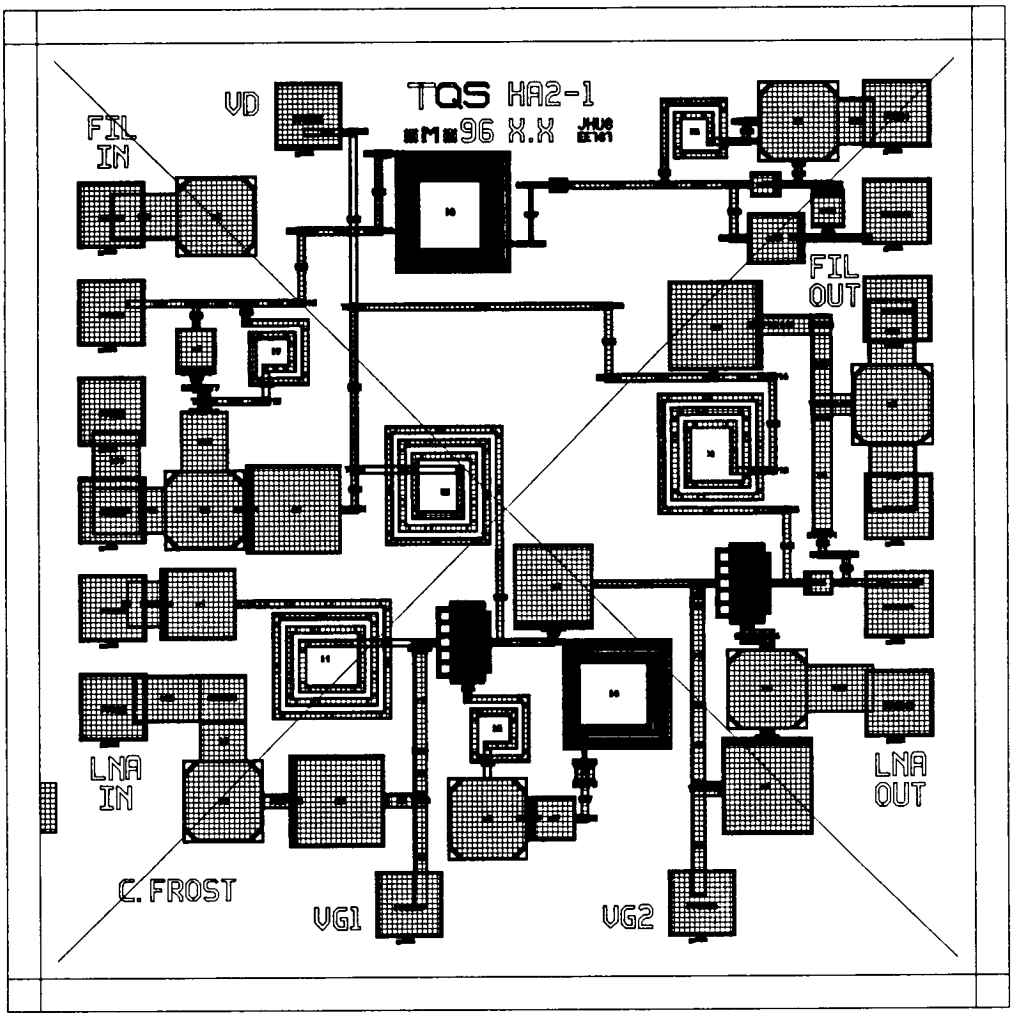

filter_tb
S21
filter
S[2,1]
dB
filter_tb
S11
filter
S[1,1]
dB
filter_tb
S22
filter
S[2,2]
dB
0.0
-10.0
-20.0
-30.0
-40.0
-50.0
5.70
5.90
Frequency 0.05 GHz/DIV

Prior to the layout, the LNA schematic and simulated performance were as follows. The performance plot indicates that there are no significant differences between pre- and post-layout simulations.





The final layout is shown below.

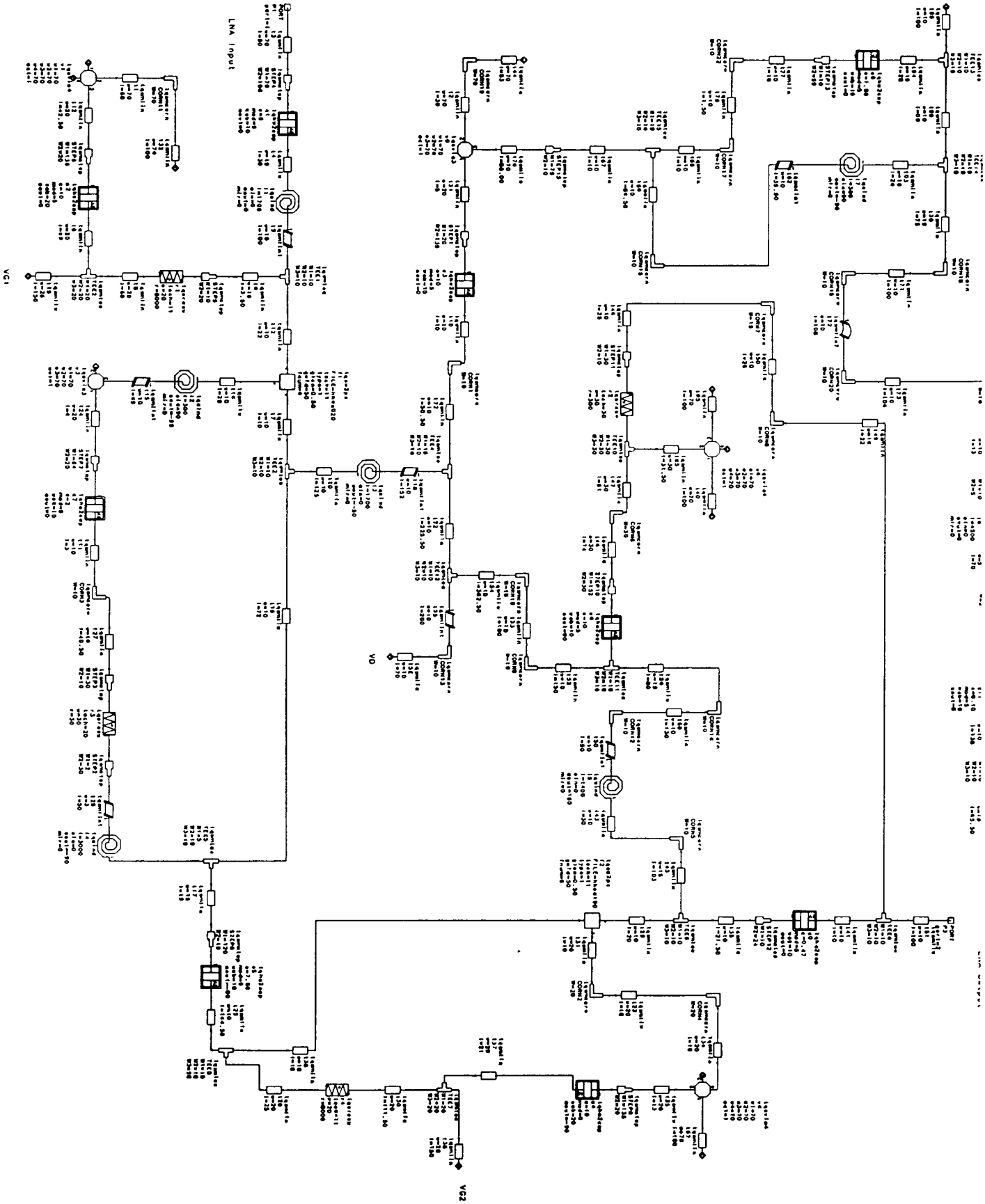


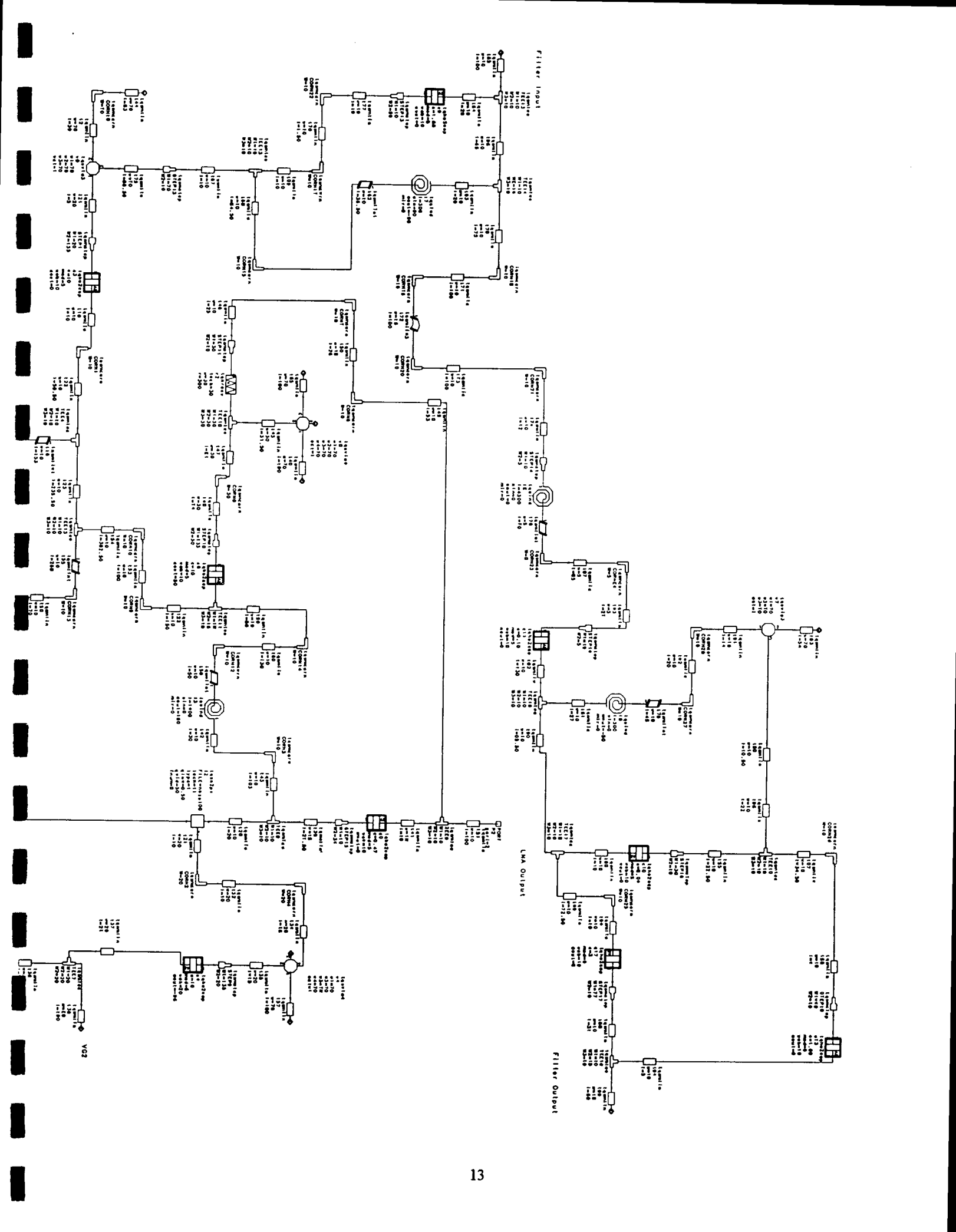
In the schematic, large (100 nH) inductors were added to the DC bias ports to simulate a wire from the power supply. Also, 43 fF capacitors were added to the input and output RF ports. These simulate the effect of the bonding pad capacitance to ground. The result was no change in gain or input return loss, 1 dB worse output return loss, and .06 dB worse noise figure. Thus, given the ample margin in the design, the probed response should be well within the specifications.

IV. Schematic Diagram

The complete schematic for the MMIC, including LNA and filter, is shown below. It has been split between two pages for easier reading. The only off-chip circuit consideration is to avoid applying more than 9 V DC to the output port since a 300 Ω, 30 μm, NiCr resistor connects it to ground. The maximum current allowed through the

resistor is 30 mA. Thus if the amplifier is used before circuit having a DC bias, a blocking capacitor should be added off-chip.


LNA Input
VG1
VG
VG2


Filter Input
LNA Output
Filter Output
VG2

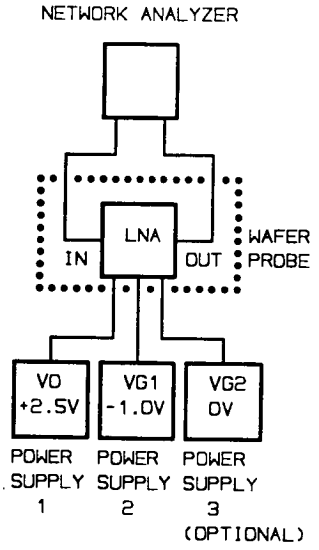
V. DC Analysis

The EESof Series IV DC Test bench was used to check the biases of the amplifier. The results showed that at the gate of FET 1, the voltage was measured as -.96 V instead of the intended -1.0 V. This indicates that 5 μA flows across the 8 kΩ gate resistor. The voltage at the drain of FET 1 was 2.45 V instead of 2.5 V. With 9 mA flowing through the channel, it is clear that there is 5 Ω of resistance in the inductor and interconnects. The voltages at both FET's sources were 0 V as expected. The voltage at the gate of FET 2 is 0 V as intended, and the voltage at the drain of FET 2 is 2.35 V instead of 2.5 V. This is acceptable. Since 45 mA flows through the channel of FET 2, the resistance of the inductor and interconnects must be about 3.3 Ω. No resistors are used in series with the channel currents. Thus the only consideration is the width of the metal.interconnects. The weak links are the Metal 1 traces, and they are all 10 μm wide. They can handle up to 90 mA. There are some 5 μm traces associated with an inductor, but a blocking capacitor prevents bias current flow in that path.

VI. Test Plan

The following block diagram shows the test equipment hookup required to probe the MMIC die. For testing noise figure, the network analyzer will be replaced by the noise figure meter. Power supply 3 will be used to experiment with the drain current in FET 2 after initial tests are performed at the designed levels. The tests for the bandpass filter will require only the network analyzer.

To be sure that the right amount of current is flowing, the power supplies will have to have an ammeter. The sequence of events will be: V_{G2} will be set to 0 V, V_{G1} will be set to pinchoff, say -4 V. Then V_D will be set to 2.5 V. I_{DSS} will be flowing in FET 2. The value for I_{DSS} can be read from the ammeter. Knowing I_{DSS}, V_{G1} can be adjusted to about -1 V until the total current out of supply 1 (the V_D supply) is 1.2 I_{DSS}. Then the FETs are biased as designed.



VII. Conclusion

The LNA should work as expected. It is not especially sensitive to matching network component values, and there is margin in the design. Also the ability to adjust the bias voltages and currents will provide extra assurance.

The bandpass filter is not expected to perform as well as the simulations show. The MIM capacitors will likely be off, and the filter is sensitive to their values. It will be interesting to see how far off it is. If it is off in frequency but still has a good match, then the midband loss will be useful in showing the improvement in inductor Q due to Triquint's new process.

VIII. References

[1] Les Besser, "Stability considerations of low-noise transistor amplifiers with simultaneous noise and power match," *IEEE MTT-S Int. Microwave Symposium Digest*, 1975, pp. 327-329.

[2] R. Lehmann and D. Heston, "X-Band monolithic series feedback LNA," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 1560-1566, Dec. 1985.

A

MMIC Design
525.787
Fall 1995

C Band Driver Amplifier

Michael Goudy
December 11, 1995

1.0) Summary

The design and design process of a multi-stage amplifier optimized to provide specified gain, bandwidth, output power and VSWR is presented. Given the environment in which this project was accomplished - i.e. the classroom - special attention should be given to the design process itself.

Specifications for this design are given in the table below.

Specifications for C Band Driver Amplifier

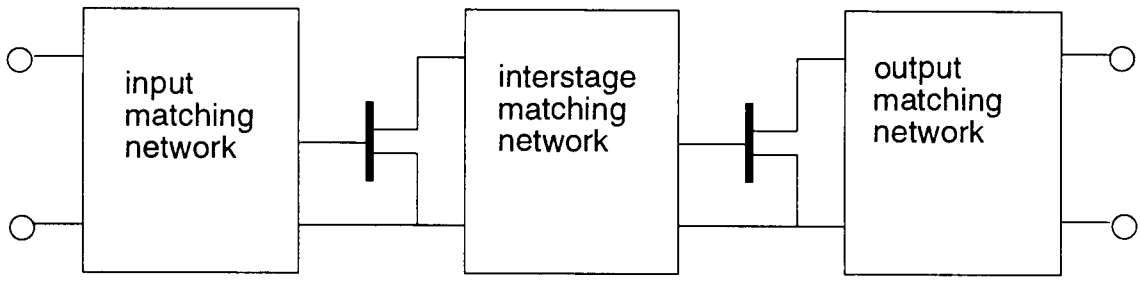
frequency	5725 to 5875 MHz
bandwidth	> 150 MHz
gain	> 15 dB > 25 dB, goal
gain ripple	± 0.5 dB goal
output power	> +15 dBm @ 1 dB compression point
VSWR, 50 ohm	1.5:1 input & output
supply voltage	± 5 Volts, + 5 volts only, goal
size	60 x 60 mil ANACHIP

2.0) Introduction

As with any design, the design process begins with the specifications; in particular, gain and output specifications dictate not only the topology of the circuit but also FET selection and bias levels. Matching networks were designed to provide optimal power and gain, respectively. The overall physical constraints of the chip provide additional concerns.

2.1) Design Philosophy

As mentioned above, the salient specifications are that of gain and output power. It is these specifications which dictate the basic topology of the amplifier. The number of stages is chosen based on the gain of any one individual stage. Given that the gain of an individual stage is approximately 7 - 8 dB, at least a two stage amplifier is required. As a three stage amplifier is preferable to meet the gain specification, the physical size of the chip - 60 mil x 60 mil - only allows space for a two stage design. With this, a two stage amplifier was chosen. This basic topology is depicted below.



2.2) 2nd Stage Amplifier Design

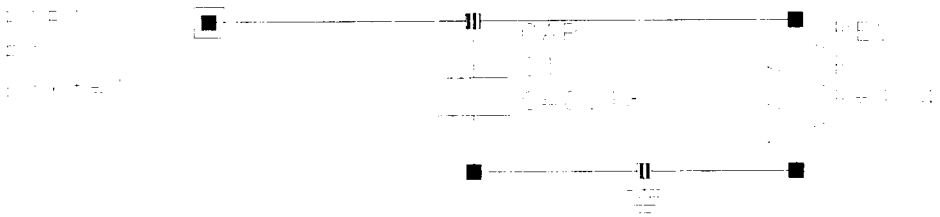
The design of the circuit begins with the second amplifier where the output matching network is designed to provide maximum power transfer. Before the output matching network can be designed, however, specifications for the FET itself must be chosen including not only the physical dimensions of the FET - i.e. number of fingers and gate width - but also stabilization and biasing considerations.

Initial biasing of the FET was chosen based on the output power requirement; that is, V_{DS} = 3.5V and Ids = 60%I_{DSS}. Biasing is typically chosen with respect to the breakdown voltage of the FET where, for the purposes of this design, the model provided by Libra was used to determine the breakdown voltage. Unfortunately, the Libra model used in this design was incorrect in that the breakdown voltage was observed to be approximately 7 Volts - some 10 Volts below the actual breakdown voltage.

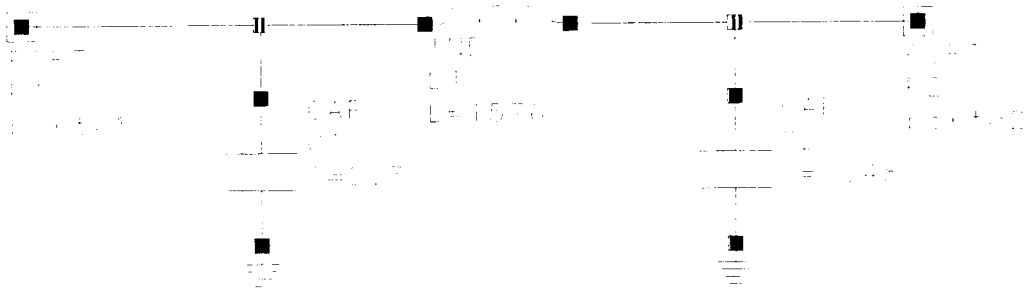
The size of the FET was then chosen to provide not only maximum power transfer, but also to provide realizable stabilization and output matching networks. Therefore, the size of the FET was initially chosen to have 6 fingers with a 90 μm gate width - i.e. a 540 μm device. As it is desirable to stabilize the device with a minimal reduction in gain, the most obvious stabilization technique is that of a shunt resistor across the gate or drain.

This, however, proved difficult in that sufficient stabilization to allow a realizable output matching network could not be achieved without adversely affecting the gain. Therefore, a source inductor was chosen to provide frequency selective feedback stabilizing the FET only at the design frequency of 5.8 GHz. Out-of-band stabilization is then achieved - hopefully - via the lossy characteristics of the TriQuint elements used in the matching networks. In the end, a 6x100 μm - i.e. a 600 μm device - was employed in the final design.

Next, the output matching network was designed to provide maximum power transfer using the Cripps method as described in lecture. Briefly stated, the S_{11} of a simple RC model of the FET is matched to S_{22} of the stabilized FET itself. This model is depicted below.



A $\lambda/4$ transformer using ideal elements was then constructed with the left-most capacitor being reduced in value by the capacitance as determined by the RC model shown above. The ideal $\lambda/4$ wave output matching network is shown below.



Implementation of this matching network can not, however, serve the dual purpose of a biasing network; meaning, an additional RF choke inductor and blocking capacitor would have to be added to the circuit. As this is not desirable - especially with regard to physical space limitations of the chip - an alternative $3\lambda/4$ transformer was implemented with S_{11} of the $3\lambda/4$ transformer being matched to S_{11} of the $\lambda/4$ wave transformer thereby allowing a "bias-friendly" design. The disadvantage in using the $3\lambda/4$ transformer vice the $\lambda/4$ transformer is a limitation in overall bandwidth. This shortcoming, however, was not a concern given the gain ripple and bandwidth specifications of this design.

2.3) 1st Stage Amplifier Design

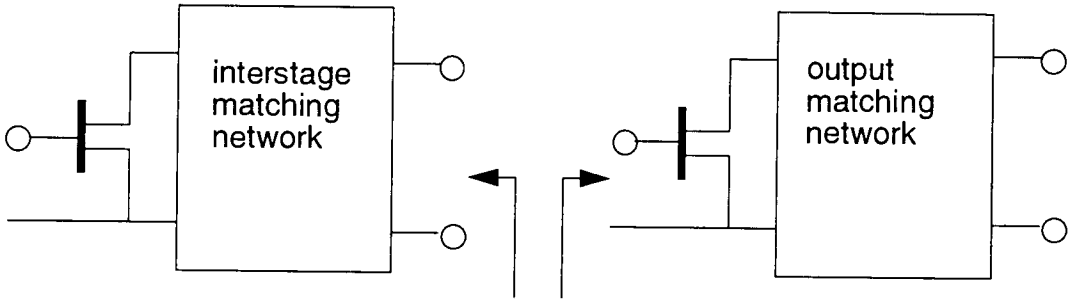
As with the second stage, design of the first stage amplifier begins with selection of the FET and biasing conditions. Where the second stage amplifier was designed to provide maximum power transfer, the first stage amplifier was designed to provide maximum gain. Biasing of the first stage FET was chosen with regard to the manner in which

the chip will be tested. Specifically, biasing was chosen to be identical to that of the second stage thereby allowing only two voltage supplies for the gate and drain. Use of "breakable" airbridges will allow the first stage FET bias conditions to be altered if required.

As alluded to previously, gain of this amplifier must be maximized in order to meet the gain design specification. Since gain is not a function of the physical size of the FET, it is advantageous to reduce the overall gate width thereby allowing the circuit to operate more efficiently - more efficient in that the circuit will "draw" less current.

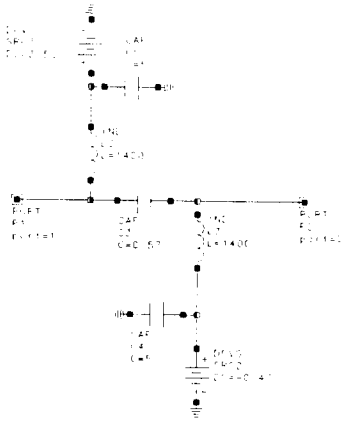
The size of the FET was chosen to have a total gate width of 360μm - approximately 2/3 the size of the power FET. As before, stabilization of the FET was achieved using a source inductor tuned for the design frequency of 5.8 GHz.

Next, the interstage matching network was designed to provide maximum gain transfer. This was accomplished by matching S_{22} of the first stage FET to GM1 of the second stage amplifier circuitry. This methodology is depicted below.

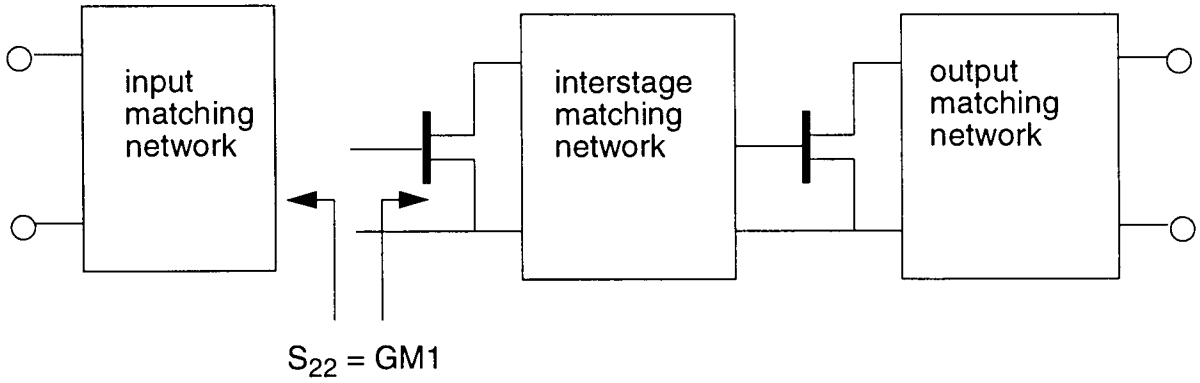


S_{22} = GM1

It should be noted the interstage matching network was achieved using a "bias friendly" LC network similar to that of the output matching network. A simplified design is shown below.

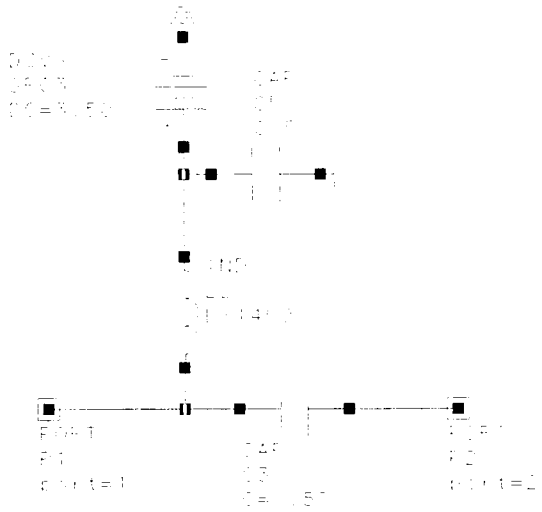


Finally, the input matching network was designed by again matching a "bias friendly" LC network to GM1 of the circuit. This methodology is depicted below.



2.4) Bias Circuitry

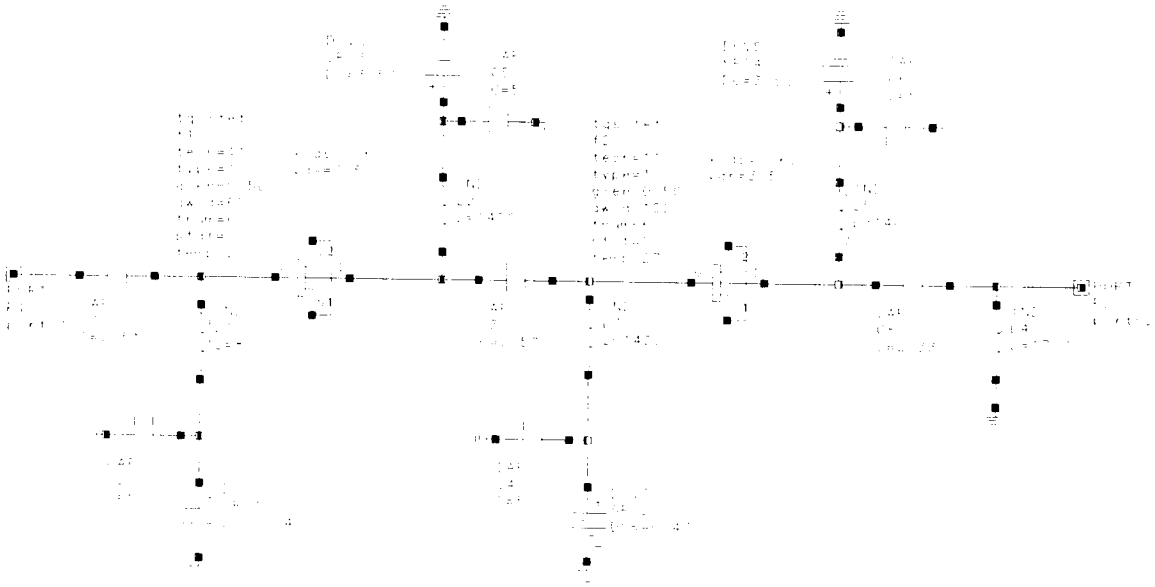
As mentioned above, all matching networks were designed to be "bias-friendly"; that is, matching networks were designed to contain a shunt inductor and a series capacitor. Additional 5 pF bypass capacitors were also included. An example of an ideal bias network is depicted below.



2.4) Final Design

Output power, gain and VSWR were measured following the design steps delineated above. Gain, output power and input VSWR were found to meet specifications; output VSWR, however, was found to exceed specifications. To correct for this, the output matching network was "tuned" to improve the output VSWR while taking care to maintain output power above the specified 15 dBm.

A simplified schematic of the final design is shown below.



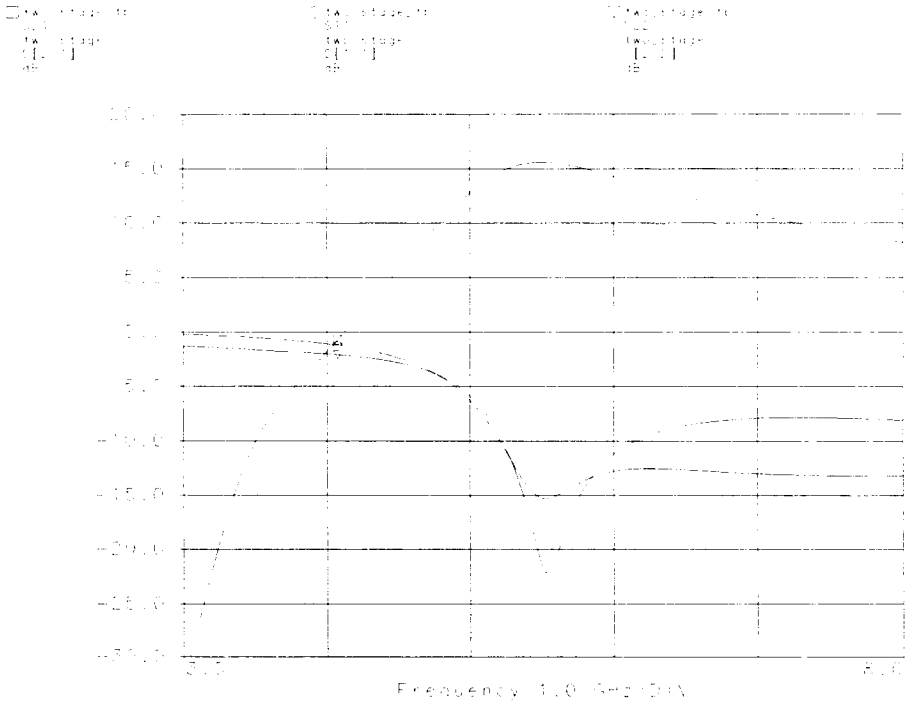
3.0) Modeled Performance

Design specifications and subsequent predicted performance is summarized in the table below.

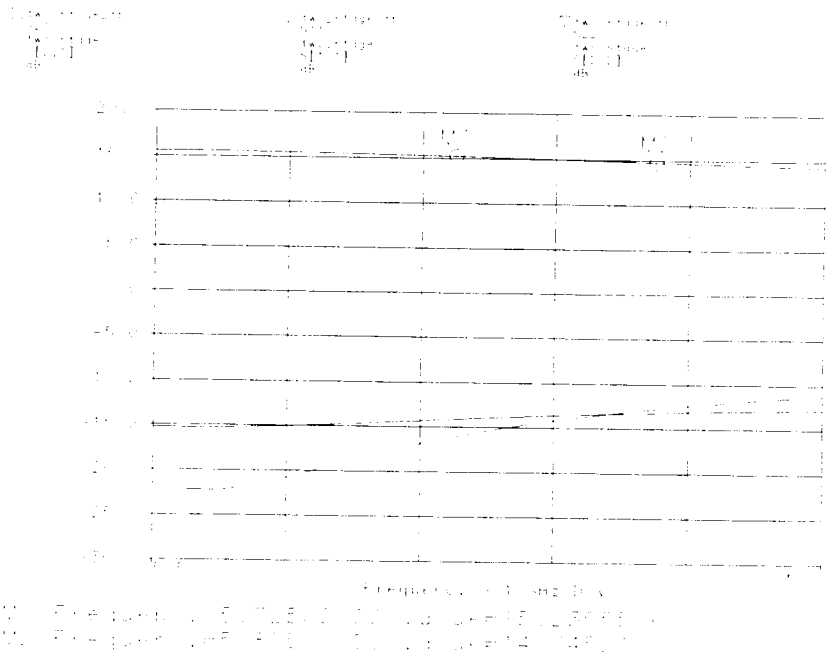
Specification	Goal	predicted
gain	>15 dB	14.74 (min)
gain ripple	± 0.5 dB	± 0.49
bandwidth	> 150 MHz	> 150 MHz
output power	> +15 dBm	+ 15 dBm
VSWR, 50 ohm	< 1.5:1	1.59:1 (max)

3.1) Gain plots

S-parameters from 3 to 8 GHz are given below. Of note is the effect of the 3λ/4 transformer used in the output matching network with regard to bandwidth.



S-parameters from 5.5 to 6 GHz follow. Markers indicate gain at design frequency band edges of 5.725 GHz and 5.875 GHz.

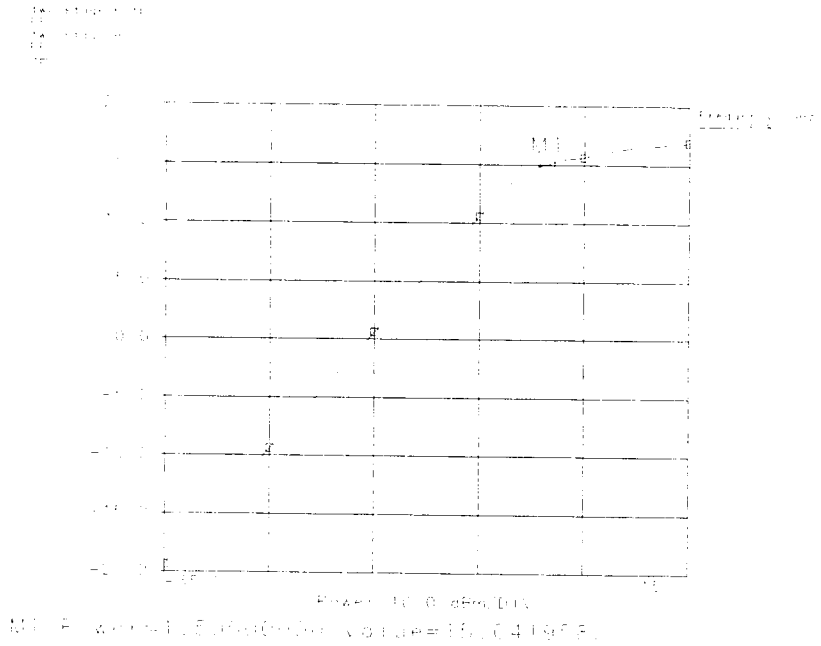


3.2) Gain Ripple

From the plots shown above, gain is shown to vary from 14.74 dB to 15.23 dB yielding a 0.49 variation of gain.

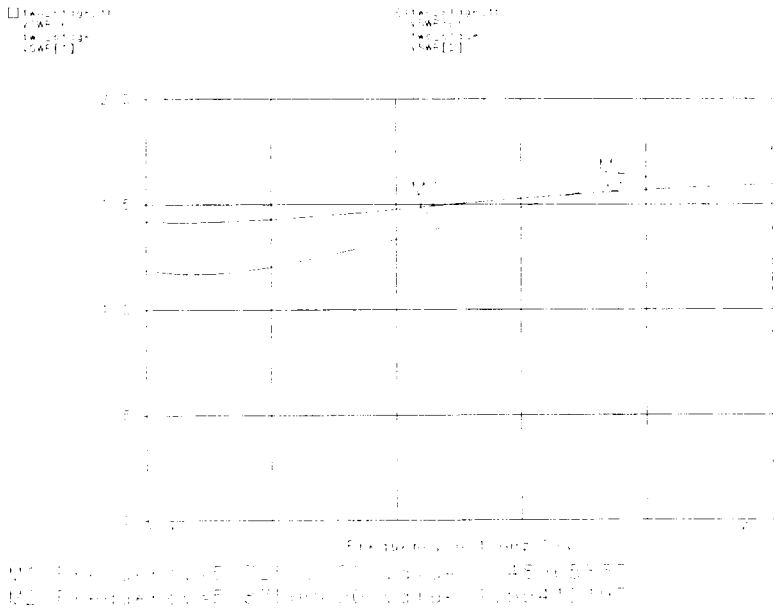
3.3) Output Power

Output power at the 1 dBm compression point is shown to be 15 dBm.



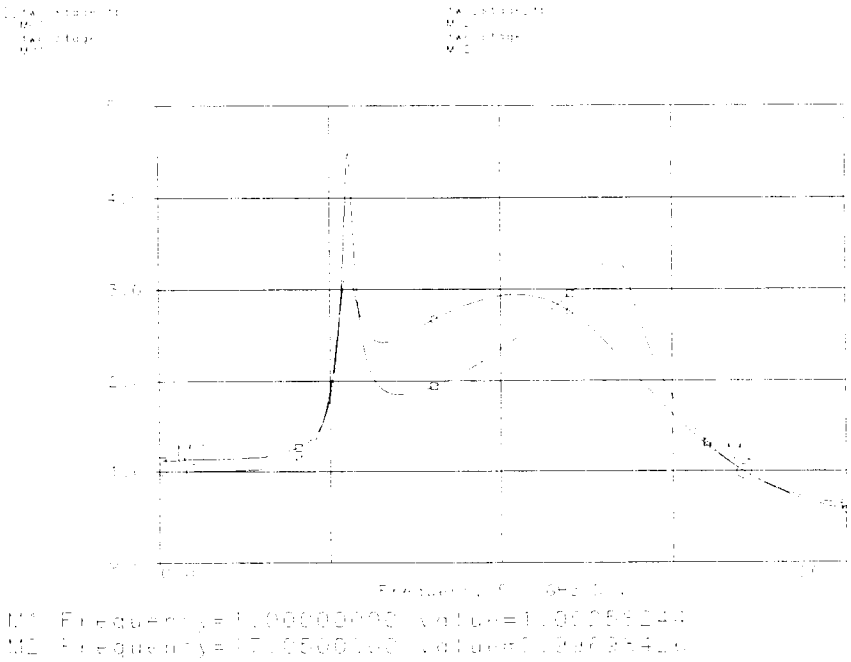
3.3) VSWR

Both input and output VSWR are measured below. Markers indicated maximum values at the frequency band edges.



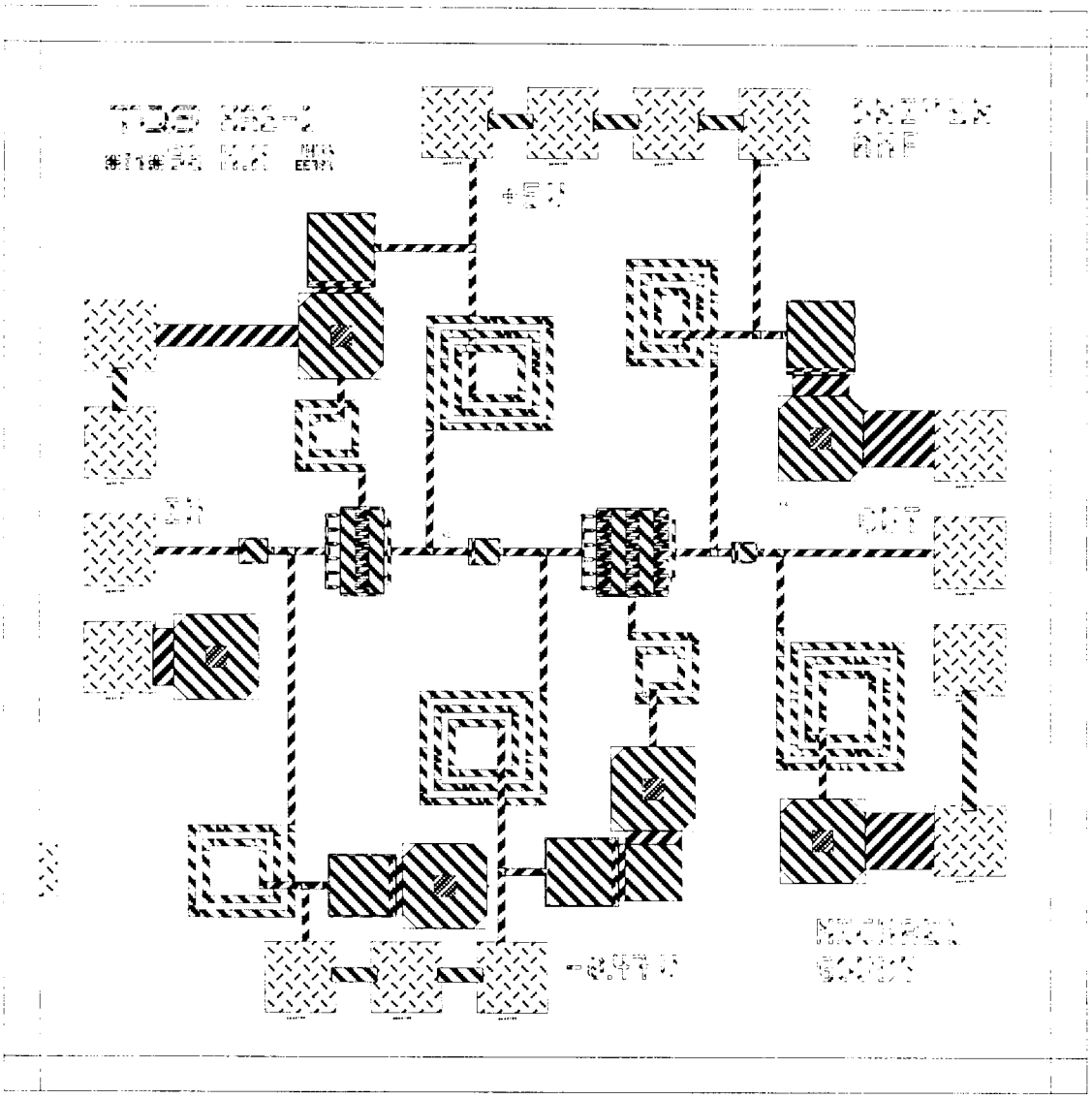
3.4) Stability

Stability measurements using the parameter μ is given below from 100 MHz to 20 GHz. Note possible instability above 17 GHz. Analysis of S-parameters above 17 GHz indicates these instabilities probably result from shortcomings of the model at high frequencies.



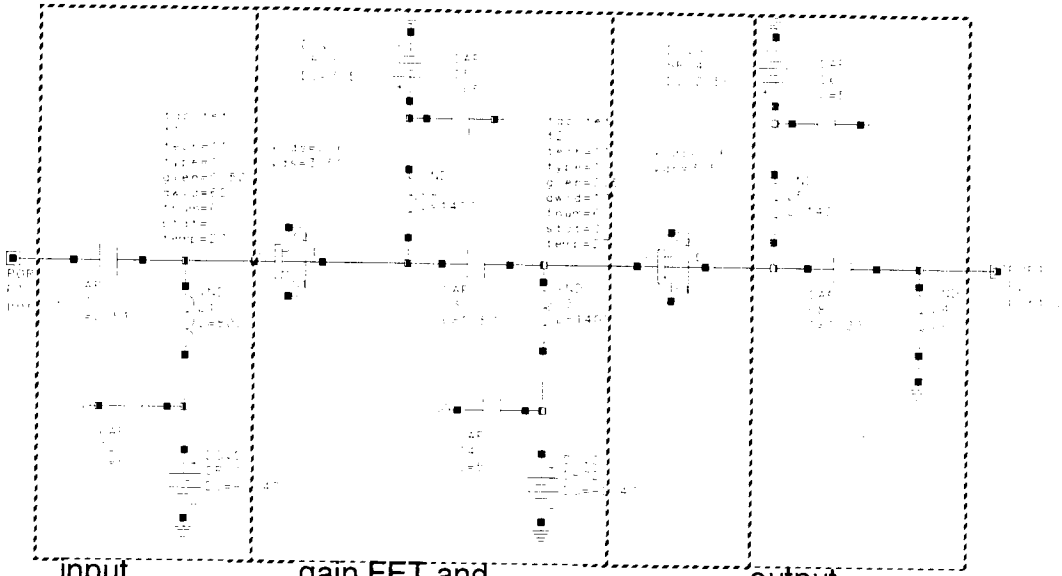
3.5) Final Layout

A final layout of the circuit is given.

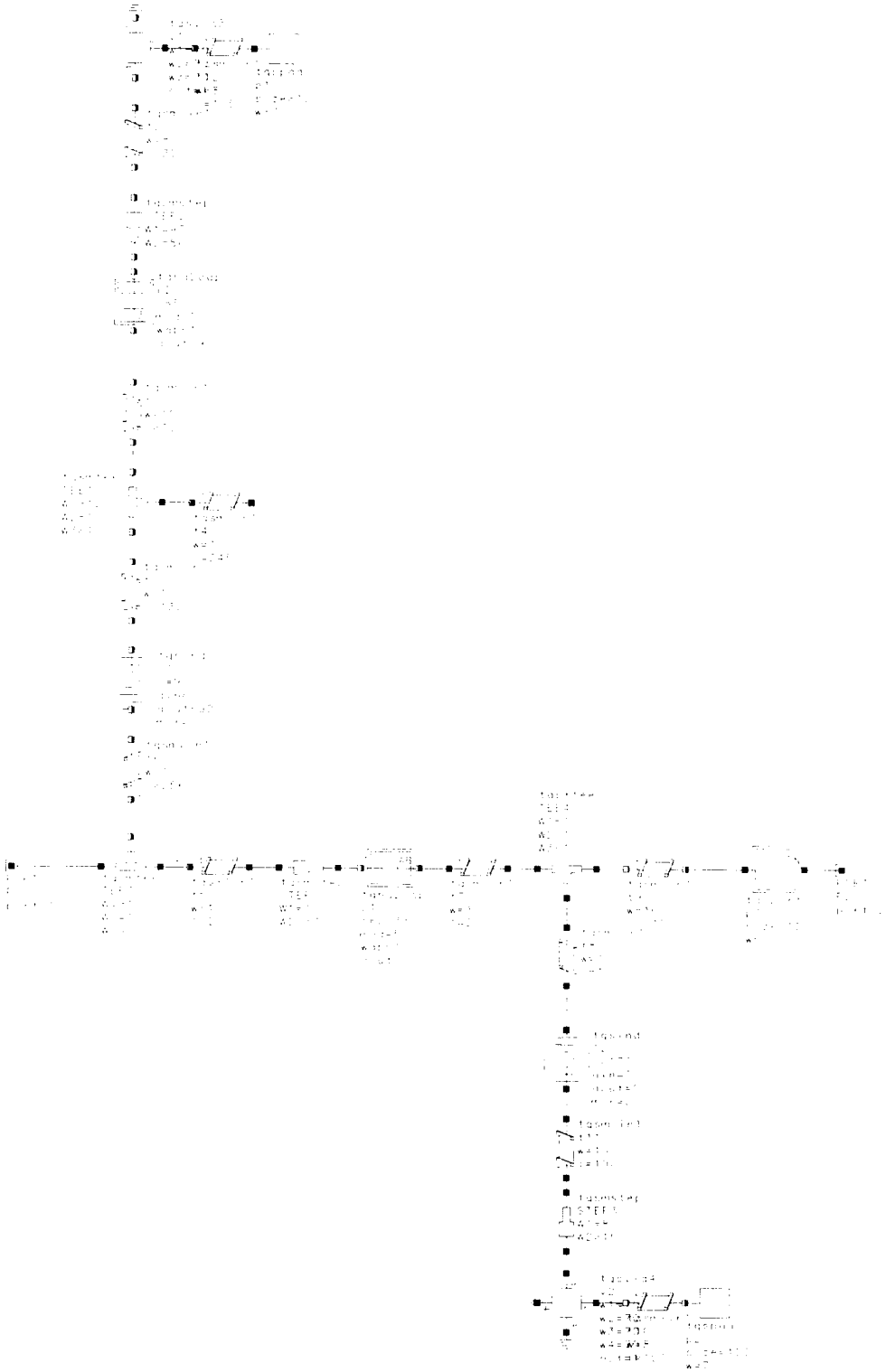


4.0) Schematic Diagrams

Schematic diagrams of each "section" of the circuit follow. Sections are defined in the figure below.

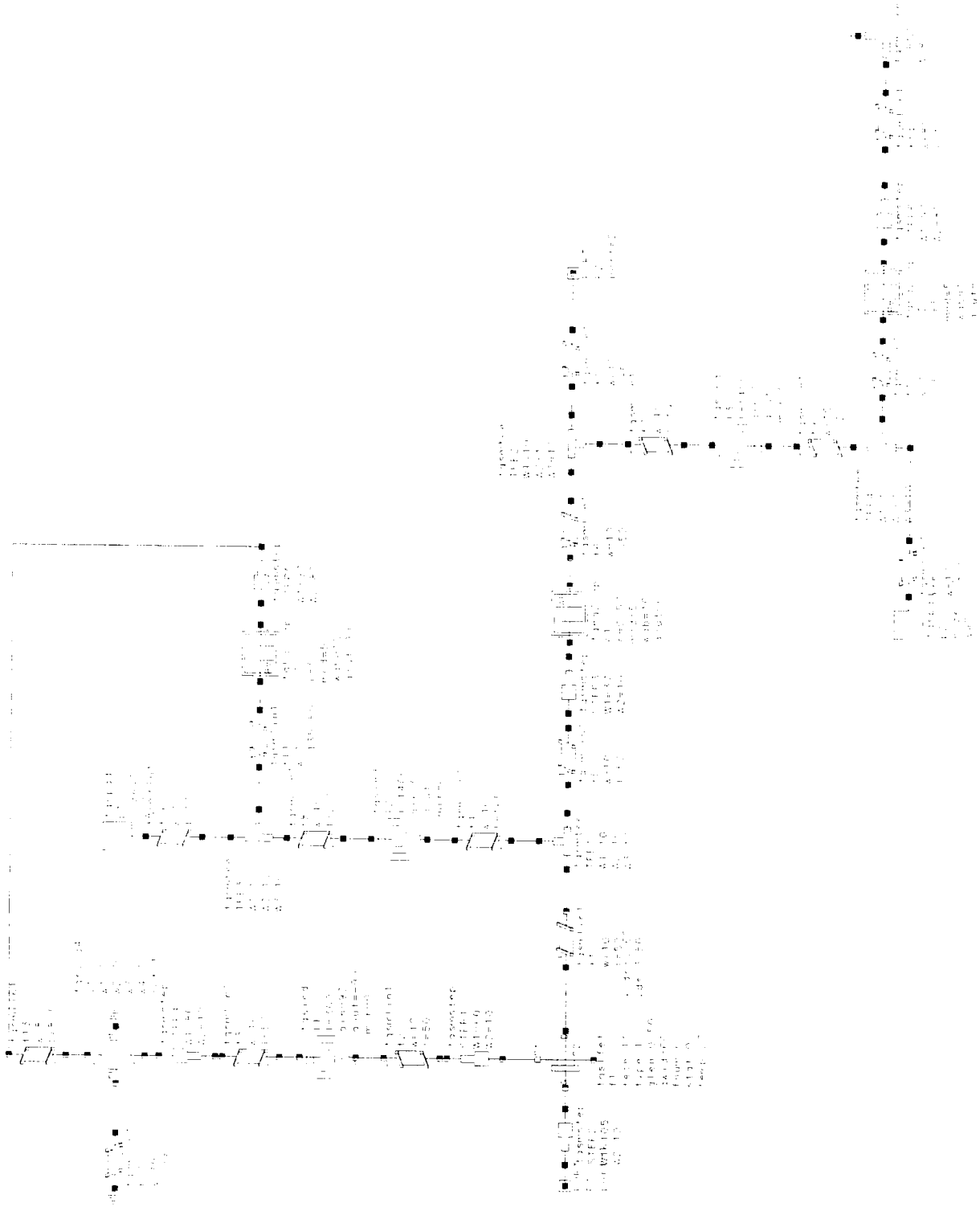


4.1) Output matching network

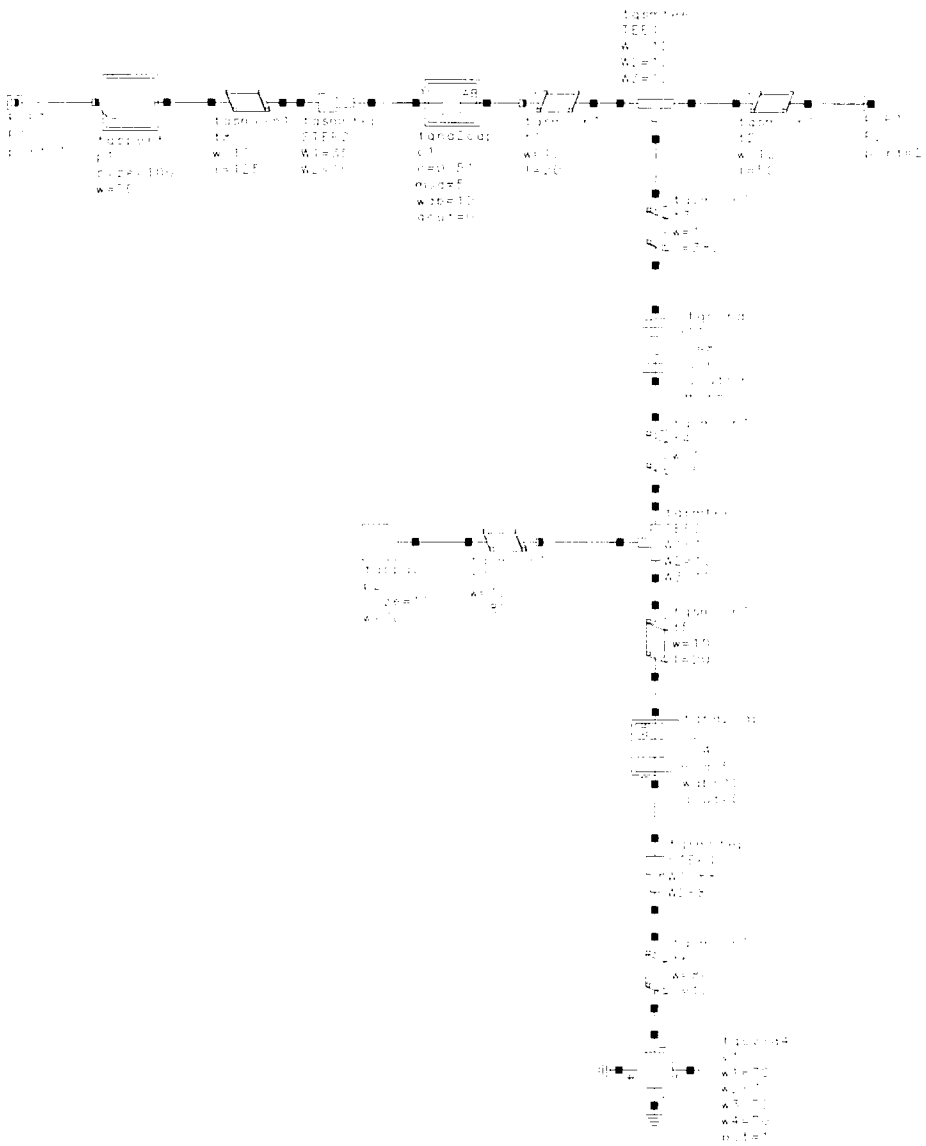


4.2) Power FET

4.3) Gain FET and interstage matching network

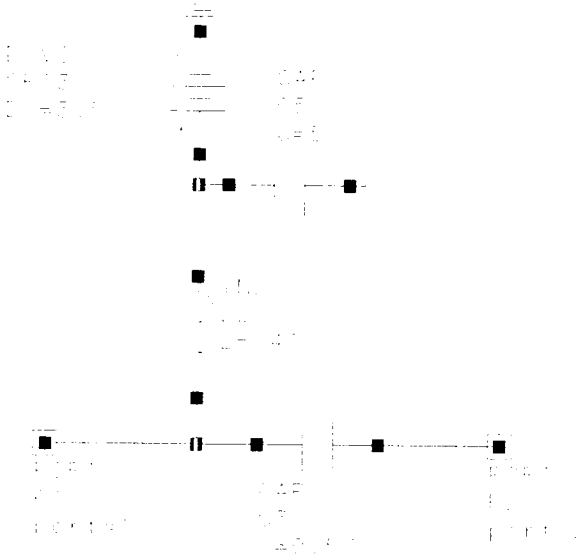


4.4) Input matching network



5.0) DC Analysis

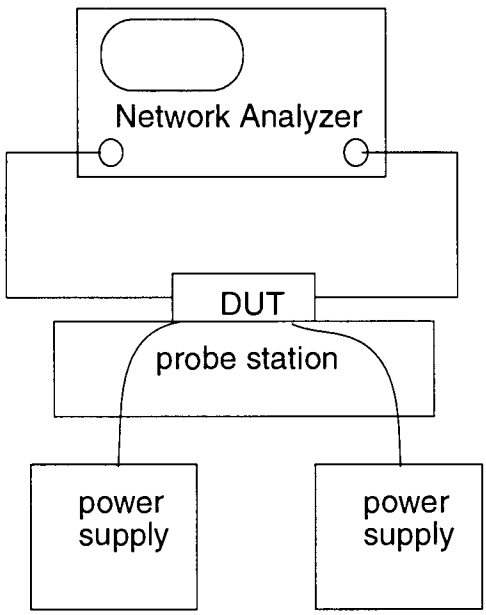
All matching networks were designed to serve the additional function of a biasing network. That is, shunt inductors, series capacitors and a 5 pF bypass capacitor was used in all cases. An example of an ideal bias network is given below.



With regard to DC current stress, areas of concern were identified as being metal-1 and various airbridges. In both cases, currents are expected to be far below maximum current densities.

6.0) Test Plan

A simplified schematic of the test setup is shown below.



S-parameter and VSWR measurements are expected to be accomplished using test equipment as supplied by JHU. Specific test procedures are relevant to the supplied Network Analyzer.

7.0) Conclusions

A two stage amplifier was designed to meet gain and output power specifications. Expected performance of the amplifier is given with the design specifications below.

Specification	Goal	predicted
gain	>15 dB	14.74 (min)
gain ripple	± 0.5 dB	± 0.49
bandwidth	> 150 MHz	> 150 MHz
output power	> +15 dBm	+ 15 dBm
VSWR, 50 ohm	< 1.5:1	1.59:1 (max)

7.1) Recommendations & Comments

As evident in the table above, specifications are met if the numbers shown above are creatively rounded-off! How could this situation be corrected? It would have been interesting to note the effect of a better FET model; specifically, I would have liked to have biased the FET(s) at a higher level. This, I believe, would have not only increased output power, but also gain.

Another approach to improve the design would have been the addition of a third stage. I believe this could have been accomplished by using a physically smaller, resistor-based biasing network. This design could have been realized by simply cascading a third amplifier in series or, more interestingly, in the form of a cascoded amplifier.

A

Dual Frequency Voltage Control Oscillator with IF offset

by

Adrian Gilbert

Microwave Monolithic Integrated Circuit Design
EE 525.787
Instructors: Craig Moore / John Penn

Abstract- A Dual frequency voltage control oscillator is presented for use in a Wlan transceiver operating in C band (5.725-5.875GHz & 6.025-6.175Ghz). The oscillator was designed using both small and large signal methods to ensure proper start-up conditions and a stable oscillation at the desired frequency. The oscillator is bosting an output power of approximately 11.72 dBm at band center (5.95 Ghz) but has a poor output reflection coefficien (S11) due to the fact that a power amplifier had to be used to obtain the desired power level.

Introduction

Today, microwave and millimeter-wave power oscillators are used widely as transmitters sources and local oscillators in communication, radar, and electronic warfare systems. Large-signal or power oscillator design traditionally has been more art than science due to the fact that the tuning of a power oscillator's performance requires extensive, empirical trial and error adjustment of the circuit structure.

This paper will concentrate on the implementation of a dual frequency voltage control oscillator to be used in both the transmitter and receiver of a Wlan Transceiver. The design specs are as follows, a dual frequency range of 5725-5875 MHz & 6025 - 6175 MHz, an output power > +5 dBm with a goal of +10 dBm a control voltage 0 - (-5) volts and a supply voltage of +/- 5 volts. The design will be laid out on a 54 X 64 mil ANACHIP

Design Philosophy

The condition of oscillation in a design is based on the negative impedance approach. Assuming that there is a steady state oscillation going on between the two networks as shown in fig 1, i.e., there is a non zero loop current I flowing through the network. Since the loop voltage $V = I (Z_D + Z_L)$ must be zero according to Kirchoff's law, we arrive at the conclusion that $Z_D + Z_L = 0$, in other words, $Z_D = -Z_L$ (negative impedance).

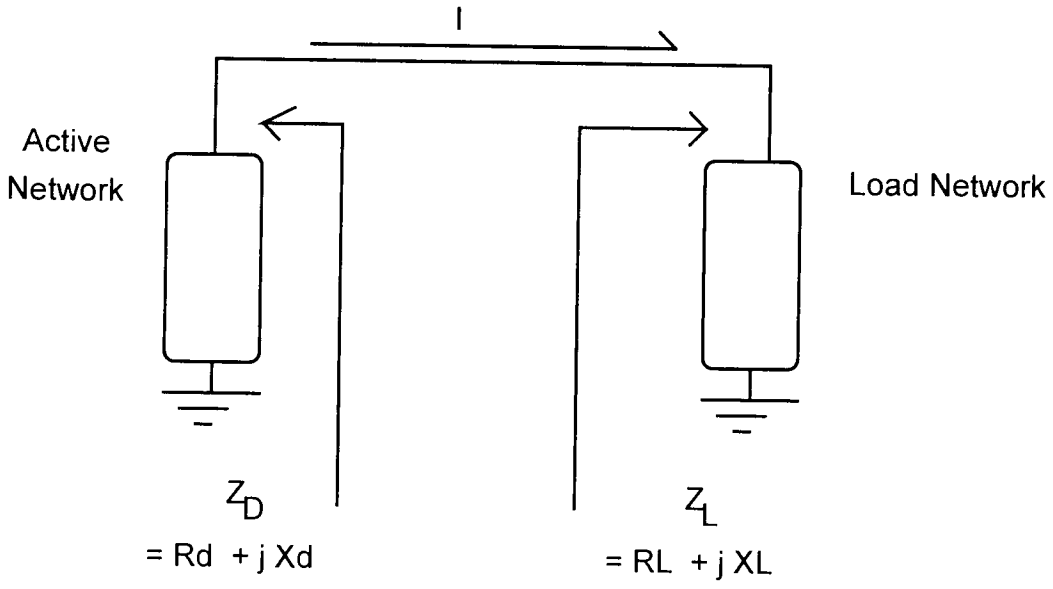


Fig 1

The negative impedance condition can further be broken down into it's resistive and reactive components i.e. $R_D = - R_L$ and $X_D = -X_L$ respectively. For a passive load ($R_L > 0$), we must have $R_D < 0$. This is obtained by destabilizing the active

device with an appropriate resonate circuit. For the reactive part, it is usually convenient to select the interface plane between the two networks such that $X_D = X_L = 0$

The negative impedance condition above is based on an on going steady state oscillation which have neither a beginning nor an end. In practice, oscillation starts because of noise signals inside the circuit, which although small in amplitude, is rich in frequency components. Therefore, at the frequency where the negative impedance condition is met, the oscillation is sustained. However, for the oscillator to be useful, the amplitude of the oscillation must be greater than the level of the noise signal. In other words, the oscillating signal must grow. It is common practice in the small signal design of an oscillator to modify the relationship between R_D and R_L so that the oscillating signal can grow. These are usually referred to as start-up conditions which are listed below.

Start-Up Conditions:

Series Resonance Oscillator $\quad |R_D| > 3\,R_L$ **and** $X_D = -X_L$

Parallel Resonance Oscillator $\quad |R_D| > \frac{RL}{3}$ $\quad$ **and** $X_D = -X_L$

After the oscillation begins, the signal will keep growing as long as the active device is still working in it's linear region, i.e. the small signal start-up

conditions are still met. When the oscillation grows so large such that the active device starts to saturate, the impedance of the network will change and the oscillating frequency will move accordingly. The final oscillating frequency, as the oscillator reaches steady state, depends on the large signal characteristics of the active device. It was suggested in some articles that this moving of the oscillating frequency is proportional to the factor in the start-up condition to set the resistive values apart. In other word, the faster the signal grows, the further away the resulting oscillating frequency is from the design point.

Modeled Performance

The design of an oscillation begins with choosing the appropriate transistor as the negative resistive element, and a suitable device topology. For this design a 50um gate width, 0.5 um gate length transistor was chosen. This transistor has a total of 6 fingers thus giving the total gate periphery of 300um. This device was chose because it displayed a saturated output power > 10 dBm, which was more than enough to meet the design specs. Biasing was accomplish using one +5v supply in a self bias configuration with the gate grounded through a shunt inductor. Series capacitive feedback in the source was used to enhance the instability of the device creating an S11 greater than one. The entire linear design

was centered around 5950 MHz and a tune voltage of -0.3v which correspond to a diode capacitance of 165ff. A block diagram of the complete design can be seen in fig 2. Each design step will be outlined as follows.

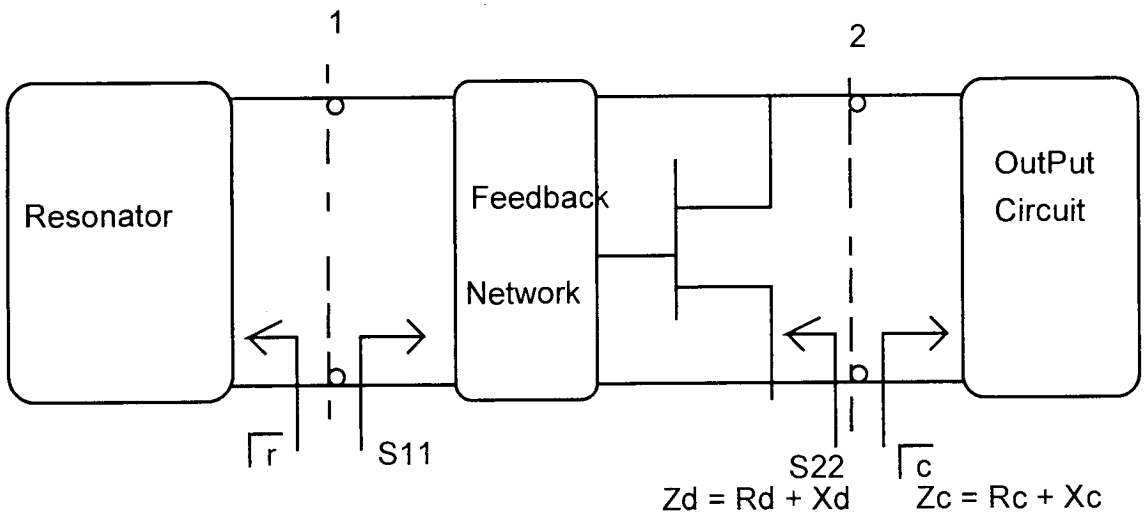


Fig 2

The resonator circuit consist of a varactor diode made from a full fet with it's source and drain terminals tied together. The device size is 100um with a capacitive tuning range between 110 and 220 ff which correspond to a tuning voltage range of -1.5 - 0 v and a tuning range of $\frac{Cmax}{Cmin} = 2$. The reflection coefficient Γr was chosen so as to produce

$$\mathbf{S}11 = \frac{1}{\Gamma \mathbf{r}} \qquad \text{Eq 1.0}$$

this expression implies that input port of the device is resonating and hence one of the criteria for oscillation has been met. Fig 3 shows the S11 of both the device

and the resonator. Notice that indeed S11 of the device is greater than one and upon careful inspection we can see that Eq 1 is also satisfied. Also note that there is no degeneracy in the oscillation frequency as the condition of Eq 1.0 is only satisfied

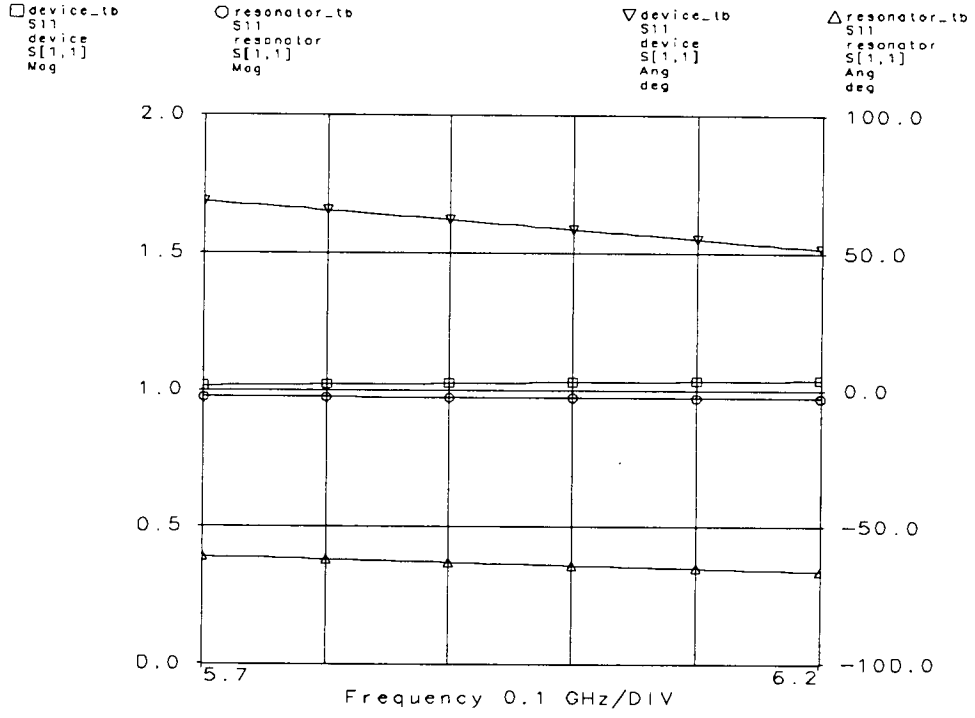


Fig 3

around the design frequency of 5950 MHz. This condition requires that the phase of 1/S11 and Γr be changing in opposite directions, in which they are.

With the resonator connected to the device, the system can now be viewed as a one port device looking into reference plane 2 in Fig 2. The input impedance Z_D looking into the device can be seen to exhibit negative resistance over the

entire band of interest as shown in Fig 4 for tuning capacitive values of 130, 165 and 220ff. Fig 5 shows the completed schematic of the Device and the Resonator. Upon inspection on the input reflection coefficient, the device was seen to be exhibiting parallel resonance and hence the load Z_C should be designed such that

$$R_C = 3\,|R_D| \quad \text{with } X_C = X_D = 0$$

since R_D has values ranging from -35 - (-65)Ω a nominal RD is chosen of value -50Ω, making Rc ~150 Ω. Notice that choosing an Rc of this value will cause the oscillation frequency to drift further from the one's shown in Fig 4.

The load network is actually a power amplifier Buffer designed for an output power of 12.7 dBm. The input was matched to meet the oscillation start-up conditions and whose output was matched to for the desired power. The input and output reflection coefficiens for the amplifier can be seen in Fig 6 along with power out versus power in curves for several frequency ranges , Fig 7. The final shematic can be seen in Fig 8

FIG 4.0

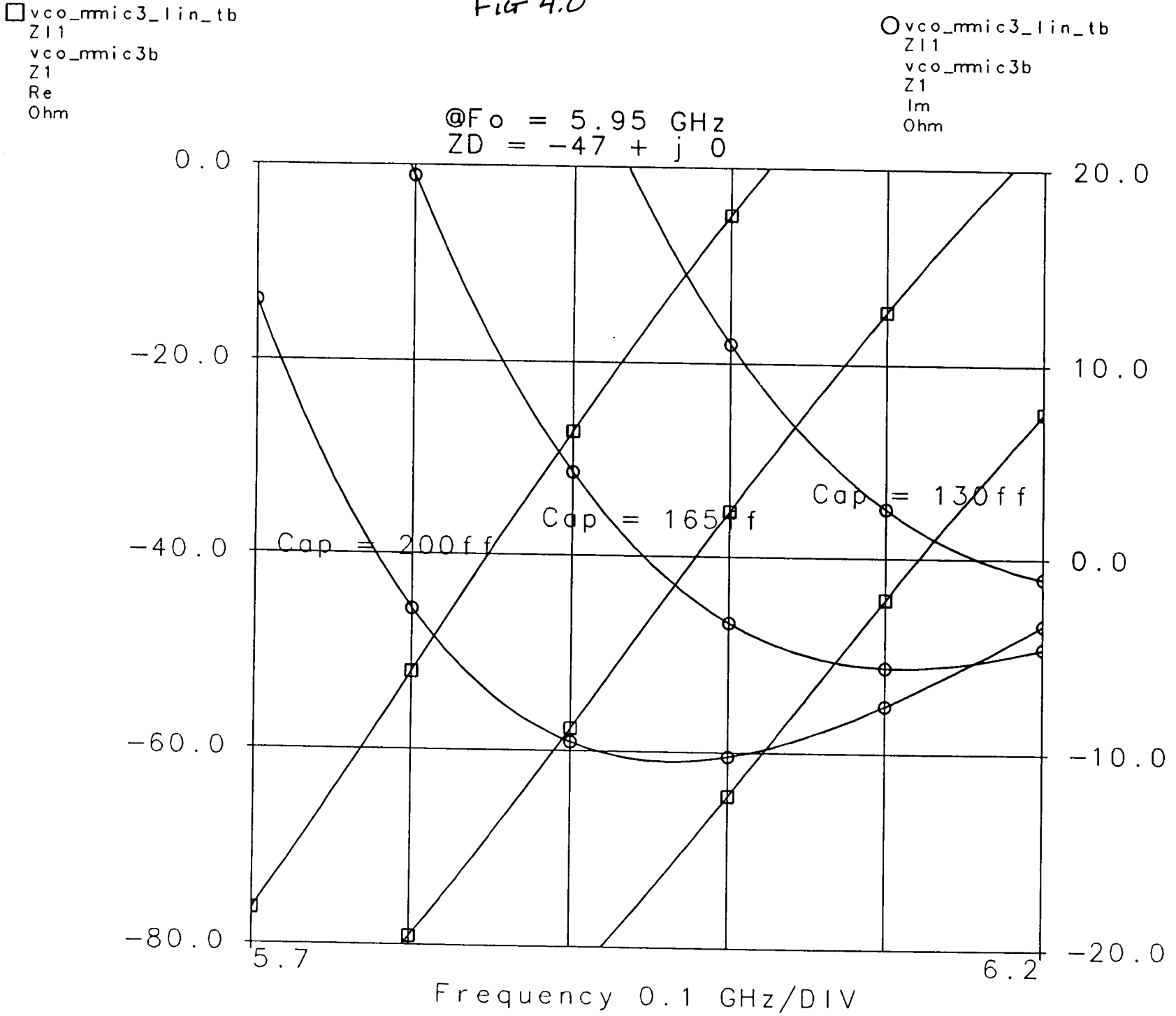
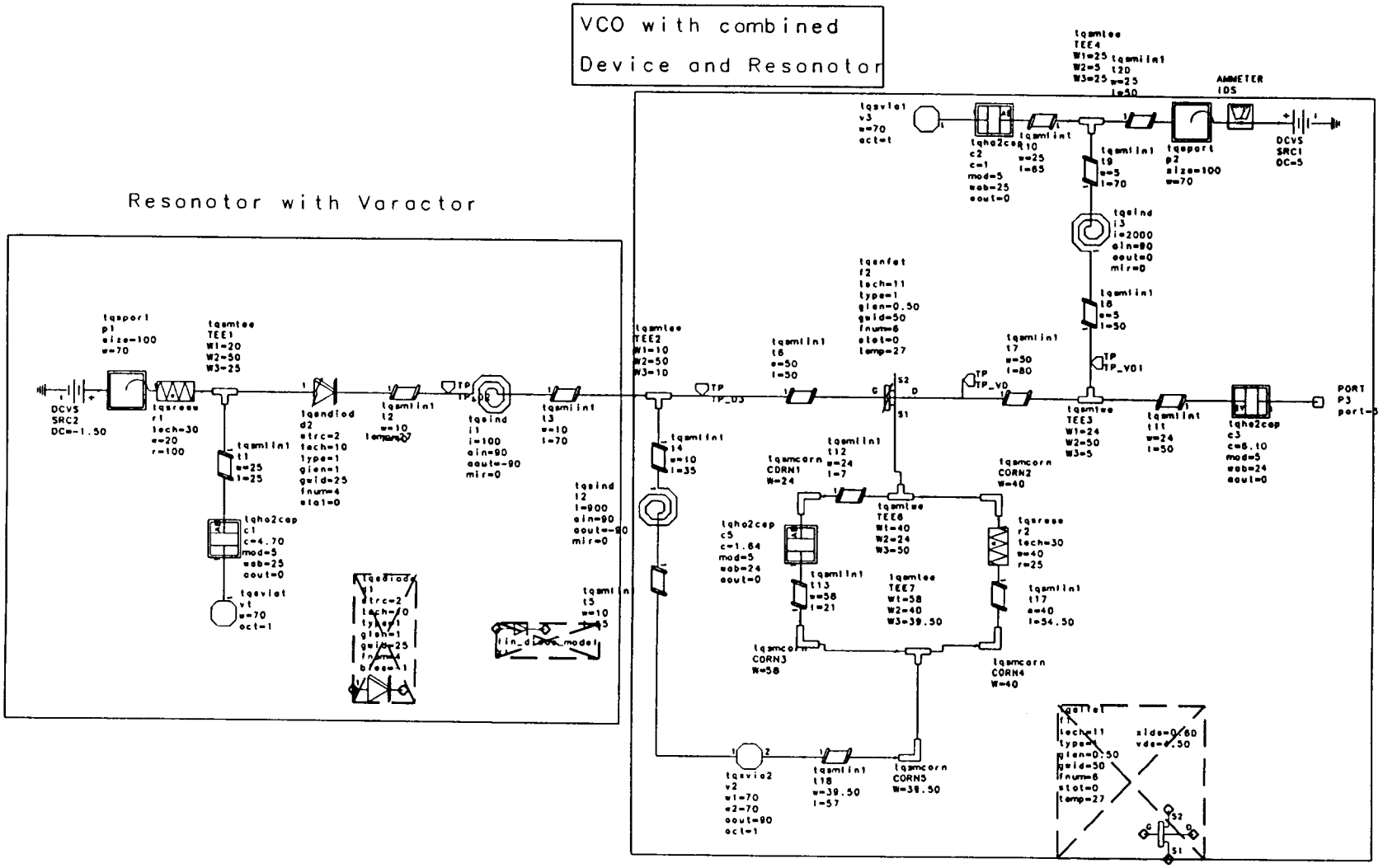

vco_mmic3_lin_tb
Z11
vco_mmic3b
Z1
Re
Ohm
vco_mmic3_lin_tb
Z11
vco_mmic3b
Z1
Im
Ohm
@Fo = 5.95 GHz
ZD = -47 + j 0
0.0
-20.0
-40.0
-60.0
-80.0
20.0
10.0
0.0
-10.0
-20.0
Cap = 200ff
Cap = 165ff
Cap = 130ff
5.7
6.2
Frequency 0.1 GHz/DIV

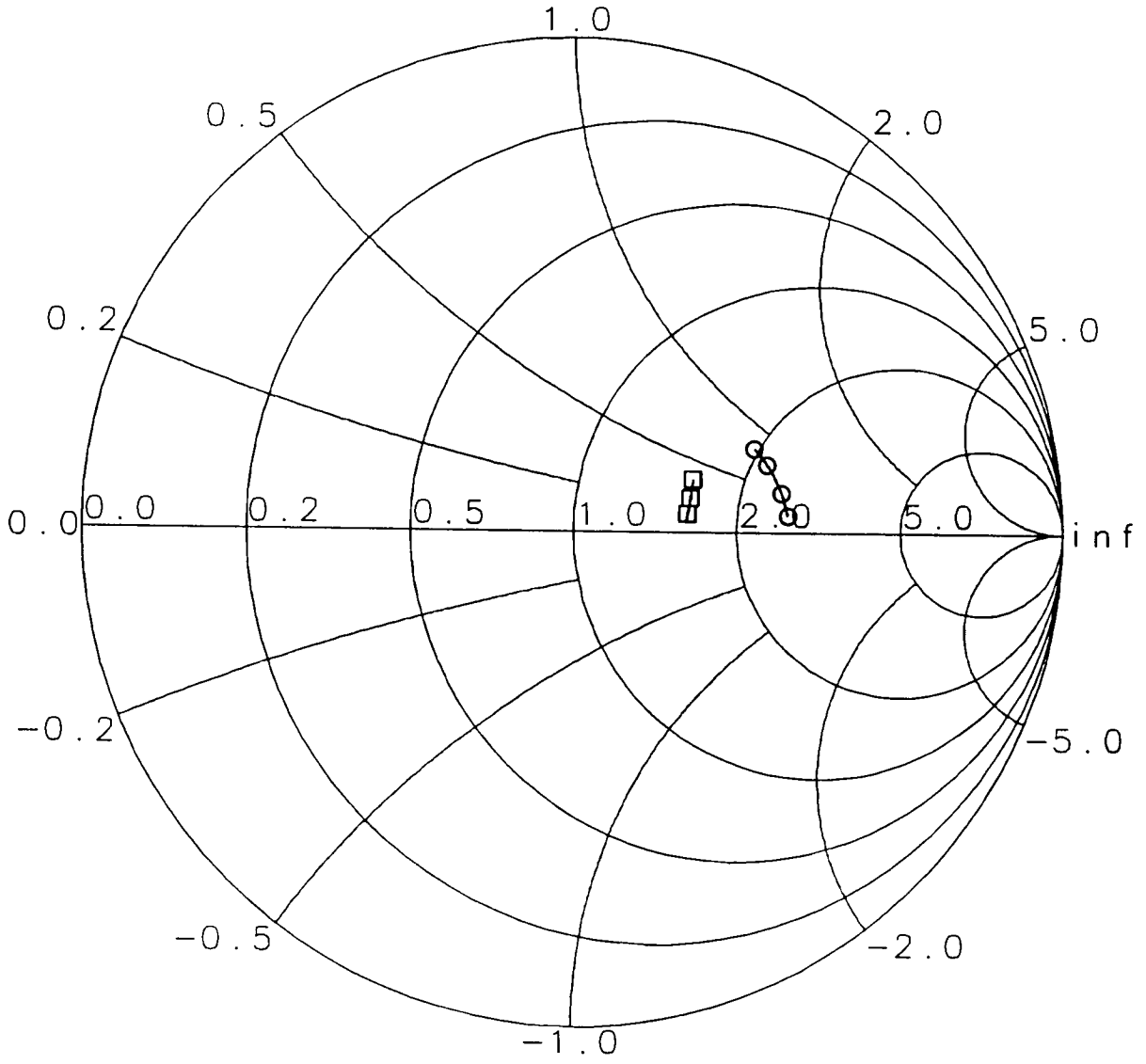
FIG 3.0


VCO with combined
Device and Resonotor
Resonotor with Varactor
Negative Resistonce Device
AMMETER
IDS
PORT
P3
port=5

□buffer_amp2_lin_mmic_tb
S11
buffer_a
S[1,1]

Fig 6.0

○buffer_amp2_lin_mmic_tb
S22
buffer_a
S[2,2]



Frequency 5.7 to 6.2 GHz

buffer_amp2_mmic_tb
Pout
buffer_amp2_
PF
dBm

FIG 7.0

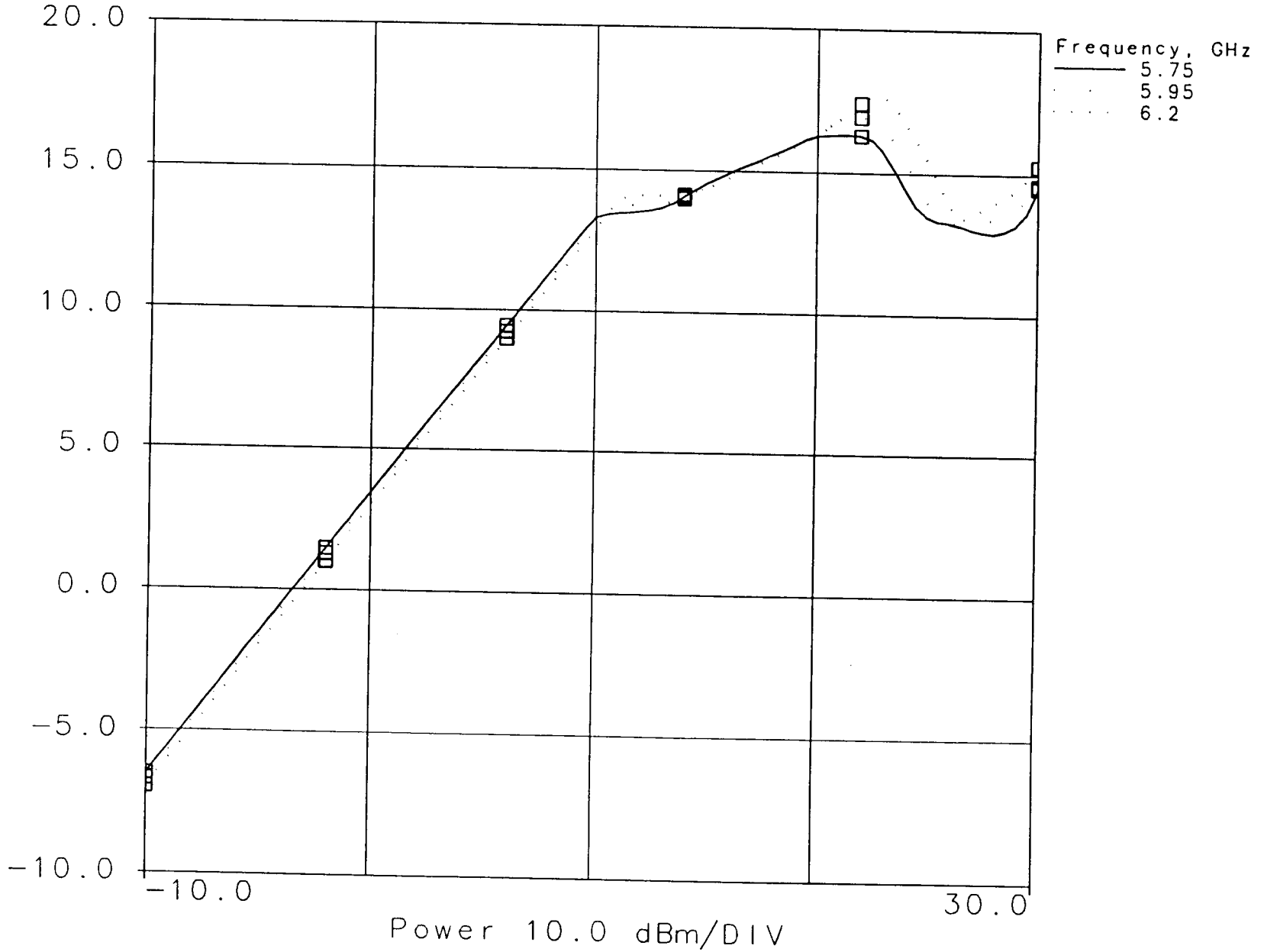
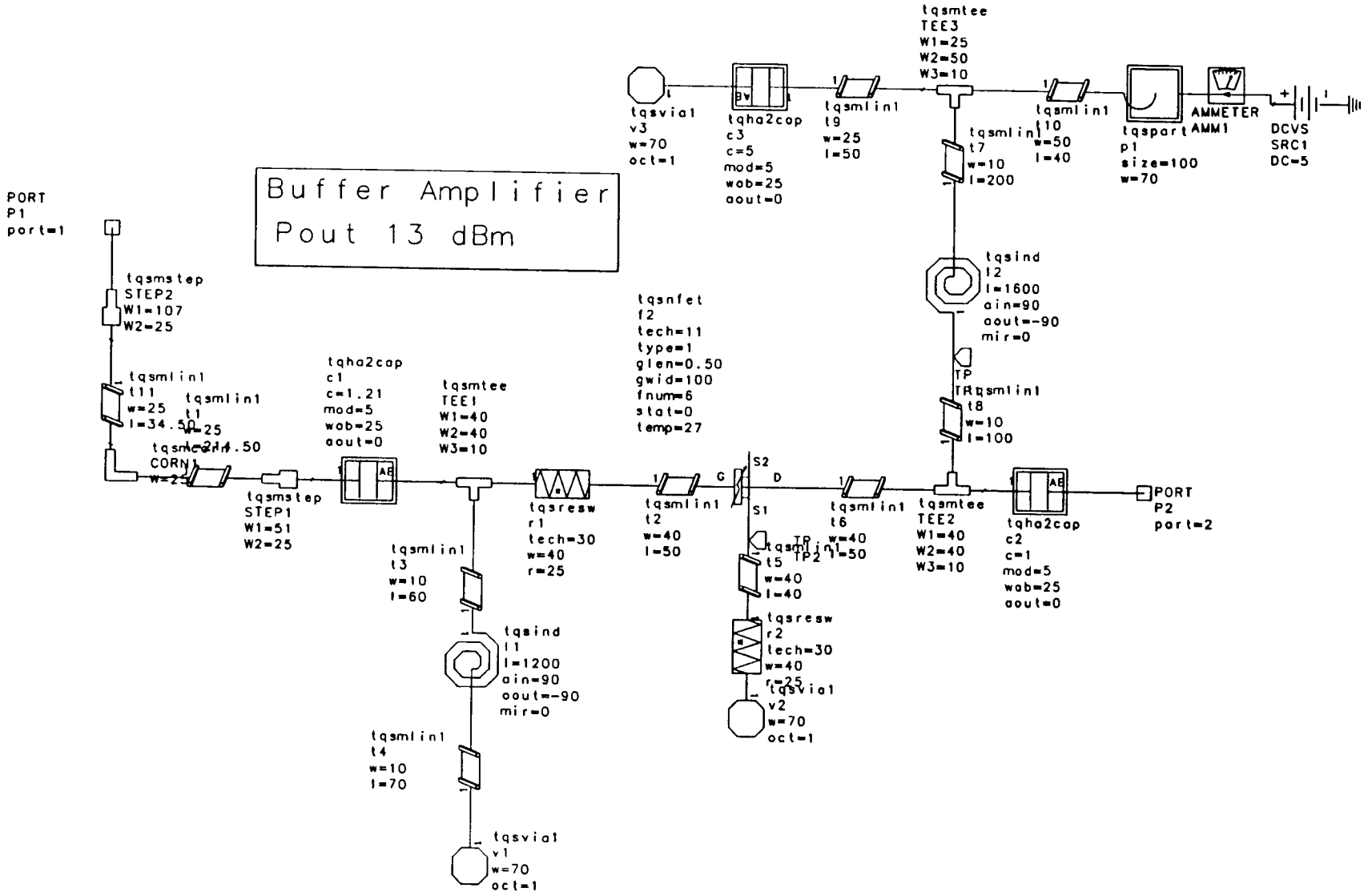


Fig 8.0


Buffer Amplifier
Pout 13 dBm
PORT
P1
port=1
tqsmstep
STEP2
W1=107
W2=25
tqsmlin1
t11
w=25
l=34.50
tqsmlin1
t1
w=25
l=24.50
tqsmcorn
CORN1
w=25
tqsmstep
STEP1
W1=51
W2=25
tqha2cap
c1
c=1.21
mod=5
wab=25
aout=0
tqsmtee
TEE1
W1=40
W2=40
W3=10
tqsmlin1
t3
w=10
l=60
tqsind
l1
l=1200
ain=90
aout=-90
mir=0
tqsmlin1
t4
w=10
l=70
tqsvia1
v1
w=70
oct=1
tqsresw
r1
tech=30
w=40
r=25
tqsnfet
f2
tech=11
type=1
glen=0.50
gwid=100
fnum=6
stat=0
temp=27
tqsmlin1
t2
w=40
l=50
G
S2
D
S1
tqsmlin1
t5
w=40
l=40
TP2
tqsresw
r2
tech=30
w=40
r=25
tqsvia1
v2
w=70
oct=1
tqsmlin1
t6
w=40
l=50
tqsmtee
TEE2
W1=40
W2=40
W3=10
tqsmlin1
t8
w=10
l=100
TP
TR
tqsind
l2
l=1600
ain=90
aout=-90
mir=0
tqsmlin1
t7
w=10
l=200
tqsmtee
TEE3
W1=25
W2=50
W3=10
tqsvia1
v3
w=70
oct=1
tqha2cap
c3
c=5
mod=5
wab=25
aout=0
tqsmlin1
t9
w=25
l=50
tqsmlin1
t10
w=50
l=40
tqspart
p1
size=100
w=70
AMMETER
AMM1
DCVS
SRC1
DC=5
tqha2cap
c2
c=1
mod=5
wab=25
aout=0
PORT
P2
port=2

Results

The design technique presented was solely base on linear analysis, however this type of design technique can be misleading. As stated earlier, the true frequency of oscillation can only be predicted form the circuit's large signal characteristics. HP/EESOF has devised a test mechanism by which the oscillation frequency of a device can be determine along with it's output power. Fig 7 through 11 represents the results of this test as plots of output power and oscillation frequency vs. tuning voltage. Fig 7.0 shows the test plan that was used to determine the frequency of operation and thee output power. Fig 8.0 shows the magnitude and angle of the open loop gain of the oscillator for different tunning voltages. The condition for oscillation is described when the magintude of the open loop gain is equal to one with a phase of zero. Note from the figure that the oscillation frequency is expected to shiff due to the fact that for all tunning voltages greater than zero the condition is not meet due to the fact that the maginitude is greater than one. Fig 9.0 show the output power as a function of frequency and tunning voltage. The power level appears to be very stable at around 12 dBm. Fig 12 - 13 represents the final schematic and layout of the Oscillator.

Fig 9.0

Oscillator Open Loop Gain Analysis

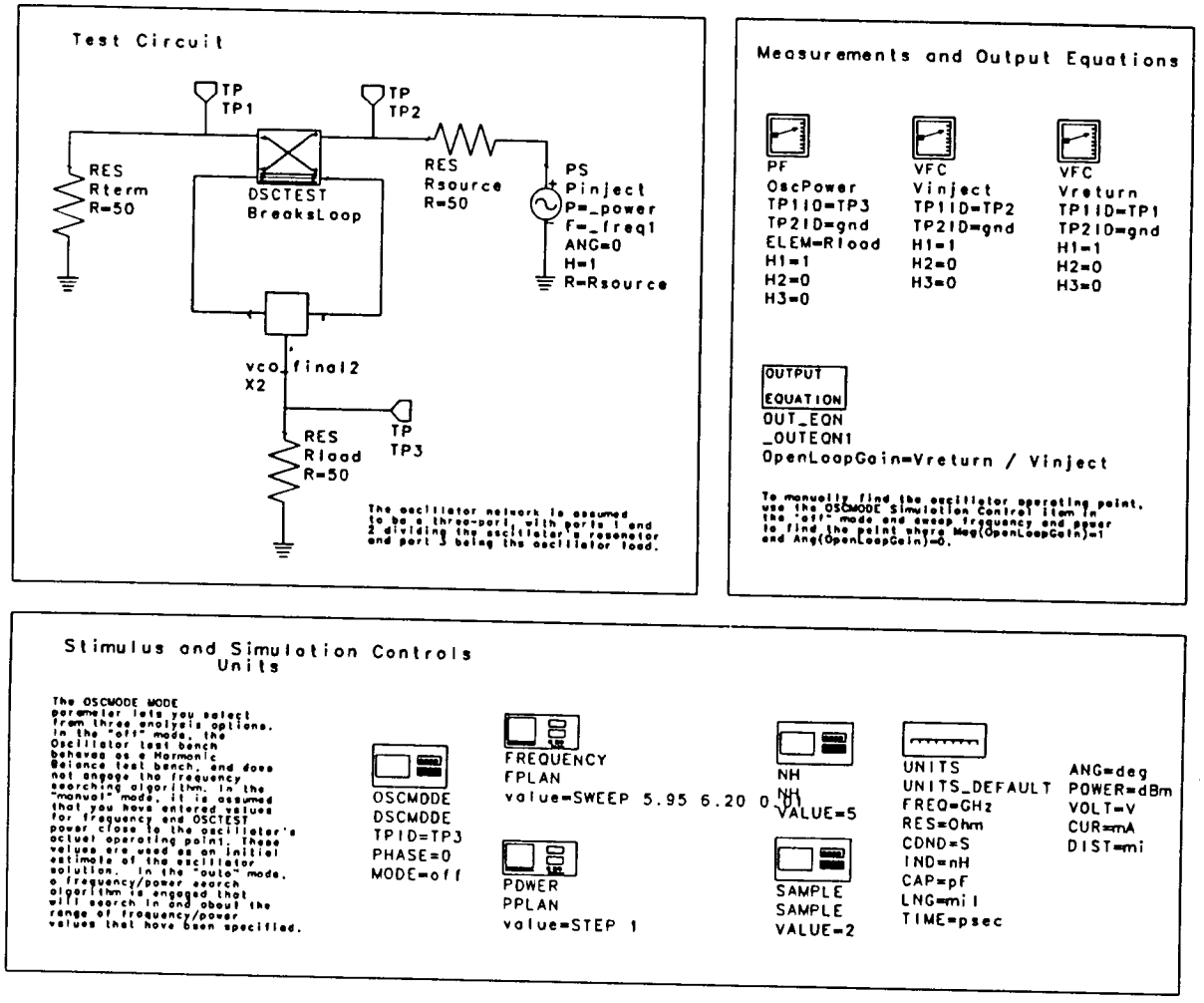
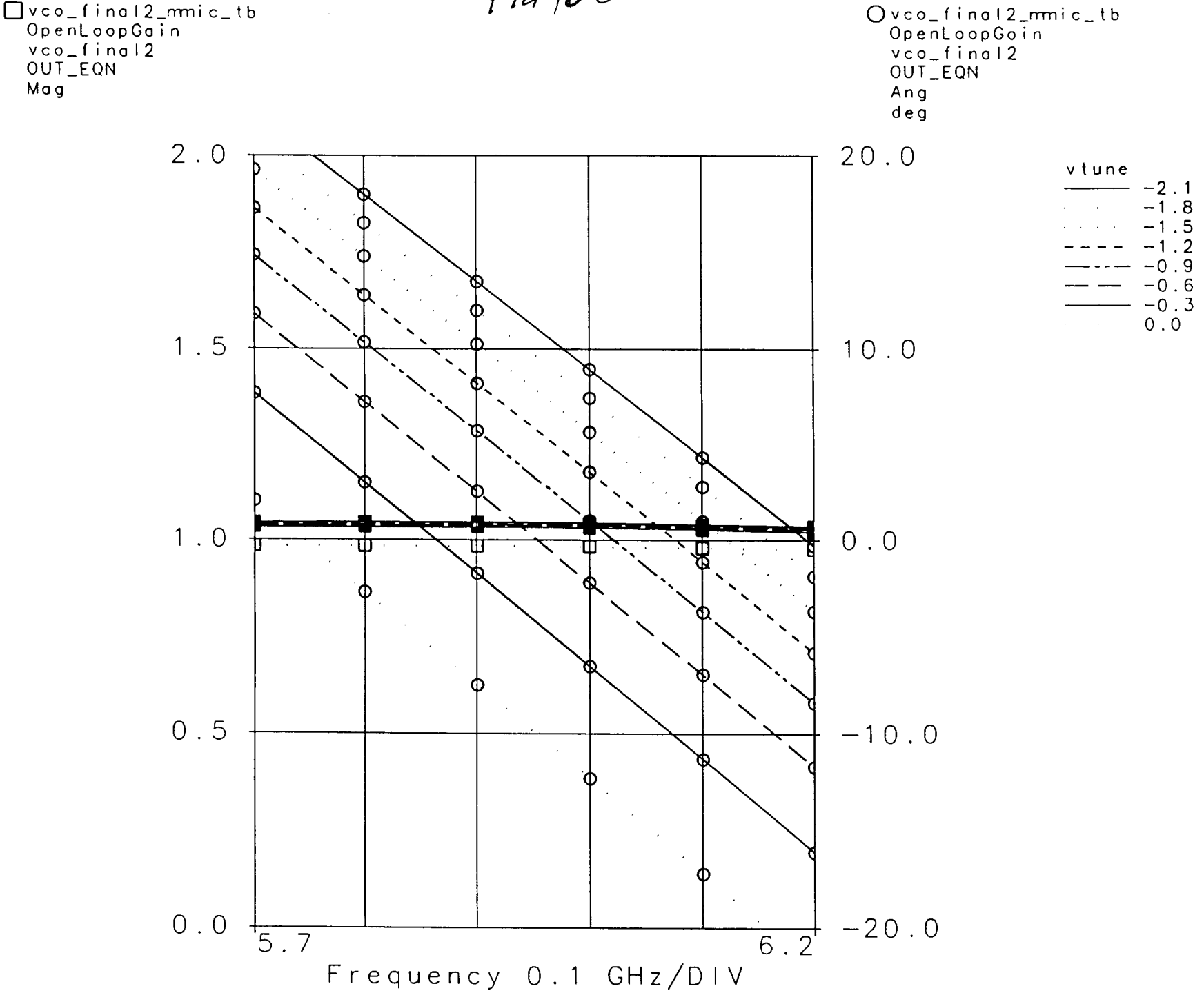


Fig 10.0


vco_final2_mmic_tb
OpenLoopGain
vco_final2
OUT_EQN
Mag
vco_final2_mmic_tb
OpenLoopGain
vco_final2
OUT_EQN
Ang
deg
vtune
-2.1
-1.8
-1.5
-1.2
-0.9
-0.6
-0.3
0.0
2.0
1.5
1.0
0.5
0.0
20.0
10.0
0.0
-10.0
-20.0
5.7
6.2
Frequency 0.1 GHz/DIV

vco_final2_mmic_tb
OscPower
vco_final2
PF
dBm

Fig A.0

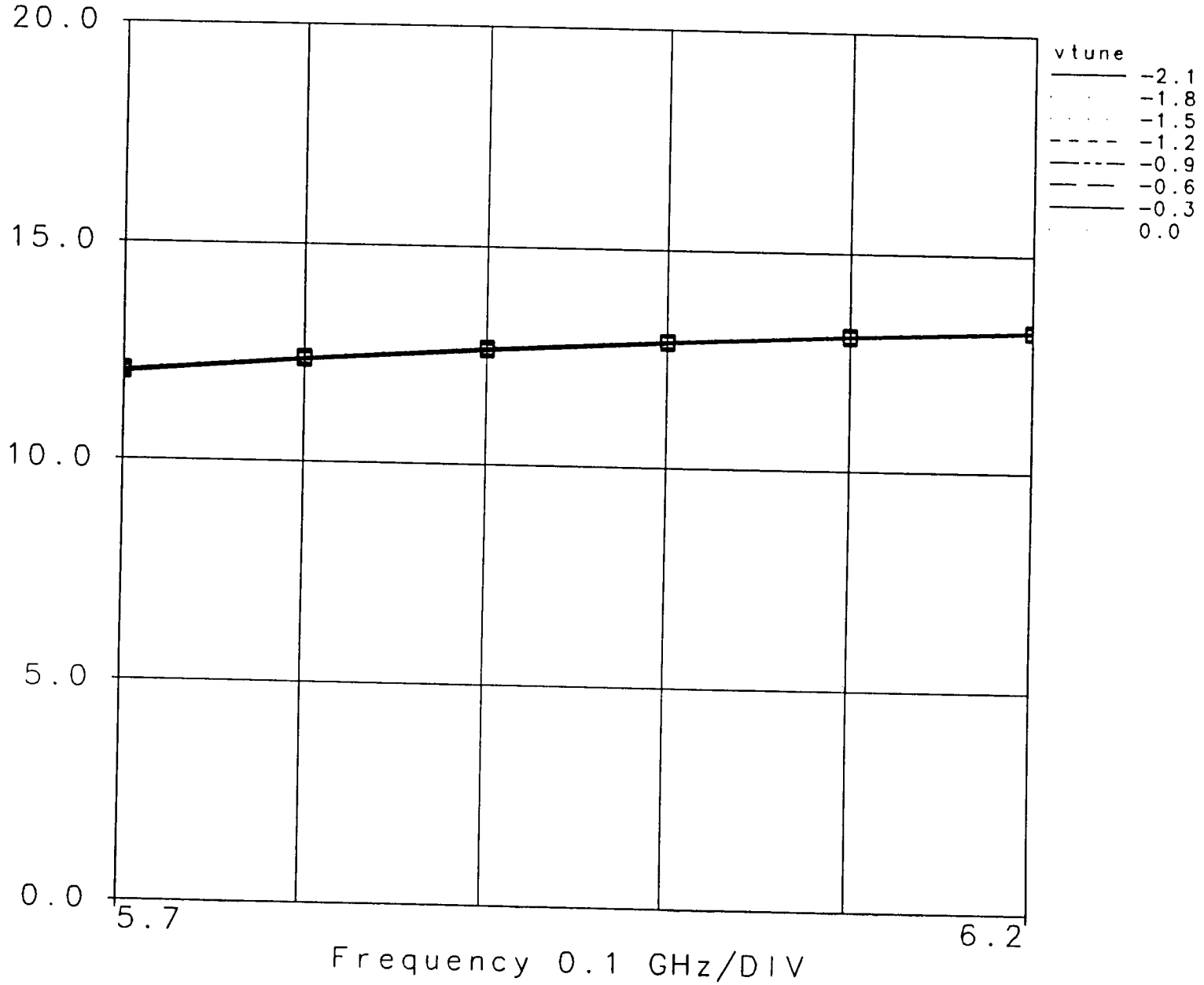


Fig 1B

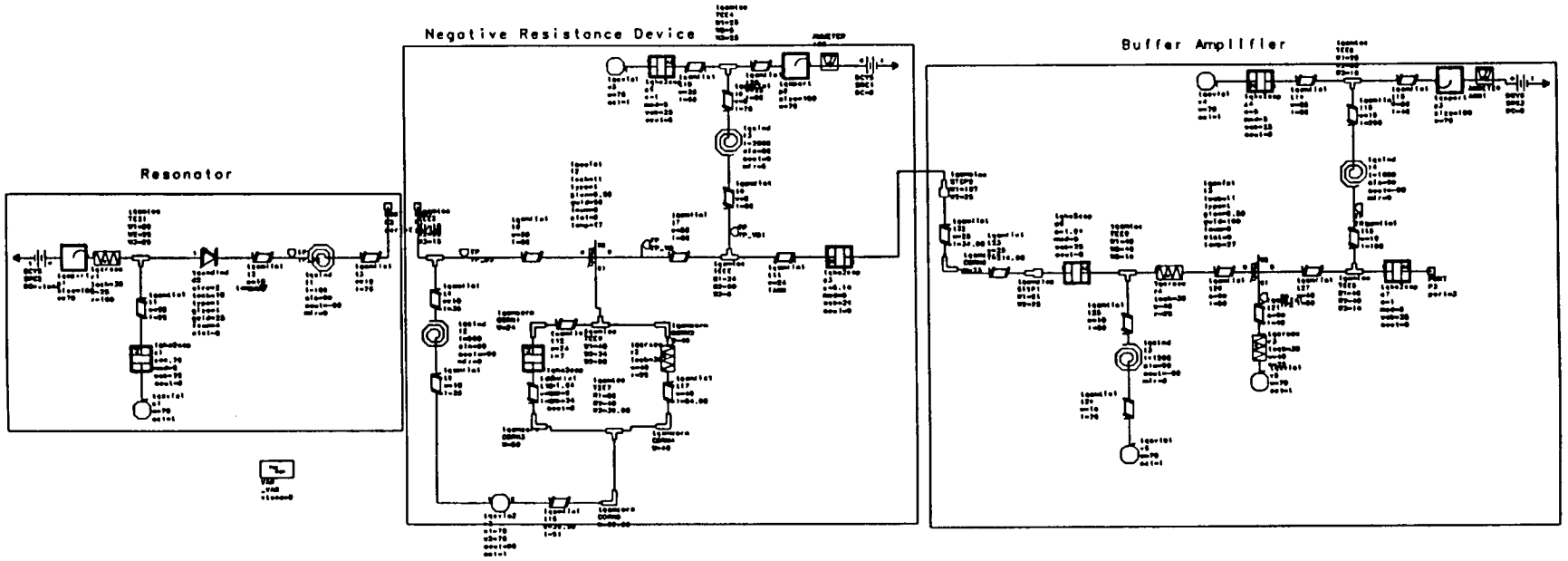
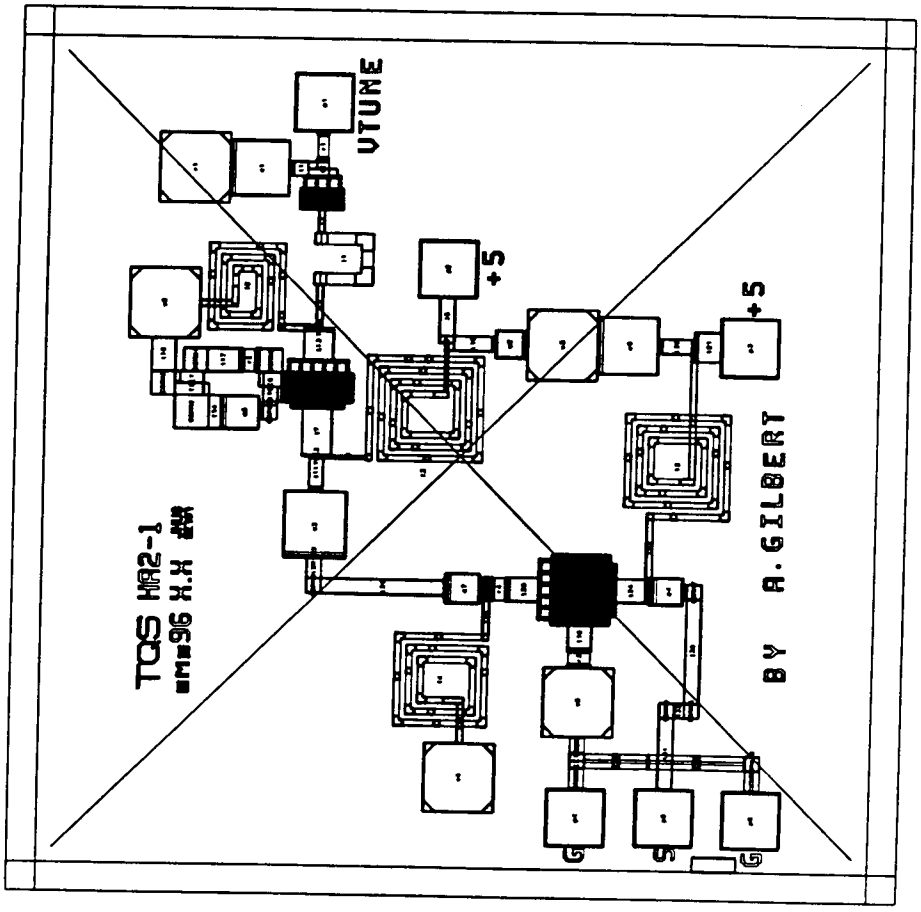


Fig 80



Conclusion & Recommendations

As set out, the design of a dual frequency oscillator was accomplished boosting an output power of 12 dBm using both small and Large signal criterion. The draw back to this design is the poor output reflection coefficient due to using a poer amlifier as the load. The output mach could possible be made a lot better by incorporating a impedance transform in the output, though this may have an effect of either decreasing or increasing the ouput power depending on amout of pulling envolved.

TEST PLAN

The DC biasing voltages are all indicated on the chip. The amplifier and the negative resistance device all require +5 volts dc.

Testing sholud commense as follows. The appropriate tuning voltage should be applied to the pad labled VTUNE, this voltage can range any where from 0 - (-2) volts. The output of the VCO should be connected to a spectrum analyzer to measure the output power and oscillating frequency. Table 1.1 show typical tunning range vs output power and frequency.

VTUNE	FO	POUT
0	5.75	
-0.3	5.87	11.38
-0.6	5.96	11.72
-0.9	6.03	11.92
-1.2	6.07	12.05
-1.5	6.12	12.144
-1.8	6.16	12.28
-2.1	6.2	12.5

4-

C-Band Down Converter

submitted by
Paul E. Laux

11 December, 1995

525.787 MMIC Design
C. Moore & J. Penn

Johns Hopkins University

I. Abstract

This project is part of a larger class project that the MMIC Design class is completing. When finished, individual projects will form a chip set for a C-band (5.7 - 5.8 GHz) wireless local area network (WLAN), A block diagram of the WLAN is shown in Figure 1.

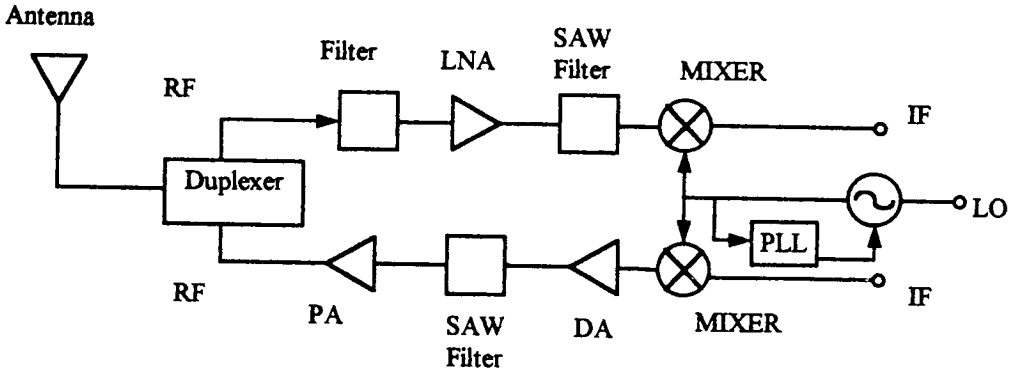


Figure 1. Block diagram of commercial transceiver, parts of which make up the class project.

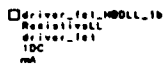
All MMICs will be fabricated using the TriQuint HA2 process, which is a gallium arsenide MESFET process utilizing a half-micron gate length.

II. Introduction

The design discussed in this paper is a down converter mixer, which was designed to convert a small RF receive signal between 5.725 and 5.875 GHz to an IF signal between 200 and 400 MHz using a high side LO signal ideally having 0 dBm of power but no more than +3 dBm. Along with other requirements discussed later, the complete circuit must fit onto a chip no larger than 60 mils by 60 mils.

The mixer used in this design is a FET drain mixer, having the RF fed into the gate, and the LO signal fed into the drain with the resulting intermediate frequency (IF) signal filtered off of the drain.

The non-linearity which provides frequency mixing in this configuration is that of the DC I-V curves near the knee voltage. As the LO pumps the drain, the source to drain voltage swings the FET in and out of saturation. Therefore, the best DC drain bias point is at the knee voltage, which for this particular mixer was +1.3 volts, as seen on the I-V curves in Figure 2. These curves were simulated using the Triquint Own Model (TOM),



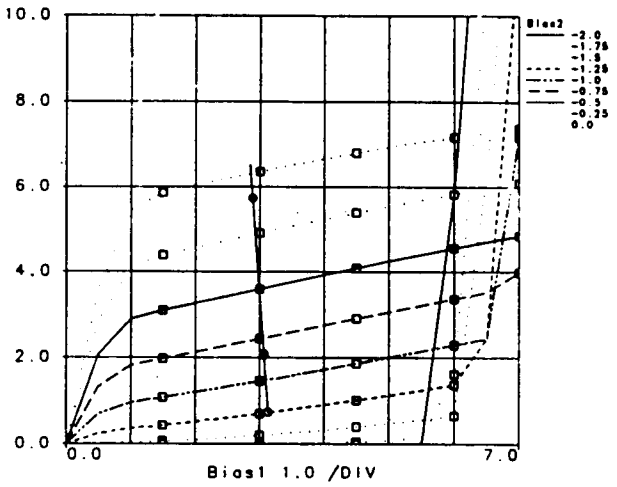


Figure 2. DC I-V curves for a 0.5µm FET having a total gate width of 60 µm.

As the TOM model tends to be most accurate at low drain-source voltages and currents close to Idss, ~~a bias~~ biasing was chosen to try ~~and~~ to maximize conversion gain and at the same time stay within the more accurate regions of the model.

It is important in any mixer design to minimize the LO leakage to the RF circuitry and vise versa. Therefore, to effectively isolate the two signals, the matching networks for the two signals must make the RF frequency on the gate look like a short to the LO frequency on the drain. Likewise, the LO must also look like a short to the RF frequency. And of course, the IF must be effectively filtered out and isolated from the LO frequency, as the two ports are connected to the FET drain. Since the RF and LO frequencies were so close, isolating the two was not as effectively accomplished as if a higher IF frequency been needed. One possible remedy would have been to use a higher LO frequency, say 11.8 to 12.1 GHz, and filtering out the (LO - 2RF) harmonic. This would have made isolating

the LO to RF an easier task, and the resulting IF would have remained the same. This too might have had its own complications, however.

During preliminary design stages, using ideal lumped elements to design the matching networks, it appeared that a LO power between 10 and 12 dBm would be more desirable than the 0 to 3 dBm LO power allowed in the design specification. Therefore, in order to better pump the mixer, a driver amplifier was designed and included in this circuit. This high impedance driver amplifier which had a total gate width shorter than that of the mixer FET was used to boost the LO power up by 7 to 8 dBm. More power could have been used, but to minimize circuit complexity and still meet minimum circuit performance, this amplifier was deemed adequate.

III. Schematic Diagrams & Modeled Performance

Table 1 below lists all of the mixer circuit specifications, as well as those achieved in the modeled prediction.

Table 1	Minimum Performance Required	Optimum Design Goal	Achieved in Simulation
Frequency	RF=5.725 to 5.825, LO=High side, IF=300MHz, 200 to 400 MHz goal.		
Signal Bandwidth	±5 MHz	--	±2.5
LO/RF Isolation	10 dB	16 dB	8.6
Conversion Loss	6 dB	3 dB	5 or 4.5
LO Power	+3 dBm	0 dBm	0 dBm, but +3 works better
VSWR	2.5 : 1	1.5 : 1	1.58
Supply Voltage	+ and - 5 volts	+5 volts only	-0.5, +1.3, +3.5
Size	60 mils by 60 mils		

Figure 3 shows the basic schematic mixer design using mostly ideal connections and lumped elements, and a minimum number of microstrip lines to make the

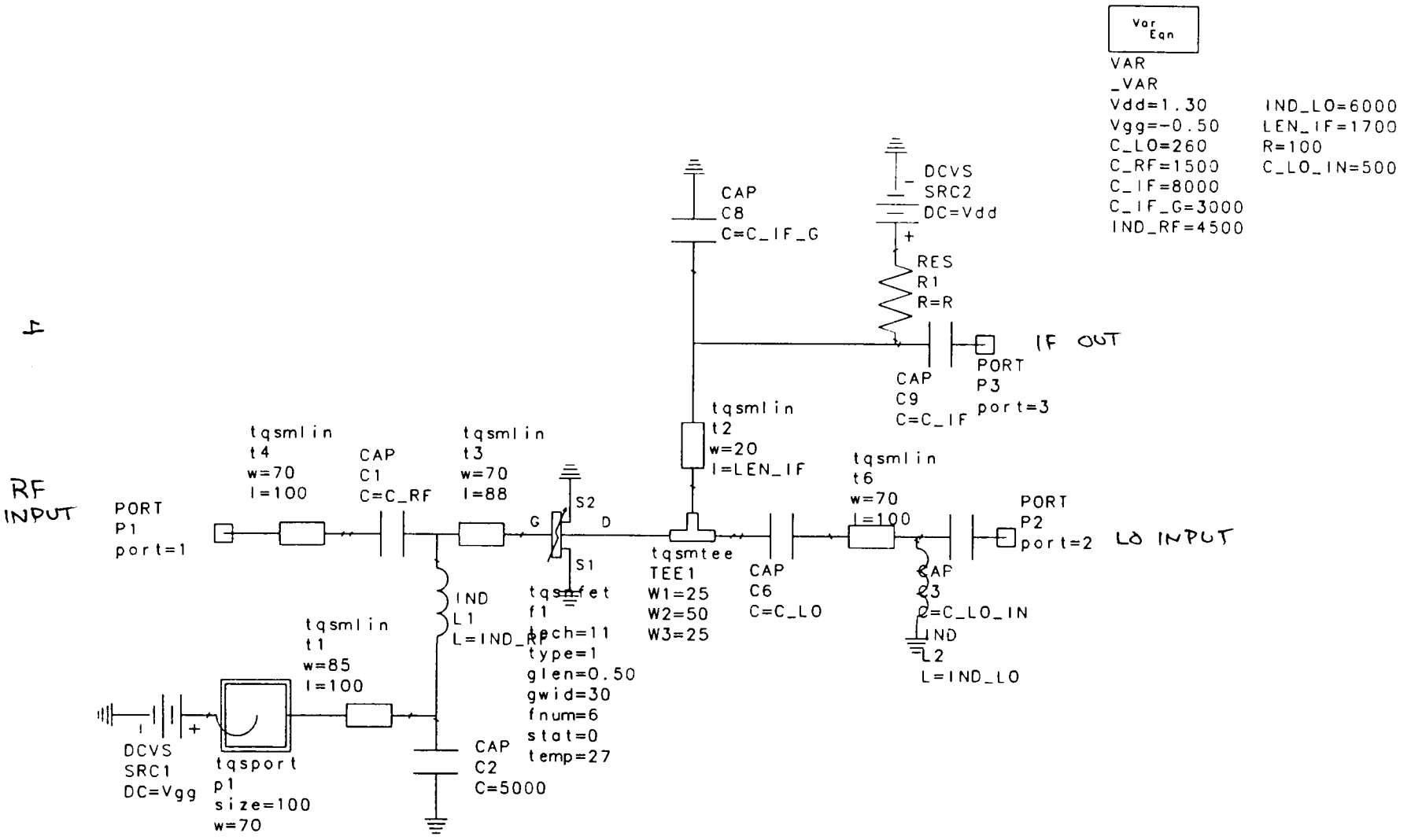


Figure 3. Initial mixer design using ideal lumped elements for matching.

circuit functional. This circuit as shown was able to achieve a 0 dB conversion gain using a LO power of about 10 to 12 dBm. When this circuit was combined with the driver and re-optimized, as shown in Figure 4, the result was then a conversion loss of about 1.5 dB. This was using a 0 dBm input to the LO buffer amplifier.

Figure 5 shows the final circuit schematic used to produce the layout, using all TriQuint elements. At center frequency, this final circuit simulated a conversion loss of 5 dB using 0 dBm LO input (see Figure 6), and 4.5 dB conversion loss when using a +3 dBm LO input. This large degradation in simulated performance is mostly due to making the final layout easily testable and compact. Also, this mixer shows to have very narrow band characteristics, as seen in Figure 7. This is due to the narrow-band input matching of both the RF and LO frequencies. With more time, this may have been corrected. The rest of the results are given at the center of the frequency band, RF = 5.8 GHz. Figures 8a and 8b show the IF spectrum using both 0 dBm and 3 dBm LO powers, respectively.

The LO to RF isolation was simulated to be about 8.5 dB, as shown as "M1" in Figure 9. This parameter misses the minimum specification of 10 dB.

The VSWR simulation, however, was simulated to be about 1.58, which exceeds the design minimum and is very close to design goal. The plot of VSWR is shown in Figure 10.

Figure 11 shows the final chip layout with all inputs and output marked. Note that both the LO driver amplifier, and the mixer FET use the same gate bias and therefore were connected together using airbridged metal. The drain biasing on the two FETs are separate.

It is a concern that the narrow bandedness of this design might cause the optimum center frequency to vary from chip to chip when small process variations are introduced.

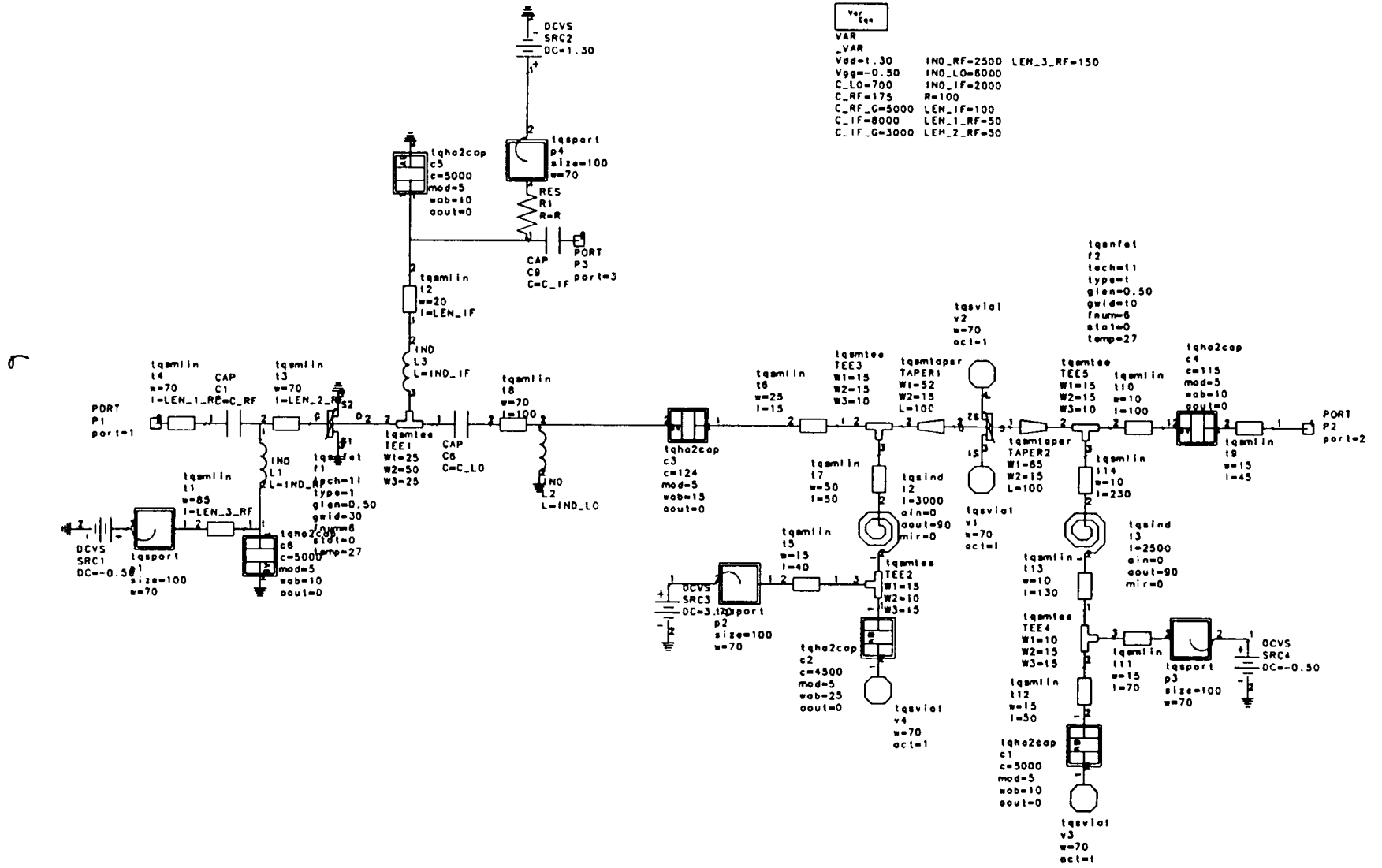


Figure 4. Same mixer in Figure 3 having LO driver FET added.

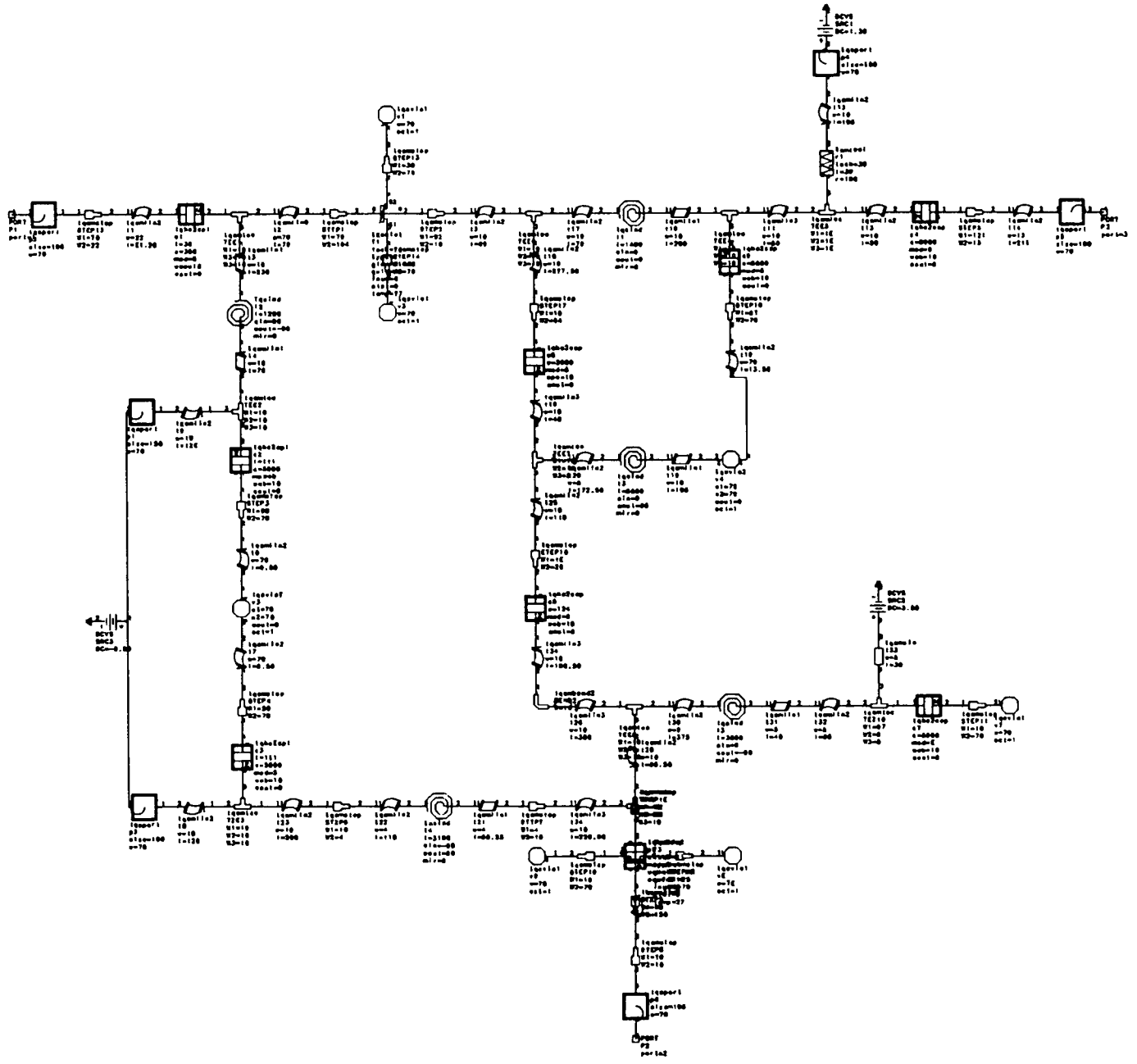


Figure 5. Scematic of final mixer circuit using all TriQuint elements

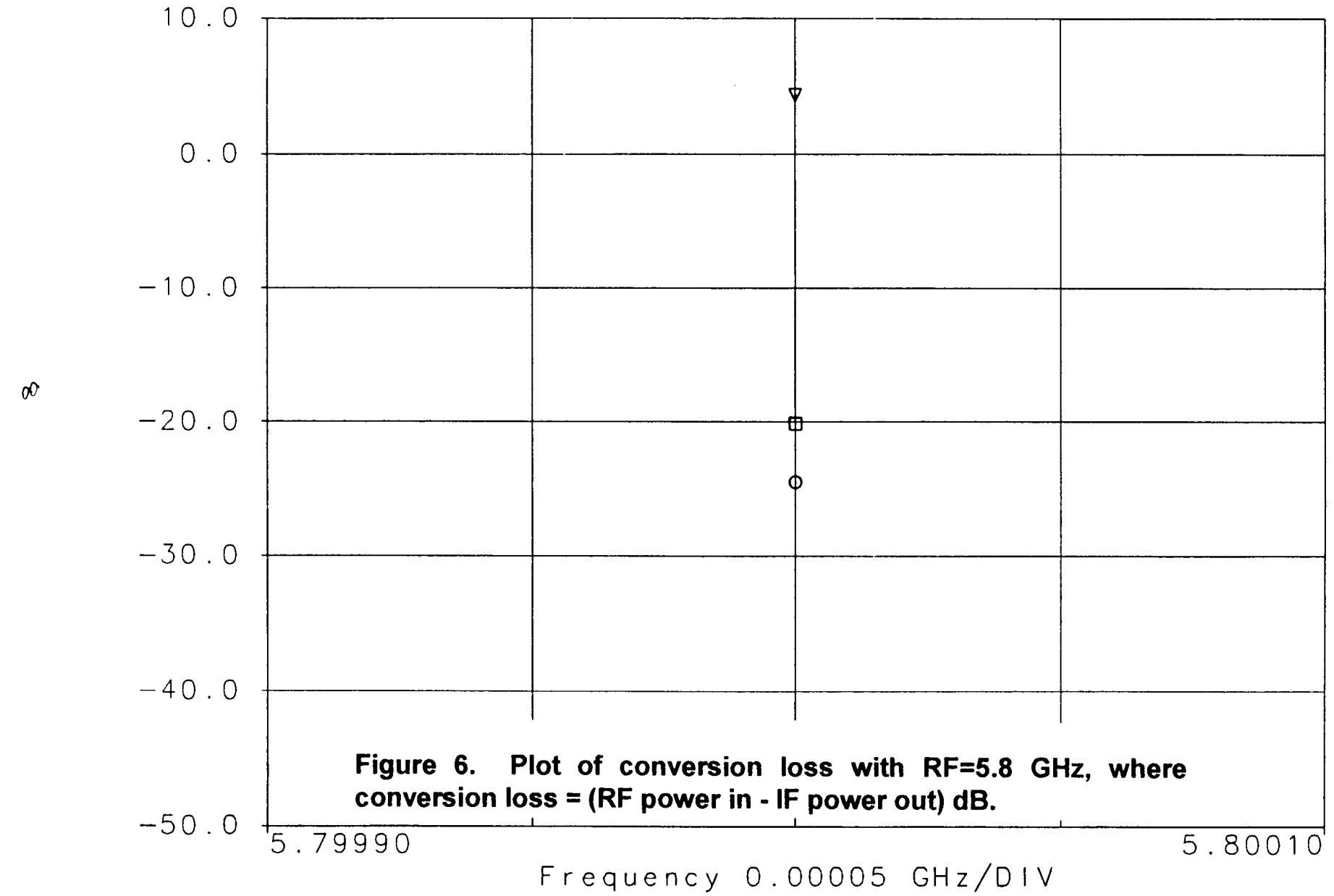


Figure 6. Plot of conversion loss with RF=5.8 GHz, where conversion loss = (RF power in - IF power out) dB.

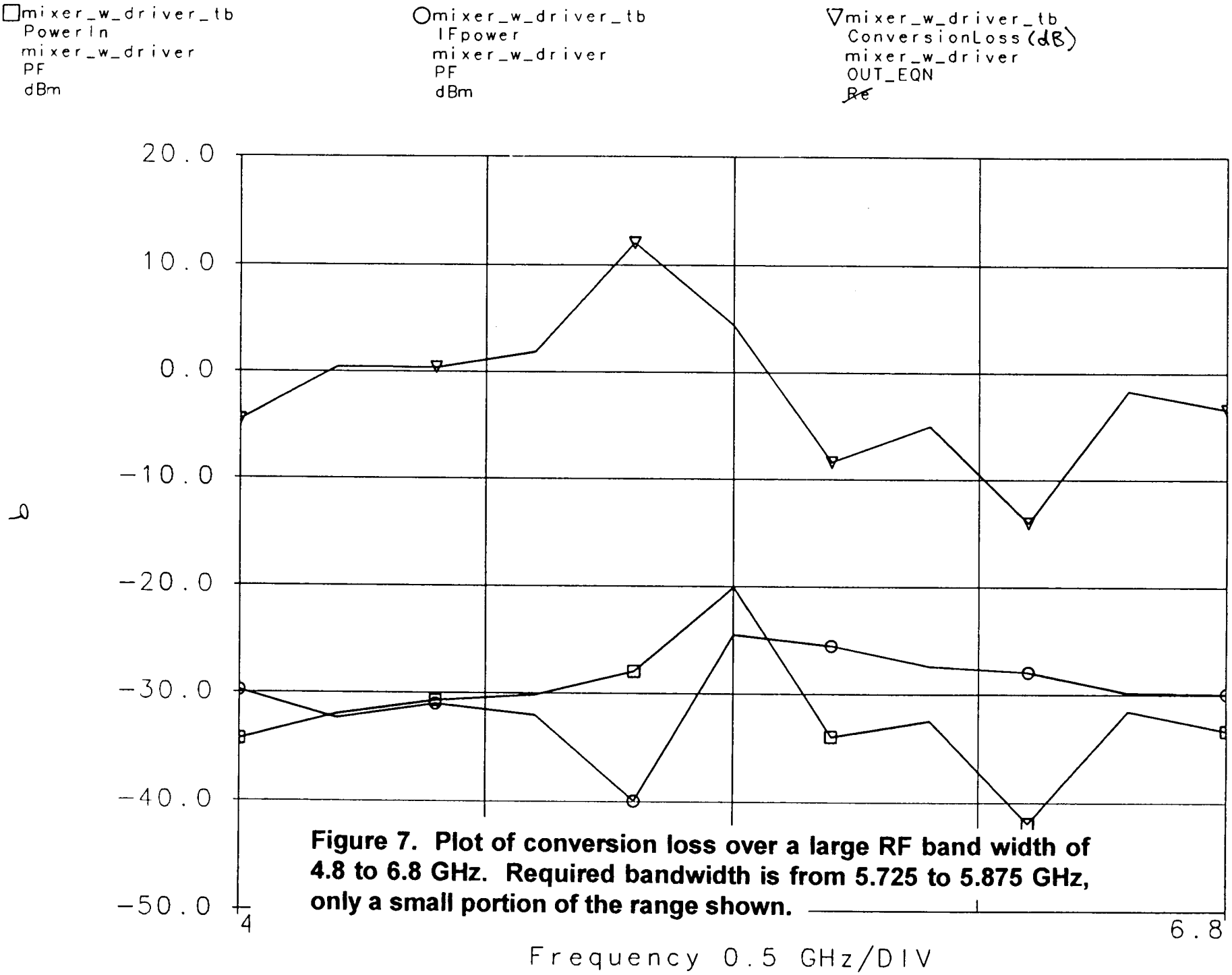
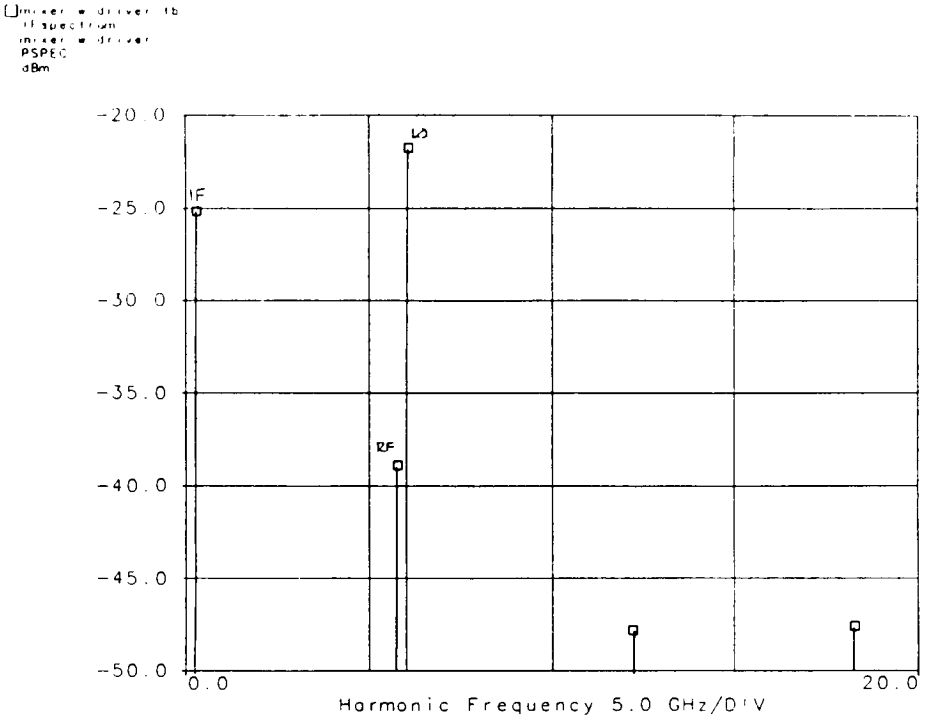
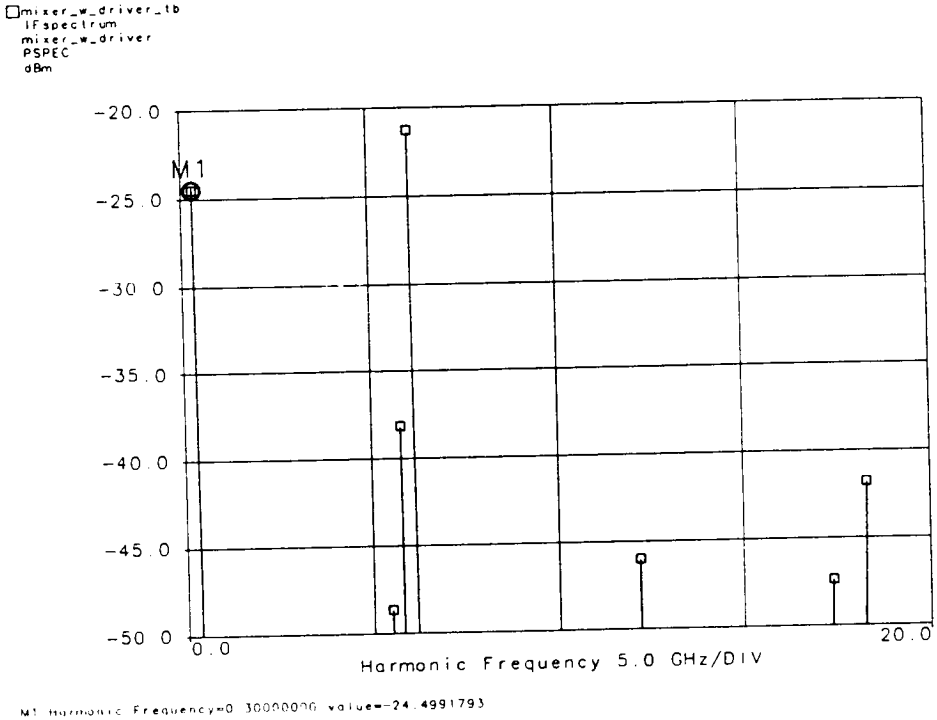


Figure 7. Plot of conversion loss over a large RF band width of 4.8 to 6.8 GHz. Required bandwidth is from 5.725 to 5.875 GHz, only a small portion of the range shown.

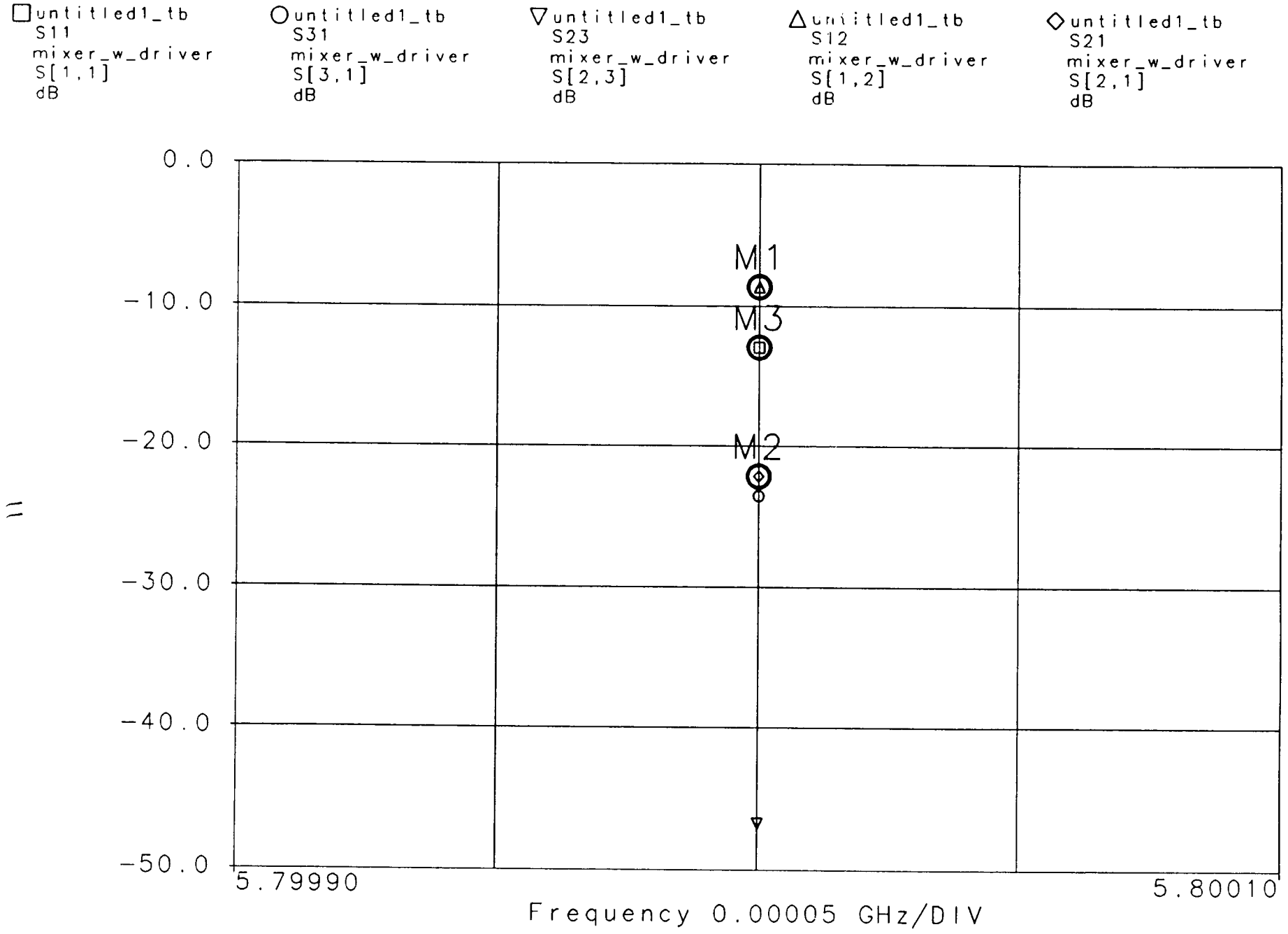


(a)



(b)

Figure 8. (a) IF spectrum at RF= 5.8 GHz and high side LO with 0 dBm input power. (b) IF spectrum at RF= 5.8 GHz and high side LO with +3 dBm input power.



M1 Frequency=5.80000000 value=-8.63173988
M2 Frequency=5.80000000 value=-22.1590730
M3 Frequency=5.80000000 value=-12.9516345

Figure 9. Point marked "M1" designates LO to RF isolation of 8.6 dB.

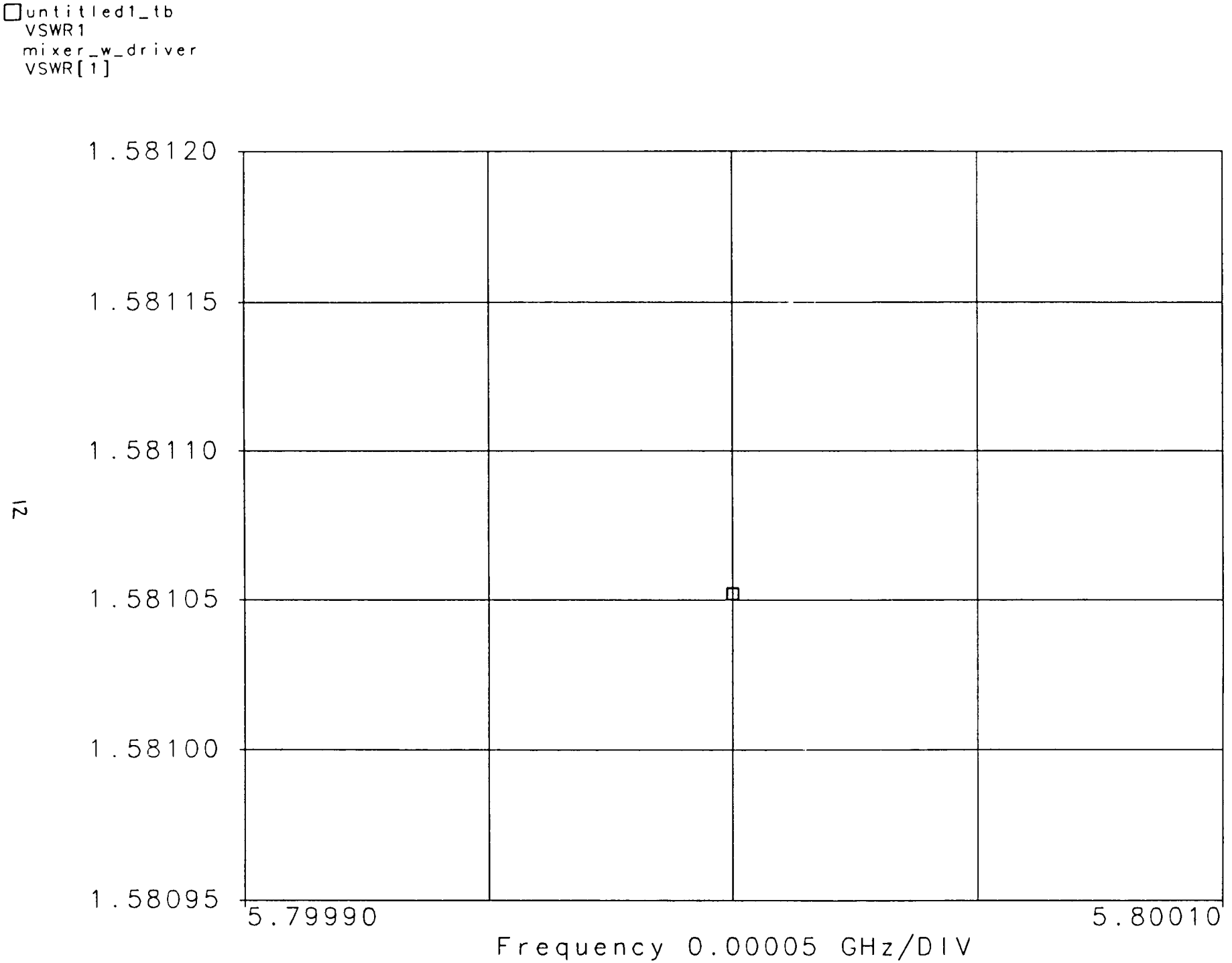


Figure 10. VSWR of mixer, approximately 1.58 : 1.

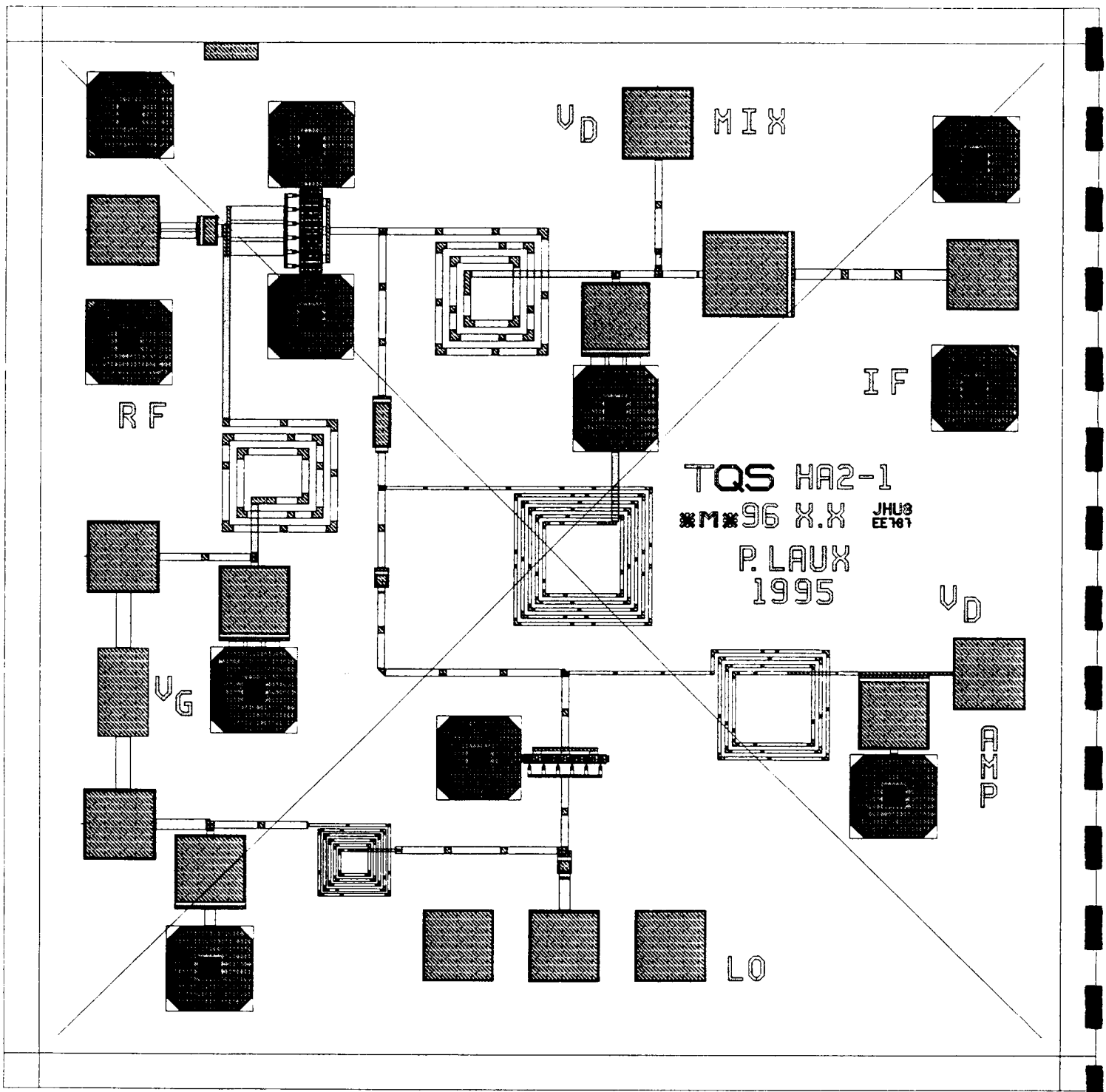


Figure 11. Final layout of mixer chip, note all ports and bias points are mark accordingly.

IV. DC Analysis

Three DC voltage sources are needed to bias this mixer: one of -0.5 volts for the combined gate biases, another of +3.5 volts for the drain of the driver FET, and a third of +1.3 volts for the drain of the mixer FET. The airbridges connecting the gate bias pads may be broken during testing if needed. Referring back to the I-V curves for the 60 μm driver FET in Figure 2, a current of about 3.5 mA is produced at V_{ds}=3.5 volts and V_{gg} = -0.5 volts. The narrowest path which must handle this current is 4 μm of metal one. The design rules for this layer specifies no more than 9 mA/μm width. This width will easily carry the 3.5 mA current.

Scaling these I-V curves up to the 180 μm gate width of the mixer FET, the Ids at V_{gg} = -0.5 volts and V_{ds} = +1.3 volts is 9 mA. The narrowest metal path which has to carry this current is 10 μm. This too will easily carry the 9 mA current. The 100-Ω resistor used in the mixer drain biasing network is approximately 50 μm wide and has a maximum current carrying limit of 1 mA/μm width. This resistor will therefore carry up to 50 mA of current and therefore is also well within the maximum current limits.

V. Test Plan

To test this mixer, the three DC biasing sources are needed, as well as two frequency synthesizers and a spectrum analyzer. The DC voltages are to be applied accordingly using needle probes. -0.5 volts should first be applied to the gate bias pad marked V_G, +3.5 volts can then be applied to the bias pad designated as "V_D AMP," and ~~+1.5~~ 1.3 volts can be applied to the bias pad designated as "V_D MIX." Connect the RF input pads to one of the frequency synthesizers via G-S-G probes. Connect the other frequency synthesizer to the LO input pads, also via G-S-G probes. The IF output should be measured using the spectrum analyzer connected to the IF port via a third set of G-S-G probes. An RF signal of 5.8 GHz with a power of -20 dBm and an LO signal of 6.1 GHz and 0 dBm power should be applied. Center the spectrum analyzer

measurement at 300 MHz and measure the strength of the resulting IF. The DC bias voltages can be varied somewhat to maximize the IF signal strength if needed. The LO frequency should be varied higher and lower by 100 MHz to measure IF frequencies of 400 and 200 MHz. The RF bandwidth should be measured by moving the RF frequency from 5.725 to 5.875 in increments while maintaining the LO at RF + 0.3 GHz. At each RF frequency tested, LO powers of both 0 dBm and +3 dBm can be used to test the improvement of increased LO power. Finally, if the mixer does not seem to be working properly, the gate biasing may be separated by breaking one of the airbridged connections between the bias pads. A fourth DC voltage source may then be used to bias the gates separately.

VI. Conclusions

This design project was difficult to get working within specified parameters, several of which were not met once put into final layout. If I were to do this type of circuit again, I would work directly with the layout and simulate from there. This is possible with the Libra software. If there seemed to be some fundamental problems with the design, only then would I go to the schematic mode and use ideal elements to work out the problems.

I think that if a mixer is to be designed next year, an interesting approach might be to try a singly balanced FET mixer. With the increased amount of circuitry needed, the student might use as much direct LO power as needed within reason, say 12 to 15 dBm.