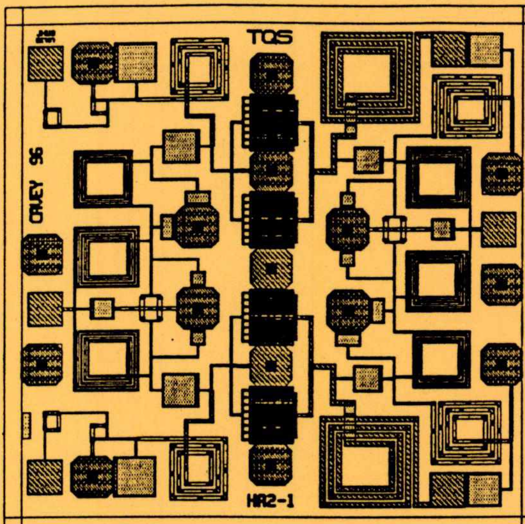
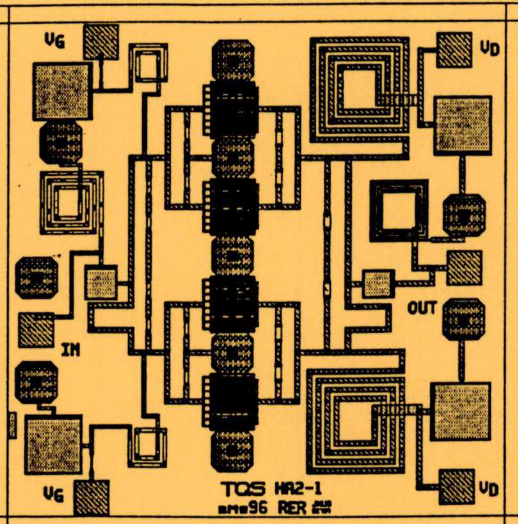
John Penn

MMIC DESIGN FALL 1996 STUDENT PROJECTS

JOHNS HOPKINS UNIVERSITY

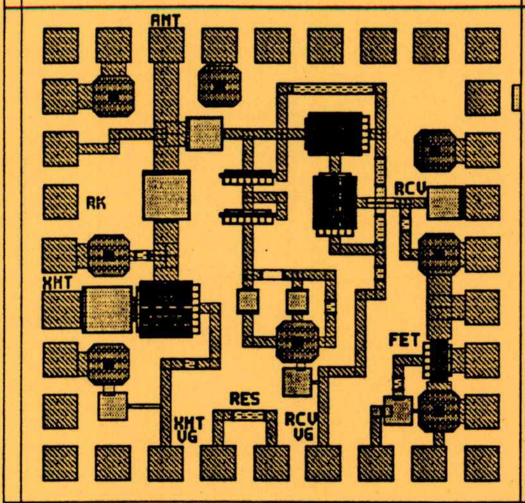
1 WATT POWER AMP
J. CAVEY

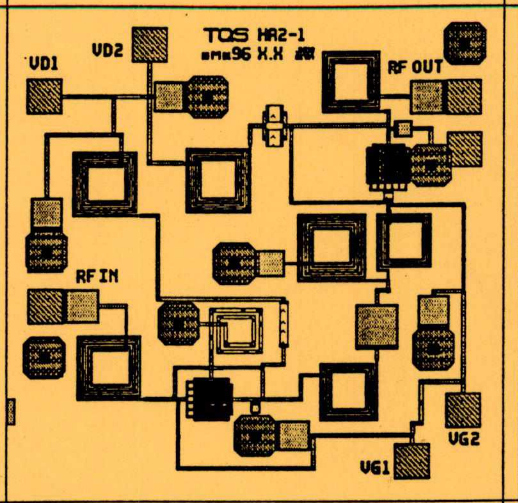




1 WATT POWER AMP
R. RODDEWIG

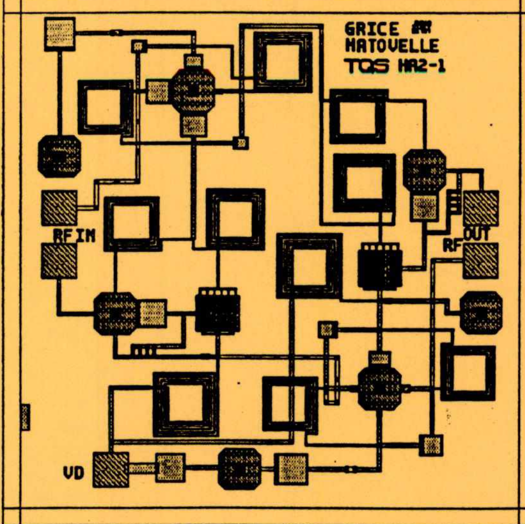
1 WATT SPDT SWITCH
R. KAUL

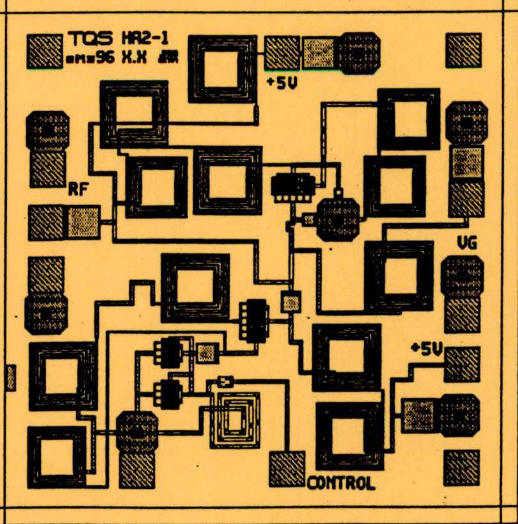




HIGH IP3 LNA
M. DIPPLOD & J. MIKINA

50 mW DRIVER AMP
N. MATOVELLE & S. GRICE





VCO
A. SHERIF & M. GORBETT

2.4 GHz ISM BAND CHIPSET in TRIQUINT HA2 PROCESS
for RADAR INTRUSION ALARM or WLAN TRANSCEIVER

MMIC Design Project

EE 787 Fall of 1996

Power amplifier design for use in the 2.4GHz ISM band

Robbin Roddewig

1. Summary

The following design was created for the Johns Hopkins MMIC course using the Triquint simulatable art work elements and Libra Series 4. The design is being submitted to Triquint for fabrication. RF testing will be performed in the summer of 1997 and the results will be added in an addendum to this report.

The power amplifier has a design requirement of 500 mW output power and a goal of 1 watt power out. The design was accomplished using four parallel FET's of 1000 micron periphery each and combing the outputs of the FET's in a reactive power combiner network. Based on matching for power the four FET's can supply over a watt of RF power at 2.4 GHz. Due to return loss constraints the power out of this design was reduced to a predicted 800 mW.

2. Introduction

The power amp is comprised of four eight fingered FET's with gate widths of 125 microns. Each FET is capable of providing 375 mW ideally based on the IV curves for the devices. This would give an ideal power out of 1.5 Watts with ideal power match, lossless components and no reactance in the FET.
The power amp design philosophy is to match the output for maximum power out using an approximate linear method called the Cripps method. In the Cripps method the linear S22 parameter of the device is analyzed and an equivalent model of the output is generated. The output resistance and reactance for an FET are comprised of the shunt resistance Rds and the shunt capacitance Cds. The current voltage curves (IV) of the FET are examined and based on a maximum RF power swing the quiescent bias is determined. An optimum load line is graphed which represents the best load for power out. The reactance of the drain shunt capacitance is canceled with a shunt inductor designed to resonate at the frequency of interest. The output matching network is then created to present the impedance to the drain which was found from the IV curves to maximize the RF power out. With the output matched the input is conjugately matched for good input return loss.
The match for the optimum power out may not be a good match to 50 ohms in which case the output return loss performance is traded for power out. Such was the trade done for this design.

3. Specifications

The required power amp performance and performance goals are shown in table 1.

Table 1

Parameter	Requirement	Goal	Design
Frequency	2400 - 2483 MHz		comply by design
Bandwidth	> 83 MHz		> 200 MHz predicted
Power gain @ P1dB	> 10 dB	> 13 dB	> 15 dB
Gain ripple	+/- 0.5 dB max		< 0.2 dB in band
Output Power @ P1dB	> 27 dBm	30 dBm	29 dBm
Efficiency	> 15 %	> 25 %	> 50 % predicted
VSWR	1.5:1 (-14 dB RL)		<-15 dB input <-10dB output
Supply voltage	+/- voltage supply	+ supply only	+ and - supply required
Size	60 x 60 mils Anachip		comply by design

4. Design Method and Modeled Performance

The IV characteristics of one of the 1000 micron FET's is shown in figure 1. The maximum voltage swing is approximately 12 volts and the maximum current swing is 250 mA. The rms power from these numbers is 375 milliWatts. An optimum load line drawn from the upper left corner of the IV curves to the lower right corner shows that a load of 44 ohms will give the best power out. 44 Ohms is the best trade off between voltage limiting near Vds=0 and current limiting at Ids = 0. The 44 Ohm load is the best output impedance to present to the drain for maximum power out. However in order to present a real impedance of 44 Ohms the reactance of the drain to source capacitance must be tuned out with a shunt inductor of appropriate value such that it resonates with the capacitor at the frequency of interest. The equivalent circuit for the FET drain is shown in figure 2. At 2.4 GHz an inductor of 9500 pH will resonate with the 0.55 pF capacitor. This inductor was also used as the RF choke for the drain bias. Since four FET's or two pairs of FET's are being used for the amp the drain inductors were combined into two inductors of 4500 pH each one on the top of the chip and one on the bottom of the chip to allow for putting multiple chips next to each other and jumpering the bias voltages from one chip to the next.

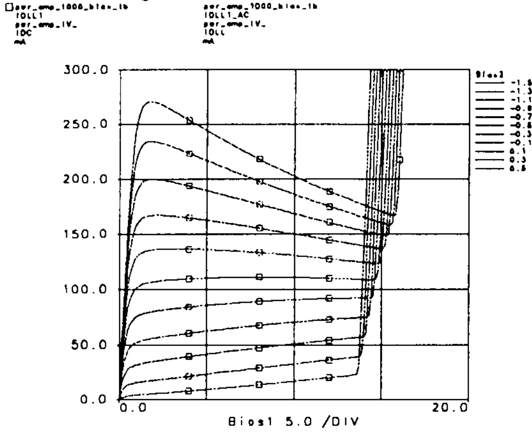


Figure 1 FET DC IV curves predicted with HA2 model

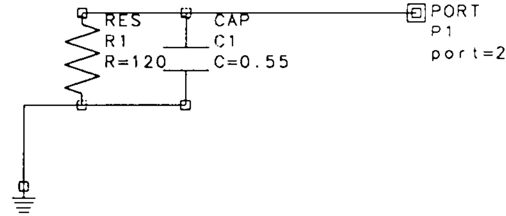


Figure 2 1000 micron FET output equivalent circuit

With the drain reactance resonated out an output matching network was designed that presented 44 Ohms to each FET or 11 Ohms to the four FET's in parallel. The output matching network consists of a series cap which also acts as a DC blocking cap and a shunt inductor. Various output matching networks were examined however a higher order matching network did little for the bandwidth. The input was conjugately matched and the performance simulated with ideal lumped elements. The power out was well over 1 Watt and the power added efficiency was 70 %. The gain was 16 dB in the band of interest. However the return loss was about -10dB on the input and -6 to -8 dB on the output. The output return loss was considered a problem. The output matching circuit was tuned with the input matching circuit to give a more acceptable return loss. The final circuit schematic is shown in figure 3. Figure 4 shows the layout of the final circuit including

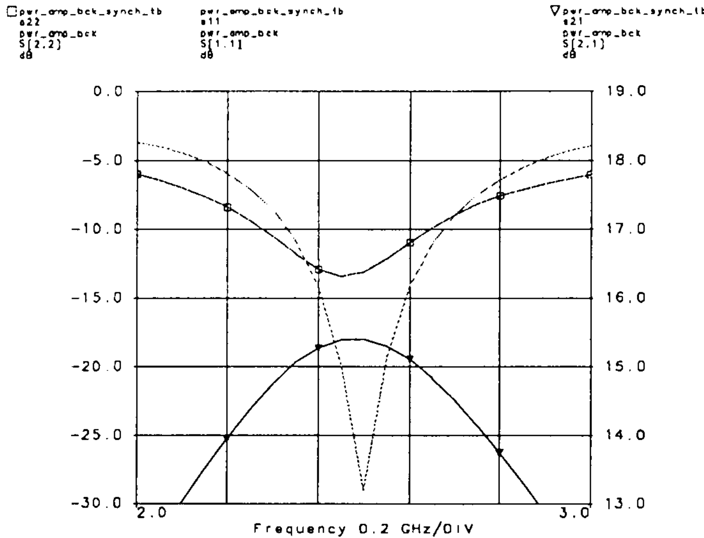


Figure 5 Predicted Gain and return loss

the probe pads and gate and drain bias pads. The predicted gain and return loss is shown in figure 5. The predicted 1 dB compression point and corresponding power out are shown in figure 6. The power added efficiency is shown in figure 7. A dc bias check was performed using the nonlinear model of the FET and ideal voltage supplies at the bias voltage input pads of the circuit. Voltage test probes were placed at the drain and gate of the FET's. The desired quiescent drain voltage is +7 volts and the desired gate voltage for 60 % Idss is -0.5 volts. The probes showed that the voltage at the drain pad needed to be raised to 7.8 volts to achieve 7 volts at the drain of the device. The gate bias voltage was essentially the same as that at the gate bias pad as shown in figure 8.

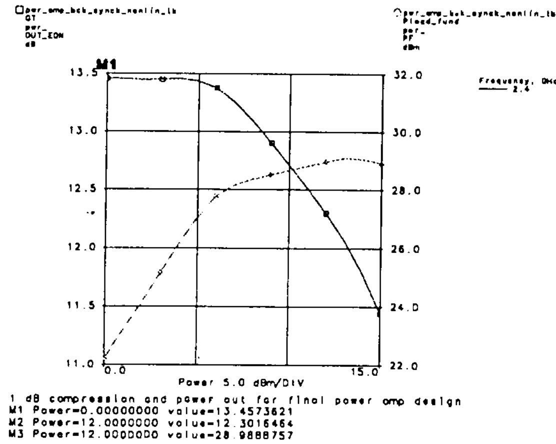


Figure 6 1 dB compression and power out

V_drain	Vgate
VFC Re V	VFC Re V
7.1676	-0.4973

Figure 8 Bias voltages at the drain and gate for -5v at the gate bias pad and +7.8 v at the drain bias pad.

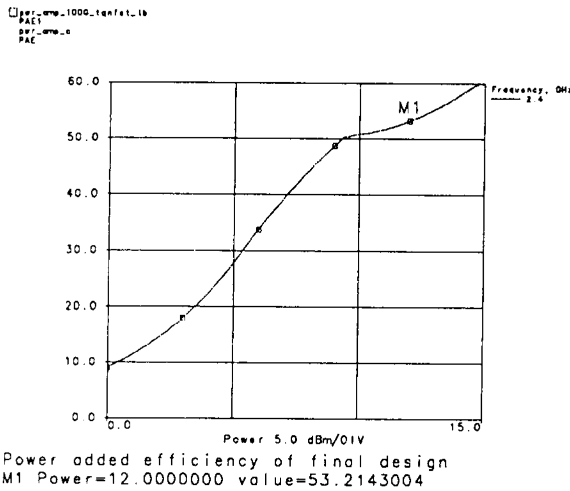


Figure 7 Power added efficiency

The bias of the circuit is set for -5 volts on the gate pad since this is a commonly available voltage and +7.8 volts on the drain. The continuity of the bias was also confirmed in the nonlinear analysis modeling that relied on the ideal voltage sources to bias the nonlinear FET models.

The stability of the final amplifier is shown in figure 9. The FET's alone had a rollet stability factor, K, of 0.3 with a very unstable output. The FET's were stabilized with 160 Ohm shunt resistors on the gate (which could have been used for bias potentially). The stability achieved with the resistors was a rollet factor, K, of 0.7 and input and output stability factor mu of 0.8. Thus the FET's themselves were conditionally stable however the losses in the input and output matching circuits stabilized the final circuit such that it is

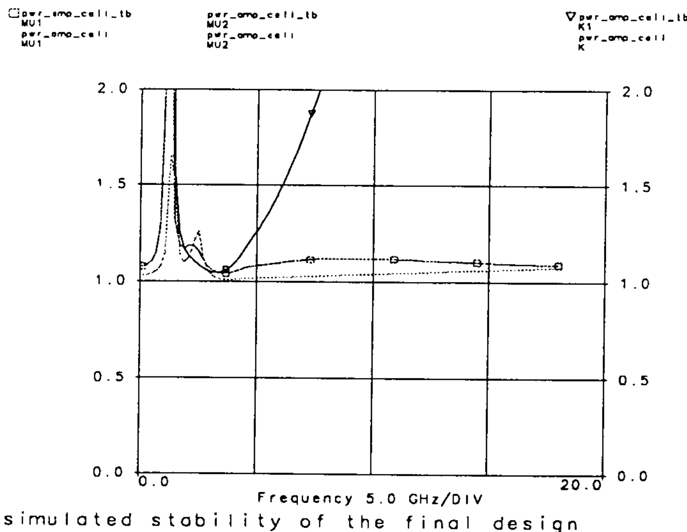


Figure 9 Amplifier stability versus frequency

unconditionally stable from 0 - 18 GHz. This final result implies that the FET's may not have needed all the stabilization used however iterating the circuit was not an option due to time constraints.

5. Test Plan

The amplifier will be tested for gain and return loss using a network analyzer calibrated to the RF probes. The S parameters of the device will be characterized over the band of interest as well as from 0.2 to 20 GHz if possible to look for out of band oscillations. This type of circuit is prone to odd mode oscillations although many preventative designs steps have been taken to avoid this. The test setup and bias voltages are shown in figure 10. For power out measurements the amplifier will need a source capable of +12 dBm output and should be hooked to a spectrum analyzer to read the in band and spurious power. The setup is also shown in figure 10.

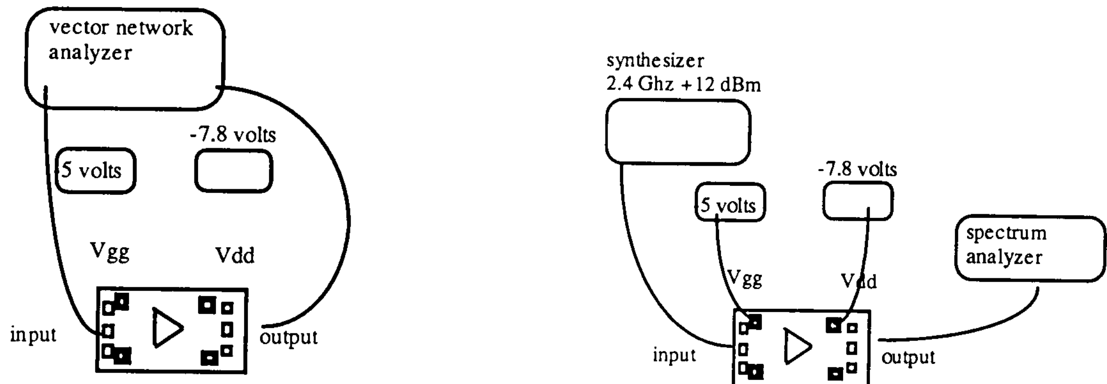


Figure 10 Test setup for S parameter measurement and compression and power out

6. Conclusions

The power amplifier design submitted meets all the performance goals except output VSWR. The power out falls between the goal and the requirement due to the trade of output VSWR and power out. Given additional chip area a balanced design would correct for the deficiencies of output VSWR versus power out and allow a better power match. A different topology of FET might provide a more optimum output match than the one chosen. Also, a single voltage supply should be possible if efficiency were willing to be sacrificed.

I would like to thank the instructors of the course for there time and effort which was considerable and also thank Triquint for the opportunity to fabricate a MMIC design. I would also like to thank Gary Ray of HP-EEsof for his assistance in the layout of this design.

S-BAND T/R SWITCH

Final Report

for
EE 525.787
Monolithic Microwave Integrated Circuit Design
The Johns Hopkins University
Whiting School of Engineering

December 9, 1996

prepared by
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Adelphi, MD
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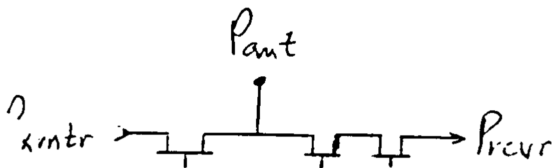
S-BAND T/R SWITCH

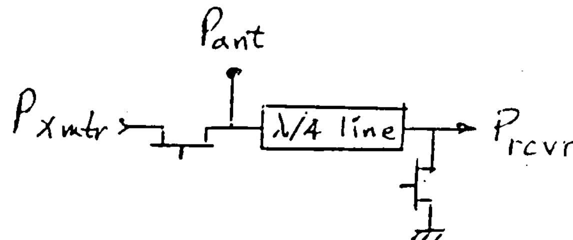
SUMMARY

The T/R switch design presented here is a broadband design suitable for use with up to a 1-Watt transmitter in the frequency range from 1 to 5 GHz. With external tuning the performance of the switch is improved with a reduction in bandwidth.

The block diagram of the switch is shown below. The current design utilizes two series FETs as switch elements. Other designs use shunt FET switch elements and a λ/4-transmission line (which is lossy in the MMIC format) when operating at the 1-W level. The success of this design is dependent on three ideas:
1. a cascode circuit for the series receiver FET switch that is able to hold-off the transmitter's peak voltage without avalanching,
2. an adaptive-bias DC circuit to keep the gate-source voltage on the cascode FETs from going positive, and,
3. a dynamic bias circuit that maintains a negative gate-source voltage throughout the transmitter's voltage swings.



Present Design



Alternative Design

The specifications and simulated (predicted) performance for the T/R switch are:

Parameter	Specification	Predicted Performance
Frequency (GHz)	2.400 - 2.483	Broadband (1 - 5 GHz)
RF Power (dBm)	+30 minimum	+30 or slightly more
Insertion Loss (dB)	< 1	1.1 xmit 2.1 rcv
Isolation (dB)	>25, 30 goal	34
VSWR (50 ohms)	<1.5:1	~~1.12~~ 1.6:1 xmit ~~1.3~~ 2.0:1 rcv
Control Voltage	single TTL line	0 and -5 V (off chip control required)
Supply Voltage (V)	± 5	not applicable
Size	60x60mil Anachip	60x60mil Anachip

The insertion loss was higher than desired for this 1-W design. A tradeoff between receiver and transmitter insertion losses was conducted. Because increased loss in the transmitter affects the communications, thermal and power designs, its performance was favored over that of the receiver. An initial design using a λ/4 transmission line yielded approximately the same loss and much reduced bandwidth.

INTRODUCTION

Circuit Description

The transmit/receive (T/R) switch is designed for a radar application in the S-band ISM (2.400 to 2.483 GHz) band. The design is a single-pole, double-throw (SPDT) switch designed for up to a 1 Watt transmitter. Because of the broadband design, other applications, such as cellular telephone, are also possible.

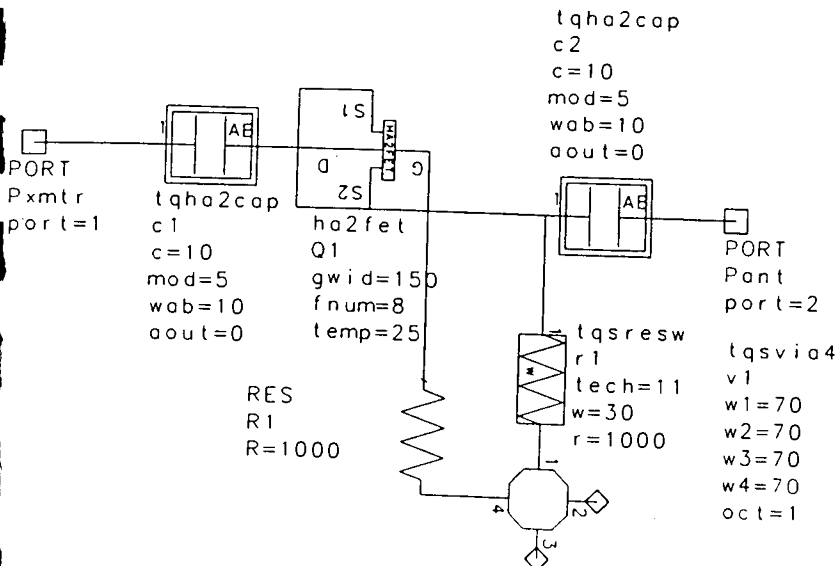
The overall block diagram of the design was presented in the summary. The T/R switch can be considered as two separate circuits, except for the effect of parasitics from the unused side of the switch. Because these parasitics are small, the switch was designed in two pieces and then joined together with DC-isolation capacitors with minimal degradation of performance.

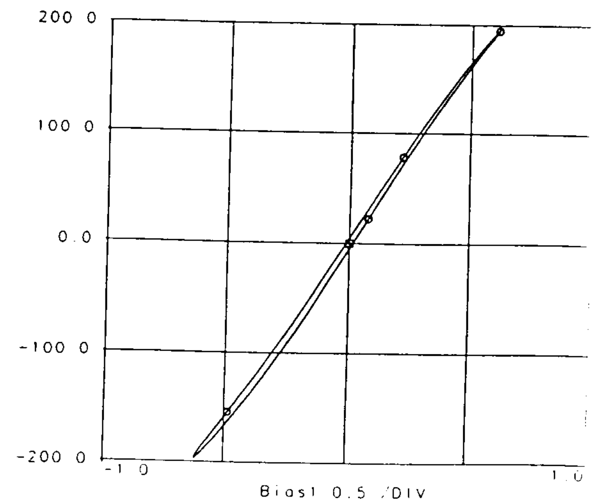
The transmitter power level drove the design of the switch. The 1-W transmitter into a matched 50-ohm transmission line has a peak voltage of ±10 V. The corresponding peak currents to a 50-ohm load (antenna) are ±200 mA. Since I_{dss} for a 300-μm FET is about 50 mA, a 1200-μm FET was chosen.

Transmitter Circuit.

The goal of the transmitter circuit was to provide minimum insertion loss to the antenna. This insertion loss was considered more important than the receiver's circuit insertion loss because the transmitter utilizes and dissipates more power, thus driving the thermal and power supply designs. Whereas, additional losses in the receiver just affect the system performance to the same degree as losses in the transmitter circuit, without driving the thermal and power designs.

The largest, standard, series FET (8 gates x 150 μm) was selected to provide minimum insertion loss. The dynamic load line for this device at the 1 W level with V_{gate}= 0 V is shown in below. Note the low distortion at the current peaks, indicating that a load impedance of less than 50 ohms should not cause generation of significant harmonic energy. The series resistance is 3 ohms, yielding an insertion loss of 0.7 dB.





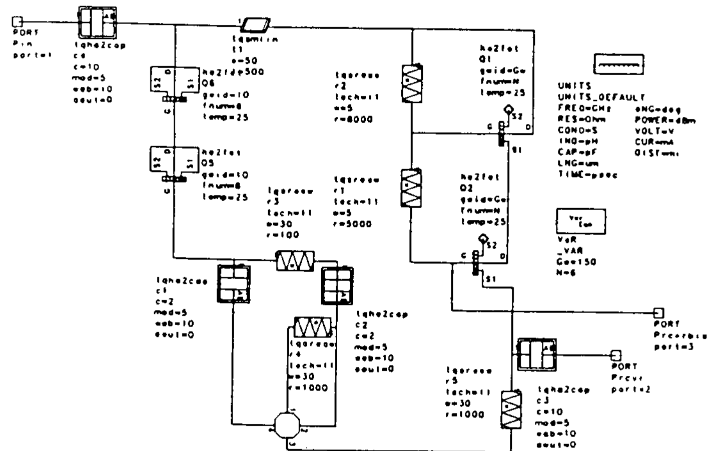
[illegible] of the series xmtr 8x150um FET at 1 W into 50 ohms

Note that there is no tuning in this transmitter circuit, so it is broadband except for the low-frequency cutoff of the series blocking capacitors.

Receiver Circuit.

This circuit consists of a cascode of two FETs and an adaptive bias supply to prevent breakdown of the FETs during the 1 W transmit period. The major problem with this design is the increased insertion loss of the two series FETs during receive. To minimize this insertion loss, each FET used 6 gates with 150 μm width. Simulations with 8 gates yielded less than 0.1 dB insertion loss reduction, so 6 gates were used in the final design.

The circuit for the adaptive-bias, cascode receiver protector (the receiver arm of the SPDT switch) is shown below. The series diodes (two were required because of breakdown) rectify the ±10 V during the transmit period. The capacitors C1 and C2 and resistor r3 filter the half-wave rectified voltage and apply the voltage to load resistor r4 which is attached to ground. As a result, the entire circuit (t1, Q1, and Q2) from C4 to C3 rises in voltage to the peak value of the applied voltage. For lower powers, a lower voltage is developed and hence the voltage adapts to the applied power level. The resistor r5 (1000 ohms) provides the DC return for the rectified voltage on the line t1.

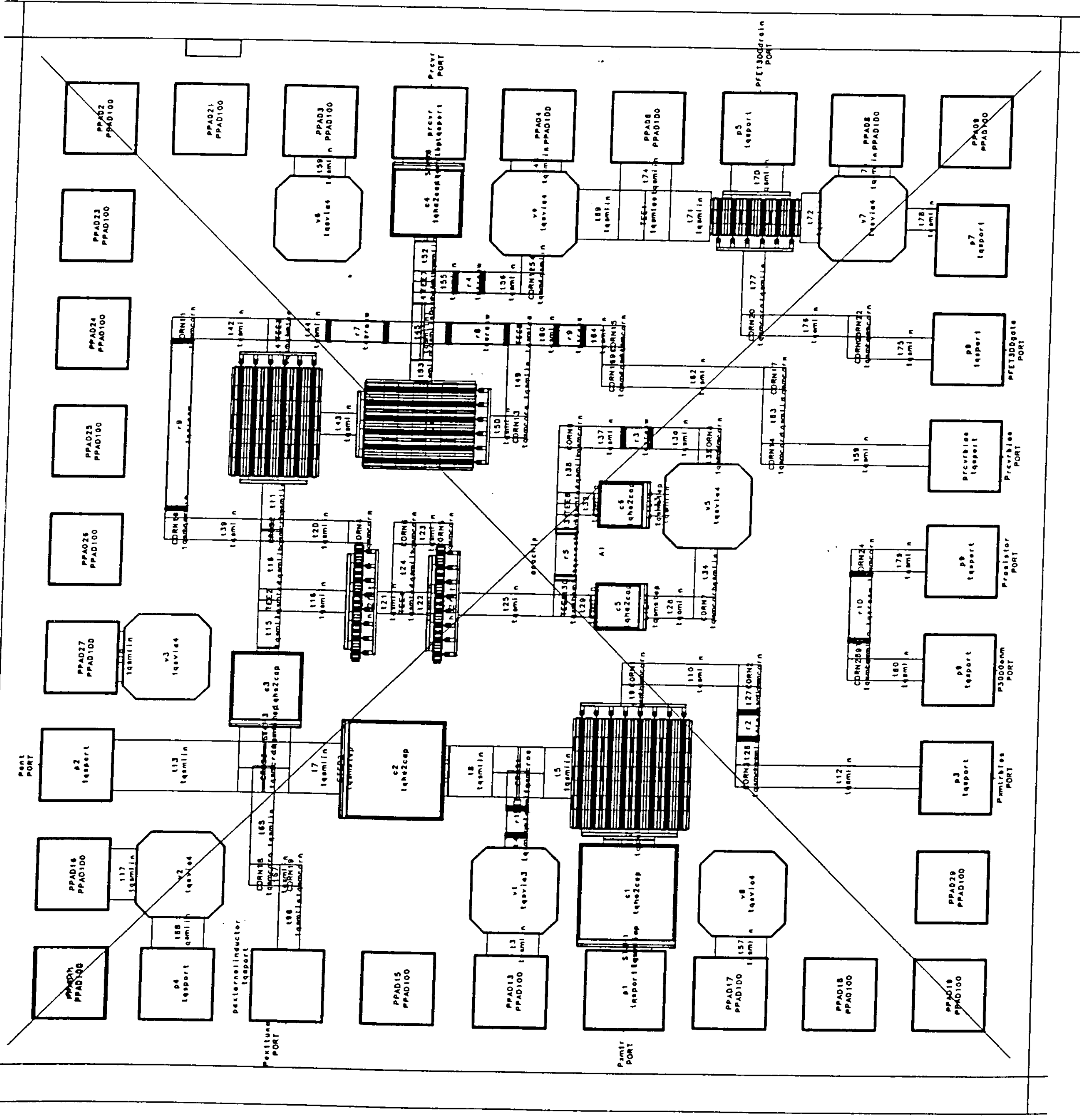


The resistors r1 and r2 act as a voltage divider to assure that the gate-drain voltages are pinched off for both FETs during transmit. The gates voltages during transmit are the sum of the voltage on line t1 and the receiver bias voltage at Port 3 (typically -3 to -5 V). During receive, Port 3 is grounded so the FETs operate at I_{dss}.

Similar to the transmitter side of the switch there is no tuning in this switch, so operation from 1 to at least 5 GHz is possible.

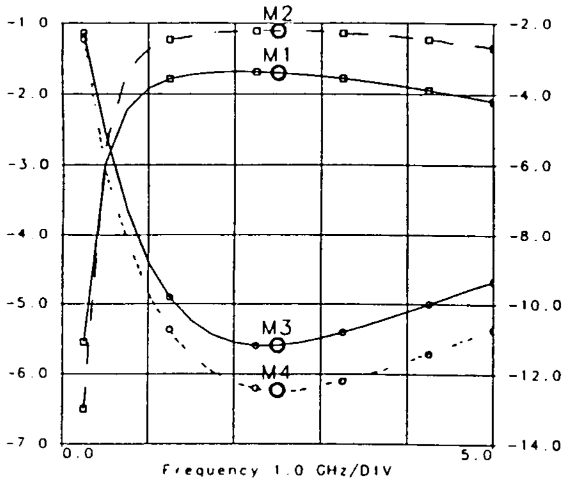
Since there is no DC bias applied to the switch, except the gate cutoff bias, no DC analysis was performed. The current in the diodes Q5 and Q6 was less that 1 mA peak, so 8x10μm FETs were utilized.

The layout of the anachip is shown in the next page.

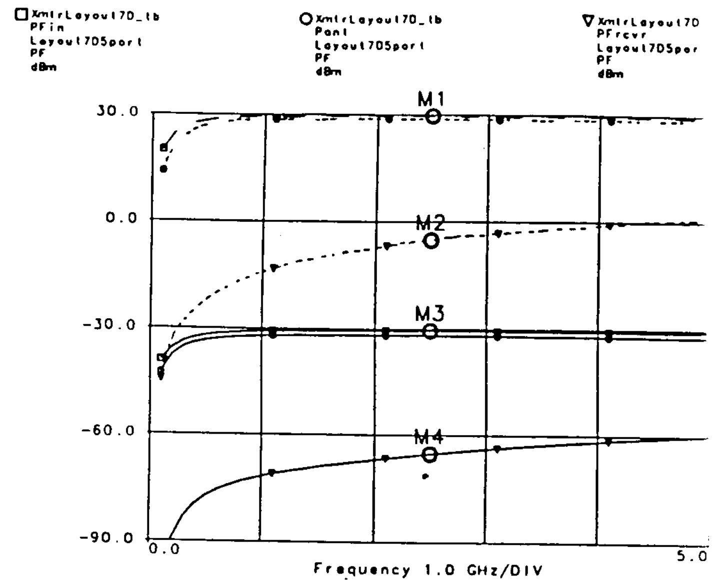


MODELED PERFORMANCE

The performance of the transmitter is shown below with no tuning included. The incident power was 1 W (30 dBm) and the receiver gate bias was -5 V, yielding an insertion loss of 1.11 dB and S11 = -12.5 dB (VSWR = 1.12:1) at 2.5 GHz.
1.6



ncy response of the T/R Switch during transmit.
No tuning, Vrcvrbias = -5 V.
S21 M1, Pinc=-30 dBm, Freq=2.5 GHz, |S21|=-1.70 dB
S21 M2, Pinc=30 dBm, Freq=2.5 GHz, |S21|=-1.11 dB
S11 M3, Pinc=-30 dBm, Freq=2.5 GHz, |S11|=-11.2 db
S11 M4, Pinc=30 dBm, Freq=2.5 GHz, |S11|=-12.5 dB

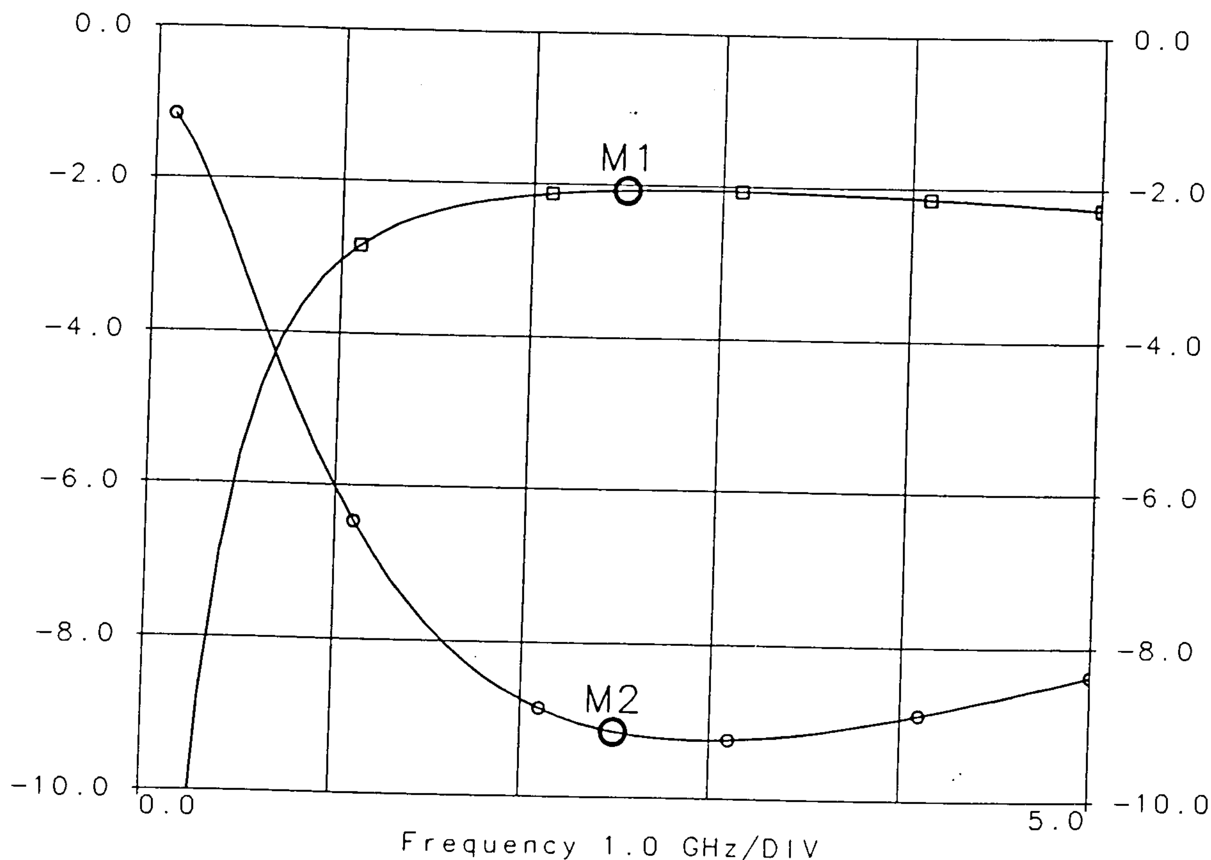


Frequency response of the T/R switch at large signal (+30 dBm) and small-signal (-30 dBm) incident power.
M1: Pinc=+30 dBm, Freq = 2.5 GHz, Pin=29.7 dBm.
M2-M1: Isolation = 34.8 dB
M3: Pinc=-30 dBm, Freq = 2.5 GHz, Pin = -30.4 dBm
M3-M4: Isolation = 34.9 dB

The insertion loss of the transmitter at low power (-30 dBm) was also simulated since that is a typical power level with the HP8510. These low-power transmitter results are shown above.

The isolation of the receiver circuit with the transmitter at 30 dBm is shown below. As expected, the isolation is reduced at higher frequencies because of the reduced reactance of the two series C_{ds} in the cascode circuit. Note that using the cascode circuit yields 3-dB additional isolation because the overall C_{ds} is 1/2 of each identical FET. The performance of the receiver circuit under small-signal and large-signal conditions is shown below. Here the small-signal level (-30 dBm) should be comparable with the HP8510 while the large-signal level (+30 dBm) associated with the transmitter shows that the receiver will have about 25 dB isolation at 2.5 GHz.

The insertion loss of the receiver circuit is higher than desired because of the use of the cascode circuit. The small-signal (-30 dBm) insertion loss is shown on the next page.



Frequency response of receiver circuit with no external tuning.
Pinc = -30 dBm, Vrcvrbias = 0 V, Vxmtrbias = -5 V.
M1, Freq = 2.5 GHz, |S21| =-2.07 dB
M2, Freq = 2.5 GHz, |S11| =-9.15 dB

I attempted to reduce this insertion loss by resonating the circuit at 2.5 GHz with a shunt inductor. The results of this tuning are shown in the Table below.

Parameter	No Matching	TQ Inductor	Ideal Inductor
|S21|	-2.07 dB	-1.85 dB	-1.54 dB
|S11|	-9.2 dB	-28 dB	-22 dB

Clearly the TQ inductor is so lossy that it only reduces the insertion loss by 0.2 dB. For this reason, a port is provided to allow an external low-loss inductor for tuning. An ideal inductor will reduce the insertion loss by 0.5 dB. Since this circuit is broadband, considered a desirable attribute, no inductor is provided and the additional insertion loss is accepted.

TEST PLAN

The adaptive T/R switch should be tested with the HP8510 for its low-power performance. The following test matrix is suitable.

Mode	S11 Probe Location	S22 Probe Location	$V_{rcvrbias}$ (Volts)	$V_{xmtrbias}$ (Volts)
Xmit	Pxmtr	Pant	-5	0
Rcv	Pant	Prcvr	0	-5

For the high-power measurements the T/R switch will dissipate about 0.25 W. This power level will probably require that the unit be mounted (soldered or conductive epoxied) in a test fixture allowing some thermal conduction. I have a coplanar fixture that maybe able to handle this power. A reflectometer and suitable attenuators powered with a TWT is available temporarily from the Army Reearch Laboratory for this test.

CONCLUSIONS AND RECOMMENDATIONS

The T/R switch is a broadband design suitable for many applications in addition to the S-band radar. With external tuning, about 0.5 dB receiver insertion loss improvement may be possible, with a reduction in operating bandwidth.

This adaptive switch design could be continued for even higher power levels. Adding another cascode FET might allow over 2 W of transmitter power to be held off without avalanching. The 8x150μm transmitter FET may still be suitable since the current peaks would only be 280 mA into 50 ohms.

ACKNOWLEDGEMENTS

I wish to thank the 525.787 instructors (Craig Moore and John Penn) for their support and suggestions. Also many thanks to Gary Wray of HPEEsof and Sheng Cheng of JHU/Dorsey who allowed me to "bug" them with a seemingly infinite number of questions about details of the layout and the program. Finally, I wish to note that Carmine Vasili, Tom Marynowski, and Elaine Merenda of (now) Northrop-Grumman reintroduced me to the use of the cascode circuit in the MMIC format. Without use of this circuit, a much inferior design with lossy quarter-wave transformers would have resulted.

Mike Dippold

Summary

The Low Noise Amplifier (LNA) MMIC design described in this report is part of a transceiver design that can be used for wireless local area network (WLAN) applications or an S band ISM FM/CW radar. The design specifications are representative of commercial transceiver products. The LNA MMIC was designed and simulated using HP EEsof Libra. All elements in the design are from the Triquint Smart Library. The design is placed on a 60 mil square Anachip and is fabricated using the Triquint HA2 process.

Introduction

The Low Noise Amplifier is a critical part of the front-end transceiver design process. The LNA determines to a large extent the sensitivity of the receiver. Therefore, an amplifier with the lowest noise figure possible is desired. It is also necessary to achieve the highest linearity performance possible in the front-end design. The front-end linearity performance determines the two-tone dynamic range of the receiver. In order to achieve high linearity performance the highest possible output intercept is sought in the design.

The design goals outlined in the above paragraph seem to be at odds with one another. The lowest noise figure is normally achieved with a low DC bias current. But a low DC bias current degrades the large signal performance, i.e., the intercept point. Thus, the LNA design is one of design specification compromises.

As the LNA designers pondered the design task at hand, a two stage amplifier architecture immediately came to mind. The designers decision became clear that it was the right choice after investigating the noise figure cascade equation and the output intercept cascade equation. A low noise figure can be achieved by biasing the input stage amplifier for low noise. The third order intercept specification can be achieved by biasing the second stage amplifier at a higher level. The higher bias level of the second stage results in better large signal performance.

Circuit design alternatives were considered in this design when confronted with stability and DC biasing. The GAas Fet was determined to be unstable while the DC biasing circuit lurked to create havoc with the noise figure. Although the Fets could be stabilized with series or parallel resistors in the gate or drain circuits, it would decrease the overall gain and increase the noise figure. It was discovered that a series inductor in the

source circuit stabilized the Fet. The source inductor not only served to stabilize the Fet but also brought Gamma Opt closer to 50 ohms on the Smith Chart. Another gem discovered by using the source inductor was that Gamma Opt could be adjusted to become S11 conjugate. This means that the Fet input matching to Gamma Opt not only achieved the lowest possible noise figure but also maximum gain. Now the DC biasing circuit design took more time since most biasing circuits affected the gain and the noise figure. The DC biasing goal was to use only one power supply. But the circuits considered to develop the gate bias took too much of a toll on gain and noise figure. Therefore, a three resistor voltage divider network using two power supplies were used in the LNA design.

As was mentioned in the above paragraph, the input amplifier stage matching network matched S11 to Gamma Opt which happened to be S11 conjugate. The result was a match for the lowest noise figure and maximum gain. The input stage amplifier output matching network matched S22 conjugate to 50 ohms.

The output stage amplifier design was a simultaneously conjugate match. At this point the designers were at a crossroads with the output amplifier. Should the amplifier be designed using the Cripps method for maximum power output or a simultaneously conjugate match for maximum gain? The designers were thinking of high gain and maximizing output power for large signal performance. The simultaneously conjugate match was chosen. It achieved gain and intercept design specification.

The intermediate matching network was not a problem since the input stage output matching network and the output stage input matching network were both designed to match to 50 ohms. Another way to think about it is to picture the center of the Smith Chart as the intermediate matching point between both stages.

DC Analysis

Figure 1 shows the DC bias for the input and output Fets. The input Fet is biased at 20% IDSS (21 ma) and 2.5 VDS for low noise performance. The interconnect microstrip lines used in the input Fet Drain circuit are 10 micron wide Metal 1. The Metal 1 has a 9 ma/um current carrying capacity. The total current capacity of the 10 micron wide Metal 1 is 90 ma. for the 21 ma. DC bias current. The Gate current for the input Fet is calculated to be 780 microamps. All resistors were sized in width to carry the the DC bias current. For the high valued Gate resistors N- process type resistors were used because of the high sheet resistance. Even though the current carrying capacity of N- is 0.025ma/um,

the Gate bias current is relatively low as compared to the Drain current.

The output Fet is biased at 50% IDSS (52ma) and 7 VDS. The higher bias condition is necessary to meet the LNA output power and intercept point specification. The microstrip lines in the Drain circuit are 10 micron wide Metal 1. The maximum current carrying capacity is 90 ma. for the 52 ma. DC Drain current. The Drain and Gate resistors are designed using the appropriate technology and sized in width accordingly.

Modeled Performance

Specification Compliance Matrix

Parameter	Design Specification	Simulation
Frequency	2400 to 2483 MHz	2358 to 2524 MHz
Bandwidth	> 83 MHz	166 MHz
Gain	>15 dB	19.5dB
Gain Ripple	+/- 0.5 dB	+/- 0.5 dB
Noise Figure	<5 dB	<4 dB
Input IP3	> +8 dBm	+12 dBm
VSWR, 50 ohm	< 1.5:1 input and output	<1.35:1 input and output
Power Supplies	+/- 5 Volts	+8 and -5 Volts

The specification compliance matrix summarizes the results of the simulated LNA design. The simulation data was extracted from the LNA layout on the Anachip with all microstrip lines in place. All parameters in the following figures are plotted over twice the bandwidth of the design specification. It may be noted that all specifications were met or exceeded over twice the bandwidth of the design specification.

The S-parameters are plotted in Figure 2. The small signal gain is centered at 19.5 dB with a deviation of +/- 0.5 dB over the bandwidth. Although the S11 and S22 are shown in Figure 1, the input and output VSWR plotted in Figure 3 is a better indication of the device matching. Both the input and output VSWR are less than 1.35:1. Also shown is the mu stability parameter for the casacded LNA. Both mu1 and mu2 are well above 1 indicating a stable device.

Figure 4 is a plot of the Transducer Gain and P1dB. It is an indication of the large signal performance. The Transducer Gain is almost 1 dB lower than the small signal gain and can be attributed to the differences between the linear and nonlinear Fet models. The P1dB is about 21 dBm. The Third-Order Output Intercept point can be extracted from P1dB but was simulated using the IP test parameter in Libra. Figure 5 indicates output IP3 point to be +33 dBm. The Input IP3 is calculated by subtracting the gain from the Output IP3. The Input IP3 is +13.5 dBm.

The last design parameter is shown in Figure 6. The Noise Figure for the input Fet is less than 3.1 dB. The cascaded Noise Figure was not modeled since a noise parameter model did not exist for a Fet biased at 50% IDSS. A model could have been constructed based upon the Fet linear model and varying the temperature of the Fet RDS resistor. Since the input Fet Noise Figure is much below the design specification of 5 dB the designers were confident the second stage's noise contribution is minimal. During the layout of the LNA on the Anachip, the input and output matching networks of the input Fet were tuned due to added inductance of the microstrip lines. The tuning process resulted in the input match moving away from Gamma Opt. It is evident in Figure 6 as the pre-layout and post layout Noise Figure plots have opposite slope lines.

An estimated Noise Figure calculation can be performed using the cascaded Noise Figure equation. The following simulated and estimated data is used.

* Simulated Input Fet Noise Figure - 3.0 dB
* Simulated Input Fet Small Signal Gain - 9.0 dB
* Estimated Output Fet Noise Figure - 3.0 dB

The cascade linear Noise Factor equation is given as follows:

$$F = F_1 + (F_2 - 1)/G_1$$

where F_1 = Input Fet Noise Factor
F_2 = Output Fet Noise Factor
G_1 = Input Fet Gain

Therefore, after converting the Noise Figures to linear Noise Factors the equation becomes

$$\begin{aligned} F &= 1.99 + (1.99-1)/7.94 \\ &= 1.99 + .124 \\ &= 2.11 \text{ (3.24 dB)} \end{aligned}$$

If $F_2 = 4$ dB, NF = 3.38 dB.
If $F_2 = 5$ dB, NF = 3.54 dB.

The Anachip layout is shown in Figure 7. The RF input is on the left face while the RF output is located on the right face of the Anachip. Figures 8 and 9 are schematics of the input Fet and output Fet, respectively. Figure 10 is a schematic of the cascaded Fets showing additional microstrip lines needed for the Anachip layout. Figure 12 is a schematic of the cascaded LNA Fets with ideal elements.

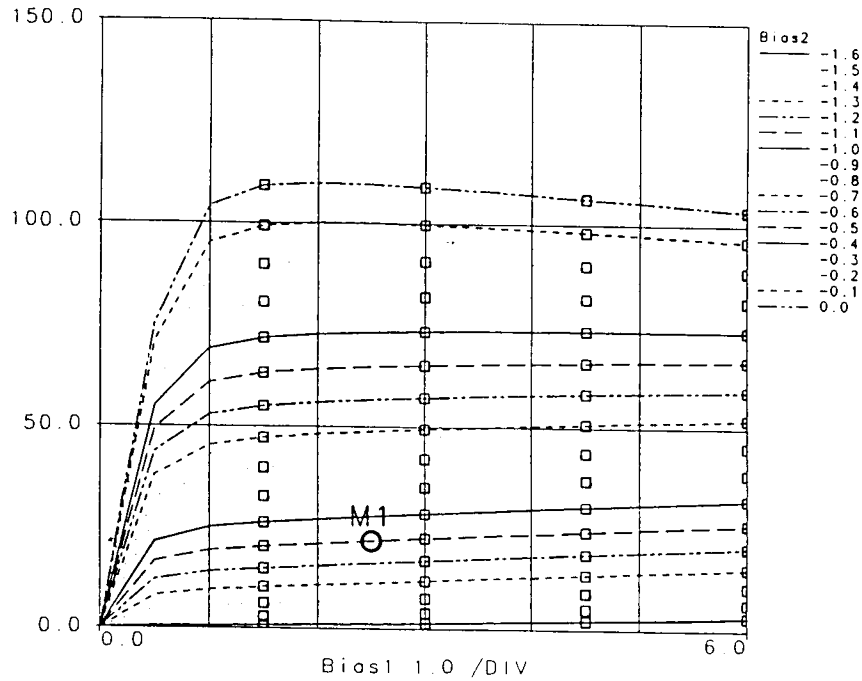
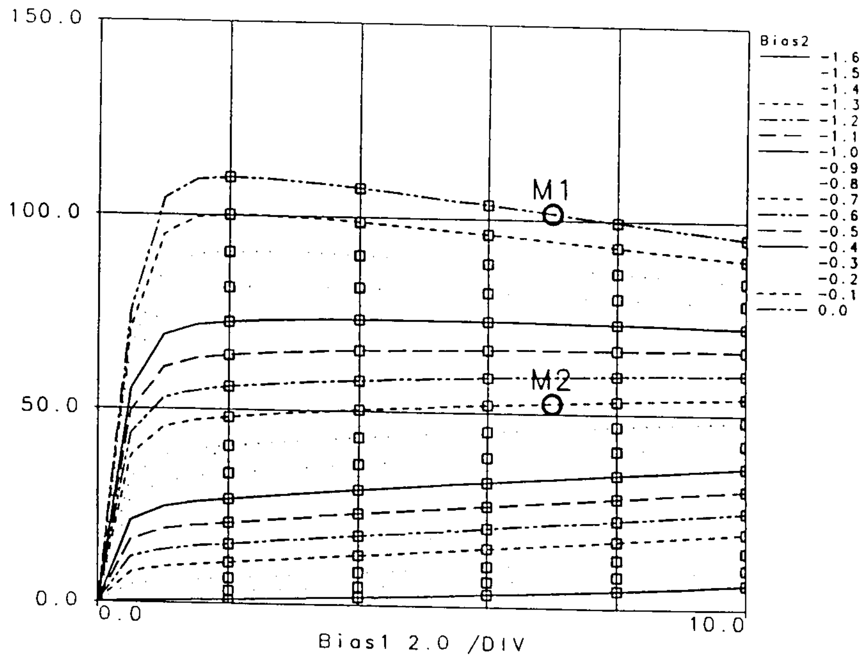
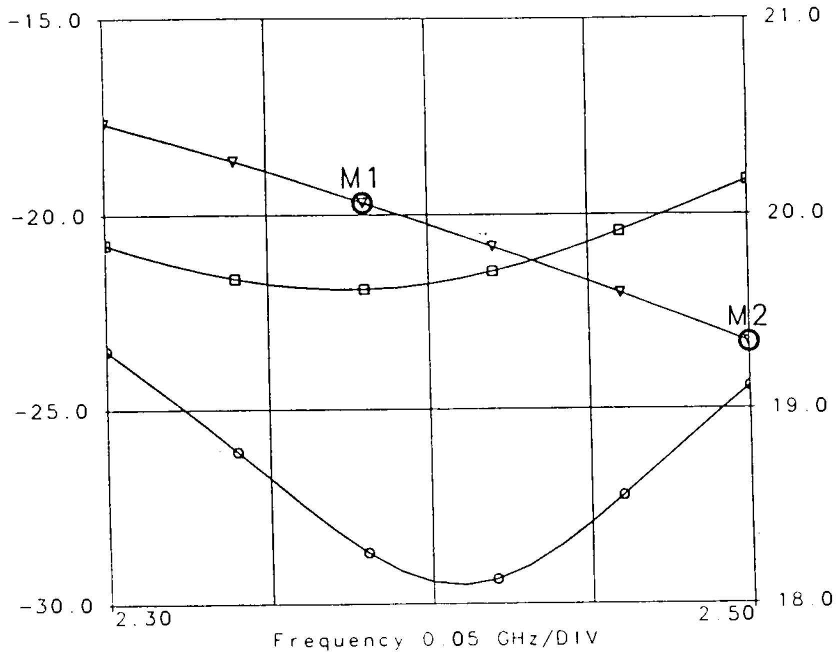


Figure 1) The above I-V curves show the input Fet biased at 20% IDSS and 2.5 VDS . The bottom I-V curves show the output Fet biased at 50% IDSS and +7 VDS.



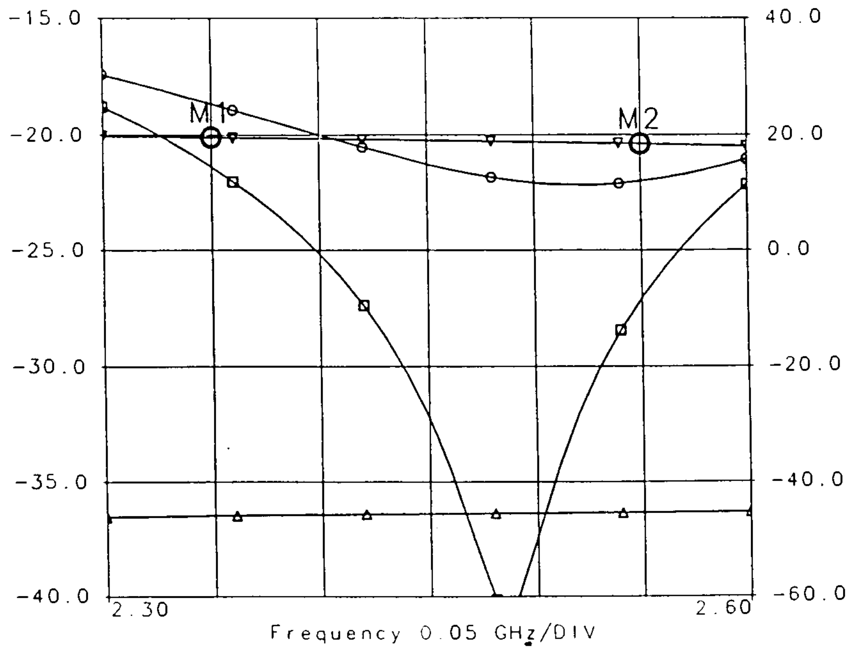
□ proj_tb S11 proj_non_linear S[1,1] dB
○ proj_tb S22 proj_non_linear S[2,2] dB
All TQ ELEMENTS
▽ proj_tb S21 proj_non_linear S[2,1] dB
△ proj_tb S12 proj_non_linear S[1,2] dB



M1 Frequency=2.38000000 value=20.0626506
M2 Frequency=2 50000000 value=19 3391928

Figure 2) The above S-parameter plot is for the pre-layout LNA MMIC design. The bottom S-parameter plot is for the LNA layout on the Anachip.

□ proj_tb S11 proj_NL_mlin S[1,1] dB
○ proj_tb S22 proj_NL_mlin S[2,2] dB
▽ proj_tb S21 proj_NL_mlin S[2,1] dB
△ proj_tb S12 proj_NL_mlin S[1,2] dB



M1 Frequency=2.35000000 value=19.5824769
M2 Frequency=2.55000000 value=18.4172766

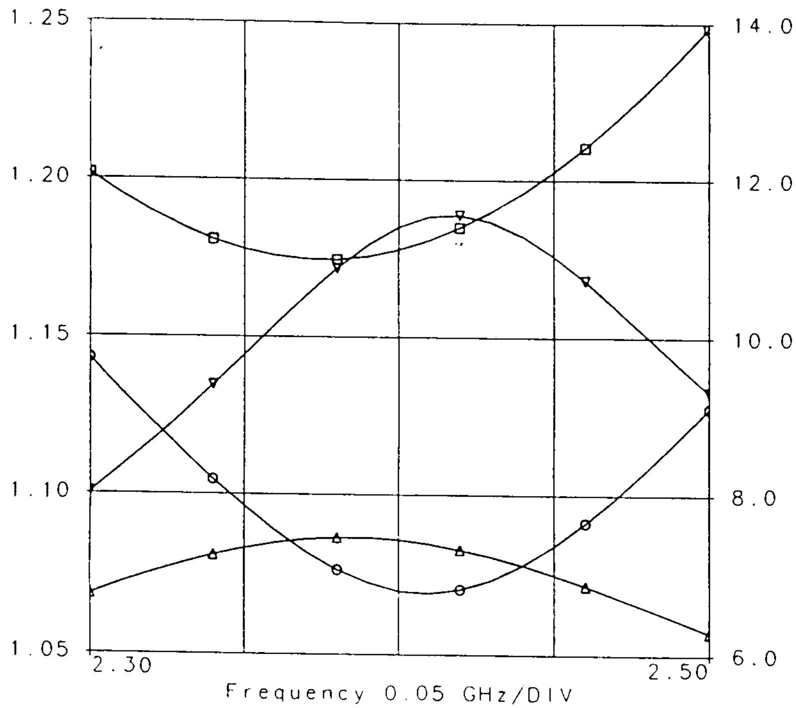
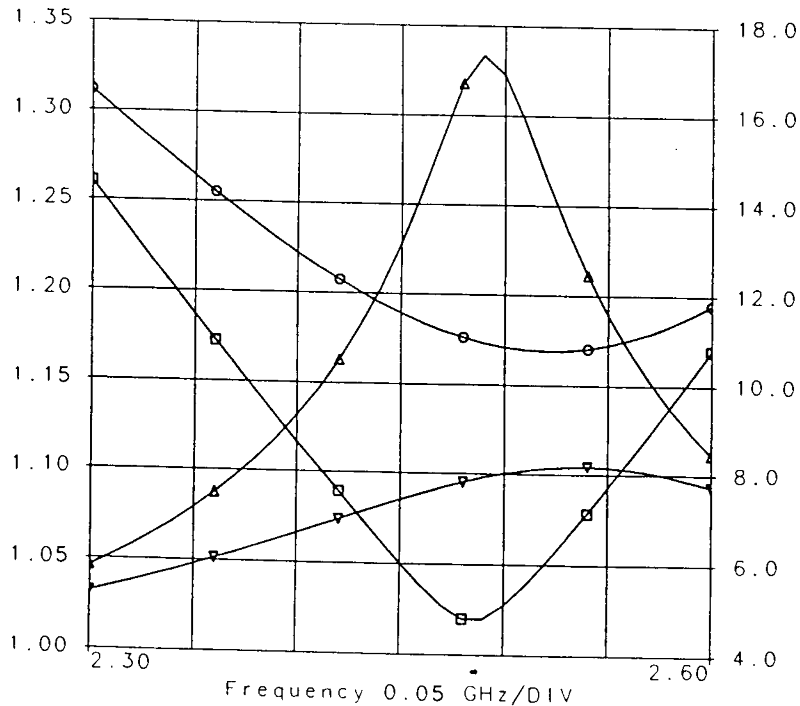


Figure 3) The above plot shows the input and output VSWR with the MU stability parameters for the pre-layout LNA MMIC design. The bottom plot shows the input and output VSWR and MU stability parameter for the LNA layout on the Anachip.



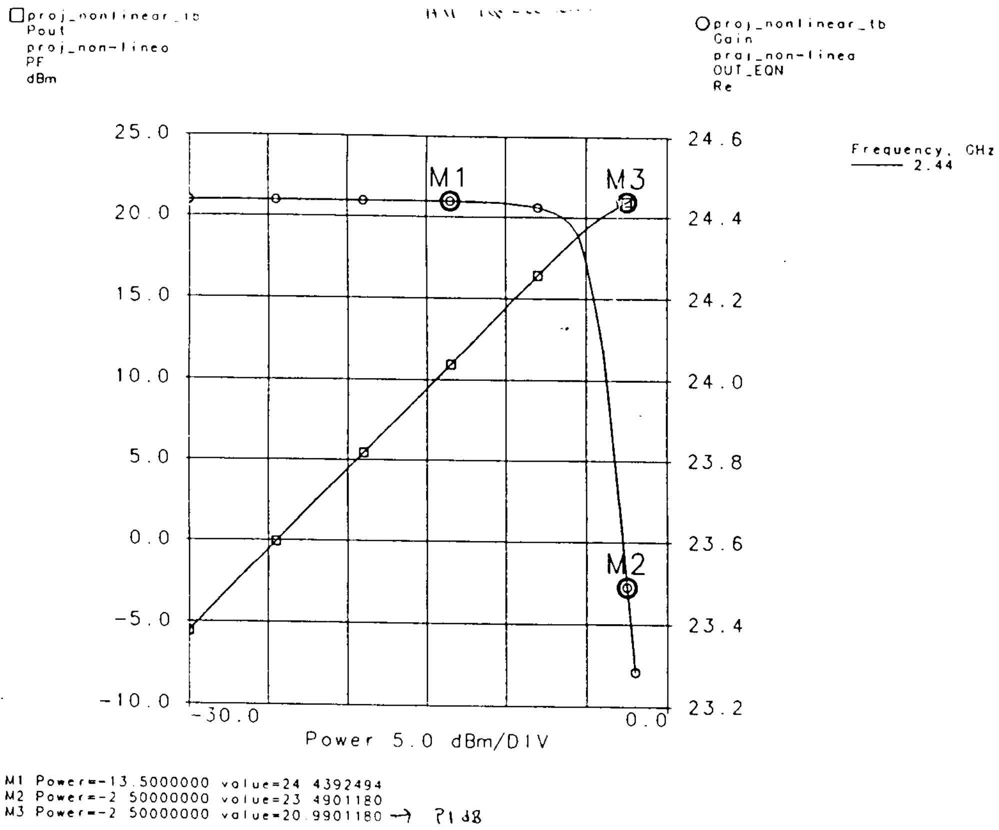
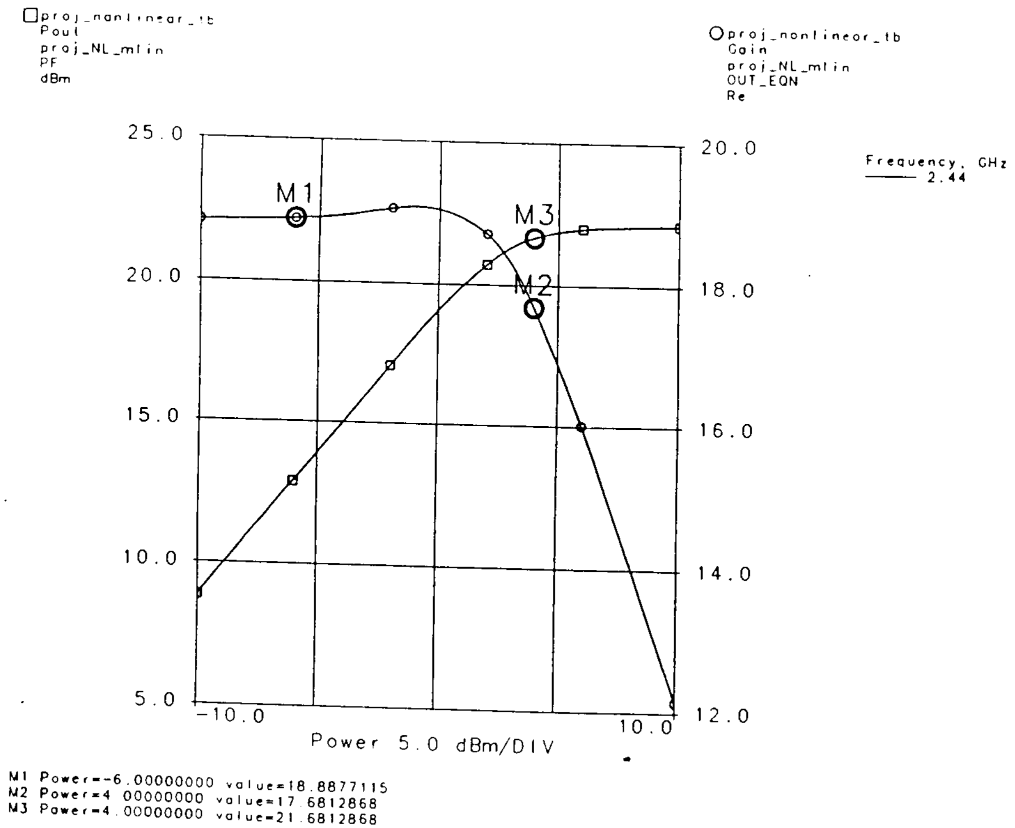


Figure 4) The above plot shows the Transducer Gain and P1dB for the pre-layout LNA MMIC design. The bottom plot shows the Transducer Gain and P1dB for the LNA layout on the Anachip.



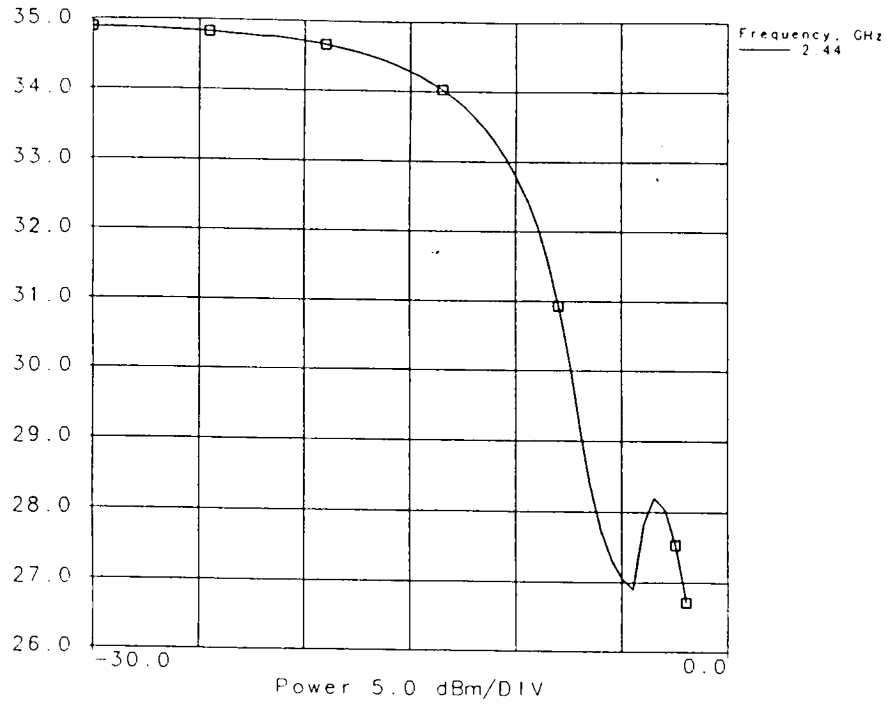
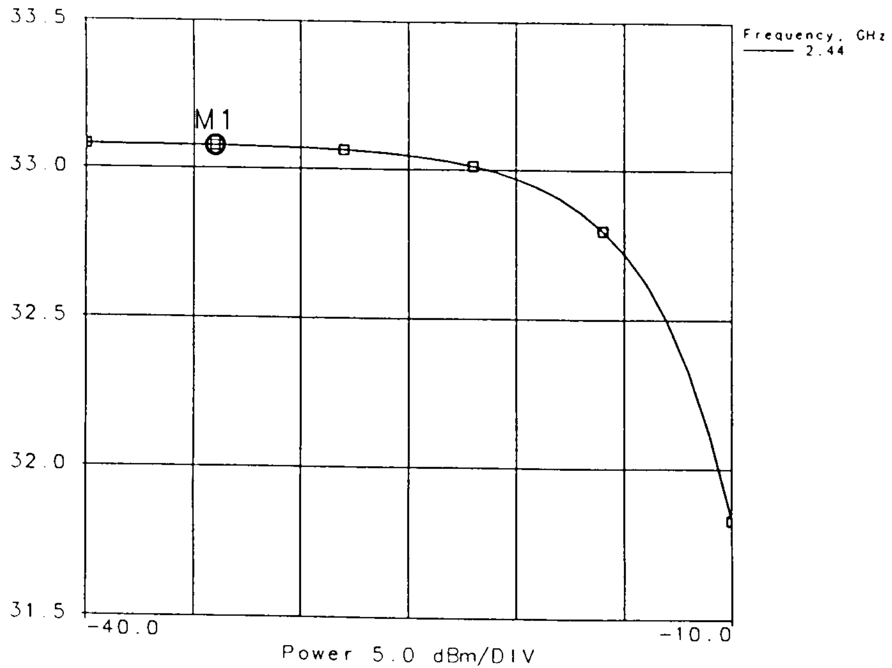


Figure 5) The above plot shows the Output Third-Order Intercept for the pre-layout LNA MMIC design. The bottom plot shows the Output Third-Order Intercept for the LNA layout on the Anachip.



M1 Power=-34 0000000 value=33 0773836

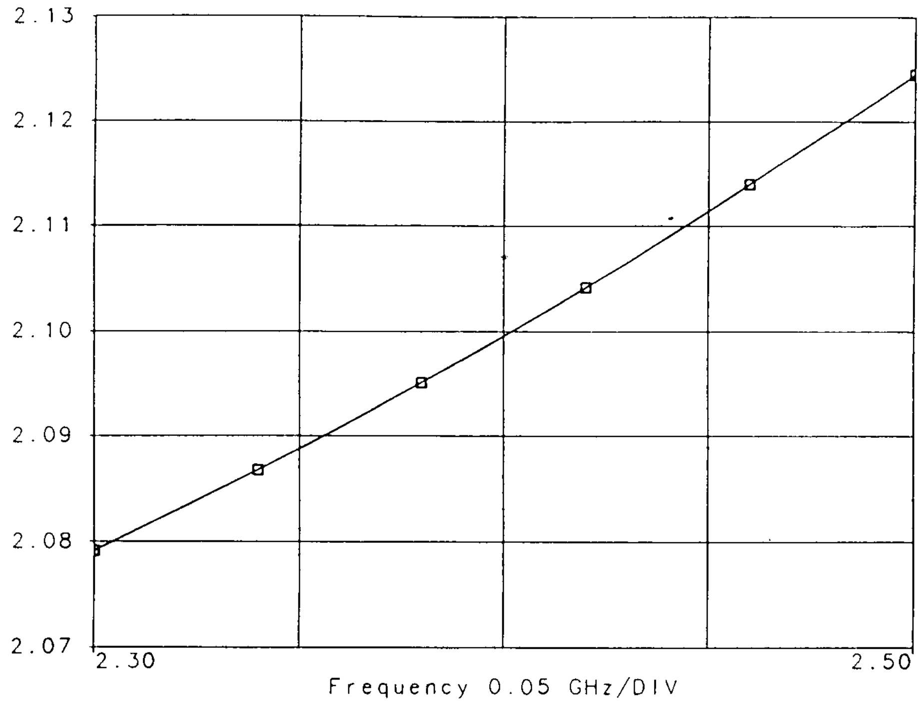
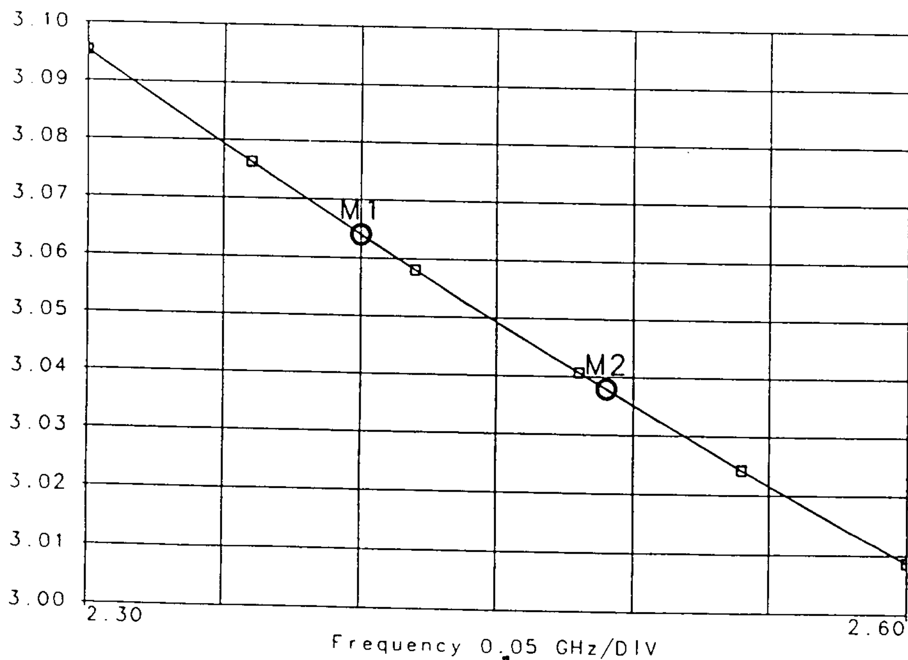


Figure 6) The above plot shows the input stage Fet Noise Figure for the pre-layout LNA MMIC design. The bottom plot shows the input stage Fet Noise Figure for the LNA layout on the Anachip.



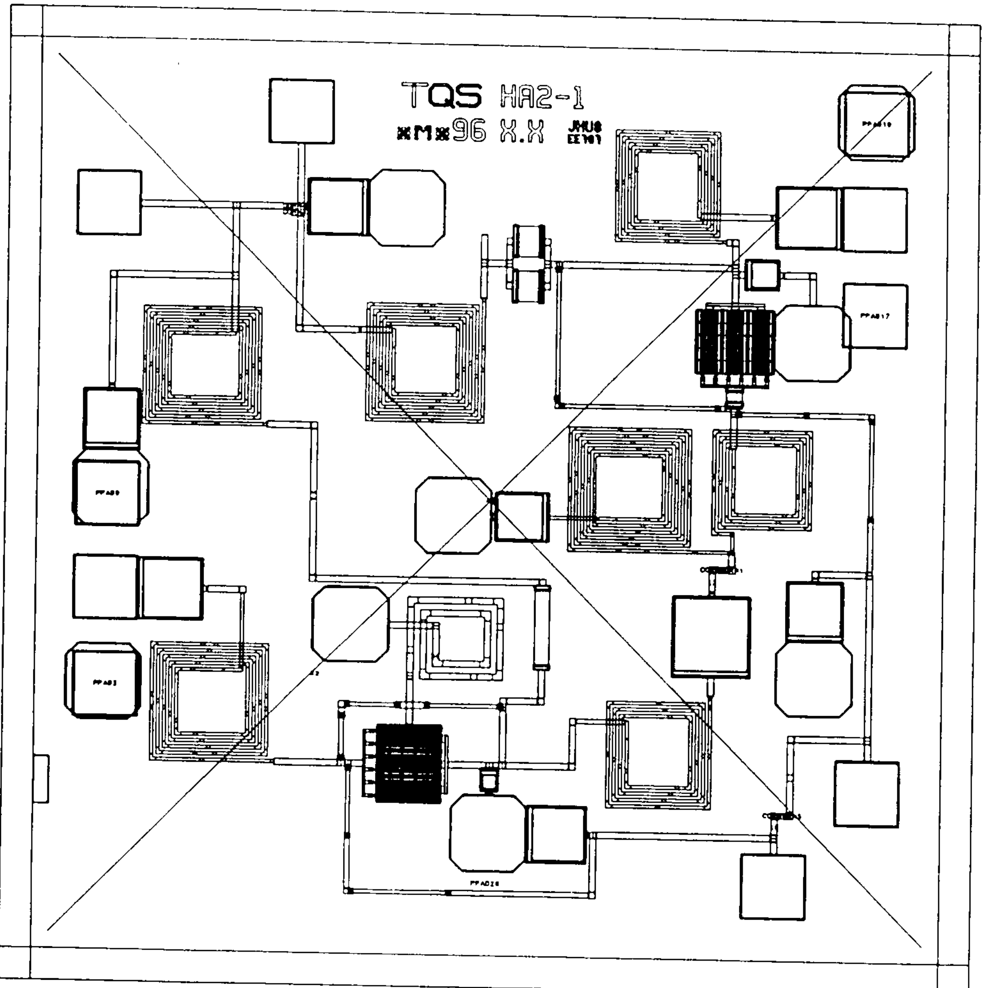


Figure 7) The LNA MMIC layout on a 60 by 60 mil Anachip.

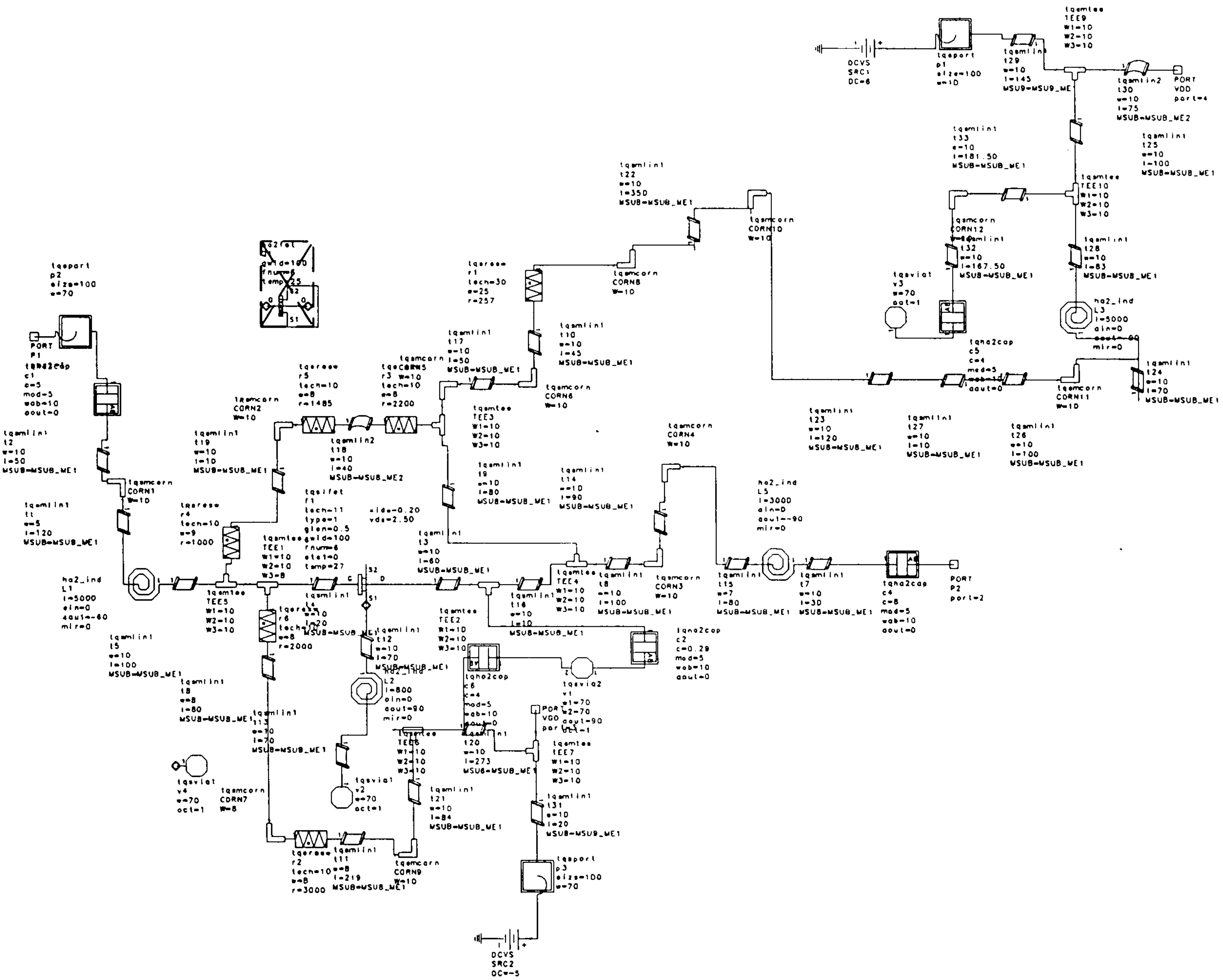


Figure 8) The input Fet schematic showing all Triquint elements and microstrip lines.

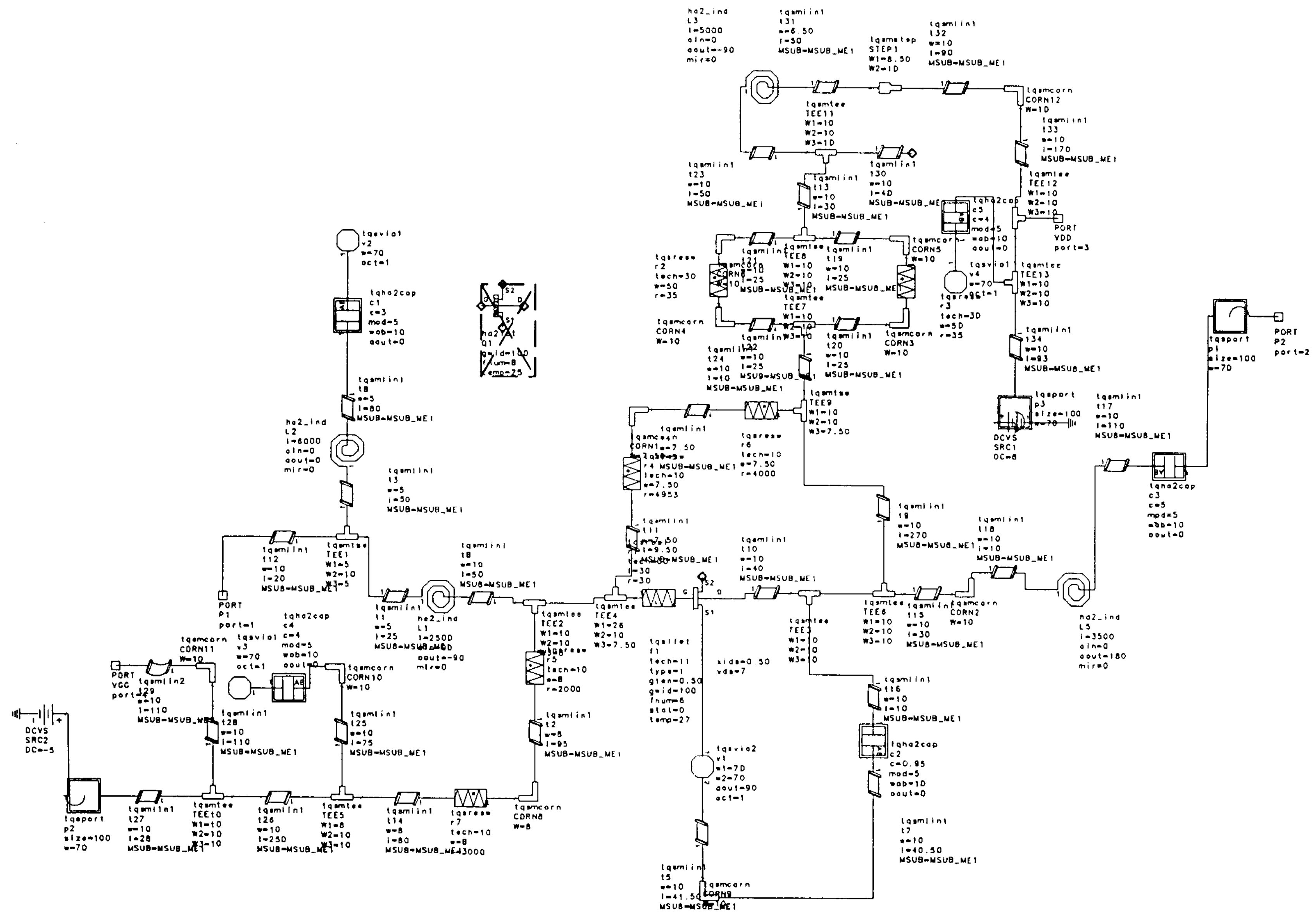


Figure 9) The output Fet schematic showing all Triquint elements and microstrip lines.

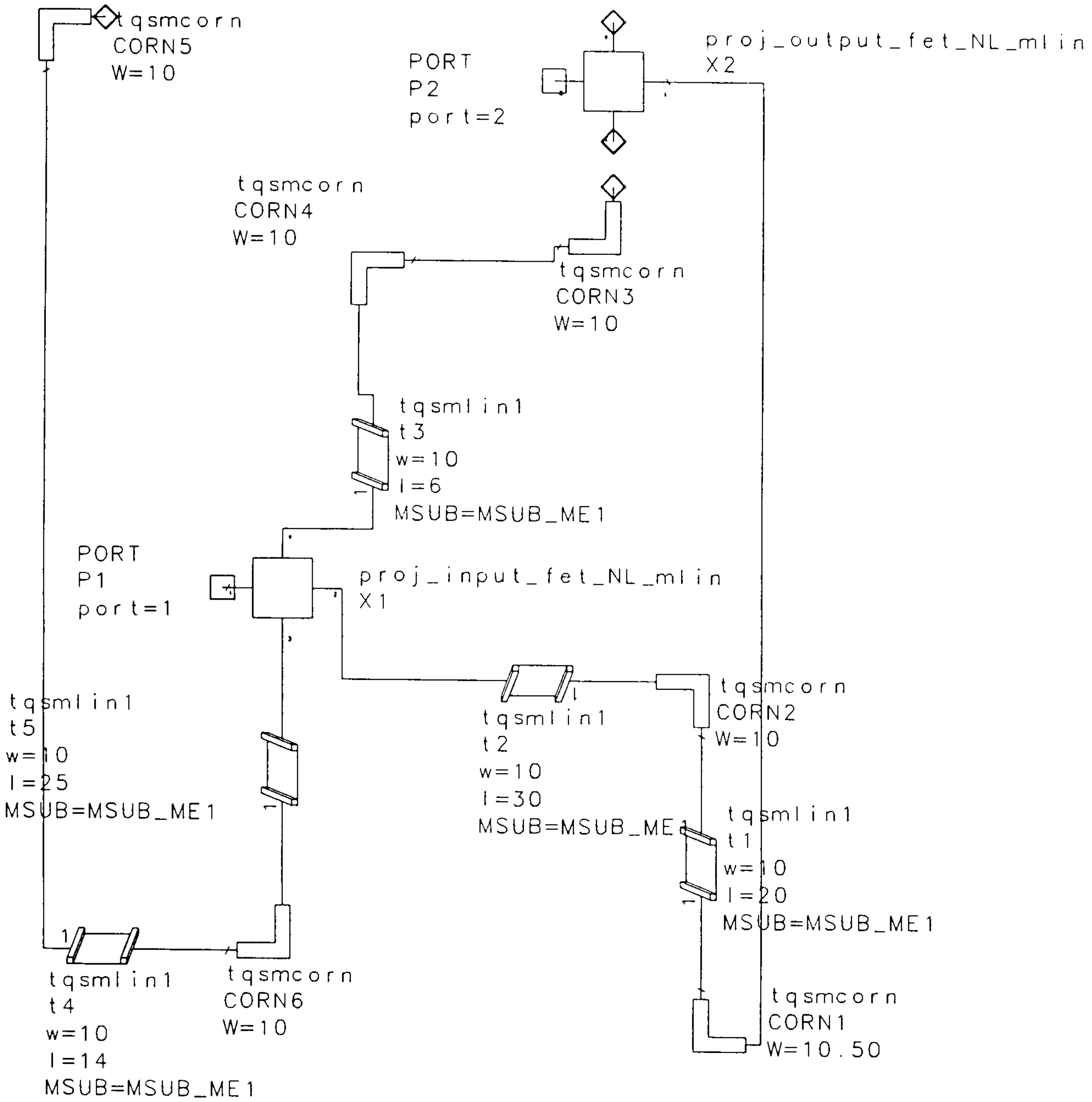


Figure 10) The cascade schematic showing additional microstrip lines needed to connect between the fets and to the additional power supplies.

Test Plan

Test Equipment Required:

* HP 8510 Network Analyzer or equivalent
* Wafer probe Station with DC and RF probes
* HP 8970B Noise Figure Meter
* +8 Volt Power Supply
* -5 Volt Power Supply
* Spectrum Analyzer
* Two Signal Generators with frequency capability to 2.44 GHz
* 3 way coupler
* 70 dB Variable Attenuator in 10 dB steps
* 10 dB Variable Attenuator in 1 dB steps

The LNA has been designed on a 60 by 60 mil Anachip with Gnd-Signal-Gnd pads for RF probing. The layout in Figure 11 illustrates where all RF and DC connections are to be made. The power supply pads designated VDD1 and VGG1 are the primary supplies for both the input and output stage Fets. The capability to operate each Fet stage with separate power supplies has been designed onto the Anachip. Pads designated as VDD2 and VGG2 are connected to the primary power supply lines with airbridges. When the airbridges are disconnected, supplies VDD1 and VGG1 bias the input Fet and VDD2 and VGG2 bias the output Fet.

Test Procedure to Measure S-Parameters:

1) Calibrate the Network Analyzer over a frequency range of 2.35 to 2.55 GHz.

2) Calibrate the Wafer Probe Station if necessary over a frequency range of 2.35 to 2.55 GHz.

3) Connect the Network Analyzer and the power supplies as shown in Figure 11 .

4) Connect the Wafer Station DC and RF probes to the Anachip.

5) As a precaution turn down the ~~negative~~ positive power, ~~VGG1~~ VDD, to zero Volts before applying power.

6) Turn on the ~~VDD1~~ VGG power supply. and set to -5V.

7) Turn on the ~~VGG1~~ VDD power supply and slowly increase the voltage to ~~-5~~ +8 Volts.

8) Measure the S-paramaters on the Network Analyzer and compare to simulated data.

Test Procedure to Measure the Output Third-Order Intercept Point:

1) Various methods exist for measuring the Intercept Point. The following method is a simple graphical approach using the test setup in Figure 11.

2) Set Signal Generator #1 to 2.440 GHz CW at -10 dBm. Use the Spectrum Analyzer to measure the signal.

3) Set Signal Generator #2 to 2.441 GHz CW at -10 dBm. Use the Spectrum Analyzer to measure the signal.

4) Connect the test setup as shown in Figure 11.

5) Switch off the output power from Signal Generator #2.

6) The Fundamental or Linear Response is measured first. It can be plotted as Pout vs. Pin. on graph paper.

   Set the 70 dB attenuator to 70 dB. Set the 10 dB attenuator to 10 dB. Now decrease the attenuation in 10 dB steps and plot the output power response. When the 70 dB attenuator has been adjusted to 0 dB, decrease the 10 dB attenuator in 1 dB steps. Be sure to plot points up to and including the P1dB. P1dB should fall between 20 and 25 dBm. Be sure to check the simulated design data.

7) Set both attenuators to maximum attenuation. Switch on Signal Generator #2. Both Signal Generator signal amplitudes must be equal to perform a two tone test.

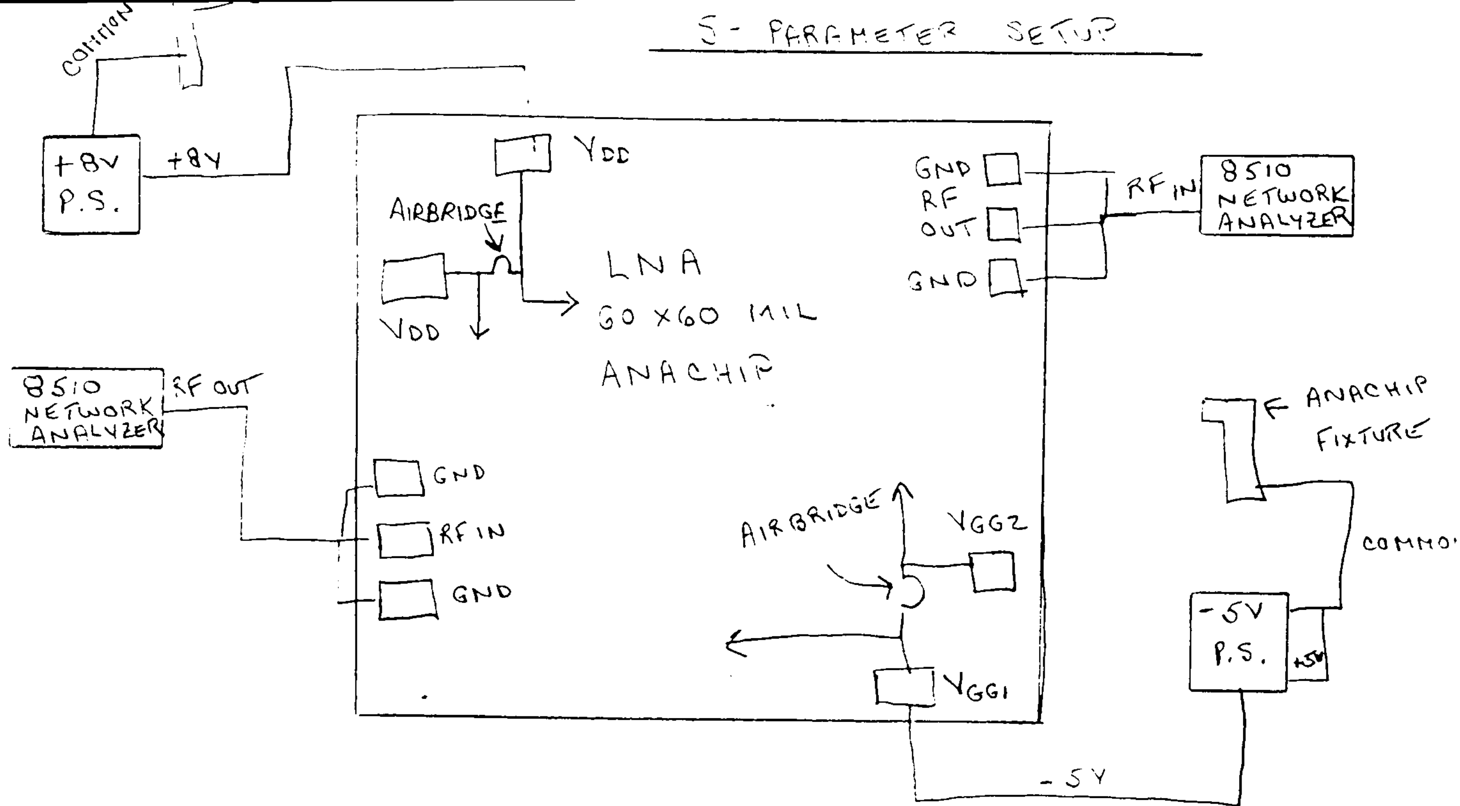
8) Increase the third-order intermodulation signal by decreasing the attenuation. Plot the intermod. power on the graph. Note the slope of the intermod. line is 3:1 while that of the fundamental is 1:1. The intercept point is located where the fundamental line intersects the third order intermod line.

Test Plan for Measuring the Noise Figure

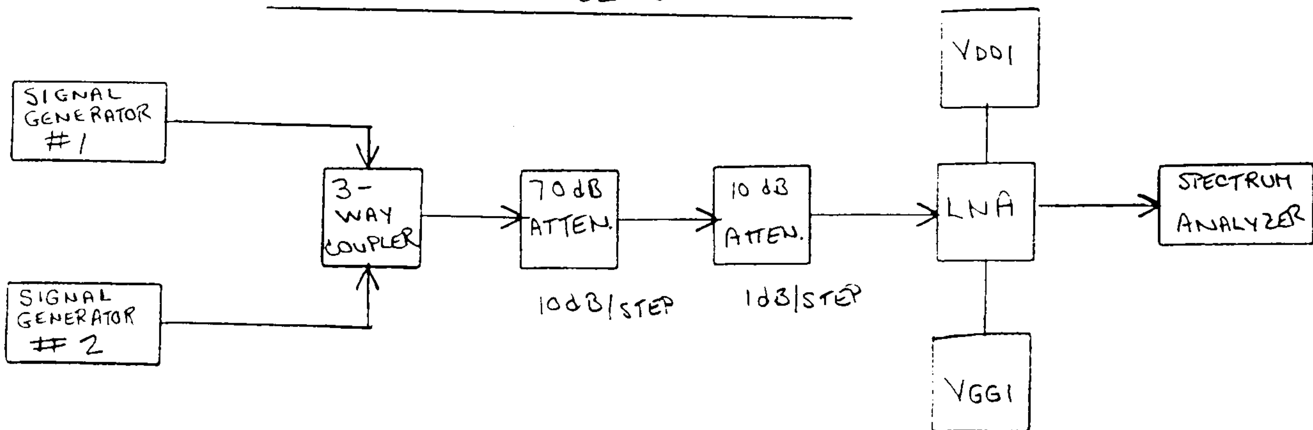
1) Calibrate the HP 8970B Noise Figure Meter.

2) Connect the Noise Figure Meter as shown in Figure 11.

3) Read the Noise Figure from the front display and compare with simulated data.



IP3 TEST SETUP



NOISE FIGURE TEST SETUP

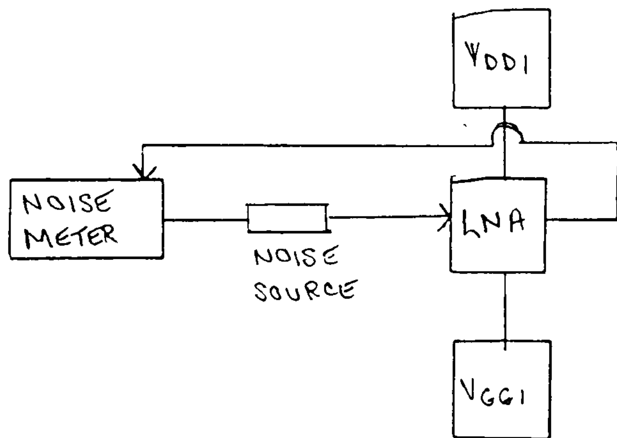


FIGURE 11 TEST SETUP

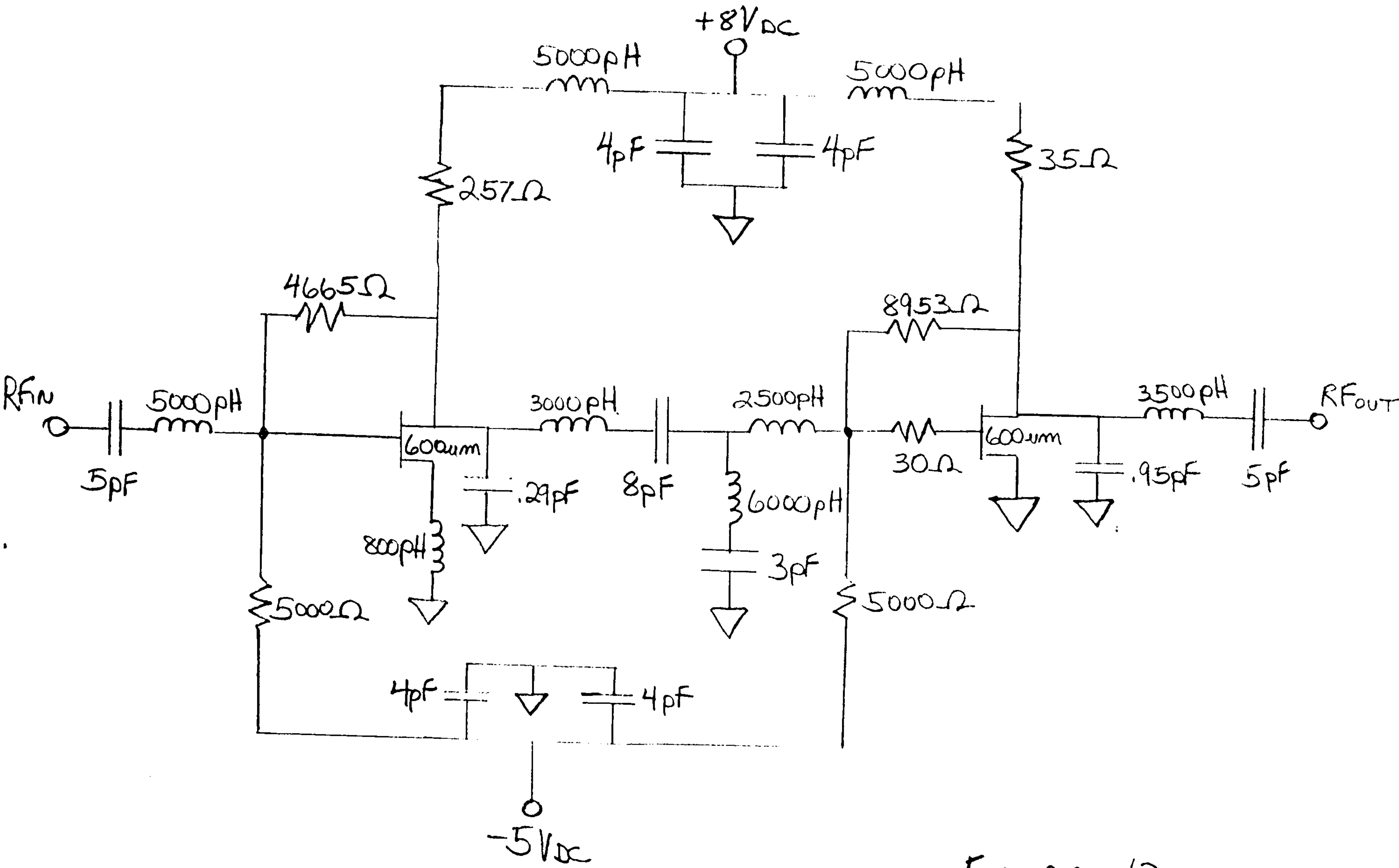


FIGURE 12.
MMIC SCHEMATIC

Conclusions and Recommendations

All design specifications were met or exceeded with the exception of using a single +5 Volt power supply. It was necessary to use two power supplies in order to achieve the gain and noise figure specifications in the allotted design time. If the MMIC is to be designed using only one power supply, the biasing circuit would probably be a bit more elaborate than a three resistor voltage divider network. Therefore, more real estate must be available for a one power supply bias circuit. In order to make more room available on the Anachip, the number of inductors in the matching networks must be reduced. Ideally the matching networks should consist of only capacitors if possible since the inductors are lossy and real estate hungry. Also, if a power supply sensitivity specification were to be added, then active Fets or diodes would be present in the bias network. Once again more real estate would be needed for the bias circuit resulting in the need for a more compact LNA design.

S Band

Voltage Controlled Oscillator

by

Mark Gorbett and Ashraf Sherif

Microwave Monolithic Integrated Circuit Design
EE 525.787

Instructors: Craig Moore / John Penn

ABSTRACT

The design of a S-band MMIC voltage controlled oscillator is described is this paper. The VCO will be fabricated on a 60 X 60 mil ANACHIP,using the Triquint HA2 process. The VCO is to operate in the frequency band of 2.4 to 2.48 GHz and deliver 10 dBm output power. The design was accomplished using small signal and nonlinear methods to ensure the correct start-up and steady state oscillation frequency.

1) INTRODUCTION

Modern microwave systems make extensive use of microwave oscillators. The complex nature of these devices make the oscillator field very interesting and challenging. There are two basic categories of oscillators, feedback and negative resistance.

1.1 Circuit Description

In this paper a negative resistance approach was chosen. A common gate FET together with a resonator were used as a one port VCO. The VCO was followed by a common source buffer amplifier as shown in figure 1. The buffer amplifier is used to provide reverse isolation and to minimize any pulling effects by an external load. The amplifier will also increase the overall output power. The FET is made unstable(K<-0.7) by adding an inductive element between the gate and ground. A varactor is connected to the source for tuning the frequency range. See figure 1.

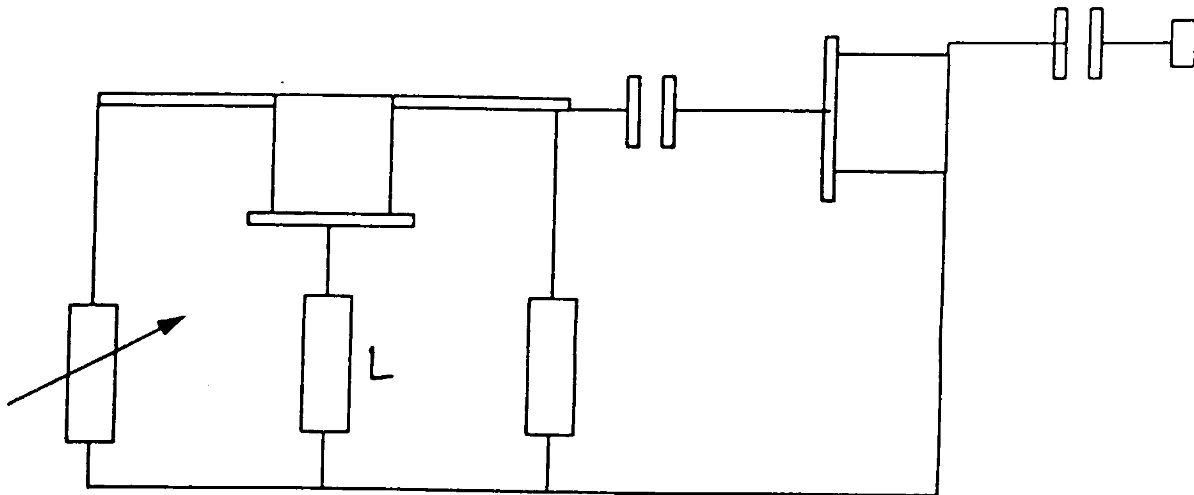
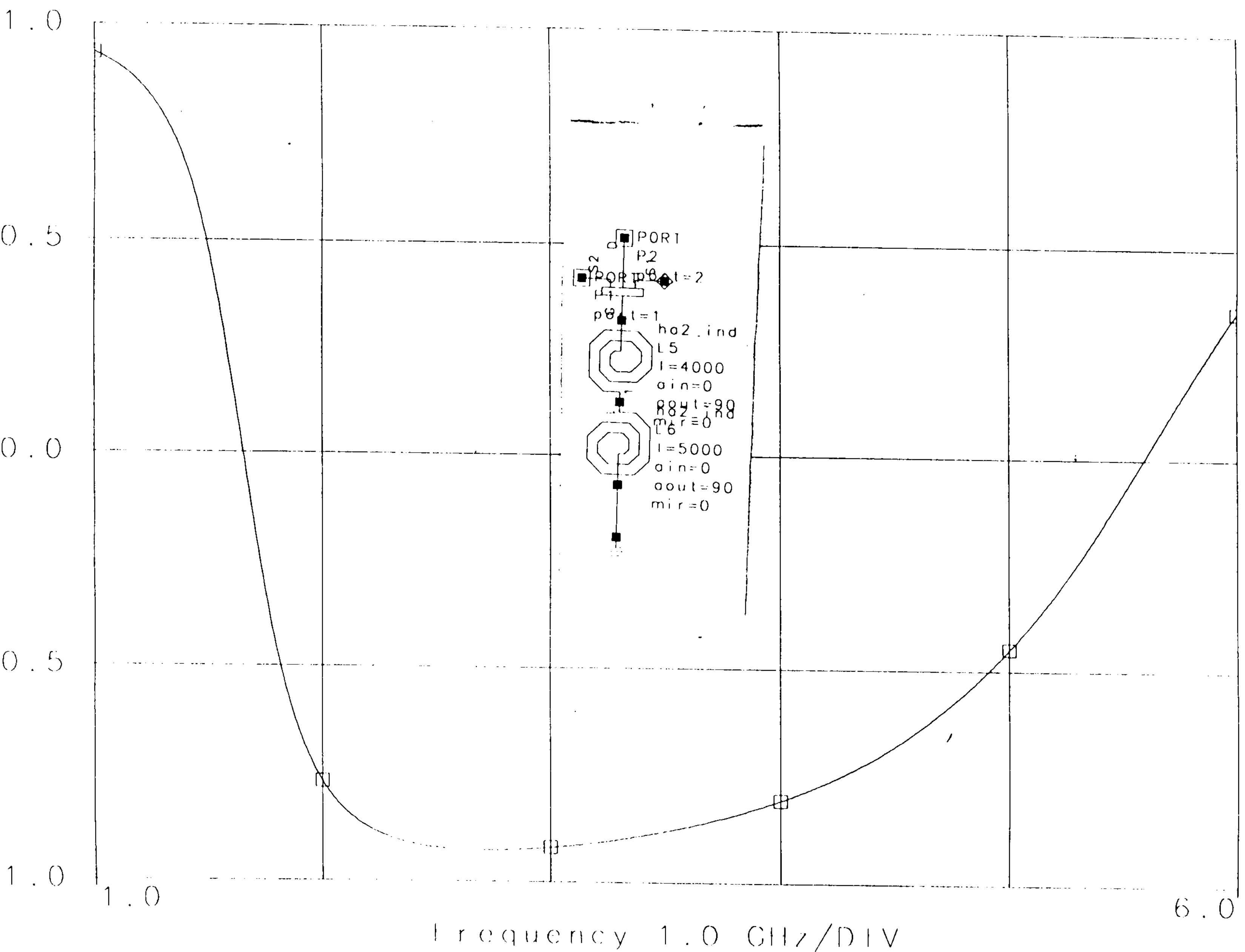


Figure 1

Figure 2



1.2 Design Philosophy

In this design, we followed the classical oscillator theory approach of negative-resistance oscillation. The microwave oscillator is modeled as a one-port where the real part of the port impedance is negative. The oscillator modeled is shown in figure 3.

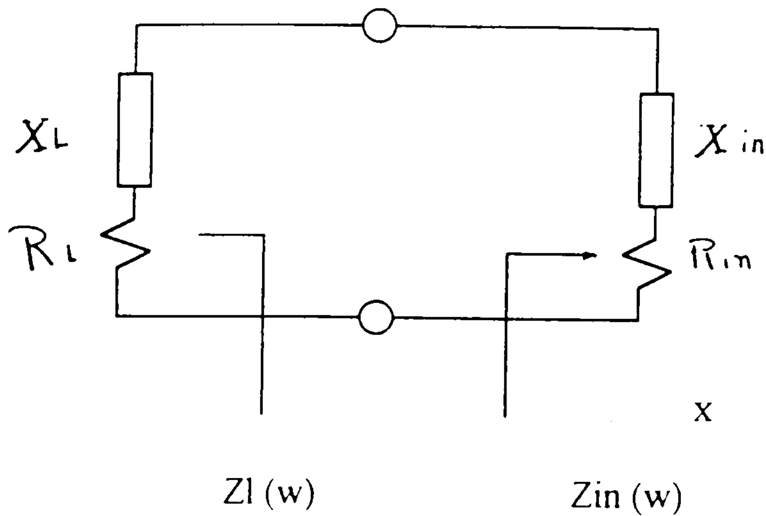


Figure 3

where the oscillation condition is

$$Rin + Rl = 0$$

$$Xin + Xl = 0$$

Although oscillators are in reality a large-signal nonlinear component, small-signal linear considerations are usually sufficient to ensure oscillation conditions. The approximate operating frequency is established at the beginning of the oscillation and before the output level reaches saturation.

Our approach to the oscillator design is as follows

1. Choose circuit topology (common gate in our case)
2. Generate and implement instability (gate inductive feedback)
3. Load the device with unstable termination on one port; should have negative resistance
4. Design a resonator at the desired frequency and maintain oscillation in steady state.

The above steps ensure that the oscillation will start at the desired frequency. They do not establish the amplitude or frequency of the large signal steady state. Therefore, we used the nonlinear model in our analysis to accurately predict the output power and steady state oscillation. Also, the phase noise and harmonic performance were estimated.

2. Modeled Performance

The goal for the output power of the VCO is 10 dBm, a 300 um FET is appropriate for this design. The drain is biased to +5V, the gate is grounded through an inductance of 12nH to increase the instability of the device.

A varactor-tuned parallel resonator is connected to the source. The parallel resonator, consists of an inductor in parallel with a varactor diode. The varactor diode was made using two 100 um FETs in parallel with the source and drain connected. Two 100 um FETs were used to provide enough capacitance to tune the VCO's frequency over the required range. The varactor is connected to the source through a series capacitor. The series capacitance sets the frequency for the tunable range. The circuit is designed to satisfy the equation of oscillation

$$S11 = 1/\Gamma r$$

S11 is the reflection coefficient of the active device and Γr is the reflection coefficient of the resonator. The drain is connected to a coupling capacitor as shown in figure 2.1.
Figure 2.2 shows the equivalent circuit of the varactor used in the simulations.

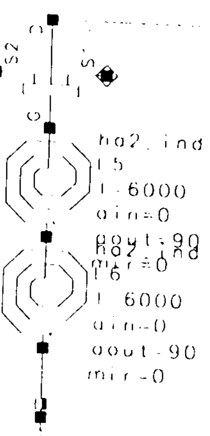


Fig 2.1

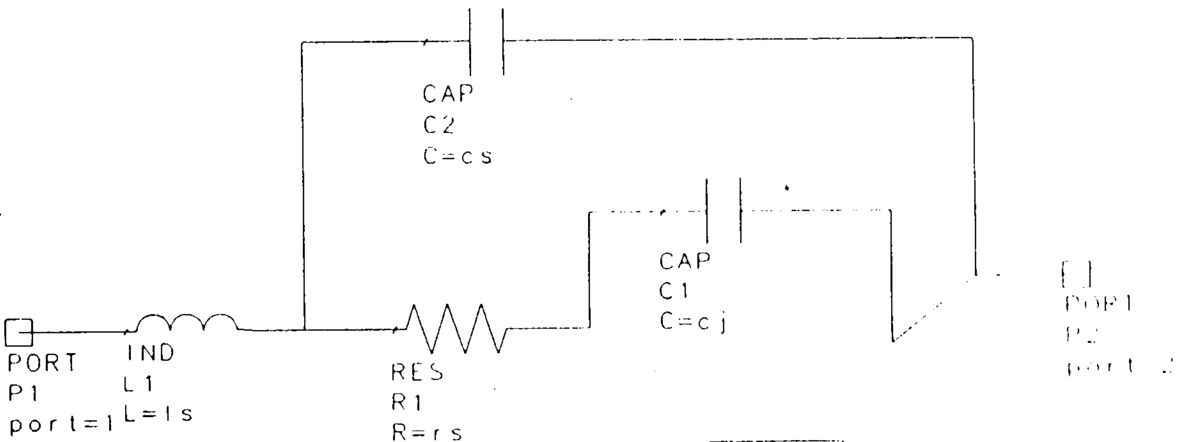


Figure 2.2

2.1 Pre-layout Predicted Performance

Preliminary analysis of the pre-layout schematic using small signal analysis indicated that the circuit is satisfying the oscillation conditions S11 > 1 and phase = 0 degrees. The oscillation conditions were met over a wide frequency range as shown in figures 2.1.1 and 2.1.2. Figure 2.1.3 shows the frequency of oscillation across the band.

Figure 2.1.1

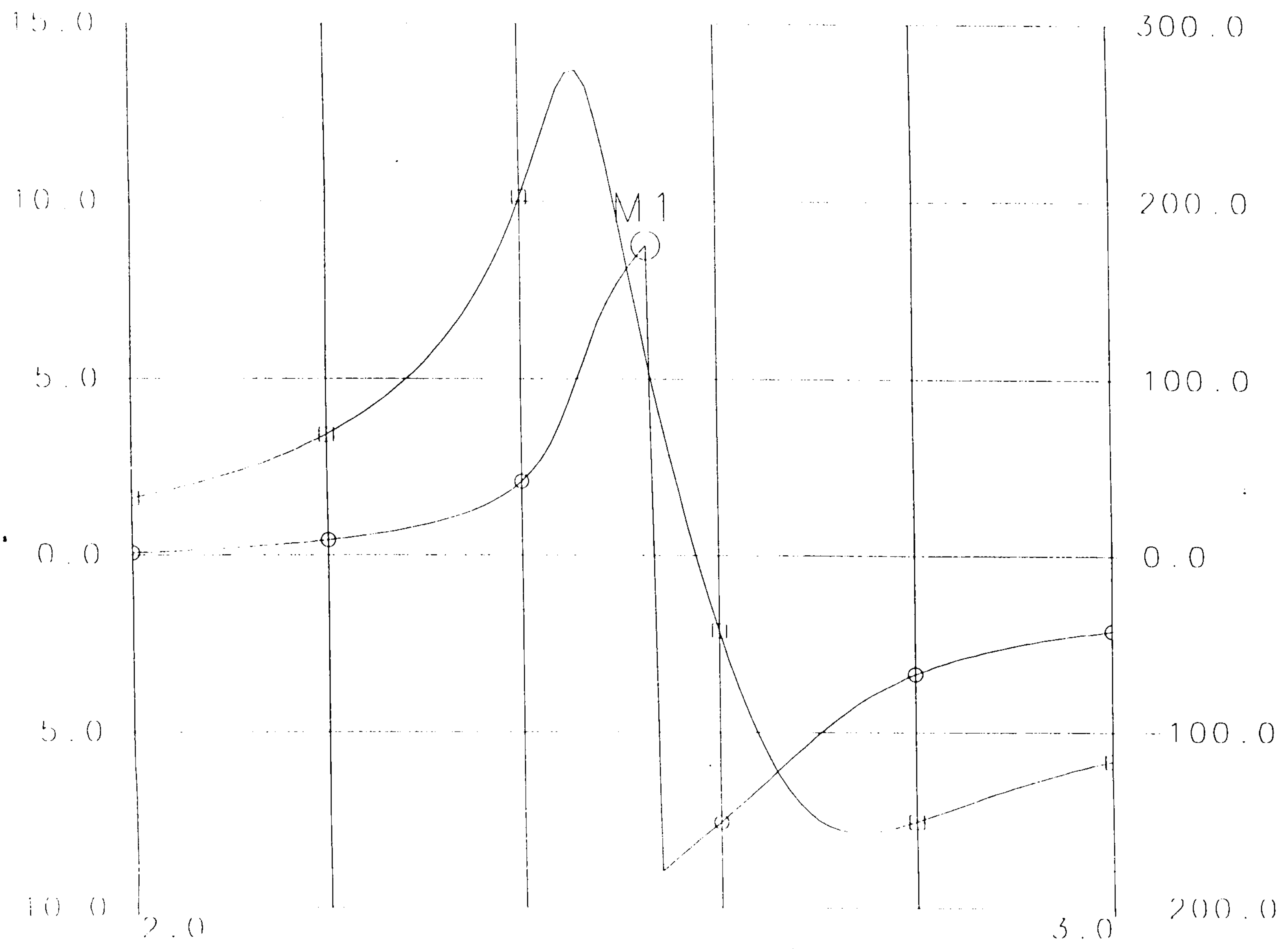


Figure 2.1.2

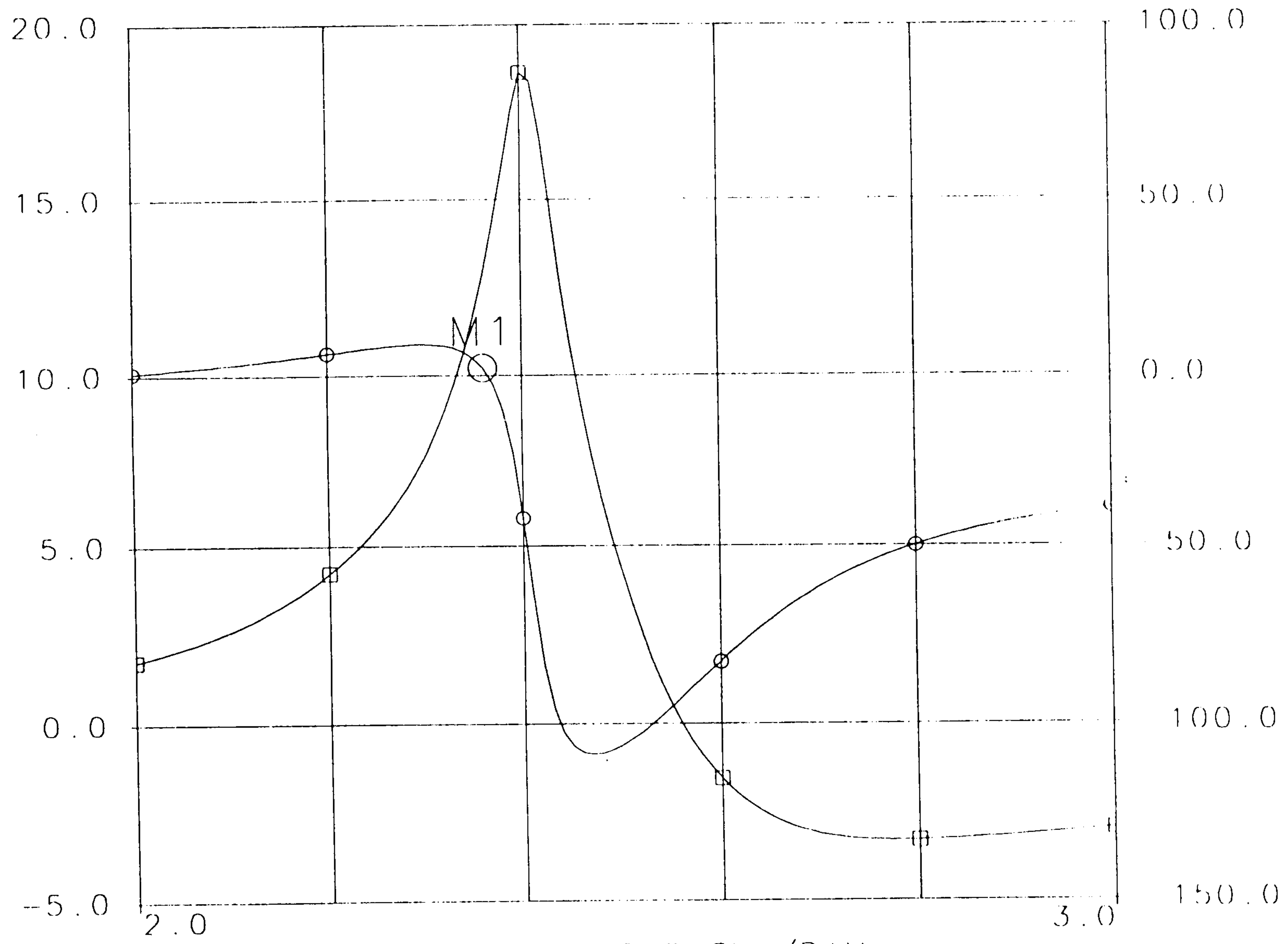
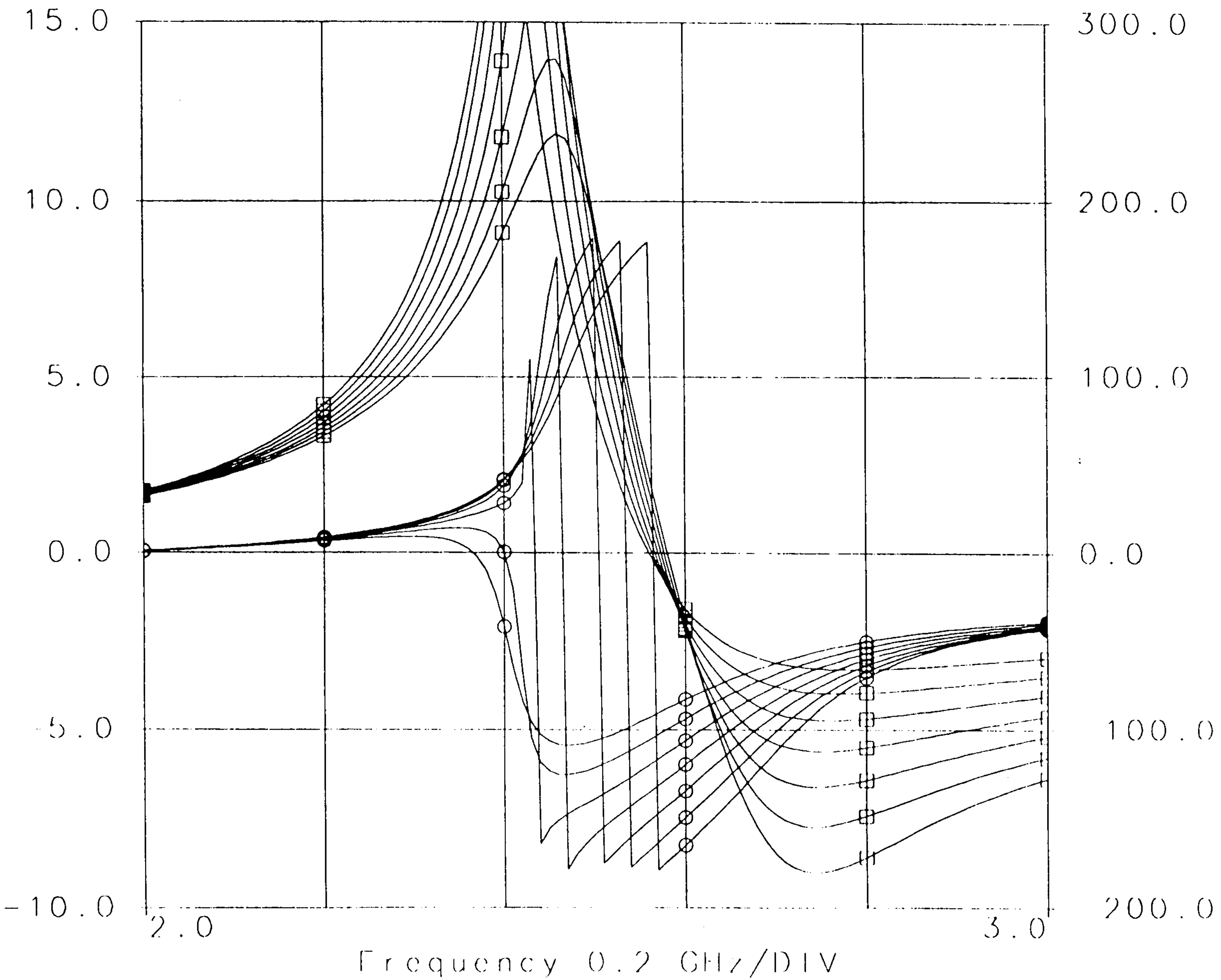


Figure 2.1.3



2.2 Post-layout Predicted Performance

The layout of the VCO and the amplifier is shown in figure 2.2.1. A final schematic was generated from the layout. The VCO's final schematic is shown in figure 2.2.2 where the two varactors were replaced by the equivalent circuit. Analysis was done separately on the VCO and amplifier. The predicted performance is shown in figures 2.2.3 and 2.2.4. Figure 2.2.5 shows the predicted performance of the tuning range.

From the phase plot, it is observed that the slope is very steep at the zero crossing, indicating a good short term stability (phase noise). The phase noise will be investigated further with a noise analysis with one of the noise test benches.

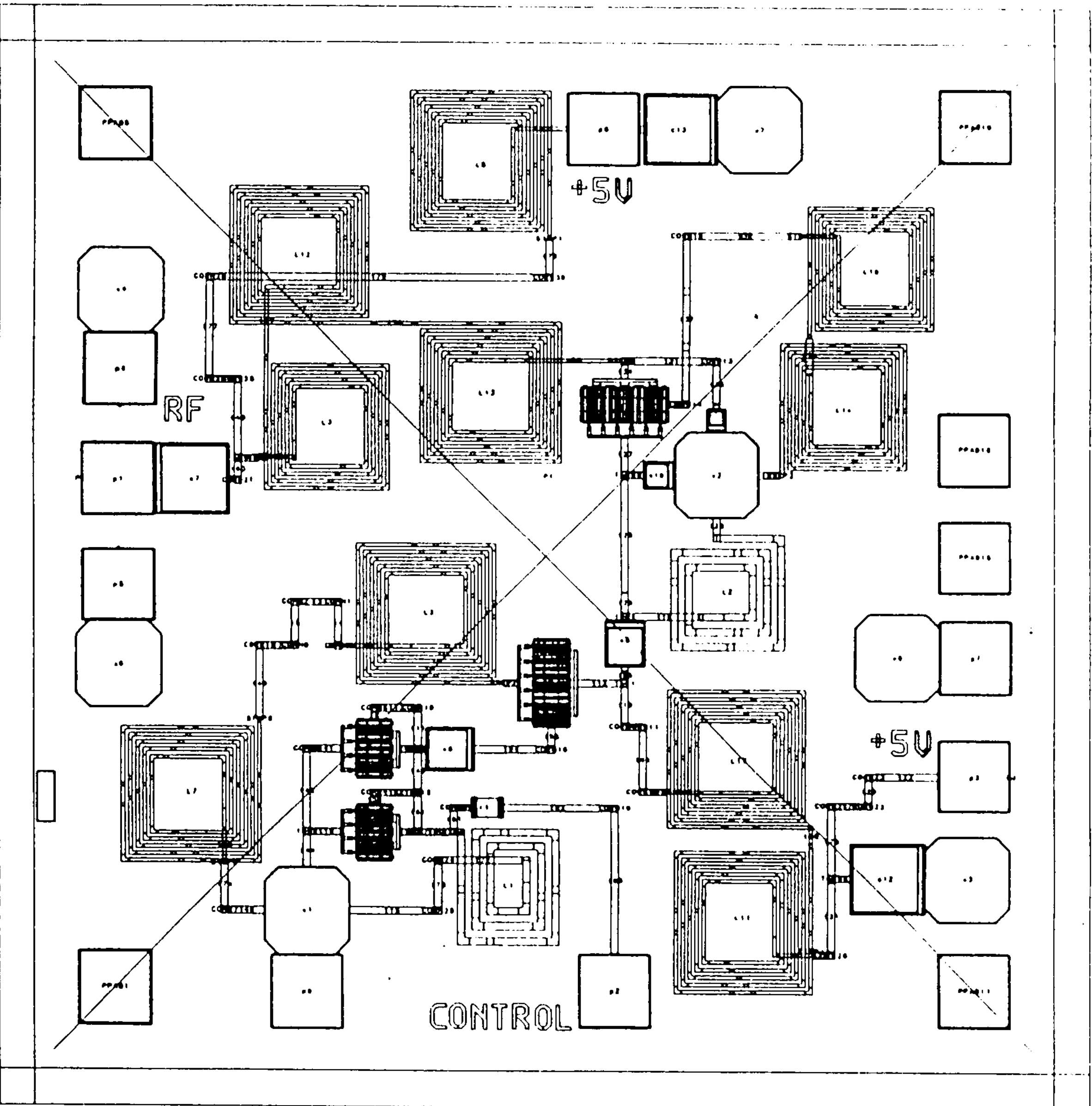


Figure 2.21

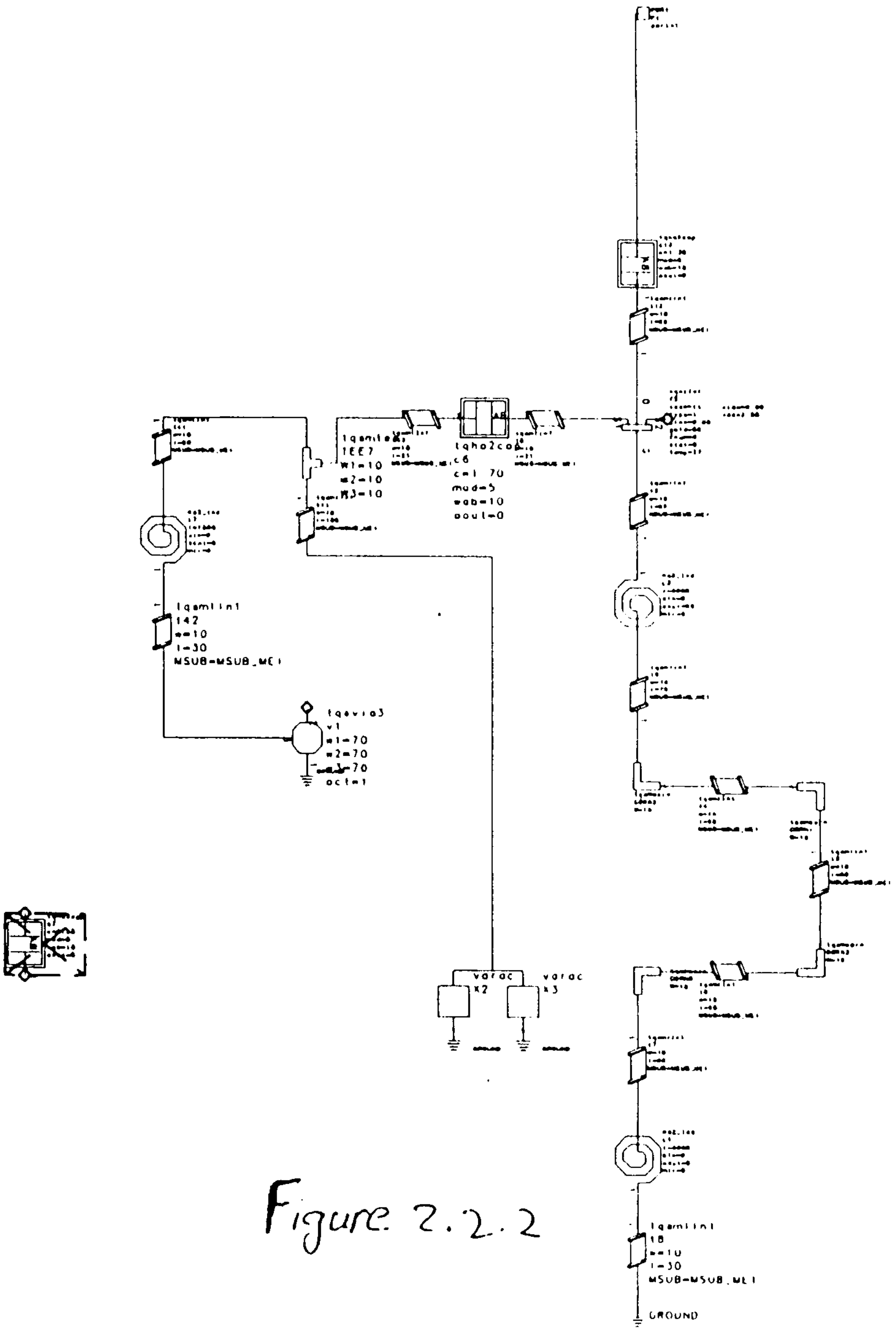
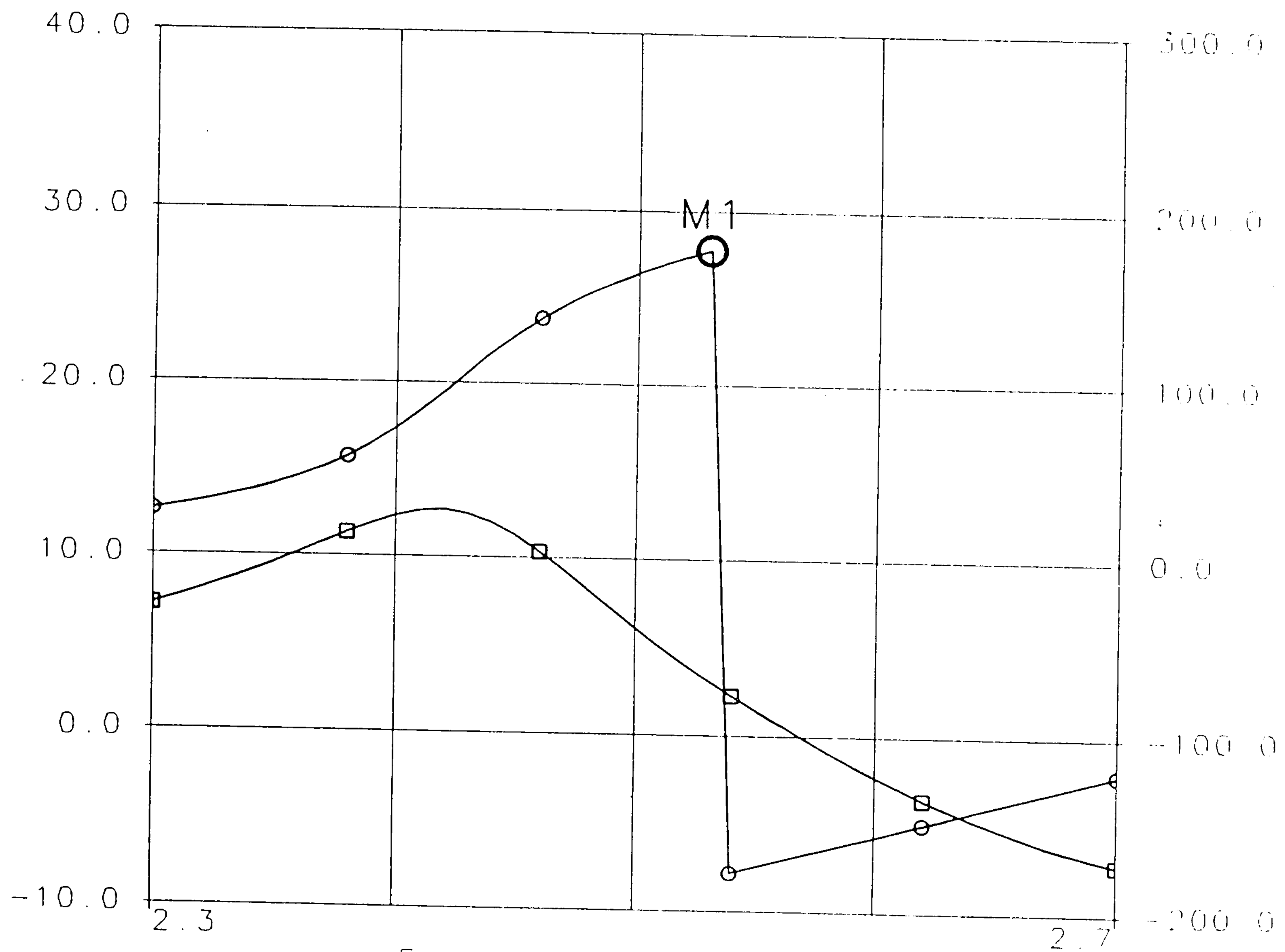


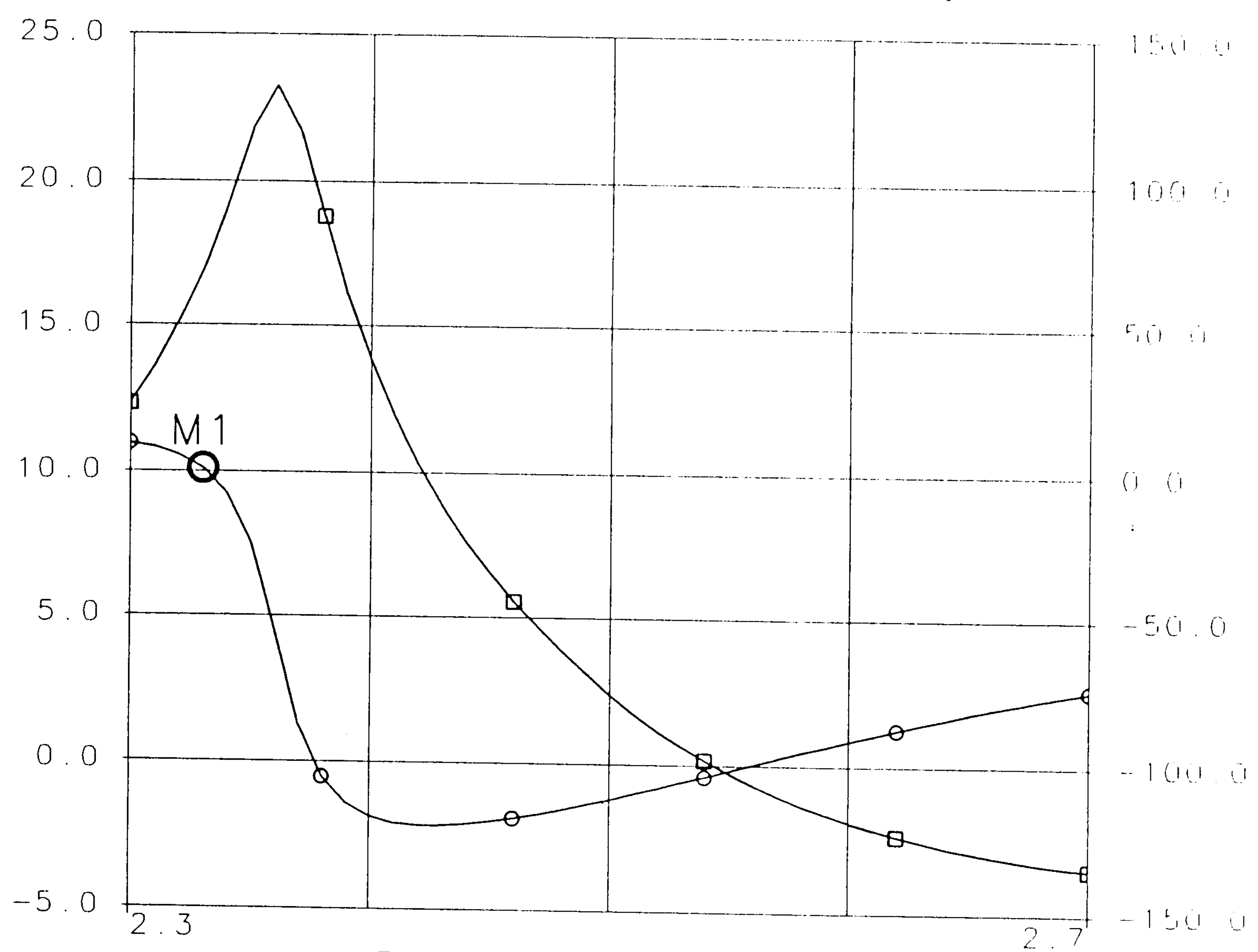
Figure 2.2.2

Figure 2.2.3



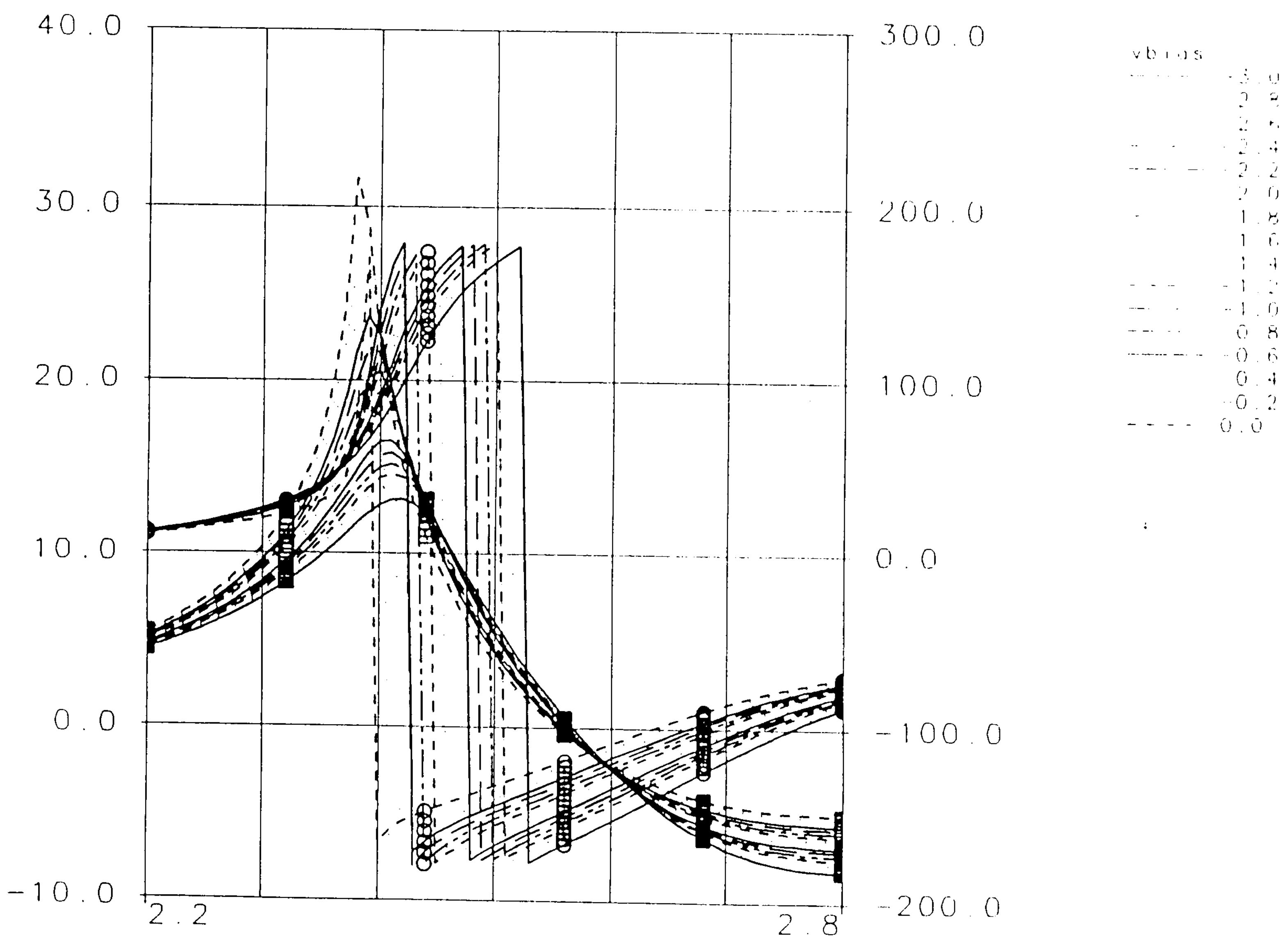
M1 Frequency=2.5300000 value=178.039830

Figure .2.2.4



M1 Frequency=2.3300000 value=1.29283931

Figure 2.2.5



2.3 Nonlinear Analysis

Using EESOF Libra's oscillator test bench a nonlinear analysis of the VCO was performed. The output power, harmonics and phase noise were predicted. Figure 2.3.1 shows the output power to be more than 14 dBm, and the first and second harmonics are less than -5 dBm. Figure 2.3.2 shows the predicted phase noise of < -37 dBc/Hz at 100 Hz offset, and decreasing by 20 dB per decade. Figure 2.3.3 shows the phase noise with a different scale and Figure 2.3.4 is a plot of the time domain results.

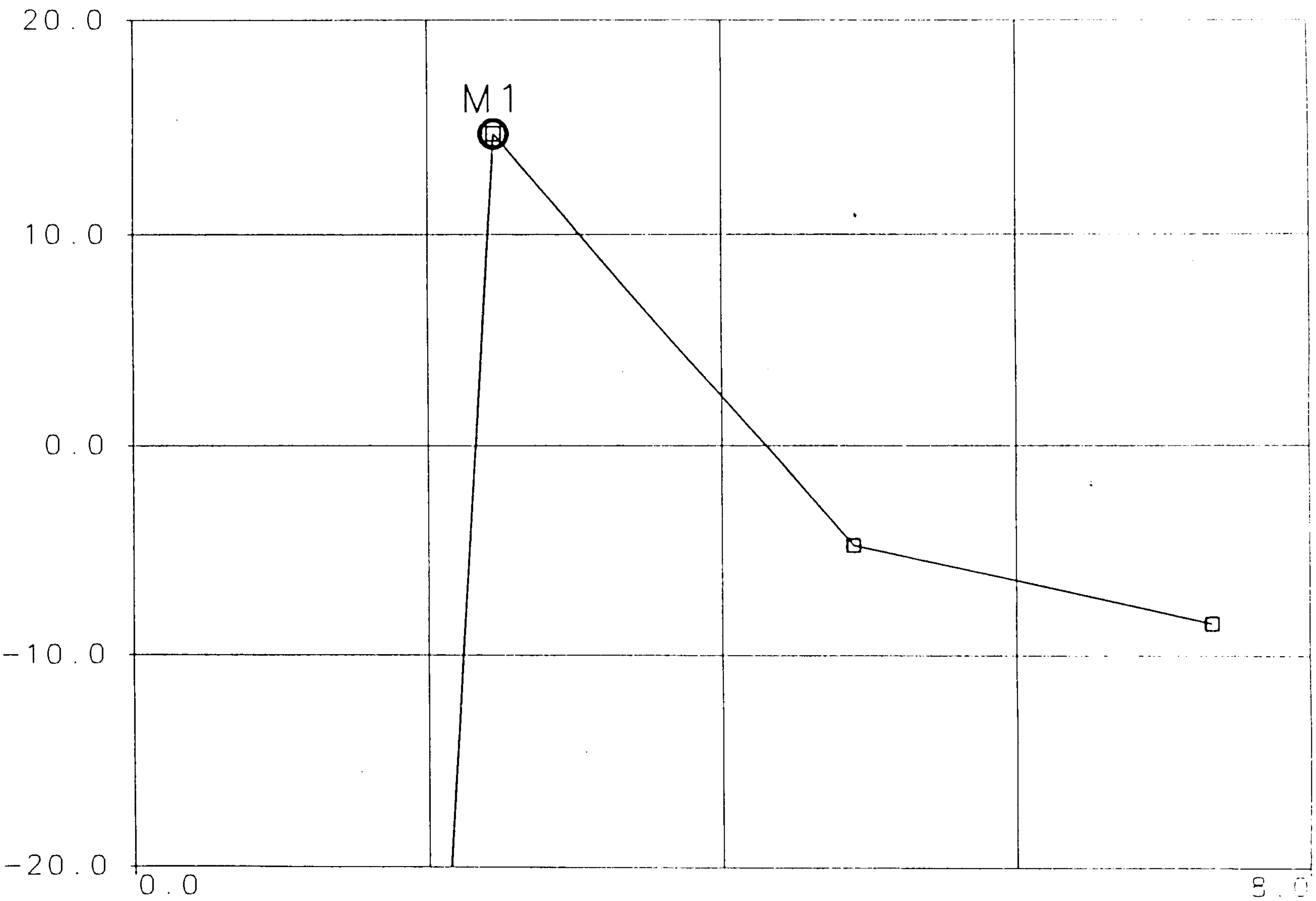


FIG 2.3.1

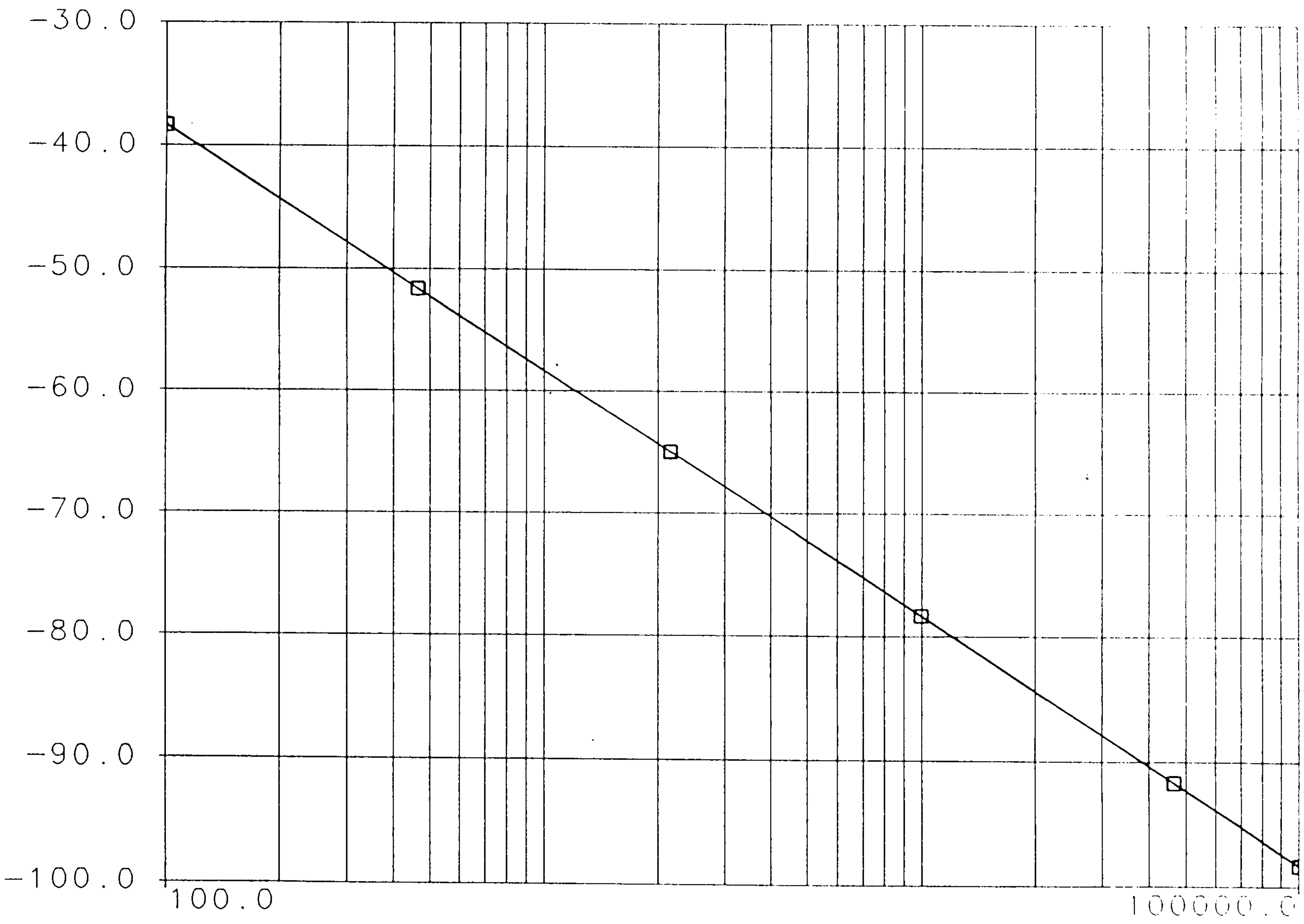


FIG 2.3.2

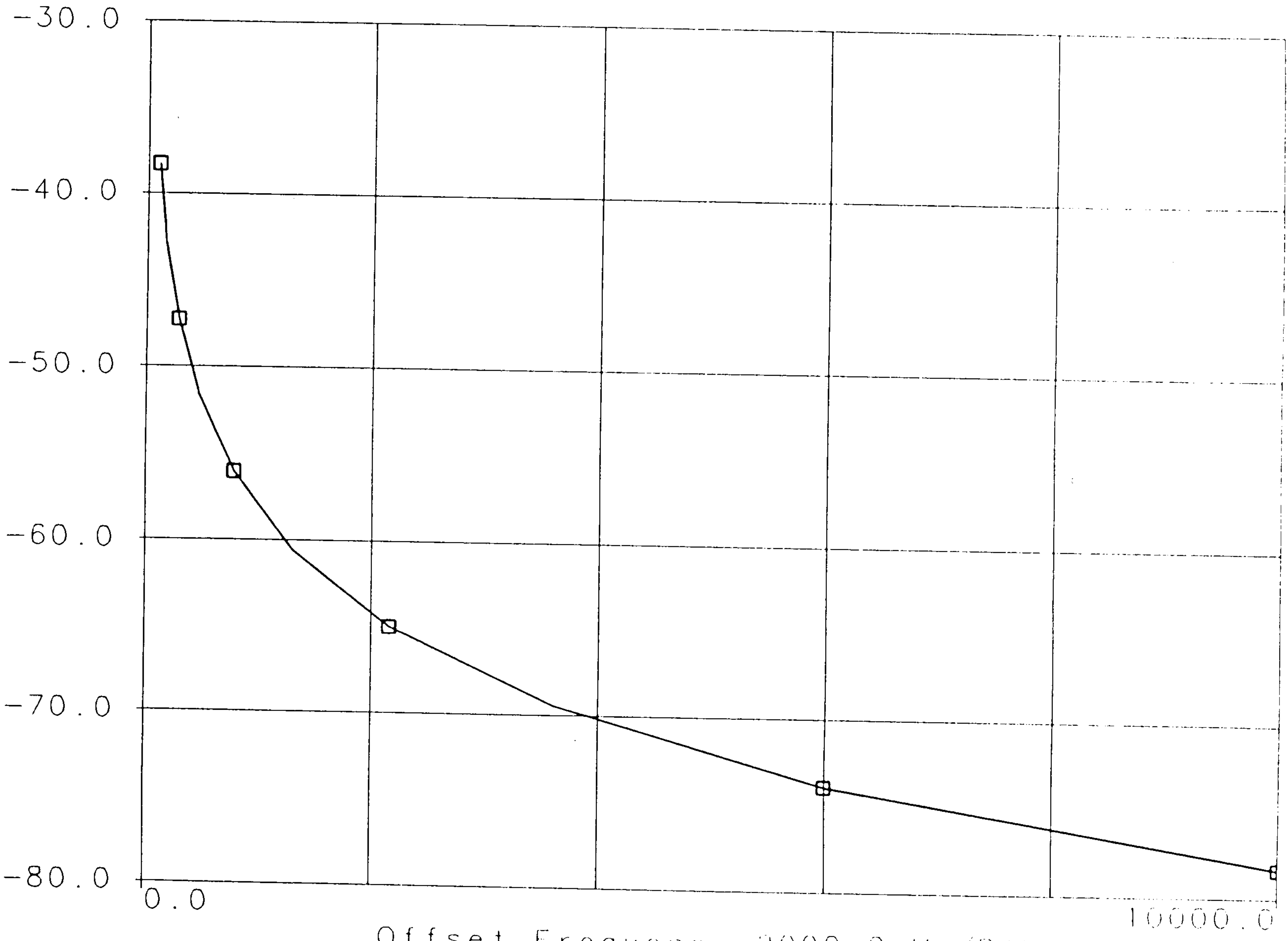


FIG. 7.3.3

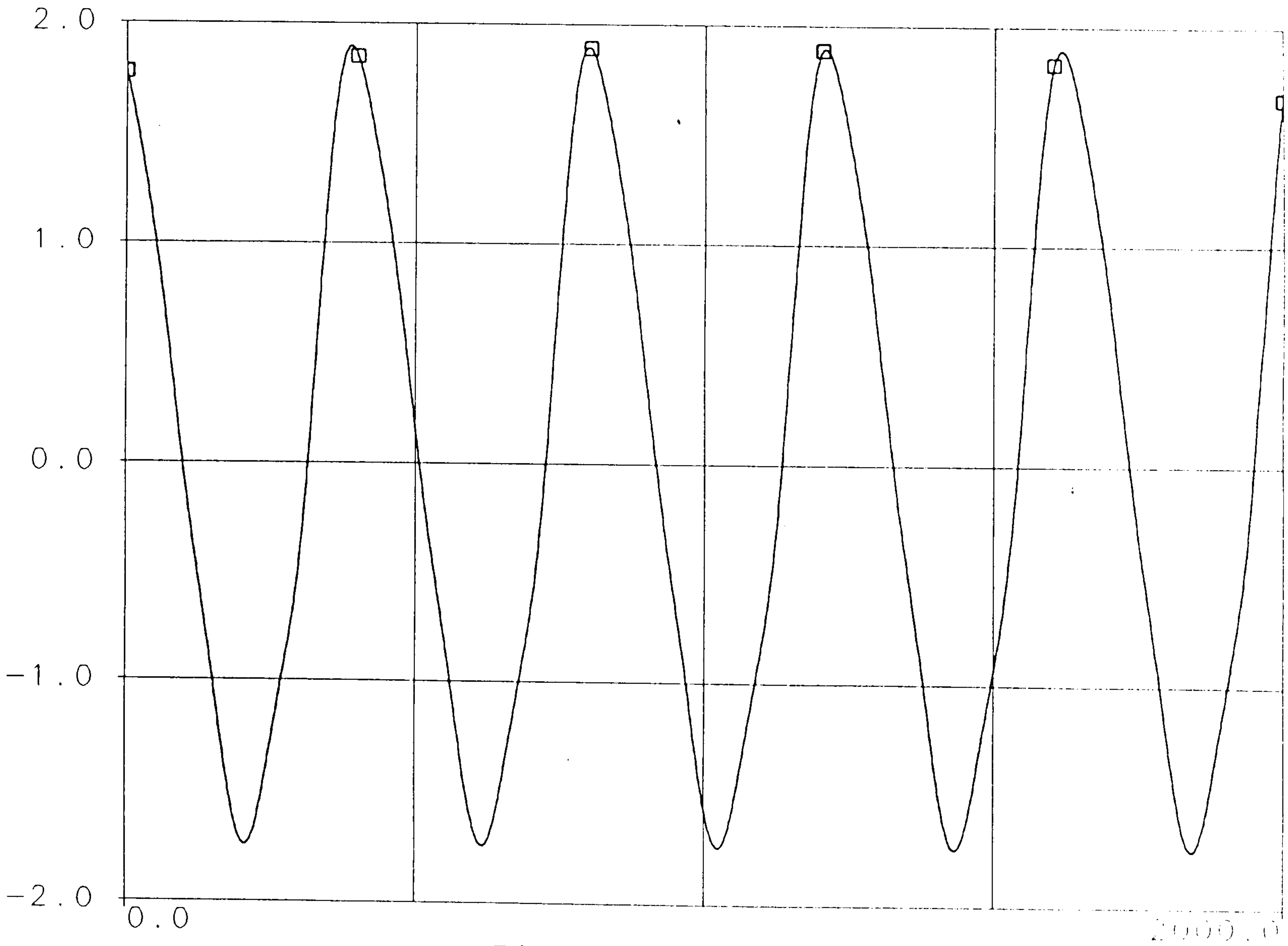
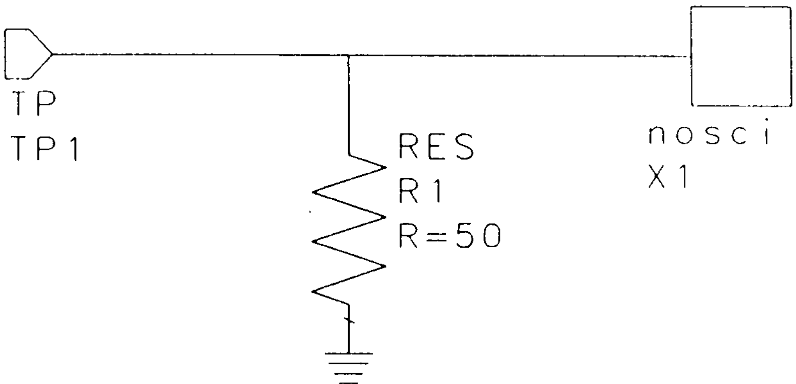
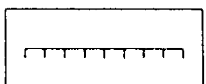
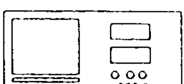


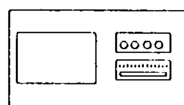
FIG 2.3.4

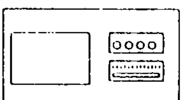


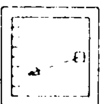
PSPEC
PSPEC1
TP1ID=TP1
TP2ID=gnd
ELEM=R1

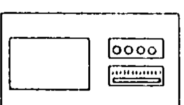


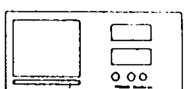


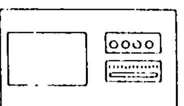












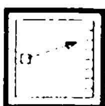


FIG 2.3.5

2.4 The Buffer Amplifier

A 300 um FET was chosen for the buffer amplifier. The amplifier is required to provide isolation for the VCO. The design goal is to have an amplifier with a very high input impedance (in order not to load the VCO), and output matched to 50 ohm.

Figure 2.4.1 shows a detailed schematic generated from the layout. A summary of the amplifier performance is shown in Figure 2.4.2. The gain is about 2 dB less than the maximum available gain. The isolation is better than -14 dB.

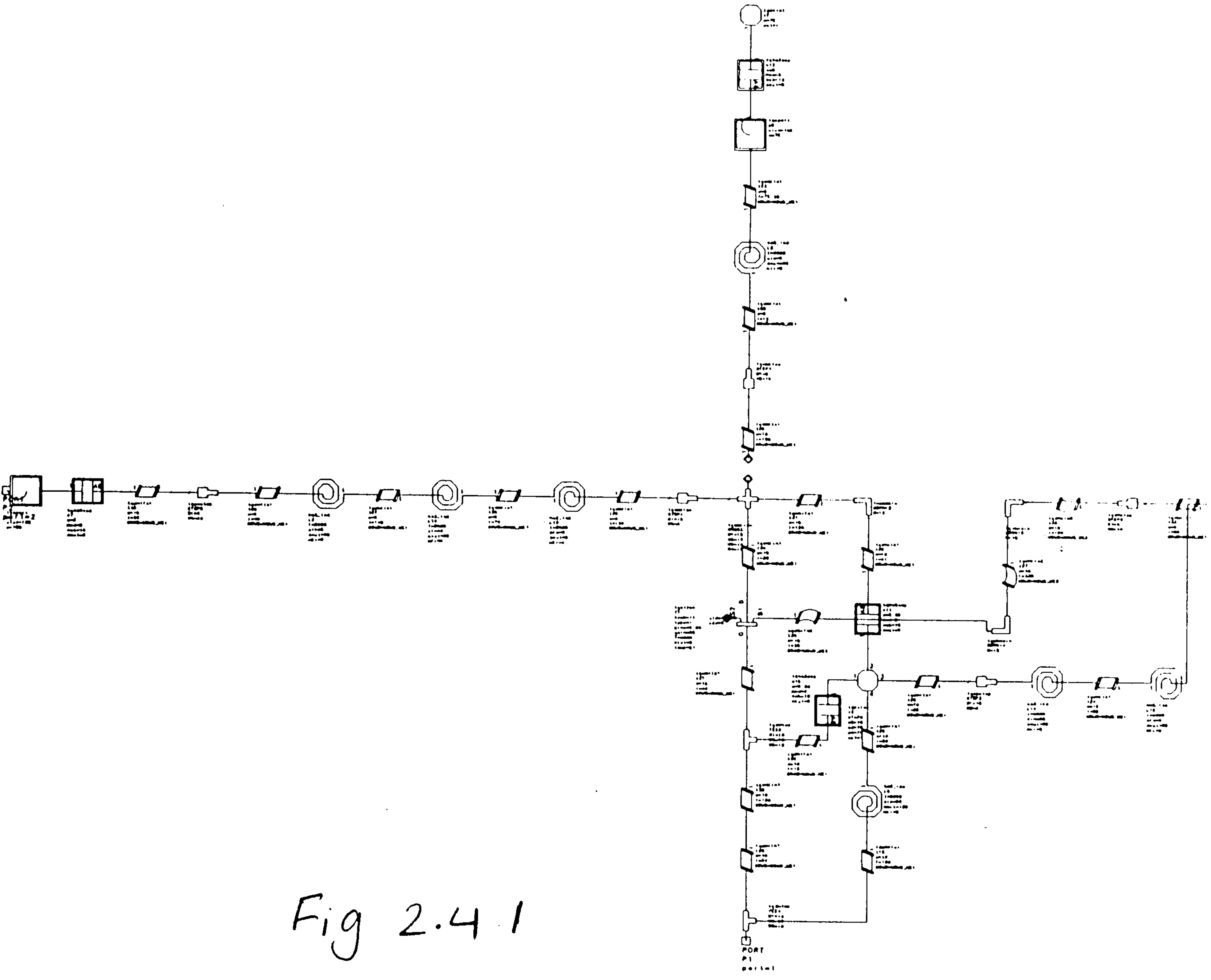


Fig 2.41

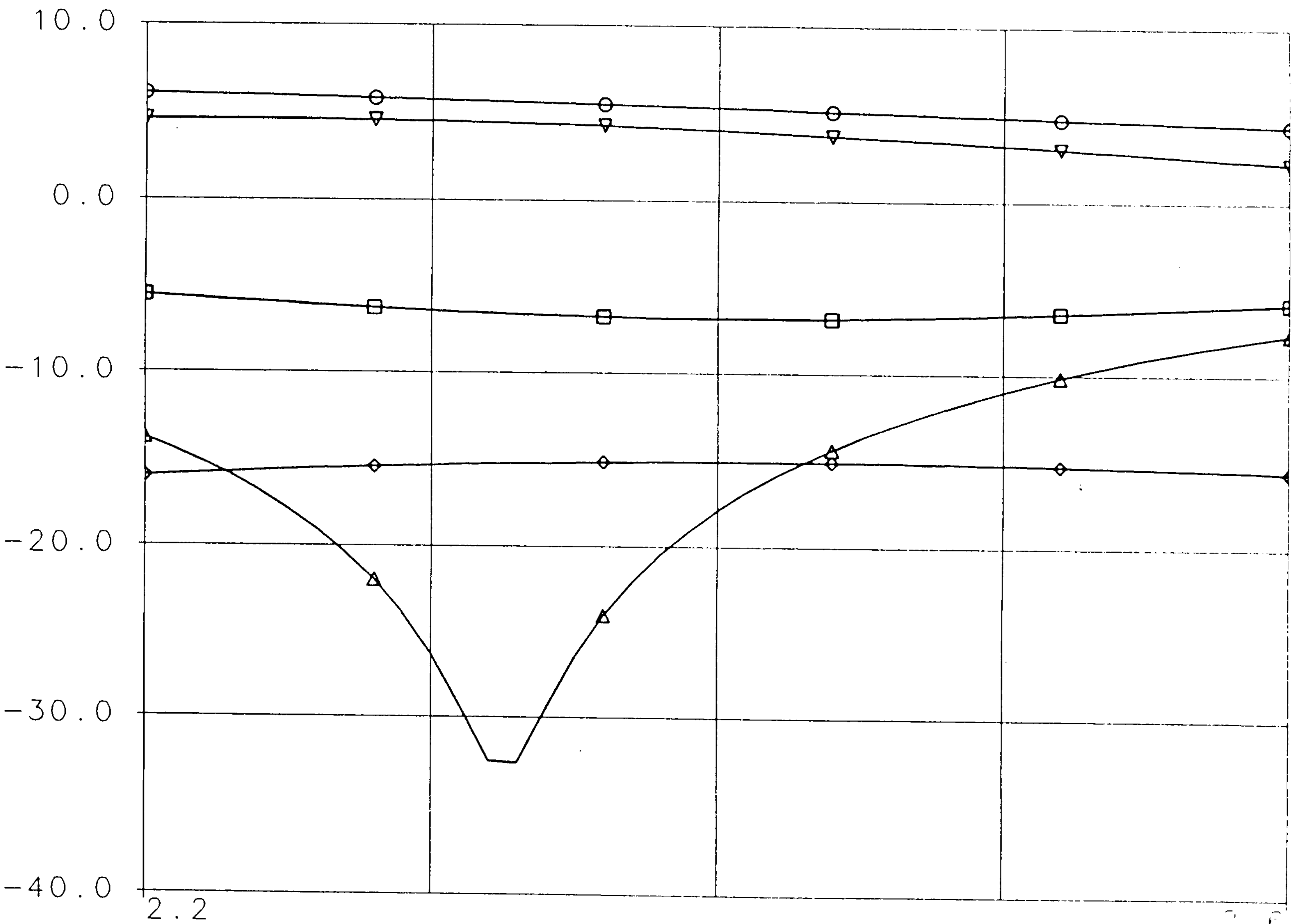
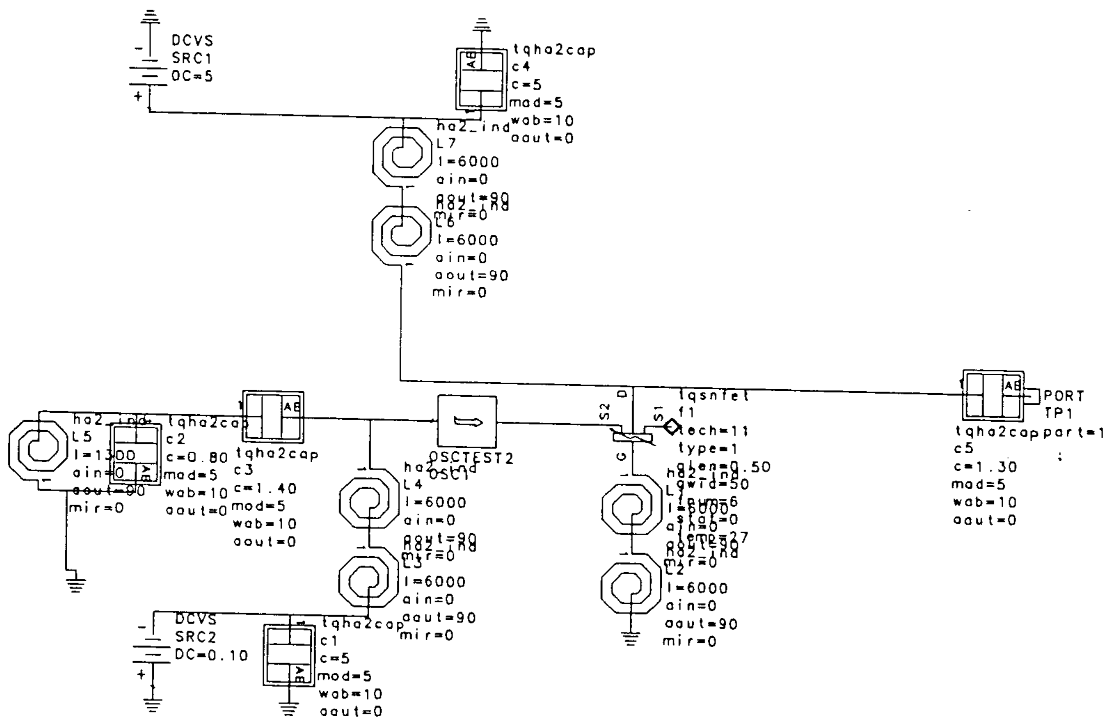


Fig 2.4.2

3. Conclusion

Analysis of the final design agrees with what was expected with little variation from the ideal circuit. The actual circuit is expected to be close to the predicted performance.



DCVS
SRC1
OC=5
tqha2cap
c4
c=5
mad=5
wab=10
aout=0
ha2_ind
L7
l=6000
ain=0
L6
l=6000
ain=0
aout=90
mir=0
PORT
TP1
tqha2capport=1
c5
c=1.30
mad=5
wab=10
aout=0
tqsnfet
f1
tech=11
type=1
OSCTEST2
OSC1
L4
l=6000
ain=0
l=6000
ain=0
aout=90
mir=0
L5
ain=0
mir=0
tqha2cap
c2
c=0.80
mad=5
wab=10
aout=0
tqha2cap
c3
c=1.40
mod=5
wab=10
aout=0
DCVS
SRC2
DC=0.10
tqha2cap
c1
c=5
mod=5
wab=10
aout=0
L2
l=6000
ain=0
aout=90
mir=0

Driver Amplifier
MMIC Design 525.787

Steven Grice Neal Matovelle

Fall 1996

Summary

DRIVER AMPLIFIERS are used extensively in communication systems (i.e., cellular telephones), and transmitters to provide amplification of desired signals. This driver amp is suitable for use in the new 2.4GHz ISM Band. This amplifier is being designed as a driver for the power amplifier. It is also suitable as the transmitting amplifier in a low power spread - spectrum application, a buffer amp for the VCO, and as a receiving amplifier with modest noise figure performance. The amplifier design and layout are created within the specified requirements and guidelines.

To insure excellent VSWR properties a reduced size 90deg hybrid technique was developed and fabricated in the design. A 0.5Watt/mm FET ratio was used to provide a first estimate of the necessary size to meet P1dB. Also, the properties of a FET that effect Nf_{min} were reviewed to better estimate the Noise Figure for various FET biases and size parameters. The chip needs no external components for performance or stability and is contained within a 60 by 60mil die.

Introduction

The driver amplifier consists of a branchline type hybrid at the inputs. This provides two signals 90 degrees out of phase (in quadrature) of equal amplitude. Each path is connected to an input matching network, followed by a single FET. The signal from each path is then recombined in an output hybrid. Use of the hybrids ensures excellent VSWR results because the reflected signals from the FET's are combined into an internal load. The effect also allowed the matching networks to be developed without VSWR being the predominate concern. Therefore a degree of freedom was realized.

To implement the coupler, a standard 1/4 wavelength hybrid, or one using the L-C equivalent network, are too large for this application. From analysis of the coupler properties, a hybrid with 2 inductors and four capacitors is concluded. It is not normally implemented this way because of very low bandwidth. However, for our application, the available bandwidth of about 3% is satisfactory.

There exists in this specification a simultaneous Noise Figure and P1dB requirement. In reviewing the power requirement, a very small FET was acceptable (+17dBm could be provided by one 100um FET). However the NF for a FET is inversely proportional to the FET's size, since larger FET's have smaller Source resistance (a smaller r_n). See Equation 1 below.

$$F = F_{min} + r_n / g_s \cdot |Ys - Yo|^2 \qquad \text{Eq. 1}$$

Where

Ys = Source admittance,

Yo = Source admittance for minimum noise figure

Another consideration is that a smaller FET size is more difficult to match even over a low bandwidth. On the other side, in very large FET's the Drain to Source resistance decreases, which requires more bias current. A compromise between these concerns was accomplished with the use of 2, 600um FET's in the design. From available Noise Figure

data on the TriQuint 300um FET and extrapolating to our size, we estimate the FET Noise Figure to be 3.8dB. Including the input hybrid resistive losses (0.4dB), the driver amplifier Noise Figure data is estimated at 4.2dB. This is within the $\leq$ 6dB goal.

Throughout the design, the bias was repeatedly being reviewed. It is desired to connect the bias to a low impedance point on the circuit, to maximize the ratio between RF and bias impedance. Initially the bias was just done only using large 5 to 10nH inductors. If applying these inductors to the circuit caused an appreciable effect, then the inductor was connected to a high impedance point. Most of the initial matching was done without a bias network. This allowed us to determine if certain matching networks were "on track" without concern about improper bias. Some articles and vendor databooks were reviewed to see how others implemented bias. Single voltage bias, and separate gate and drain bias techniques were considered.

To match the FET's a smith chart technique was first used. However this approach became ineffective because when developing an input matching network (IMN), S22 > 1. Also S11 > 1, when developing an output matching network (OMN). So a simultaneous match was required. However development of separate matching networks was useful in the sense that it provided a starting point. Optimizing for gain and checking for stability were the primary goals at this stage. The individual stage (IMN - FET - OMN) met gain and P1dB designer goals of 18dB and +16dBm before combining the hybrids.

The hybrids were now added to the design. A benefit was provided here because it was learned that part of the IMN and OMN could be implemented in the hybrids. This reduces the total number of elements in the layout. The resultant IMN became a hybrid at the input, followed by a series and shunt inductor. The series inductor is required for placement of T(in) near T(opt). The shunt inductor rotates T(in) towards a power gain circle. Hence a compromise of where to put T(in) on the constant noise and power gain circles is made. The resultant OMN is simply the hybrid on the output. Initial circuits showed the gain and P1dB to be within acceptable limits.

The next step was to replace the inductor and capacitors in the schematic with TriQuint elements. The effect was to detune the response, degrade the VSWR, and lose about 2.5dB of gain overall. The P1dB stayed at about 20dBm, providing reasonable margin. In tuning the unit, the models for linear and non-linear simulations were checked and found not to be exactly the same with respect to bias. When corrected, the P1dB was no longer in specification. By performing some trials, it was determined the change that would repair this with minimum effect to the linear circuit analysis was to adjust the bias from 50 to 60% Idss. With the unit being retuned at this stage, and performing many iteration cycles, the Gain and VSWR requirements could be obtained.

Bias was also checked for size, and effect on electrical performance. With the TriQuint elements in the circuit analysis, the single bias method was implemented without significant change to performance. The main requirement is to use a sufficiently large capacitance for the bypass capacitor. A value of 4pF was selected since it did not

degrade performance and has enough margin with respect to a 5% fabrication tolerance. Other considerations for the single bias technique were the elimination of oscillating due to separate bias lines feeding back on each other in the layout. Also, the shunt inductance at the input for the IMN allowed for implementation of a single bias design. The overall size of the bias was also reduced with single bias verses dual bias. This tradeoff was between using two bypass capacitors, inductors and resistors, verses 4 inductors, 1 resistor and routing a gate bias line to the perimeter of the chip. To layout an 8ohm resistor in the circuit, four 32ohm resistors had to be placed in parallel (all TriQuint resistors are $\geq$ 25ohm). However in using single voltage bias, the availability to adjust the gate with an external voltage source is eliminated. The gate voltage bias is expected to range less than 0.05V with respect to processing variations.

Modeled Performance

Parameter	Specification	Result
Frequency	2400 to 2483mhz	Compliant
Bandwidth	>83mhz	Compliant
Gain	>15dB	15.5dB
Gain Ripple	+/- 0.5dB	+/- 0.5dB
Output Power	> 17dBm at 1dB compression	>20dBm
Noise Figure	< 6dB goal	4.2dB estimated
VSWR (wrt 50 ohms)	<1.5:1 Input and Output	1.5: 1 Worse Case
Supply voltages	TBD	5.0V at 120mA
Size	60 X 60 mil ANACHIP	Compliant

DC Analysis

Within DC Analysis, 1) the inductors and m-lines that carry DC voltages must be capable of conducting the expected current, 2) the DC bias circuit must provide the correct bias to the FET's, and 3) the circuit implementation must not degrade the RF performance.

Each item will be addressed separately.

1) The mlin 1,2 and mlin1+2 can conduct 9,18, and 27mA/um linewidth respectively. The TriQuint inductors are essentially mlin1+2 metal, with the smallest line width being 5um. Therefore the inductors can carry $\geq$135mA. This will satisfy our case, with 100mA expected current. For the transmission lines that carry bias, keep the conductor width $\geq$10um for mlin1, and $\geq$5um for mlin2, which provides an acceptable current level of 180mA along any lines.

2) The DC bias circuit is basically a voltage supply to the FET drain to source, to a resistor to ground. Setting the resistor value given the load line for the FET, will set the gate bias appropriately.

3) To account for possible RF performance changes, the linear model analysis did include the bias.

Test Plan

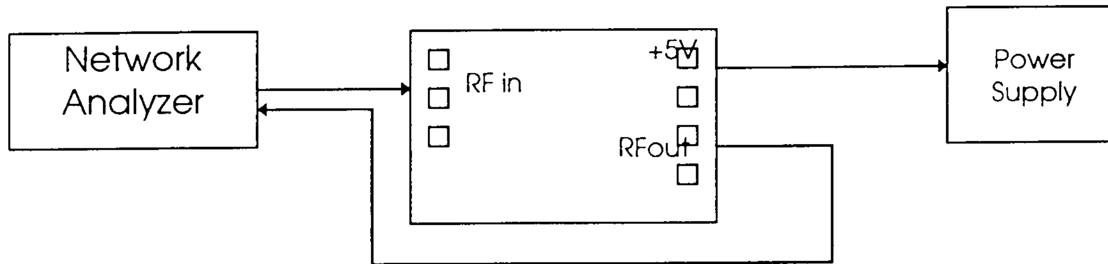
The Driver chip layout has RF input and output ports on opposite sides of the chip. These pads are ground - signal - ground type with 150um center to center spacing for implementation of RF probes. A single bias supply and associated ground return are the only DC inputs to the chip. There will be sufficient spacing between the RF and DC probes to allow their placement on the chip. The test equipment required for measuring the device is stated below:

For all measurements:

1. Wafer probe station with 2 RF probes and 1 DC probe. Ground Return will be attached to the baseplate the chip rests upon.
2. Power supply (5V at > 200mA)

For S-parameter measurements:

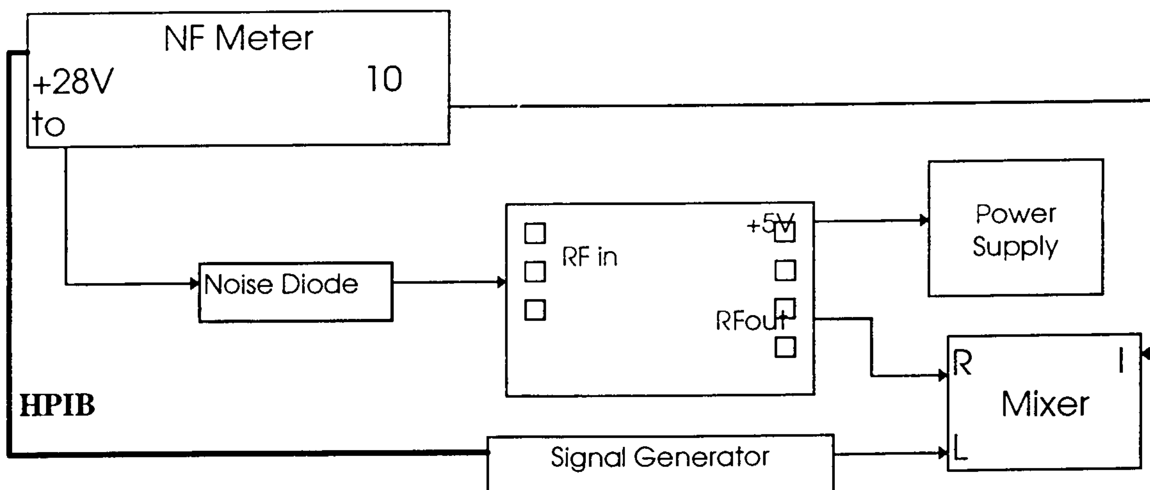
1. Scalar or network analyzer with L, C-Band capability.



Notes: Input power to driver amp should be < -5dBm (linear range)
Calibrate Network Analyzer with probes and cables in circuit

For Noise Figure measurement

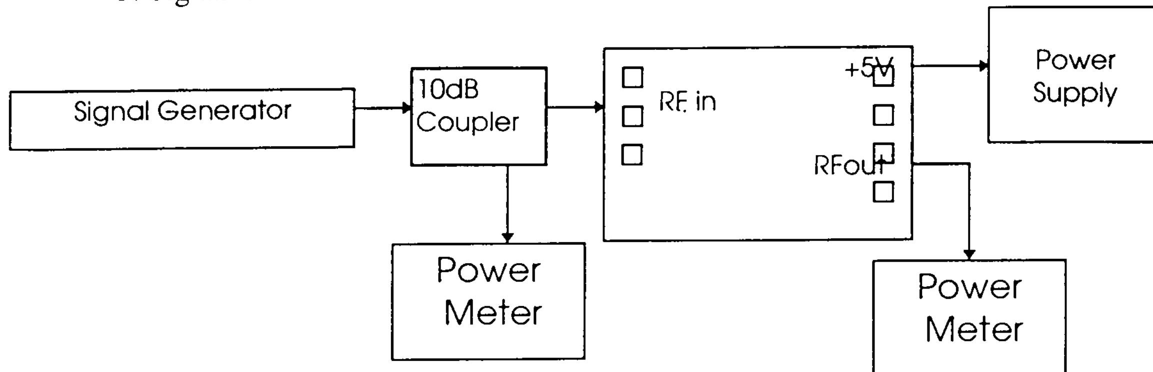
1. Noise Figure Test set up, with Noise Diode, mixer for down conversion and frequency generator.



Note: Set Signal Generator power out at about +10dBm for Mixer L-Port

For 1dB compression measurement

1. Power meters (2)
2. 10dB Coupler (for sampling the input power level)
3. Signal Generator



Note: Start the input power level at -5dBm (linear range for device) and increase the power in 1dB steps monitoring the output. Plot power in verses power out to determine P1dB.

Conclusion & Recommendations

The modeled performance shows a simulated response meeting the design specifications, except for the gain ripple at +/-0.8 verses +/-0.5dB. Stability was checked over a wide frequency band for the complete circuit, and for the individual FET's with their matching circuits, showing the unit to be unconditionally stable. The locations of the RF input and output are within the guidelines. Putting them on opposite sides is consistent with common practice, so the chip can be used in multiple applications.

Throughout the design process certain ideas were attempted. Some of them were used in the final design, and others were scrapped. The lessons learned from this design process were;

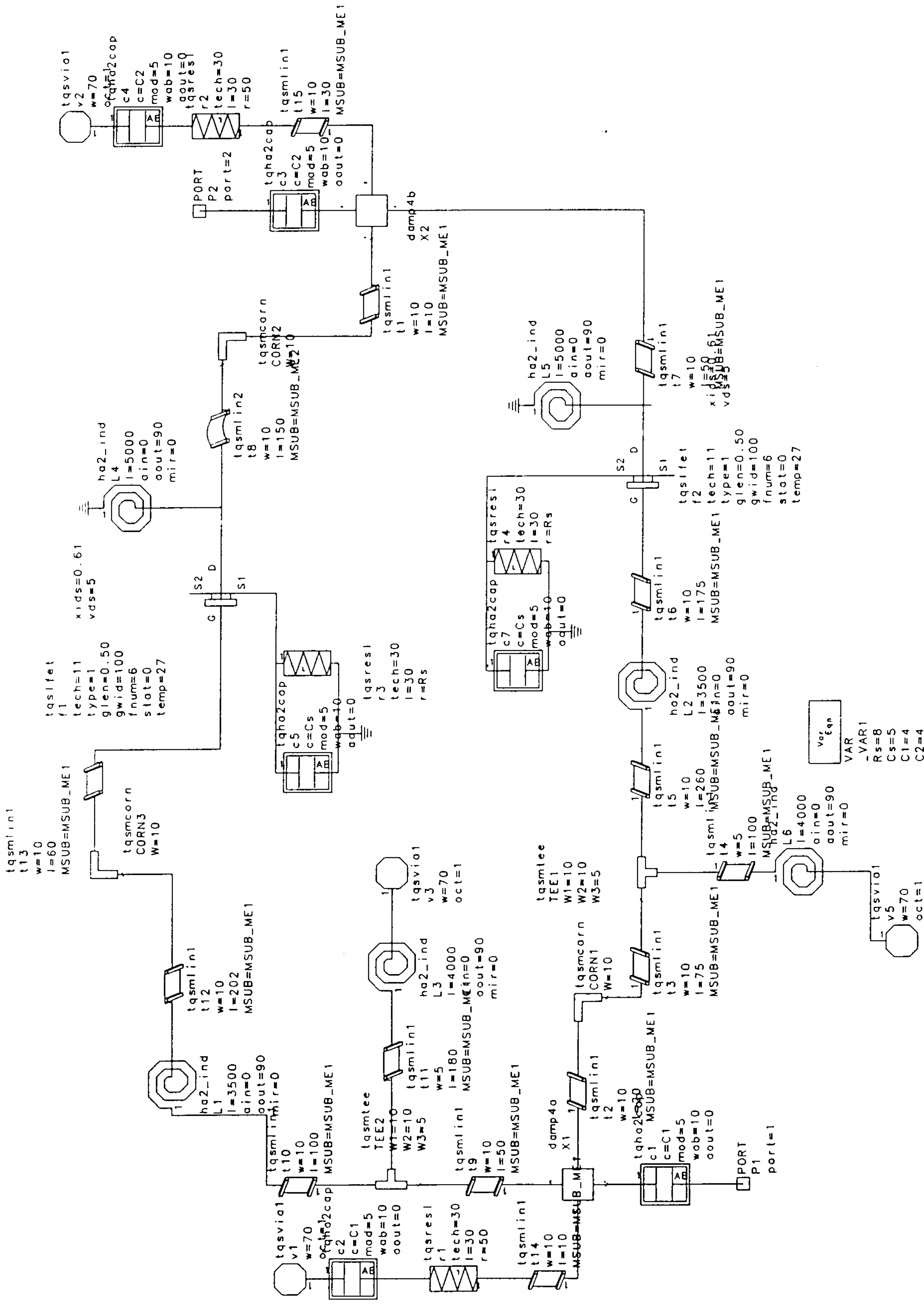
1) Perform sufficient research to determine a reasonable approach.

2) Verify during the design that the FET models used for linear and non-linear simulations are consistent.

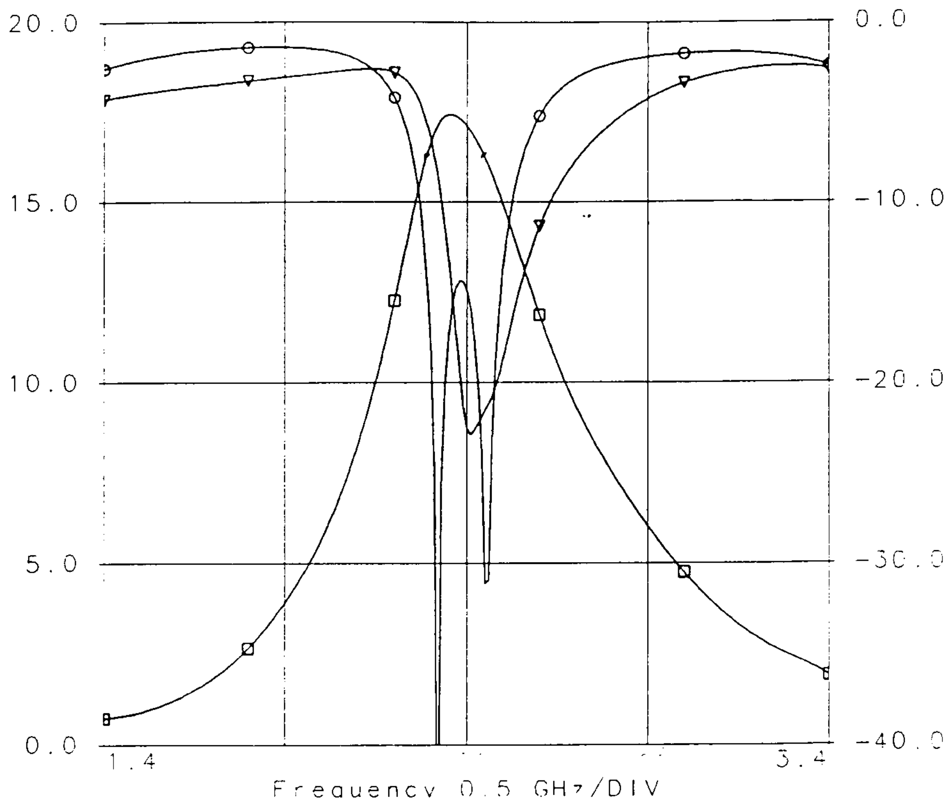
3) Do not attempt to completely optimize your design with ideal elements. Once the elements and value ranges are determined, switch over to physical elements.

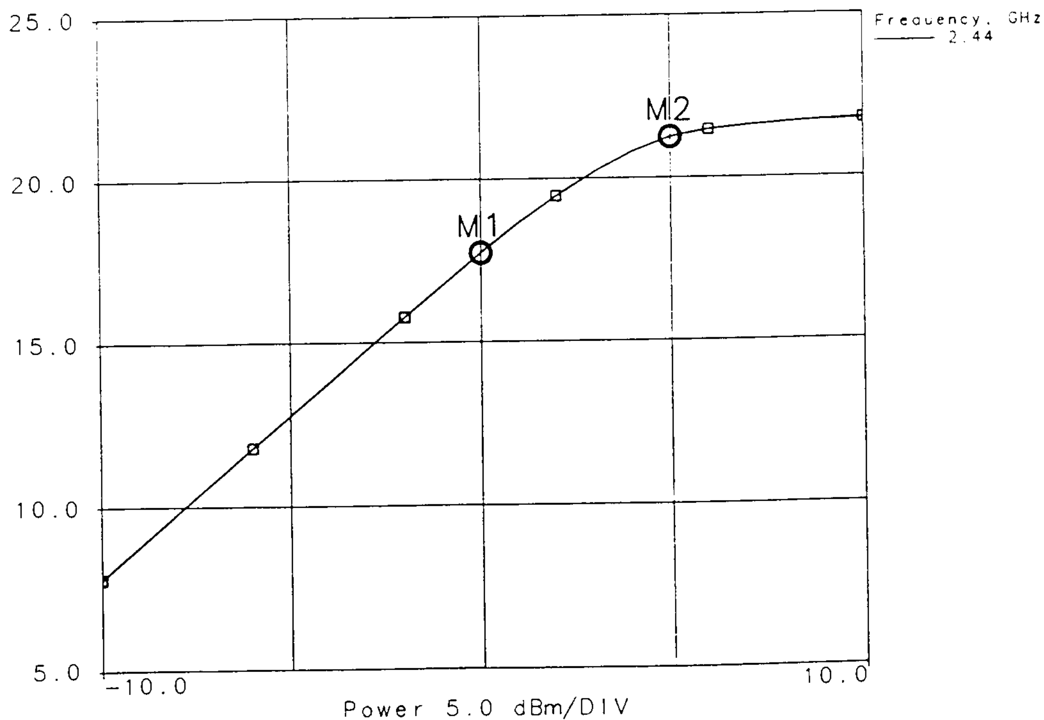
4) Continually check your design with bias attached, to see if the performance is greatly effected. If so, a) Set up a layout with just the bias, and see on the Smith Chart if the port that will connect to the circuit is at a very high impedance. b) Determine the impedance of the circuit at the place intended to connect the bias. This should be a low impedance point.

Pre-Layout Schematic



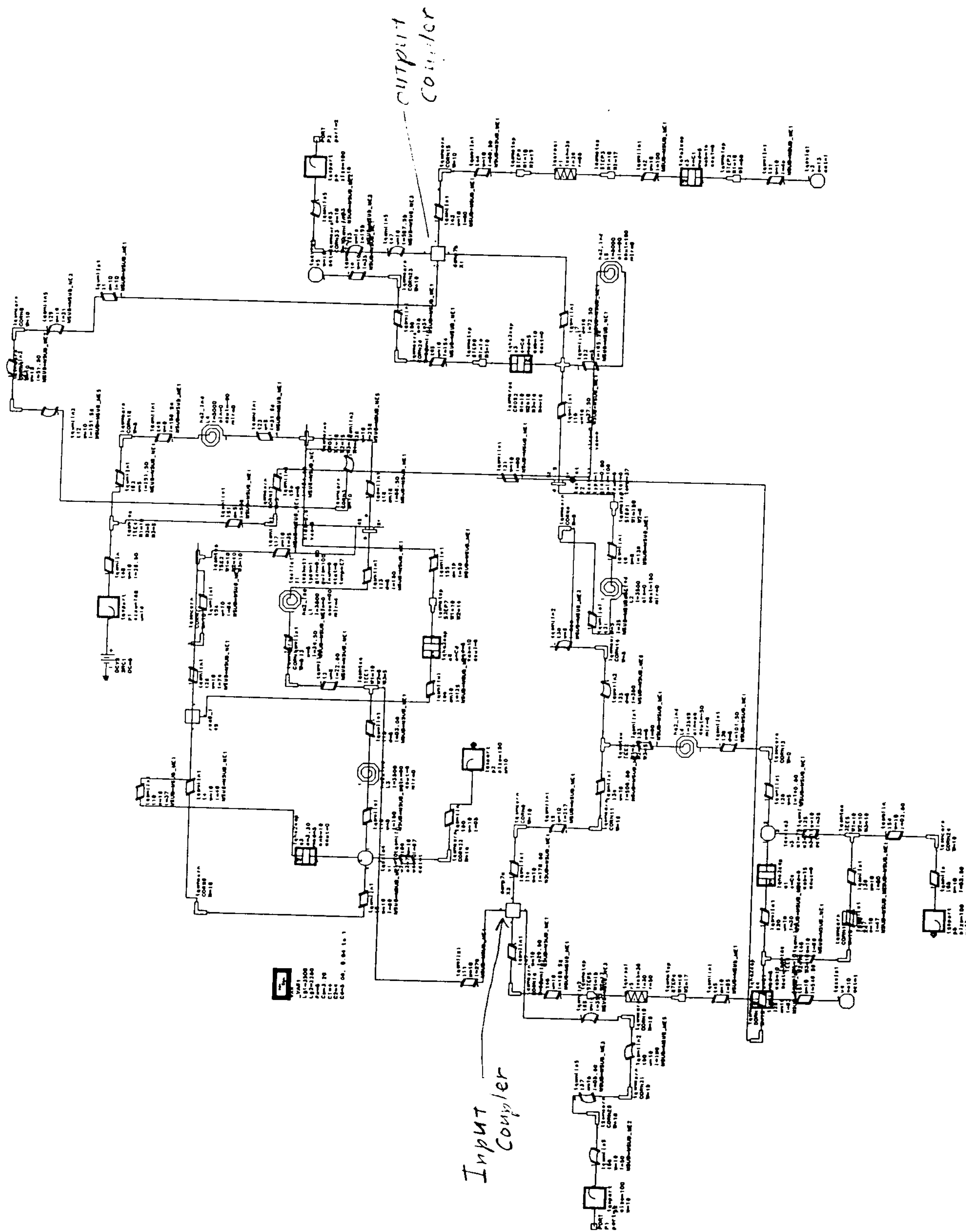
Pre - Layout S-parameter Performance





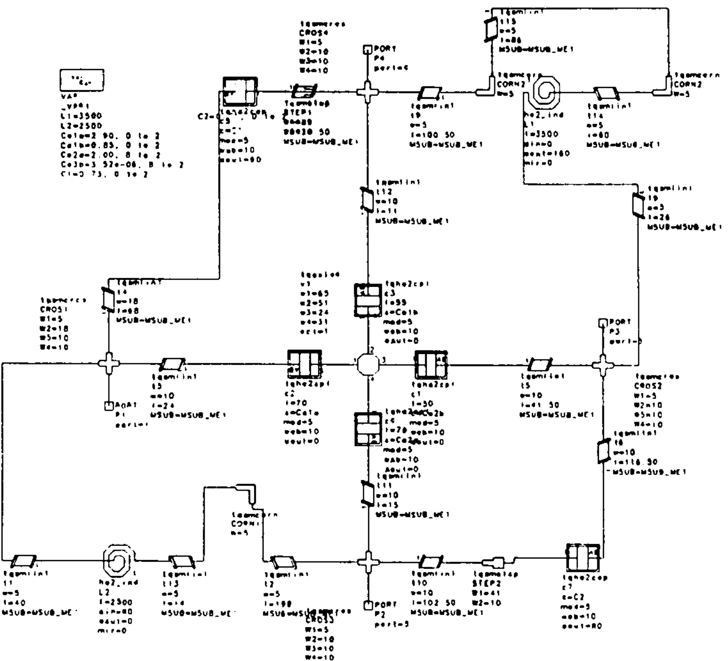
M1 Power=0.00000000 value=17.7264659
M2 Power=5.00000000 value=21.2605384

Post-Layout Schematic

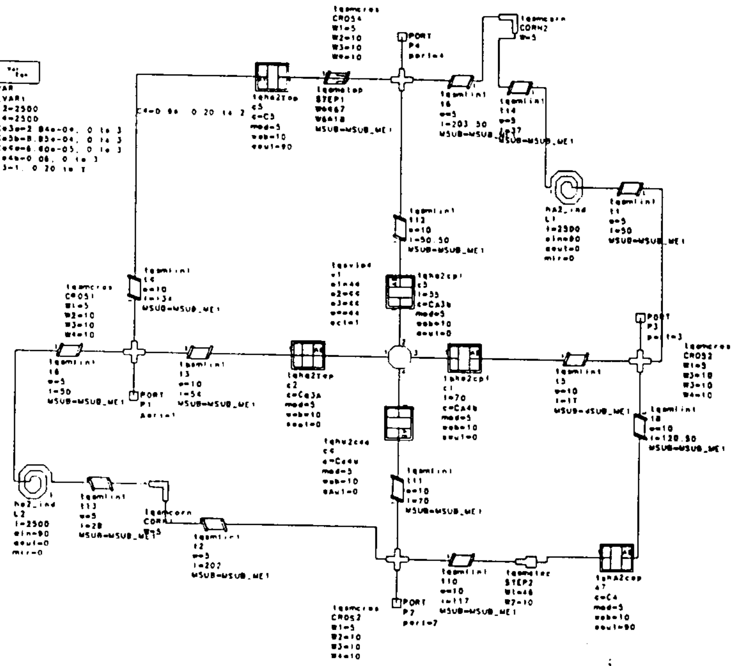


Post-Layout Coupler Schematics

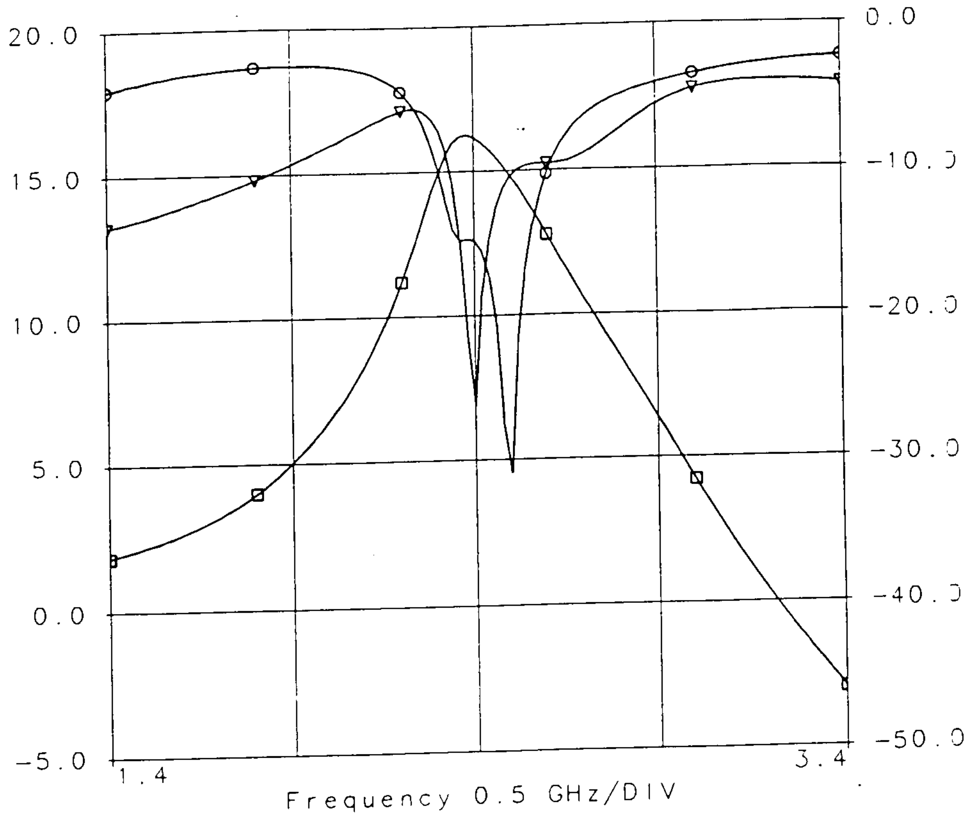
Input Coupler

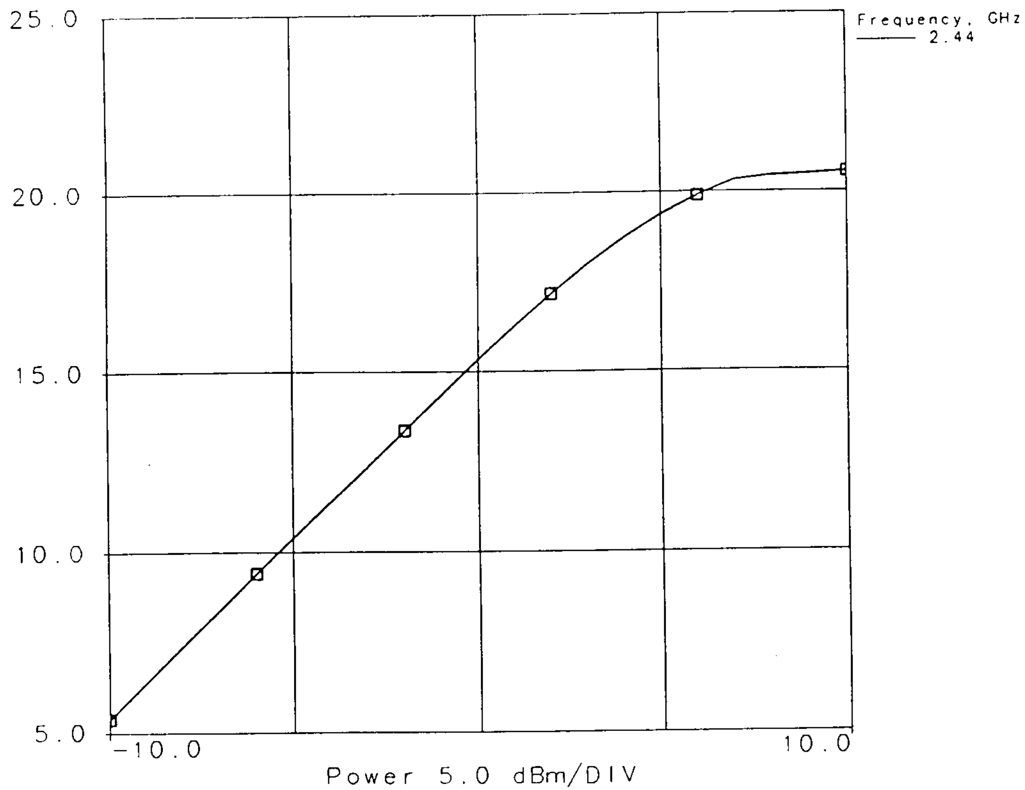


Output Coupler

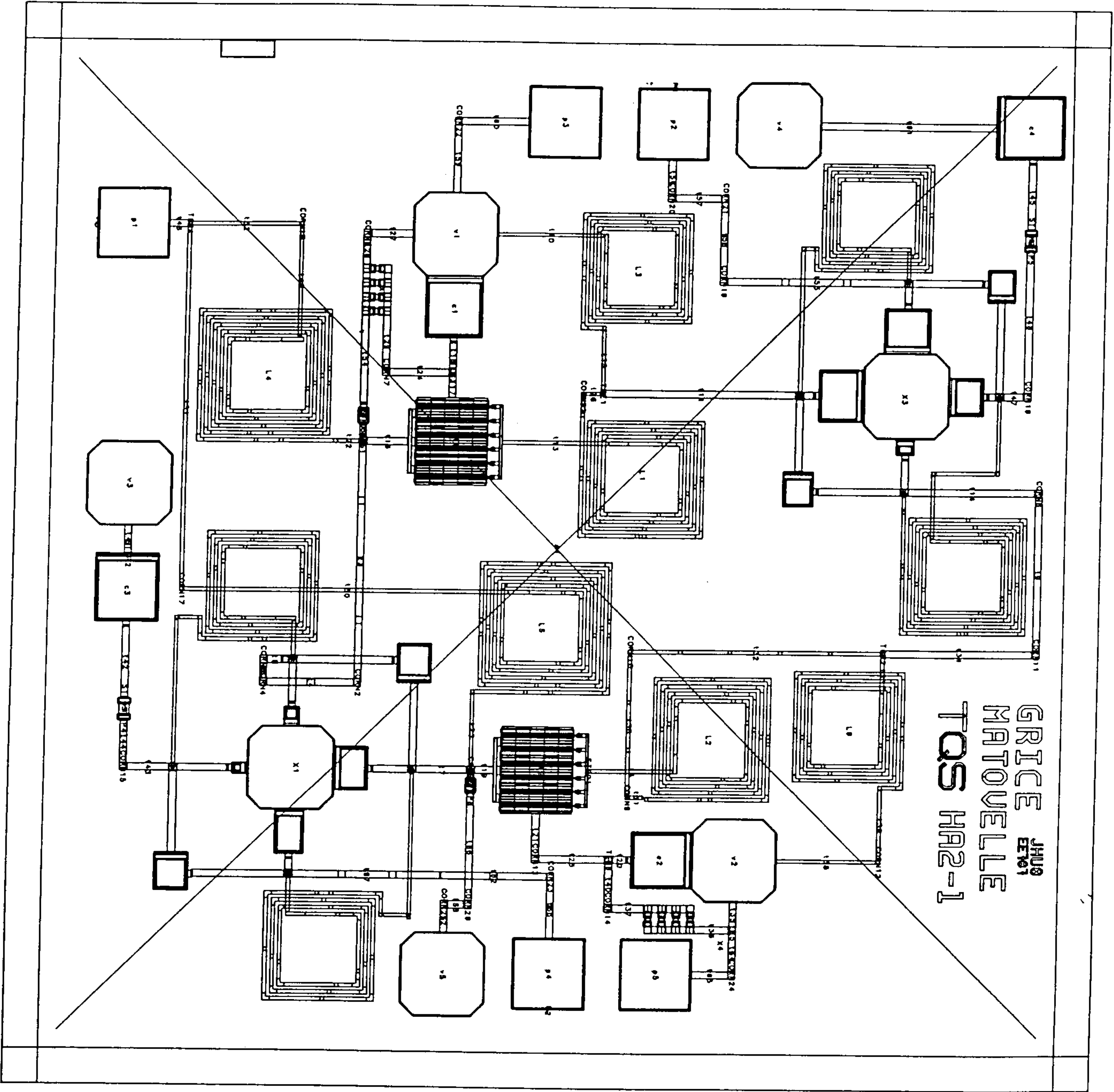


Post-Layout S-parameter linear analysis





Final Layout



S Band Power Amplifier
for
FM/CW, WLAN Applications

Prepared for:

Craig Moore and John Penn
525.787 MMIC Design
The Johns Hopkins University
Whiting School of Engineering

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1. Introduction

An S band power amplifier has been designed as part of a chip set for wireless local area network (WLAN) applications. Using Triquint Semiconductor's HA2 Process (0.5um gate length, 4mil thick GaAs), the design incorporates four 1mm MESFETs (2 pair parallel-connected) in a common source configuration. Additionally, the following building blocks are utilized in a balanced amplifier topology: power-dividing hybrid coupler (90 degree), input matching network (IMN) with bias, output matching network (OMN) with bias, and power-combining hybrid coupler (90 degree). Using HPEESof Libra 6.0 and Triquint's Smart Library (HA2 process), the power amplifier design was schematically captured, layed out (ANACHIP), and simulated at Johns Hopkins University Dorsey Center. Fabrication of the circuit at Triquint Semiconductor is intended following Layout Versus Schematic (LVS) and Design Rule Checker (DRC) analyses.

2. Specification

Table 1 below lists the proposed specifications for the S band power amplifier. The transducer gain (G_T) specified at the 1 dB power compression point (P_{1dB}) and the gain ripple refer to a nonlinear analysis; the transducer gain shall also be ascertained via a linear analysis (S parameters) in addition to the gain ripple (bandwidth) and input/output VSWR (return loss) measurements. It is convenient to note that 1.5:1 VSWR corresponds to approximately $\Gamma \approx -14dB$ and that $P_{1dB}=27dBm \approx 500mW$ rms. The following design goals were also proposed:

G_T @ P_{1dB}=13dB
P_{1dB}=30dBm
Power-Added Efficiency (PAE)=25%

A bandwidth greater than 83 MHz was also desirable, though no specific goal was proposed. Although the chip size is 60 mils x 60 mils, approximately 4 mils is allocated for street scribe; that is, the available chip area is only 56 mils x 56 mils.

Table 1: S Band Power Amplifier Specifications

Parameter Name	Min Value	Typ Value	Max Value	Units
Frequency (f)	2400		2483	MHz
Bandwidth (BW)	83			MHz
G_T @ P_{1dB}	10			dB
Gain ripple			1	dB, p-p
P_{1dB}	27			dBm
PAE (η) @ P_{1dB}	15			%
I/O VSWR			1.5:1	-
Supply Voltage, +/-	4.5	5	5.5	V
Chip Size (Area)			60 x 60	mil^2

3. Design Approach

The availability and viability of GaAs MESFETs for power amplification has rendered this device suitable in an attempt to achieve the performance associated with the proposed specifications. Upon careful consideration of the design goals for the S band power amplifier, the following has been deduced:

1. PAE specification is achievable in class A operation (<50%)
2. Maximum power dissipation has not been specified; however, thermal considerations and PAE specification demand that power consumption be kept at the required minimum
3. Input/Output return loss specification (VSWR ≤ 1.5:1) poses difficult design tradeoff (power out, VSWR)
4. Transconductance increases with device size; therefore, ample gain should be available to achieve transducer gain specification
5. Bandwidth (≈2%) and gain ripple specifications are achievable using lumped element reactive matching (such as 'L' networks)

Based upon these observations, it was determined that MESFET class A operation was appropriate, thereby providing the additional benefit of good linearity. The output power and power-added efficiency for the MESFET are given by

$$P_{OUT} = \frac{I_M V_M}{8}$$

$$\eta = \frac{P_{OUT} - P_{IN}}{P_{DC}}$$

$$P_{DC} = I_{DQ} V_{DSQ}$$

where I_M denotes the drain current swing, V_M denotes the drain voltage swing, I_{DQ} refers to the quiescent drain current, and V_{DSQ} refers to the quiescent drain-source voltage. Upon considering the I-V characteristics of the MESFET in class A operation, the required size and biasing for the MESFET was determined; total gate width of 4 mm, $V_{GS} \approx -0.6V$ ($I_{DQ} \approx 60\%$ of I_{DSS}) and, $V_{DSQ}=+5.0V$. At this bias point approximately 400mA of DC current needs to be supplied from $V_{DD}=+5V$, which amounts to $P_{DC} \approx 2$Watts; thus, for $V_{DSQ} \approx 5.0V$, it is not possible to realize 1 watt of output power ($\eta<50\%$ due to finite amplifier gain and lossy passive elements). Since the possibility of model degradation arises if a single MESFET of width greater than 1mm is used, it was decided that four 1mm MESFETs would be employed. The S parameters and associated stability circles for the cases of two and four paralleled MESFETs was investigated. As mentioned in the review of the specifications, the analysis of the four paralleled MESFETs configuration indicated that the output matching network design required a costly tradeoff between output power and output VSWR. Instead, two paralleled 1mm MESFETs in a balanced amplifier design was selected with the following justification:

1. Optimal power output match with good input/output VSWR achievable
2. Despite lossy lumped combining/dividing networks, sufficient gain available
3. Easier to impedance match two paralleled MESFETs than four paralleled MESFETs
4. Additional stability provided by hybrid combiner/divider

The system block diagram of the S band power amplifier appears in Figure 1. Perhaps the greatest challenge associated with on-chip combining/dividing networks is efficiently using the significant chip area required. It was thus concluded that careful layout would be imperative. Once the general topology of the S band power amplifier had been determined each block was subsequently designed and layed out. The building blocks were then integrated together in an iterative process that involved modifying layout in an effort to efficiently utilize chip area while resimulating

groups of blocks to ensure that good electrical performance was maintained. Due to the balanced nature of the design, it was critical that the circuit design exhibit excellent symmetry. A hierarchical approach to schematic capture and layout was implemented.

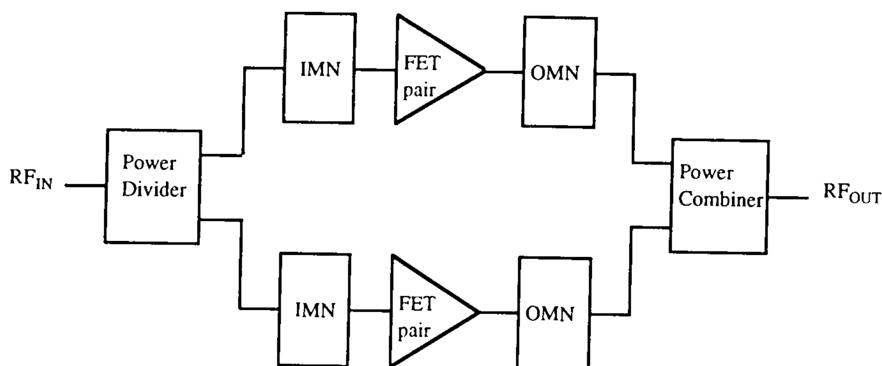


Figure 1: S Band Power Amplifier Block Diagram

4. Building Blocks

The top-level schematic as well as the schematic and layout for each building block appear in Appendix B. A general discussion of each building block follows.

4.1 Parallel-connected 1000um MESFETs

The MESFET (1000um total gate width) device parameters appear in Table 2. The MESFET used in the S band power amplifier design is a depletion mode device (n- depletion channel implant). The gate length, gate width, and number of gate fingers are user-defined parameters common to the linear TQLFET and nonlinear HA2FET (Triquint's Own Model) models contained in the Triquint Smart Library. The gate-drain and gate-source spacing are user-defined parameters of the TQLFET model. The listed S parameters refer to Z_O=50Ω system.

Table 2: 1000um MESFET Device Parameters

Parameter Name	Value	Units	Notes
Gate length (L)	0.5	um	
Finger gate width (w)	125	um	Total gate width=W
Number of gate fingers (n)	8	–	W=n*w
Gate-drn, Gate-src spacing	1	um	
S11 @ f=2.45GHz	0.83∠-111.8	V/√Ω	TQLFET model; V_{DS}=5V, I_D=60%I_{DSS}

S12 @ f=2.45GHz	$0.07\angle 28.6$	$V/\sqrt{\Omega}$	TQLFET model; V_{DS}=5V, I_D=60%I_{DSS}
S21 @ f=2.45GHz	$4.67\angle 108.1$	$V/\sqrt{\Omega}$	TQLFET model; V_{DS}=5V, I_D=60%I_{DSS}
S22 @ f=2.45GHz	$0.36\angle -72.7$	$V/\sqrt{\Omega}$	TQLFET model; V_{DS}=5V, I_D=60%I_{DSS}
I_{DSS}	180	mA	TQNFET model; V_{GS}=0V, V_{DS}=5V

The schematic diagram for the parallel connection of two 1000um MESFETs appears in Figure 2. It was decided as a result of a linear analysis using the geometrically-derived μ and μ' stability parameters (based only on device S parameters) for the parallel connection of two 1000um

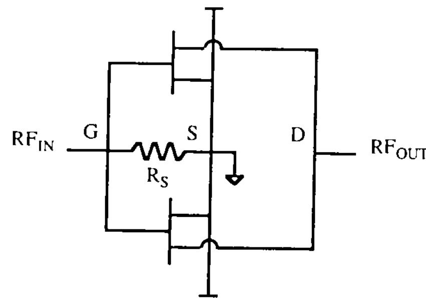


Figure 2: Paralleled 1000um MESFETs

MESFETs that resistive stabilization would be utilized. Specifically, a shunt gate resistor R_S was selected due to the fact that source plane stabilization is preferable for power amplifier design. Furthermore, due to the negligible DC gate current of a MESFET device, gate biasing can be accomplished using a simple resistor divider circuit. Although this simple biasing technique is supply and process dependent, it is easy to troubleshoot using breakable airbridge and can be designed to have a minimal effect on the input matching network.

As a first order approximation (assuming that two 1000um devices can be represented by a single 2000um device), the small-signal (linear) model device parameters can be determined by simply scaling the known model parameters (capacitances and resistances) associated with the standard 300um MESFET using identical bias conditions and identical gate-drain / gate-source spacing. Since the drain-source capacitance (C_{DS}) and drain-source resistance (R_{DS}) are critical in designing the initial output matching network these parameters appear in Table 3. Although V_{GS}=-0.75V corresponds to I_D=50%I_{DSS} (I_{DSQ}=60% I_{DSS} preferable for class A power amplification), the associated C_{DS} and R_{DS} are sufficient to determine an initial OMN.

Table 3: Scaleable MESFET Linear Model Device Parameters for OMN Design

Parameter Name	W=300um	W=2000um	Units	Notes
C_{DS}	70.34	468.93	fF	V_{DS}=5V, V_{GS}=-0.75
R_{DS}	410.85	61.63	Ω	V_{DS}=5V, V_{GS}=-0.75

4.2 Hybrid (90 degree) Combiner/Divider

Since the power amplifier is to operate at S band, distributed element couplers are not practical due to the chip area required. Thus, a method of combining/dividing, using a lumped element 90 degree hybrid, was necessary. Recalling the fact that two hybrids (one for dividing at the input and one for combining at the output) are required in the balanced amplifier design, the inductor count (regarding chip area, because MMIC inductors are generally much larger than capacitors) and electrical performance must be considered. Table 4 presents a comparison of ideal lumped element quadrature hybrid electrical performance (S parameter values in dB) for 2 percent bandwidth

Table 4: Lumped Element Quadrature Hybrid Comparison

Type of power combiner/divider	Inductors required	S_{21} $0.98f_0$	S_{21} $1.02f_0$	S_{31} $0.98f_0$	S_{31} $1.02f_0$	S_{23} $0.98f_0$	S_{23} $1.02f_0$
Narrow Branchline	4	-2.69	-3.41	-3.38	-2.68	-27.84	-27.27
Wilkinson + quarter-wave section	3	-3.01	-3.01	-3.01	-3.01	-35.08	-35.03
Standard Branchline	2	-3.05	-3.05	-3.01	-3.01	-25.99	-26.00

Ports: 1=Input, 2=Direct, 3=Coupled, 4=Isolated (Terminated in Z_0=50Ω)
centered at f_0=2.45GHz. Realizing the standard branchline hybrid requires 4 inductors, which was deemed excessive, considering the fact that a total of 12 inductors would be required to complete the power amplifier design (since at least 1 inductor is required to reactively match each IMN/OMN). The narrow branchline proved to be bandlimited, such that the bandpass characteristic is not symmetrical about f_0. The lumped element hybrid combiner/divider consisting of a Wilkinson power combiner/divider with single-sided quarterwave section, which appears in Figure 3, was selected based on its electrical performance and inductor count. It was concluded that only 3 inductors would be required to realize each hybrid. Since phase delay is extremely critical in a balanced amplifier design, the hybrid was tuned for exactly 90 degree phase shift. It was expected that the lumped element realization would present 1dB of loss.

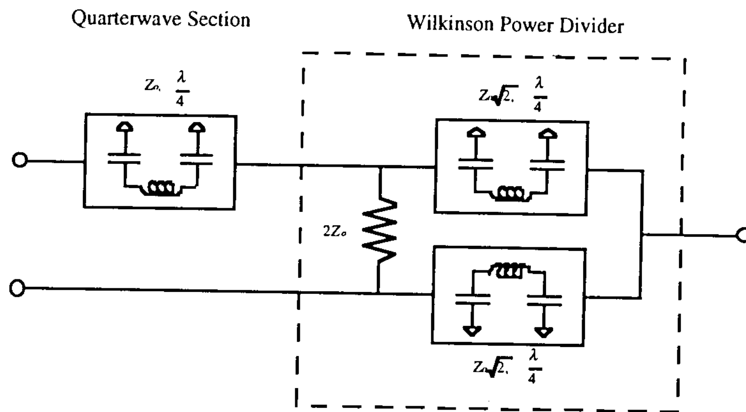


Figure 3: Hybrid Combiner/Divider

4.3 Output Matching Network (OMN) With Bias

Upon viewing the output reflection coefficient on the Smith chart, it was concluded that a shunt inductor followed by an impedance transformer would provide the optimal power match as illustrated in Figure 5; that is, the shunt inductor would be used to resonate C_{DS} while the impedance transformer is used to transform Z_o=50Ω to the optimal power matching impedance given by the dynamic load line (R_{DLL}≈20Ω). The drain inductor (approximately lossless passive element) facilitates quiescent drain voltage biasing such that $V_{DSQ} \approx V_{DD}$ while the quiescent drain current (I_{DQ})is established by the gate bias (V_{GS}).

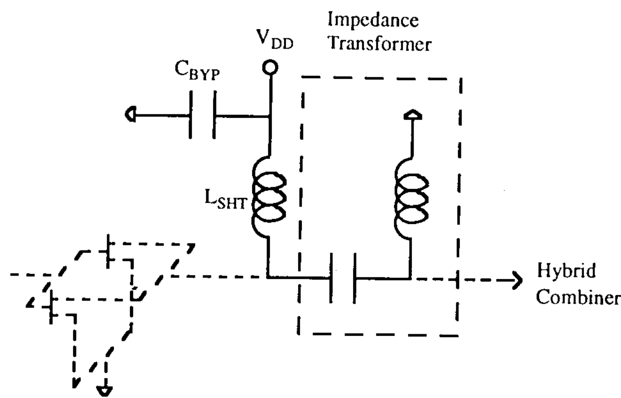


Figure 4: Output Matching Network

4.4 Input Matching Network (IMN) With Bias

Since the bandwidth requirement can be satisfied using lumped element reactive matching, a simple 'L' network consisting of a shunt inductor and series capacitor was selected for the input matching network, which appears in Figure 5. The effective series resistance (R_B) used for biasing is effectively shorted out by the bypass capacitor C_{BYP} such that R_B does not significantly effect the stability of the paralleled FETs or the input matching network. The gate bias is established as

$$V_{GS} = \frac{R_S || R_{SHT}}{R_S || R_{SHT} + R_{SER}} V_{GG}$$

$$R_{SHT} = R_{1A} + R_{1B} || R_{1AB} \approx R_{1A}$$

$$R_{SER} = R_{2A} + R_{2B} || R_{2AB} \approx R_{2A}$$

whereby R_S is the shunt source plane stabilization resistor, R_{SHT} is the shunt bias resistance, R_{SER} is the series bias resistance, R_{1AB} and R_{2AB} are negligible air-bridge resistances, and $R_{1A}/R_{2A}/R_{1B}/R_{2B}$ are nichrome resistors. The air-bridges can be broken for gate bias adjustment (troubleshooting) such that $R_{SHT}=R_{1A}+R_{1B}$ and $R_{SER}=R_{2A}+R_{2B}$.

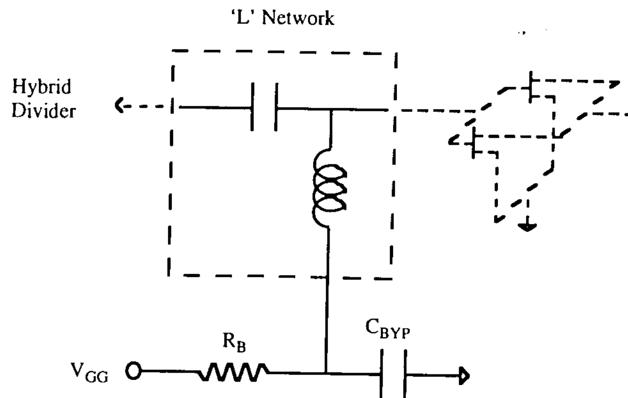


Figure 5: Input Matching Network

4.5 Layout

As already mentioned careful layout was imperative for the power amplifier design. The following considerations led to the floor plan that appears in Figure 6:

1. Available chip area
2. Power dissipation/management
3. Symmetry
4. Chip combining arrays (power amplifier modules)
5. Testability; RF I/O (gnd-signal-gnd) on opposite sides

The two source nodes of all four MESFETs were connected directly to vias (some shared) in an attempt to minimize source inductance and facilitate heat sinking. The placement of the RF (input and output) and DC (V_{GG} and V_{DD}) bond pads is conducive to chip combining arrays and on-wafer measurement. The design (layout) is symmetrical such that both IMNs are identical, both OMNs are identical, both paralleled FETs are identical, and both couplers (input and output) are identical. This minimizes phase mismatch and provides good output VSWR.

The following layout techniques were exercised in an effort to fit the power amplifier design on the ANACHIP: in the coupler layout, the 100Ω resistance between the two input/output ports of the Wilkinson power divider/combiner was realized by routing metal2 (air-bridge) over two paralleled 200Ω nichrome resistors (ρ_{NiCr}=50Ω/); in the coupler layout, unfortunately non-square metal-insulator-metal (MIM) capacitors were used in the Wilkinson power divider/combiner due to chip area constraints; in the output matching network layout, custom (not part of the Triquint Smart Library) shunt drain inductors were designed, using landed air-bridge (LAB), to handle the quiescent drain current density required.

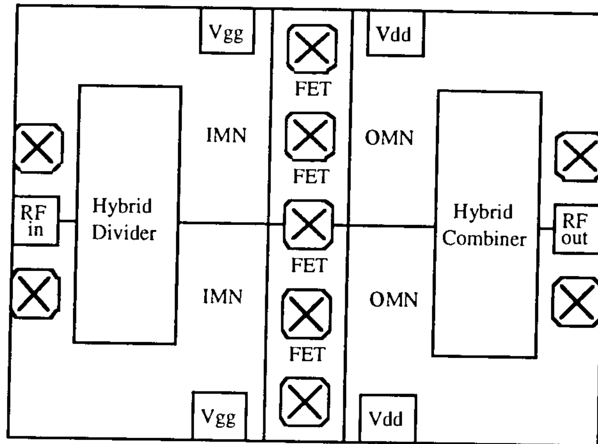


Figure 6: S Band Power Amplifier Floor Plan

5. Test Plan

The wafer probe test strategy is depicted in Figure 7. The HP4142B Modular DC Source/Monitor contains one HP41420A Source/Monitor Unit (40µV-200V/20fA-1A) for V_{DD} supply and one HP41421B Source/Monitor Unit (40µV-100V/20fA-100mA) for V_{GG} supply. Small signal (S parameter) measurements are made using the HP8510C Network Analyzer and associated HP8517B Test Set. Large signal measurements are made using the HP83752A Synthesized Sweeper and HP437B Power Meter.

Since the n channel MESFET is a depletion mode device, the power supply sequence is critical in order to avoid burnout. The following sequence shall be exercised:

1. The negative supply V_{GG} shall be powered on first such that $V_{GG}=2(V_{GG})_{nom}$
2. The positive supply V_{DD} shall be powered on next to its nominal value
3. The negative supply V_{GG} shall be adjusted to its nominal value

Due to the significant chip power consumption, the S band power amplifier will be powered on for minimal periods of time to perform accurate measurements. Automated measurement using the Hewlett Packard Interface Bus (HPIB) will assist in this effort. Additionally, pulsed measurement techniques are being considered.

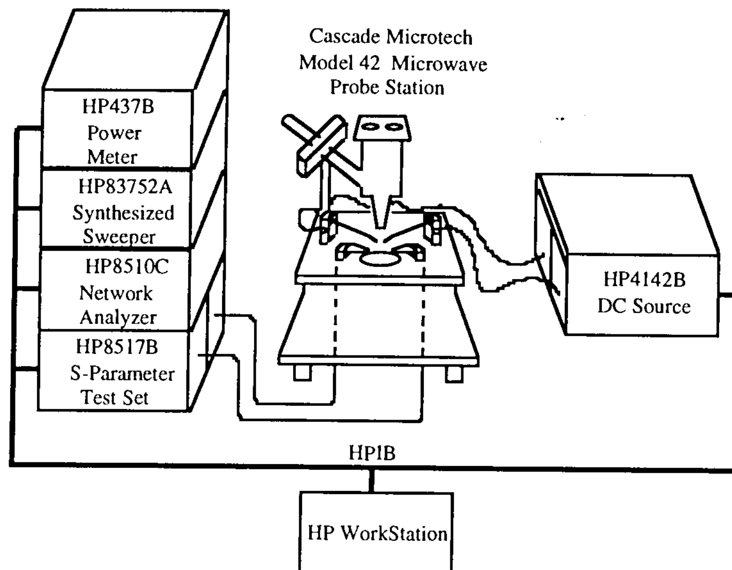


Figure 7: Wafer Probe Test Setup

6. Results

Simulation of the S Band Power Amplifier was performed using HPEESof's Libra version 6.0 and the Triquint HA2 Smart Library. The simulation plots appear in Appendix 8.1. Wafer-probe test data was acquired as shown in Figure 7. The small-signal and large-signal results are summarized in Tables 4a and 4b, respectively.

Table 4a: S Band Power Amplifier Performance (Small Signal)

Parameter Name	Simulated Value	Measured Value	Simulated Value	Measured Value	Units	Notes
f_o	2.45		2.45		GHz	
BW	100		400		MHz	
T_{typ}	27		27		°C	
Drn-Src Voltage	+ 4.5/5.5		+ 4.5/5.5		V	$V_{DS} \approx V_{DD}$
Drain Current (I_D)	50/70		50/70		% I_{DSS}	
G_{Tmin}	11.52		10.57		dB	
$Ripple_{max}$	0.20		1.37		dB	G_{Tmax}-G_{Tmin}
IRL_{min}	14.80		14.74		dB	
ORL_{min}	13.61		11.32		dB	
μ_{min}	1		1		–	

Table 4b: S Band Power Amplifier Performance (Large Signal)

Parameter Name	Simulated	Measured	Simulated	Measured	Units	Notes

	Value	Value	Value	Value		
f_o	2.45		2.45		GHz	
BW	100		400		MHz	
$(G_T \text{ @ } P_{1dB})_{min}$	10.91				dB	
$Ripple_{max}$	0.17				dB, p-p	
$(P_{1dB})_{min}$	25.94				dBm	
$(PAE \text{ @ } P_{1dB})_{min}$	13.06				%	
Supply Voltage						
V_{GG}	- 4.5/5.5		- 4.5/5.5		V	
V_{DD}	+ 4.5/5.5		+ 4.5/5.5		V	
T_{typ}	27		27		°C	

Figures 8a and 8b illustrate the simulated power amplifier performance for nominal supply voltages V_{DD}=+5V and V_{GG}=-5V while Figures 8c and 8d illustrate the simulated power amplifier performance for nominal supply voltages V_{DD}=+6.5V and V_{GG}=-5V.

As can be deduced from Table 4a above, the simulated linear performance meets nearly all of the proposed linear specifications (ORL=13.61dB is equivalent to 1.53:1 output VSWR which is slightly greater than the proposed 1.5:1 value). Additionally, the linear simulation results indicate unconditional stability since $\mu_{min}>1$. Referring to Table 4b, the simulated nonlinear performance does not meet the P_{1dB} and PAE @ P_{1dB} proposed specifications. This is because the V_{DD}=+4.5V case does not permit enough drain-source voltage swing under class A operation. However, for $+5.0V \leq V_{DD} \leq +5.5V$, the proposed nonlinear specifications are met. Furthermore, it is shown in Tables 4a and 4b that a respectable linear and nonlinear performance can be achieved over a much wider bandwidth.

The following summary describes supply voltage dependency on the linear and nonlinear simulation results: the input return loss (Input VSWR) varies little with V_{GG} variation but varies significantly with V_{DD} variation; the output return loss (Output VSWR) varies significantly with supply voltage variations; the transducer gain (G_T) does not vary much with supply voltage variations; the 1dB output power compression (P_{1dB}) varies little with V_{GG} variation but varies significantly with V_{DD} variation; the power-added efficiency (PAE) varies significantly with supply voltage variations. Unfortunately, the S band power amplifier design could not be simulated over temperature due to the unavailability of temperature model data.

It should be noted that a +/-15% change in I_D corresponds to a change in V_{GS} of approximately +/-0.1V.

Figure 8a: S Band Power Amplifier Nonlinear Simulation Results (Vdd=+5V, Vgg=-5V)

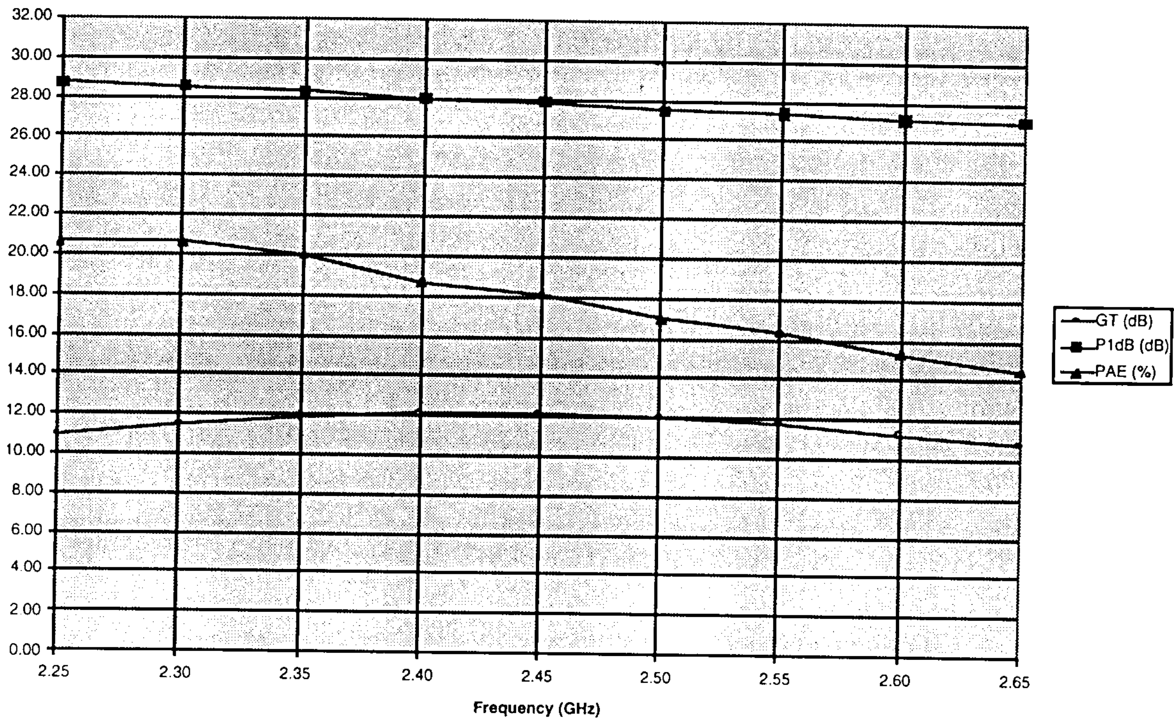


Figure 8b: S Band Power Amplifier Linear Simulation Results (Vds=+5.0V, Id=0.6Idss)

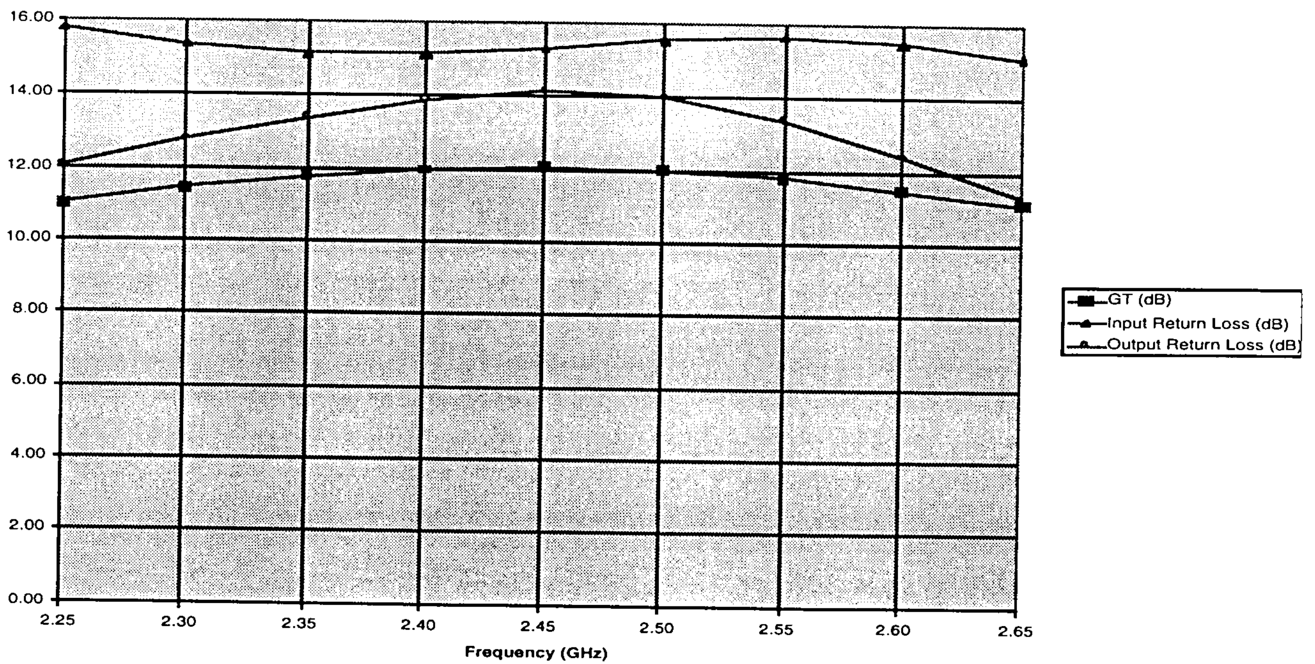


Figure 8c: S Band Power Amplifier Nonlinear Simulation Results (Vdd=+6.5V, Vgg=-5V)

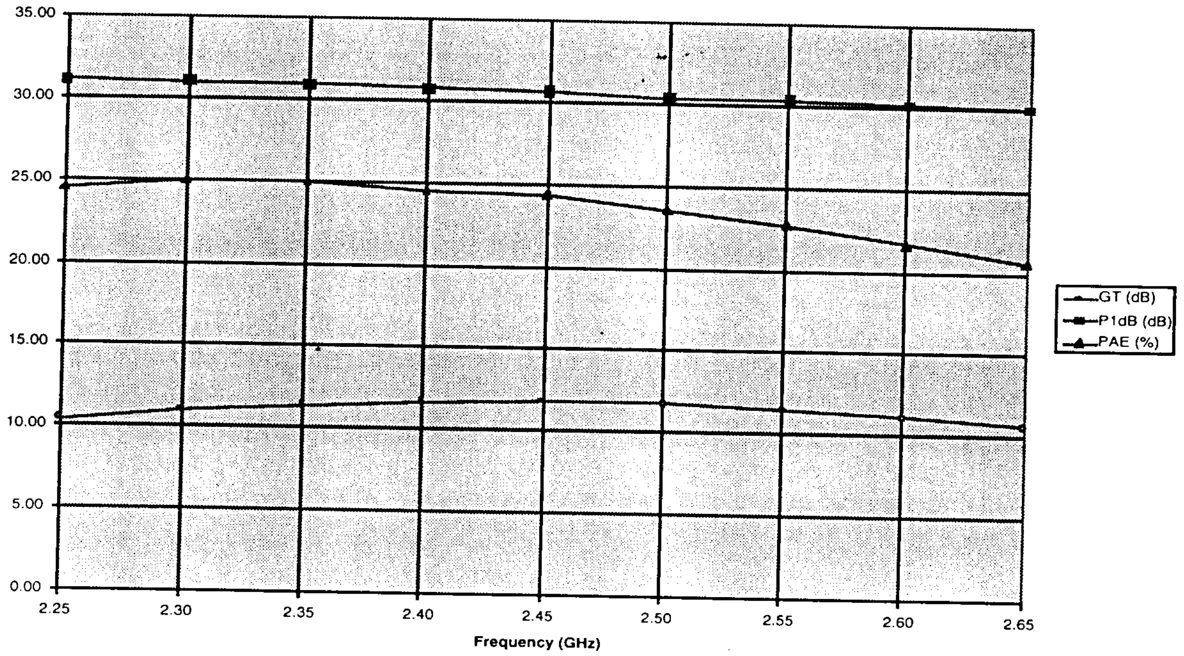
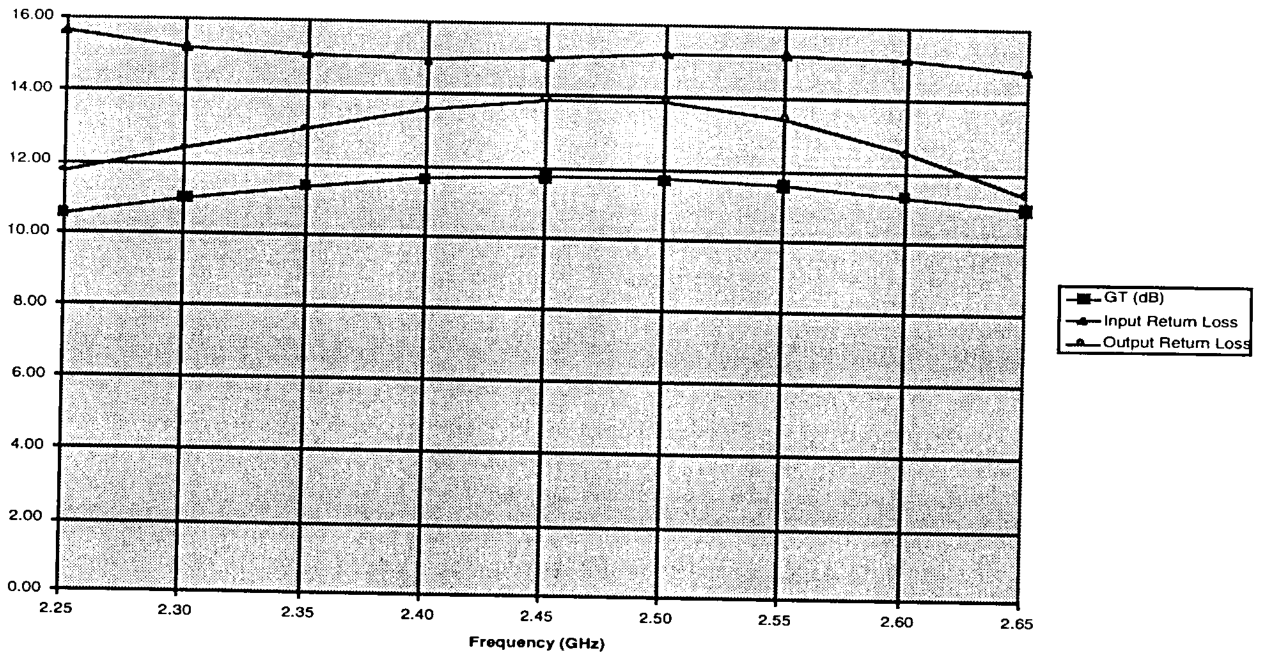


Figure 8d: S Band Power Amplifier Linear Simulation Results (Vds=+6.5V, Id=0.6Idss)



7. Conclusion

-Performance summary
-Observations
-over an octave bandwidth
-Application (what does additional bandwidth buy?)
-Vary drain voltage (how about 3.3V)
-Over temperature! SMALL SIZE

8. Appendix

8.1 References

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8.2 Schematic, Simulation, and Layout Plots

All of the following schematic, simulation, and layout data was acquired using HPEESof Libra v. 6.0 running on HP Workstations at The Johns Hopkins University Dorsey Center.