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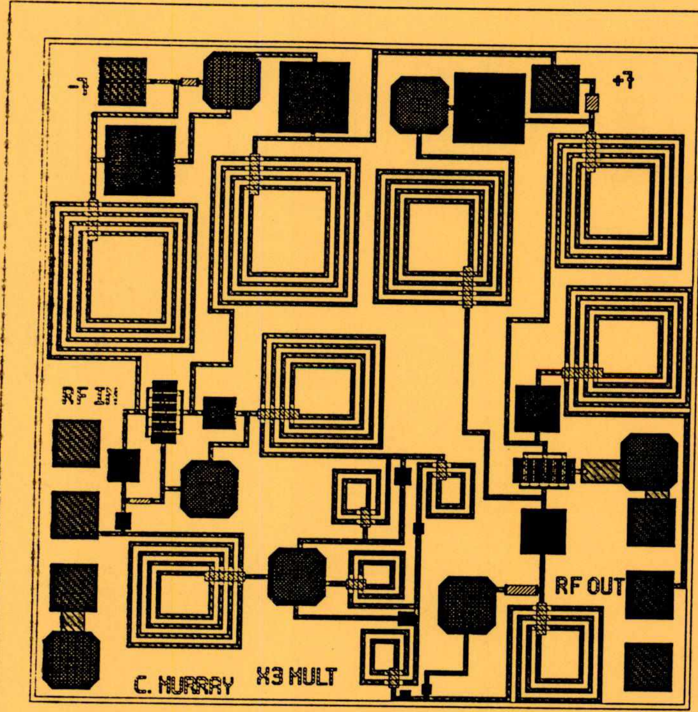
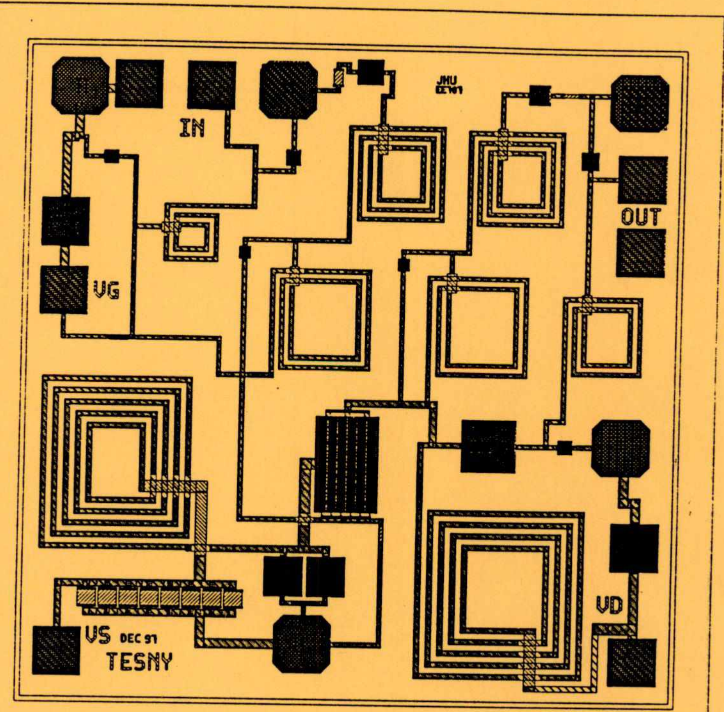
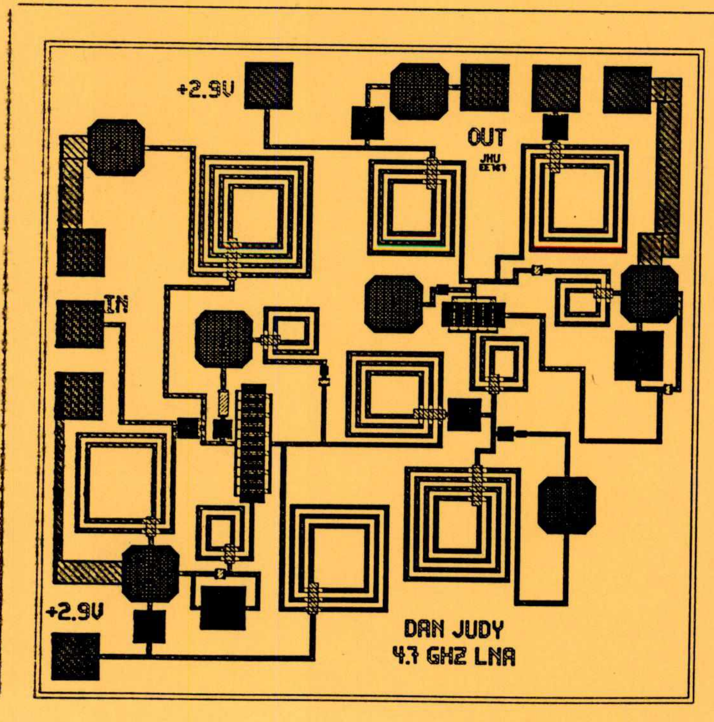
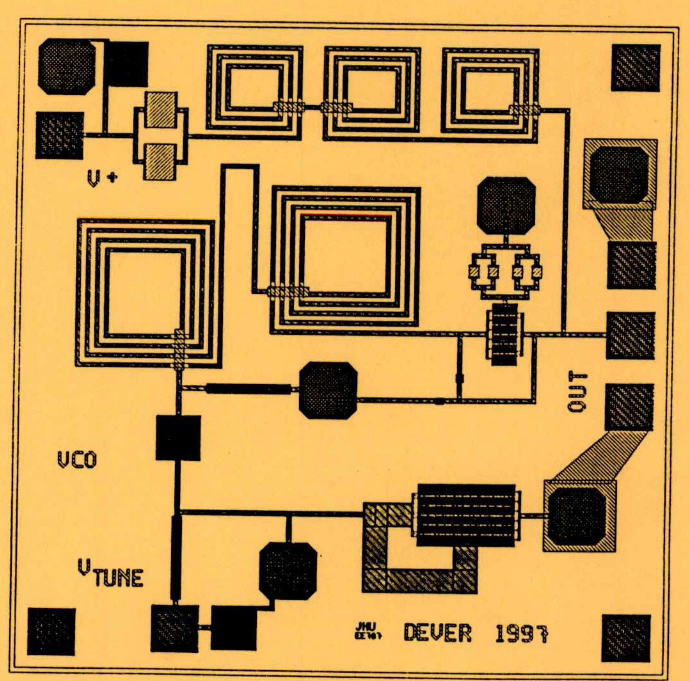
MMIC Design
JHU EE787
Fall 1997 Student Projects

Tripler -- C. Murray
Power Amplifier -- N. Tesny
Low Noise Amplifier -- D. Judy
Voltage Controlled Oscillator -- P. Dever
Distributed Amplifier (MACOM) -- J. Larner









Dan Judy
MMIC Design
Final Report

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1.

1. Introduction

My original design was a Ka band low noise amplifier (LNA). The design was to be realized using the MA/COM LH5 GaAs process. The process used 0.18 mm T-gate pHEMT transistors designed for ultra low noise and millimeter wave MMICs. The design goals called for a two or three stage amplifier with simultaneous noise and power match at the input achieved with P-HEMT sizing, source inductor feedback, and design of the interstage network. Unfortunately, the foundry where my design was to be fabricated closed about halfway through the design cycle. I was given the choice to finish the design on paper and write the report or to redesign the amplifier at a lower frequency using the TriQuint TQTRx process and get the chip fabricated for testing. I chose to redesign using the TriQuint process, so the final LNA design is not as polished as it would have been if I had the benefit of the full design cycle.

With all this in mind the design goals are as follows:

FREQUENCY:	4.635 to 4.685 GHz
BANDWIDTH:	>50 MHz
GAIN:	13 dB (2 stages)
GAIN RIPPLE:	±2 dB, ±0.5 dB goal
GAIN SLOPE:	±0.01 dB/MHz
NOISE FIGURE:	<3 dB <2 dB goal
INPUT IP3:	> -15 dBm
RETURN LOSS, I/O:	>10 dB
BIAS:	Single drain and gate pads
SIZE:	fit on anachip

2. Design

Preliminary design simulations indicated that I would get 4-7 dB gain for the input low noise stage. This then dictated that I would need a high gain (simultaneous conjugate match) stage for the output in order to realize the design goal of 13 dB gain. The following sections outline the design cycle for each of these stages.

2.1. Stability (Low Noise Stage)

I presented a preliminary design at the layout design review in class. The preliminary design had a 50x12 DFET biased at 2.5 volts and 10 mA for the input stage and a 50x6 DFET biased at 35 mA for the output stage. The low noise stage had an in band gain of 8 dB and the high gain stage had 13 dB gain and a cascade gain of 20 dB. When I presented this design in class I was told "that's going to sing" meaning the gain was to high to be stable. Taking this criticism in the spirit it was intended I decided to stabilize the FET "DC to light" before I attempted any redesign.

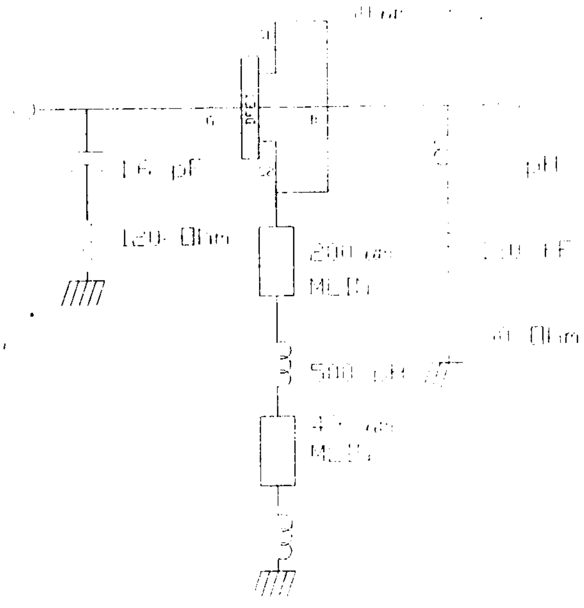


Figure 1 Schematic of the stabilization circuitry for the low noise stage.

The problem with stabilizing "DC to light" is that it will lower the expected gain of the circuit, so the trick is to stabilize the circuit out of band without affecting the in-band performance. I tried to do this by adding a series resonant circuit (Figure 1) to the drain circuit of the FET to stabilize the circuit above band and by adding a capacitor and resistor in the gate circuit that controlled the below band stability. By setting the resonant frequency of the drain circuit to 20 GHz and tuning the resistor values while observing the geometrically derived stability parameter (MU1) I was able to eliminate above band instabilities. By tuning both the resistance and capacitance of the gate circuit I was able to control the below band instabilities. Figure 2 shows the geometrically derived stability parameter for the low noise stage, notice that the FET is stable throughout the frequency range tested.

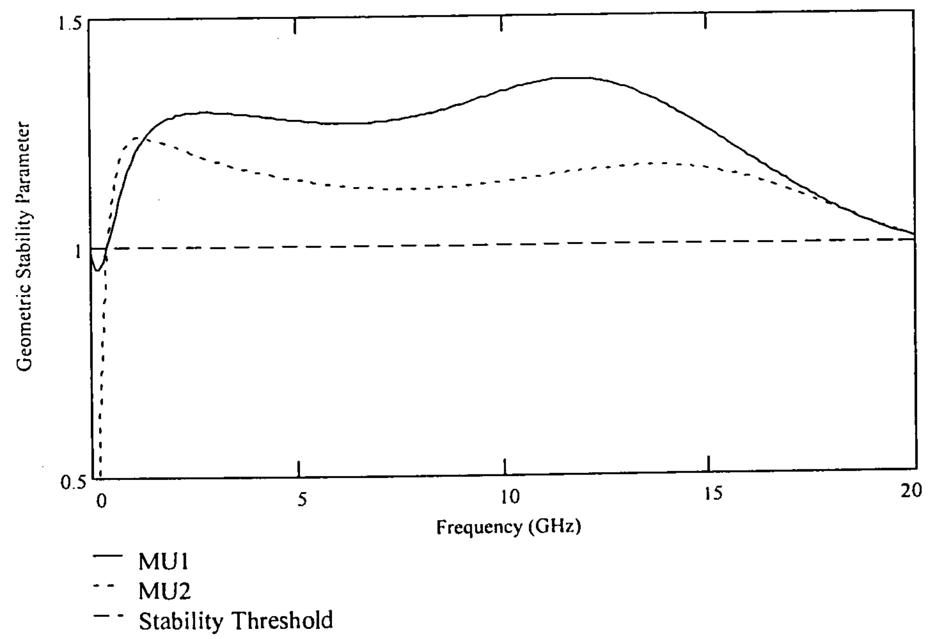


Figure 2 Geometrically derived stability parameter for the input low noise stage.

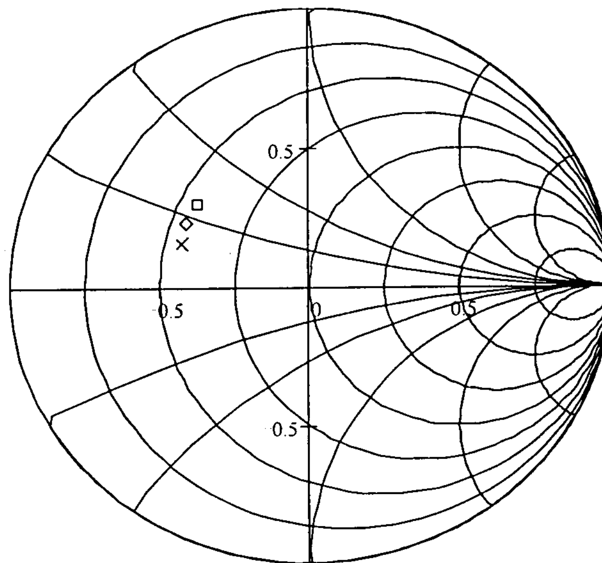
2.2. *Input Match (Low Noise Stage)*

During the preliminary design process, I designed the matching network using a simple two element network, then I added a bias tee after the matching network design was complete. I quickly realized that the TriQuint process did not have big enough stock inductors to completely isolate the input/output matching circuits from the bias power supply. I then decided that I would be sure to include an inductor to ground in all my matching networks for the redesign, so that all loading due to the power supply and bias tee would be accounted for in the design of the matching network.

The first order of business was to adjust the DFET size and source inductance to achieve a simultaneous power and noise match at the input of the low noise stage. Because of the abbreviated design cycle I only tried a couple of FET sizes. For the small size FET I used the DFET300.S2P (50x6 mm DFET biased at 2.5 volts and 10 mA) linear file, and for the large FET I simulated a 50x12 mm DFET biased at 10 mA by paralleling up two DFET300.S2P files in the schematic. I then used the LIBRA optimizer to adjust the source inductance to minimize the distance between minimum noise match point (GMN) and the simultaneous input match point (GM1), that is

$$|GMN - GM1|$$

Figure 3 shows the result of the optimization for the large (50x12) FET, which had the minimum distance between the points, the square is the input simultaneous match point and the X is the minimum noise match.



— Smith Chart
□□□ GM1
××× GMN
◇◇◇ S22 imn

Figure 3 Optimized input simultaneous conjugate match (square) and minimum noise match (x) point for the 50x12 mm DFET as well as the optimized input matching network S22 (diamond).

The next order of business was to design the actual input matching network. First I set up a input matching network using two reactive elements that I thought would take me to the desired input match through the shortest path. I then used the optimizer in LIBRA to minimize two parameters. The first of these parameters was the distance between S22 of the IMN and GMN, and the second was the distance between S22 and GM1, that is

$$|S_{2,2} - GMN|$$

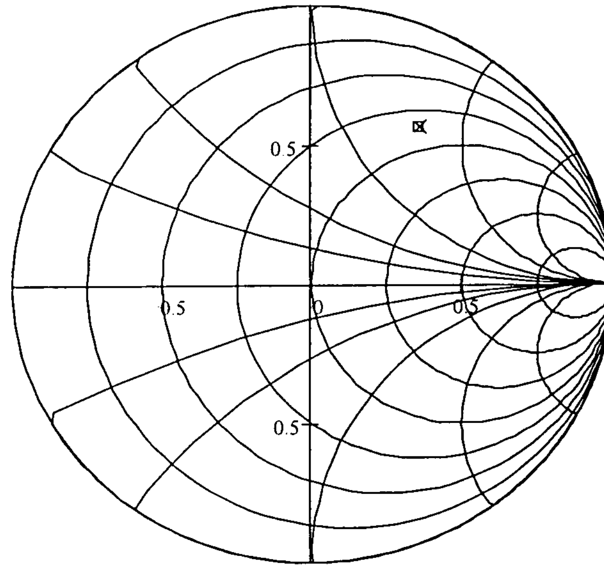
and,

$$|S_{2,2} - GM1|$$

Figure 3 shows the result of the optimization, where the diamond is the resultant S22 of the IMN.

2.3. Output Match (Low Noise Stage)

I designed the output matching network (OMN) by looking at the combination of the IMN and FET S22 and matching S11 of the OMN to the conjugate of S22. Figure 4 shows the conjugate of S22 of the FET, IMN combination (square) and the resultant S11 of the OMN (X).



— Smith Chart
□□□ Conjugate S22 (FET)
××× S11 OMN

Figure 4 Ouput matching of the low noise stage. The conjugate of S22 of the IMN and FET combination is the square, and the S11 of the OMN is the X.

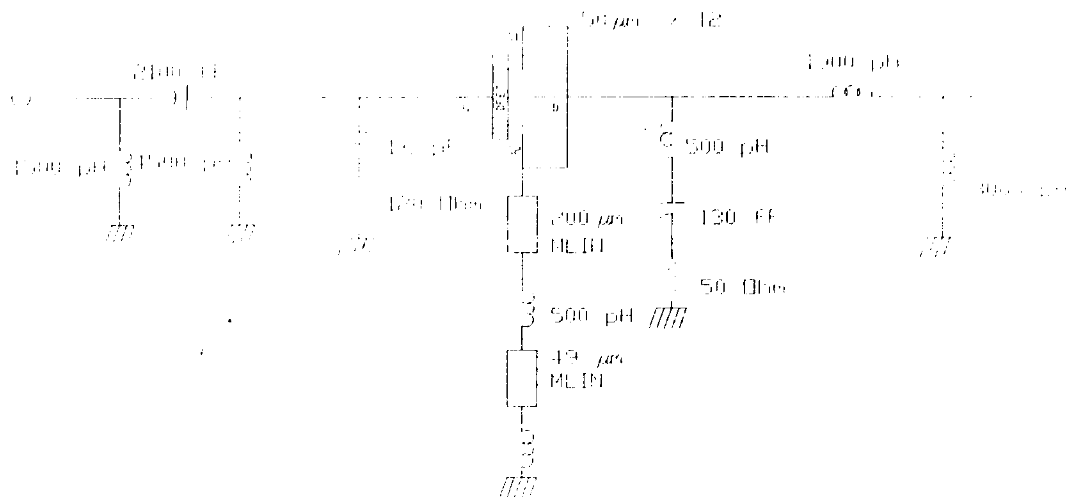


Figure 5 Schematic of the completed electrical design including, FET, input matching network, output matching network, and stabilization circuitry.

2.4. S Parameters (Low Noise Stage)

I tested the circuit of Figure 5 using the linear test bench. Figure 6 shows the S parameters of the completed electrical design of Figure 5. S11 (input return loss) is shown by the solid line and is below 10 dB for the frequency range of 4.1-6.3 GHz, so its reasonable to expect that when the amps are cascaded the return loss specification will be met. S21 (gain) is shown by the dotted line and is 6 dB at the design frequency of 4.7 GHz, so with a reasonable gain in the output stage I can expect the gain to be in spec.

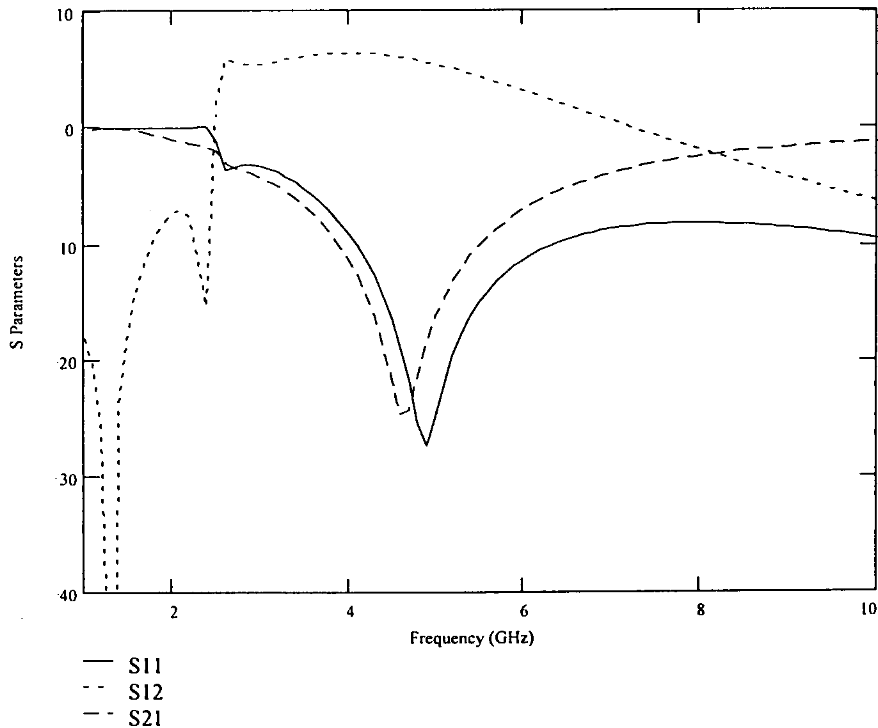


Figure 6 shows the S parameters of the completed electrical design of Figure 5.

2.5. *Stability (High Gain Stage)*

I used a similar approach to stabilization of the output high gain stage as I did in Section 2.1, except that I used no source inductor for in band stabilization , but I did use input and output stabilization circuitry for the stabilization. Figure 7 shows the geometrically derived stability parameters for the output high gain stage. Figure 8 shows the resultant input and output stabilization circuitry.

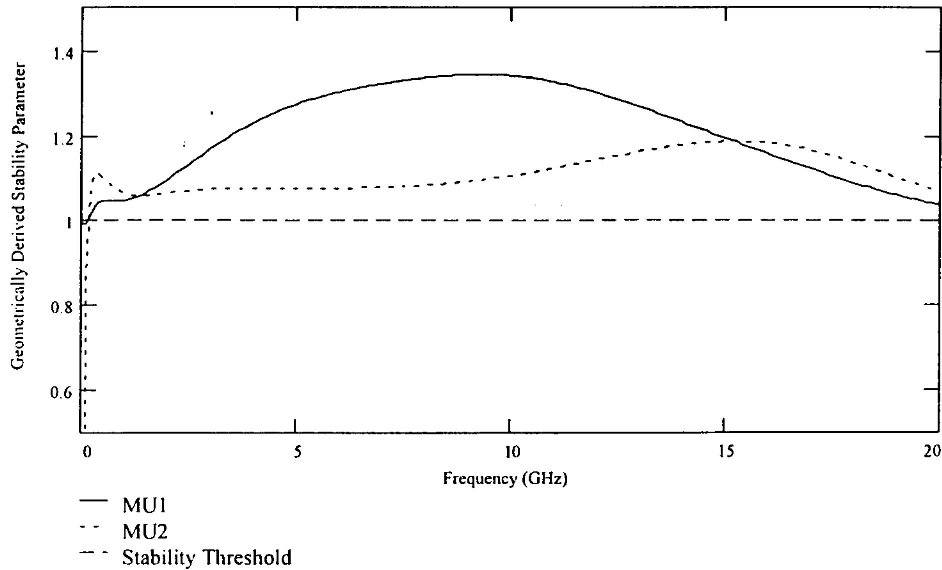


Figure 7 shows the geometrically derived stability parameters for the output high gain stage.

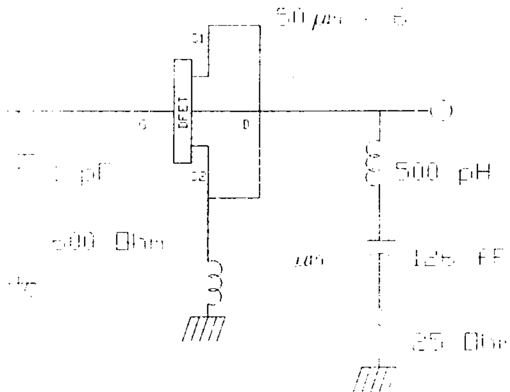


Figure 8 shows a schematic of the stabilized FET used in the output high gain stage.

2.6. *Matching (High Gain Stage)*

Matching for the output high gain stage was much simpler, since all I had to due was design matching networks for the simultaneous conjugate match points. I used a similar procedure as in Section 2.2, that is I made sure I had an inductor to ground next to the FET and I used the LIBRA optimizer to minimize the distance between either S11 of the OMN or S22 of the IMN and GM2 and GM1 respectively. Figure 9 shows the complete output high gain amplifier with input matching, output matching, and stabilization circuitry.

I tested circuit of Figure 9 on the linear test bench and the results are shown in Figure 10. The dashed line is S22 (output return loss) which is below 10 dB for the frequency range of 4.35-5 GHz, so its reasonable to expect that the output return loss will be in spec when the circuits are cascaded. The dotted line is S21 (gain) which is 7 dB at the design frequency of 4.7 GHz.

Figure 9 shows the complete output high gain amplifier with input matching, output matching, and stabilization circuitry.

Figure 10 shows the results of the linear test bench measurement of the S parameters of Figure 9.

2.7. Cascaded Performance

Since the output matching network of the first stage is designed to turn 50 Ω to the desired output match and the input matching network is designed to turn 50 Ω into the desired input match it seems reasonable that simply cascading the two amplifiers would provide sufficient interstage matching. I make no claims that this is the optimal interstage matching, but because of the limited time available to redesign the circuit this was the most expedient approach. So I simply cascaded the two amplifiers and tested them on the linear bench. Figure 11 shows the performance of the cascaded amplifiers. The S11 parameter is the solid line and it is below 10 dB for the frequency range of 4-5.5 GHz which is well within spec. The dashed line is the output return loss, and its 10 dB bandwidth is 4.2-5 GHz which is also well within spec. The S21 parameter is shown by the dotted line and is marginally within spec with 13 dB gain at 4.7 GHz.

The 3 dB bandwidth of the amplifier is 3.4-5.2 GHz or 1.8 GHz. The noise figure of the cascaded circuit is shown in Figure 12. The Noise figure is below 3 db for 2.5-10 GHz.

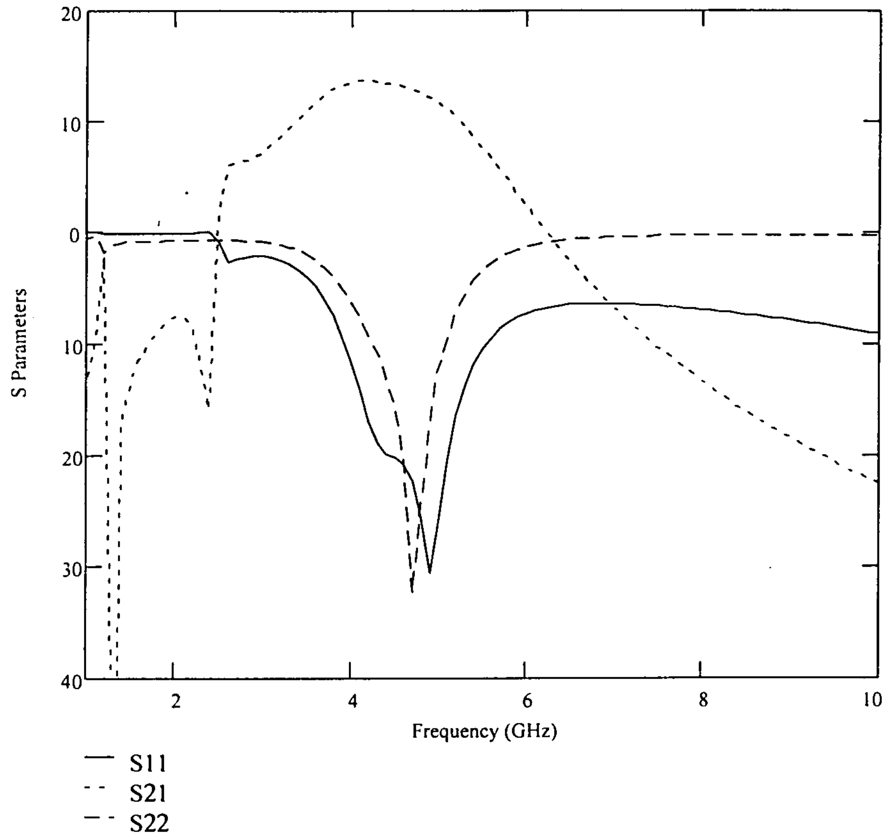


Figure 11 shows the performance of the cascaded amplifiers.

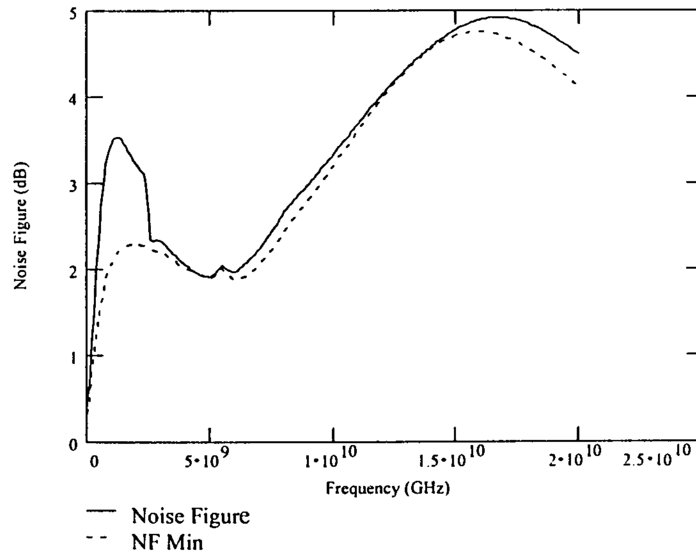


Figure 12 shows the cascaded noise figure of the electrical design.

3. Layout

The layout was difficult because of the large number of inductors in the circuit, but somehow I managed to squeeze the amp on the Anachip.

3.1. *Bias Circuitry*

As I discussed in sections 2.2, 2.3, and 2.6 I included the bias inductor in the input and output matching network design, so all I had to do to add bias tees was to add as large a MIM capacitor as I could fit in the layout and provide a wire bond pad to complete the bias tee. I decided to use self bias, because I thought this would require less space overall then added bias pads for both gates and both drains. Both FETs require Vds to be 2.5 and Id to be 10 mA. I obtained the resistor value by getting an approximate value from homework #5 and tuning Vdd and Rs to get the desired bias point for each FET. See section 3.2 for the resistance and voltage values.

3.2. *Simulation*

After laying out the circuit with TriQuint elements and interconnecting MLINs, I simulated the circuit. I found that the input and output matches were out of spec. I then tuned the input and output matching networks to bring the circuit back in spec. After tuning I simulated the circuit for bias, linear S parameters, and 3 dB compression point.

3.2.1. Bias

Table I shows the bias simulation results. I tuned the source resistance and Vdd bias voltage while monitoring the source voltage, drain voltage, and drain current until the desired results for Vds and Id were obtained.

	Id (mA)	Vdd Bias (Volt)	Vds (Volt)	Source Resistance (Ohm)
Low Noise FET	10.01	2.9	2.52	20
High Gain FET	9.81	2.9	2.64	35

Table 1 shows the bias simulation results.

3.2.2. Linear S parameters

Figure 13 shows the S parameters of the cascaded circuit The S11 parameter is the solid line and it is below 10 dB above 3.9 GHz which is well within spec. The dashed line is the output return loss, and its 10 dB bandwidth is 3.9-5.1 GHz which is also well within spec. The S21 parameter is shown by the dotted line, and it meets spec with 13.5 dB gain at 4.7 GHz. The 3 dB bandwidth of the amplifier is 3-5.3 GHz or 2.3 GHz. The noise figure of the cascaded circuit is shown in Figure 14. The Noise figure is below 3 db for 3.6-5.3 GHz. Figure 16 shows the input 3 dB compression point of the cascaded circuit. When the input power is 2 dBm the output power is 12 dBm, so the IP3 is 2 dBm which is in spec. The rest of the design goals and simulated specs are tabulated in section 5.

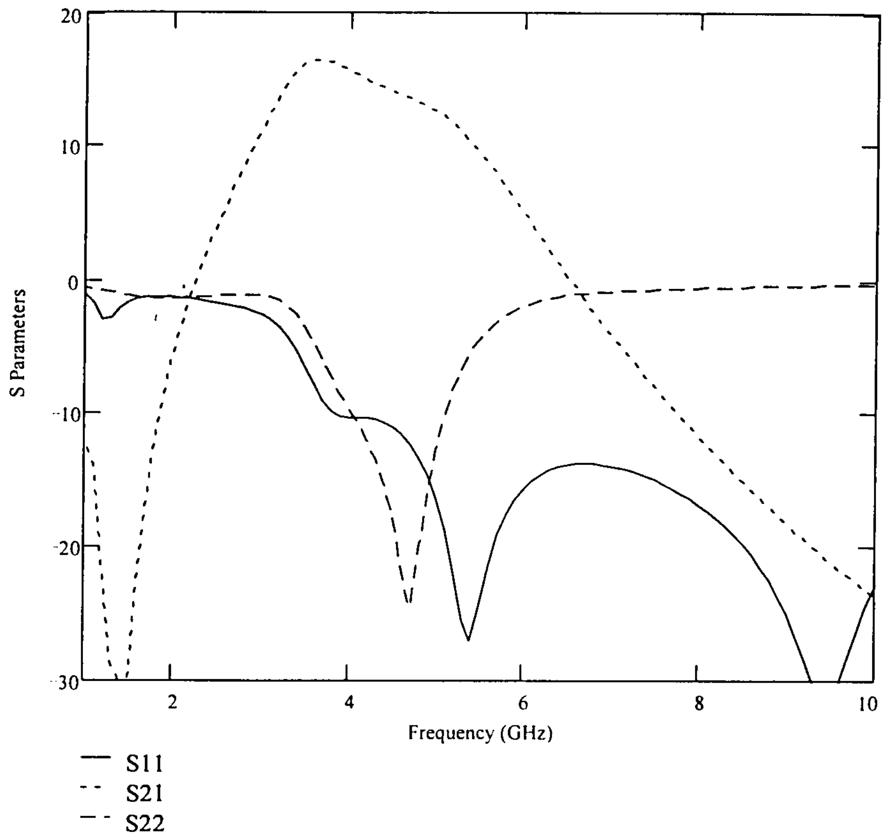


Figure 13 shows the S parameters of the cascaded circuit

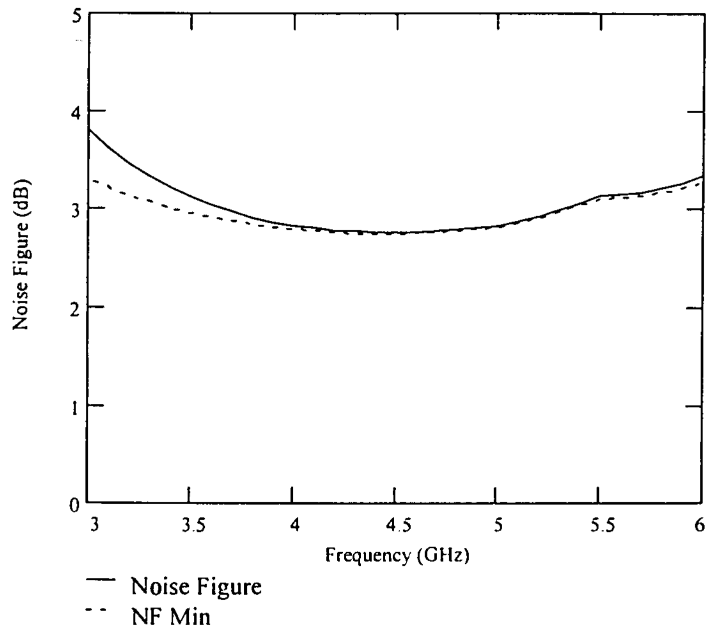


Figure 14 shows the noise figure of the cascaded circuit.

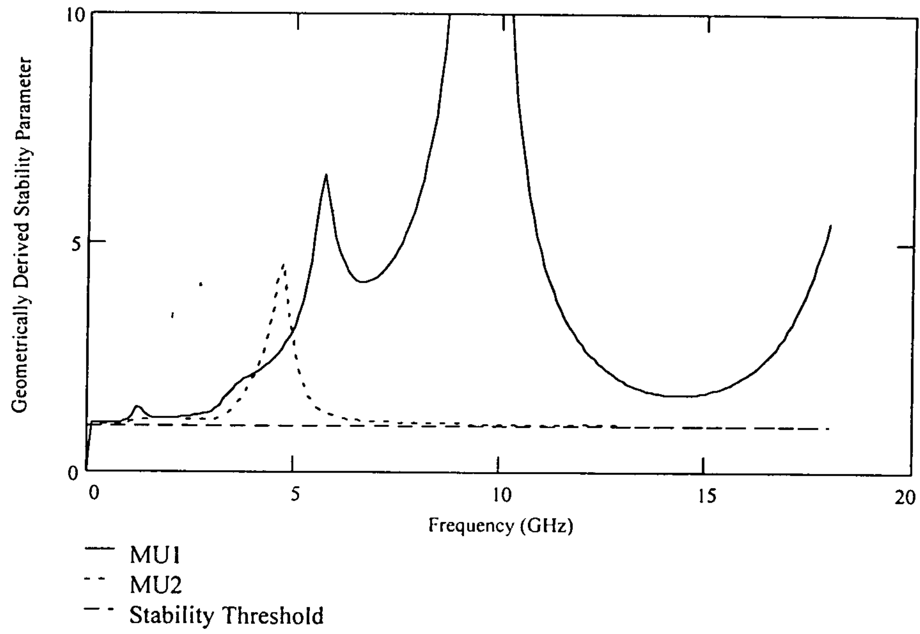


Figure 15 shows the stability of the final layout.

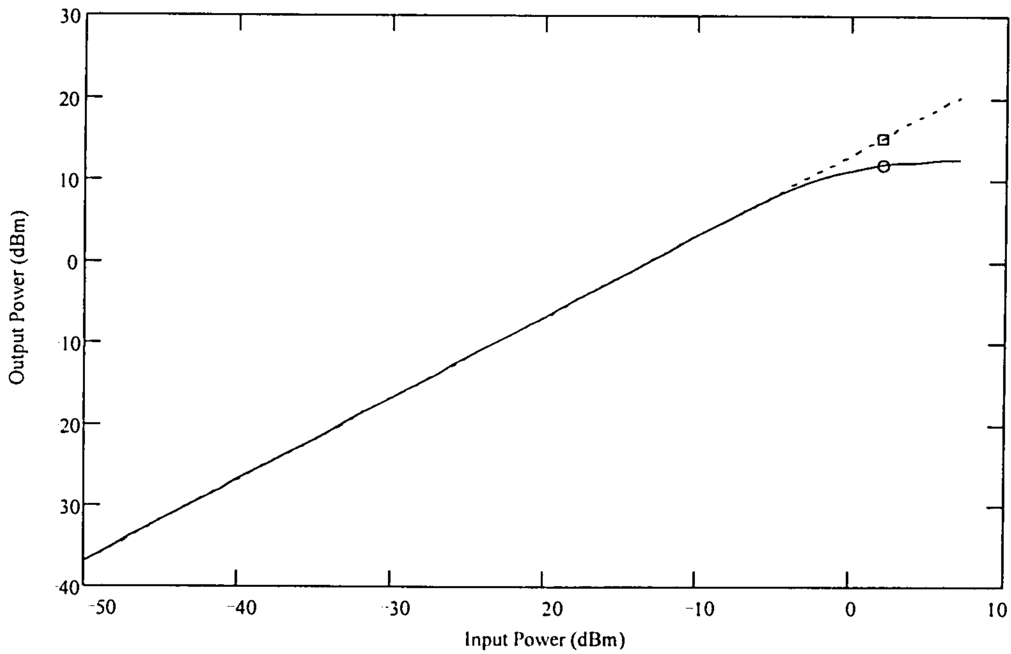


Figure 16 shows the input 3 dB compression point of the cascaded circuit.

3.3. Topology

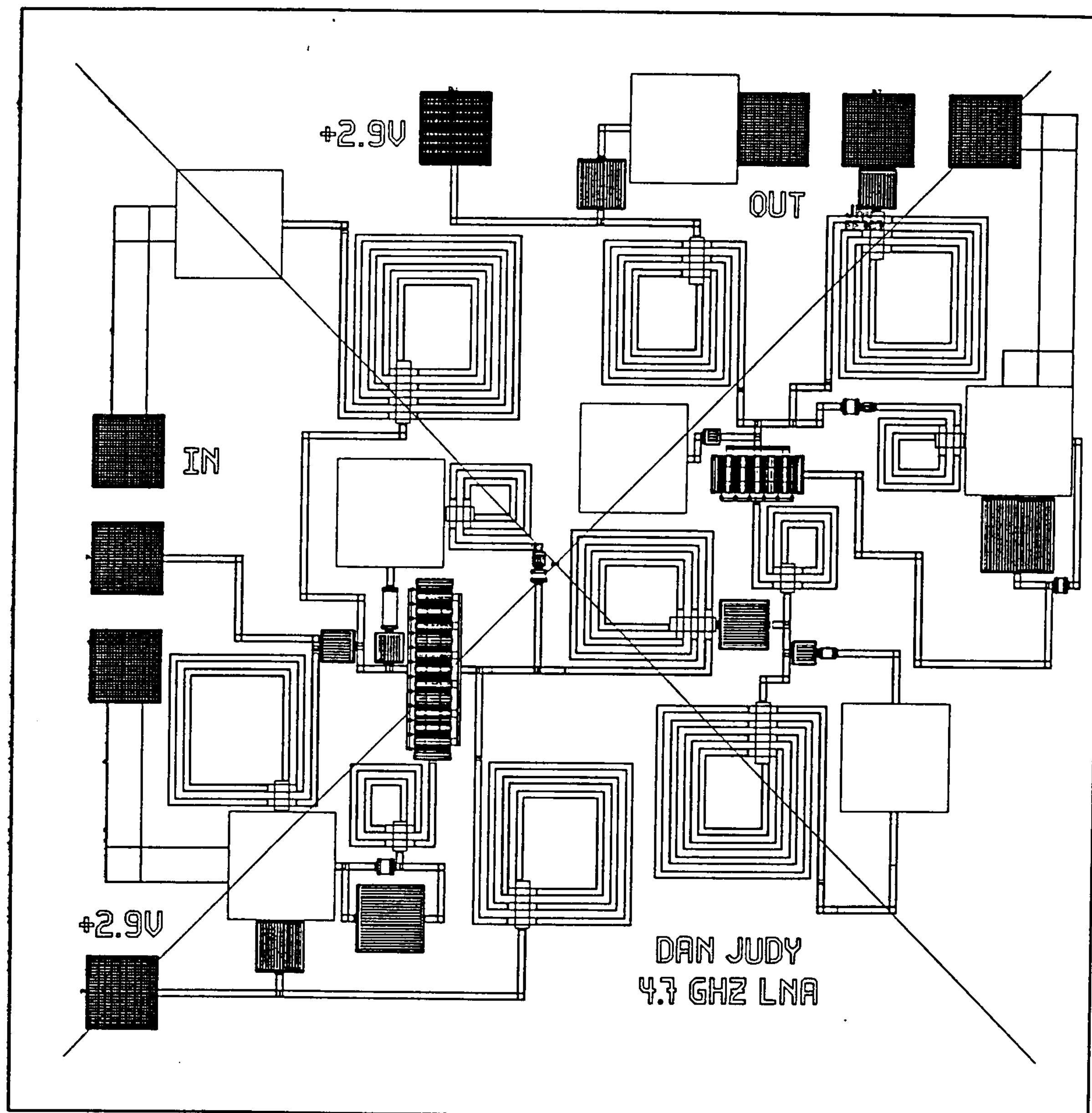


Figure 17 shows the final layout of the circuit.

4. Test Plan

4.1. Equipment

The equipment required to perform the test are as follows

network analyzer	spectrum analyzer	noise figure test set
3 volt power supply	sweep oscillator	2 x ammeter

4.2. *Procedure*

4.2.1. Network Analyzer Setup

4.2.1.1. set the bias supply at 2.9 volts

4.2.1.2. connect the bias through the ammeters to the pads marked on the chip

4.2.1.3. calibrate the network analyzer

4.2.1.4. position the port 1 probe head to the ground signal ground pads marked IN on the chip

4.2.1.5. position the port 2 probe head to the ground signal ground pads marked OUT on the chip

4.2.1.6. measure and record the S parameters

4.2.2. Noise Figure Test Setup

4.2.2.1. set the bias supply at 2.9 volts

4.2.2.2. connect the bias through the ammeters to the pads marked on the chip

4.2.2.3. calibrate the noise figure test set

4.2.2.4. position the port 1 probe head to the ground signal ground pads marked IN on the chip

4.2.2.5.position the port 2 probe head to the ground signal ground pads marked OUT on the chip

4.2.2.6. measure and record the noise figure over the frequency range 4-6 GHz

4.2.3. dB Compression Measurement

4.2.3.1. set the bias supply at 2.9 volts

4.2.3.2. connect the bias through the ammeters to the pads marked on the chip

4.2.3.3. position the port 1 probe head to the ground signal ground pads marked IN on the chip

4.2.3.4. position the port 2 probe head to the ground signal ground pads marked OUT on the chip

4.2.3.5. connect the sweep oscillator to the input probe head

4.2.3.6. connect the spectrum analyzer to the output probe head

4.2.3.7. set the sweep oscillator to CW operation at 4.66 GHz

4.2.3.8. adjust the output power of the sweep oscillator until the spectrum analyzer is 10 dB above the sweep oscillator power, this is the IP3

5. Specifications

Specification	Goal	Simulation	Test
Frequency	4.635 to 4.685 GHz	3-5.3 GHz	
Bandwidth	50 MHz	2.3 GHz	
Gain	13 dB	13.5 dB	
Gain Slope	0.01 dB/MHz	0.005 dB/MHz	
Gain Ripple	±2 dB	±3 dB	
Noise Figure	2 dB goal, 3 dB	2.8 dB	
Input IP3	-15 dBm	2 dBm	
Return Loss Input	10 dB	12.3 dB	
Return Loss Output	10 dB	24.5 dB	
Size	FIT ON ANACHIP	MET	

Frequency Tripler

MMIC DESIGN 525.787
Fall 1997

Carson Murray

I.Summary

This MMIC design is a x3 multiplier using the TriQuint Semiconductor process. The goal is to have an rf input of 1545 - 1761 Mhz at 0 dBm and an rf output of 4635 - 5283 Mhz at 0 dBm with the other harmonics attenuated by > -15 dBc. This MMIC will be part of a chip set for use in a WLAN Transceiver application.

II.Introduction

Circuit Description:

The schematic design consists of three stages, which are the input multiplier, filter, and output amplifier. The input multiplier is a GFET biased to operate close to the pinch-off region of the DC I-V curves. This is done in order to have a very low Pout compression point and by doing this will force the output to have something close to a square wave, which is rich in third order products.

The filter is a 3 pole series/shunt resonance topology which is done to attenuate unwanted 2nd order and fundamental frequency components. The output amplifier is designed to further boost the output power to approximately 0 dBm.

Design Philosophy:

The 300μm GFET device was choosen as the active device for use in both the input multiplier and output amplifier stages. This type and size of FET was choosen both because of its power handling capabilities and its relatively small footprint.

The biasing scheme for these devices is a simple LC network, which consists of a 600μh inductor and a 25 pf capacitor. 10pf capacitors are also used as DC blocks on both the gate and drain of the GFET.

The input/output matching networks are simple series L/shunt C topologies. The input matching circuit of the input multiplier is optimized for the input band of 1545 - 1761 Mhz, whereas the output matching circuit is designed for the upconverted band of 4635 - 5283 Mhz. The matching networks were designed to work for a slightly larger bandwidth than the actual operating bandwidth, which will increase the yield of the MMIC because process variations will cause the frequency response to shift.

The bias point for the input multiplier stage was choosen to be +7 volts at the drain and -2 volts at the gate. This puts the GFET close to pinchoff and reduces the output compression point such that the 3rd order products are maximized. The bias point for the

output amplifier was chosen for maximum gain which was +2volts at the drain and 0 volts at the gate.

The filter was designed to reject the fundamental and the second harmonic and pass the 3rd harmonic with as little attenuation as possible. The higher order products are already low enough coming outside of the input multiplier that further filtering is not necessary. The filter consists of three sections of LC resonators, including 2 shunt and 1 series. These are few components as possible in order get the desired rejection and minimize chip area. The inductors were also choosen to be the minimum value of 500 μh and the capacitors were optimized to give the desired response. This was done becasue inductors take up much more real estate than capacitors. The filter is placed before the amplifier instead of after because this improves the rejection of the unwanted harmonics.

The MMIC uses +/- 7 volts as its bias supply and used GSG for its RF input/output in order to make use of on-wafer probing. Resistor dividers are used to provide the designed bias condition at the FET.

Trade Offs:

The modeled performance of the MMIC gives an output power of the 3rd order at about 0 dBm and a bandwidth of approximately 0.7 Ghz. Because of limited chip space, I was unable to add another gain stage to boost the output power up to the goal of +10 dBm, and I could not add 2 pole matching networks, which would increase the bandwidth to the desired 1.1 Ghz.

A full-wave diode bridge would be the optimal way to design a frequency tripler because the output would be a pure square wave, which has relatively high power odd harmonics. This approach was not used because there is no model for a TriQuint process diode. Using the GFET as the multiplier is not ideal because it puts out a fairly high level 2nd harmonic which creates the need for the filter stage.

III. Modeled Performance

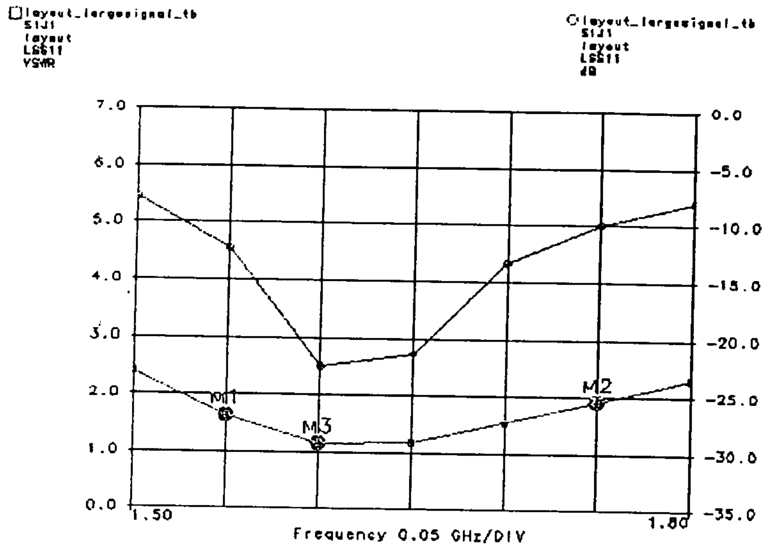
The following is a table showing the expected performance vs. the desired performance.

	Specifications	Final Layout Results
Input Frequency (Mhz)	1545 - 1761 min.	1500 - 1800
Output Frequency (Mhz)	4635 - 5283 min.	4600 - 5300
Bandwidth (Ghz)	1.1 goal	0.7
Input Level (dBm)	0	0
Output Level (dBm)	0 (+10 goal)	0
VSWR	1.5:1 IN/OUT	1.05:1 - 2.37:1
Spectral Purity (dBc)		
Fundamental	> -15	> -25
2nd Harmonic	> -15	> -12
4th Harmonic	> -15	> -25
Supply Voltage (volts)	+/- 7	+/- 7
Size (mils)	60 X 50	60 X 50

Table 1. Comparison of Specs. vs. Final Layout Results

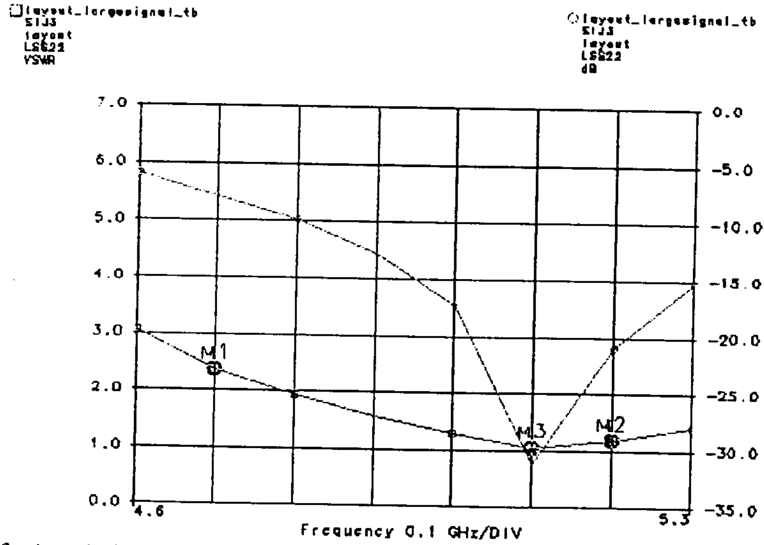
The maximum attainable bandwidth was approximately 0.7 Ghz, which fell short of the 1.1 Ghz goal. More bandwidth would have been possible using 2 pole matching networks, but limited chip space prevented doing this. The worst case second order harmonic attenuation was approximately -12 dBc. This could have been improved by adding an additional resonator in the filter, but space was again the limiting factor.

The following plots are final layout simulations.



Input VSWR of x3 Multiplier
M1 Frequency=1.55000000 value=1.65294696
M2 Frequency=1.75000000 value=1.93268272
M3 Frequency=1.60000000 value=1.16269563

Figure 1. Input Return Loss and VSWR plot



Output VSWR of x3 Multiplier
M1 Frequency=4.70000000 value=2.37403756
M2 Frequency=5.20000000 value=1.19698741
M3 Frequency=5.10000000 value=1.05662347

Figure 2. Output Return Loss and VSWR plot

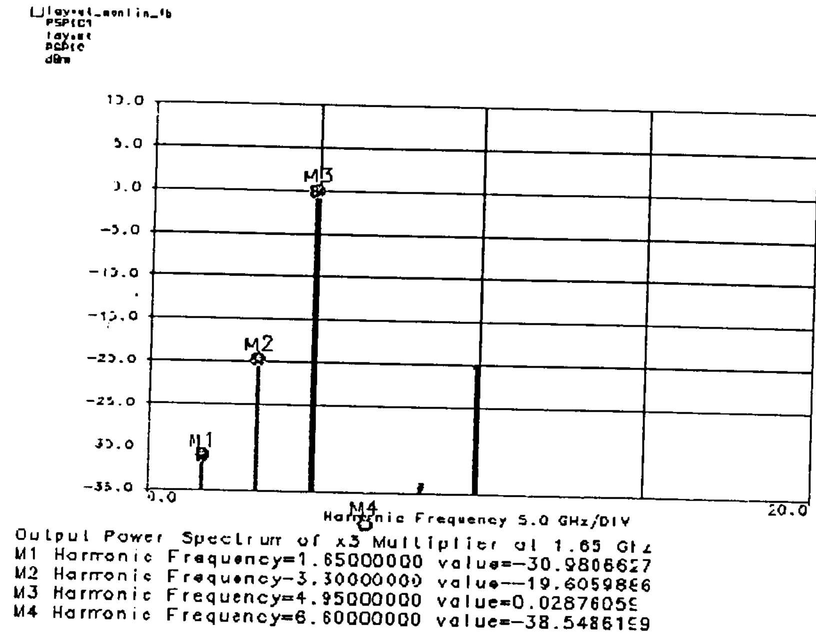


Figure 3. Output Spectrum Plot

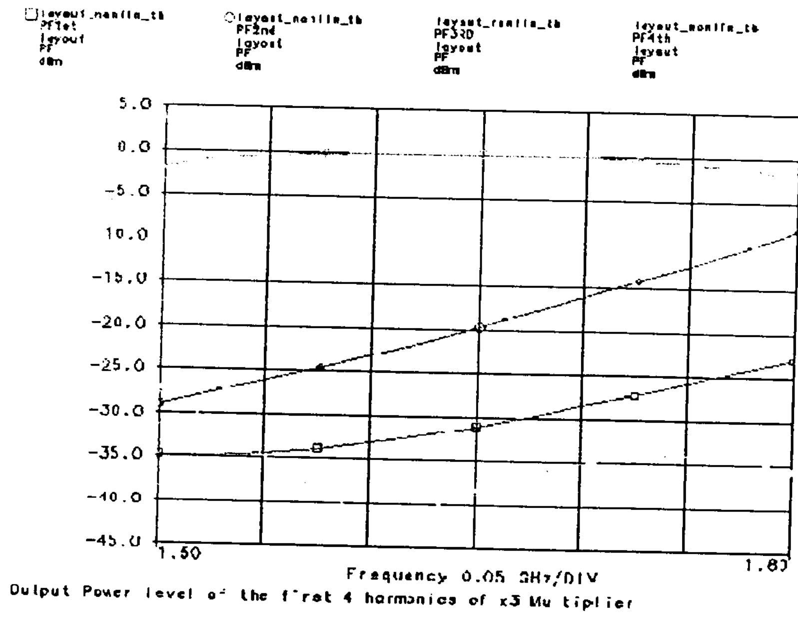


Figure 4. Output Power Level of the first 4 Harmonics

IV. Schematic Diagram

A simplified schematic showing all of the major TriQuint elements is shown in Figure 5. This includes everything but the line interconnects. All functionality is contained on-chip, therefore there is no off-chip schematic. The final layout is shown in Figure 6

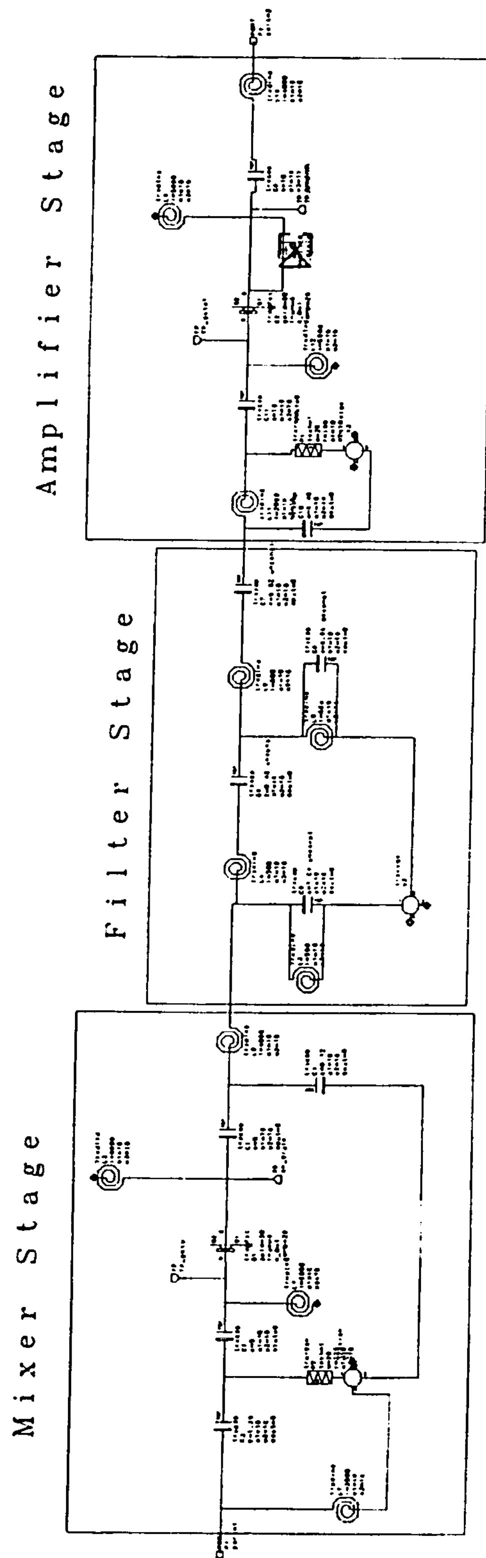


Figure 5. schematic

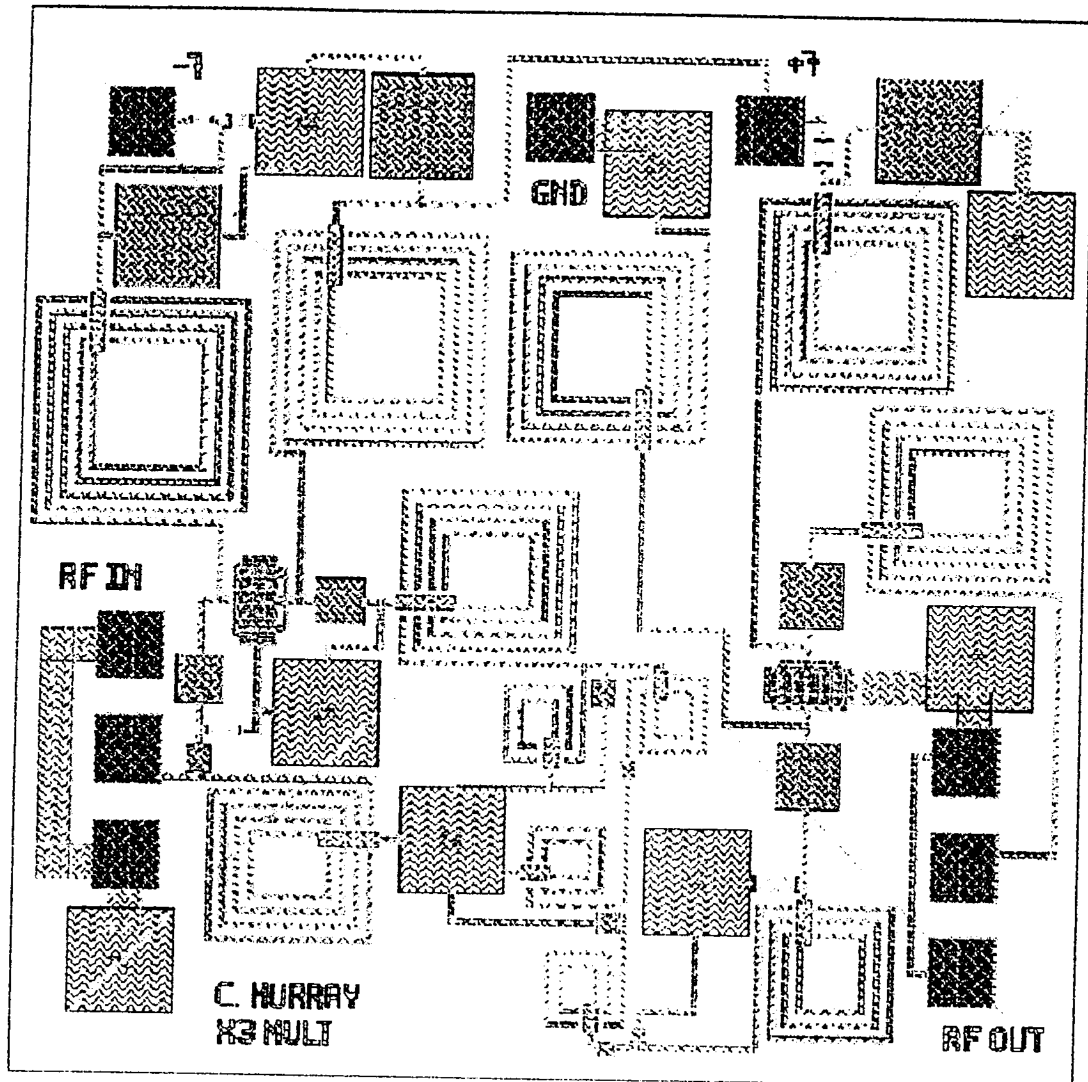


Figure 6. Final Layout of x3 Multiplier MMIC

V. DC Analysis

The libra simulations measure a total of 98ma of current for the +7 volts source and 20 ma for the -7 volt source, therefore the total power consumption of the device is 0.826 Watts. The input multiplier GFET drain current ≈ 13 ma and the output amplifier GFET drain current ≈ 84 ma

The line interconnects are using 1-ME and 2-ME which combined have a current carrying capacity of 27 ma/μm. The DC lines used for the X3 multiplier are 10μm lines, and these can carry up to 270 ma of maximum current.

VI. Test Plan

The test equipment needed for this MMIC are listed below.

- Cascade model 43 wafer probe station with 2 RF GSG probes and 3 DC needle probes. See Figure 2 and 3
- HP synthesized signal generator
- HP spectrum analyzer

The test setup is shown in Figure 1. and will use the signal generator to sweep the RF input from 1.4 - 1.8 Ghz at 0 dBm. The spectrum analyzer will be connected to the RF ouput and will measure the power level and the frequency range of all the harmonics. A power supply will supply the +/- 7 volts, which will require the use of 2 DC needle probes. A DC ground will also require another DC needle probe.

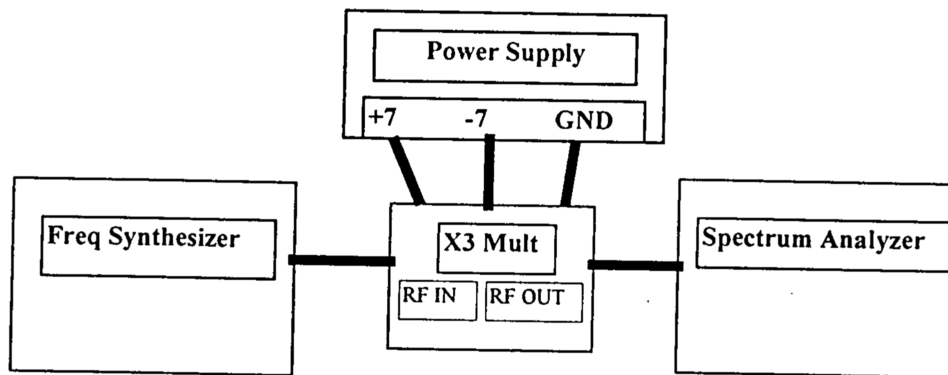


Figure 7. Test Setup for X3 Multimplier

The **MAX HOLD** feature of the HP Spectrum Analyzer will be used for the entire sweep of the Freq Synthesizer. This will display the power output for the entire swept band and using the marker function on the Spectrum Analyzer can be used to read the exact power level at each frequency.

The DC and Rf pads on the die layout are labeled as to their function. See the layout in Figure 6

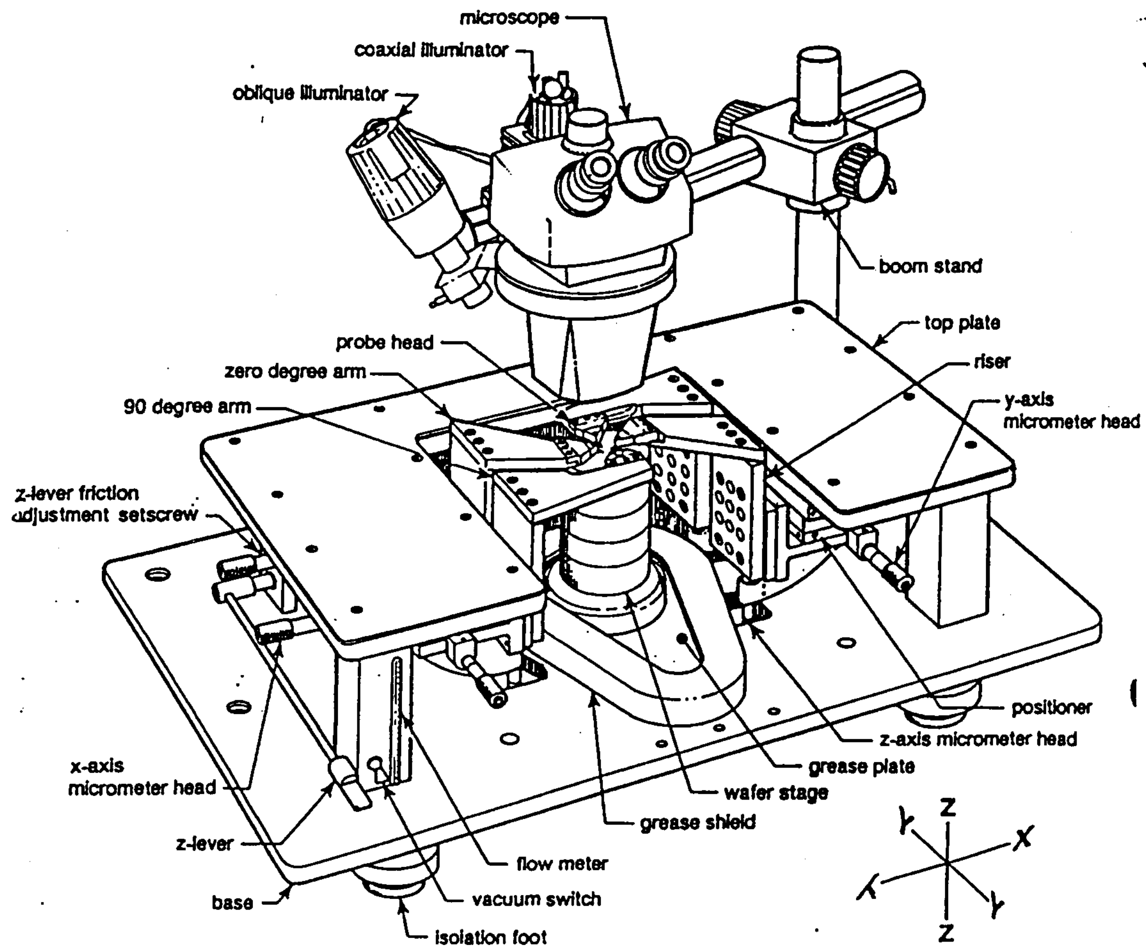


Figure 8. Cascade Probe Station

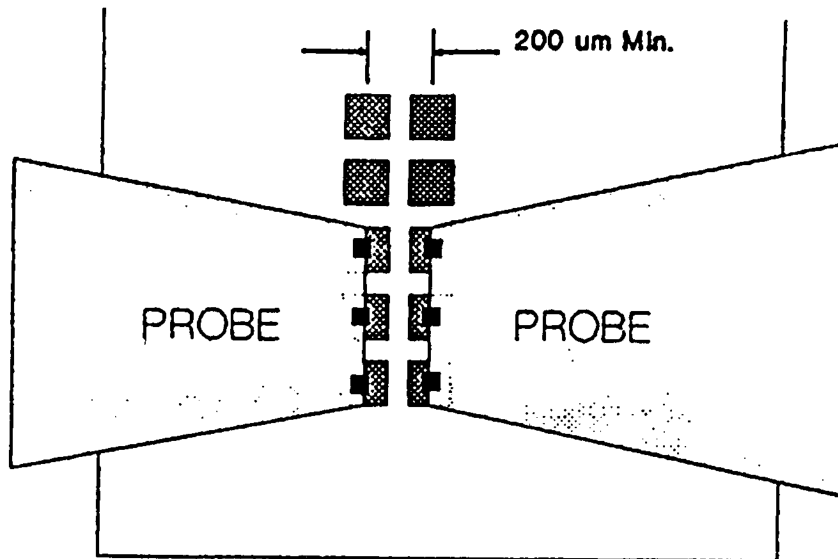


Figure 9. Close-up view of GSG probe onto RF pad of MMIC

VII. Conclusions and Recommendations

This design gives a relatively simple method for upconverting a frequency band. Since all of the specifications could not be met for a 60 X 50 mil chip, a future redesign should be considered using diodes (assuming that a model can be found) in order to maximize the 3rd order output and hopefully eliminating the need for the filter.

MMIC POWER AMPLIFER

Neal Tesny
December 8, 1997

EE787
Craig Moore
John Penn

Abstract

A design for a Microwave Monolithic Integrated Circuit (MMIC) C-band power amplifier is described. The amplifier has a 3-dB bandwidth of from 3.70 to 5.02 GHz, a gain of 12.1 dB, and an output power of 24.2 dBm at its 1dB compression point. Circuit design, layout and performance are presented.

Introduction

Circuit Description

The circuit is a 1-stage, class AB, MMIC power amplifier. It was designed to have an output power of at least +23 dBm for an operating range of from 4.635 GHz to 4.685 GHz. Other requirements were: a bandwidth of at least 50 MHz, a gain of at least 12 dB, a maximum gain ripple of ±0.5 dB, an efficiency of at least 15 % @ 1dB compression, and input and output VSWRs of less than 1.5:1. The supply voltages were limited to +8 V and –5 V. The circuit was to be placed on a 60×60 mil ANACHIP. The TriQuint process was used for design and production of the circuit.

A basic schematic of the circuit is shown in Figure 1. It uses a 6×200 μm G-FET which is biased in the AB operating region with $V_D \cong 8.0$ V and $I_D \cong 160$ mA. It uses input and output matching networks which are low-pass pi networks, i.e., 2 shunt capacitors separated by a series inductor. The drain bias network is a bias-T with RF choke and blocking capacitor. The gate bias is separated from the RF circuit by a large, 2 kΩ resistance. In addition it has input and output stability networks which provide stability at the lower frequencies while preserving gain in the operating band. The structure of these networks is shown in figure 2.

Design Philosophy

The design was started with the FET. A 1200 μm G-FET was selected in order to provide adequate output power. A DC bias check was performed and I-V curves were obtained. A Cripps load resistance of 21 Ω was chosen, and output and input networks were designed along with bias networks. Stability networks were then designed and added, and then overall tuning was performed. The circuit was designed to be self-biasing, i.e., require only drain bias voltage. However, the layout was designed to allow the overriding the self bias and the application of gate-biasing voltage if it is needed. This, however, is not recommended because the circuit was optimized for self bias and overriding may produce unstable results. This is described further in the Test Plan.

Tradeoffs

Since it was very difficult to optimize for all the design requirements at the same time, it was decided to maximize the output power ($P_{out,1dB}$) while keeping gain and VSWR just within specification. Also it was designed to operate with only a + Voltage at the expense of some output power.

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

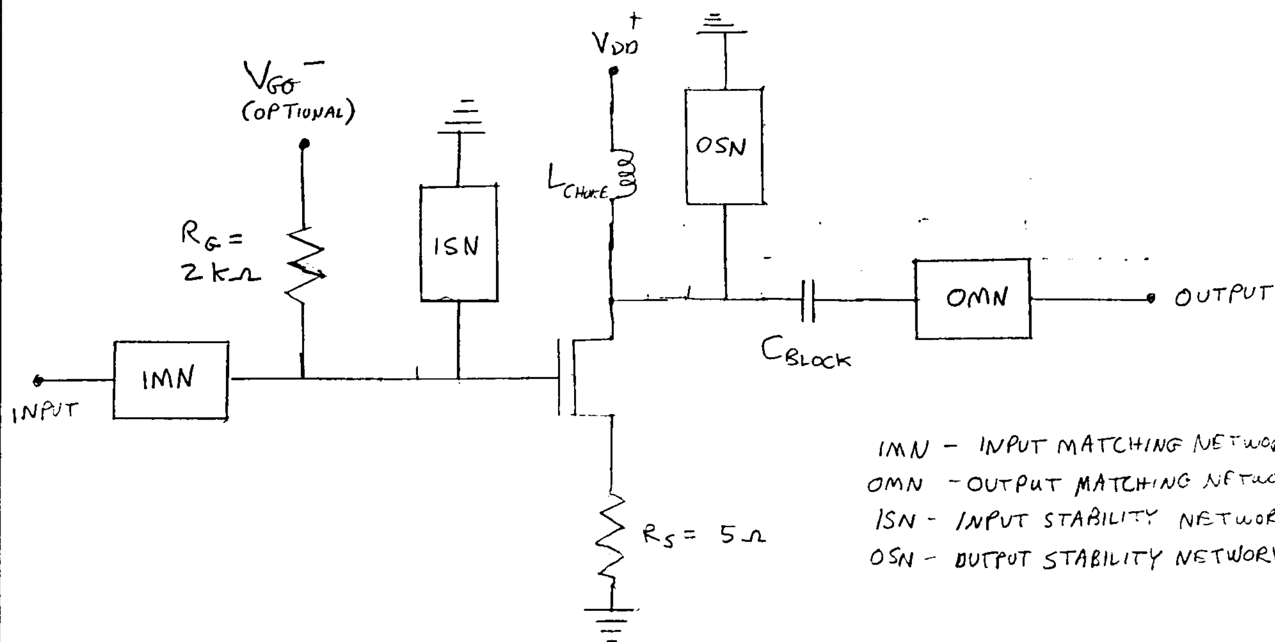


FIGURE 1. BASIC CIRCUIT SCHEMATIC.

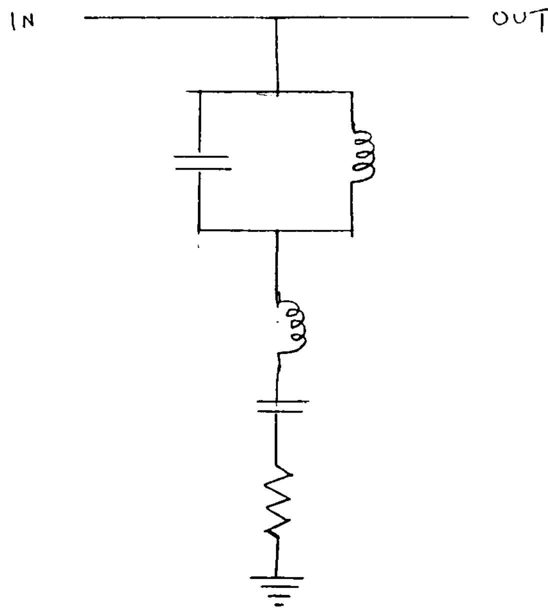
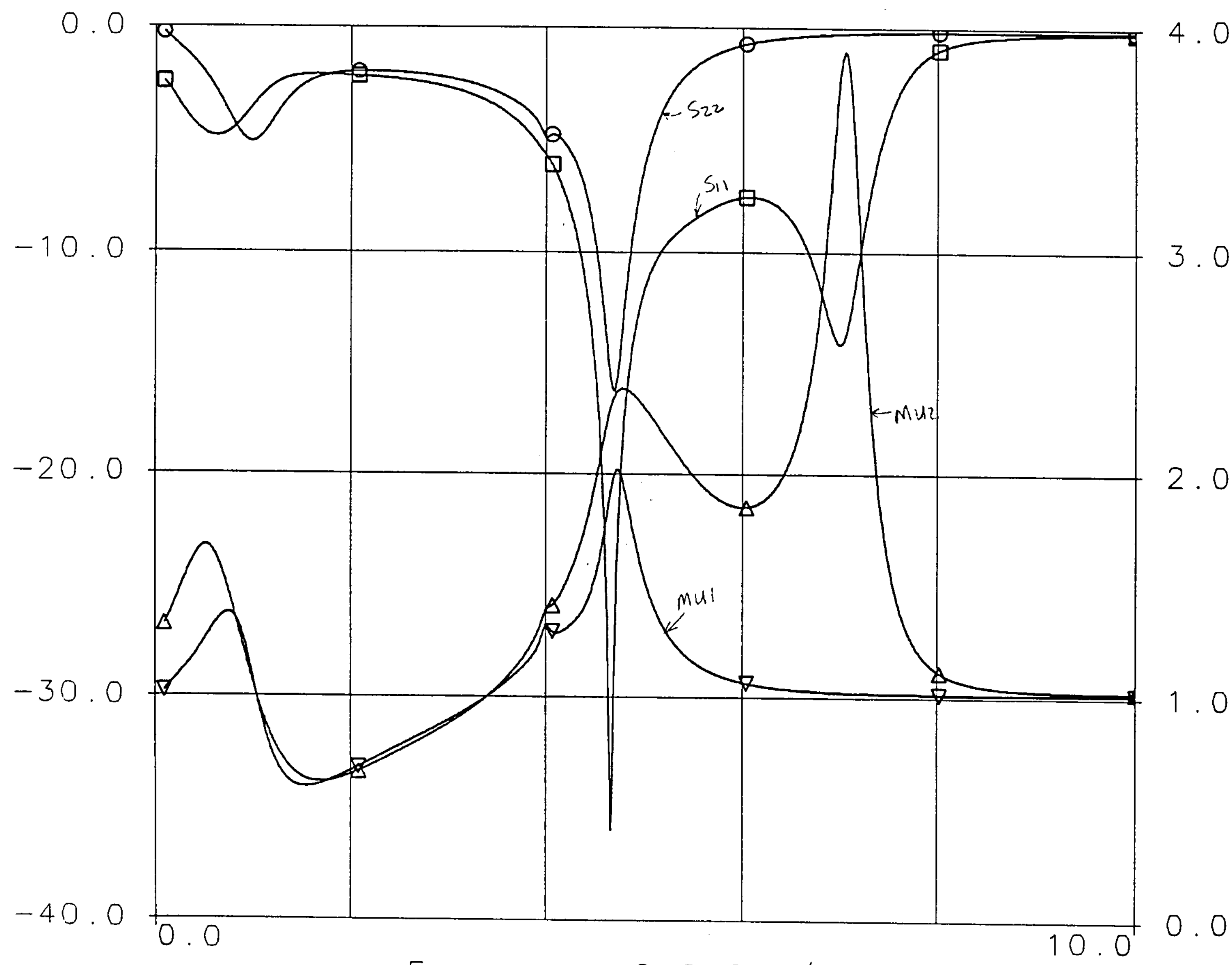


FIGURE 2. STABILITY NETWORK.

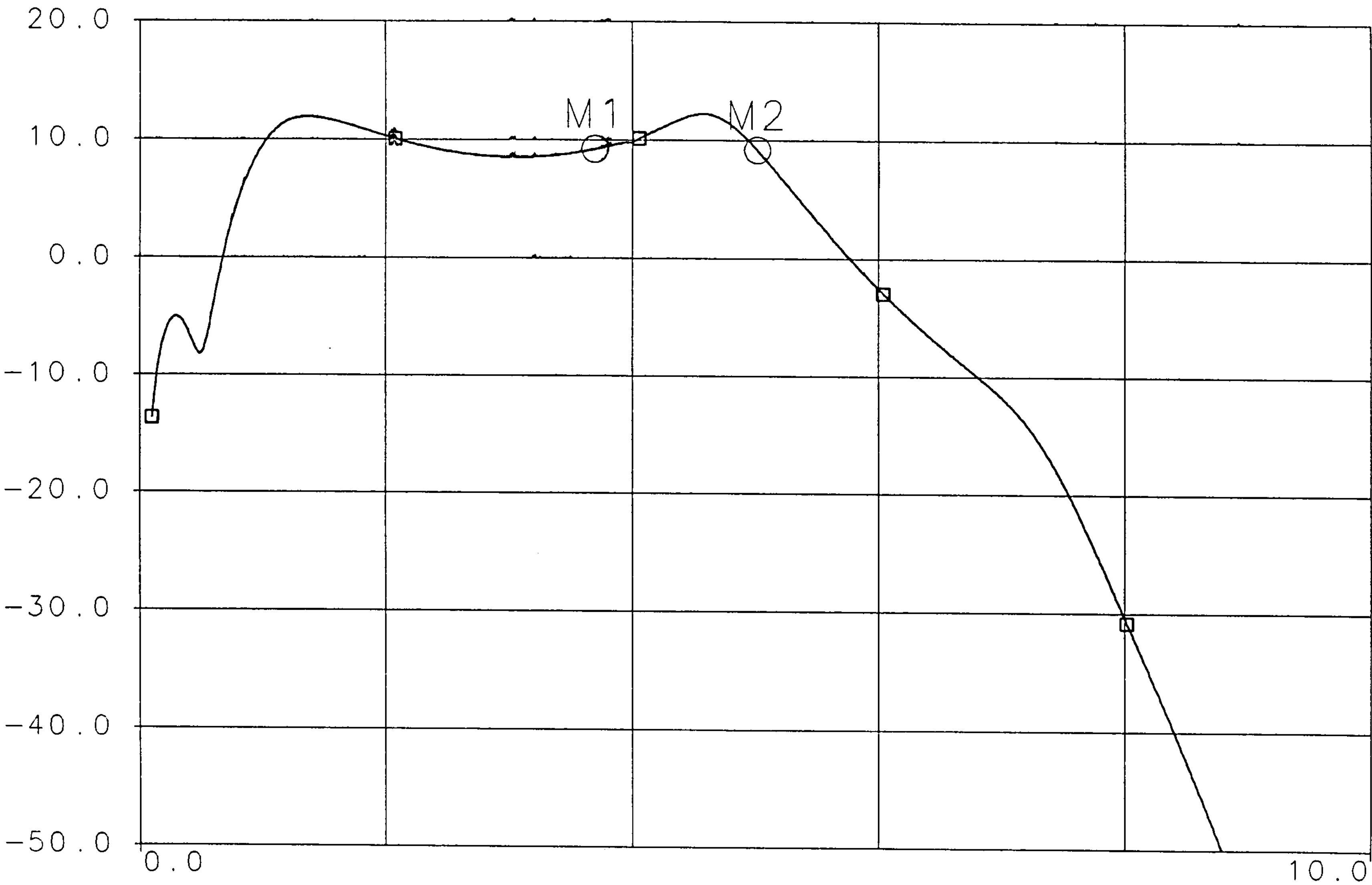
Modeled Performance

Specification Compliance Matrix

	Specification	Simulated Performance
Frequency	4.635 – 4.685 GHz	3.70 – 5.02 GHz
Bandwidth, 3 dB	> 50 MHz	1.32 GHz
Gain, small signal	> 12 dB, 15 dB goal	12.02 – 12.16 dB over spec freq.
Gain Ripple	± 0.5 dB, max.	0.14 dB over specified freq. range
Output Power, @ 1 dB compress.	> +23 dBm, +27 dBm goal	+24.2 dBm @ 4.66 GHz
Efficiency , @ 1 dB compress.	> 15 %, 25 % goal	18.37 % @ 4.66 GHz
VSWR, 50 Ω, input	< 1.5 : 1	1.03 – 1.07 over spec. freq. range
VSWR, 50 Ω, output	< 1.5 : 1	1.36 – 1.45 over spec. freq. range
Supply Voltage	+8 V, –5 V; + Volts only, goal	+8.0 V only
Size	60 × 60 mil ANACHIP	60 × 60 mil ANACHIP



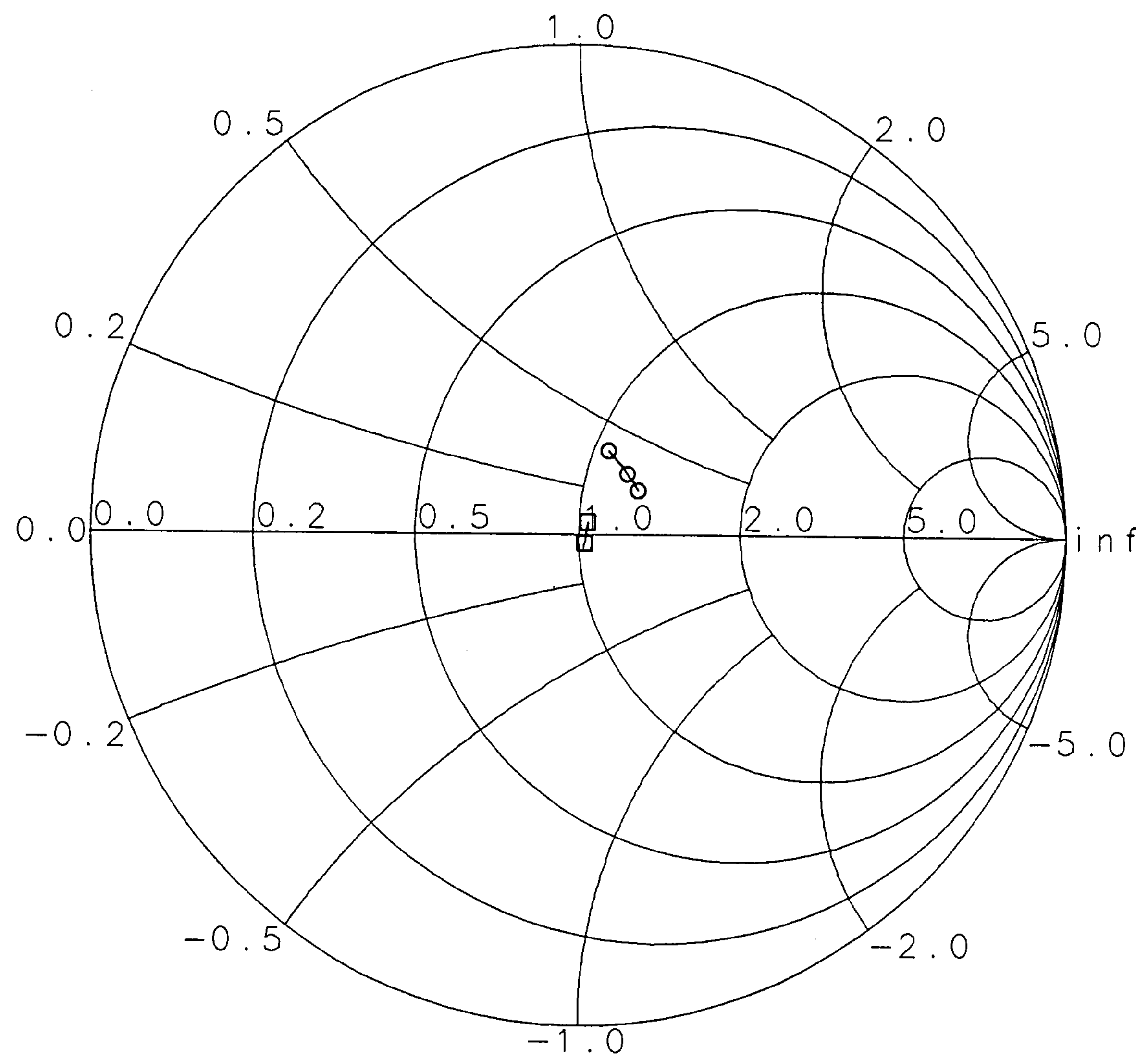
S11, S22, MU1, AND MU2 OF CIRCUT



GAIN OF CIRCUIT
3DB BANDWITH IS 1.32 GHZ (3.70 TO 5.02 GHZ)

S-PARAMETERS AND VSWR OF CIRCUIT IN OPERATING BAND:

Frequency GHz	plin1_tb S11 schema7 S[1,1] dB	plin1_tb S22 schema7 S[2,2] dB	plin1_tb S21 schema7 S[2,1] dB	plin1_tb VSWR1 schema7 VSWR[1]	plin1_tb VSWR2 schema7 VSWR[2]
4.635000000	-29.5160	-14.7297	12.1620	1.0692	1.4493
4.640000000	-30.8020	-14.9380	12.1519	1.0594	1.4364
4.645000000	-32.2022	-15.1386	12.1409	1.0503	1.4243
4.650000000	-33.6645	-15.3295	12.1290	1.0424	1.4132
4.655000000	-35.0254	-15.5086	12.1162	1.0361	1.4030
4.660000000	-35.9412	-15.6738	12.1026	1.0324	1.3939
4.665000000	-36.0181	-15.8226	12.0880	1.0321	1.3859
4.670000000	-35.2243	-15.9530	12.0725	1.0353	1.3791
4.675000000	-33.9324	-16.0627	12.0561	1.0410	1.3735
4.680000000	-32.5066	-16.1499	12.0388	1.0485	1.3690
4.685000000	-31.1304	-16.2129	12.0206	1.0571	1.3659



Frequency 4.635 to 4.685 GHz

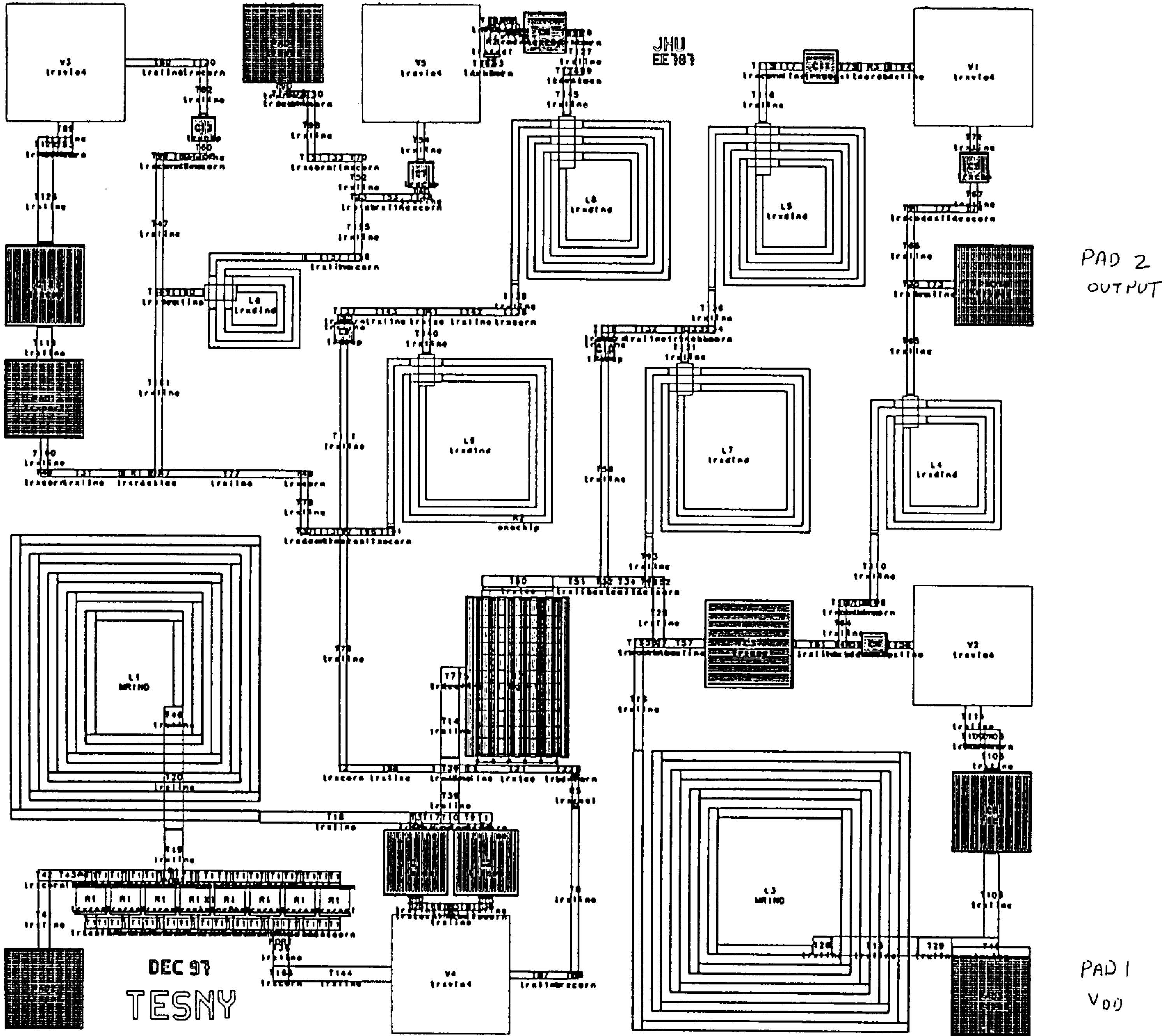
S11 AND S22 IN OPERATING BAND

POWER OUT, POWER IN, POWER-ADDED EFFICIENCY, AND DC-TO-RF EFFICIENCY

Frequency = 4.660000000 GHz

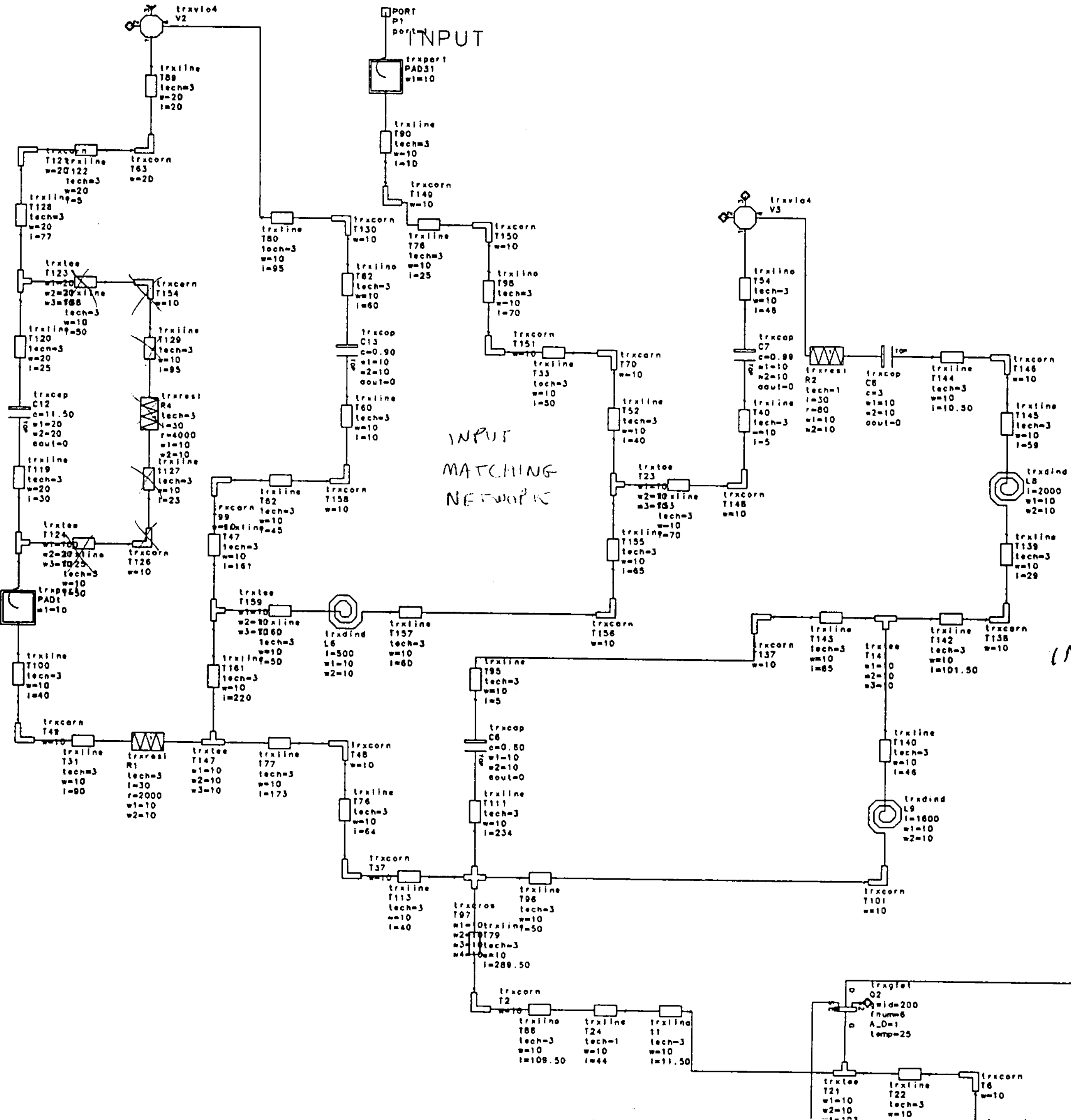
Power dBm	pharmbal1b_tb PF1 schema7b PF dBm	pharmbal1b_tb PF2 schema7b PF dBm	pharmbal1b_tb PAE1 schema7b PAE	pharmbal1b_tb DCRF1 schema7b DCRF
10.000000000	20.8405	9.9786	8.8995	9.6945
10.100000000	20.9434	10.0784	9.1090	9.9221
10.200000000	21.0463	10.1781	9.3234	10.1549
10.300000000	21.1491	10.2778	9.5427	10.3931
10.400000000	21.2519	10.3774	9.7670	10.6367
10.500000000	21.3545	10.4771	9.9962	10.8856
10.600000000	21.4570	10.5767	10.2303	11.1399
10.700000000	21.5592	10.6762	10.4693	11.3995
10.800000000	21.6611	10.7758	10.7130	11.6643
10.900000000	21.7625	10.8752	10.9613	11.9342
11.000000000	21.8635	10.9747	11.2139	12.2089
11.100000000	21.9637	11.0741	11.4706	12.4881
11.200000000	22.0632	11.1734	11.7311	12.7717
11.300000000	22.1619	11.2728	11.9951	13.0593
11.400000000	22.2595	11.3720	12.2623	13.3506
11.500000000	22.3560	11.4712	12.5322	13.6452
11.600000000	22.4514	11.5704	12.8046	13.9429
11.700000000	22.5454	11.6695	13.0790	14.2431
1.800000000	22.6379	11.7686	13.3549	14.5456
1.900000000	22.7290	11.8676	13.6320	14.8498
12.000000000	22.8184	11.9665	13.9096	15.1552
12.100000000	22.9060	12.0654	14.1870	15.4611
12.200000000	22.9917	12.1642	14.4639	15.7671
12.300000000	23.0755	12.2629	14.7399	16.0729
12.400000000	23.1574	12.3616	15.0151	16.3787
12.500000000	23.2377	12.4603	15.2898	16.6848
12.600000000	23.3162	12.5589	15.5641	16.9914
12.700000000	23.3931	12.6574	15.8372	17.2975
12.800000000	23.4677	12.7559	16.1070	17.6010
12.900000000	23.5395	12.8542	16.3697	17.8983
13.000000000	23.6072	12.9524	16.6201	18.1839
13.100000000	23.6698	13.0503	16.8520	18.4519
13.200000000	23.7263	13.1480	17.0597	18.6962
13.300000000	23.7763	13.2455	17.2369	18.9103
13.400000000	23.8194	13.3432	17.3743	19.0846
13.500000000	23.8557	13.4416	17.4655	19.2120
13.600000000	23.8868	13.5408	17.5170	19.2992
13.700000000	23.9149	13.6404	17.5442	19.3618
13.800000000	23.9464	13.7396	17.5944	19.4488
13.900000000	23.9889	13.8376	17.7222	19.6167
14.000000000	24.0409	13.9352	17.9136	19.8510
14.100000000	24.0953	14.0336	18.1216	20.1035
14.200000000	24.1421	14.1332	18.2768	20.3029
4.300000000	24.1763	14.2339	18.3461	20.4149
.400000000	24.2028	14.3346	18.3678	20.4789
14.500000000	24.2223	14.4348	18.3539	20.5075
14.600000000	24.2331	14.5344	18.3002	20.4971
14.700000000	24.2376	14.6340	18.2620	20.5089

1dB compression
24.2 dBm



CIRCUIT LAYOUT

Schematic Diagrams



INPUT
INPUT MATCHING NETWORK
INPUT STABILITY NETWORK
open/Vgg
GATE BIAS

OUTPUT

OUTPUT MATCHING NETWORK

OUTPUT STABILITY NETWORK

← FET

trxvia4 V5

trxline T71 tech=3 w=10 l=30

trxcap C5 c=1.35 w1=10 w2=10 oout=0

trxline T67 tech=3 w=10 l=28

trxcorn T74 w=10

trxline T72 tech=3 w=10 l=70

trxcorn T91 w=10

trxline T66 tech=3 w=10 l=85.50

trxtee T35 w1=10 w2=10 w3=10

trxline T03 tech=3 w=10 l=50

trxport PAD3 w1=10

PORT P2 port=2

trxline T65 tech=3 w=10 l=133.50

trxdind L4 l=1000 w1=10 w2=10

trxline T110 tech=3 w=10 l=82

trxcorn T108 w=10

trxline T109 tech=3 w=10 l=29

trxcorn T107 w=10

trxline T84 tech=3 w=10 l=43

trxline T117 tech=3 w=10 l=45

trxcap C11 c=1.85 w1=10 w2=10 oout=0

trxline T75 tech=3 w=10 l=18

trxresw R3 tech=2 w=20 r=176 w1=10 w2=10

trxline T94 tech=3 w=10 l=30

trxcorn T115 w=10

trxline T116 tech=3 w=10 l=65

trxdind L5 l=2000 w1=10 w2=10

trxline T136 tech=3 w=10 l=42.50

trxcorn T134 w=10

trxline T135 tech=3 w=10 l=24

trxtee T133 w1=10 w2=10 w3=10

trxline T131 tech=3 w=10 l=36

trxdind L7 l=1600 w1=10 w2=10

trxline T93 tech=3 w=10 l=50

trxline T132 tech=3 w=10 l=91

trxcorn T118 w=10

trxline T112 tech=3 w=10 l=5

trxcap C10 c=0.60 w1=10 w2=10 oout=0

trxline T56 tech=3 w=10 l=274

trxtee T50 w1=15 w2=15 w3=10

trxline T51 tech=3 w=15 l=58.50

trxtee T32 w1=15 w2=15 w3=10

trxline T34 tech=3 w=15 l=46

trxtee T92 w1=15 w2=15 w3=10

trxcorn T152 w=15

trxline T28 tech=3 w=15 l=83.50

trxcorn T153 w=12

trxline T55 tech=3 w=12 l=11.50

trxtee T27 w1=12 w2=12 w3=15

trxline T57 tech=3 w=12 l=50

trxcap C3 c=14 w1=10 w2=12 oout=0

trxline T61 tech=3 w=10 l=54

trxtee T44 w1=10 w2=10 w3=10

trxline T59 tech=3 w=10 l=20

trxcap C4 c=0.85 w1=10 w2=10 oout=0

trxline T58 tech=3 w=10 l=30

trxvia4 V4

trxcorn T102 w=20

trxline T104 tech=3 w=20

trxline T16 tech=3 w=12 l=129.50

MRIND L3 N=4.50 L1=350 L2=352 W=12 S=12

W2=24

MSUB=MSUB1

trxline T26 tech=3 w=24 l=23

trxline T15 tech=1 w=24 l=110

trxline T29 tech=3 w=24

trxline T144 tech=3 w=10 l=10.50

trxcorn T146 w=10

trxline T145 tech=3 w=10 l=59

trxdind L8 l=2000 w1=10 w2=10

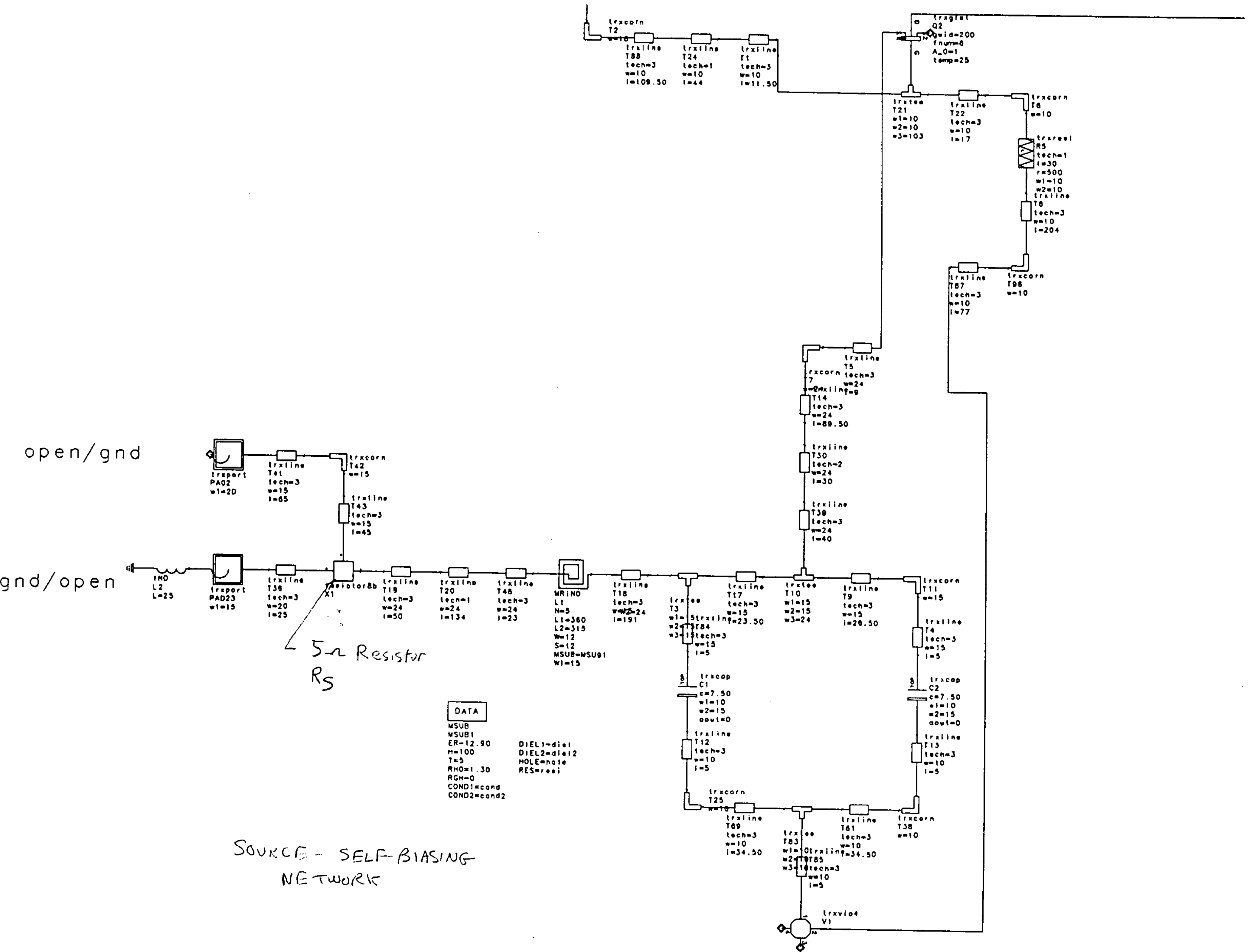
trxline T139 tech=3 w=10 l=29

trxline T142 tech=3 w=10 l=101.50

trxcorn T138 w=10

trxcorn T6 w=10

trxresl R5 tech=1 l=30 r=500 w1=10 w2=10

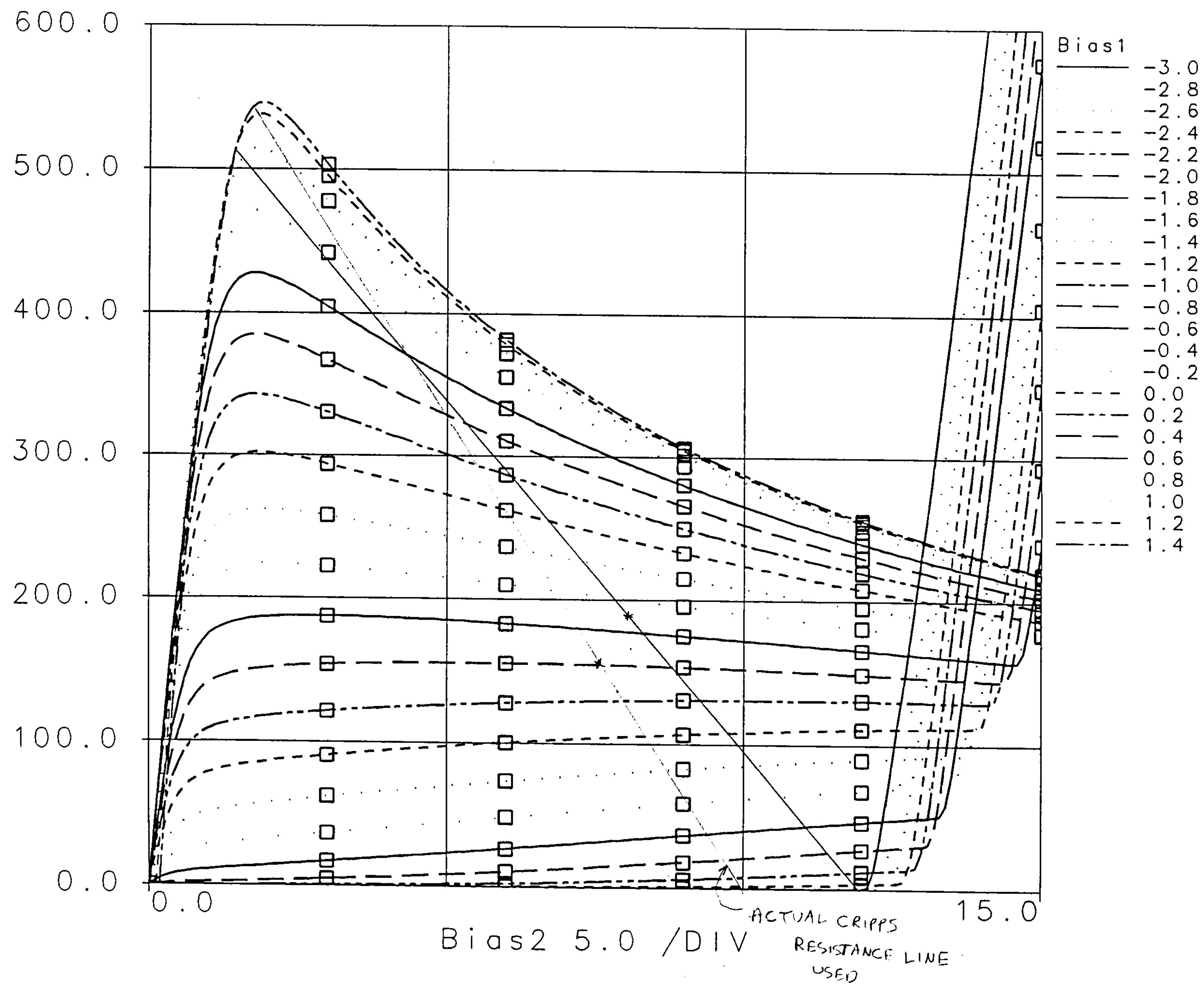


open/gnd
gnd/open
5Ω Resistor
R_S
DATA
MSUB
MSUB1
ER=12.90
H=100
T=5
RHO=1.30
RGH=0
COND1=cond
COND2=cond2
DIEL1=diel
DIEL2=diel2
HOLE=hole
RES=resi
SOURCE - SELF-BIASING
NETWORK

DC Analysis

The FET bias check and Cripps load line are shown on the following page. Since the drain bias current, I_D, may be close to 200 mA, it was necessary to use lines that were 12 μm wide or more for the bias circuit. This involved using MRIND inductor rather than the standard TRQ inductor with 10 μm lines which can handle only ~180 mA safely. This implementation can be seen in the layout diagram.

IDC1
pgfet2
IDC
mA



The Test Plan

No V_{GG} bias voltage is needed. The circuit is self-biasing. However if necessary for troubleshooting purposes a V_{GG} bias voltage may be applied as described below.

Testing:
Ground MMIC chip. Apply a V_{DD} of +8.0 V to PAD 1. Connect output to PAD 2 and input to PAD 3. Apply input signal at frequency 4.660 GHz. Measure test parameters listed in table on next page. Vary frequency over the operating range of 4.635 GHz to 4.685 GHz. V_{DD} may be varied slightly (~±1V) in order to observe the results.

Checking V_S and I_D:
A high-impedance voltage probe is recommended. Apply probe to PAD 5. This will give a direct reading of V_{source}. (Note: since the FET gate is tied to ground, V_{GS} is the negative of the voltage reading.) Drain bias current I_D is derived by dividing the voltage reading by 5 Ω: $I_D = V_{PAD5} \div 5\Omega$.

Applying V_{GG}:
If the amplifier does not function optimally, V_{GG} may be applied to PAD 4. Due to the presence of stability and isolating resistors, a very small current will be drawn and a 5-to-1 voltage division will take place. Hence to get the actual voltage applied: $V_{GG,\ applied,\ actual} = V_{PAD4,\ applied} \div 5$. This applied voltage will be **in addition to the self-biasing gate voltage** from the 5Ω source resistor. If a positive voltage is to be applied to PAD 4, V_{GG}, it is highly recommended to monitor I_D as described above to be sure that it stays below 200 mA. An I_D bias current exceeding 215 mA will cause burnout of the biasing lines on the chip. Grounding PAD 5 to override the self bias is not recommended. However if this does become necessary, the following procedure is given. Also when applying a V_{GG}, the input must be isolated from DC.

Overriding the self bias:
Be sure to follow these steps to avoid burnout of chip lines. Remove drain voltage from PAD 1. Apply at least –5.0 V to PAD 4 to ensure proper cutoff of the FET.. Apply V_{DD} to PAD 1. If possible monitor I_D externally. Do not apply a voltage more positive than –2.0 V to PAD 4, as this will cause a bias current exceeding 215 mA on the bias lines.

22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS
AMPAD

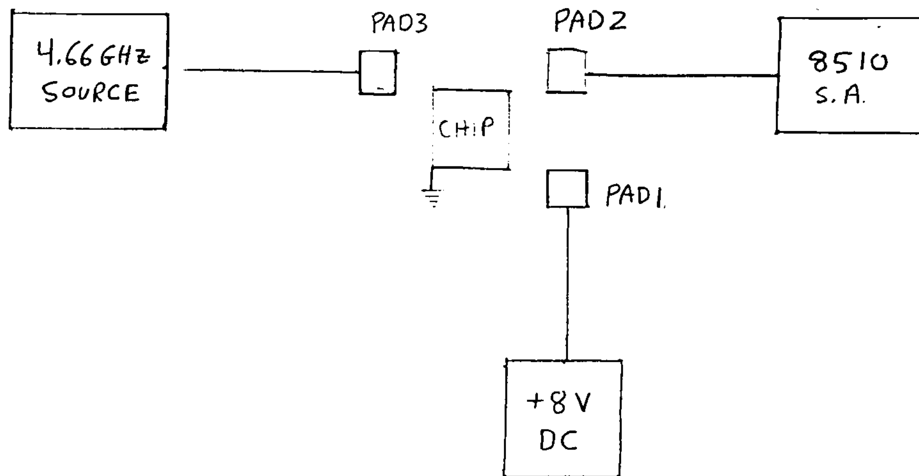
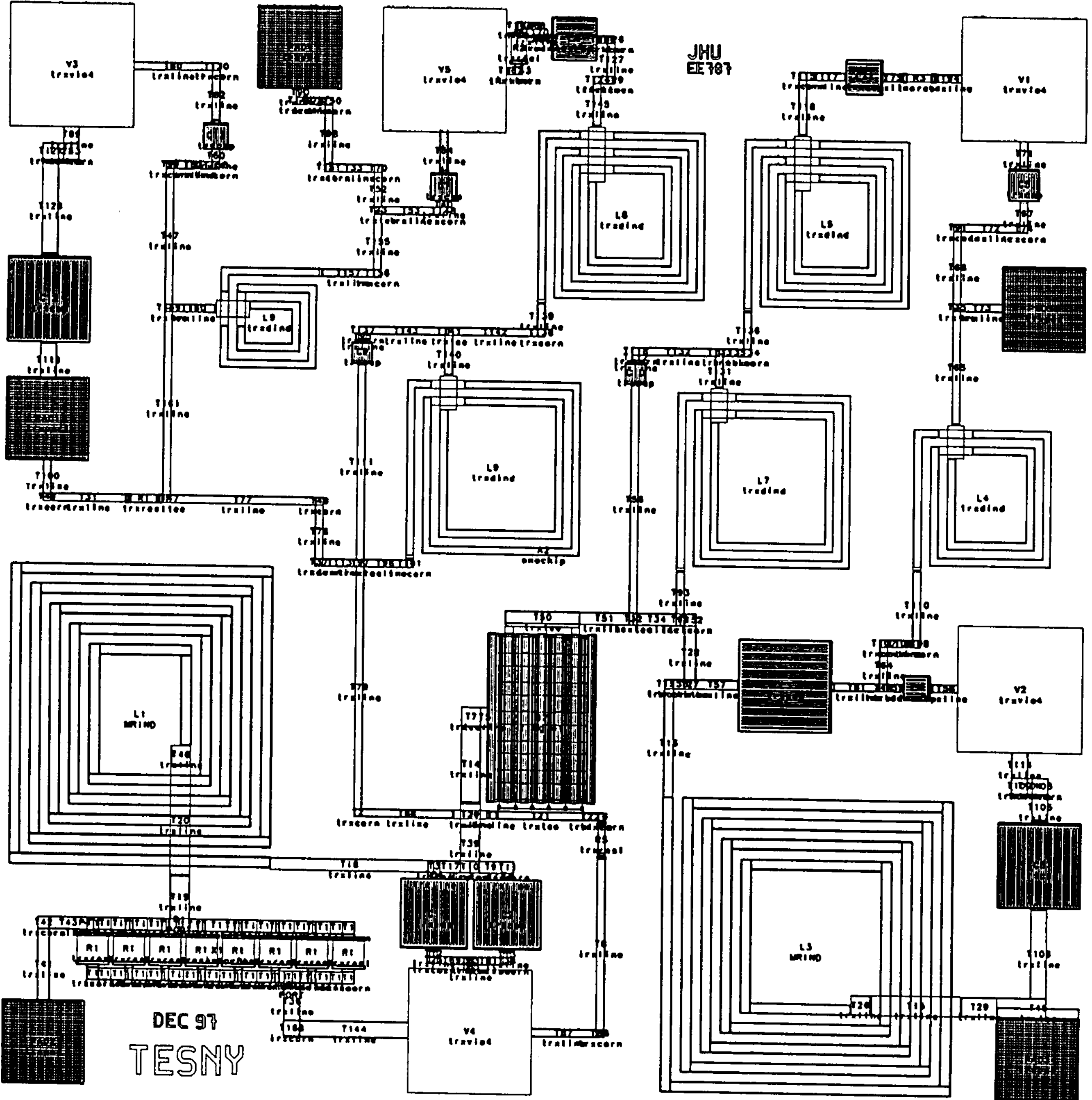


FIGURE 3. TEST EQUIPMENT HOOK UP.


INPUT
PAD 3
JHU
EE787
PAD 2
OUTPUT
PAD 4
(VGG,
IF NEEDED)
PAD 5
Vc, ID
CHECK
DEC 97
TESNY
PAD 1
VDD
CIRCUIT LAYOUT

LABORATORY TEST RESULTS
C BAND POWER AMPLIFIER

Date tested:______________

	Simulated	Measured
Gain	12.1 dB	________
Bandwidth (3 dB)	1.32 GHz	________
	3.70 – 5.02 GHz	________
Gain ripple at operating bandwidth (4.635 – 4.685 GHz)	0.14 dB	________
Power at 1dB compression point (@ 4.66 GHz)	24.2 dBm	________
Efficiency (@ 4.66 GHz)	18.37 %	________
VSWR, input (@ 4.66 GHz)	1.03	________
VSWR, output (@ 4.66 GHz)	1.39	________
V_{DD} (drain bias)	+8.0 V	________
V_{GG} (gate bias, after ÷5 correction)	0.0 V	________
I_D (drain bias current)	153.13mA	________
Other	________	________
Other	________	________

Explanation for discrepancies:

Conclusions and Recommendations

A MMIC C-band power amplifier was designed to meet given specifications. The most difficult problem to solve in this effort was probably overcoming stability problems while preserving gain and output power. Also it is difficult to optimize for output power, gain, VSWR, and efficiency at the same time. It seems that only one thing can be fully optimized at the expense of the others. It would be beneficial to assign priorities to the different requirements as to which is more important to optimize.

Bandwidth was no problem whatsoever since this was a very narrow-band device. Layout was, of course, what was the most time-consuming part of the effort. I think this can be aided greatly by better circuit planning, i.e., schematic planning as well as layout planning.

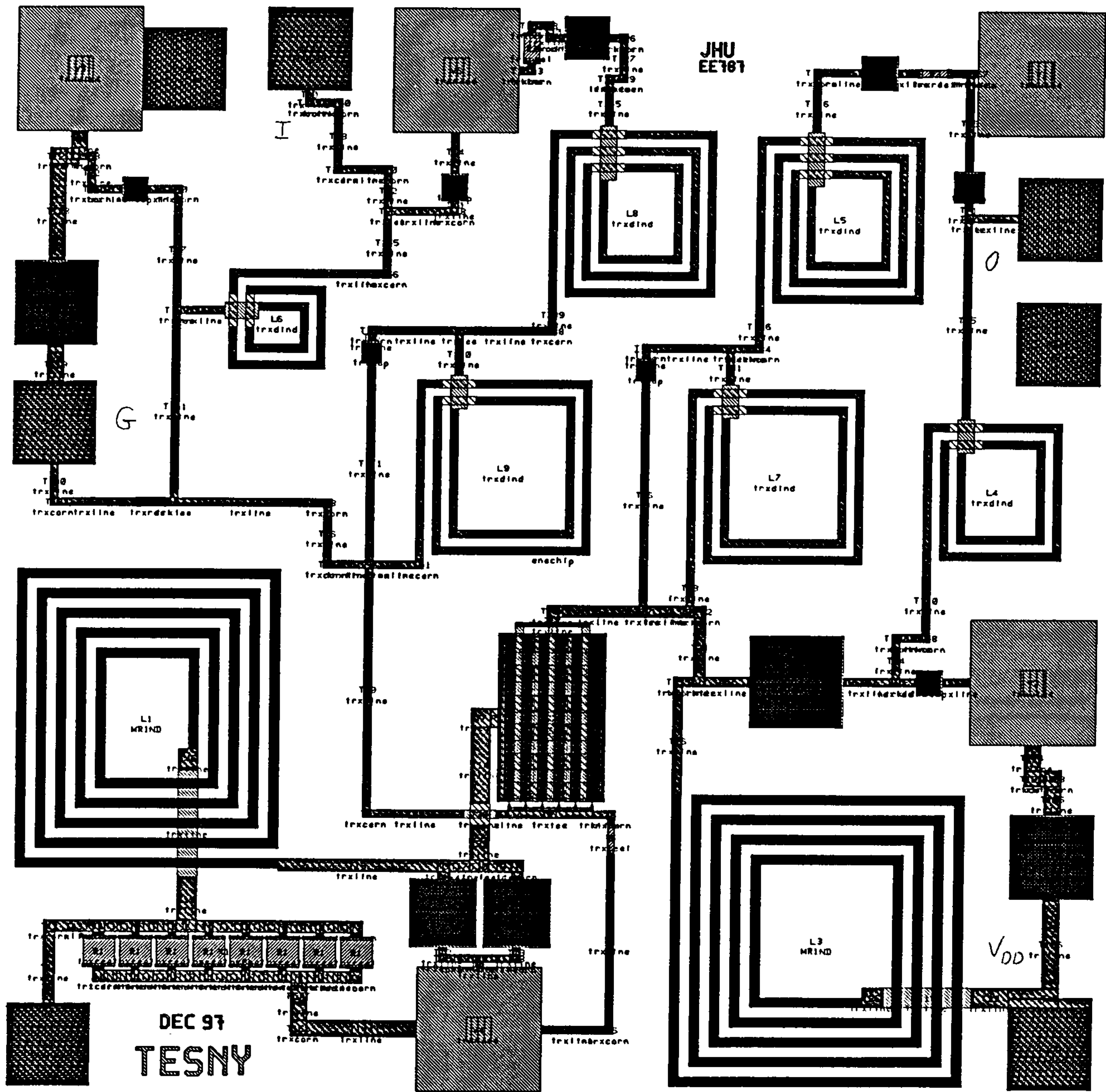
Also perhaps a 2-stage design would have given better performance. This may have reduced the number of stability networks needed, but it would have added complexity to the layout.

ADDENDUM 8 DEC 97

SLIGHT REROUTING OF THE OUTPUT MATCHING AND INPUT MATCHING NETWORKS HAD TO BE PERFORMED AT THE LAST MINUTE. THE FINAL LAYOUT IS SHOWN ON THE FOLLOWING PAGE. THIS MAY AFFECT THE INPUT AND OUTPUT MATCHES SLIGHTLY FOR THE CHIP TESTING.

ALSO FURTHER TESTING HAS SHOWN THAT GROUNDING PAD 5 WILL NOT CREATE AN UNSTABLE CIRCUIT BUT WILL IN FACT PRODUCE VERY GOOD RESULTS AS LONG AS THE PROCEDURE IS FOLLOWED PROPERLY AND SUFFICIENTLY NEGATIVE VOLTAGE (−4 TO −5 V) IS APPLIED TO V_{GG} PAD 4.

AMPAD 22-141 50 SHEETS 22-142 100 SHEETS 22-144 200 SHEETS



FINAL LAYOUT

1.6 GHz VCO Design Using the TriQuint TRx Process

8 Dec. 1997

Patrick Dever

1. Summary

An L-band voltage controlled oscillator (VCO) was designed as part of the MMIC Design course at Johns Hopkins University (525.787). This year's class objective was to design a chip set for a WLAN transceiver in the 4635 - 4685 MHz NII Band. The VCO requirement was a frequency of 1645 to 1662 MHz with an output power of +5 dBm. It was implemented using two GFETs and passive components. Frequency tuning was accomplished through a diode formed by shorting two ports of one GFET. Five of the six design goals were met. The design meets the minimum requirements for frequency, power, control voltage, supply voltage, and size. However, an impedance transformer is needed to meet the output impedance requirement. This report summarizes the design philosophy, predicted performance, and provides a test plan.

2. Introduction

Circuit Description

The VCO was designed for 7 mil GaAs using the Triquint TRx process. It consists of two GFETs (depletion mode power MESFETs). The first GFET, a 6x50 um device is unstable at the desired frequency and is the primary circuit element. The second GFET, a 6x200 um device, is used as a varactor diode. The diode is created by shorting the drain and source of the FET. The drain/source becomes the cathode and the gate serves as the anode.

The varactor is used in a series L-C circuit on the gate of the 6x50 GFET. An additional fixed capacitor in parallel with the varactor provides more capacitance to the series resonant circuit. This is explained in more detail in the tradeoffs section. Another capacitor provides a feedback path between the drain and the gate. The control voltage (Vtune) is supplied via a 5 kΩ resistor and isolated is from the 6x50 GFET via a 10 pF blocking capacitor.

Biasing is achieved through a single +5 V supply using gate, drain, and source resistors. The drain and source resistors were implemented using the NiCr layer (50 Ω/). Since the gate resistor is large (5kΩ), the G- layer, with a sheet resistivity of 600 Ω/ , was used.

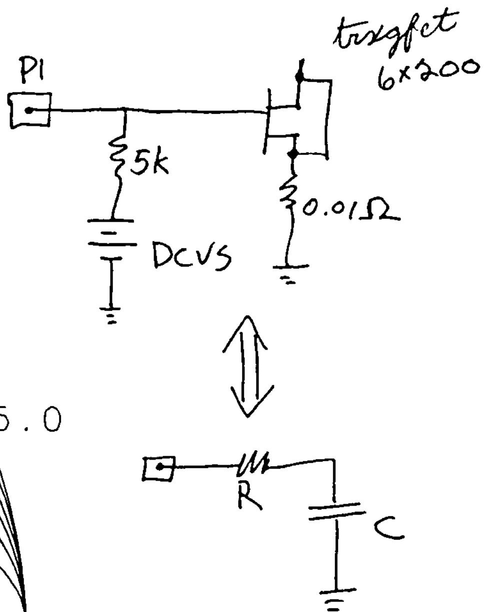
Design Philosophy

A small signal design approach was used for this oscillator. The advantage of the small signal approach is that most simulations can be done using a linear test bench and the small signal s-parameters for the FET. However, a non-linear model is needed to properly model the junction capacitance of the diode. This is not a problem since a non-linear device can be simulated in a linear test bench if it is biased properly. For simplicity, this was done for both the diode and the FET. This eliminates the need for the large signal s-parameter test bench.

The object of an oscillator is to create a predictable instability. The stability circles of the 6x50 GFET and the stability factor μ were examined. The intent was to design a resonant circuit on the gate of the device such that S11 of the device is in the unstable region. In this situation the drain will present a negative resistance to the load.

Most of the difficulty in this design involved the diode model. An accurate model of the diode capacitance versus voltage is necessary to design the resonant circuit. Several methods were tried but the simplest involved shorting the drain to the source, connecting it to ground using a small resistance, and providing bias through a large resistor. This circuit, shown in figure 1, can be simulated in a linear test bench. A second circuit, a series R-C, was then tuned to match S11 of the diode on a Smith Chart. In this way, the range of capacitance was accurately measured for the tuning range of 0 to -5 V.

S11
FET_diode_lin
S[1,1]



Frequency 1.655 to 1.655 GHz

FIGURE 1

S11 of 6x200 gfet used as a diode for gate bias of 0 to -2.4 V (step = 0.2)
Pat Dever - 1 Dec. 1997

In the simulations, TRx circuit elements and ideal interconnects were used while developing the design architecture. Since the parasitic elements are already included, little tuning is required when the real interconnects are added during layout.

A helpful method for synchronizing the layout and schematic was also learned. From the "ideal" schematic, place the last circuit element in the layout window and synchronize from the layout window. Add components one by one always synchronizing from the last element. Then re-simulate to verify performance. It helps to disconnect the real and ideal elements before synchronizing to prevent the software from creating a cluttered schematic. Repeat this procedure until all components and interconnects have been added to the layout.

Trade-offs

The first trade off involved the L-C resonant circuit. The small diode capacitance required a large series inductor to move the impedance into the unstable region of the Smith Chart. To minimize the size of the inductor, the diode was constructed from the largest FET allowed (6x200). The larger area has more capacitance. However, more capacitance was needed. This was accomplished by adding a fixed capacitor in parallel with the varactor. Its value is a compromise between minimum inductance and tuning range. If the fixed capacitor was too small, a large inductor would still be needed. If the fixed capacitor was too large, the changing diode capacitance would have a negligible affect on the resonant frequency.

The second trade off involved the feedback capacitor. The series L-C circuit on the gate did provide the desired oscillation around 1.6 GHz but it also supported an oscillation at 8 GHz. The capacitor between gate and drain helped stabilize the circuit. There are no unwanted oscillations through 10 GHz. (See figure 3.)

The third tradeoff required the 6x50 GFET. The advantage of the 6x50 GFET is that the Cripps resistance required for maximum power is 50 Ω. Thus the 6x50 GFET was used although it may have been easier to design a resonant circuit for a DFET or another size GFET.

3. Modeled Performance

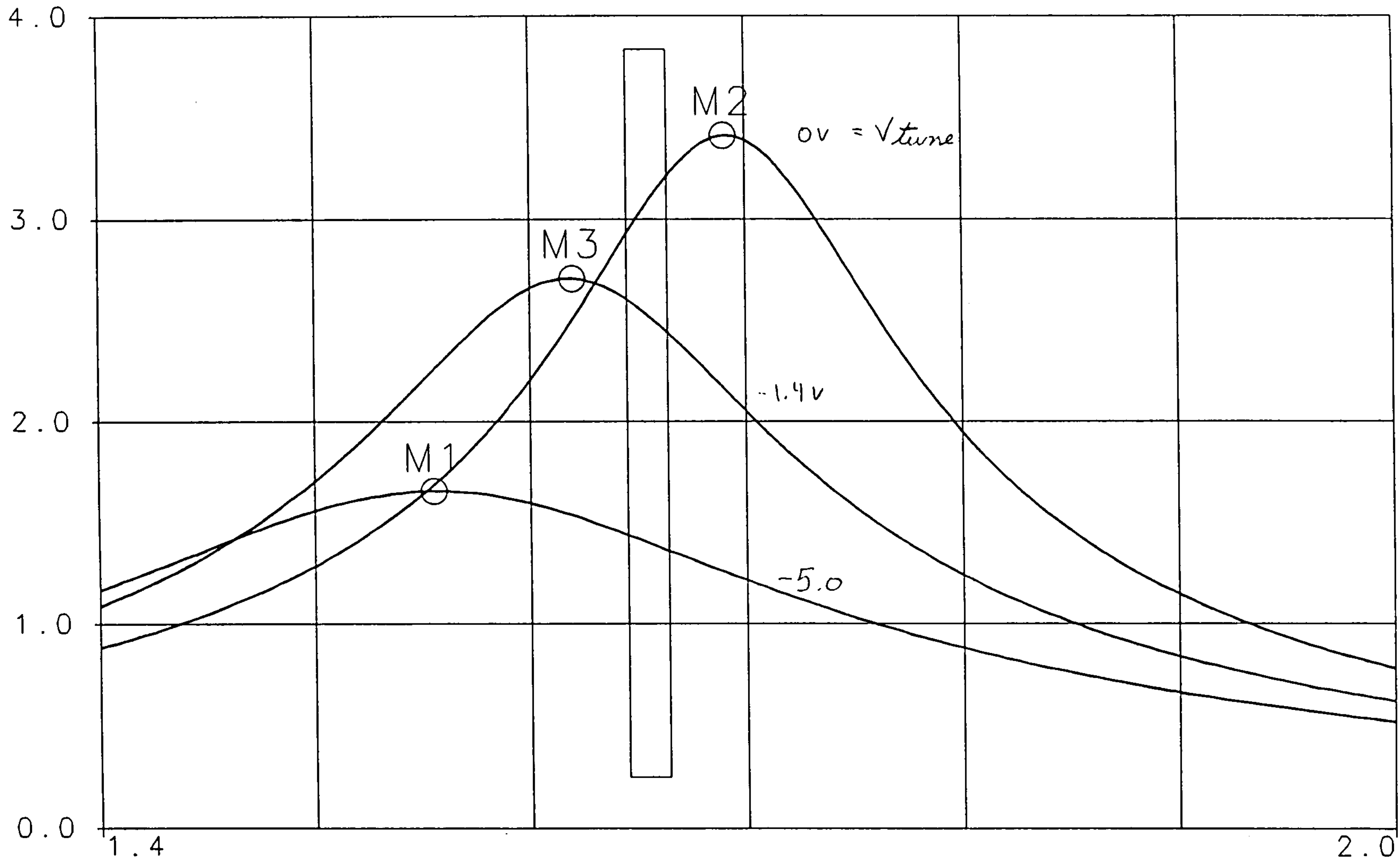
All circuits were simulated using HP's Libra software. The following specification compliance matrix summarizes the requirements, design goals, and predicted performance.

Parameter	Specification	Design Goal	Predicted Performance
Frequency	1645 - 1662 MHz	1645 - 1662 MHz	1555 - 1690 MHz
Power Out	> +5 dBm	+10 dBm	+13 dBm predicted from load line analysis.
Control Voltage	0 to -5 V	0 to -5 V	0 to -5 V
Supply Voltage	+/- 5V	+5V	+5V
Output Impedance	50 ohms	50 ohms	Negative Resistance (No on chip impedance transformer.)
Size	60 x 60 mil Anachip	60 x 60 mil Anachip	60 x 60 mil Anachip

The primary requirement of the VCO is the proper output frequency. Figure 2 compares the simulated VCO response. The minimum frequency range as marked by a box. As shown by markers 1 & 2, the predicted tuning range is 1555 to 1690 GHz since oscillations may be supported when the magnitude of S11 is greater than one. However, the useful tuning range may be less since $|S11| \cong 3$ is preferred to guarantee an oscillation. For this reason, the useful tuning range (markers 2 & 3) is probably 1620 to 1690 MHz which still meets the required frequency range.

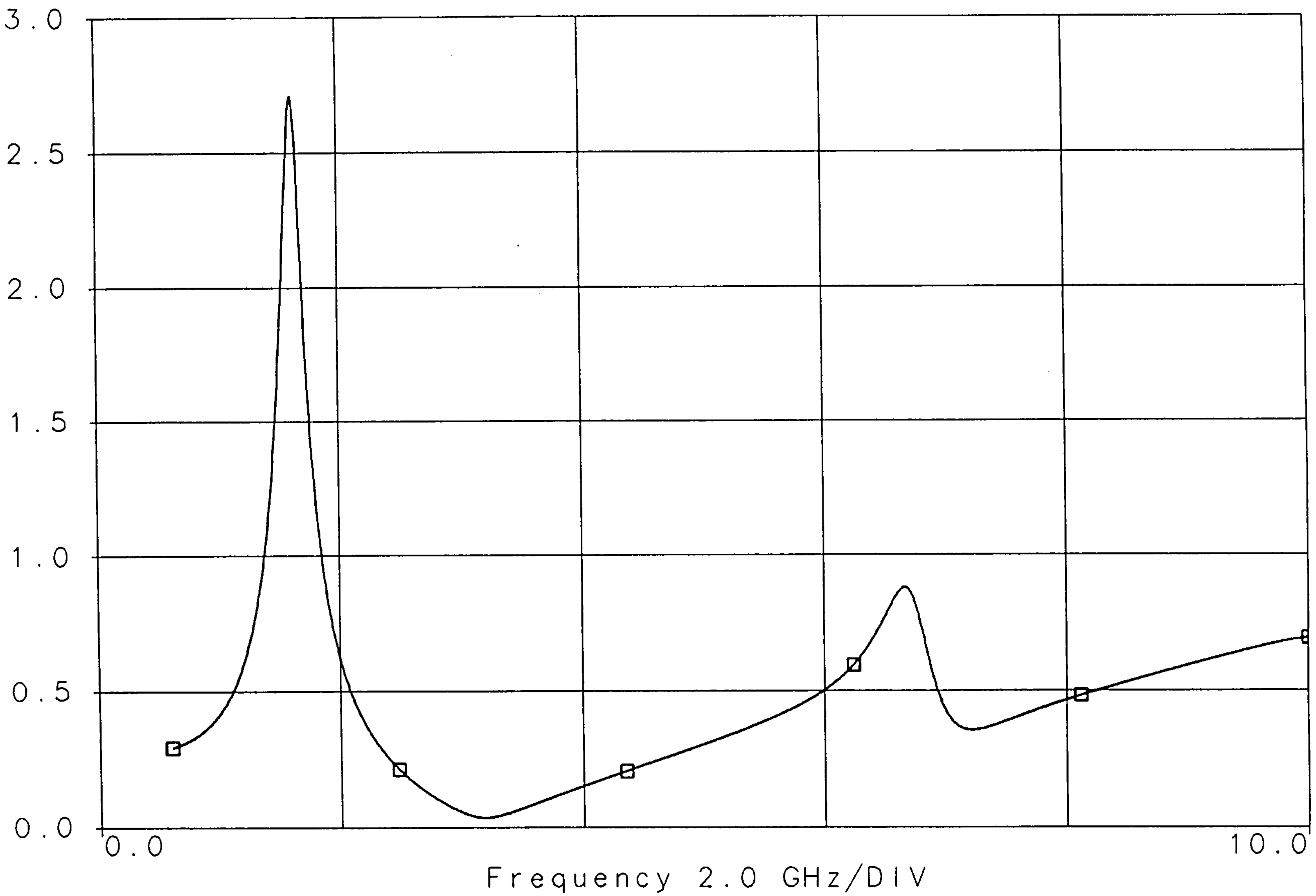
A wide band simulation was also performed to verify that the VCO will oscillate only at the desired frequency. Figure 3 shows that the design has no unwanted oscillations through 10 GHz while figure 4 verifies that the input impedance has a negative real part. Remember that a negative resistance is a necessary condition for oscillation. Finally, a layout identifying the major circuit elements is shown in figure 5.

The output power of +13 dBm was predicted from a load line analysis for the 3V, 50 mA bias of the FET. The output impedance is a negative resistance. Although this meets the requirement for oscillation it does not meet the design goal. Time allowing, an on chip impedance transformer should be added.



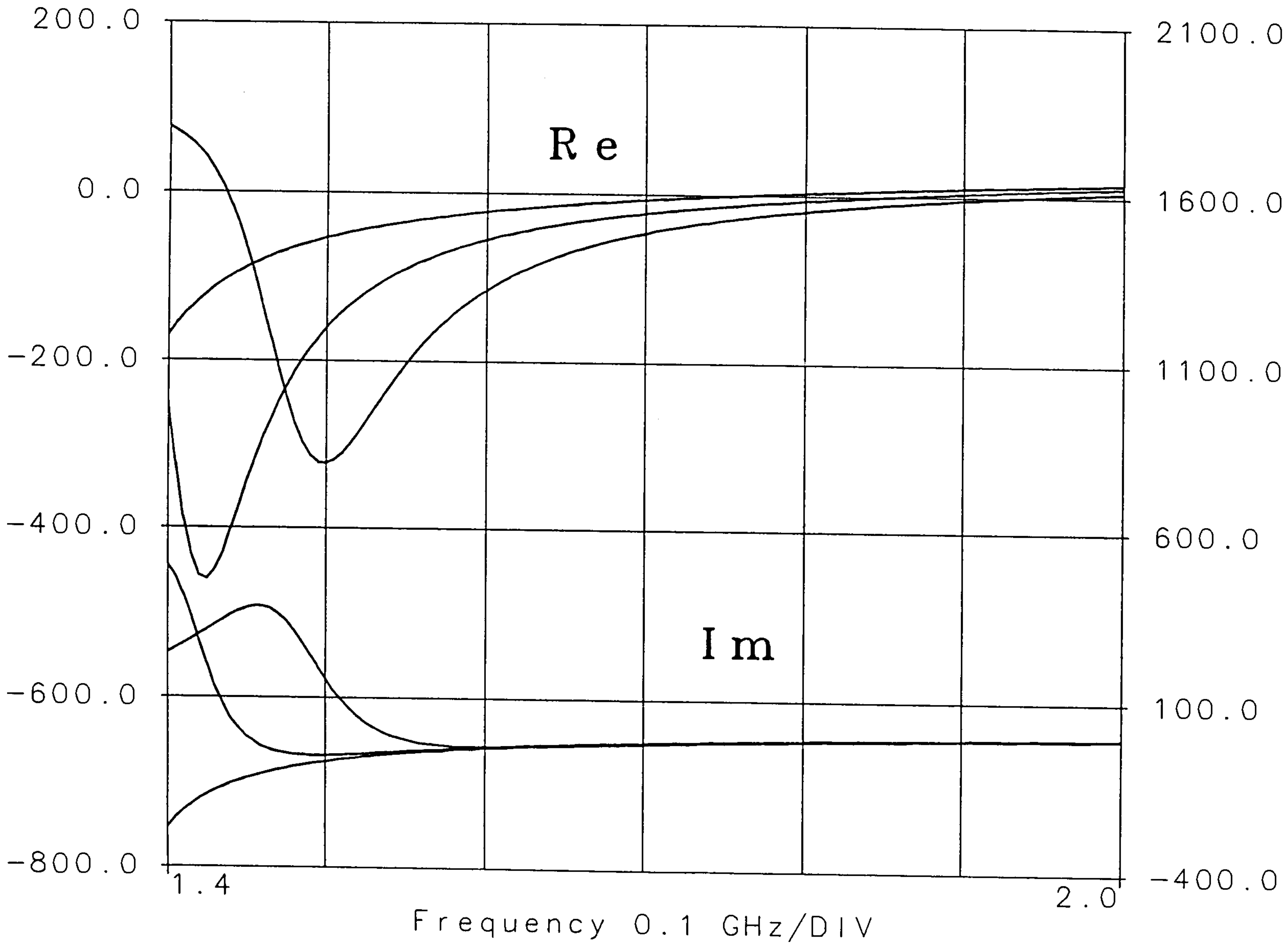
Comparison of VCO tuning range to the requirements
Markers 1 & 2 denote the VCO tuning range while the box shows the requirement
M1 Frequency=1.55500000 value=1.65494456
M2 Frequency=1.69000000 value=3.41216845
M3 Frequency=1.62000000 value=2.70902171

FIGURE 2



The VCO is unstable only at the desired frequency.
There are no other instabilities through 10 GHz.
6 Dec 1997

FIGURE 3



VCO input Impedance has a negative resistance.
6 Dec 1997

FIGURE 4

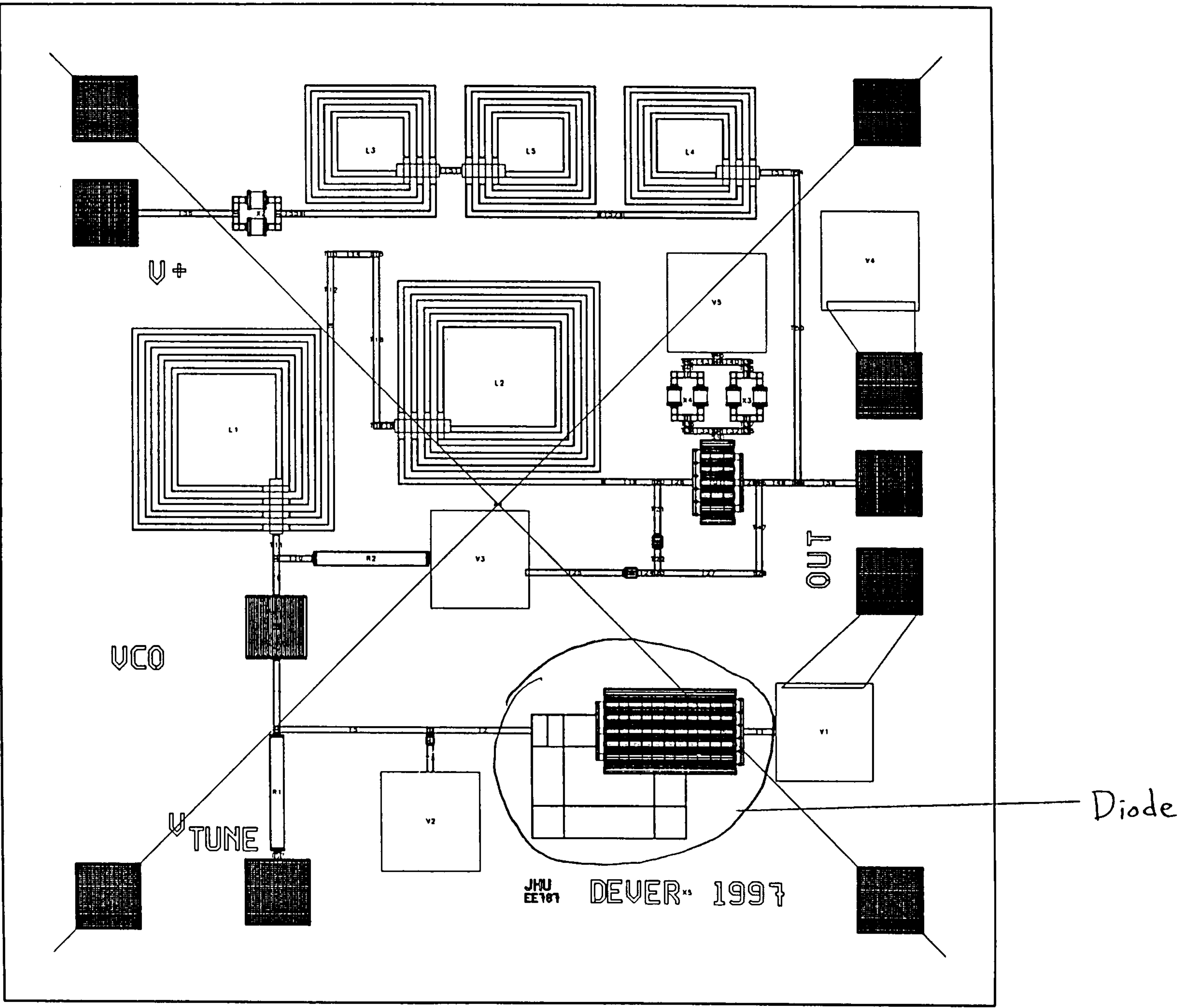


FIGURE 5

4. DC Analysis

Using a dc test bench, a dc analysis was performed on the circuit. This analysis verified the desired 3V, 50 mA bias condition on the 6x50 FET.

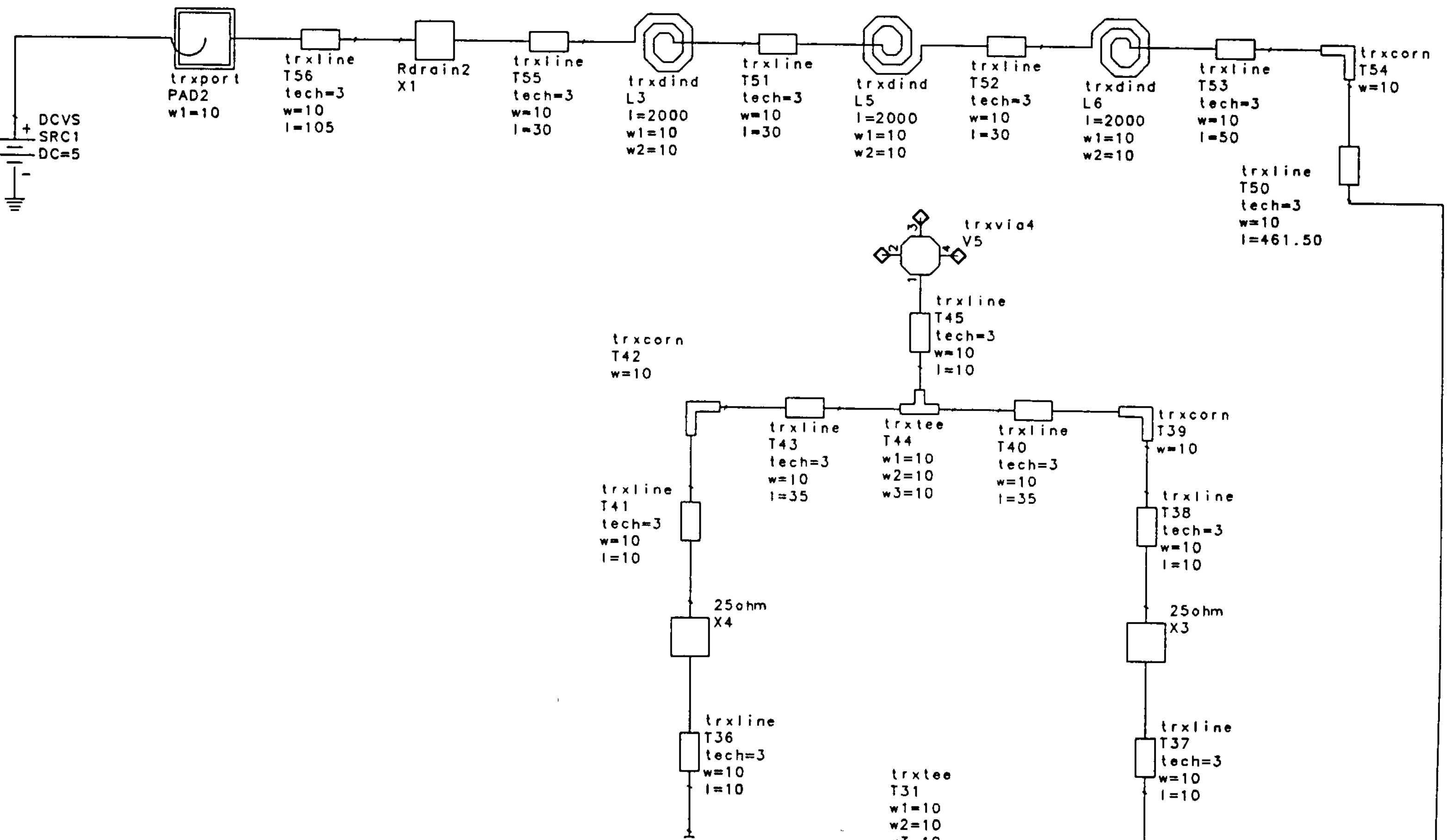
	Desired Bias Point	Simulated Bias Point
VDS	3 V	2.9567
Id	50 mA	53.8889 mA
VGS	-0.6 V	-0.6603 V

The stress caused by dc current on the circuit elements is examined in the table below. It verifies that all components have sufficient current carrying capacity.

Component	Comment
GFET (6x50)	6x50 GFET (3V, 50 mA) Taken from TQ library.
GFET (6x200)	6x200 is used as a varactor. Small current on gate.
TRXDIND and 10 um wide interconnect.	The 10 um wide inductors are made up of ME-1 and ME-2. The current capacity of ME-1 alone is 9 mA/um. (10 um * 9 mA/um = 90 mA capacity.) Additional capacity is added by ME-2 (18 mA/um).
NiCr Resistors	1 mA/um of width. Resistors must be a minimum of 53 um wide.
G- Resistors	0.025 mA/um of width. 5 kΩ resistors are 20 um wide. Used in the varactor and gate circuits. Small current on gate.

5.0 Schematics

Supply Voltage Section



trxvia4
V5

trxline
T45
tech=3
w=10
l=10

trxcorn
T42
w=10

trxline
T43
tech=3
w=10
l=35

trxtee
T44
w1=10
w2=10
w3=10

trxline
T40
tech=3
w=10
l=35

trxcorn
T39
w=10

trxline
T41
tech=3
w=10
l=10

trxline
T38
tech=3
w=10
l=10

25ohm
X4

25ohm
X3

trxline
T36
tech=3
w=10
l=10

trxline
T37
tech=3
w=10
l=10

trxtee
T31
w1=10
w2=10
w3=10

trxcorn
T34
w=10

trxline
T33
tech=3
w=10
l=35

trxline
T32
tech=3
w=10
l=35

trxcorn
T35
w=10

trxline
T14
tech=3
w=10
l=60

trxcorn
T15
w=10

trxcorn
T13
w=10

trxline
T12
tech=3
w=10
l=100

trxline
T16
tech=3
w=10
l=250

trxline
T30
tech=3
w=10
l=10

TP
Vs

trxtee
T20
w1=10
w2=10
w3=10

TP
Vg

trxdind
L4
l=6000
w1=10
w2=10

TP
Vd

S1

trxtee
T46
w1=10
w2=10
w3=10

trxcorn
T17
w=10

trxline
T18
tech=3
w=10
l=20

trxdind
L1
l=6000
w1=10
w2=10

trxline
T19
tech=3
w=10
l=75

trxline
T26
tech=3
w=10
l=50

S2

trxgfet
Q1
gwid=50
fnum=6
A_D=1
temp=25

trxline
T29
tech=3
w=10
l=20

trxline
T48
tech=3
w=10
l=50

trxtee
T49
w1=10
w2=10
w3=10

trxline
T58
tech=3
w=10
l=85

trxport
PAD3
w1=10

PORT
P1
port=1

trxline
T11
tech=3
w=10
l=30

trxline
T10
tech=3
w=10
l=50

trxline
T21
tech=3
w=10
l=75

trxtee
T9
w1=10
w2=10
w3=10

trxres
R4
tech=3
w=20
r=5000
w1=10
w2=10

trxvia4
V4

trxcap
C1
c=0.25
w1=10
w2=10
aout=0

AMMETER
AMM1

trxline
T47
tech=3
w=10
l=130

trxline
T8
tech=3
w=10
l=50

trxline
T22
tech=3
w=10
l=31

trxcap
C4
c=10
w1=10
w2=10
aout=0

AMMETER
AMM3

trxline
T25
tech=3
w=10
l=150

trxcap
C2
c=0.20
w1=10
w2=10
aout=0

trxline
T24
tech=3
w=10
l=25

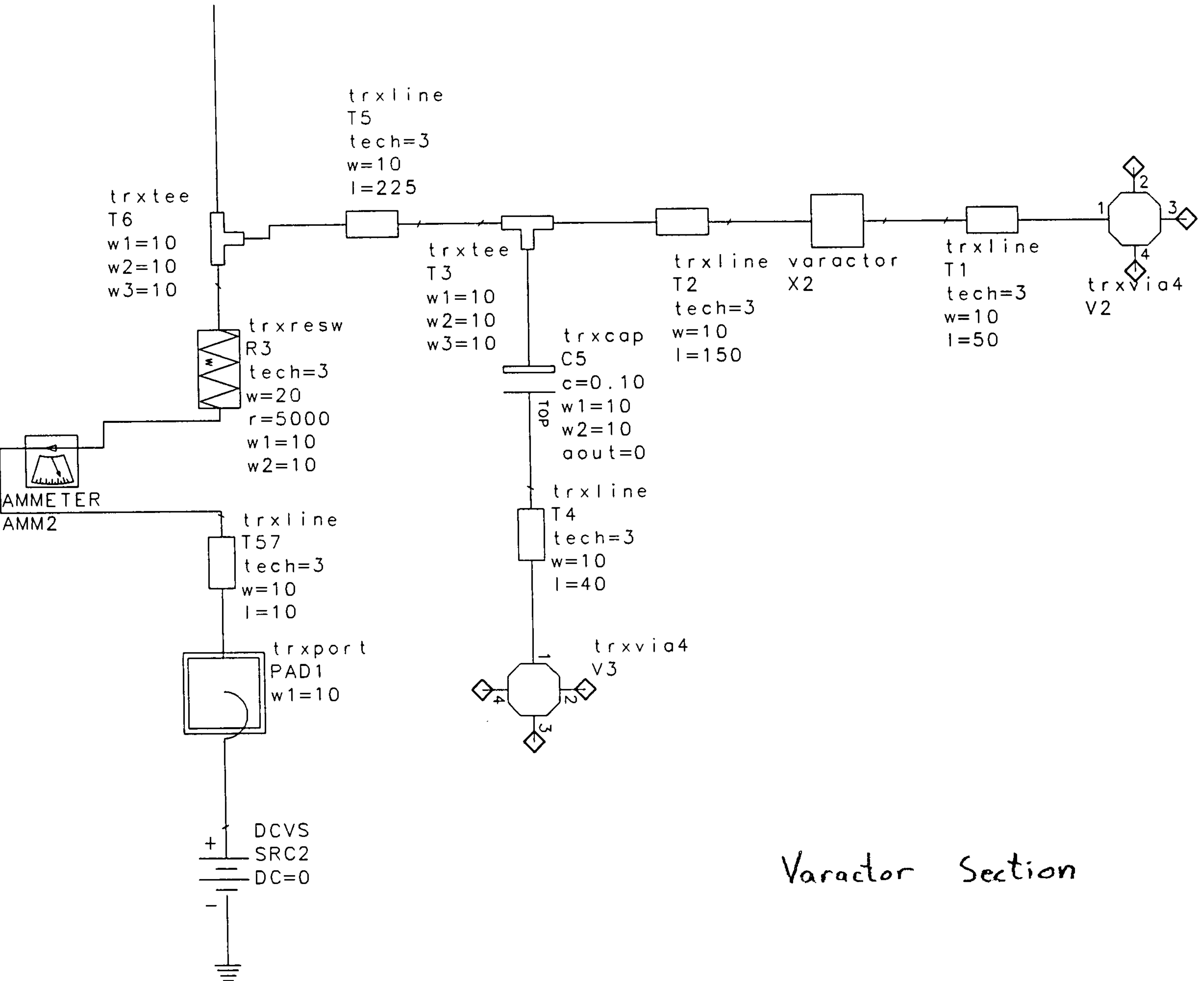
trxtee
T23
w1=10
w2=10
w3=10

trxline
T27
tech=3
w=10
l=144.50

trxcorn
T28
w=10

Main Circuit

trxline
T7
tech=3
w=10
l=100


trxtee
T6
w1=10
w2=10
w3=10
trxline
T5
tech=3
w=10
l=225
trxtee
T3
w1=10
w2=10
w3=10
trxline
T2
tech=3
w=10
l=150
varactor
X2
trxline
T1
tech=3
w=10
l=50
trxvia4
V2
trxresw
R3
tech=3
w=20
r=5000
w1=10
w2=10
trxcap
C5
c=0.10
w1=10
w2=10
aout=0
TOP
AMMETER
AMM2
trxline
T57
tech=3
w=10
l=10
trxline
T4
tech=3
w=10
l=40
trxport
PAD1
w1=10
trxvia4
V3
DCVS
SRC2
DC=0
Varactor Section

6. Test Plan

The test plan consists of the following tests:

1. DC Current
2. Unwanted Oscillations
3. Tuning Frequency Range and Output Power

All tests are to be performed as described below. A VCO test data sheet is provided to collect the data.

Required Test Equipment

(1) Spectrum Analyzer (HP8563 or equivalent)
(1) Network Analyzer (HP8510 or equivalent)
(1) Multimeter
(2) Power Supply

A. DC Current

1. Verify all connections as shown in figure 6.
2. Apply +5 V to the V+ port.
3. Measure dc current.

B. Unwanted Oscillations

1. Connect the RF output of the VCO to a spectrum analyzer as shown in figure 6.
2. Apply +5 V to the V+ port and 0 V to the Vtune port.
3. Verify that no oscillations exist in the range 0 to 1.5 GHz and 2 to 10 GHz.

C. Tuning Frequency Range and Output Power

1. Connect the RF output of the VCO to a spectrum analyzer as shown in figure 6.
2. Apply +5 V to the V+ port
3. Measure the oscillation frequency and amplitude for 0 to -5 volts as shown on the test data sheet. The step size may be reduced as necessary to verify the tuning frequency range of 1645 to 1662 MHz.

TEST SETUP

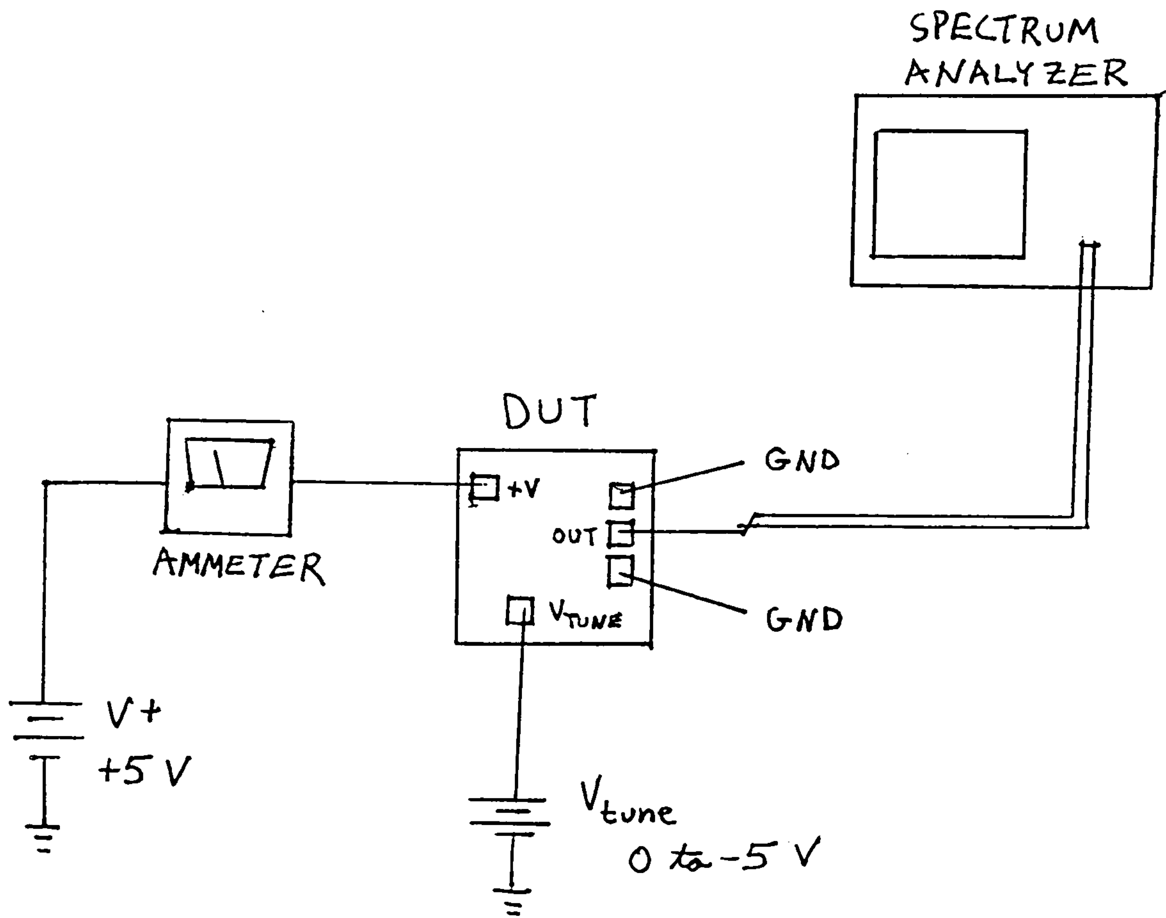


FIGURE 6

PBO

VCO Test Data Sheet

Date: _______________

A. DC Current

50 mA nom.

Current (mA) [ ]

B. Unwanted Oscillations

No oscillations 0 - 1.5 GHz & 2 - 10 GHz

Oscillations? (y/n) [ ]

C. Tuning Frequency and Output Power

1645 to 1662 MHz min.

+5 dBm min.

Vtune (V)	Frequency (MHz)	Power (dBm)
0		
-0.2		
-0.4		
-0.6		
-0.8		
-1.0		
-1.2		
-1.4		
-1.6		
-2.0		
-3.0		
-4.0		
-5.0		

7. Conclusion and Recommendations

The 1.6 GHz VCO described above successfully meets 5 of the 6 design requirements. It meets the minimum frequency range, operates from a single supply, uses a 0 to -5 V tuning voltage, and fits on the 60x60 mil Anachip. The output power is also predicted to exceed the minimum requirement. However an impedance transformer is needed to meet the output impedance requirement.

Time allowing, there are two recommendations that should be followed. First, the impedance transformer should be added to the circuit. Second, more attention could be given to simulating the actual output power rather than relying on the load line analysis.

Four Stage Distributed Amplifier Using a Distributed Biasing Technique

EE787
MMIC Design Techniques
Fall 1997

John Larner
12-8-97

Abstract:

A four stage distributed amplifier was designed using a distributed biasing technique. The amplifier was designed for implementation with the LH5 process currently under development at M/A-Com. Both linear and non-linear models were available for a 25x6 FET, so the design was based on this FET size. The goal of the design was to maximize the bandwidth of the amplifier while keeping a reasonable gain and maintaining low VSWR on the input and output. The design presented here shows an amplifier with 9dB of gain from 1GHz, to a -3dB point at 24GHz. The VSWR is less than 2:1 over the entire band and less than 1.5:1 from 10GHz to 24GHz. The amplifier is unconditionally stable.

Introduction:

A goal of this design was to maximize amplifier bandwidth by using distributed amplifier techniques. A 25x4 PHEMT linear model was available, which would have resulted in an amplifier with higher frequency operation, but a 25x6 PHEMT was chosen since both linear and non-linear models were available for that part.

Design Goals:

Bandwidth:	26GHz, -3dB bandwidth.
Gain:	At least 7dB.
VSWR:	Less than 1.5:1, both input and output.

Achieved:

Bandwidth:	1-24GHz, -3dB bandwidth.
Gain:	9dB.
VSWR:	Less than 1.5:1 from 10GHz to 24GHz. Less than 2:1 from 1GHz to 10GHz.

Design Philosophy:

Distributed amplifiers have the widest bandwidth operation of any amplifier topology. In a distributed amplifier design, isolation and gain are sacrificed to produce an amplifier with the widest bandwidth possible. A distributed amplifier is designed by connecting FETs in such a way that they form an artificial, lumped element transmission line. The idea is to combine a FET's gate and drain capacitances with inductive gate and drain lines in order to match to the desired input and output impedances, normally 50 Ohms.

The design of an ideal distributed amplifier begins with modeling the gate and drain capacitances of the FET. The needed inductance for the gate and drain lines can then be calculated by Z=sqrt(L/C), where C is either the gate or the drain capacitance. Since smaller FETs have lower gate and drain capacitances, they are capable of higher frequency operation. The gate capacitance, Cg, is usually the larger of the two and is thus the limiting factor on the high frequency operation of the device. The upper frequencies are limited because the artificial transmission line formed by Cg and the inductor form a low pass filter with a cutoff frequency f=1/(Z*pi*Cg).

Actual Design:

For the 25x6 FET the input was easily modeled as a 200fF capacitor in series with a 12 Ohm resistor (See Smith chart). A 500pH inductor would be required to form the 50 Ohm transmission line for the gate line. At the frequencies of operation desired, coiled, lumped inductors could not be used due to the fact that they became self-resonant. Instead, a length of narrow transmission line, MLIN, was used to create the needed inductance between adjacent FETs. Even a piece of transmission line would become self-resonant if it were too long. Due to the self-resonance problem and the fact that the lines were lossy as well, the inductors were far from ideal at high frequencies. The lack of ideality of the inductors meant that design techniques which assumed ideal components were of little help. Instead, Libra modeling was used to achieve a balance between transmission line inductance and loss in order to optimize the overall amplifier performance.

The output of the 25x6 FET could not be modeled very well by a simple RC circuit (see Smith chart). This made it difficult to make a meaningful choice of inductor values. Libra modeling was again used to find a combination of drain line length and width which gave acceptable performance to the overall amplifier design.

Biasing:

An initial idea was to supply all of the amplifier FETs from the drain line through the drain termination resistor. This would have resulted in a power dissipation of 50x(4x25mA)^2=0.5 Watts in the terminating resistor. Due to lack of power handling capability in the TaN resistors, this option was rejected. Another idea, due to Chuck Cook of M/A-Com, was to use one FET per stage of the amplifier as a current source. This seemed like an interesting, easy to implement solution.

It was decided to bias the FETs at Idss. Operation near Idss should result in an amplifier with high gain and was also the simplest configuration for the constant current FETs. Idss for the 25x6 FETs is 18mA according to the linear model, and 25mA according to the non-linear model. The two models were derived from different samples of FETs.

This biasing technique required that in addition to the drain capacitance of the amplifier FETs being absorbed into the output transmission line, the shorted gate and source capacitance of the constant current FETs also had to be absorbed. Since Cg of the amplifier FETs is larger than Cd, one should be able to add extra capacitance to the drain line without hurting performance.

The initial design fed each amplifier stage from a seperate bond pad. It was concluded that this might not be a practical way to bias the circuit. It was desireable to supply all of the drain current through a single bond pad. It was found that in order to supply the drain current from one bond pad and maintain adequate isolation from stage to stage, a small resistance (~8 Ohms) was required on the drain of the constant current FETs. The drain resistors were made as wide as possibe to maximize power handling. Since the current through each resistor is only Idss, the power dissipation in that resistor is approximately (8 Ohms)x(25mA)^2=5mW. The TaN resistors can carry a maximum current of 0.2mA/um. The resistors used are 180um wide, with

a maximum current of 36mA.

The maximum current density on the top conductor traces is 10mA/um with a 5um minimum trace width. Feeding each amplifier FET seperately meant that the lines feeing these devices only had to carry 25mA so that a 5um line width was adequate. On the bond pad side of the drain resistors, wider lines are used since all the current is carried through that line.

A large value resistor was added to the gate biasing line to isolate that line from the rest of the circuit. Since there is essentially no gate current, this resistor should not affect the amplifier's performance.

Bandwidth:

Bandwidth of the amplifier was tuned by looking at both S21 and VSWR at the same time. Getting good numbers for S21 while the VSWR degraded was not acceptable. The upper limit frequency of operation for the amplifier was calculated as f=1/(Z*pi*Cg)=1/((50 Ohms)*pi*200fF)=31GHz. The amplifier bandwidth was most sensitive to changes in the gate to gate and drain to drain line lengths, the gate terminating resistor, and the bias feed line. Varying the gate termination resistor affected the lower frequencies the most, and created ripple in the pass band. A termination resistor was chosen so that the amplifier had a pass band with minimal ripple down to 1GHz. The bias feed lines from the constant current biasing FETs acted as tuning stubs and had some effect on bandwidth. The upper frequency operation was limited by the low-pass effect of the artificial transmission line. Getting a flat frequency response over a wider band would have required lowering the overall gain of the amplifier. See the graphs for S21 and VSWR.

VSWR:

Obtaining a good VSWR on the input of the amplifier was relatively easy. Tuning the length of the amplifier's gate input line and the gate to gate lines between the FETs resulted in good input VSWR. The gate termination resistor should have been 50 Ohms in an ideal system, but varying the gate resistor's dimensions improved the input VSWR somewhat.

It was found during the initial simulations and verified on the final circuit that making the drain lines from the lossier base metal improved the output VSWR of the amplifier. This resulted in a slightly lower peak gain than could be achieved with the more conductive top metal, a difference of about 1dB. The length (inductance) of the gate and drain lines was critical in achieving good input and output VSWR. The length of the drain output line and the size of the drain output capacitor were also critical to achieving a good output VSWR. Concern was expressed about the large size of the output capacitor. I kept the capacitor large to get the VSWR numbers down to where I wanted them. If this does not work, a smaller on-chip capacitor could be used, or an off chip capacitor could be substituted in its place. The design is fairly insensitive to the length of the drain termination line and the size of the drain termination resistor. A larger drain termination resistor was chosen to better absorb any power reflected from an open circuit.

Stability:

The distributed amplifier design is unconditionally stable (See graph). Preliminary tests with ideal elements indicated the possibility of stability problems, but once real elements were placed, the amplifier became stable. The initial amplifier design had a seperate bond pad to feed drain current to each stage. It was decided that this was not practical. When the drain feeds were connected to each other, it affected gain and stability negatively. Resistors were added to improve the isolation from stage to stage, restoring the stability and gain flatness.

Power:

From the I-V curves of the 25x6 PHEMT (See Graph), a maximum power output for a single FET can be calculated from P=(I*V)/8 to be about 11dBm. Non-linear analysis on the pre-layout model seemed to indicate that the amplifier began to compress around 13dBm out. An attempt was made to do a Harmonic Balance test to find the compression point for the final design. Convergence problems on an amplifier with eight FETs prevented me from getting this. More time and experience with the Harmonic Balance test would be required.

Modeling:

A comparison was done between the linear and non-linear models for the completed layout. The non-linear FET model was substituted for the linear model in the schematic, and the gate voltage was tuned until the amplifier was biased at 18mA per FET, to agree with the linear model. The models are in good agreement over most of the band. A comparison of the results for S11, S21, and S22 can be seen in the graphs.

Test Plan:

To measure the frequency response and gain, the amplifier would be connected to an HP8510 through a probe station. The drain power would be supplied through a probe station pin, about +6V at 100mA maximum current would be required. The gate supply voltage would be in the range of -0.2 to 0 Volts. Since the amplifier is powered through constant current sources on chip, there should not be a problem with supplying too much drain current and destroying the chip. Proper testing procedure would be to apply negative voltage to the gate before turning on the drain supply in order to limit the initial current. The gate voltage would then be increased until a drain current of 4x(18mA)=72mA were measured. Because of the power limit of the drain resistors, the maximum current into the device should not exceed 4x(36mA)=144mA. At worst case, the chip would dissipate 6Vx144mA=0.864Watts of power. Attaching the chip to a heat sink might be required.

A power compression test could then be performed using a synthesizer as the input, and measuring the output power with a spectrum analyzer or power meter.

Conclusions:

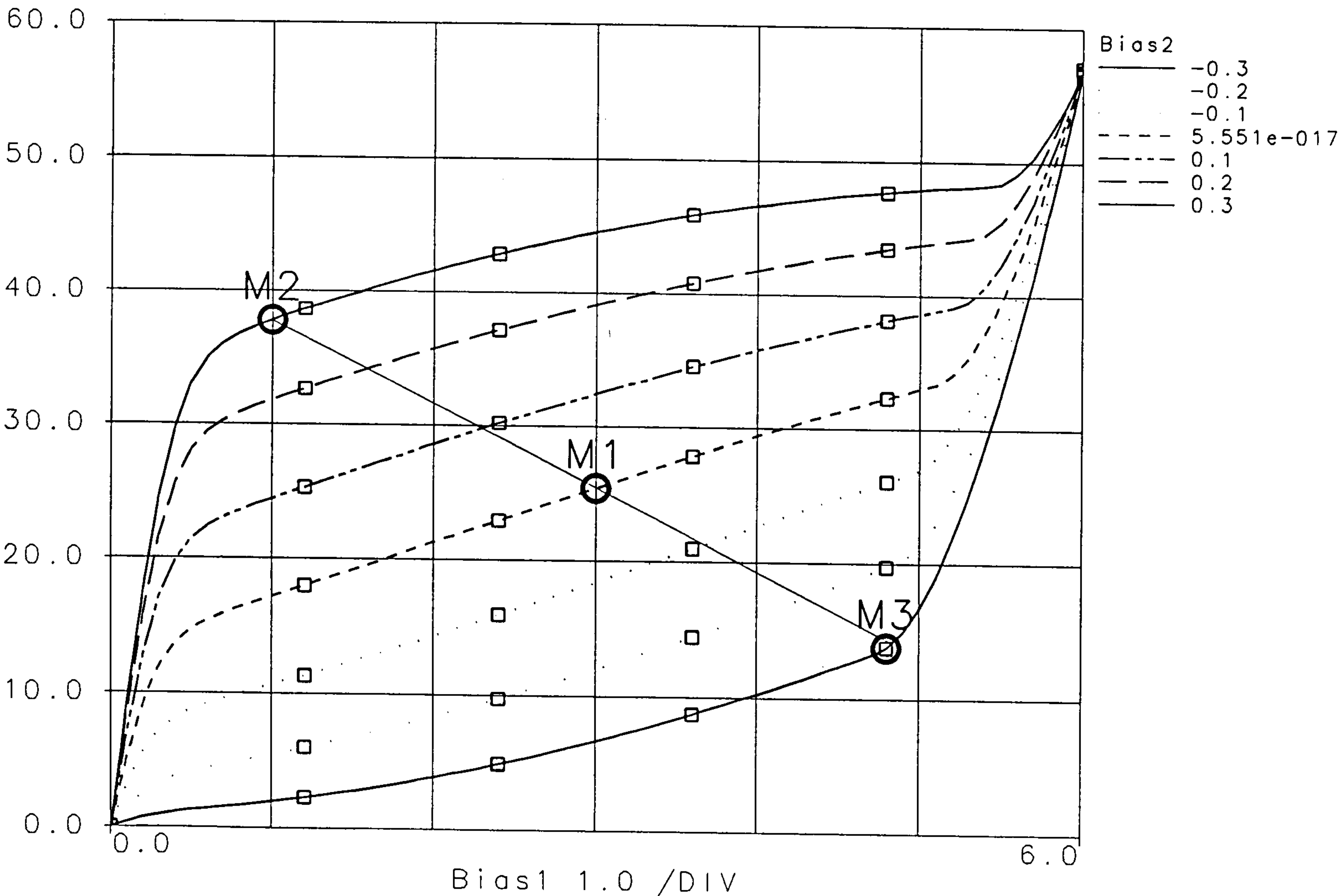
The distributed amplifier design appears to have good gain and VSWR over a wide bandwidth. The distributed biasing technique simplified the design of the amplifier. This biasing technique has the advantage of putting current stabilization directly on the chip. This should

help the amplifier's performance over temperature. It also reduces power that would be wasted by passing the drain current through the drain termination resistor; about 4x(8 Ohms)x(25mA)^2=20mW instead of (50 Ohms)x(4x25mA)^2=500mW in this case.

It may be possible to improve the amplifier further by using the more conductive top metal instead of base metal for the drain lines. The drain lines in the current design may be meandered more than they need to be, since the via keepout layer shown is really on the bottom of the chip and need not have been avoided.

25x6 PHEMT I-V Curves.

□DCbias_25x6_tb
Id
DCbias_25x6
IDC
mA



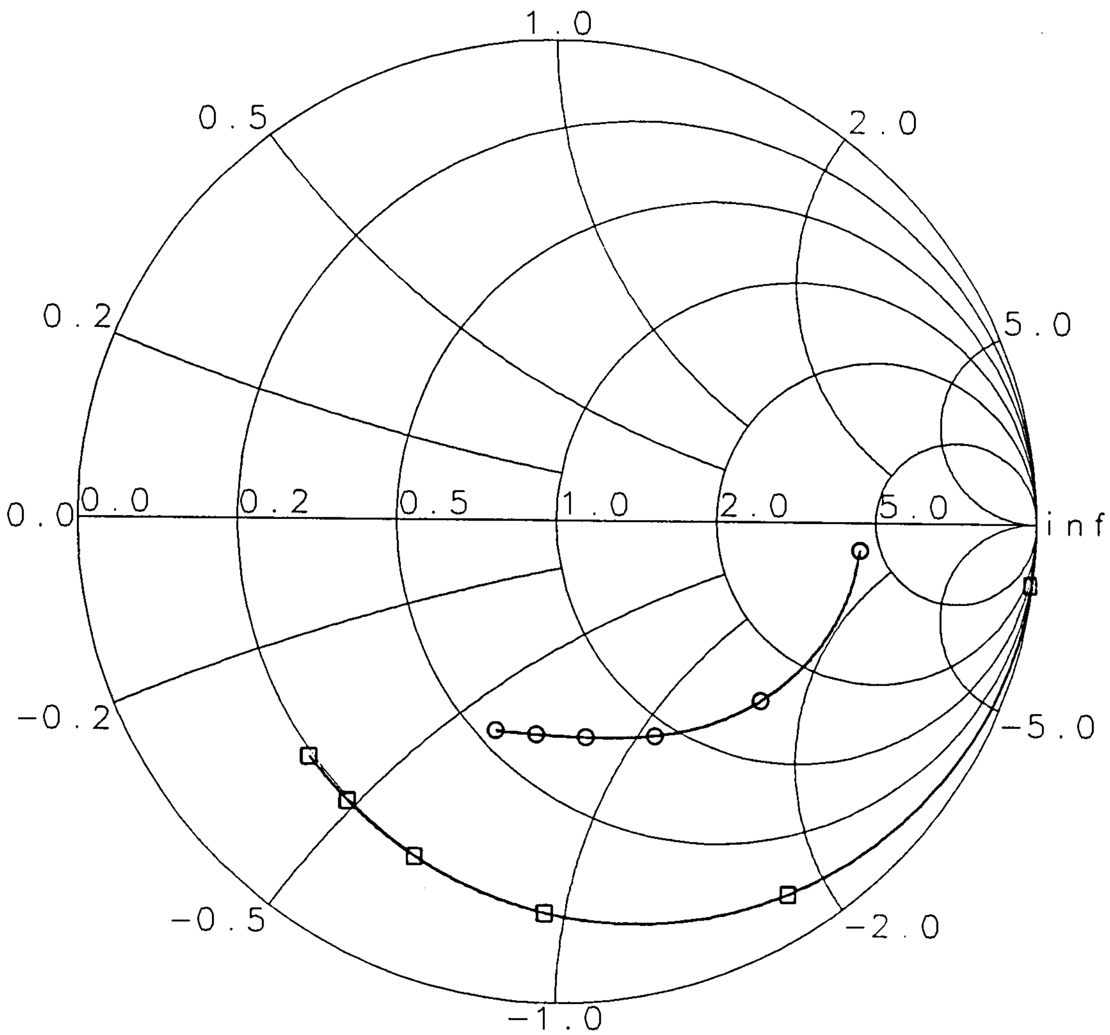
M1 Bias2=5.551e-017 Bias1=3.00000000 value=25.4364734
M2 Bias2=0.30000000 Bias1=1.00000000 value=37.8308309
M3 Bias2=-0.30000000 Bias1=4.80000000 value=13.8174459

25x6 PHEMT

Linear model, Ids=18mA, Vgs=0V.

□ ECP25x6_tb
INPUT
InputCap
S[1,1]

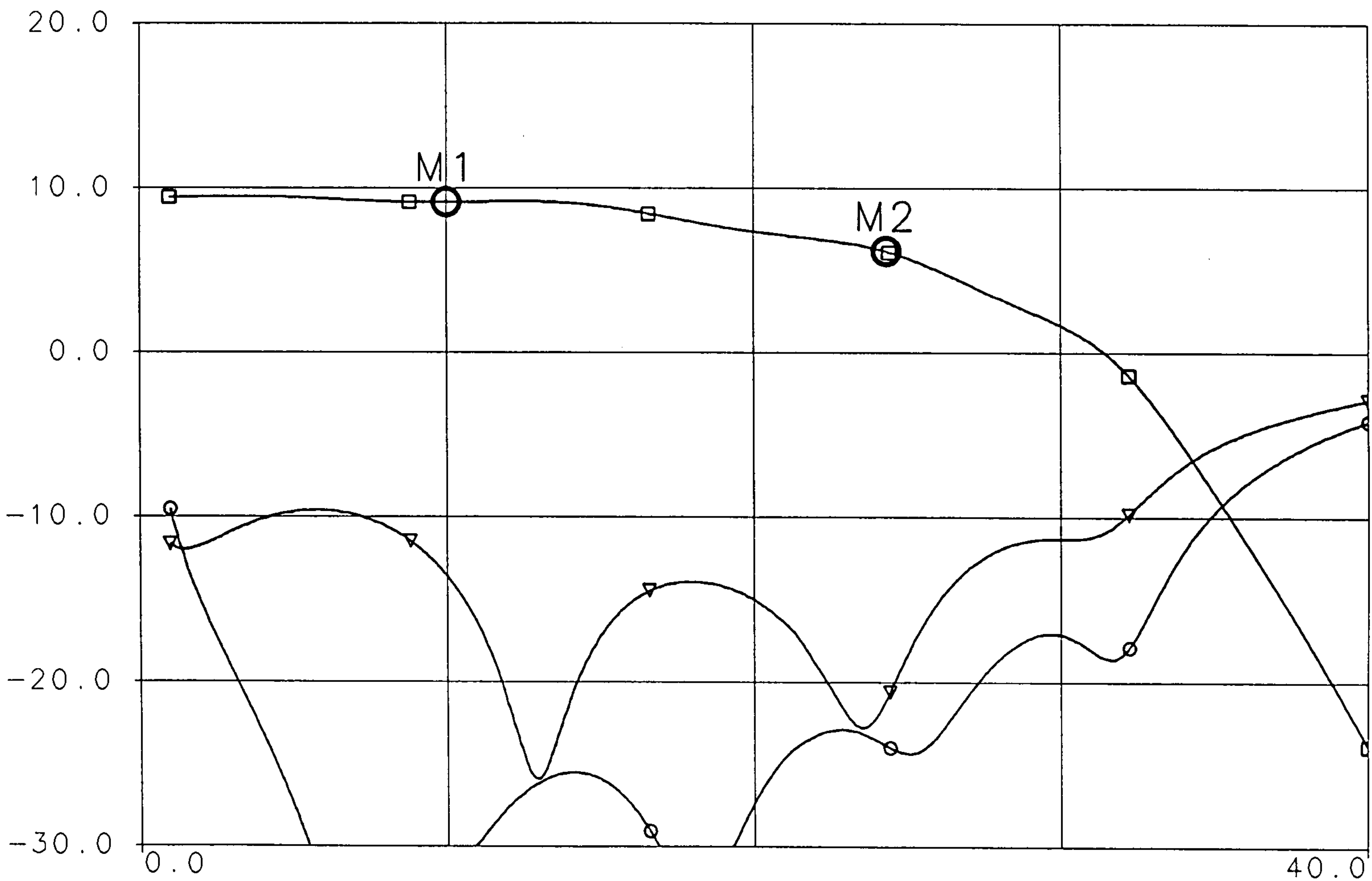
○ ECP25x6_tb
OUTPUT
InputCap
S[2,2]



Frequency 1.0 to 40.0 GHz

Four Stage Distributed Amplifier.

25x6 PHEMTs @ Ids=18mA. Linear Model.

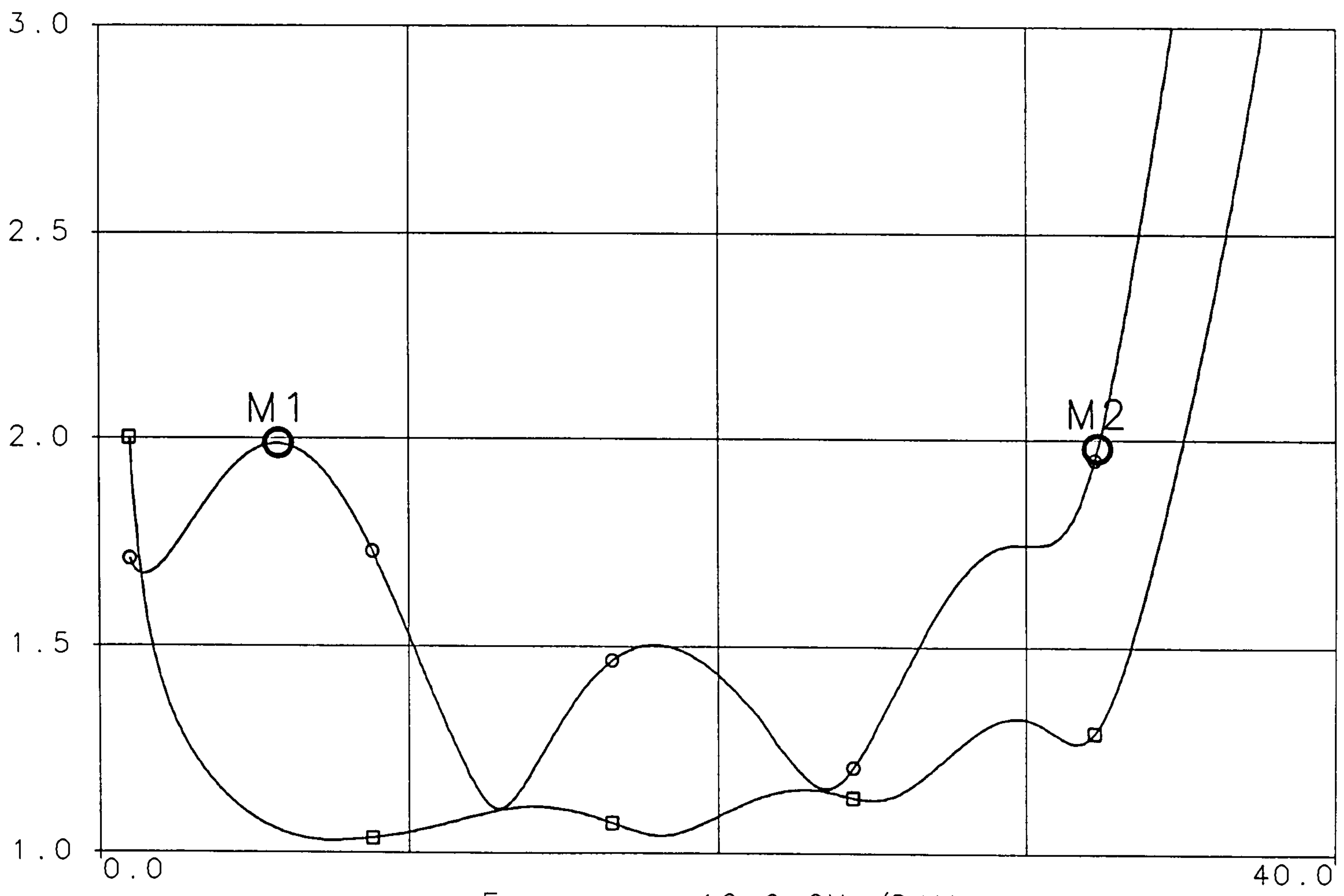


M1 Frequency=10.0000000 value=9.13649496

M2 Frequency=24.3000000 value=6.16883913

Four Stage Distributed Amplifier.

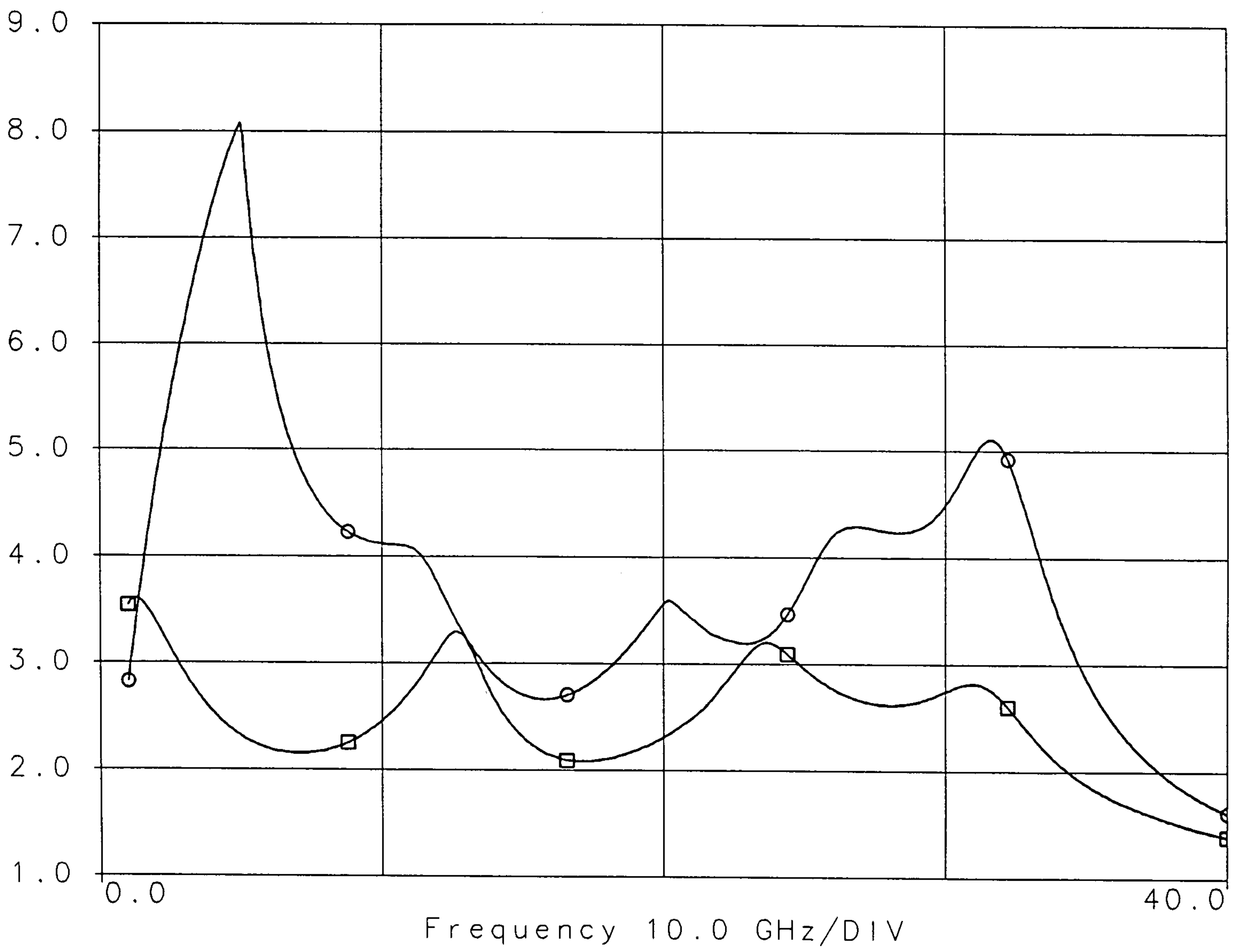
25x6 PHEMTs @ Ids=18mA. Linear Model.



M1 Frequency=5.80000000 value=1.98828782
M2 Frequency=32.3000000 value=1.98077700

Four Stage Distributed Amplifier.

25x6 PHEMTs @ Ids=18mA. Linear Model.



Four Stage Distributed Amplifer.

Linear vs. Non-Linear Models. 25x6 PHEMTs, Ids=18mA.