

# MMIC Design JHU EE787

## Fall 1998 Student Projects

C-Band General Purpose Amp -- H. Sutcliffe & T. Longreen

C-Band Power Amp1--T. Knibbe & C. Martin

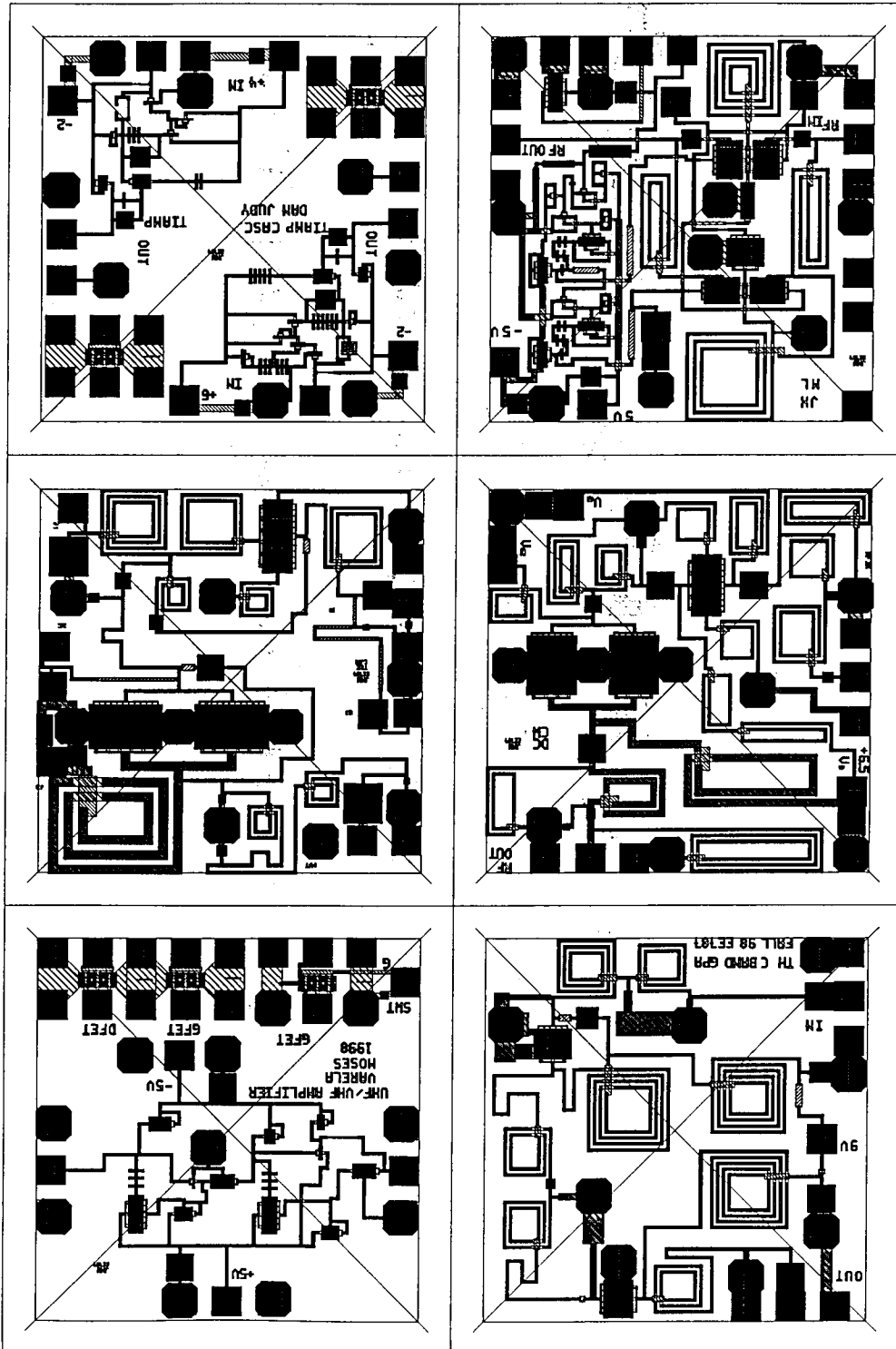
C-Band Power Amp2--D. Cross & C. Wilson

C-Band Quadrature Modulator--M. Long & J. Xiang

UHF/VHF General Purpose Amp--J. Varela & C. Moses

Plus Graduate Student Project

MMIC Transimpedance Amp--Daniel Judy



# **C BAND GENERAL PURPOSE AMPLIFIER**

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MMIC DESIGN  
EE787  
FALL 98

**Abstract:**

The object of this report is the design a general-purpose monolithic amplifier for use in the emerging C band wireless market. This design has progressed through several stages where significant milestones have been achieved and problems circumvented. The original design concept was based upon the schematic of a Ma/Com 2-8 GHz wide band amplifier.

This approach utilized a two section distributed amplifier design where each section included two amplifier stages in cascade. Extreme caution was required in this design to ensure that the phasing of the section outputs added properly. The input and output amplifier capacitance was compensated by a series inductance and bandwidth was compensated by using an intermediate stage HPF to roll off the low-end frequency response. Due to the difficulty achieving the expected power combination from the two distributed sections, a more conventional approach was taken.

The second approach evaluated was a low noise front end followed by an output power stage. This design used the noise data from a previous low noise amplifier along with the Cripps method for the power amplifier. The LNA utilized a 300um DFET while the power amplifier was resized to a 600um DFET, however, problems existed achieving the overall system bandwidth and power output even with interstage coupling comprised of HPF and LPF sections. This design strategy made it evident that a wider bandwidth performance on the front end was required.

The ultimate approach selected for this design utilizes a cascaded input feedback amplifier to increase the system bandwidth and an output power amplifier to achieve maximum power. This simple approach allows the use of two 600um DFETs while providing 19dB of gain from 4.5 to 6.0 GHz. The typical expected input and output VSWR is 1.5:1 and 1.4:1, respectively. A single nine-volt power supply with on-chip amplifier bias provides 22dBm at 1-dB gain compression. The 60x60 mil chip size includes DC decoupling for direct system level cascading.

## Introduction:

### Circuit Description:

This design is a two stage C band general purpose amplifier utilizing two 600um DFETs. A first stage amplifier with LRC feedback followed by a second power amplifier stage provide gain of 19dB across the extended band. Output power is typically 22dBm at 1-dB gain compression with expected noise figures better than 6dB. Both amplifiers operate from a single +9 volt input isolated via large LC decoupling networks. On-chip DC blocks provide direct cascading capability for implementation in a wide range of applications. The overall chip size is 60 x 60 mil.

### Design Philosophy:

The overall design was separated into the two individual stages so that the specific stage goals could be simulated and tuned for maximum performance. The first stage was goal was to provide a wide band flat gain with drain current set for low noise. A secondary goal was to provide adequate gain so that the noise figure for the overall design would be set by this stage. The chosen approach was an LCR degenerative feedback amplifier. Stability was gained as a result of limiting gain while increasing the bandwidth. In addition, the power output of the first stage was restricted using the series stabilization resistor.

A series LCR network was added between the drain to gate of the first stage 600 $\mu$ m DFET with the initial values set so that the feedback appears nonexistent. The input and output of the amplifier system was matched to S11 and S22 conjugate of the 1<sup>st</sup> stage. This first conjugate match was implemented at the end and center points of the specified bandwidth (4.5, 5.25, 6.0GHz).

While observing S21 for maximum flat gain and input/output return loss better than -10dB, the LCR feedback network elements were tuned. Once maximum flatness and gain were achieved, the IMN and OMN of the 1<sup>st</sup> stage were re-tuned while the input and output VSWR were observed for a maximum value of 1.5:1.

It should be noted here that prior to tuning any of the circuit elements, discrete bias sources with associated RF decoupling networks and large value dc blocking capacitors were in place. In the case of the 1<sup>st</sup> stage, V<sub>ds</sub> is set at 2.0Vdc while V<sub>gs</sub> is set at -0.2Vdc.

Once the desired performance was attained, the DFET was self-biased using a decoupled source resistor, a series drain resistor with a RF decoupling network, and a high value gate return resistor. The 1<sup>st</sup> stage amplifier was rechecked to verify that maximum flatness and gain along with minimum I/O VSWR were maintained. After completing this verification, slight IMN and OMN retuning was required to achieve optimal performance.

The 2<sup>nd</sup> stage power amplifier was biased using an input series drain resistor with a RF de-coupling network and a high value gate return resistor. V<sub>ds</sub> was set to 8.0Vdc while V<sub>gs</sub> was set to 0Vdc. R<sub>opt</sub> (80Ω) for the biased 600μm DFET Cripps model was determined from the IV curves and substituted for R<sub>ds</sub> once a reasonable network was designed to emulate S<sub>22</sub> of the DFET. Stabilization of the 2<sup>nd</sup> stage was achieved using an input series resistor.

The 2<sup>nd</sup> stage OMN was now tuned to match Cripps conjugate where a broadband match from 4.5-6.0GHz was the goal. The IMN was adjusted to the 2<sup>nd</sup> stage S<sub>11</sub> conjugate. Slight re-tuning was done after completion of the input match in order to achieve an output VSWR maximum of 1.4:1 across the band of interest.

The 1<sup>st</sup> and 2<sup>nd</sup> amplifier stages were then combined to complete the general-purpose amplifier system and the overall S<sub>21</sub>, S<sub>11</sub>, and S<sub>22</sub> were observed. The intermediate stage matching network, consisting of the 1<sup>st</sup> stage OMN and the 2<sup>nd</sup> stage IMN elements, were tuned while overall performance was observed. The result of this process was the reduction of the total number of components while achieving the same circuit performance.

Now with the reduced intermediate stage finalized, the INM of the 1<sup>st</sup> stage and the OMN of the 2<sup>nd</sup> stage were re-tuned for an input VSWR maximum of 1.5:1 and an output VSWR maximum of 1.4:1. Throughout the entire design of the amplifier, gain was observed to be above +20dBm and periodic checks of output power showed better than 22dBm @ 1-dB gain compression using the harmonic balance test bench. In addition, the dynamic load line was

implemented for both stages ensuring that there was no clipping of the signal and minimum harmonic generation.

**Trade-offs:**

Several different design approaches were evaluated before the final feedback and power amplifier combination was chosen. The combination two section distributed design with two stage cascade sections proved difficult to get proper power combination. The LNA and power amplifier combination did not provide the specified bandwidth required for this design.

The second amplifier noise figure was sacrificed for output power and gain. This design required a lot of large inductors and hence used up a lot of chip real estate. During the layout process, some of the spiral (TRXIND or MRIND) inductors were reduced in size and line lengths were substituted to use for component interconnects. This fact along with other layout parasitic required re-tuning of the circuit after extracting the schematic from the layout .

## Modeled Performance

The modeled performance can be broken into three main phases of the design: pre-layout, layout, and post-layout. The initial design schematic was setup with lumped Triquint elements and ideal interconnects. This design was then simulated and tuned for optimal performance. Figure 1 shows the resulting s-parameter simulated for this design. The gain is approximately 23 dB across the desired band while the input and output return loss are better than  $-10$  dB. Figure 2 displays the input and output VSWR across the band.

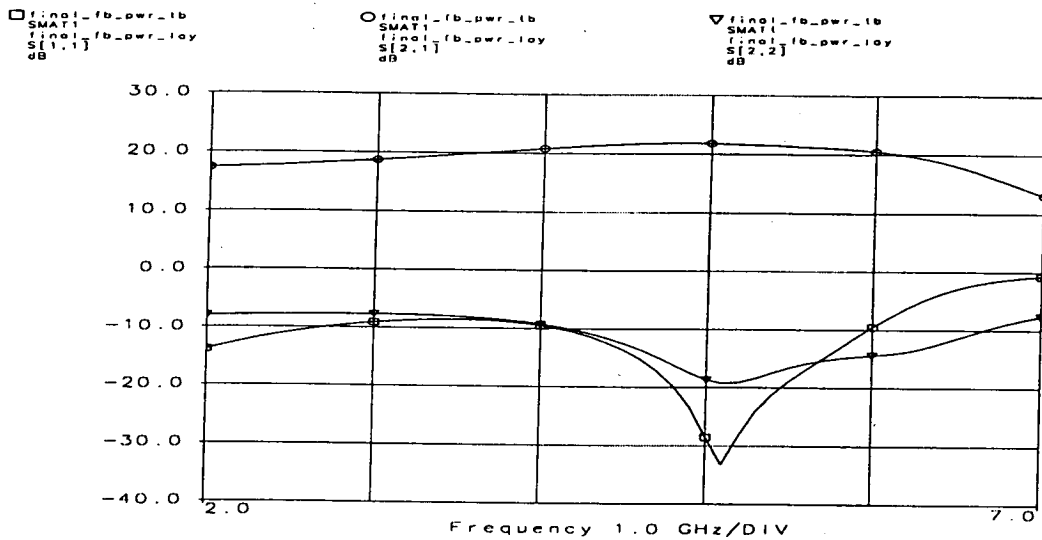


Figure 1 S-Parameters

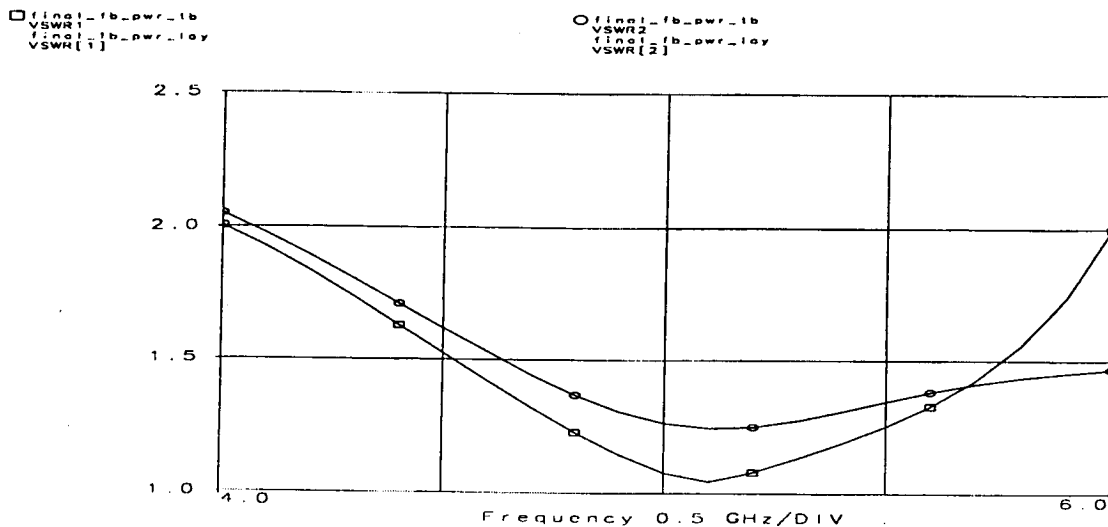


Figure 2 Input/Output VSWR

Output power for the design was then simulated for a sweep of input power at the midpoint and ends of the frequency band resulting in 23dBm at 1-dB gain compression, as shown in Figure 3. The third order intercept of 39dB was then determine using graphical methods, Figure 4. (This number seems high and may be the product of an incorrect test setup)

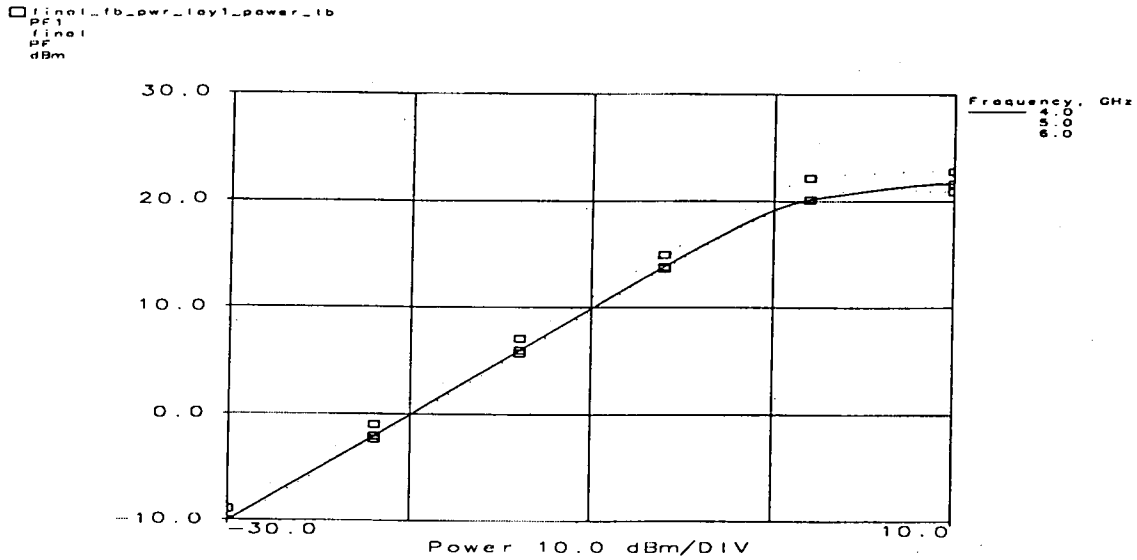


Figure 3 Output Power

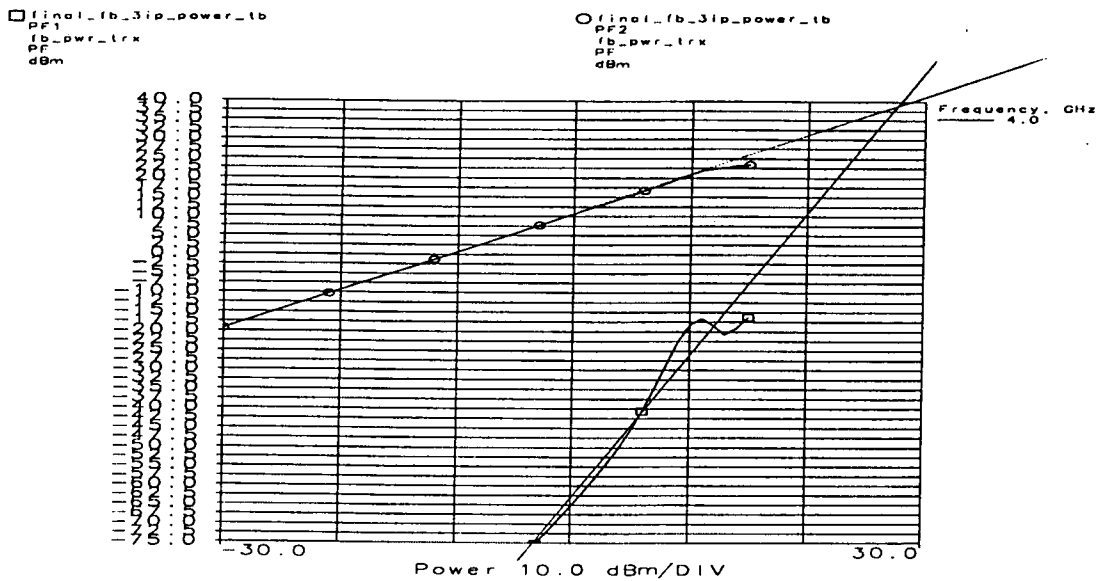


Figure 4 Third Order Intercept



Stability of each of the individual amplifier stages were checked to ensure that the input and output was stable ( $\mu >= 1$ ). The overall system stability was also simulated, Figure 5.

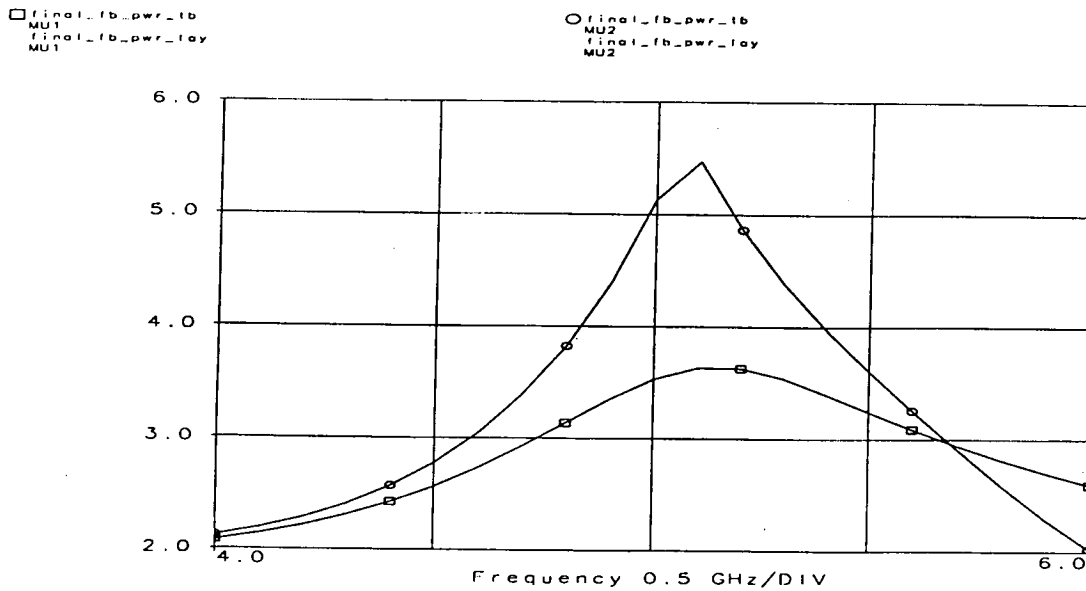


Figure 5 Stability

The following compliance matrix shows a comparison of the specification, goal, and simulated performance criteria, Table 1. The achievement of the noise figure is based on the first amplifier biased at a comparable level to the previous LNA design, but scaled for the 600um FET size.

Requirement	Specification	Goal	Simulated
Frequency	4.5 to 6.0 GHz	2.0 to 6.0 GHz	4.0 to 6.0 GHz
Gain	>15 dB	18 dB	20 dB
Noise Figure		6 dB	Achieved
Output Power	> 12 dBm @ 1dB comp		23 dBm @ 1dB comp
Output IP3		25 dBm	39 dBm
VSWR	1.7:1 input, 1.3:1 output		1.5:1 input (typ) 1.4:1 output (typ)
Supply Voltage	Vd=9 volts Vg on chip	Vd=8 volts Vg on chip	Vd=9 volts Vg on chip
Size	60 x 60 mil ANACHIP		60 x 60 mil ANACHIP

Table 1 Compliance Matrix

This lumped schematic was then used as the basis for the layout phase. The layout of the design required the addition of small lines lengths, the twisting of lines to fit, and the unraveling of some of the spiral inductors so that it could be used for interconnect. The resulting layout is shown in Figure 6.

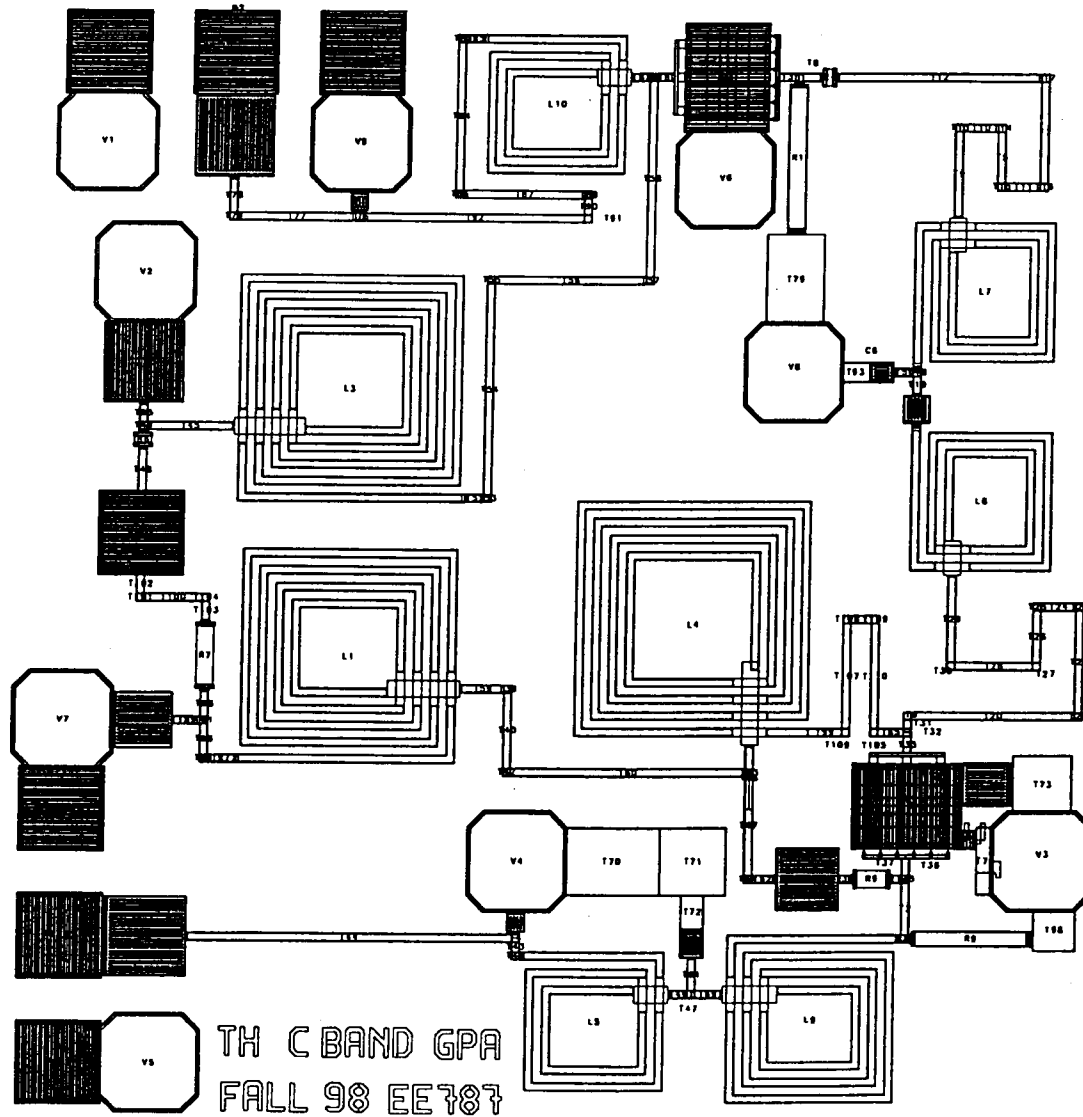


Figure 6 Final Layout

Throughout the layout process, additional tuning and component value adjustments were required to make the post-layout schematic as close as possible to the original lumped element model. The resulting design was then simulated and performance plotted. Figure 7 shows the resulting s-parameter simulated for this design. The gain is approximately 19dB across the desired band while the input and output return loss are better than -10dB. Figure 8 displays the input and output VSWR across the band.

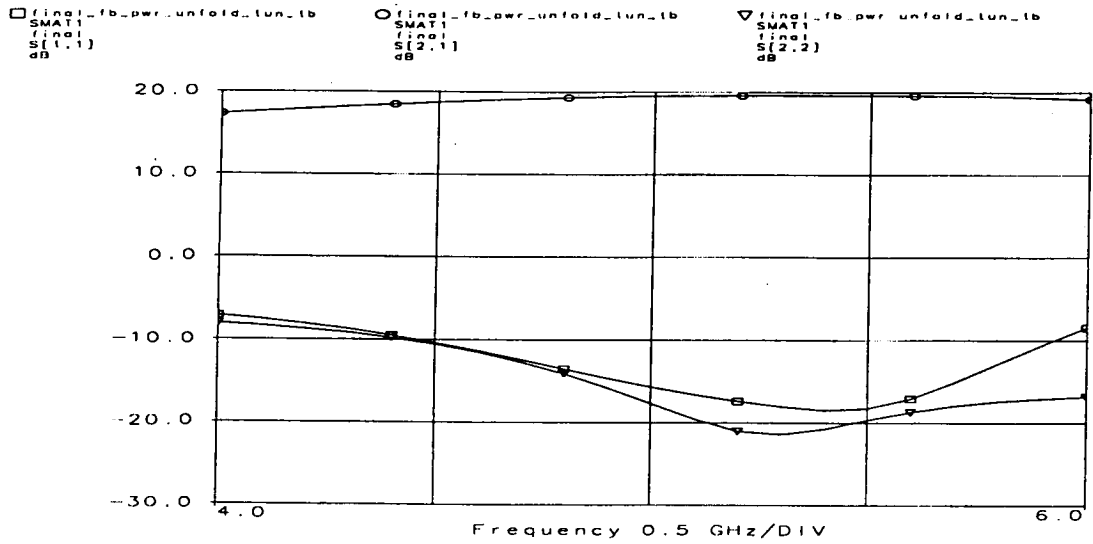


Figure 7 S-Parameters

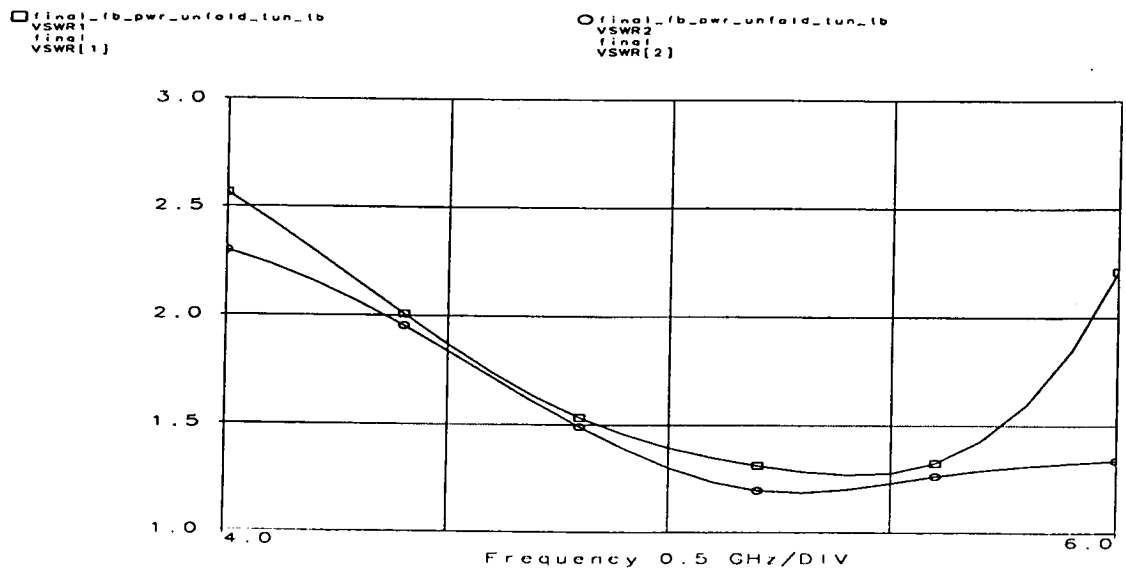


Figure 8 Input/Output VSWR

Output power for the design was then simulated for a sweep of input power at the midpoint and ends of the frequency band resulting in 22dBm at 1-dB gain compression, as show in Figure 9. Lastly, the overall system stability was resimulated with no change.

\_fb\_tb  
\_fb\_pwr\_unfold\_

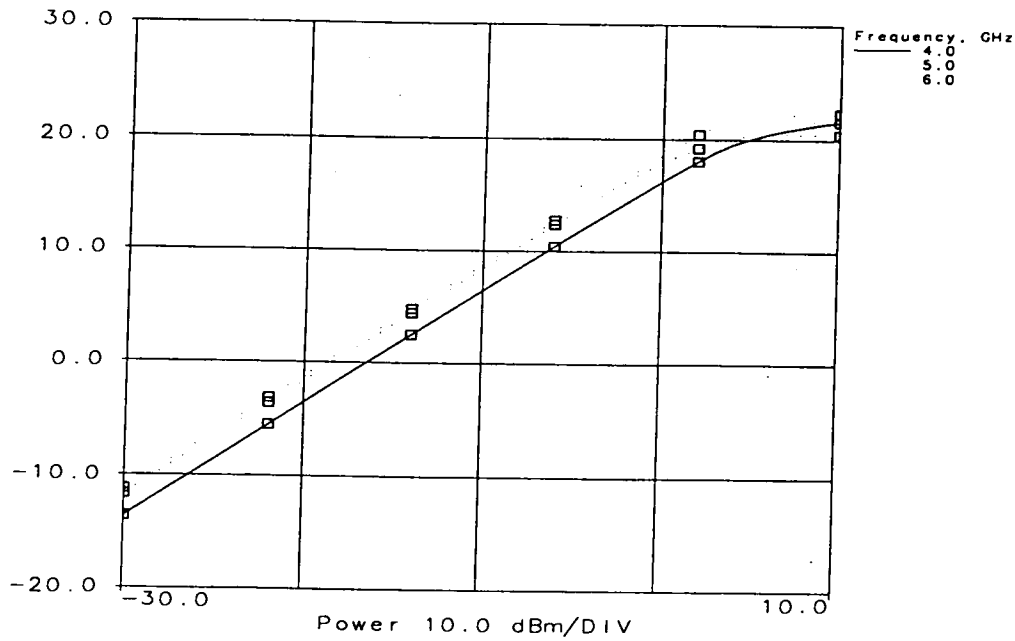


Figure 9 Output Power

### Schematic Diagram:

The original schematic was drawn in Libra with lumped elements, ideal interconnect, and ideal biasing, Figure 10. The baseline circuit of the GPA amplifier was simulated using this document. After optimum performance was achieved through simulation, the GPA was synchronized and the layout was extracted.

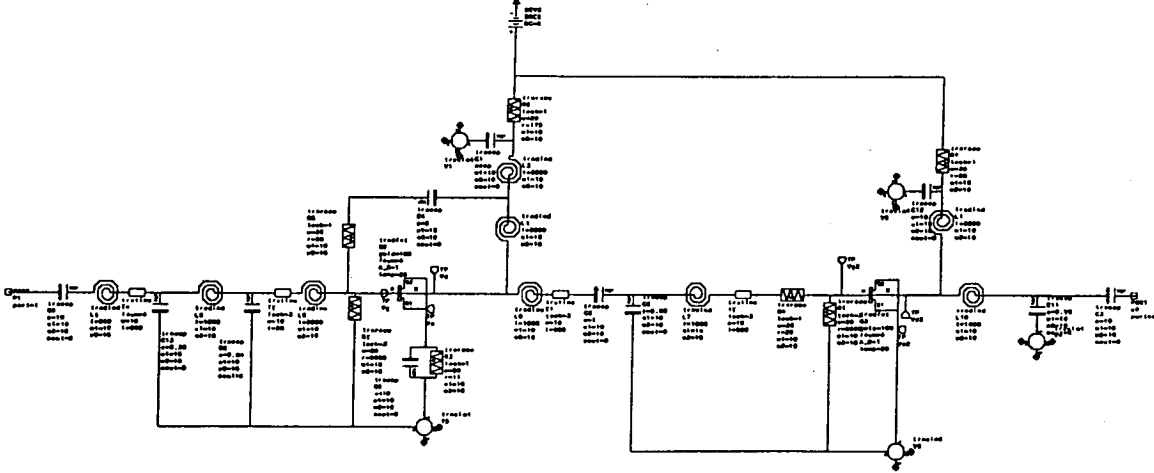


Figure 10 Original Lumped Element Schematic

Another schematic was extracted from the final layout and unfolded so that final simulation and optimization could be accomplished. After completing the design of the GPA, the circuit elements were lumped in order to draw a definitive schematic in ORCAD. This schematic is presented as Figure 11.

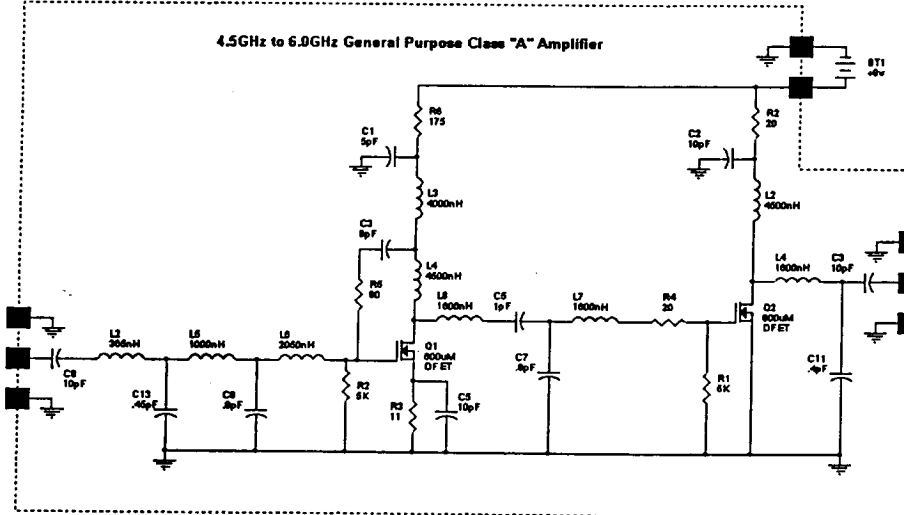


Figure 11 ORCAD Final Unfolded Lumped Element Schematic

### DC Analysis

The DC biasing for both amplifiers was setup to run from a single drain supply voltage of 9 volts. This design feature was achieved by on chip resistor networks setting the appropriate drain current and gate voltage. The feedback amplifier bias was selected for low noise performance by scaling the drain current to match the 600um DFET size. The power stage was biased for high gain and power. In order to simplify the layout, a gate voltage of close to zero volts was chosen for the second stage. The resulting performance was then simulated and tuned, Table 3,

	Vgs (volts)	Vds (volts)	Ids (mA)
Stage 1 (Feedback Amp.)	-0.2272	4.6240	22.9410
Stage 2 (Pwr/Gain Amp.)	0.0379	7.7585	54.9892

TABLE 3 Modeled DC Analysis

### Test Plan

The initial step of the test plan is to apply the +9 volt DC supply in series with an ammeter. The total current should be around 78mA based on the combined current from the DC analysis in section 5. The second aspect of testing will be chip level probe testing with the HP 8510 network analyzer and a single source power supply configured as soon in Figure 12.

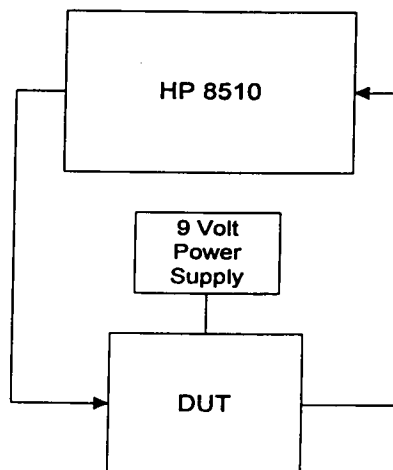


Figure 12

The tested s-parameter results will be saved as a S2P file, graphed in Libra, and compared to the modeled S2P file. This will allow an accurate comparison of the actual vs. simulated chip performance across the desired frequency band.

The last phase of chip testing will involve a signal generator, spectrum analyzer, and a single source power supply configured as soon in Figure 13.

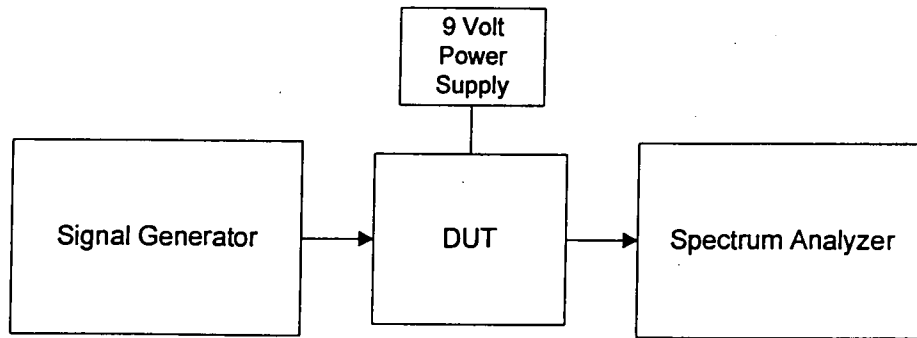


Figure 13

The input power will be incrementally increased while the output power is recorded. This data will then be compared to the simulated power data and 1-dB gain compression shown in section 3.

The third order intercept will be determined by finding the input power point where the first and third order harmonics are equal on the spectrum analyzer.

## Conclusion & Recommendations

The cascaded feedback and power amplifier combination proved to be a good overall design with the ability to meet all specifications. We recommend a resizing of the second power amplifier so that the drain current could be reduced. This would guarantee the low noise requirement of the design, which was difficult to simulate without reliable data. This design should work well in the role as of a general purpose C band amplifier.





## Final Report

### Summary

Our project is a 1 watt wide band power amplifier using TriQuint's GaAs process. The requirements for the amplifier are:

Power output	1 watt saturated output over the 2 to 6 GHz range
Gain, small signal	>18 dB
VSWR (input)	<2:1
VSWR (output)	<2.2:1
Efficiency	25%
Supply Voltage	<8 Volts
Chip size	60 x 60 mil

These specifications are the same as the MA-COM MAAM26100 Power GaAs MMIC Amplifier. This part uses a higher voltage process with a breakdown above twenty volts.

### Introduction

To accomplish these goals we designed a two stage amplifier using the power GFET devices from the TriQuint library. The first stage amplifier uses one GFET with 12 .6x100u long fingers and 500 nH source inductance per source contact for stability. A negative feedback loop consisting of a series resistor, capacitor, and inductor is used improve wide-band response by keeping the input and output S-parameters within the Smith chart over a wider band. This negative feedback peaks the high frequency gain and reduces low frequency in-band gain to flatten the overall response while making the input and output better matches to 50 ohms.

Interstage matching is accomplished with a simple blocking capacitor and a shunt-C, series-L combination.

The second stage uses two GFET devices with 12 .6x150u fingers to get better ground contact for the source node and to reduce phase shift between the different gate fingers of the devices. The width/number of fingers ratio was played with to get an aspect ratio that best fit into the available space on the chip. Again, negative LRC feedback was employed to better match the input and the output over a wide band. The output match is to 16.7 ohms to get the desired 1 Watt output with the 14 Volt DC breakdown seen on the devices. This impedance is transformed to 50 ohms by the OMN to match to the external world. No extra inductors or capacitors are on chip to attempt to quash out problems with bond wires since space is such a premium on the chip. Large DC blocking capacitors are on the input and output nodes; 10pF and 20pF respectively.

Our design goal was to meet as many of the specifications as possible while still fitting into the 60 x 60 mil chip size. This chip size required us to make extensive use of the optimizer in an iterative process of trying to fit everything, optimizing, and then seeing if the new optimized chip would still fit. We ended up having to sacrifice some on inductor and capacitor sizings in order to fit the chip. This did not too adversely affect the design as we still achieved most of the design goals. To best instill a sense of confidence with our design, we varied the components over reasonable two sigma process variations; capacitors +/-15%, resistors +/-20% N+ and +/-7% NiCr, and the GFETS +/-10% in size. These changes had minimal impact on the results of the design, therefore we feel that it is quite robust to process

variations. Possible simulated instability was only achieved when all four variations went two sigma in the wrong direction, a very unlikely event assuming all four parametric variations are independent. The inductors were not varied, as the 500nH delta in value is far greater than any variance that is assumed will be seen. Also inductance value being primarily controlled by the etching of the physical elements themselves makes the inductors the least variable component.

### Modeled Performance

The following is the compliance matrix we used in the design

Parameter	Design Goal	Simulation Results
Frequency	2 to 6 GHz	1.75 to 6.5 GHz
Gain, small signal	18 dB	23 dB
Output Power (P1dB)	1 watt	~1 watt
Efficiency	25%	Unable to get convergence here
VSWR, 50 ohm, input	<2:1	1.6:1
VSWR, 50 ohm, output	<2.2:1	1.4:1
Supply voltage	8 Volts	7 Volts
Size	60 x 60 mil	60 x 60 mil

The supply voltage of 7 Volts is required because this is the center for the load line with the TriQuint GFET device's comparatively low breakdown of about 14 Volts as simulated. With the maximized ~12V output swing (1-13V), it is impossible to get the 1 watt out into a 50 ohm load. To accomplish this, we drive a 16.7 ohm load and then do an impedance transformation to get it to 50 ohms at the output terminal. This works well in simulation, with saturation (and model non-convergence) beginning ~2 dB shy of +30dBm output power mark, indicating that in hard saturation we should be able to achieve the desired +1W saturated output power.

The simulation results show that we should see performance as good as the designed goals. The problem with the simulation results has been trying to get convergence for many of the power graphs. Therefore much of this data is extrapolated or inferred from the results that we were able to obtain.

The over band S-parameters (Figure 1) show that the input and output matching is better than -10 dB over the whole band of interest and usually better than -15 dB. The small signal forward gain for the amplifier is better than 21 dB over the band of interest and typically between 22 and 23 dB peaking to 25 dB at 6 GHz. When viewing the S11 and S22 on the Smith chart in band (Figure 2), it can be seen that both circle 50 ohms quite well.

When looking over a 1 to 8 GHz bandwidth (Figure 3) it is seen that S11 and S22 are always less than 0, and that the small signal gain for the amplifier drops below 18 dB at about 1.75 GHz and 6.5 GHz. Looking at the broadband Smith chart for S11 and S22 (Figure 4), it can be seen that they stay well inside the edges of the Unit Smith Chart, and show no signs of going outside the chart. In fact, looking at the stability plots MU1 and MU2 (Figure 5) it can be seen that both are well above 1 over the 1 to 8 GHz range. The lossy nature of the real TriQuint elements, as well as the 500nH source stability inductance in the first stage and the RC high-frequency shunt at the input, helped achieve this broadband stability. Finally the VSWR graph (Figure 6) shows that over the desired band, that VSWR is always less than 1.8, and for most of the band, it is better than 1.6 for the input and 1.4 for the output.

Although we had some difficulty is getting power output simulations to converge, we can show simulated Pout versus Pin for 2.5GHz (Figure 15), 4.0GHz (Figure 16), and 5.0GHz (figure 17). Power simulation at 2.5GHz produces a linear power gain of 20dB up to +27dBm output (at which point the models will not converge any further). Power simulation at 4.0GHz yields 18dB of power gain until +29dBm output (at 0.6dB compression). Finally, power simulation at 5.0GHz shows 16dB of power gain up to +27dBm

output (at 0.9dB) compression. All of these results leave the design within shooting distance of +30dBm (1W) output power in hard saturation, with the possible exception of the high end. Due to the negative slope in the DC characteristics of the TriQuint GFET model at high operating currents, we were unable to exercise the full range of current swing for available for a given size GFET, thus impacting our power-added efficiency. Although we were unable to get this simulation to converge, we would not expect the design to meet the 25% PAE goal.

When simulating with the 2-sigma process variances, the design is rather immune to a 2-sigma change in any one of the significant process variations. The nominal design is shown in Figure 7. A ~~10% increase~~ GFET size increase of 10% slightly reduces the high frequency gain, whereas a 10% reduction peaks the high frequency gain and creates a slight dip in the stability plot at high frequency (although a 50 ohm load is still quite stable) (Figure 9). Similarly, a 2-sigma increase in the capacitor values (+15%) yields a high frequency gain peaking, with an associated dip in the stability (but not as great as due to GFET sizing), while a 2-sigma decrease (-15%) also decreasing the high frequency gain (Figure 9). A 2-sigma decrease in the NiCr resistor values (-7%) (Figure 10) or a 2-sigma increase in the N+ resistor values (+20%) (Figure 11) also has a high-end gain peaking effect, but without a corresponding dip below unity for MU1/MU2. Simulated instability is achieved if all four variations are allowed to deviate 2-sigma in the wrong direction; GFET size -10%, capacitors +15%, NiCr resistors -7%, and N+ resistors +20% (Figure 12). If we can assume each of the process variations to be independent, this should indeed be an unlikely event (2-sigma  $\rightarrow$  97%: 3% reject occurs four times independently  $\rightarrow$  0.000081%).

### Schematic Diagrams

The schematic (Figure 13) and layout (Figure 14) shows a two stage amplifier design with both stages having drain-gate negative feedback. The first stage also uses source inductance to reduce instabilities but not so much as to destroy the gain from this stage. The LCR series feedback is set to reduce feedback at high frequencies thereby enhancing overall gain for the stage. Matching networks were optimized using the maxim that inductors are big so anything to reduce or remove them is best. So, whenever possible, capacitors were increased to allow for reduction in inductance.

The gate biases are brought in using series resistors so that the bias voltage can be set externally depending on the process results. The drain biasing is done through large series inductors on the drain to isolate the drain port from the bias voltage while not dropping much DC voltage across the isolation device. This is important as we are biasing the output stage at approximately 450 mA of current.

Several inductors in the initial schematics were "unrolled" to make better use of space and since to reach one point to another some length of metal run would be required, often of a length close to the values of the inductors that were in series with these lines. Where extra line was needed to create an equivalent inductance, "trombones" were stuck in the metal runs. These could then be adjusted to get the correct inductance values.

### DC Analysis

The biasing for the devices uses drain inductors and gate resistors to isolate the bias voltages from the internal ports. The two drain and two gate biases are isolated so that no coupling should be seen between the drains or gates. The bias currents for the drains are 150 mA for the first stage and 450 mA for the second stage. The DC current path for the second stage was set 30u wide to allow for 540 mA DC current (assuming that only ME2 is this narrow and that all ME1 by itself is twice as the ME2) and we are biasing at 450 mA in this stage so that should be safe (with 20% upside variation). The AC path is 10u wide since the RMS current through the AC signal path in the output is about 171 mA. This can be handled by ME2 of 10u, which is the narrowest seen for the inductors with most of the path being ME1, and ME2 combined.

## Test Plan

The testing shall work as follows:

Test Number	Test	Results
Pre-test setup	Put RF probes on the input and output pads. Put four other probes down for the Gate and Drain voltages of the two stages. Place an extra ground probe for the DC path.	All the pads have probes on them. The DC supplies and the RF test equipment are set up for testing the part.
1	Bias the gates of the two stages to cut-off (approximately -3 V)	No bias current is seen
2	Bring up the Drain voltage on the first stage to 7 Volts	No bias current is seen
3	Bring up the Gate voltage on the first stage to where we get the bias current expected (XXX mA) (approximately -1 V)	Expected bias current is seen at the expected gate bias voltage
4	Bring the Gate voltage and then the Drain voltage on the first stage back down to ground	
5	Bring up the Drain voltage on the second stage to 7 Volts	No bias current is seen
6	Bring up the Gate voltage on the second stage to where we get the bias current expected (XXX mA) (approximately -1 V)	Expected bias current is seen at the expected gate bias voltage
7	Bring the Gate voltage and then the Drain voltage on the second stage back down	
8	With both drain voltages set to 0, set the Gate voltages to the values found above	No bias current is seen
9	Bring up the Drain voltage on the first stage to 7 Volts	Expected bias current is seen for the first stage
10	Bring up the Drain voltage on the second stage to 7 Volts	Expected bias current is seen for the whole circuit
11	Measure small signal performance of the amplifier	It should match the S-parameter measurements from simulation
12	Measure large signal performance of the amplifier	It should match the measurements from simulation

The test setup is very simple. Four power supplies for the for DC connections, and the HP 8510 to measure the S-parameters. (Figure 13)

## Conclusion and Recommendations

Our 1 watt 2 to 6 GHz power amplifier design shows promise for working over the 2 sigma variations of TriQuint's models. The small signal results are very good, and the large signal results are good where we are able to get the models to converge. Problems with the negative slope seen in the GFET model have hampered much of the large signal analysis.

gfet2out\_tb  
 S11  
 allprocess  
 S[1,1]  
 dB

gfet2out\_tb  
 S22  
 allprocess  
 S[2,2]  
 dB

gfet2out\_tb  
 S21  
 allprocess  
 S[2,1]  
 dB

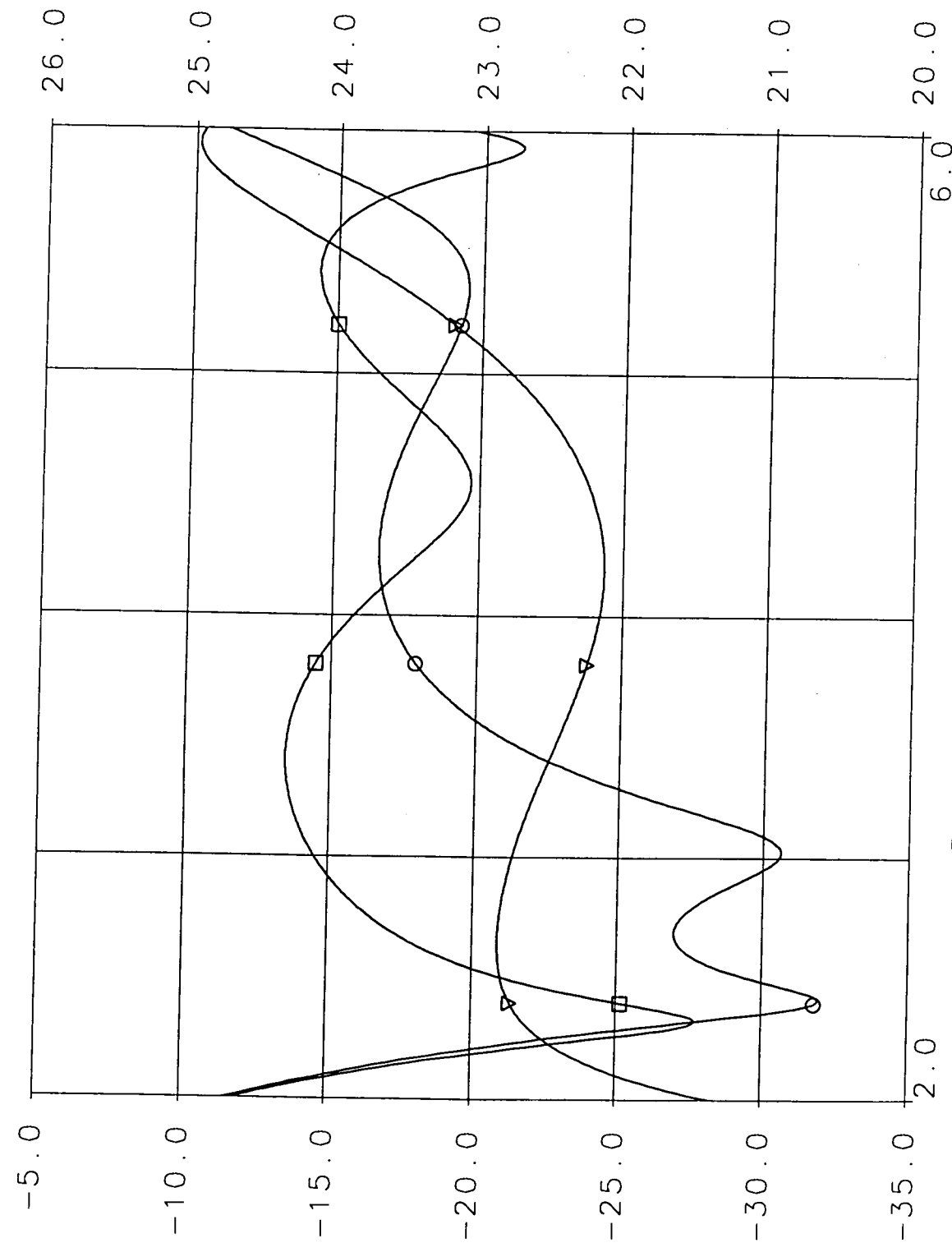


Figure 1: S-Parameters from 2-6GHz

□ gfet2out\_tb  
S11  
gllprocess  
S[1,1]

○ gfet2out\_tb  
S22  
gllprocess  
S[2,2]

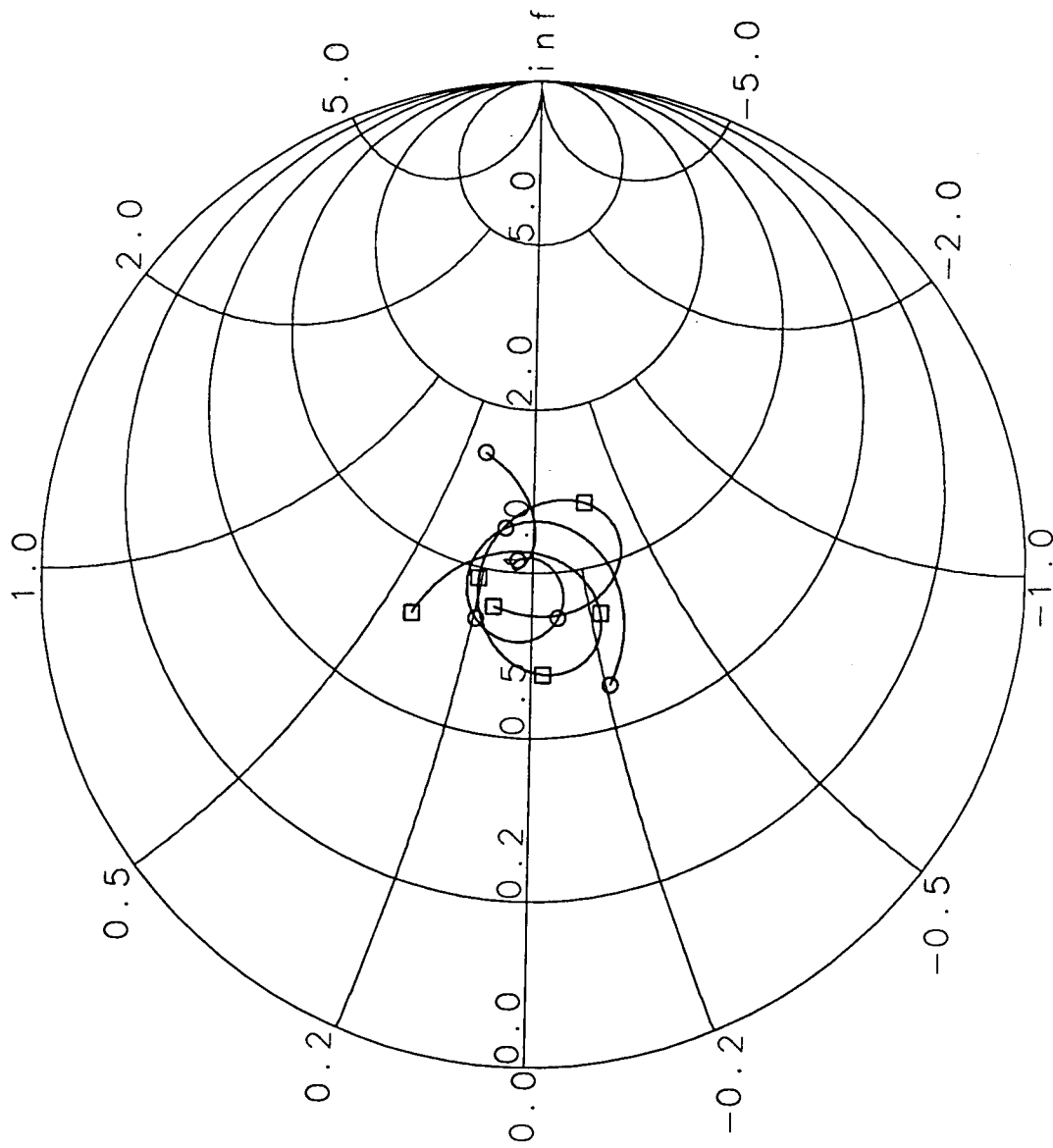
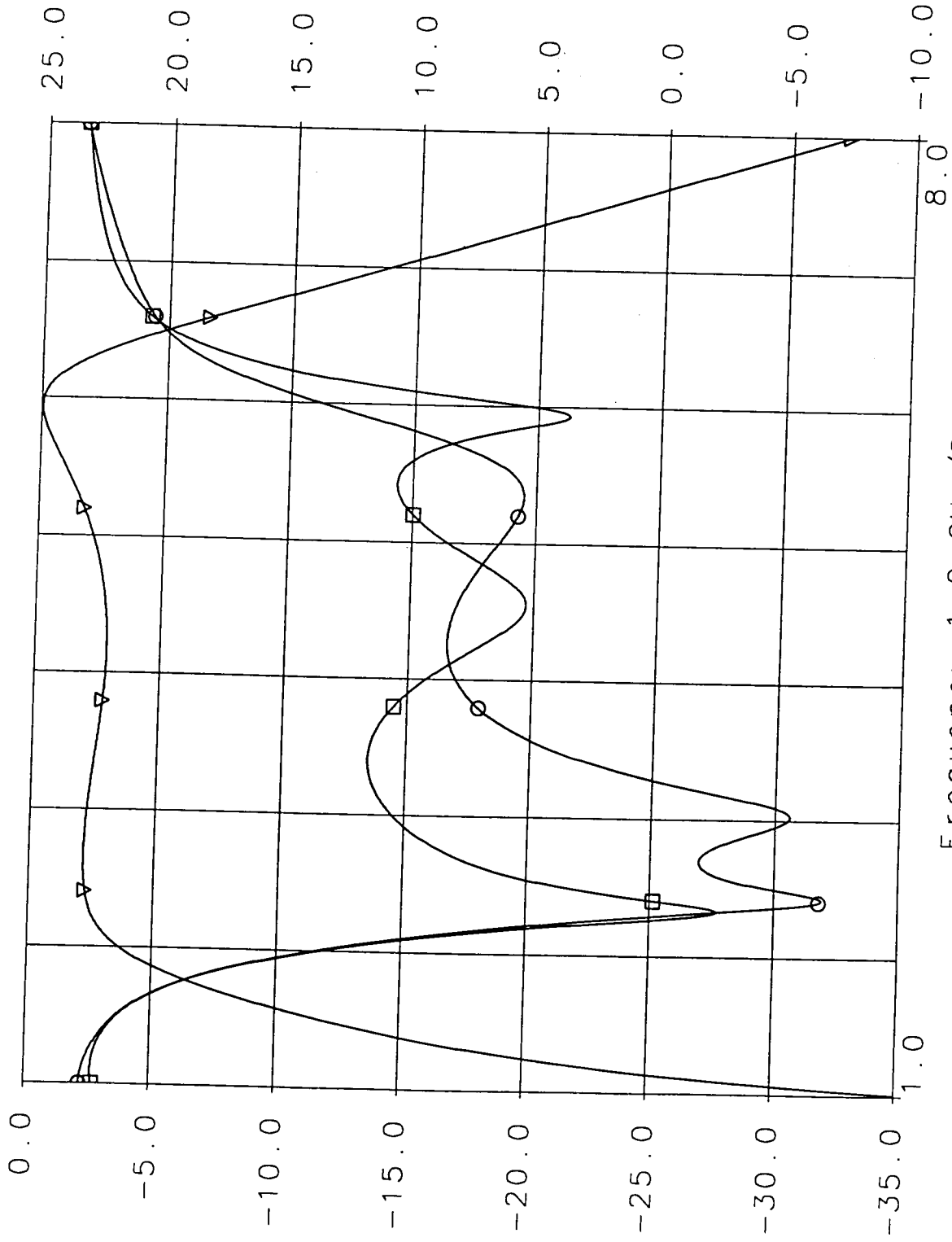


Figure 2: S11 and S22 from 2-6GHz  
Frequency 2.0 to 6.0 GHz

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



Frequency 1.0 GHz/DIV

Figure 3: Broadband S-Parameters from 1-8GHz



□ gfet2out\_tb  
S11  
allprocess  
S[1,1]

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]

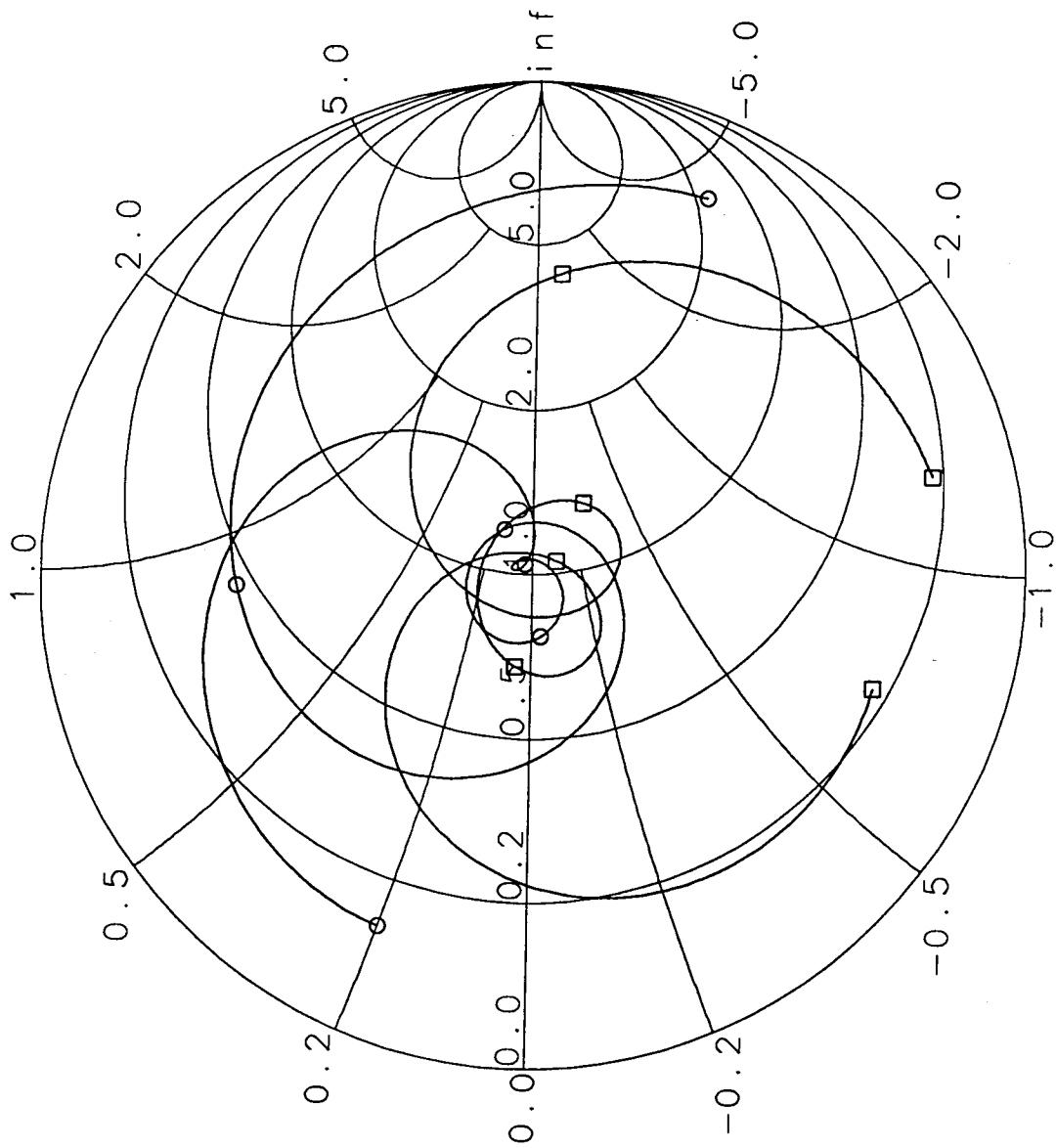


Figure 4: Broadband S11 and S22 from 1-8GHz

□ gfet2out\_tb  
MU1  
allprocess  
MU1

○ gfet2out\_tb  
MU2  
allprocess  
MU2

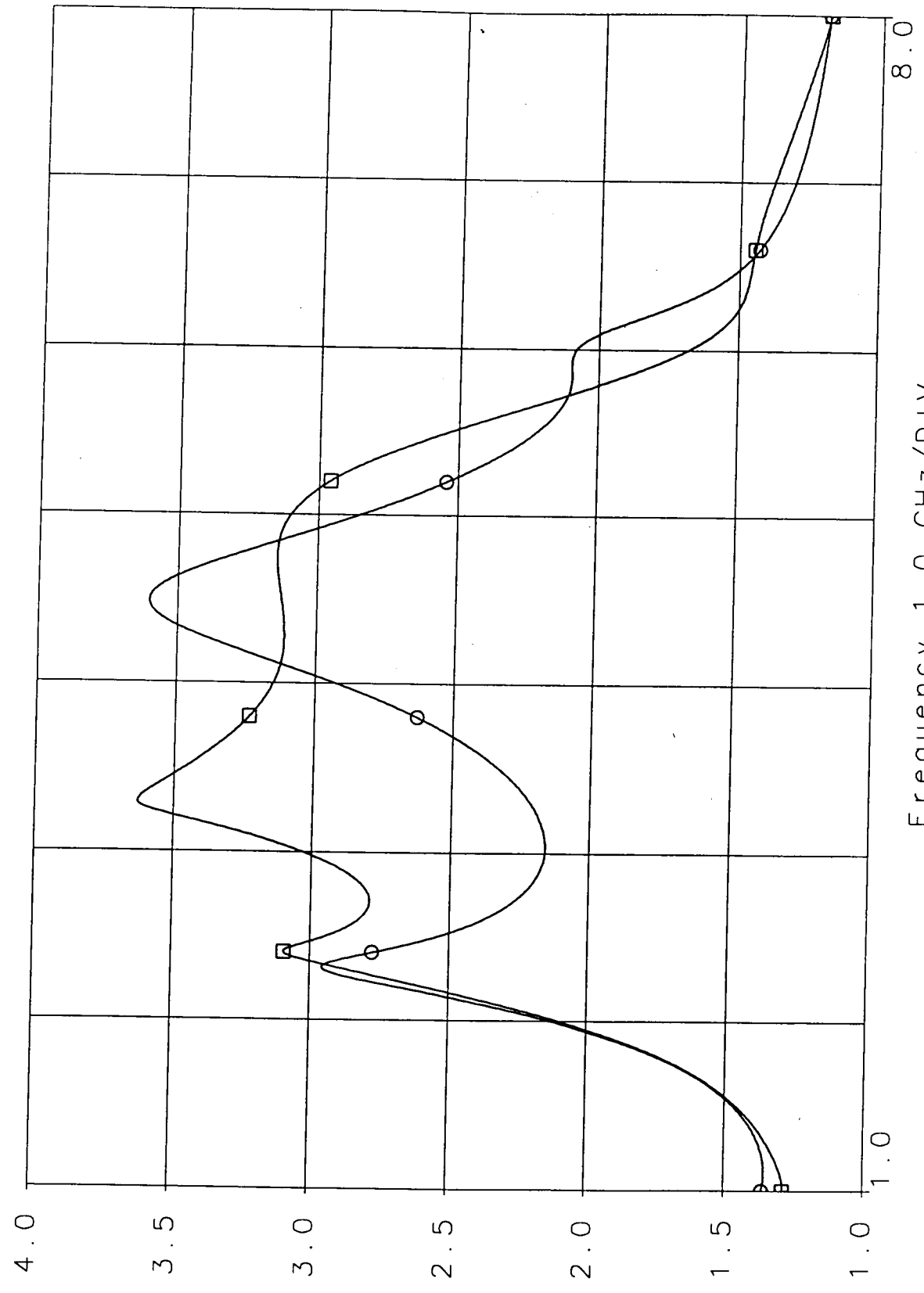


Figure 5: MU1/MU2 Broadband Stability 1-8GHz

□ gfet2out\_tb  
VSWR1  
allprocess  
VSWR[1]

○ gfet2out\_tb  
VSWR2  
allprocess  
VSWR[2]

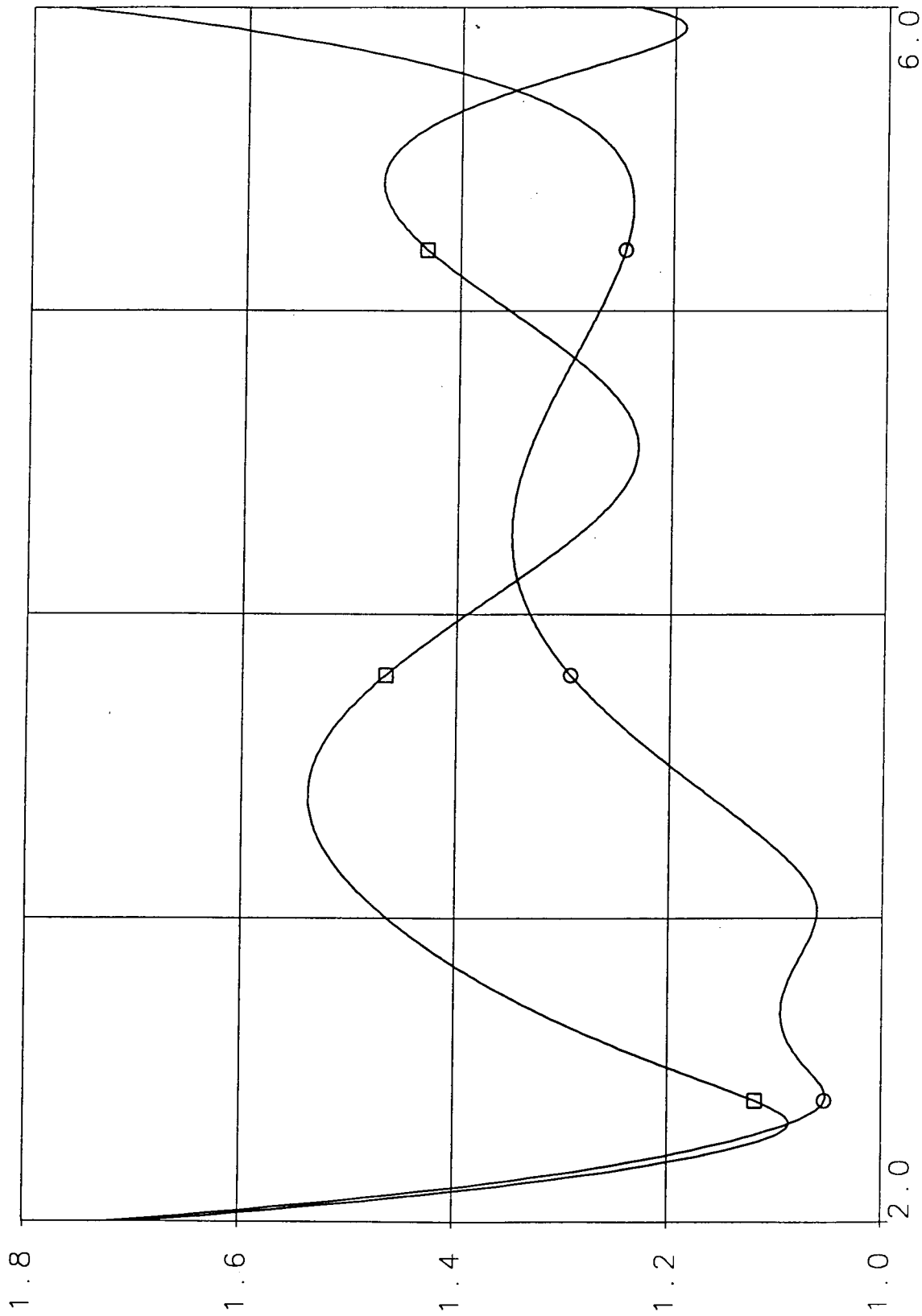
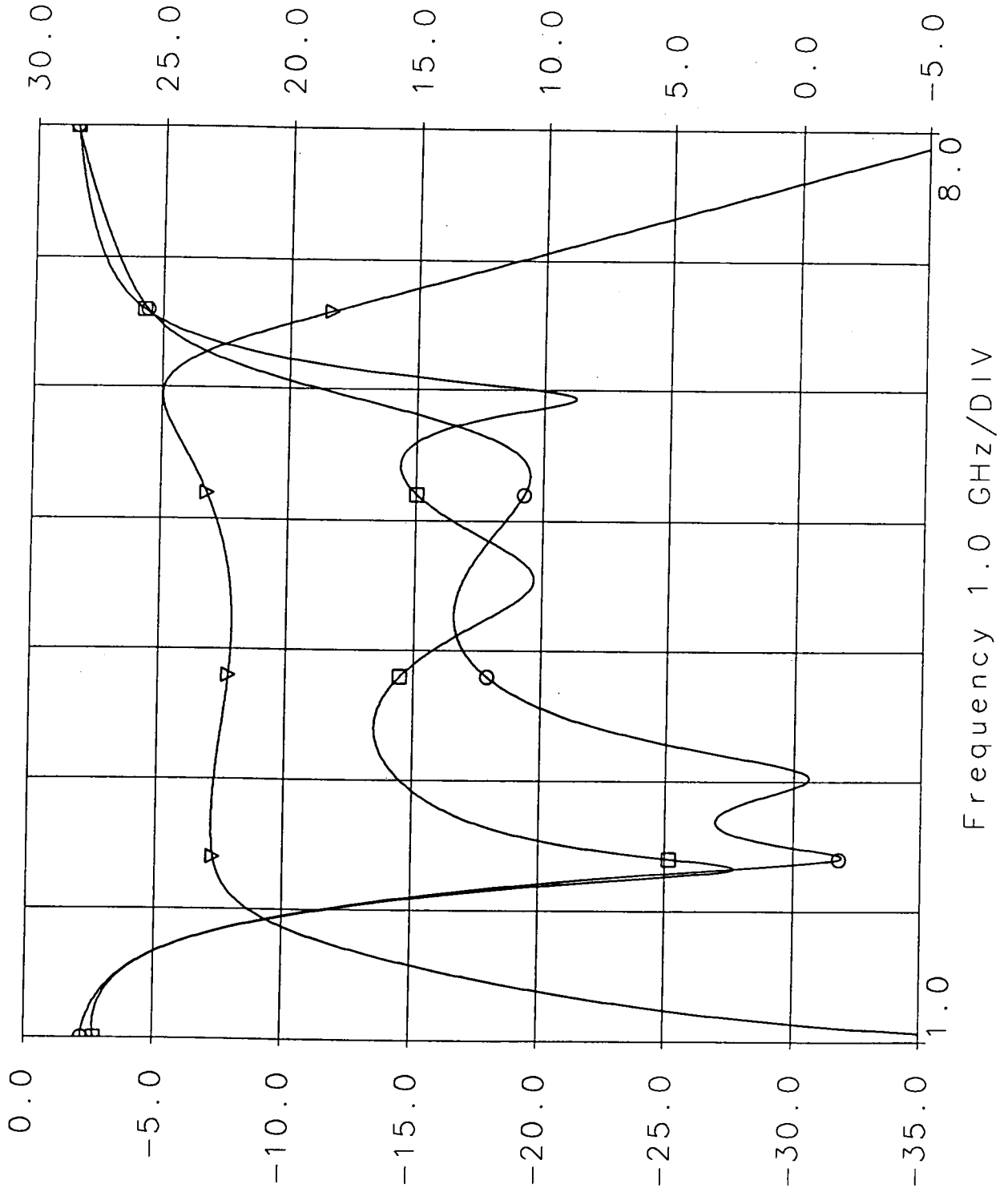


Figure 6: Input/Output VSWR 2-6GHz

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



NORMAL  
FIG 7:  
NORMAL

7/21/50

○ gfet2out\_tb  
MU2  
allprocess  
MU2

□ gfet2out\_tb  
MU1  
allprocess  
MU1

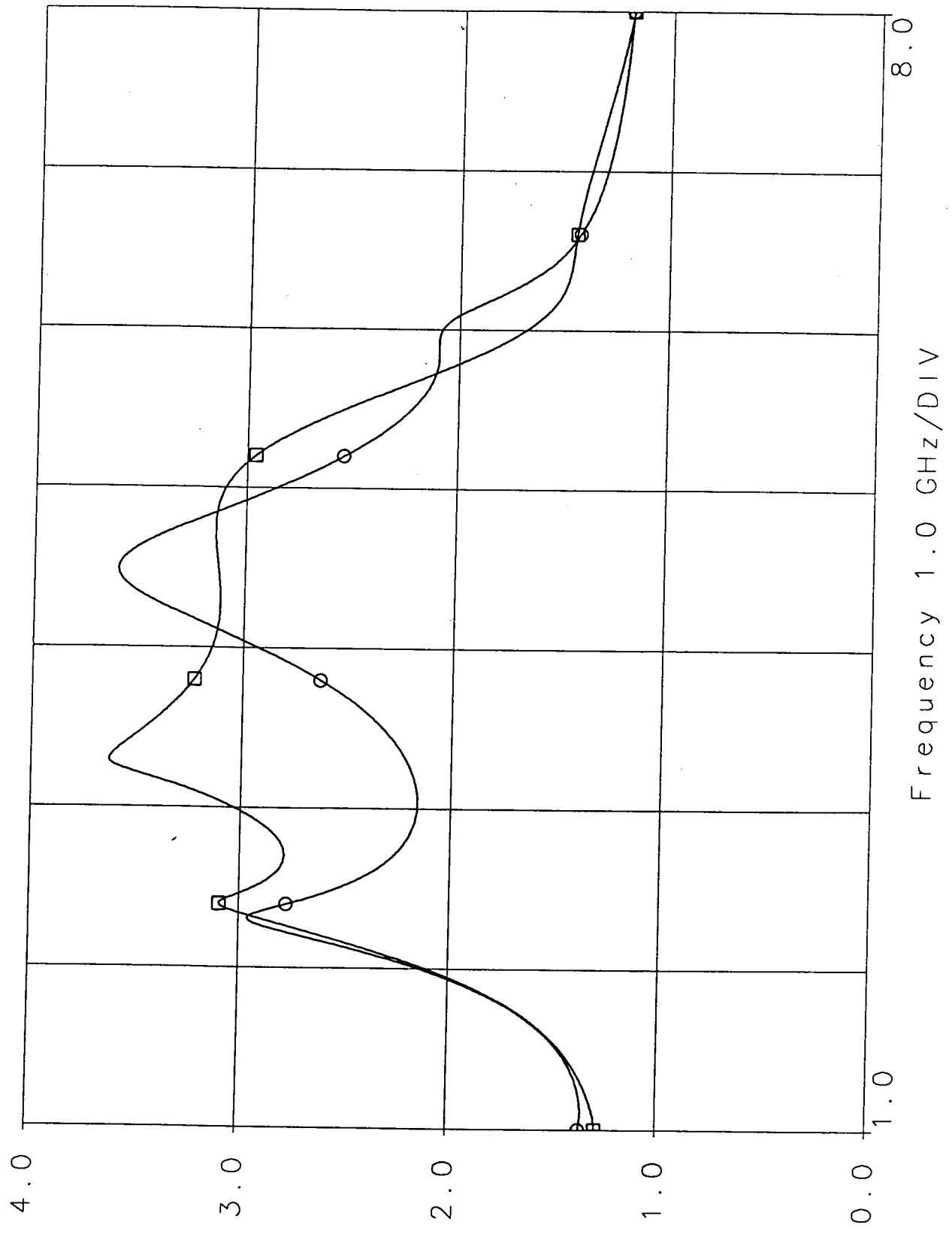
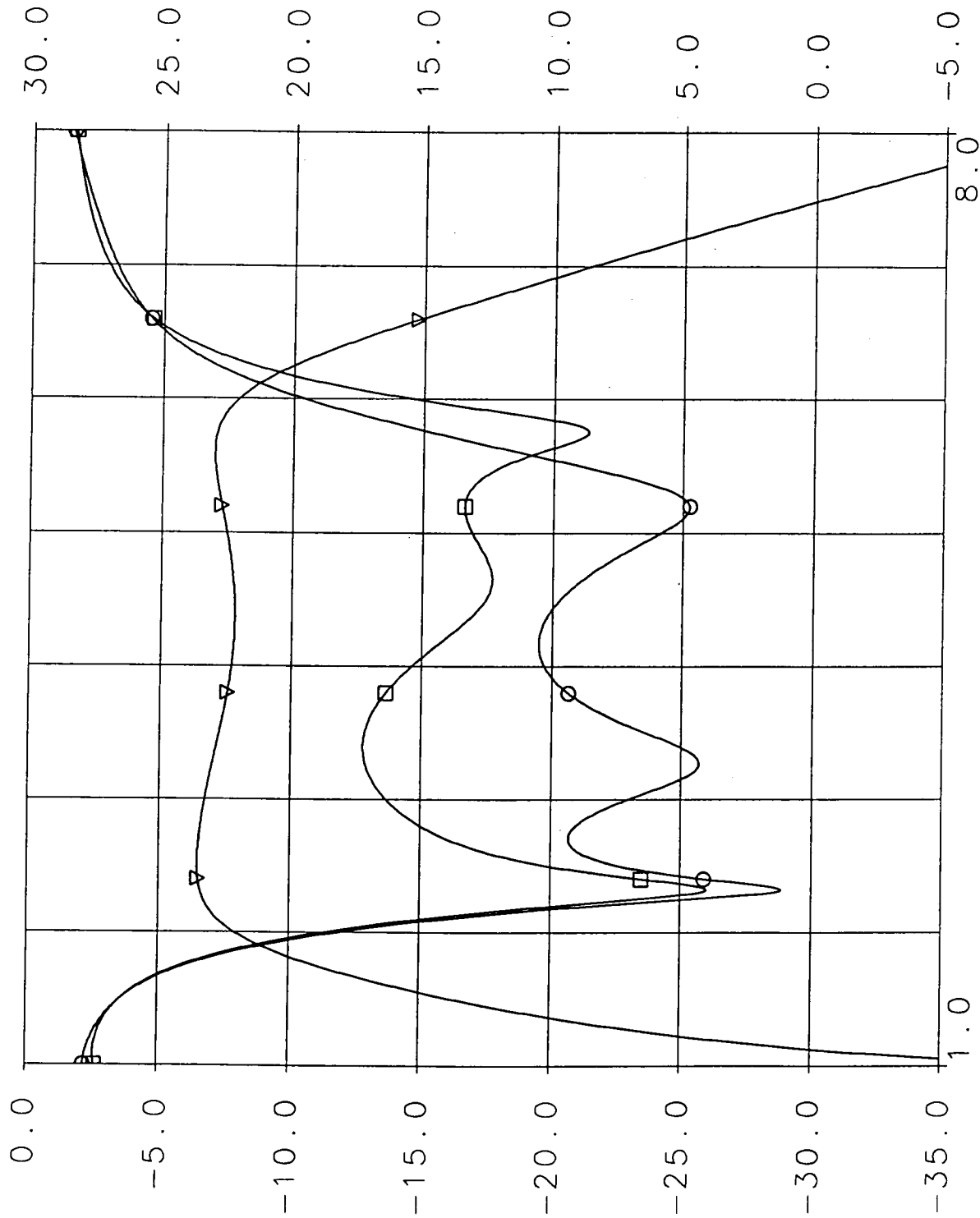


FIG 7:  
NOMINAL

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



FET W/ +10%  
SIZE

FLG 8a:

G FET SIZE +10%

Frequency 1.0 GHz/DIV

□ gfet2out\_tb  
 MU1  
 o llprocess  
 MU1

○ gfet2out\_tb  
 MU2  
 o llprocess  
 MU2

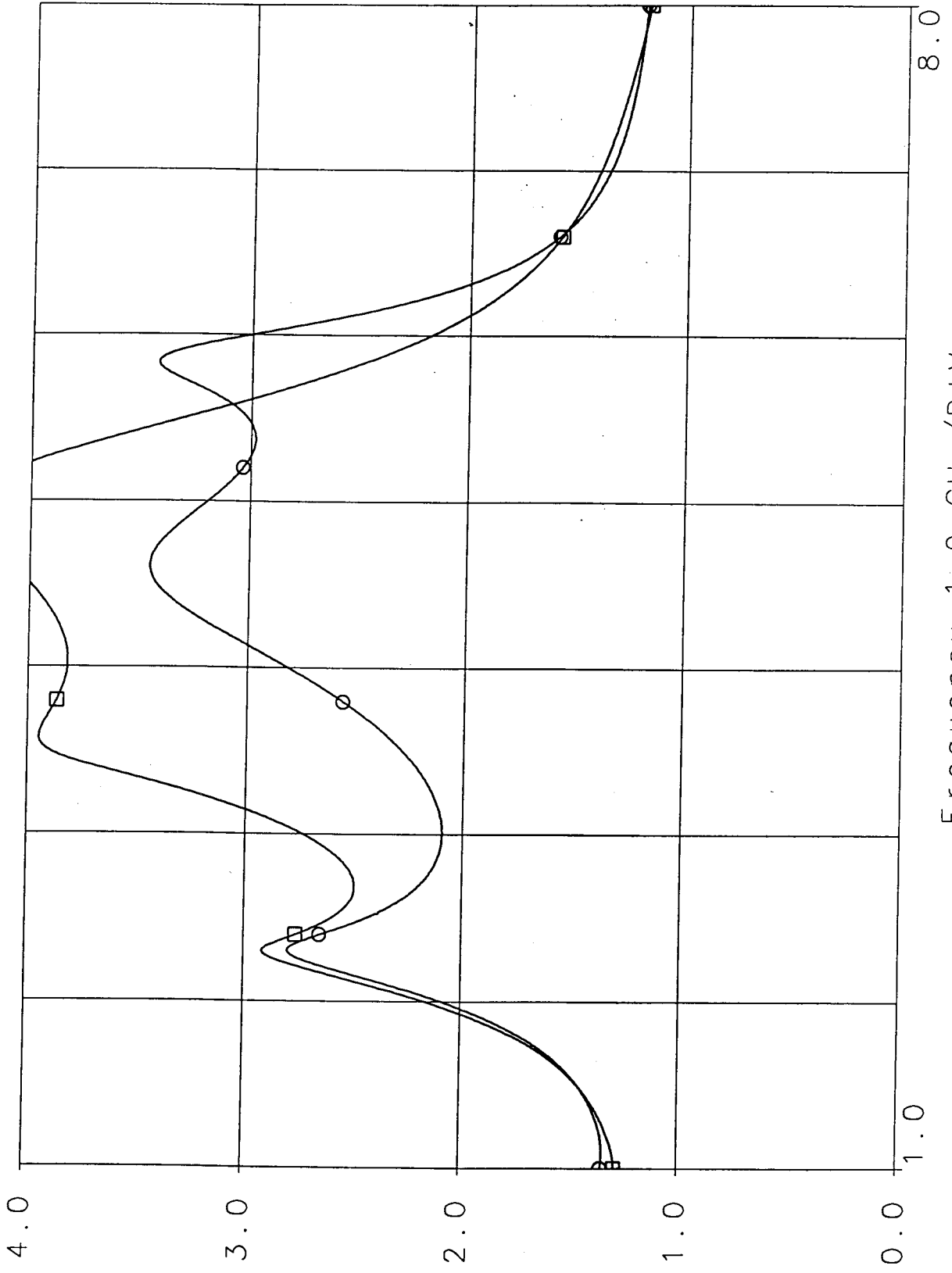


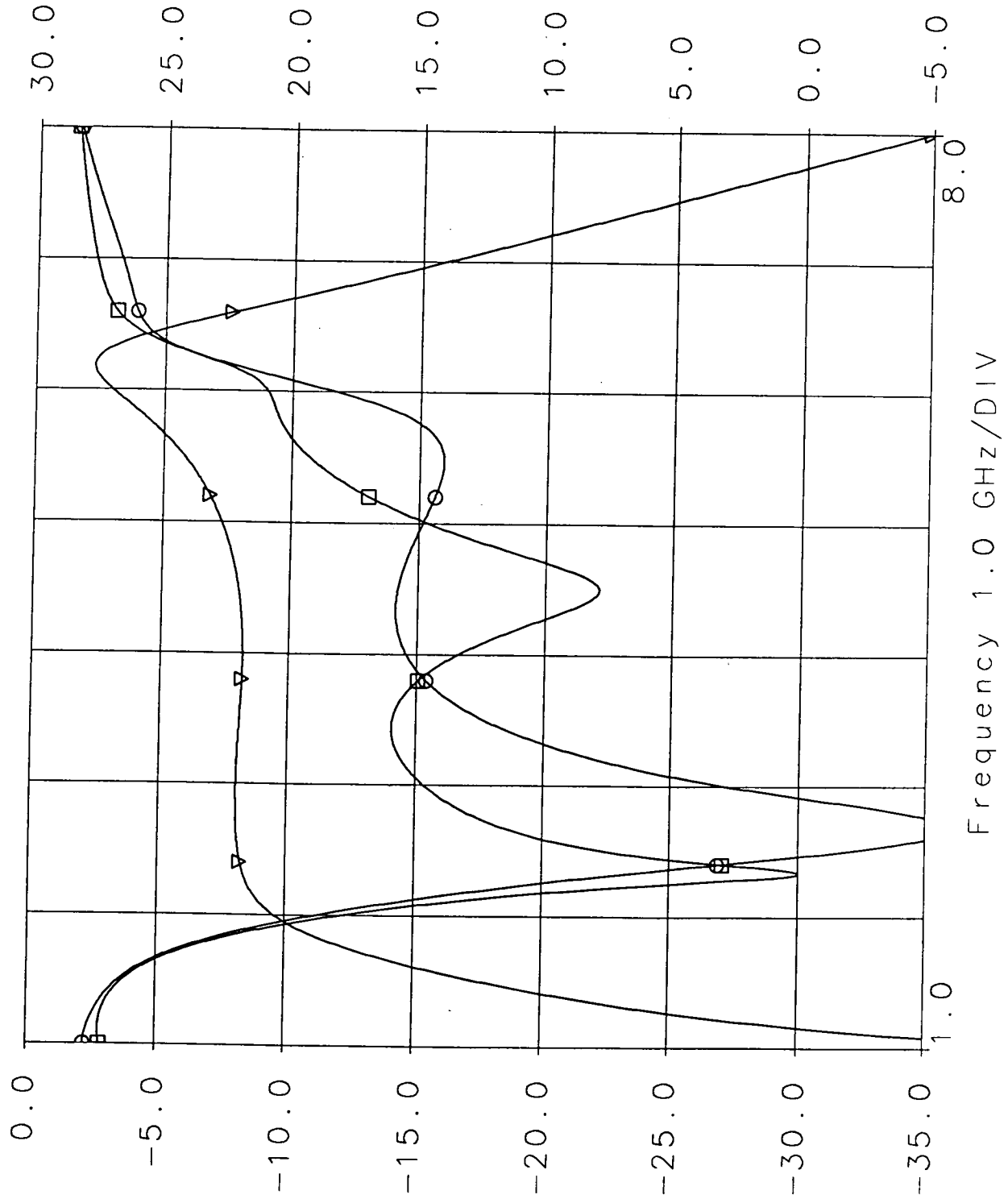
FIG 8a:  
 Gfet size  
 + 10%

Frequency 1.0 GHz/DIV

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB

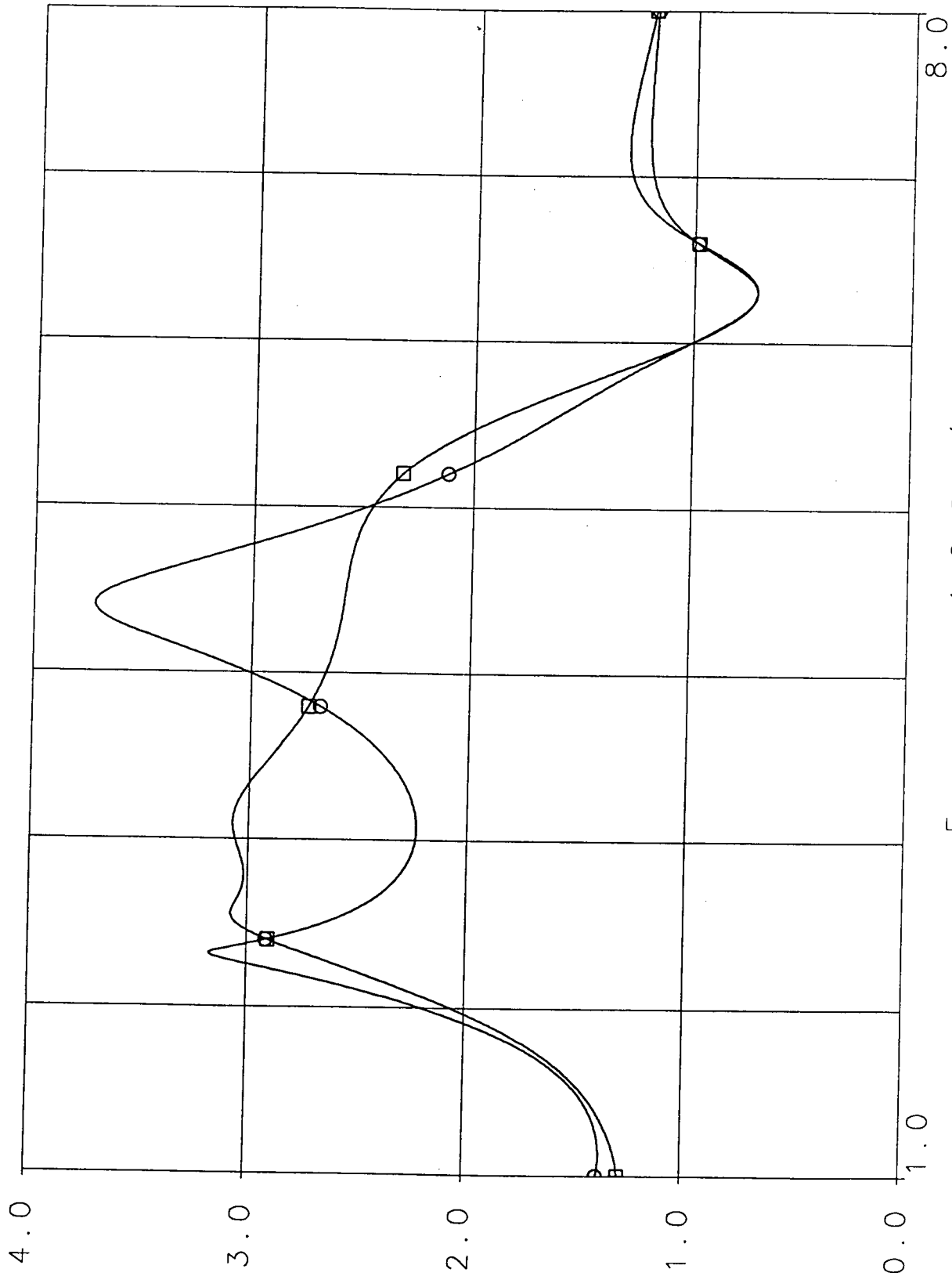


FET size: -10%  
FIG 86:  
GFET SIZE -10%



□ gfet2out\_tb  
MU1  
allprocess  
MU1

○ gfet2out\_tb  
MU2  
allprocess  
MU2



GFET SIZE  
-10%

FIG 86:  
GFET SIZE  
-10%

Frequency 1.0 GHz/DIV

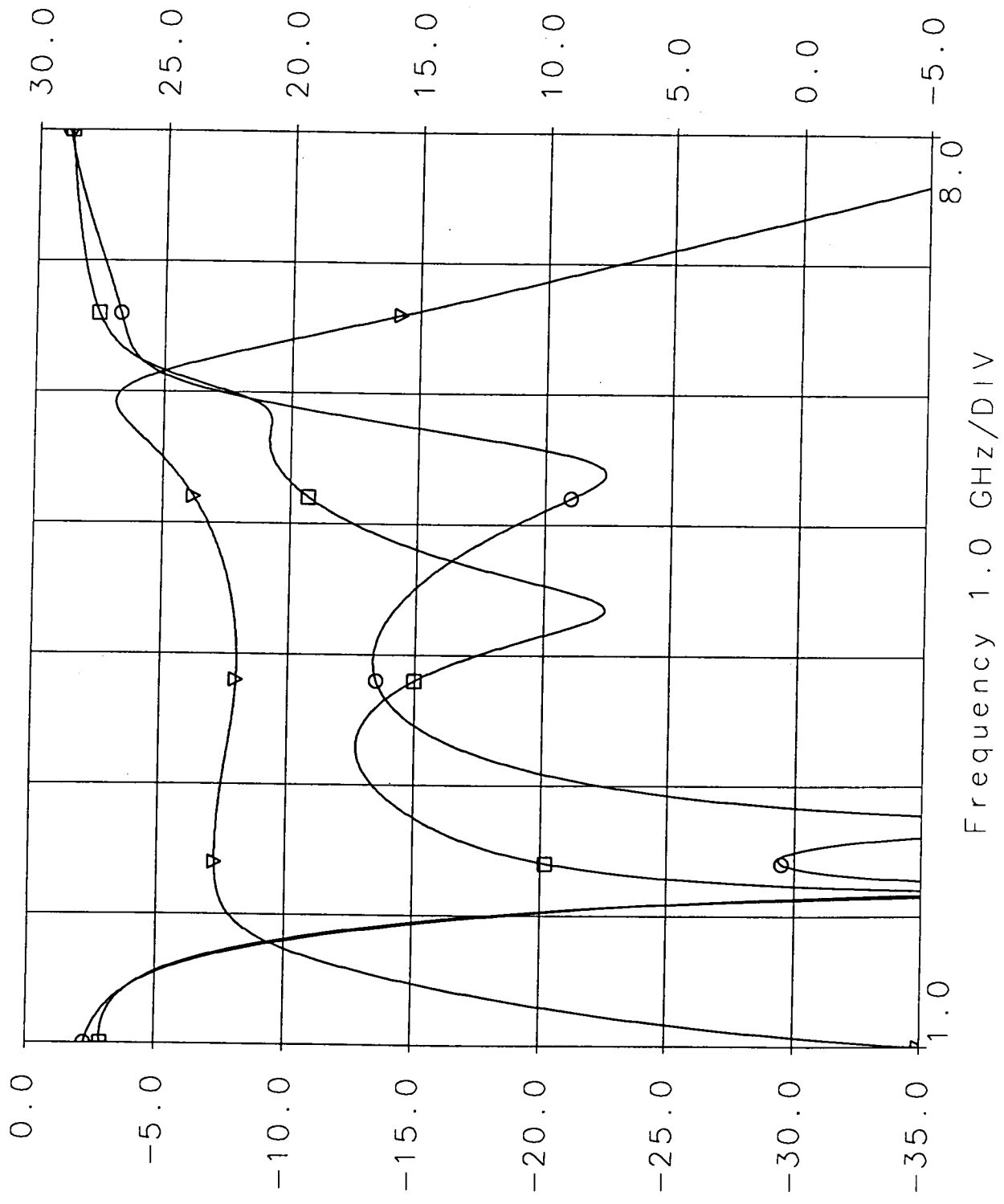
FIGURE 2:  
CAPACITORS  
+15%

C + 15%

□ gfet2out\_tb  
S11  
o11process  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
o11process  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
o11process  
S[2,1]  
dB



□ gfet2out\_tb  
MU1  
allprocess  
MU1

○ gfet2out\_tb  
MU2  
allprocess  
MU2

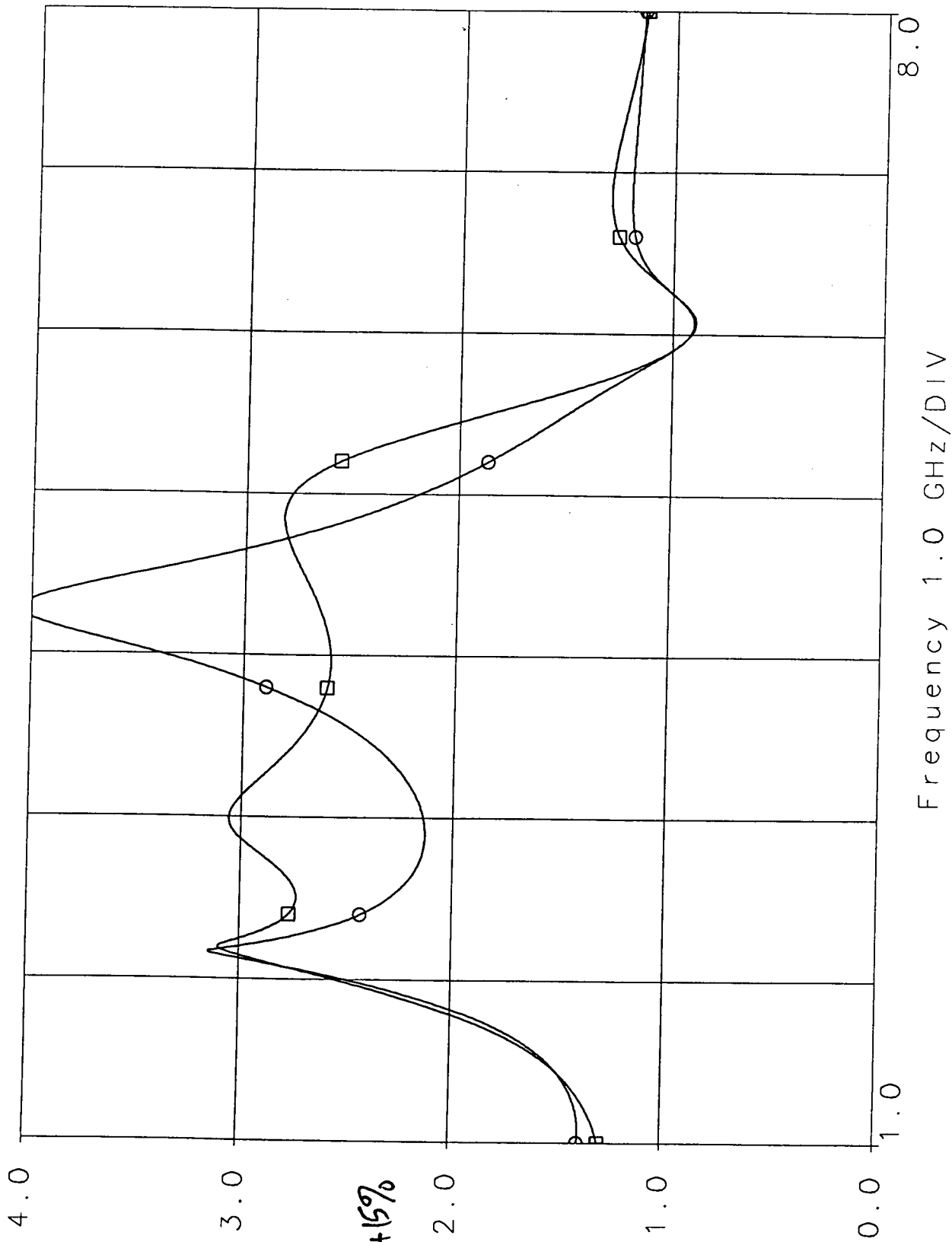


FIGURE 9a:  
CAPACITORS +15%

C +15%

Frequency 1.0 GHz/DIV

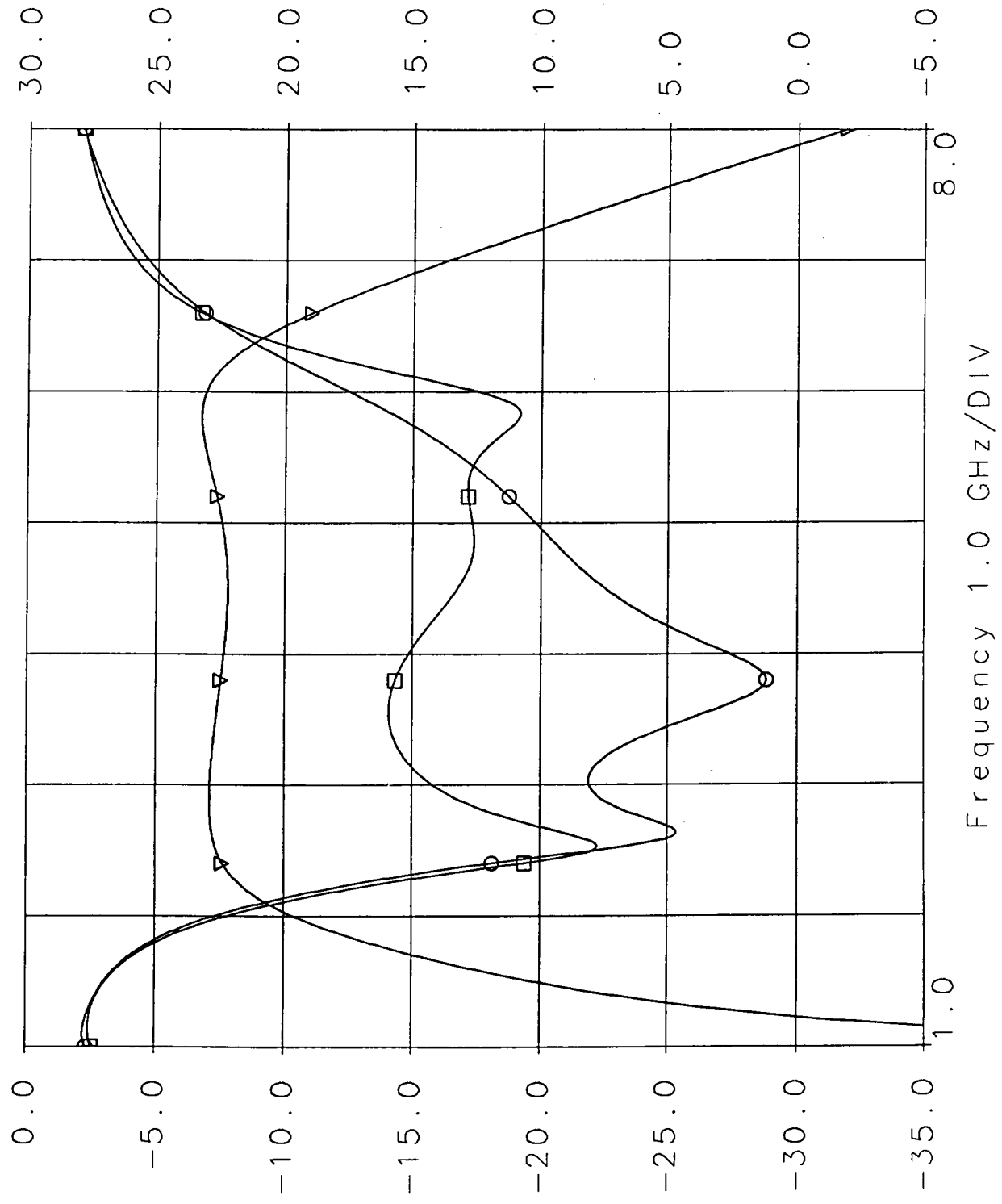
C-15%

FIGURE 96:  
CAPACITORS  
-15%

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



C-15

○ gfet2out\_tb  
MU2  
allprocess  
MU2

□ gfet2out\_tb  
MU1  
allprocess  
MU1

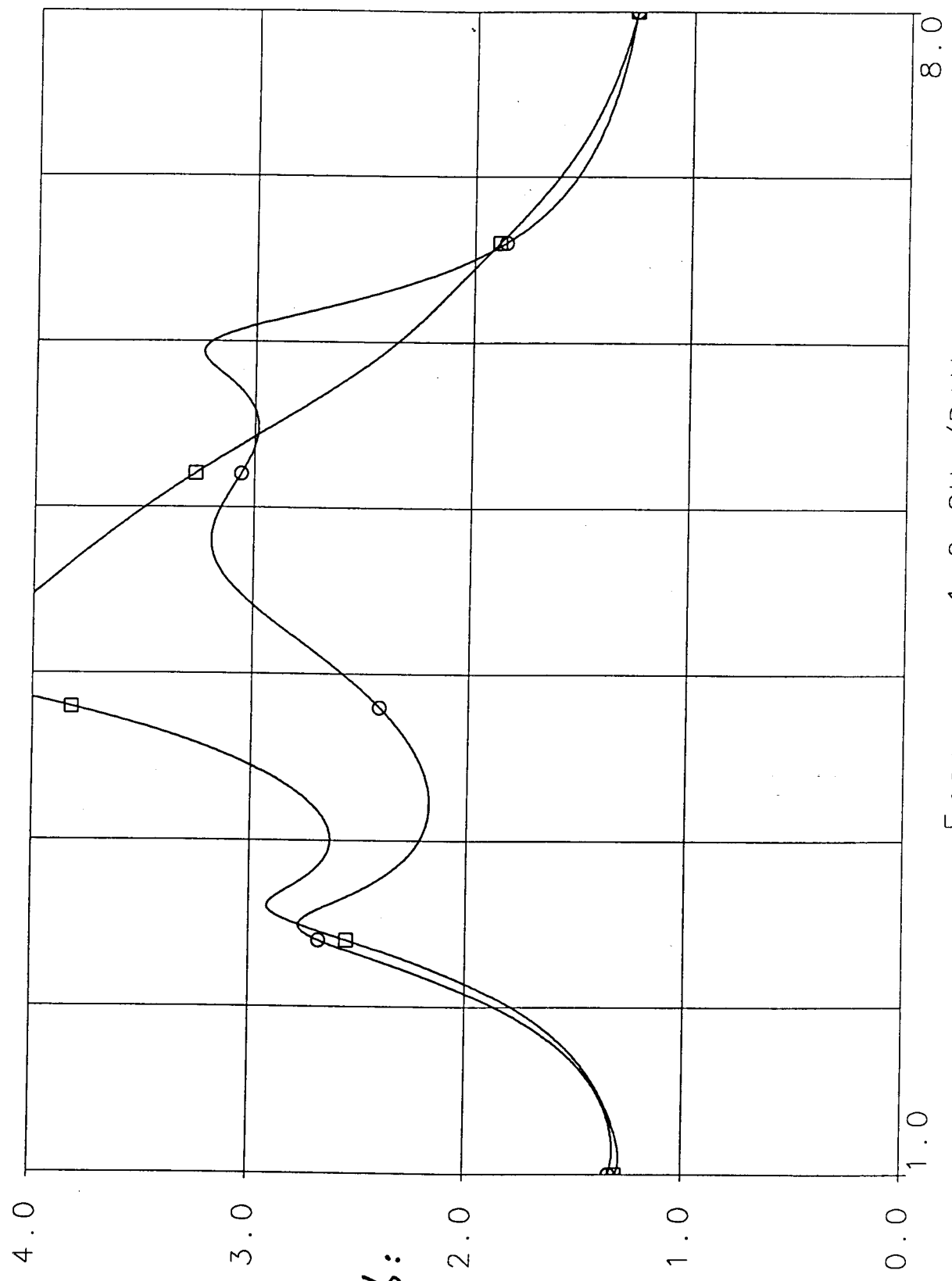


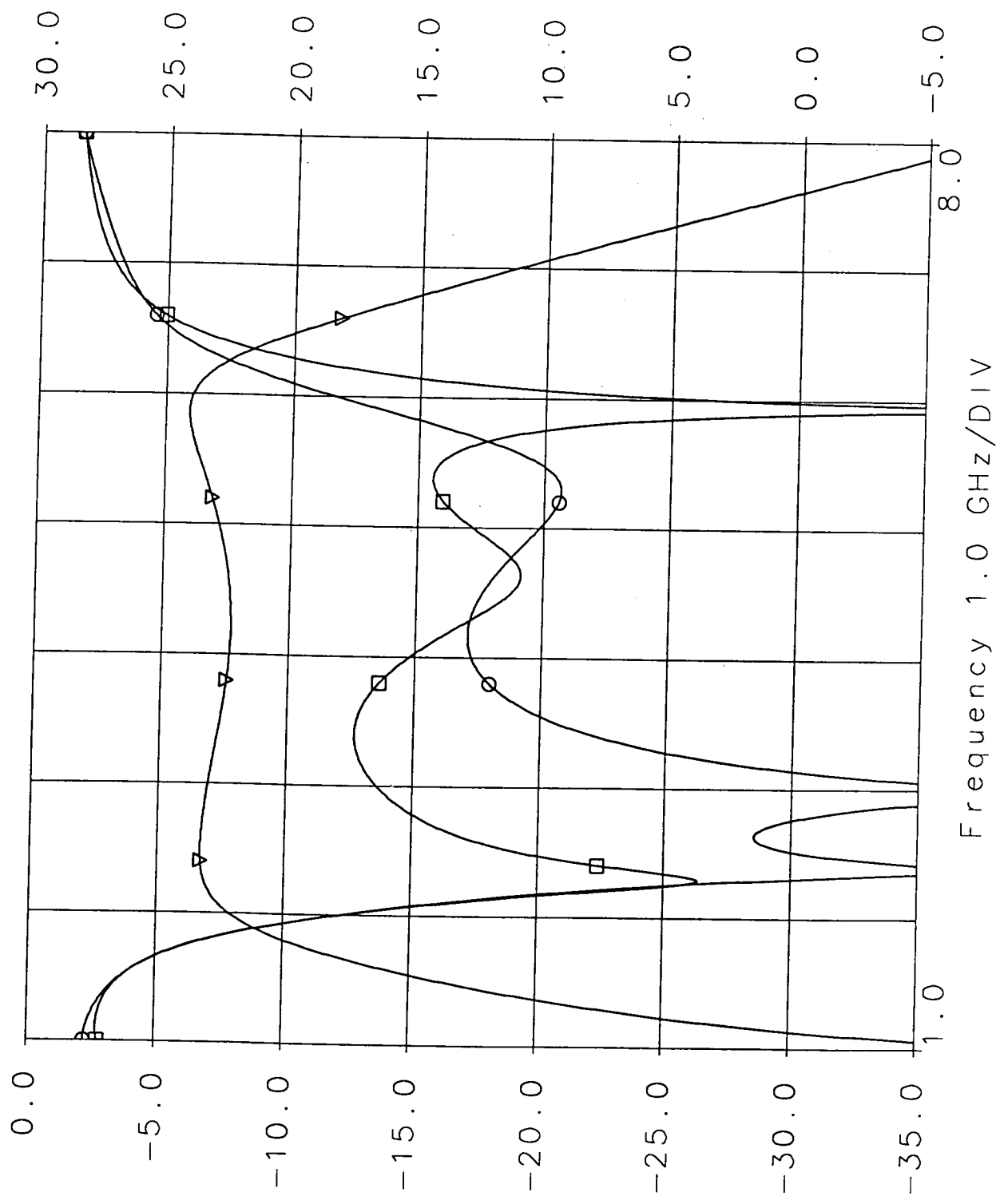
FIGURE 9b:  
CAPACITORS  
-15%

Frequency 1.0 GHz/DIV

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



FLANGE (Q:  
R\_NCR + 7%  
R + 1%  
NCR

□ gfet2out\_tb  
MU1  
o1lprocess  
MU1

○ gfet2out\_tb  
MU2  
o1lprocess  
MU2

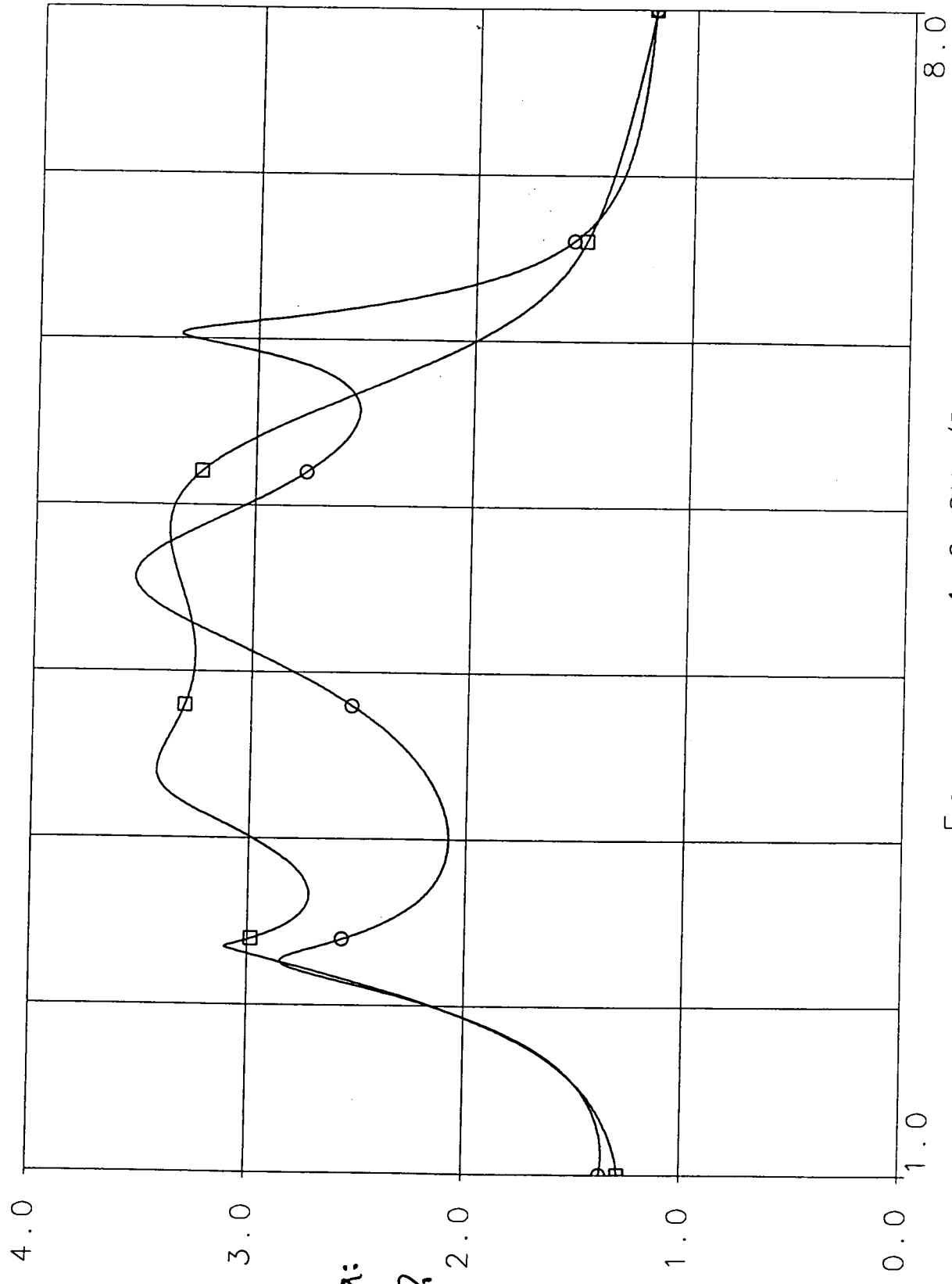


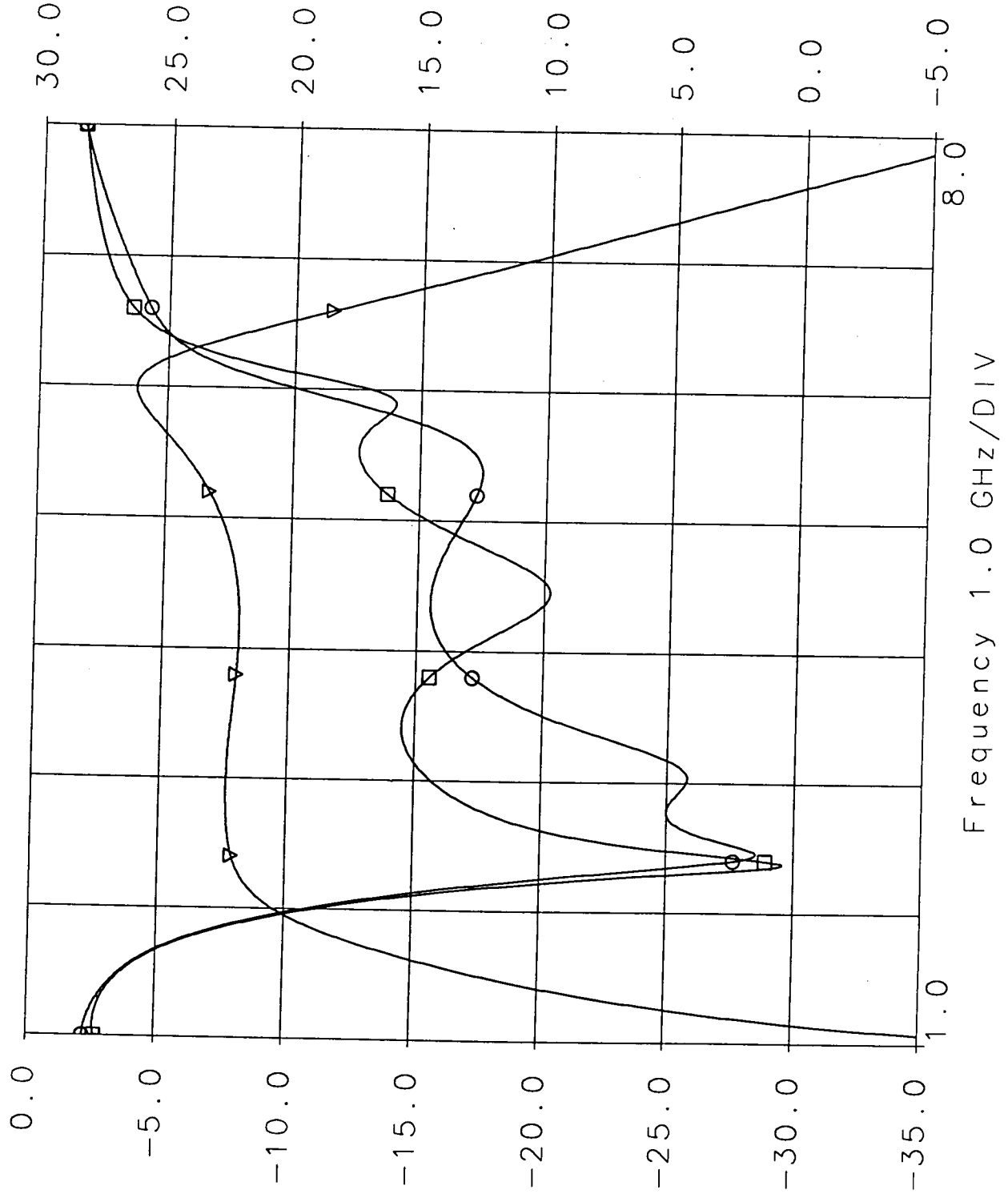
FIGURE 10a:  
RNG + 7%

$\beta + 7\%$   
NIR

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



R -19%  
N=6  
FIGURE 106:  
RNG -7%



□ gfet2out\_tb  
MU1  
o11process  
MU1

○ gfet2out\_tb  
MU2  
o11process  
MU2

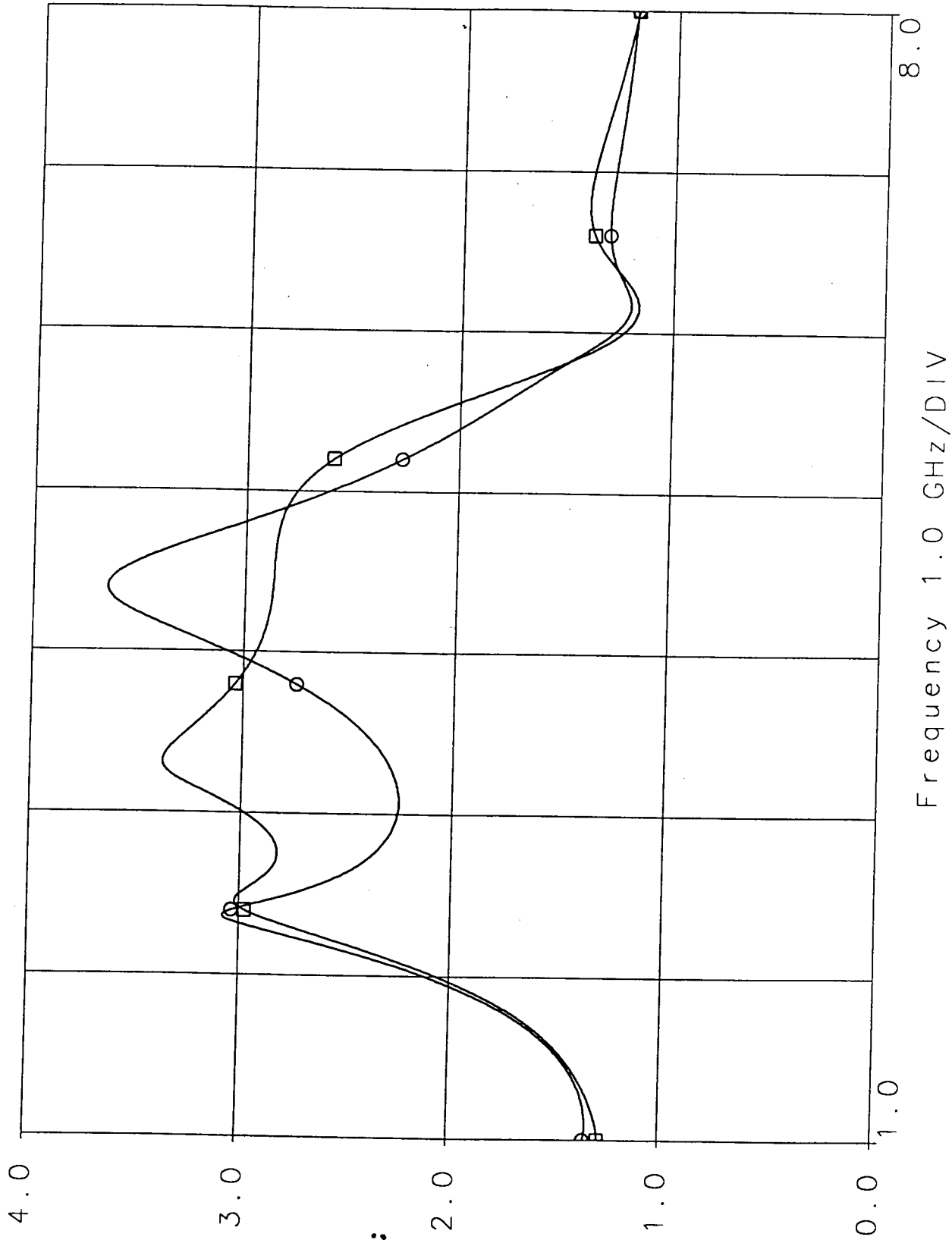


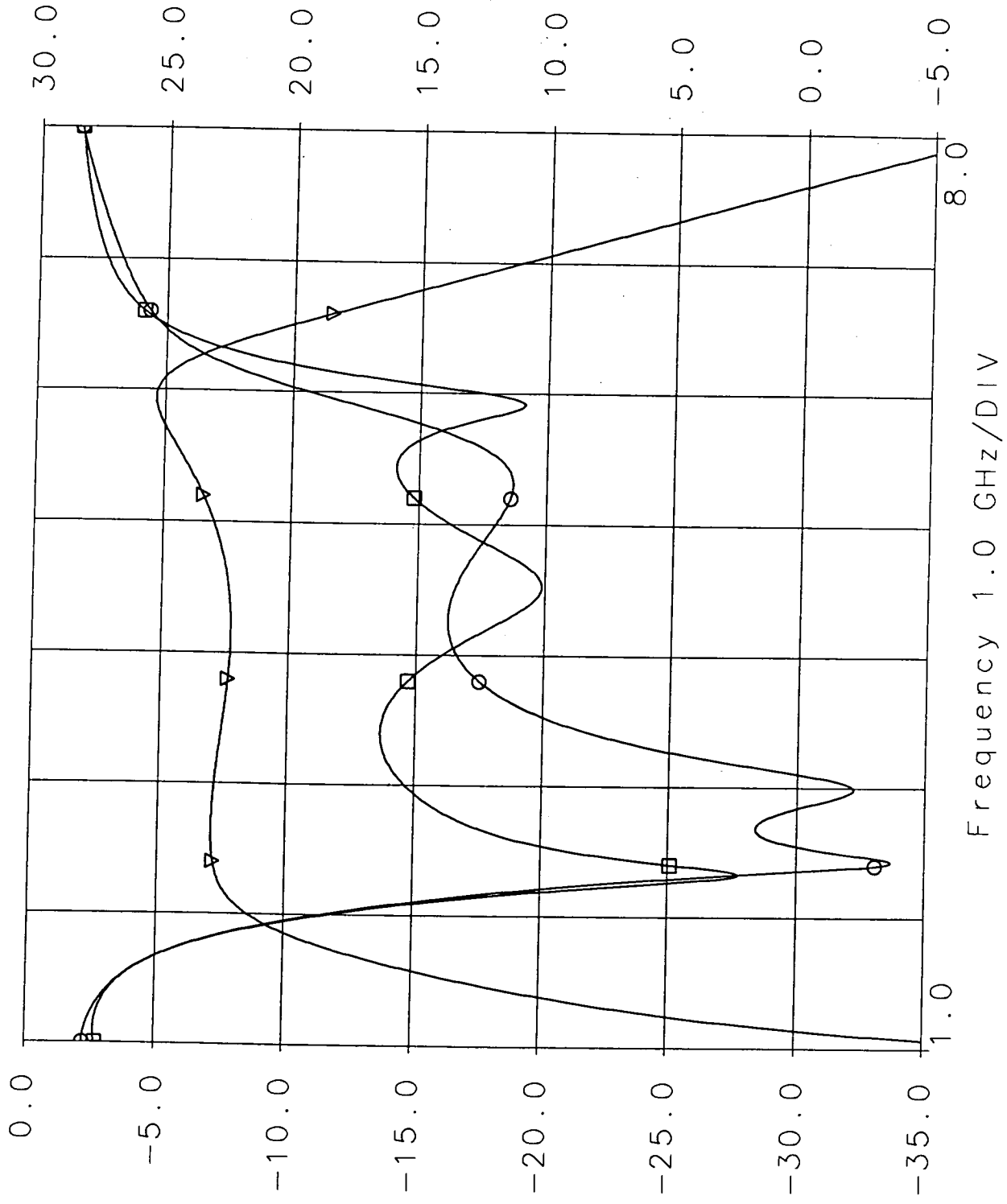
FIGURE 10b:  
R<sub>MSR</sub> - 7%

R<sub>MSR</sub> - 7%

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



□ gfet2out\_tb  
MU1  
allprocess  
MU1

○ gfet2out\_tb  
MU2  
allprocess  
MU2

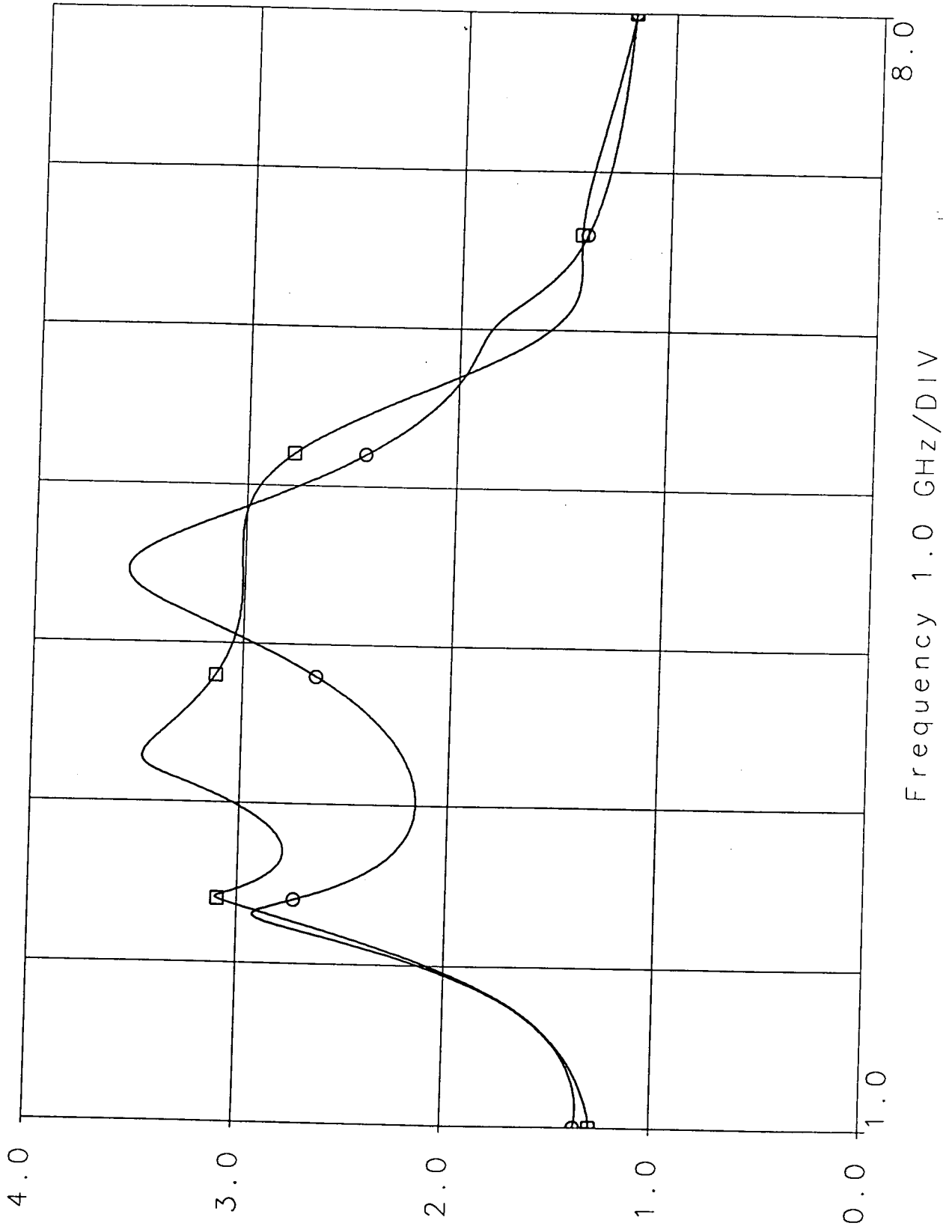


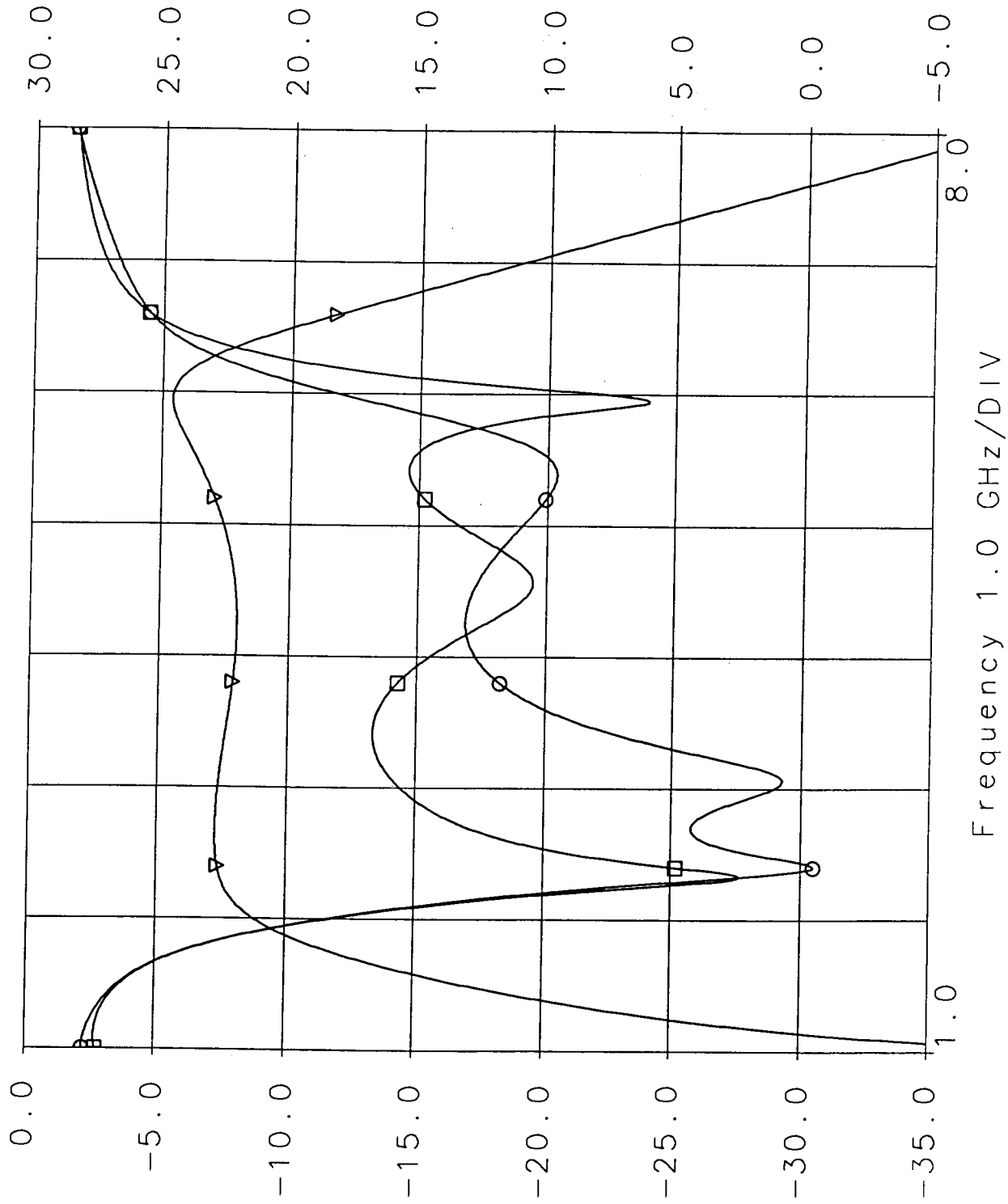
FIGURE 1/9:  
RNT 10%

RNT 10%

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



R - 20%

FIGURE 116:  
R<sub>N</sub> - 20%

□ gfet2out\_tb  
MU1  
o1lprocess  
MU1

○ gfet2out\_tb  
MU2  
o1lprocess  
MU2

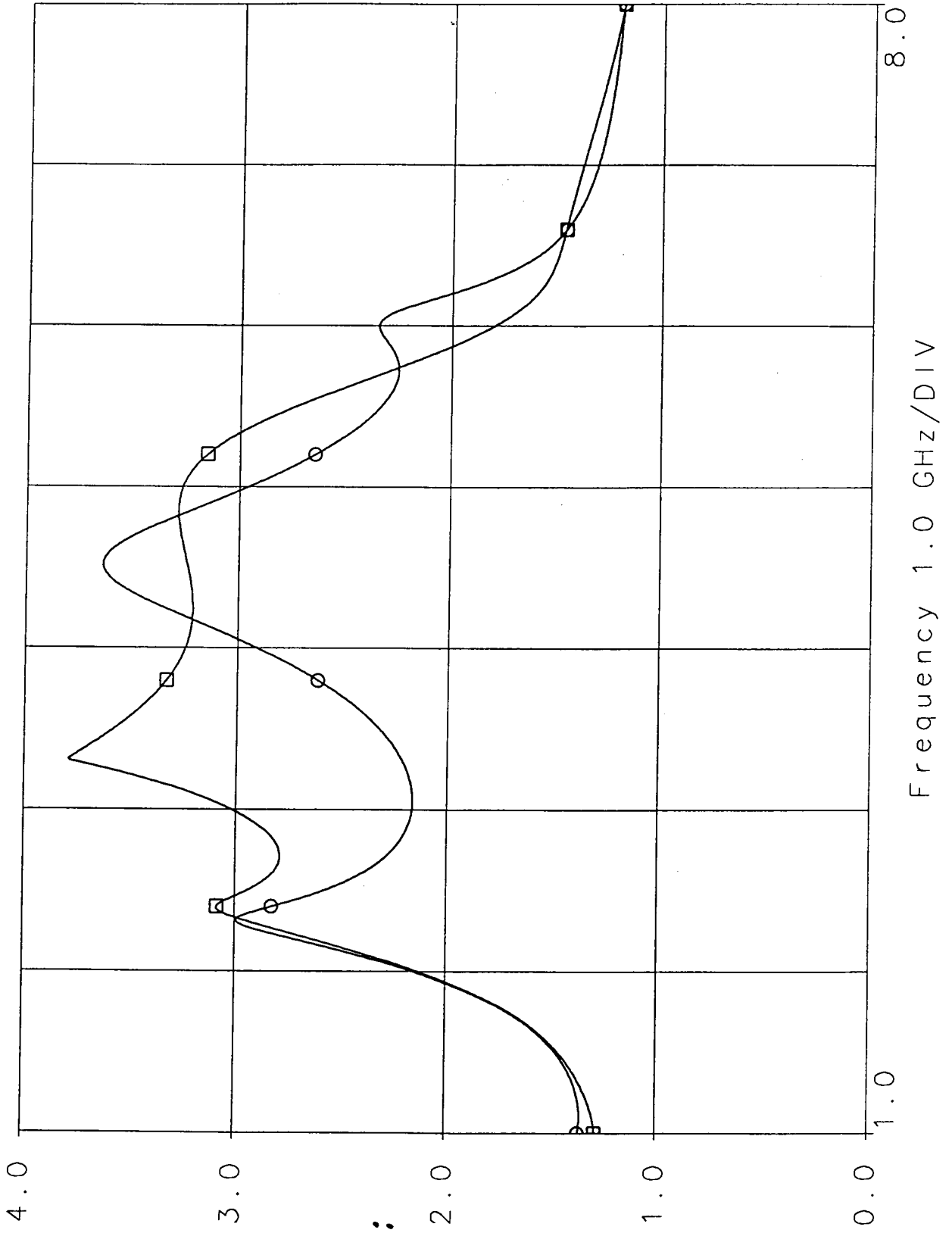


Figure 11b:  
R<sub>nt</sub> - 20%

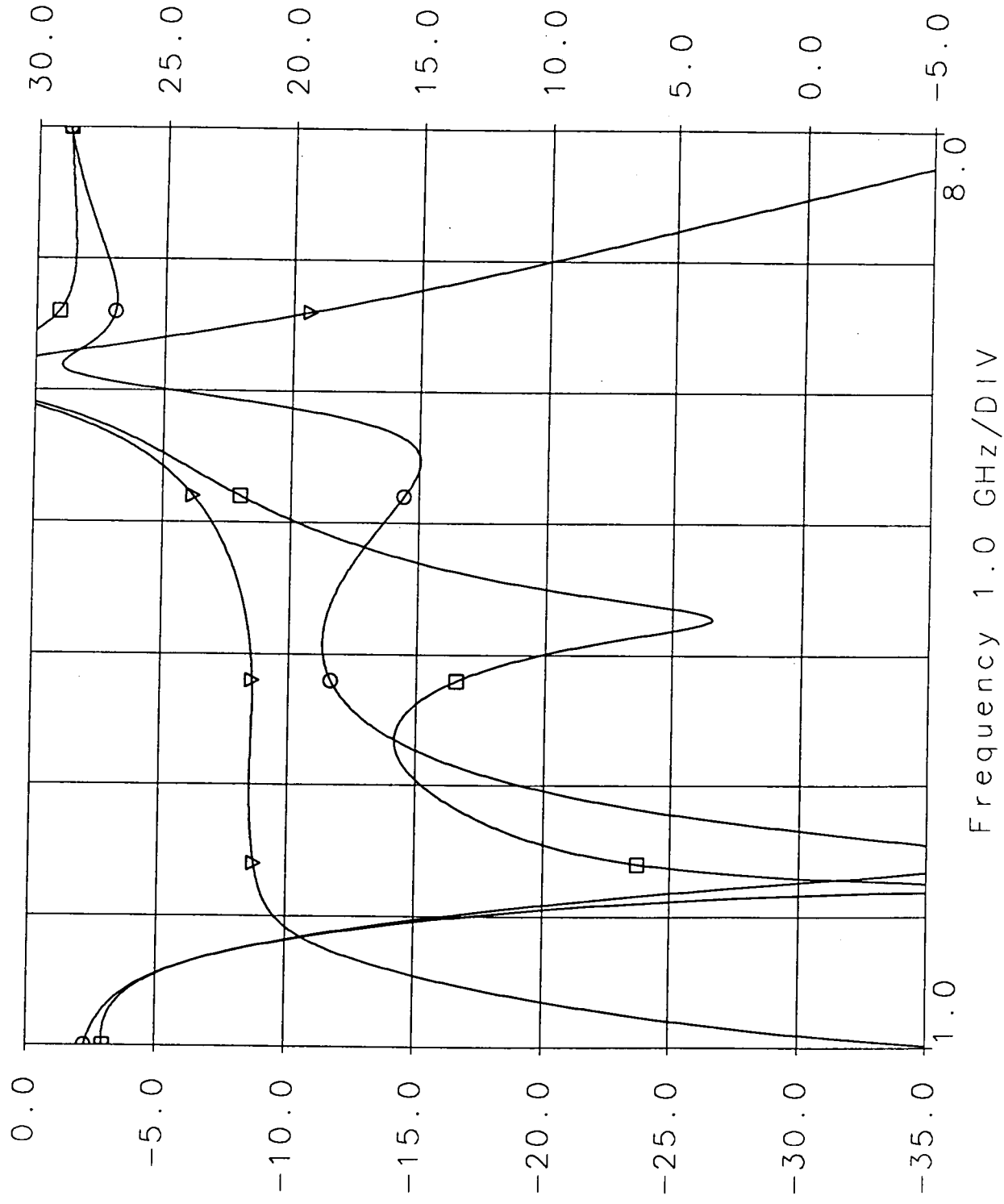
R<sub>nt</sub> - 20%

Frequency 1.0 GHz/DIV

□ gfet2out\_tb  
S11  
allprocess  
S[1,1]  
dB

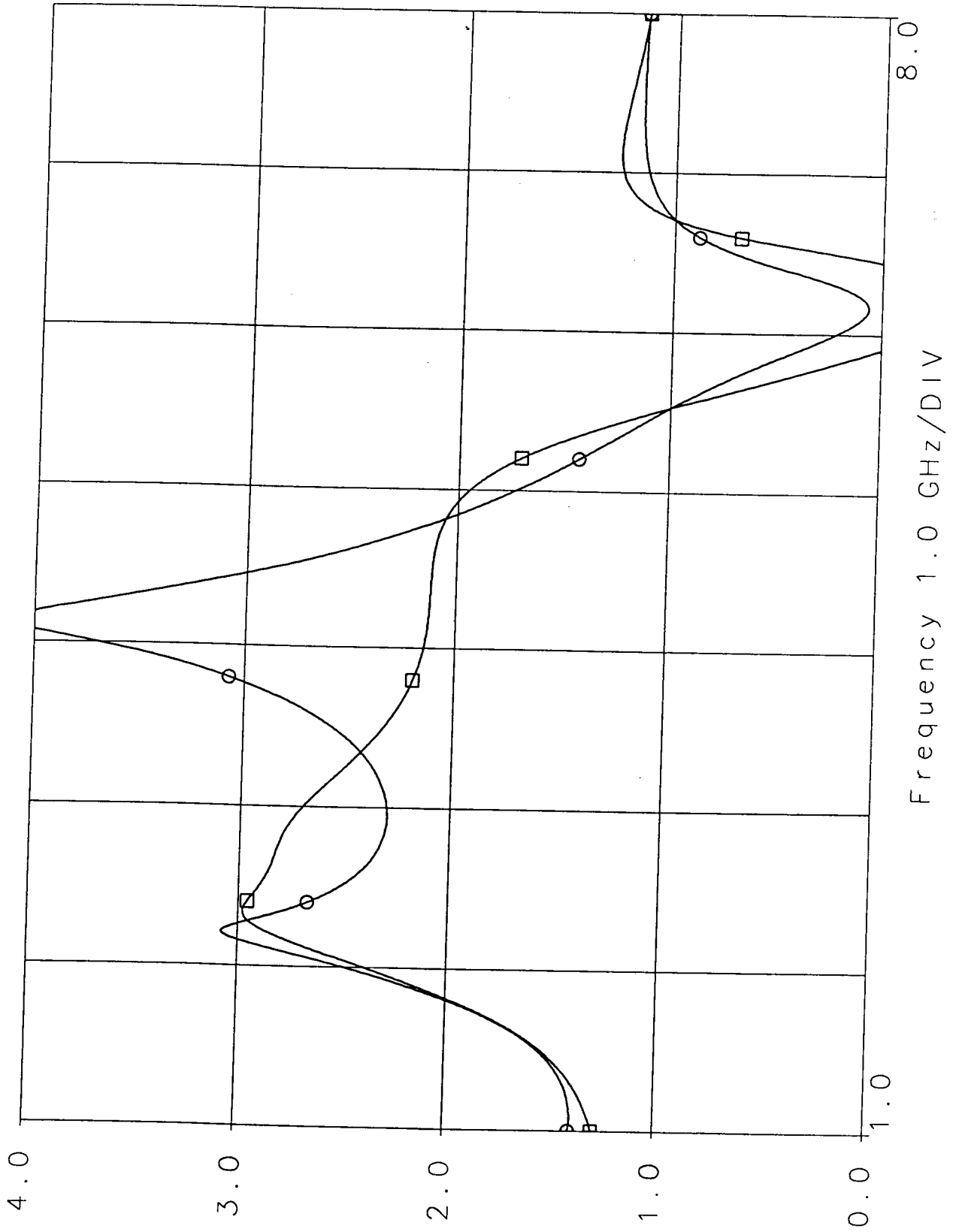
○ gfet2out\_tb  
S22  
allprocess  
S[2,2]  
dB

▽ gfet2out\_tb  
S21  
allprocess  
S[2,1]  
dB



□ gfet2out\_tb  
 MU1  
 o11process  
 MU1

○ gfet2out\_tb  
 MU2  
 o11process  
 MU2



*Worst Case Results*

FIG 12:  
WORST  
CASE





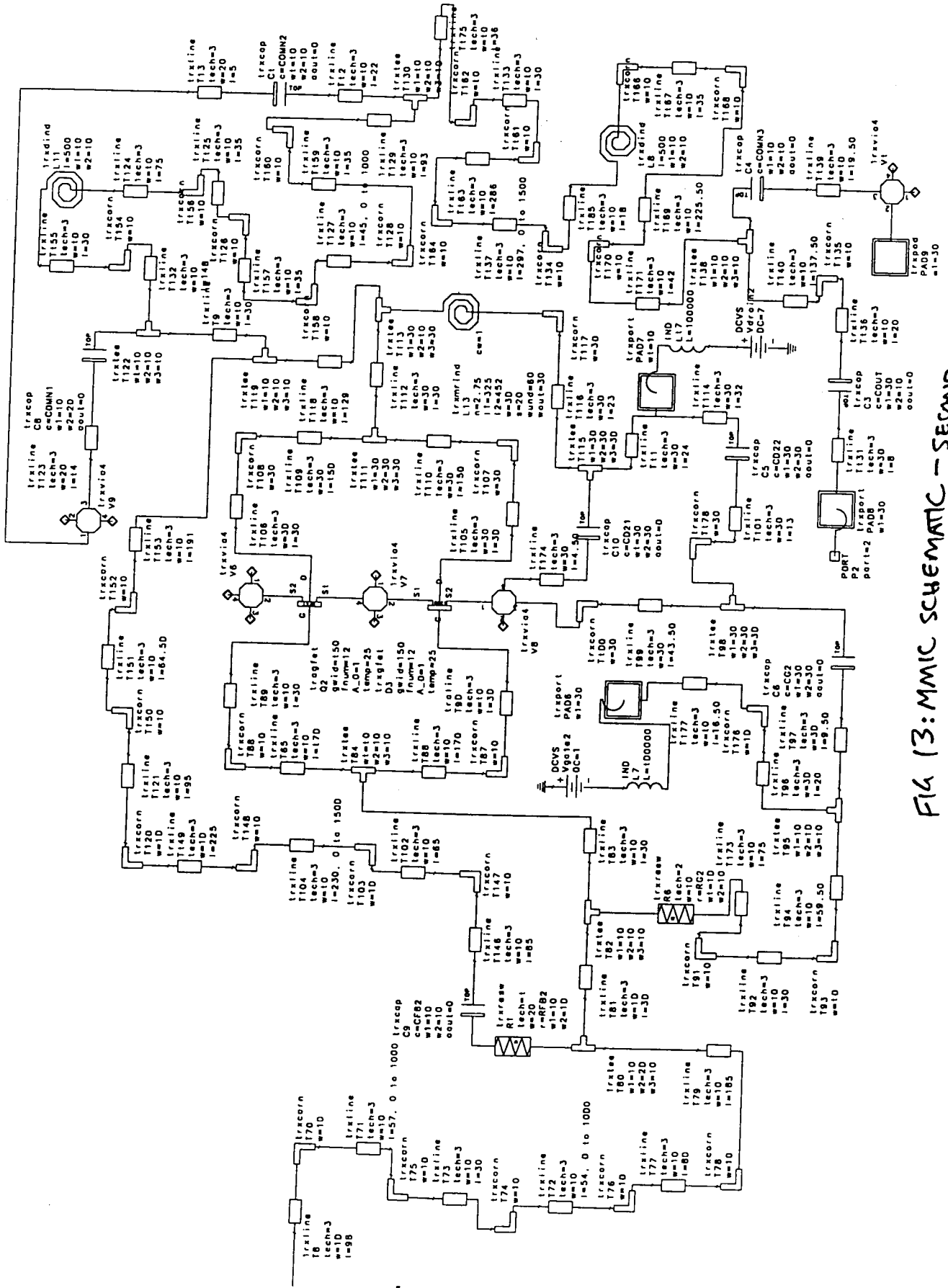
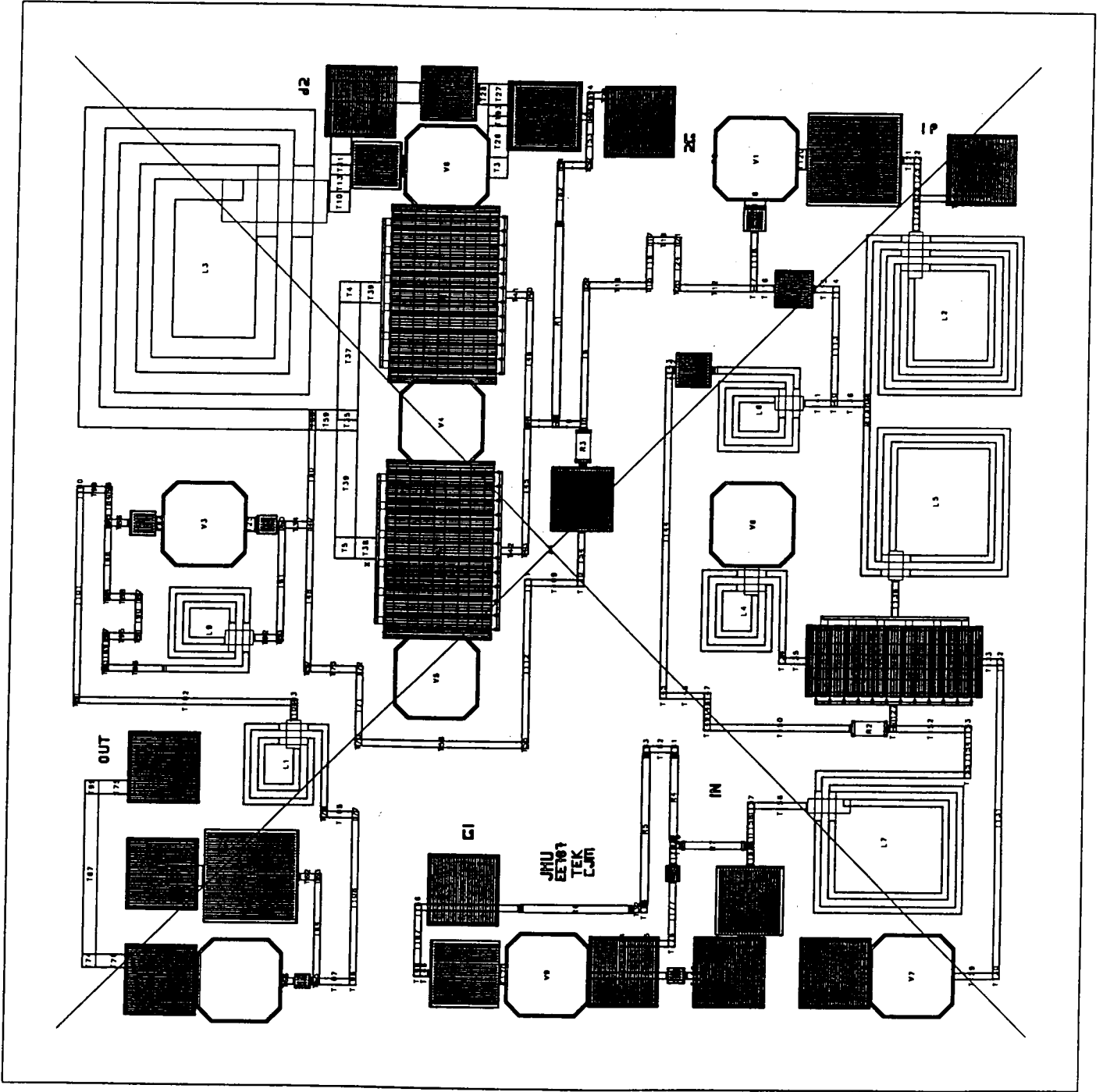


FIG 13: MMIC SCHEMATIC - SECOND STAGE  
*all process*

FIG 14:  
MMIC  
LAYOUT



alltofit

FIGURE 15:  
25GHz POWER  
GAIN

□ inpwr\_tb  
PTin  
allprocess  
PT  
dBm

○ inpwr\_tb  
PTout  
allprocess  
PT  
dBm

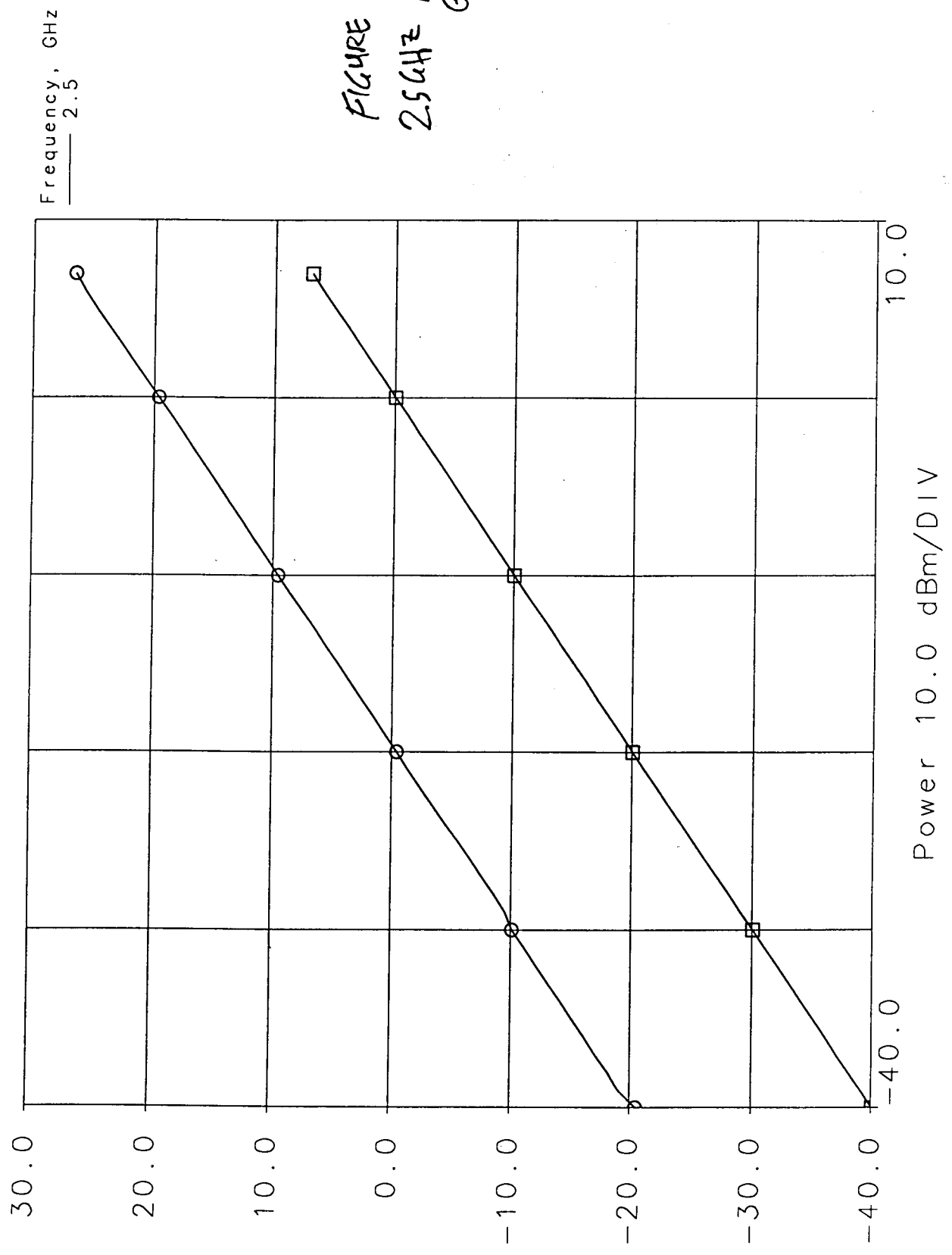
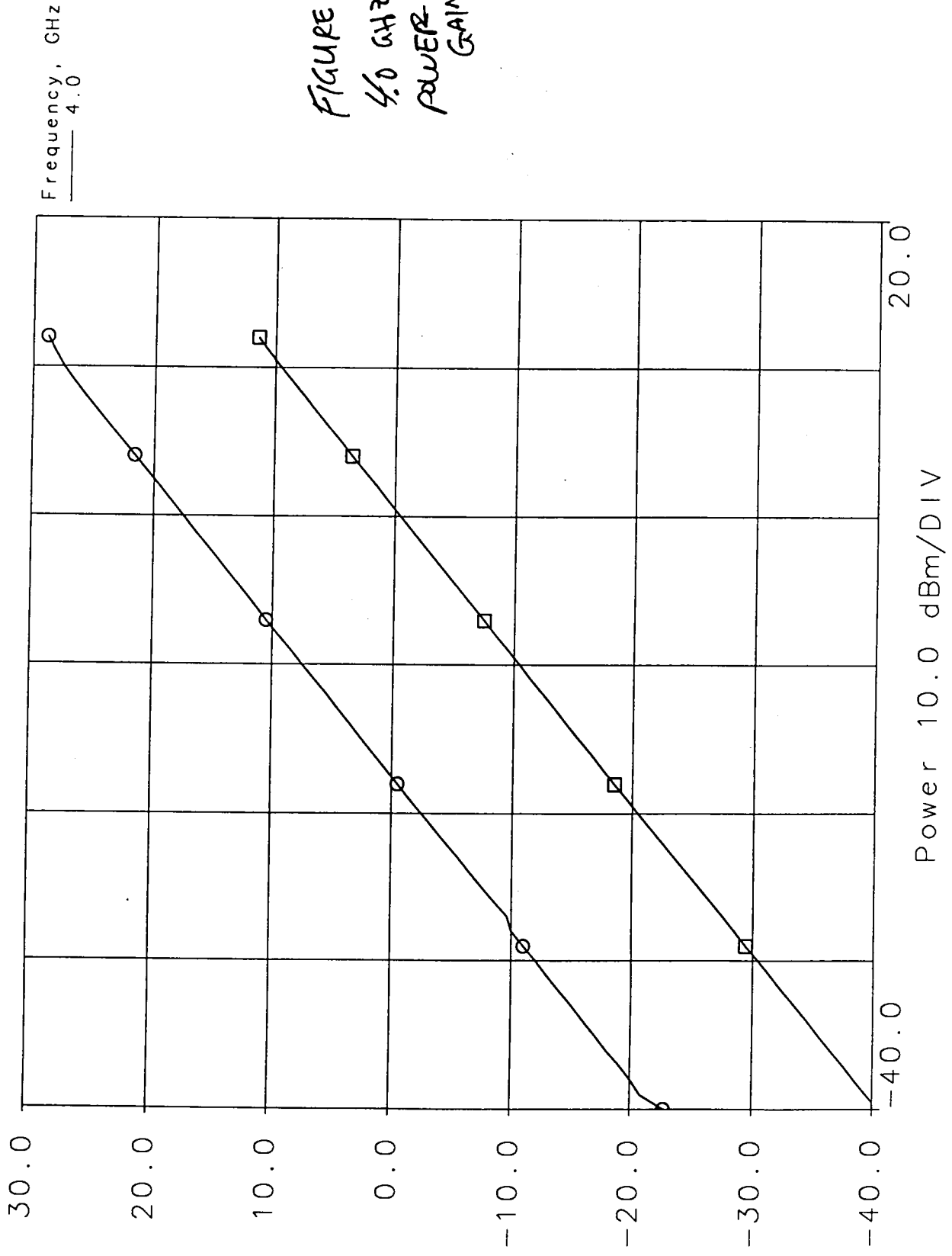


FIGURE 16:  
4.0 GHz  
POWER  
GAIN

□ inpwr\_tb  
PTin  
allprocess  
PT  
dBm

○ inpwr\_tb  
PTout  
allprocess  
PT  
dBm



□ inpwr\_tb  
PTin  
allprocess  
PT  
dBm

○ inpwr\_tb  
PTout  
allprocess  
PT  
dBm

Frequency, GHz  
5.0

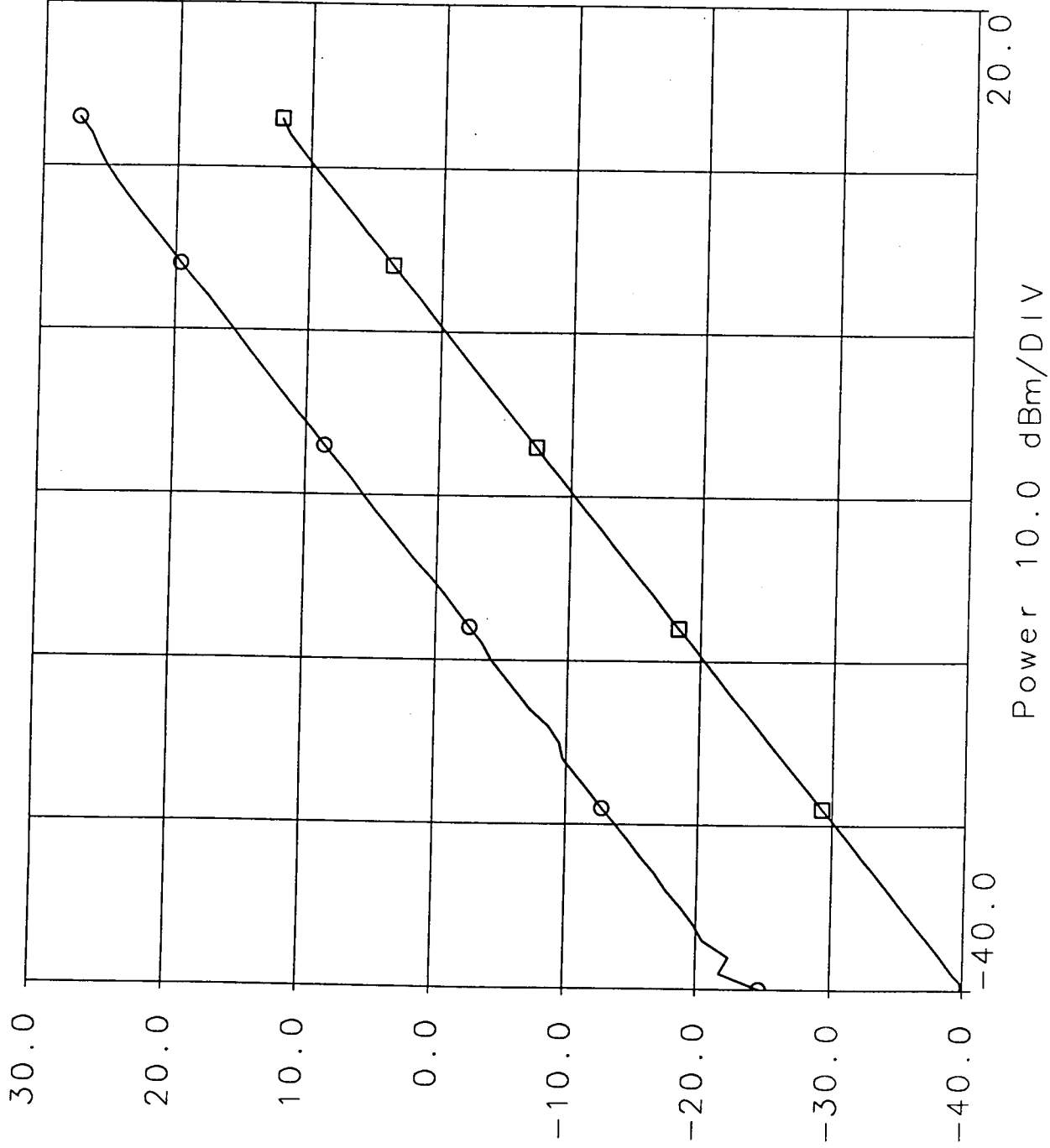
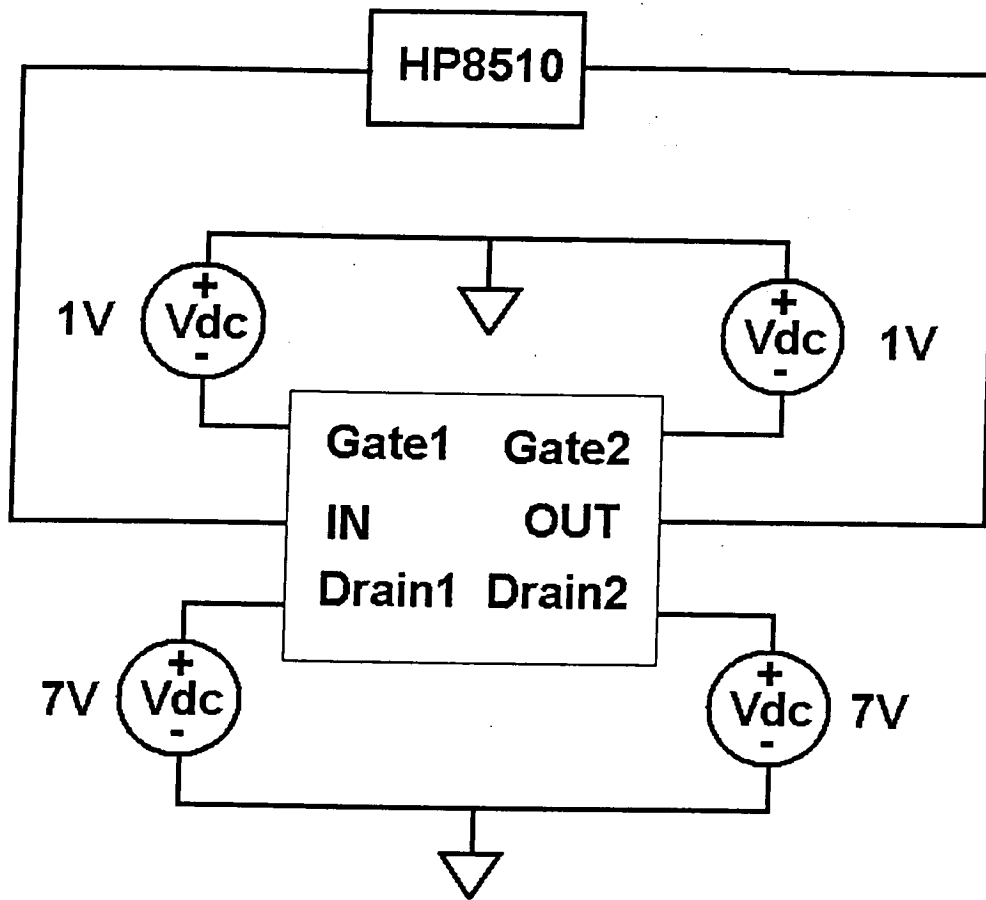


FIGURE 17:  
5.0 GHz  
POWER  
GAIN



**Test Setup**

*FIGURE 18: TEST SETUP*



# C-Band Power Amplifier

*Designed & Presented By:*

David Cross  
Chad Wilson

12/14/98

For: John Penn & Craig Moore  
525.787 MMIC Design



## Summary:

Our fundamental task was to design a C-band Power amplifier with a minimum of 0.5 Watt output power from 4.5-6 GHz using the Triquint TRX process. Desired performance was 1 Watt out from 2-6 GHz. Other key parameters that were specified (see performance compliance matrix) include input and output match, gain, and power added efficiency. Requirements were not provided for noise figure, constant gain (over frequency) or constant 1dB compression points. Additional physical constraints included a +9V maximum supply voltage and a fixed chip size of 60x60 mils. All bias networks and matching networks were required to be on-chip. As for the active devices, there were choices of DFET or GFET devices.

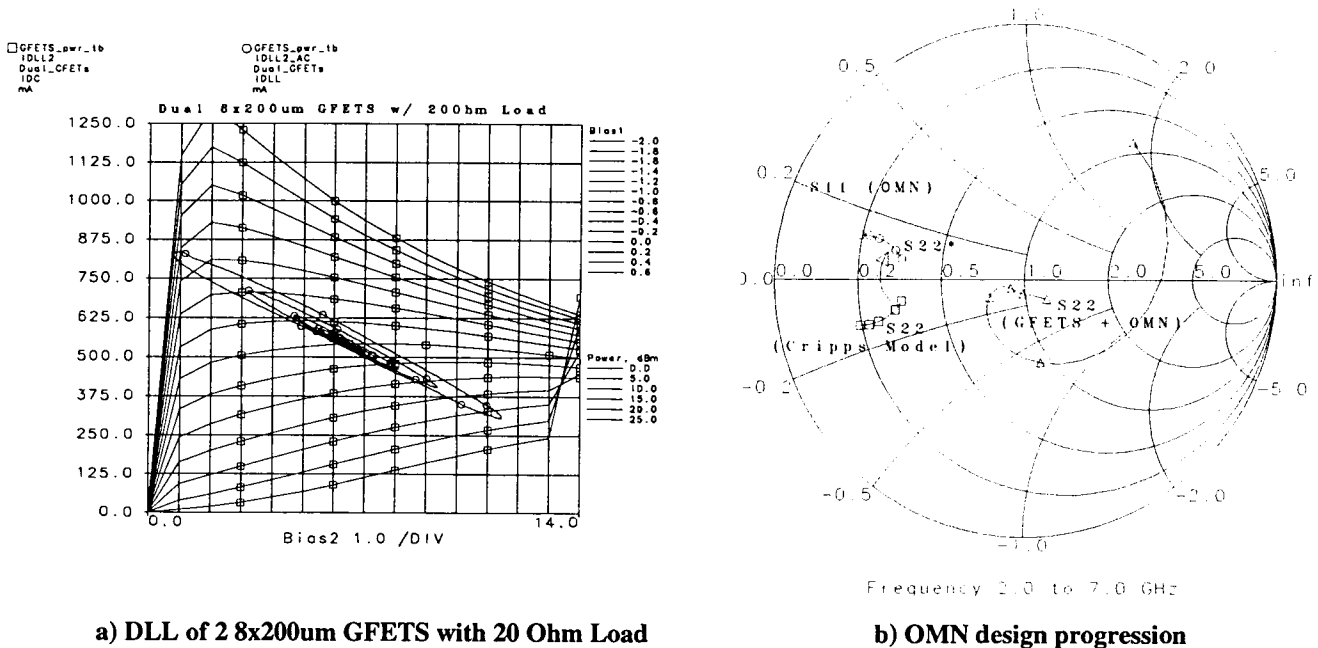
Early in the design process we made the decision to design an amplifier with at least 0.75 Watt output power from 3-6 GHz. A usable die area of 50x50 mils proved to be the most limiting factor in the design. Some bandwidth was sacrificed to allow matching networks of reasonable size to be constructed. The relatively low breakdown voltage of the GFET (approximately 15 V) necessitated a low 6.5V drain voltage which prevented a design yielding 1W across the entire 2-6 GHz band.

## Design Philosophy:

The first step in the power amplifier design process is to design the power stage. This requires choosing a device type and sizing it to operate at an appropriate bias point for the desired output power. We chose the GFET device because it is optimized for higher currents and, thus, more power. The power out is a function of allowable voltage and current swings along a particular load line. The voltage swing is determined by choosing a bias point and is limited by turn-on and breakdown voltages, which, for the GFET, are around 1V and 15V, respectively. This means that maximum voltage swing would be about 14V (for a bias of 8V). The current swing is determined by the load impedance but is limited by device size. Lower impedances create very large current swings (and in accordance, higher power) but are tougher to match to 50 Ohms in a broadband design. In addition, the nonlinear modeling of the device proved to be flawed for too low of impedance levels. For large values of gate voltage, where the load line entered the knee area just above the triode region, the I-V curves started to bend back on themselves and caused non-convergence issues in the model. Therefore, we chose a slightly higher than optimum load and sized the device a bit larger than actually required. It made the modeling more practical and the design a bit easier. We selected two 8x200  $\mu\text{m}$  (1.6mm) devices in parallel.

We used the Cripps method to design our power stage. The Cripps method concentrates on developing an output matching network (OMN) which transforms the system characteristic impedance (in our case 50 Ohms) to a load which maximizes power out of the amplifier. Initially taking an OMN with ideal elements, nonlinear models predicted output power approaching 1W (30dBm) at < 1dB compression. It turned out that we chose a moderate impedance level (20 Ohms) which happened to be very close to that of our device output. Figure 1a shows the dynamic load line. What that means is that not only should we get very good power out, but the OMN should provide good

output match as well! Figure 1b shows the progression of the OMN as well as the final output match of the OMN & GFETs.



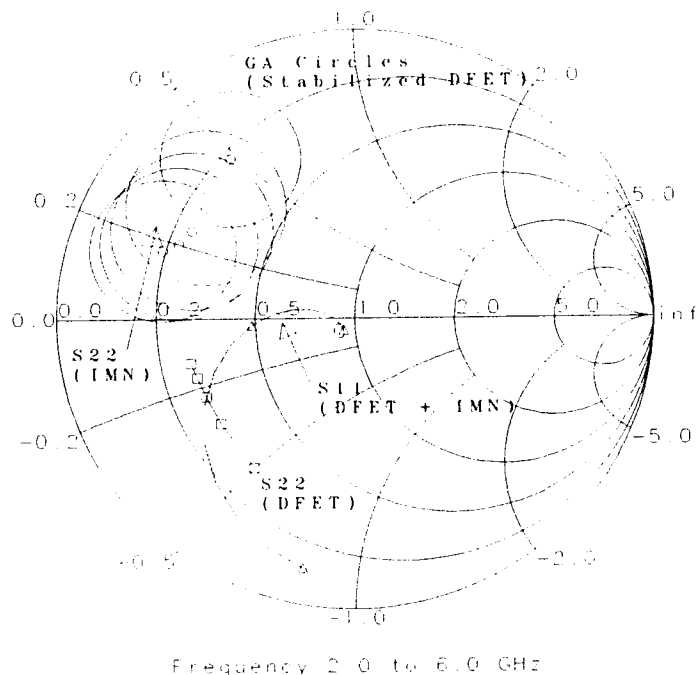
a) DLL of 2 8x200um GFETS with 20 Ohm Load

b) OMN design progression

Figure 1: OMN Design

After the power stage was designed, the power and gain parameters required for driver stages were available. Chip size constraints forced the use of a single driver stage. We chose a  $10 \times 100 \mu\text{m}$  DFET device for this stage because a linear scalable model at appropriate bias conditions was available. To generate between .75W and 1W of power from the GFETs, up to 23 dBm of drive power is needed. The driver amplifier was designed with an emphasis on high gain and efficiency rather than noise performance. Stabilization is accomplished by 400 pH source inductors. The input matching network for the driver amplifier was designed to match 50 ohms to the Available Gain (GA) circles generated by Libra for the linear DFET model. Next, the nonlinear model was used to estimate available linear output power. The driver circuit was iterated several times to ensure adequate gain and power potential. The Smith chart shown in Fig. 2 indicates the progression and final performance of the input matching network.

The interstage matching network was another simple matching problem. We created S-parameter data (S1P) files of the output of the driver stage (IMN w/ DFET) and input of the power stage (GFETs w/ OMN). We attempted to use ESYN (a filter construction program) to match the two impedances in a minimum number of elements. We were not able to effectively tweak the allowable ripple of the response (which sacrifices some level of match) to find a solution with a minimum number of elements. So we went back to simple Smith Chart matching and chained a shunt C, series L, shunt L, series C together and optimized the match. Finally we chained the entire circuit together and optimized the interstage circuit only to sacrifice a little overall match to get appropriate gain levels.



**Figure 2: IMN Design**

It was our intention to do the RF design initially, add the necessary bias networks and DC blocking capacitances and then go back and tweak the networks as required. This was assuming that the added circuitry would be insignificant to RF performance for the most part. In other words, we assumed we would be able to use large blocking C's which aren't too low in impedance and large L's to produce high impedance shunt bias networks. As it turned out, this was not the case in most areas. The IMN and interstage networks had to be designed with these extra components as a part of the networks, but the OMN was a bit more insensitive to these additions.

**Circuit Descriptions and Performance:**

The power stage consists of two 1.6 mm (8x200µm) GFETs. Bias circuits, consisting of large value RF chokes with bypass capacitances, were included on the chip as well. DC blocking capacitors were placed in several locations to isolate the bias voltages of each stage and to ensure that DC is not present of the MMIC output. All bias networks are incorporated into the MMIC model for accurate prediction of s-parameters. A schematic diagram of the power stage is shown below in Figure 3. The -0.8V nominal gate bias yields a typical drain current of around 540 mA. Figure 4 shows the output match and output power possible from the power stage alone.

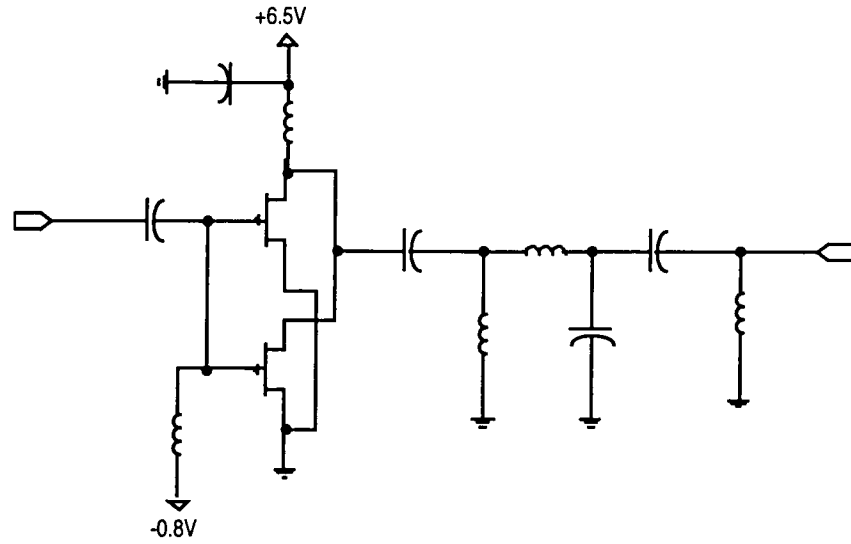
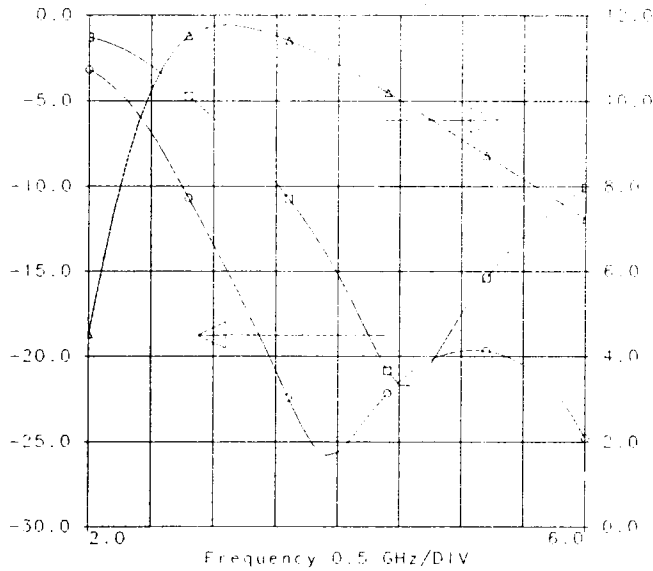
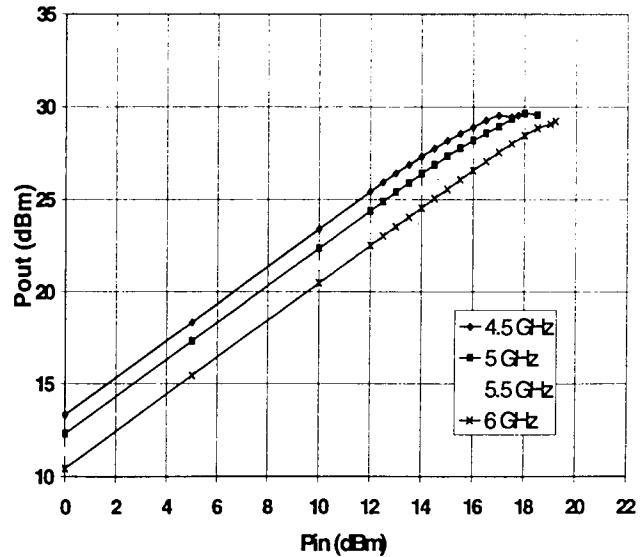


Figure 3: Schematic for Power Stage



a) linear S-parameters



b) potential output power

Figure 4: Performance of Output/Power Stage  
(Ideally matched IMN used for simulation purposes)

A schematic of the DFET driver amplifier is shown in Figure 5. DC isolation is provided by several 10 pF blocking capacitors. The +0.4V nominal gate bias generates a quiescent bias current of 210 mA. The design shown in Figure 5 can provide > 15 dB input return loss from 3-6 GHz. Driver power output at 2,4 and 6 GHz as predicted by the TOM2 nonlinear model is shown in Figure 6.

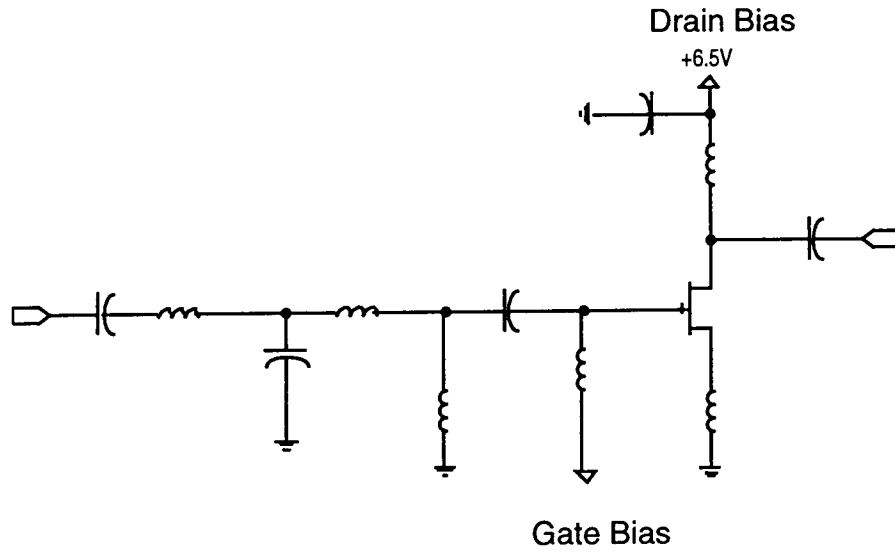


Figure 5: DFET Driver Amplifier

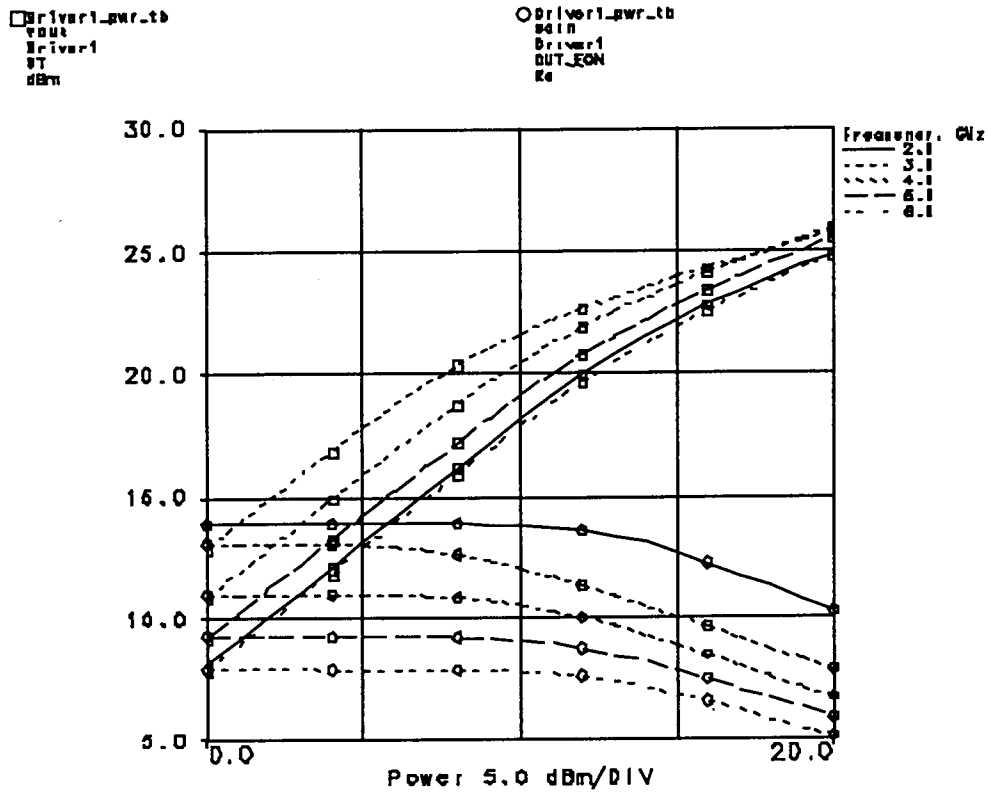


Figure 6: Simulated power output of driver stage

### Modeled Performance:

Table 1 summarizes the design specifications for the power amplifier MMIC. As shown, targeted performance for this MMIC meets or exceeds the required performance.

**Table 1. Specification Compliance Matrix**

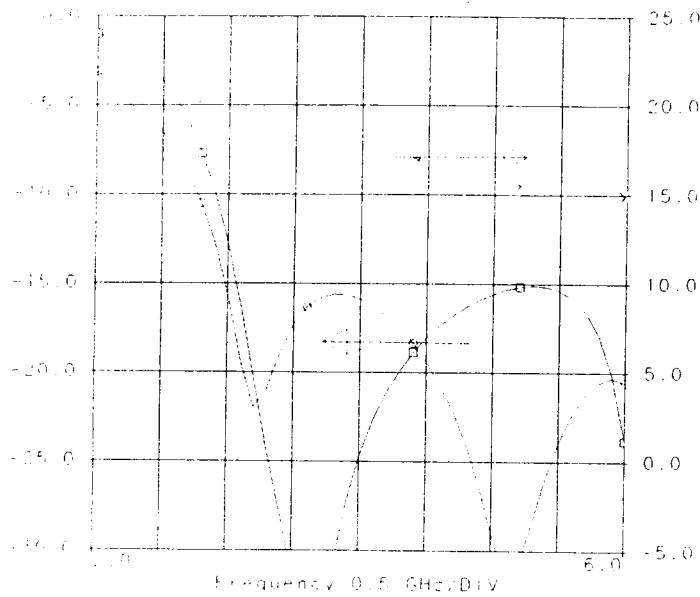
	<b>Required</b>	<b>Desired</b>	<b>Targeted</b>
<b>Frequency</b>	4.5-6 GHz	2-6 GHz	3-6 GHz
<b>Output Power</b>	0.5 Watt	1 Watt	0.75 Watt
<b>Gain</b>	>15dB	18dB	15dB
<b>Efficiency</b>	-	25%	20%
<b>Input VSWR</b> (Return Loss)	< 2:1 (-9.5dB)		<1.6:1 (-12.5dB)
<b>Output VSWR</b> (Return Loss)	<2.2:1 (-8.5dB)		<1.9:1 (-10dB)

### Bias Check:

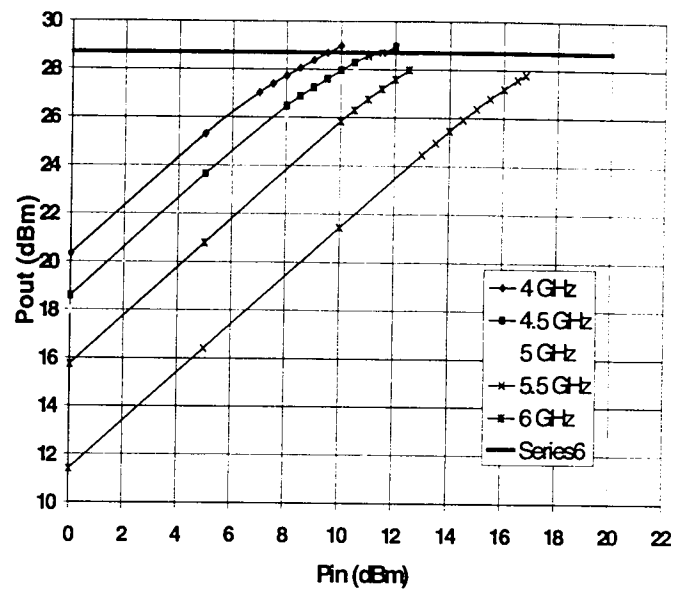
A DC bias test was conducted on the final circuit. It turns out that the line losses of the Drain inductors require that we use a slightly larger supply voltage of 7.2V to bias the devices at 6.5V. The drain currents are 210mA for the driver stage and 540mA for the power stage. The gate voltages are 0.4V for the driver stage (DFET) and -0.8V for the power stage (GFETs). Seeing that the gate currents are negligible, the DC power in can be approximated by  $7.2V \times 750mA$  or 5.4 W.

### Final Simulated Performance:

A complete schematic and layout for the Power Amplifier MMIC is included in the appendix. The graphs below in Figure 7 illustrate final simulated performance of this device. Note the low gain simulation of the nonlinear model caused the 5.5GHz curve to fall slightly above the others. Also, drain bias (Vd) was at 6.5 V and models with higher bias levels show slightly greater power out levels.



a) linear S-parameters



b) output power

Figure 7: Performance of Final Amplifier

**Power Amplifier Test Plan:**

1) Required Equipment:

spectrum analyzer, HP8510 network analyzer, RF signal generator, 3 independent DC power supplies, RF wafer probe station, DC and RF cables, 20 dB attenuator.

2) DC Bias and RF Stability / Power Test Procedure:

Configure the RF generator to 2 GHz, 0 dBm output, RF off

Set the two gate power supplies to -2 VDC

Set the drain power supply to + 7 VDC, current limit 1A

Connect the circuit as shown in the following diagram. **CONNECT THE DRAIN SUPPLY LAST!**

To power on the amplifier, bring the VG1 (Driver) voltage up slowly while monitoring drain current. The voltage should be increased until the drain current reaches 210 mA. The final gate voltage should be approximately +0.4 V. Next bring up the VG2 (Power stage) voltage until an additional 540 mA is measured on the drain supply.

3) RF Gain Test:

Perform a 2 port calibration on the 8510 with a 20 dB pad on port 2

Connect the circuit as shown in Figure 9. **CONNECT THE DRAIN SUPPLY LAST!**

Power the amplifier on as described in the previous Bias / Stability / Power Test.

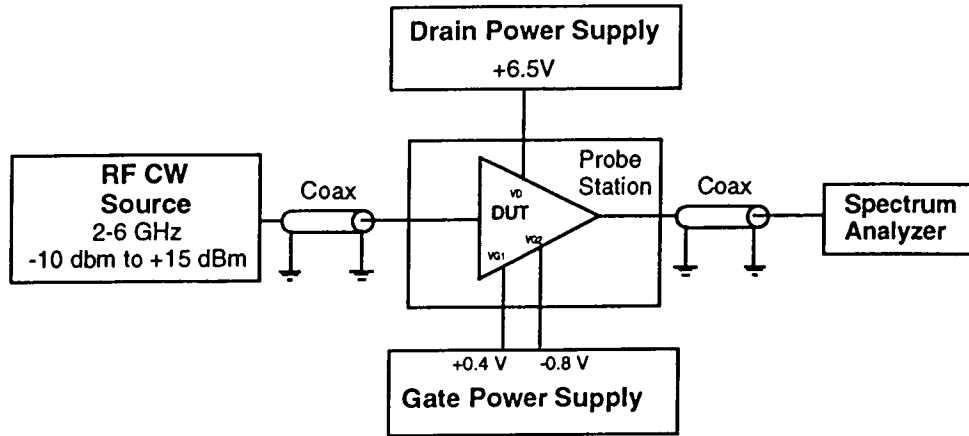


Figure 8: Equipment connection for Stability Test

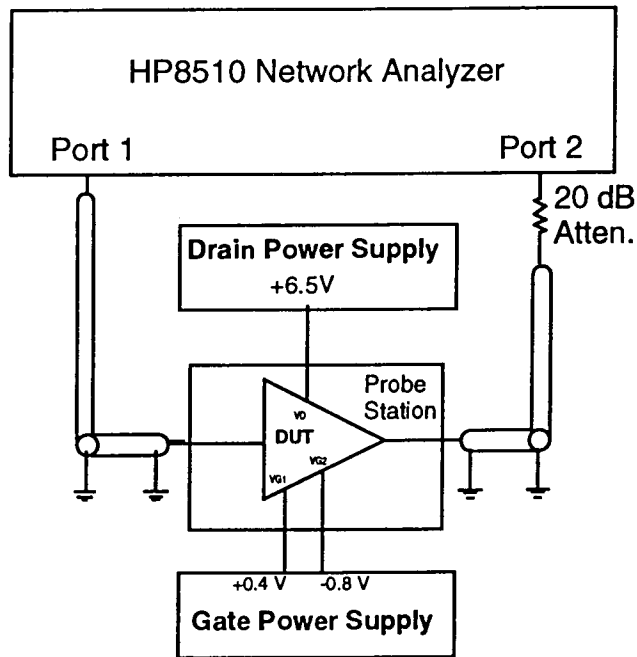


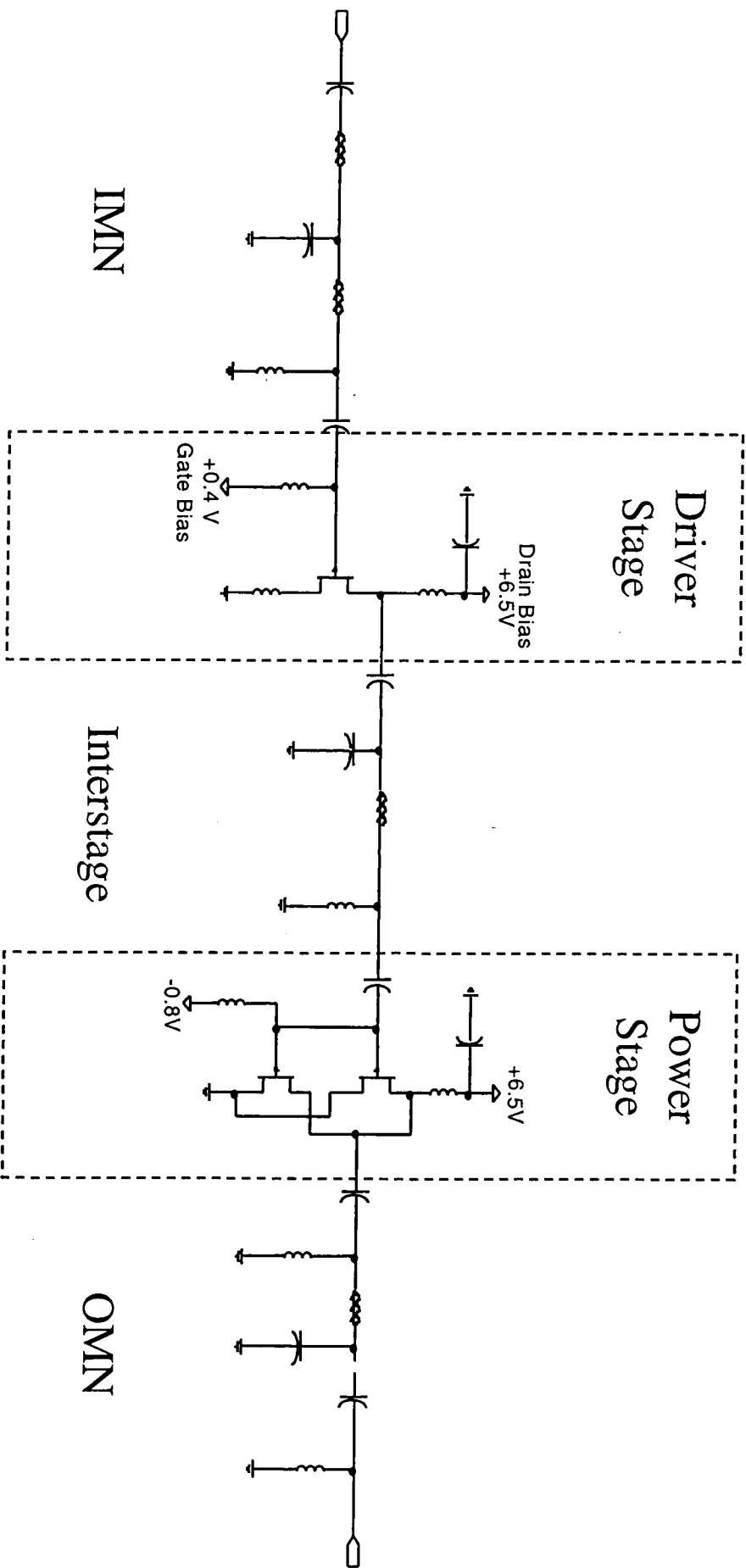
Figure 9: Equipment connection for Gain Measurement.

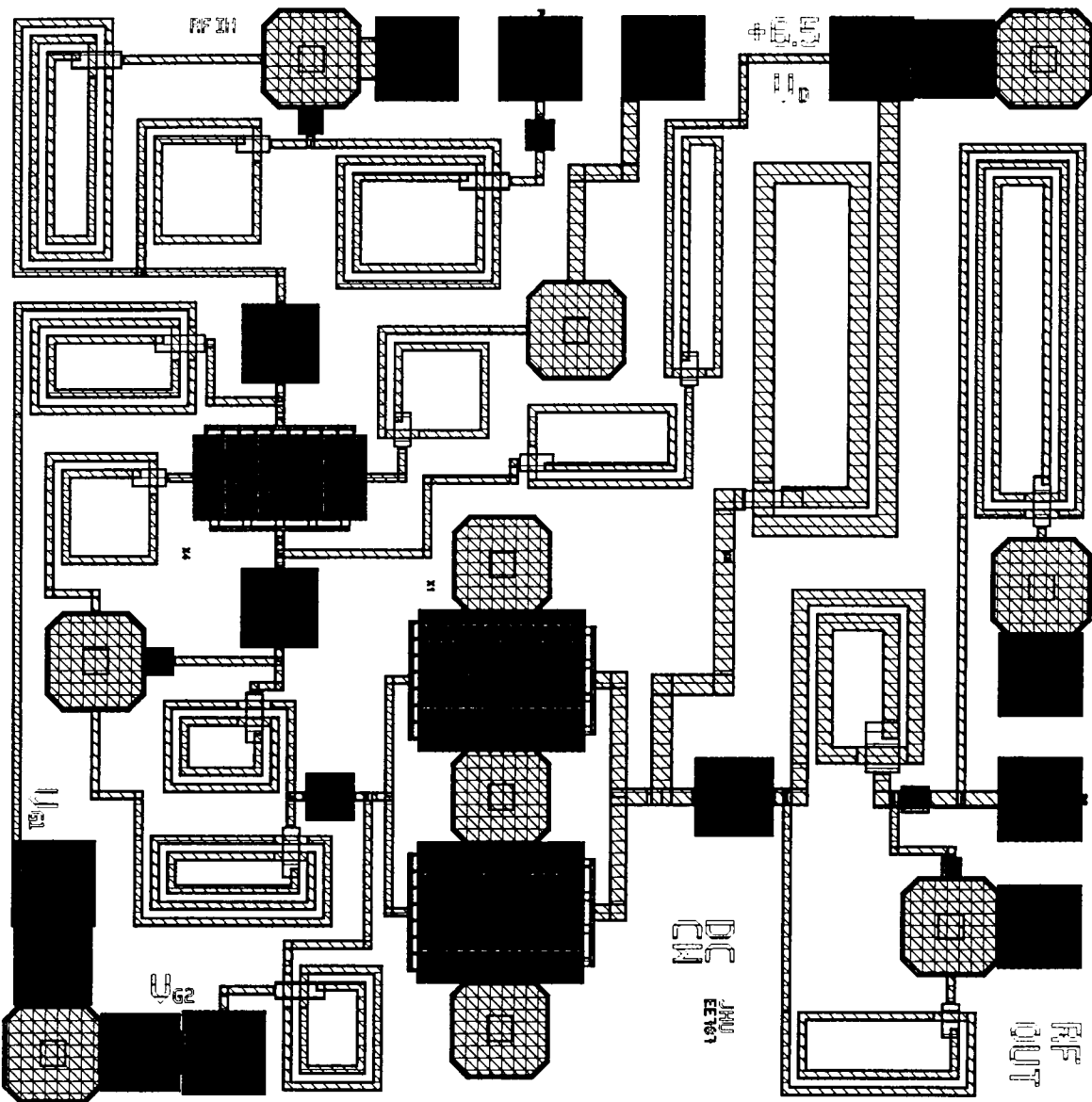


## **Conclusion and Recommendations:**

This report details our work during the MMIC design course EE525.787 to design and simulate a C band power amplifier using the Triquint TRX process. We would consider our effort a success based upon the simulated results presented here. The final MMIC design meets most of the given performance guidelines. Several compromises were necessary to produce a working design in the time and die area allocated to us. As stated earlier, low breakdown voltage of the GFET device and small 50x50 mil die area ultimately limited the power and bandwidth, respectively, of this device. Design time was not available to attempt more complex feedback topologies which may have increased bandwidth or gain flatness.

# Appendix A: Power Amplifier Schematic





Final Report for the EE787 Design Project

90 Degree Digital Phase Shifter

Microwave Monolithic Integrated Circuit (MMIC) Design

Fall 1998

(525.787)

Professors: Craig Moore and John Penn

Matthew G. Long  
and Jimmy Xiang

Submitted: December 14, 1998

## 1. Summary

This report presents a design for a one-bit digital (binary) 90-degree phase shifter based on the Triquint TQTRx Monolithic Microwave Integrated Circuit (MMIC) process. The design approach follows the methodology described in chapter 6 of reference 1. The circuit topology defined in this reference uses the "on-state" low resistance and "off-state" source-to-drain capacitance of a MESFET device as an electrical component in two parallel switched-filter structures which have a 90-degree phase difference in the forward S-parameter across the design frequency band. Engineering work to implement this circuit topology in a functional MMIC design is documented with performance simulation results, schematic diagrams, dc bias analysis, a wafer probe station test plan, and recommendations for further design enhancements. Simulation data indicates that the amplitude and phase shift design requirements are met across a frequency span of 3.3 GHz to 6.0 GHz. The design goal for VSWR of 1.5:1 is met from 3.7 GHz to 5.05 GHz, and the VSWR held to less than 2.3:1 across 3.3 GHz to 6.0 GHz. Harmonic balance simulation of the complete MMIC circuitry verifies the design functionality and phase shift. Test data will be collected on a fabricated MMIC wafer based on this submitted design at a future date.

## 2. Introduction

The principle of operation of this 90-degree phase shifter is based on switching between paths in a parallel combination of high pass and low pass filters. This type of topology has the benefit of not requiring long transmission lines needed to implement distributed elements, and therefore, conserves MMIC substrate area. A low pass filter provides phase lag to signals passing through it, while a high pass filter provides phase advance. The low pass filter is made up of series inductors and shunt capacitors and the high pass filter is made up of series capacitors and shunt inductors. The MESFET switches are realized by employing the GFET device in the Triquint process. The gate controls the ON and OFF state between the source and drain of the GFET. In comparison to a reverse-biased PIN diode, the total capacitance of the GFET switch in the OFF state is large. To achieve a broad bandwidth, this capacitance is absorbed into the design of the low pass and high pass filters.

The parallel filter circuit topology incorporating the GFETs is shown in Figure 1. There are six GFETs, connected into two sets of T-network filter configurations. The series elements of one T network and the shunt element of the other T network are connected from a single gate control voltage. When the control voltage  $V_1$  is zero, and  $V_2$  is beyond the pinch-off voltage, the circuit of Figure 1 can be simplified to the low pass filter circuit in Figure 2 (a). In the opposite switch state, the circuit of Figure 1 can be simplified to form the high pass filter circuit shown in Figure 2 (b). It is obvious that the GFET OFF state capacitance is no longer an undesired parasitic, instead it has been used as an integral component in the realization of the filter network.

A critical factor for successful implementation of this design is an accurate model for the GFET device when used as a switch. The standard TOM-2 model is outside the suggested range of accuracy for use in this application, but appears to provide simulation results which are in close agreement with the linear model described in the references. The linear model used in this design is shown in Figure 4, which is adapted from the last page of class handout #4. Figure 3 (a) shows that when the GFET is in the ON state, it can be modeled as a single resistor. The resistance value is derived from the IV curve of the GFET. It is computed from the slope of the  $I_{dss}$  curve when  $V_{ds}$  is close to zero volts. For the OFF state, shown in Figure 3 (b) the gate-to-source and gate-to-drain model is a resistor and capacitor in series. The capacitance  $C_g$  represents approximately half of the gate capacitance with the channel fully depleted. Note that all element values in the model can be scaled to a realizable FET size from the standard  $300\ \mu\text{m}$  ( $6 \times 50$ ) FET. This scaling is suited to adjusting the capacitance incorporated into the filter networks.

The schematic diagram for the TTL driver circuit is shown in Figure 4. This circuit takes one TTL voltage range input and produces the two MESFET drive signals needed to switch between the two filter paths. The second driver output signal is the complement of the first. Positive and negative five volt supplies are used.

The control signal is applied to the gate of an enhancement mode DFET in the first stage through a resistor voltage divider. Hysteresis provided by the bias-dependent equivalent series gate resistance of this device provides noise immunity to the TTL driver circuit first stage. Two depletion mode DFETS serve as constant current sources at the source and drain of the enhancement mode device and limit the voltage across the device. The source connects to the current source through a level-shifting diode to complete the first stage.

The output from the level-shifting diode switches the voltage level applied to the gate of a depletion mode amplifier where the design follows the circuit example in the handout supplement to lecture #5. This second stage is completed by a depletion DFET serving as a constant current source connecting to the positive supply.

The output driver stage has a larger DFET output transistor driving a level shifting network consisting of five Schottky diodes in series with a DFET constant current source connecting to the negative supply. The complementary output is generated by tapping the level shifting diode network to drive a second gain and output circuit block, essentially identical to stages 2 and 3 used to generate the first output.

In the actual circuit implementation used in the MMIC design, the transistors employed as diodes by shorting the source and drain together shown in Figure 4 are replaced by Lap diodes to conserve layout area. For the same reason, the transistor gate lengths used in stages 1 and 2 were made as small as possible. The stage 3 output transistors were scaled up to 4 gate fingers by 36 micron gate length in order to provide current drive capability. A dc bias bench simulation indicates that the transition voltage at the input needed to induce switching between states at the driver outputs is between 1.5 and 1.9 volts. The outputs used to drive the switching GFET gates have a voltage swing range of -2.45 volts to +0.3 volts, to provide the pinch-off and saturated states, respectively.

### 3. Modeled Performance

A specification compliance matrix which indicates the design requirements, goals and simulation results for the 90 degree phase shifter design is provided in Table 1. The phase shift difference between the two signal paths exceeds 95 degrees below 3.25 GHz. The loss of the HPF network signal path increases to more than 1 dB of the LPF network path loss for frequencies less than 2.8 GHz. The VSWR design goal of 1.5:1 is met within the frequency range of 3.7 GHz to 5.05 GHz. Simulation data available for the finished design layout is summarized in the list of plots below.

Performance Parameter	Requirement	Goal	Design Simulation Result
Frequency Range	4.5 GHz to 6.0 GHz	2.0 GHz to 6.0 GHz	3.25 GHz to 6.0 GHz
Phase Difference	90 degrees +/- 5 deg.		Yes, freq. range given above.
Insertion Loss		-1.0 dB	-2.1 dB max.
VSWR (50 ohms nom.)		< 1.5:1.0	<2.3:1.0
Control Voltage	TTL Level		Threshold at 1.75 volts
Supply Current +5 volts			24.0 mA
Supply Current -5 volts			23.0 mA
Size	60 x 60 mil Anachip		Yes, with test structure.

Table 1. Specification Compliance Matrix

List of Figures containing plots of performance data:

<u>Figure</u>	<u>Performance Data</u>
5	Phase shift and forward S-parameters
6	Input and output reflection coefficients
7	Worst-state VSWR
8	End-to-end simulation at 4.5 GHz
9	DC bias bench simulation of driver output voltages and input current as a function of control voltage
10	Current consumption from +/- 5 volt supplies

4. List of Figures for schematic diagrams and layout

<u>Figure</u>	<u>Circuit Function</u>
11	Phase shifter with layout items
12	TTL driver with layout items
13	Driver-to-phase shifter interconnections
14	Complete phase shifter MMIC layout

5. DC Analysis

Bias check results for the TTL driver circuit are presented in Figure 9. Current consumption for the driver circuit is estimated to be close to 24 mA each for the positive and negative supply voltages. This plot is presented in Figure 10. A summary of critical component DC current stress values is presented in Table 2.

Critical Part	Value	Max. Design Current	Minimum Feature Size
Lap diode	voltage drop	20 mA	36 $\mu\text{m}$
G- res. at GFET gate	5.0 k $\Omega$	0.1 mA	4.0 $\mu\text{m}$
NiCr res. driver output	400 $\Omega$	6.25 mA	20 $\mu\text{m}$
G- res. at driver input	2.0 k $\Omega$	1.2 mA	40 $\mu\text{m}$
G- res. input shunt to gnd	6.0 k $\Omega$	0.5 mA	20 $\mu\text{m}$

6. Test Plan – diagram of test setup provided in Figure 15.

- 1) Calibrate the 8510 network analyzer for 2-port measurements using GSG die probes across a frequency span of 2.0 to 6.0 GHz.
- 2) Connect GSG probes on wafer test station to the DUT RF Input and RF Output pad areas. Use dc blocking capacitors external to the DUT die.
- 3) Connect needle probes to +5.0 vdc and -5.0 vdc pads on the DUT die.
- 4) Connect needle probe to TTL input control line and make connection to an adjustable voltage source.
- 5) Provide measurement capability for +5 and -5 volt supply currents. Apply power to the device and verify that the current drawn from each supply is less than 25 mA.
- 6) Set adjustable voltage source connected to the input control line to zero volts. Measure indicated DUT phase shift on the 8510 network analyzer.

- 7) Increase the control voltage to 3.0 volts and measure the phase shift on the 8510. Do not allow the control voltage to exceed 4.0 volts at the TTL control input, unless the current drawn into this port is held to less than 1 milliampere.
- 8) If a change in the amount of phase shift provided by the DUT is not evident, use the TTL driver circuit monitoring pads to check the gate drive voltage levels applied to the phase shifter GFET elements.
- 9) If necessary, drive the gate voltages to zero and  $-3.0$  volts from the monitoring pads. Exchanging complementary drive voltages should cause the DUT to produce desired phase shift.
- 10) Measure phase shift from 2.0 GHz to 6.0 GHz with at least 401 steps with the control input voltage applied to the GFET switch gates held to at least 0 volts for the ON state and below  $-2.0$  volts for the OFF state.
- 11) Use s-parameter data collected from test structure measurements to evaluate simulation model accuracy.

## 7. Conclusions and Recommendations

Experience with tuning this design in the simulator shows that the total phase shift difference between the two signal paths can be adjusted by scaling the inductor values and GFET total gate lengths. Applications intended for use at a specific frequency range will benefit from selecting a combination of values which provide optimal performance over the specific band of interest. To maintain proper small-signal performance of the phase shifter, a designer with more die area available may want to add dc blocking capacitors on the input and output paths.

Further analysis can be performed to determine the input power damage threshold, sensitivity of the design to process variation in component values, and sensitivity of the TTL driver circuit to power supply voltage variation. Monte Carlo simulation of shifts in component parameters would have particular value in assessing yield sensitivity to process variations.

One area specifically requiring the attention of a designer is to obtain necessary measurement data to characterize more accurately the linear switch model parameters for the GFET device. A test structure is incorporated on the wafer for this purpose. Unfortunately, the limited chip area precluded providing GSG ports for both the source and drain. A compromise solution of providing one GSG port to connect to the source while terminating the drain with a 50 ohm resistor was adopted. A separate pad connects to the gate through a large resistor to provide a control input. A simple theoretical investigation should be performed to determine the level of accuracy with which the off-state capacitance and on-state resistance can be extracted from reflection coefficient measurements made with the network analyzer connected to this one-port test structure.



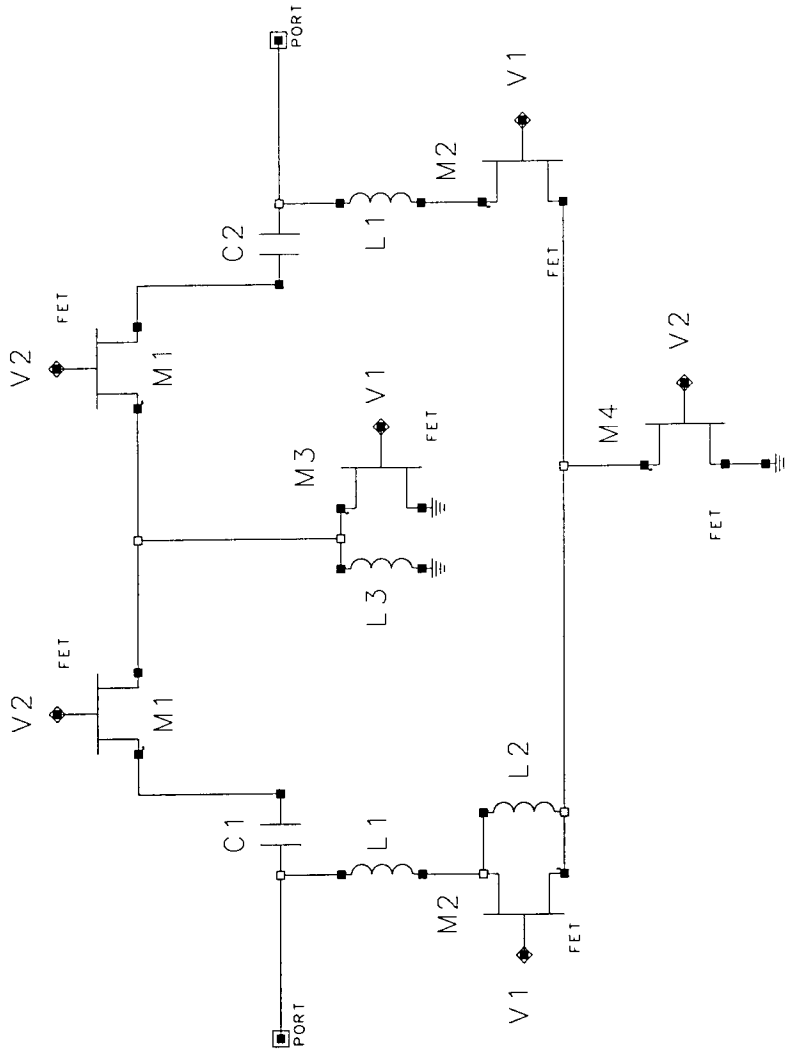
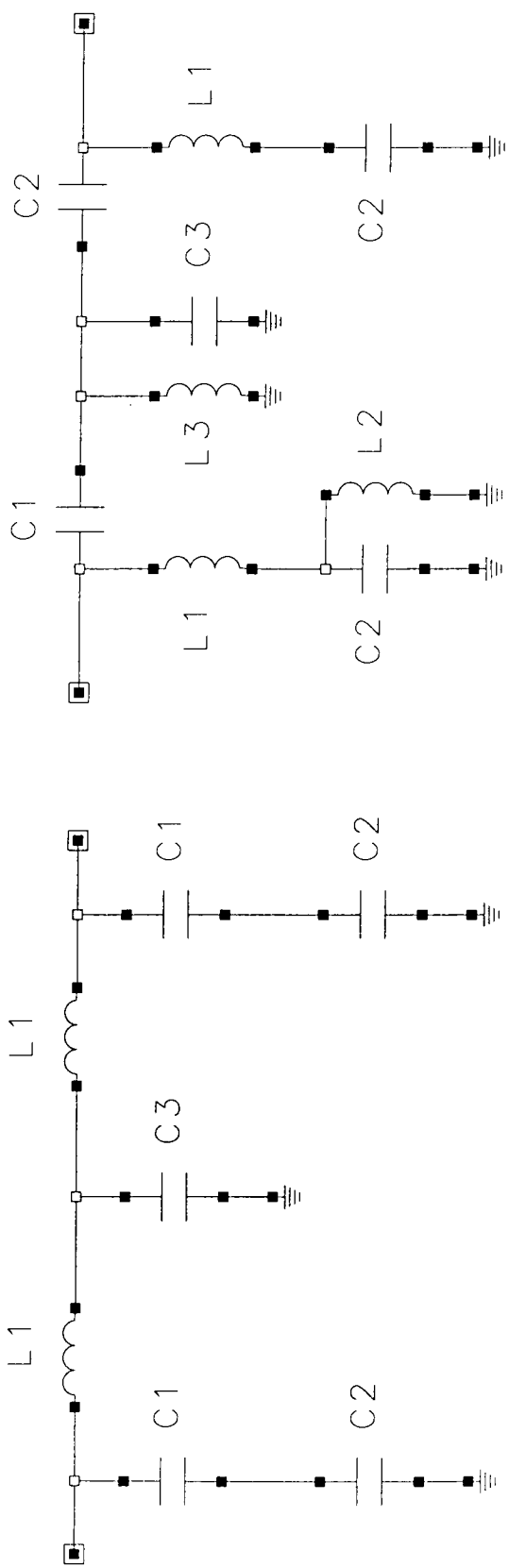


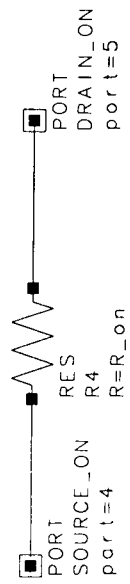
Figure 1. Parallel Filter Topology for 90 Degree Phase Shifter



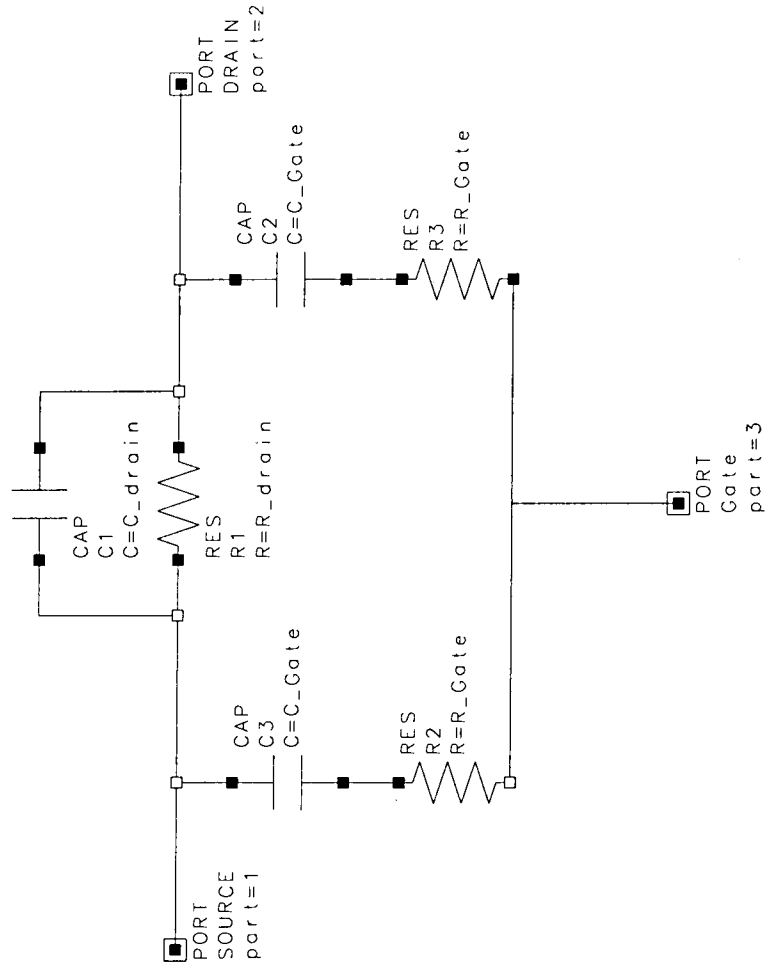
(a) LPF Path

(b) HPF Path

Figure 2. Separation of LPF and HPF Paths in 90 Degree Phase Shifter



(a) ON State



(b) OFF State

Figure 3. Linear FET Model Parameters

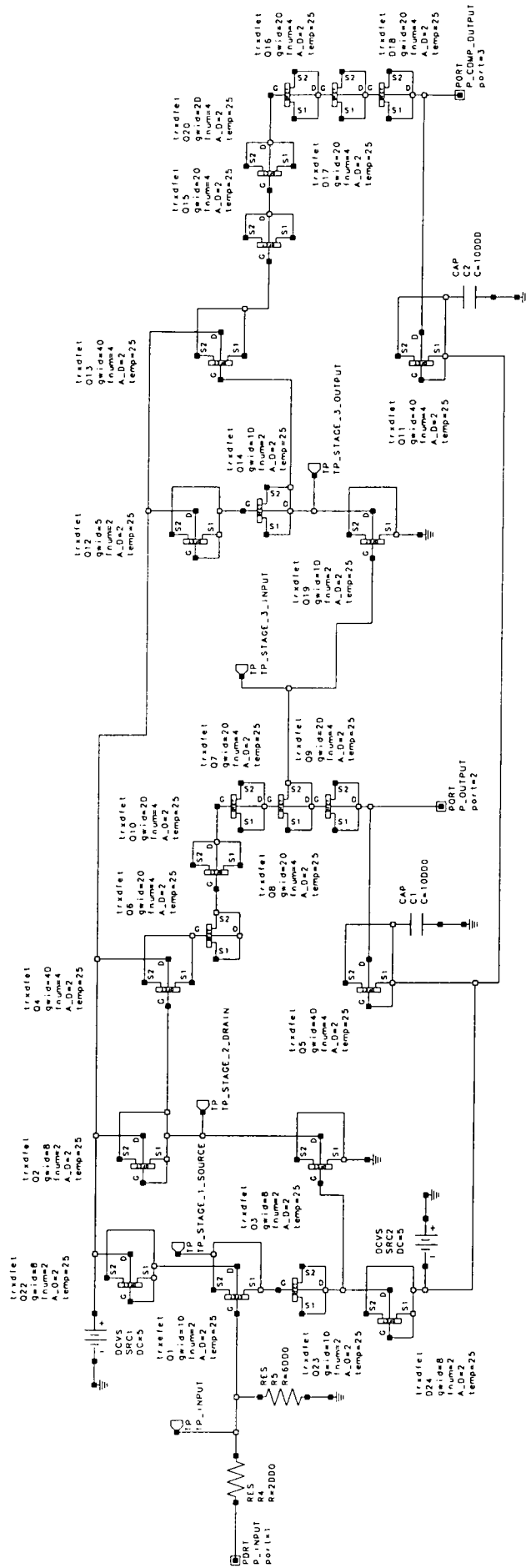


Figure 4. Simplified TTL Driver Schematic

□ tq\_Phase\_90\_sim\_tb  
 phase\_difference  
 tq\_Phase\_90\_s  
 OUT\_EQN  
 Ang  
 deg

○ tq\_Phase\_90\_sim\_tb  
 phase\_difference  
 tq\_Phase\_90\_s  
 OUT\_EQN  
 Ang  
 deg

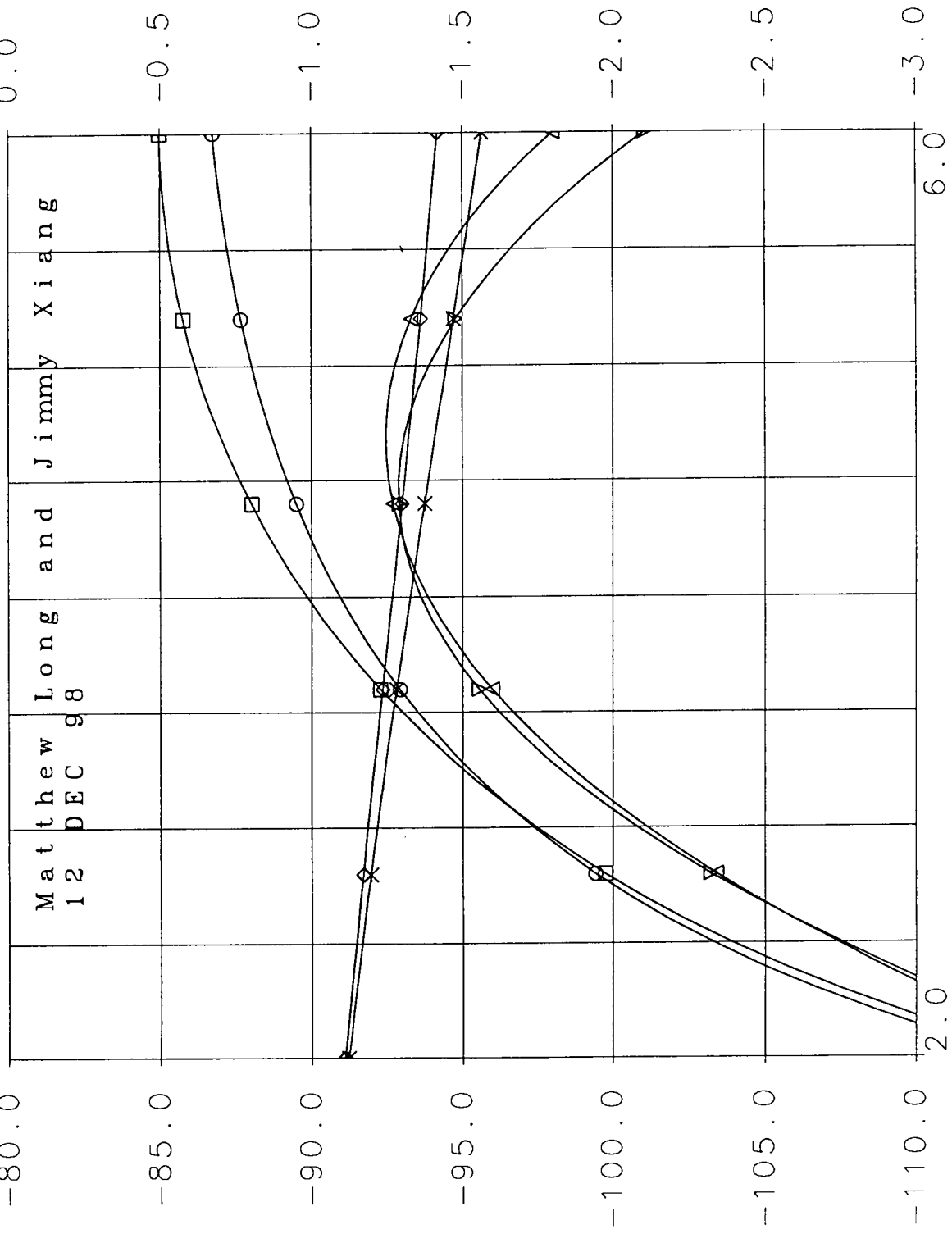
▽ tq\_Phase\_90\_sim\_tb  
 S21  
 tq\_Phase\_90\_s  
 S[2,1]  
 dB

△ tq\_Phase\_90\_sim\_tb  
 S21  
 tq\_Phase\_90\_s  
 S[2,1]  
 dB

◇ tq\_Phase\_90\_sim\_tb  
 S43  
 tq\_Phase\_90\_s  
 S[4,3]  
 dB

\* tq\_Phase\_90\_sim\_tb  
 S43  
 tq\_Phase\_90\_s  
 S[4,3]  
 dB

Phase Shift and Forward S-Parameter for  
 Six-Element Linear Model and TOM-2 Model

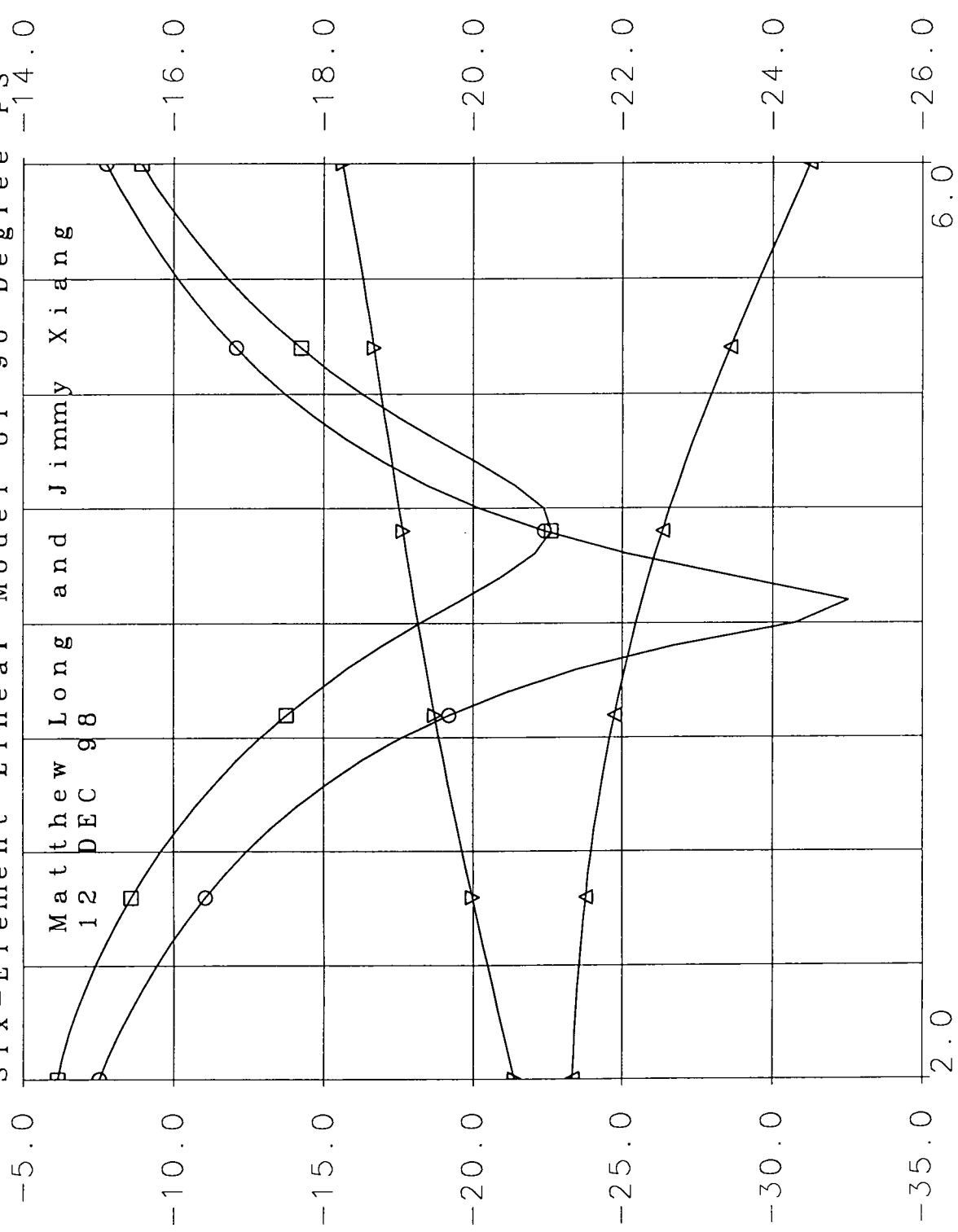


Frequency 0.5 GHz/DIV

Figure 5. Phase shift and forward S-parameters

□  $t_{q\_Phase\_90\_sim\_tb}$  S22  $t_{q\_Phase\_90\_sim\_tb}$  S33  $t_{q\_Phase\_90\_sim\_tb}$  S44  
 $t_{q\_Phase\_90\_s}$  S[1,1]  $t_{q\_Phase\_90\_s}$  S[2,2]  $t_{q\_Phase\_90\_s}$  S[3,3]  $t_{q\_Phase\_90\_s}$  S[4,4]  
 dB dB dB dB

Input and Output Reflection Coefficients for Six-Element Linear Model of 90 Degree PS

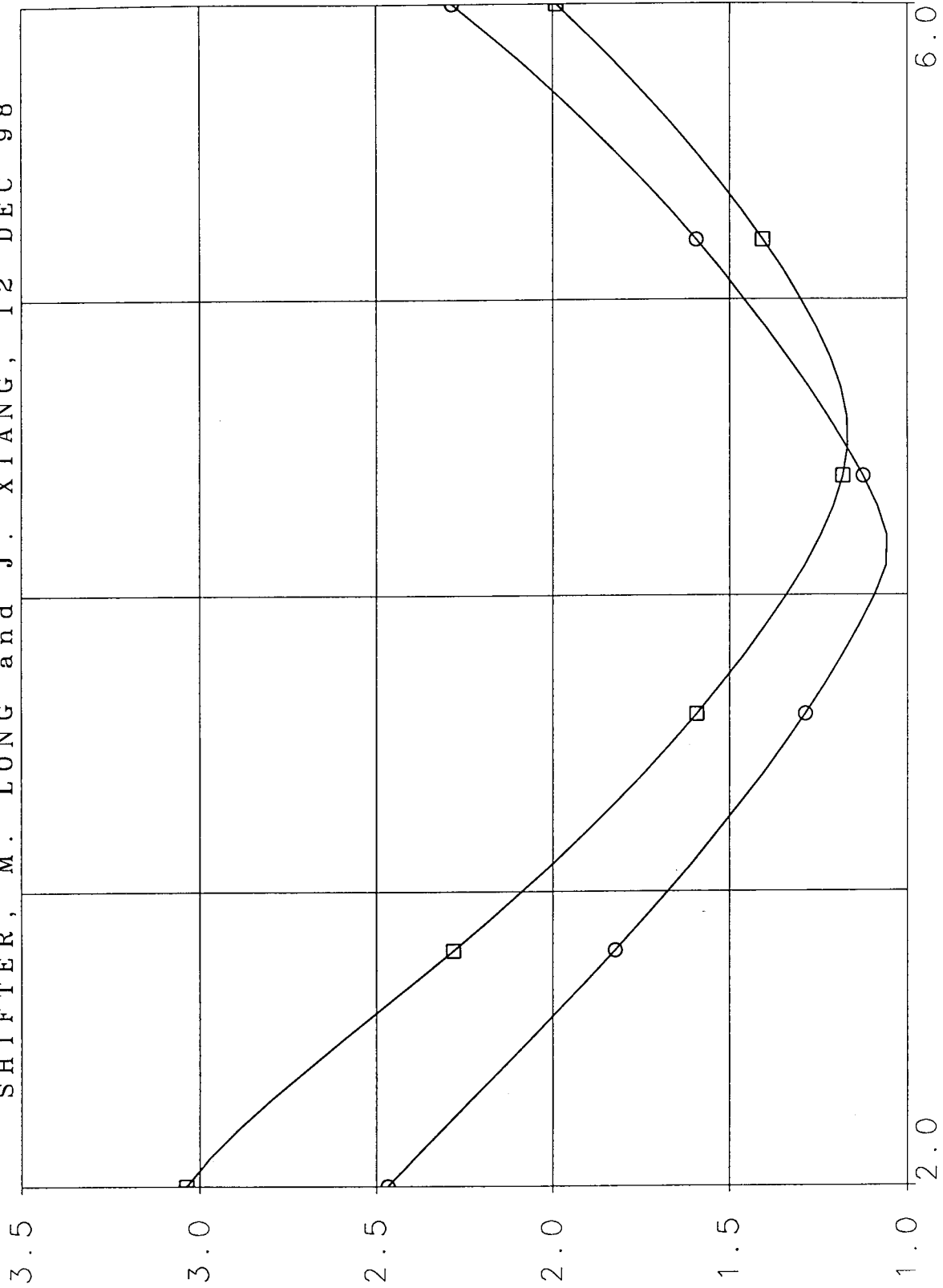


Frequency 0.5 GHz/DIV  
 Figure 6. Input and output reflection coefficients

□ tq\_phase\_90\_sim\_tb  
 S11  
 tq\_phase\_90\_s  
 S[1,1]  
 VSWR

○ tq\_phase\_90\_sim\_tb  
 S22  
 tq\_phase\_90\_s  
 S[2,2]  
 VSWR

WORST-STATE VSWR FOR 90 DEGREE PHASE  
 SHIFTER, M. LONG and J. XIANG, 12 DEC 98



Frequency 1.0 GHz/DIV

Figure 7. Worst-state VSWR

□ tq\_ph\_90\_final\_rev1\_HMB\_tb  
 V\_OUTPUT\_0  
 tq-ph  
 VT  
 V

○ tq\_ph\_90\_final\_rev1\_HMB\_tb  
 V\_OUTPUT\_90  
 tq-ph  
 VT  
 V

Phase Shift for Two Input Control States  
 End-to-End Harmonic Balance Simulation

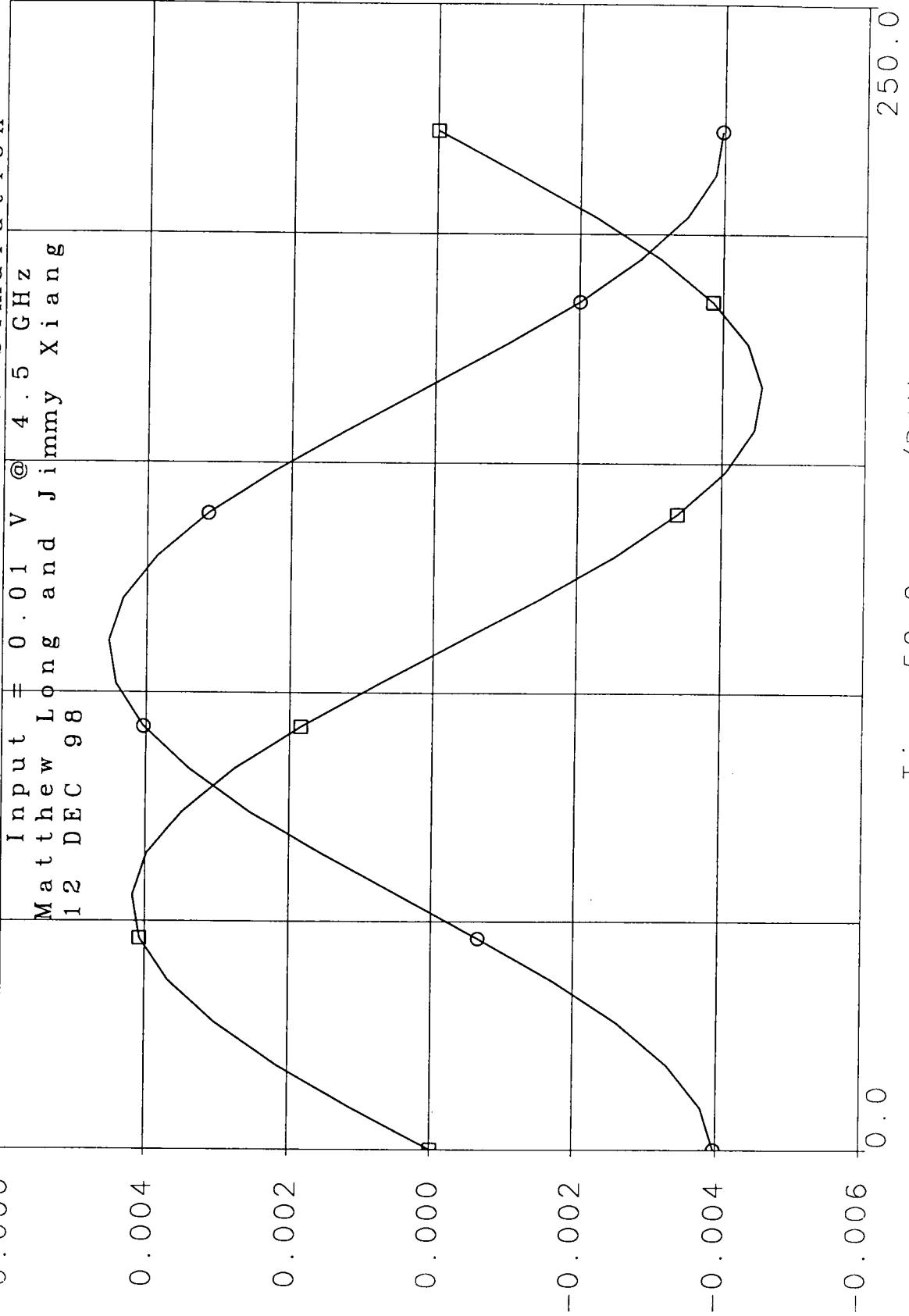


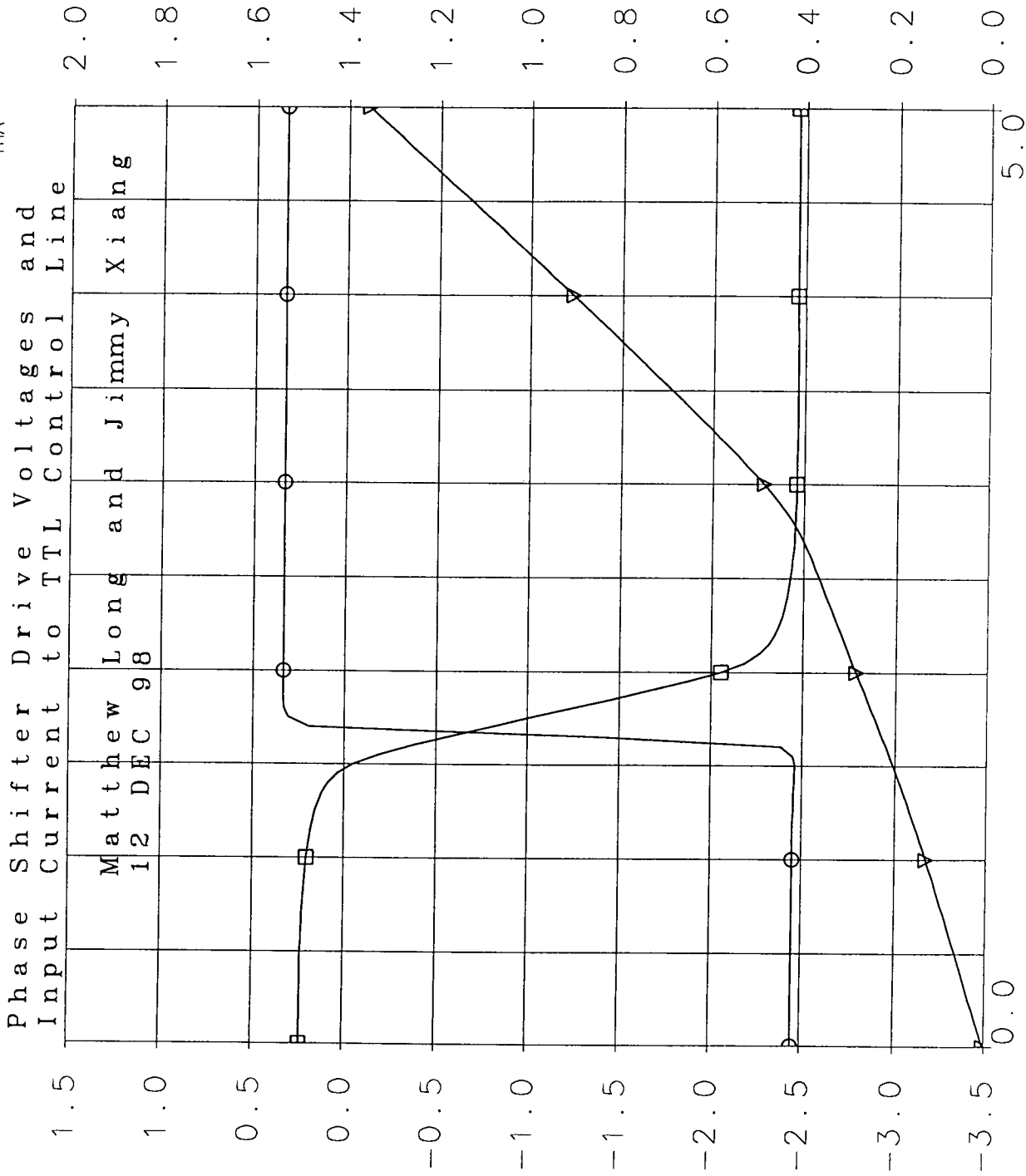
Figure 8. End-to-end simulation at 4.5 GHz. Time 50.0 psec/DIV



□ TTL\_Driver\_Rev\_9\_tb  
 V\_OUTPUT\_SIGNAL  
 TTL\_Driver\_R  
 VDC  
 V

○ TTL\_Driver\_Rev\_9\_tb  
 V\_OUTPUT\_COMPLEMENT  
 TTL\_Driver\_R  
 VDC  
 V

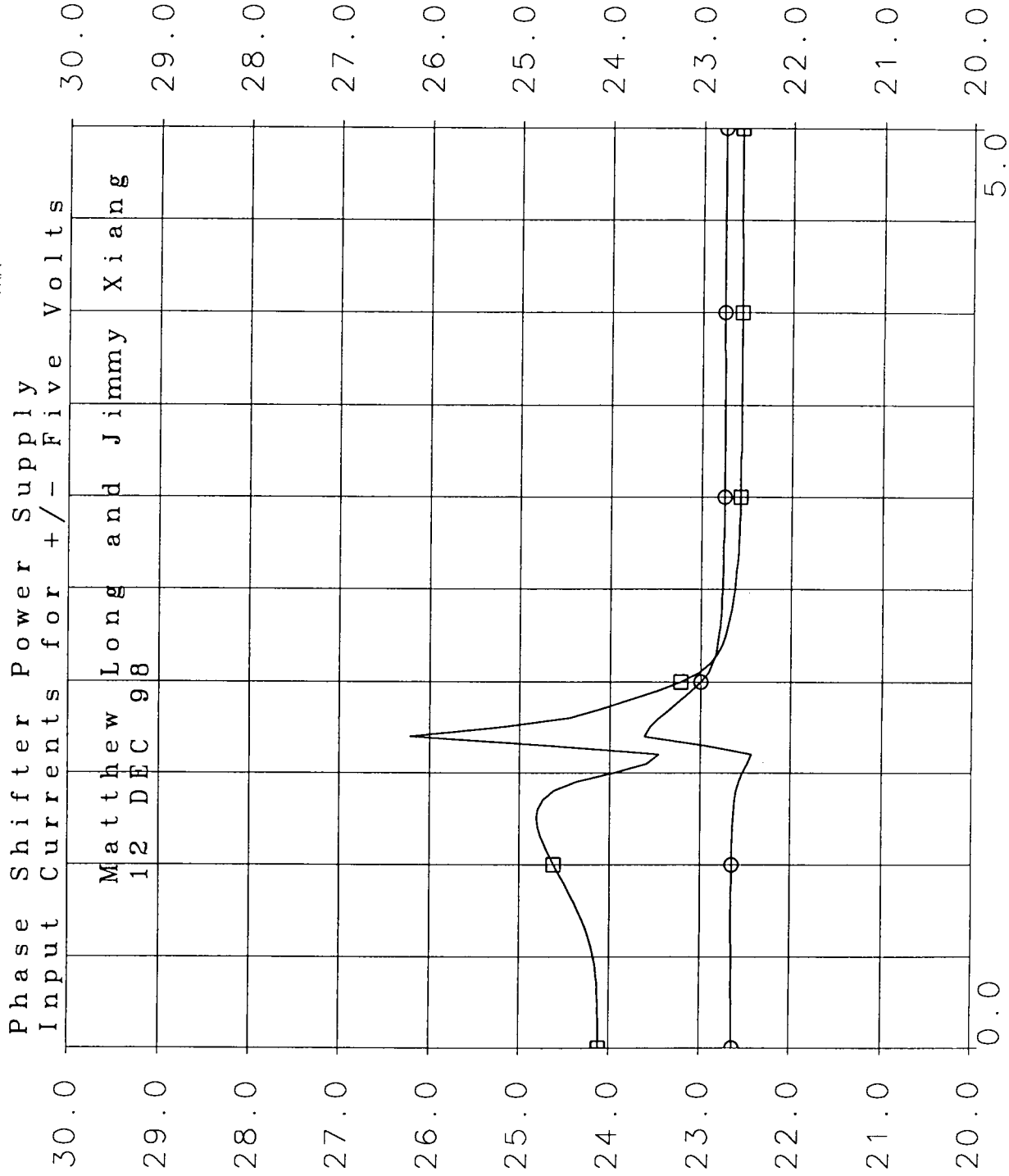
▽ TTL\_Driver\_Rev\_9\_tb  
 IDC1  
 TTL\_Driver\_R  
 IDC  
 mA



Bias 1 0.5 / DIV  
 Figure 9. DC bias bench simulation of driver output voltages and input current as a function of input voltage.

□ TTL\_Driver\_Rev\_9\_tb  
 IDC\_PLUS\_FIVE\_SUPPLY  
 TTL\_Driver\_R  
 IDC  
 mA

○ TTL\_Driver\_Rev\_9\_tb  
 IDC\_NEG\_FIVE\_SUPPLY  
 TTL\_Driver\_R  
 IDC  
 mA



Bios1 0.5 /DIV  
 Figure 10. Current consumption from +/-5 volt supplies

FINAL VERSION OF PHASE-SHIFTER LAYOUT WITH THE TOM-2 MODEL FOR PERFORMANCE SIMULATION  
 MATTHEW LONG AND JIMMY XIANG - DECEMBER 12, 1998

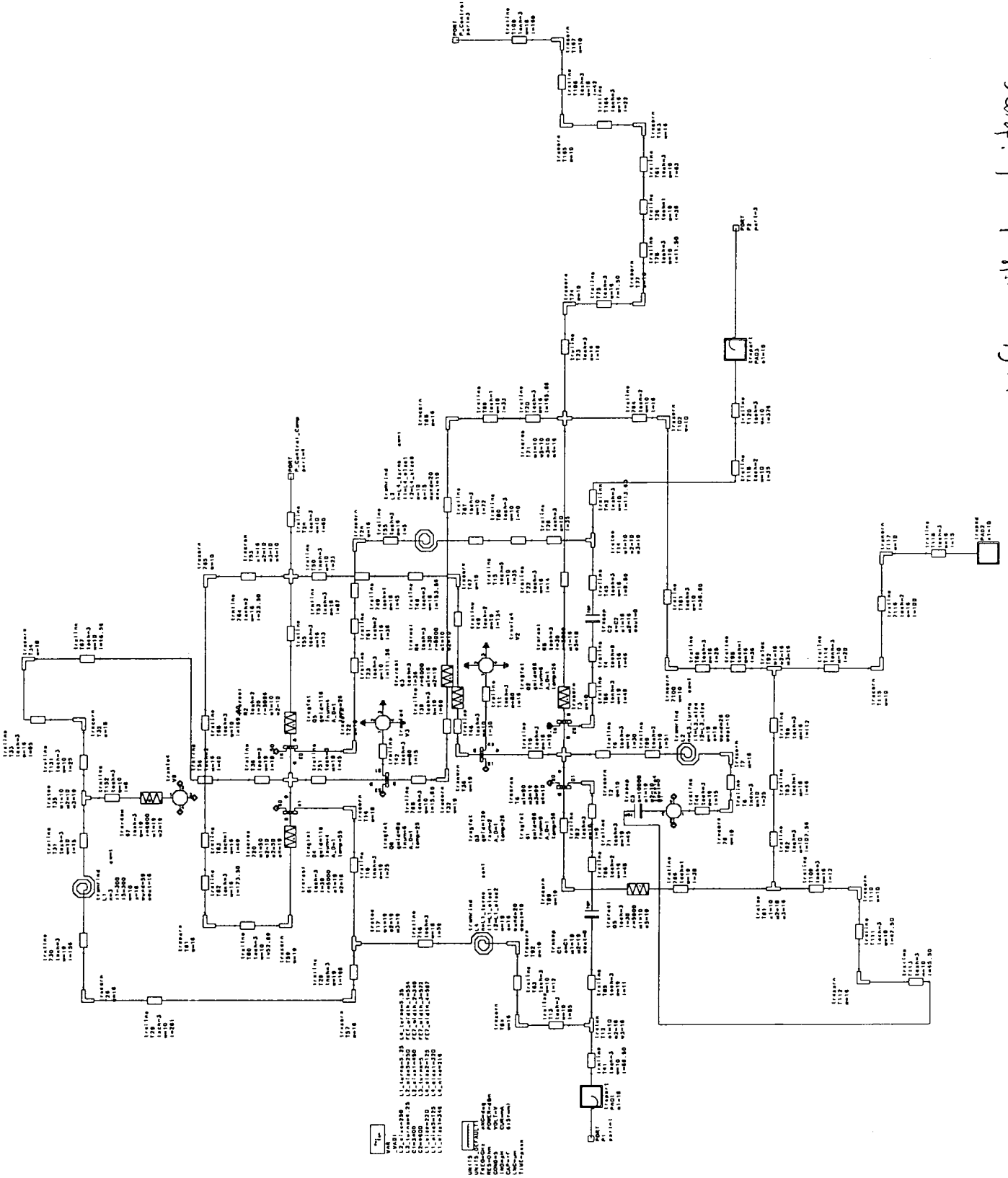


Figure 11. Schematic for Phase-shifter with layout items

TTL DRIVER CIRCUIT FINAL LAYOUT WITH LAP DIODES AND AFTER HARMONIC BALANCE SIMULATION - M. LONG AND J. KIANG, 17 NOV 88

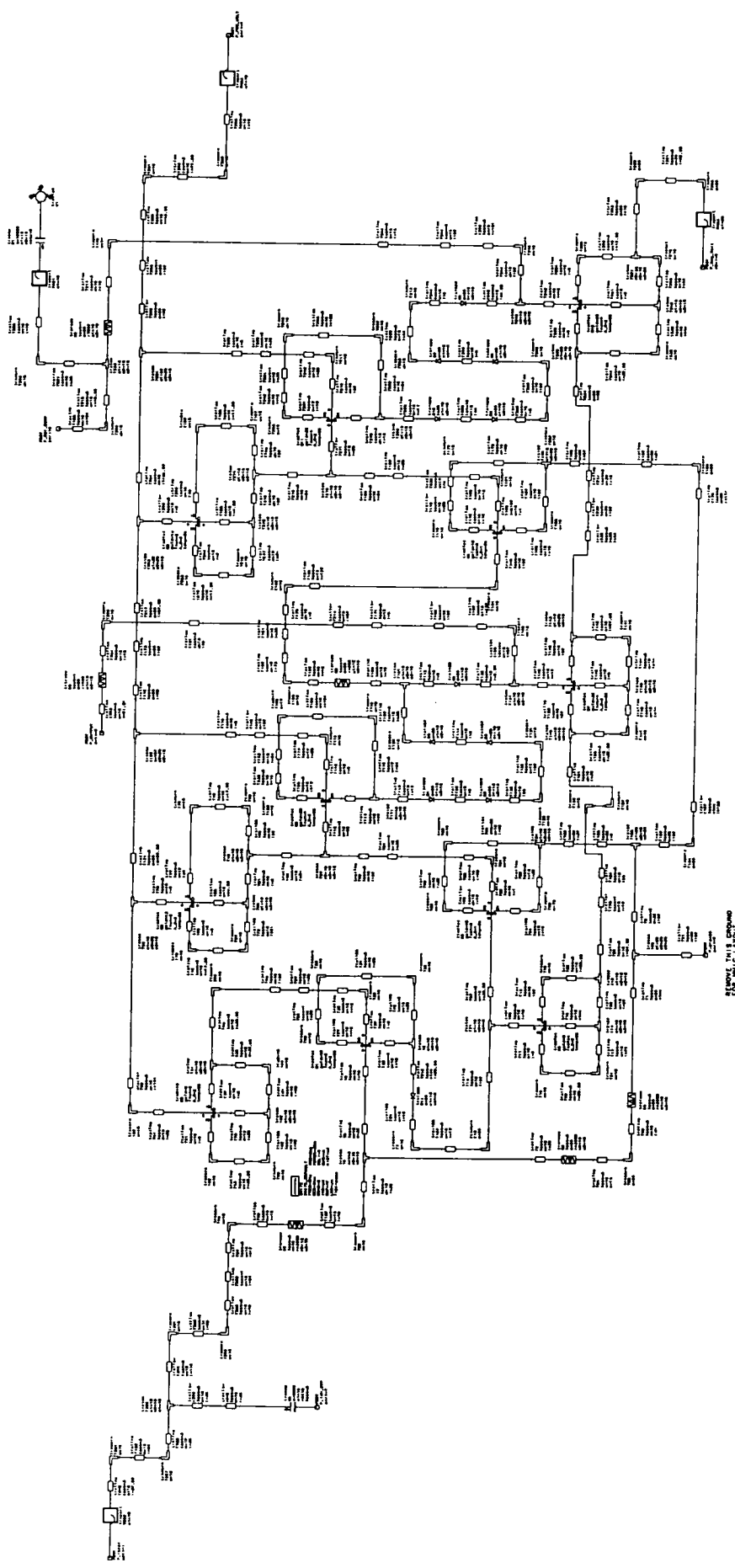
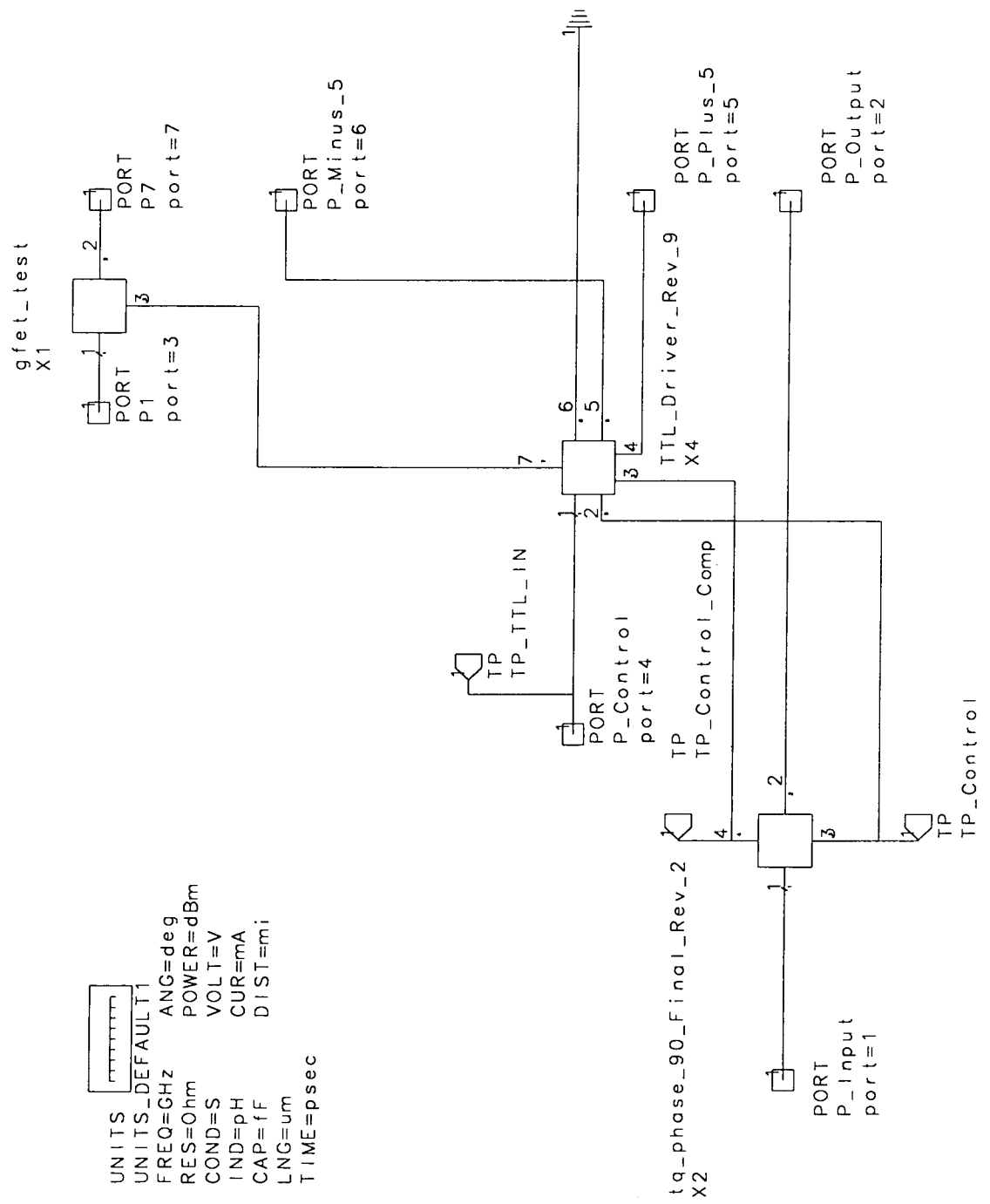


Figure 10. Schematic for TTL driver with layout items

MERGED PHASE SHIFTER AND DRIVER - M. LONG AND J. XIANG  
 DECEMBER 12, 1998



UNITS  
 UNITS\_DEFAULT1  
 FREQ=GHz  
 RES=Ohm  
 COND=S  
 IND=pH  
 CAP=fF  
 LNG=um  
 TIME=psec  
 ANG=deg  
 POWER=dBm  
 VOLT=V  
 CUR=mA  
 DIST=mi

Figure 13. Schematic for driver-to-phase shifter interconnections.

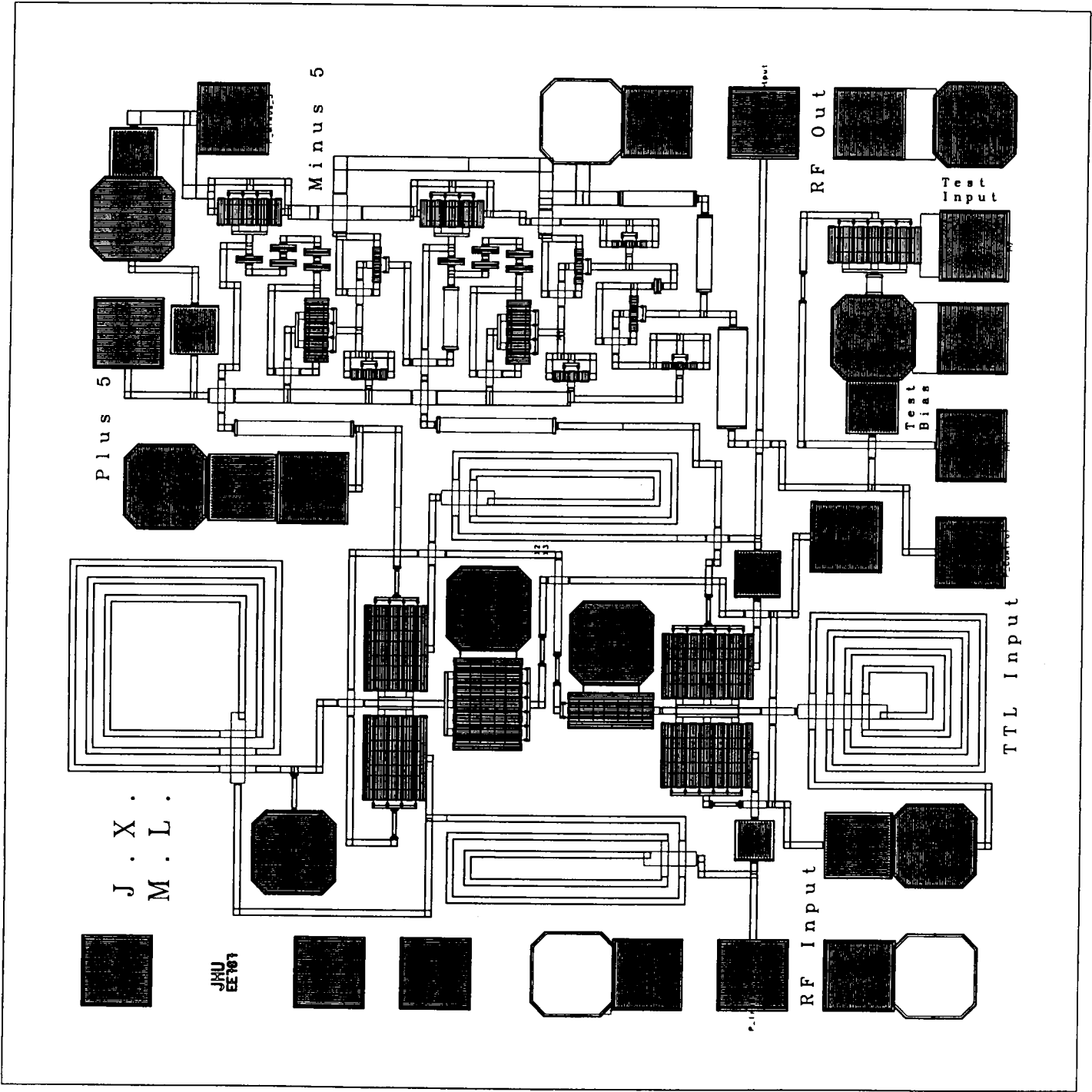


Figure 14. Complete Phase Shifter MMIC Layout.

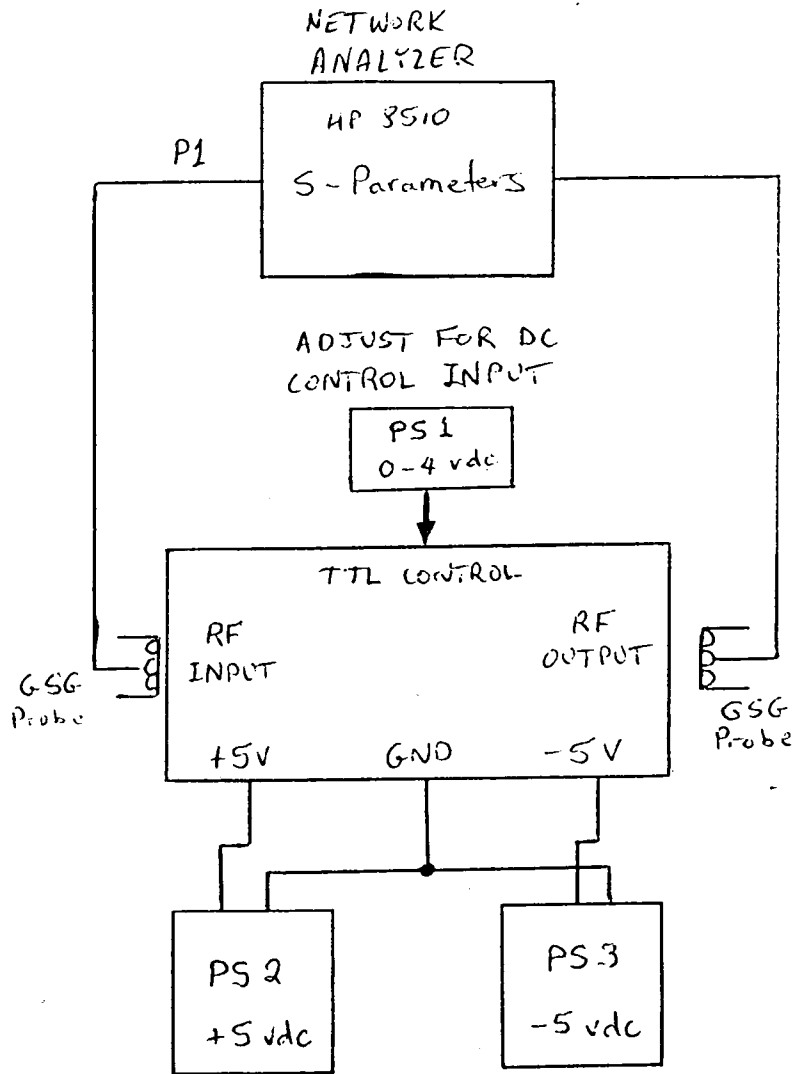


Figure 15. Test Set-up for the 90 degree Phase Shifter

**MMIC UHF / VHF General Purpose Amplifier Project**

**Final Report**

**EE525.787**

**December 14, 1998**

**Julio Varela**

**Chuck Moses**



## 1. SUMMARY

A MMIC general-purpose amplifier designed to cover the frequencies ranging from 30 MHz to 1500 MHz can serve many applications. One application is as an element in an intermediate frequency (IF) amplifier chain. The amplifier described in this manuscript is intended to complete a series of chips designed for the emerging C band wireless applications that were the focus of the 1998 Johns Hopkins University MMIC course (EE 525.787). The chips are designed based on the TriQuint TRx process --- a 0.6  $\mu\text{m}$  gate length GaAs process --- with a maximum chip area of 60 mil by 60 mil. In designing the general-purpose amplifier, the chosen topology was a DC coupled, bias stabilized FET design with feedback tuned for broadband gain and good VSWR across the entire operating band. As a goal, the amplifier is to achieve a gain of 18 dB, greater than 12 dBm output power, a third-order intercept point of +25 dBm, input and output VSWR (into 50 Ohms) of less than 1.5:1, and operate from dual 5 Volt supplies. Our simulations, based on the TriQuint TRx models and 5 Volt supplies, show a gain exceeding 20 dB from 30 MHz to above 2 GHz, an output power near 8 dBm, a third-order intercept greater than 25 dBm, input and output VSWR of 1.3:1 (or better) across the band. The only specification not met is on output power; however, greater power can be achieved by simply increasing the supply voltages at the possible expense of increased DC at the input and output ports.

## 2. INTRODUCTION

The amplifier described here is intended to operate from 30 MHz to 1500 MHz and may serve as an element in an IF amplifier chain. The design philosophy is based on the concept of active loads to realize a very wide-band amplifier for which the operating frequency range spans over six octaves. Using active elements as loads offers additional benefits other than wide-band performance; for example, with current sources taking the place of bias chokes, chip area is significantly reduced. In addition, the current source offers a degree of bias stabilization that is difficult to obtain with purely passive elements. The active load bias topology is not without some drawbacks, however, since amplifiers designed around such a topology usually display high noise figure and require dual supplies. Never the less, to obtain the desired performance, this topology seems most attractive.

The circuit schematic is shown in Figure 4-1 and layout in Figure 4-2; as can be seen, the circuit contains seventeen inherently nonlinear devices, eleven of which are depletion mode FETs, and the remaining six are overlap diodes. The only other circuit elements on-chip are two bypass capacitors and a feedback resistor; off-chip we require additional bypassing and a matching resistor at the input. As shown in the schematic, the circuit can be considered as a cascade of two stages with the differential pair (Q4 and Q5) at the front-end of the second stage. The two stages are similar in their use of active loads for current sources, but differ in the type of intra-stage feedback employed. The first stage uses resistive feedback (R3), while the second stage uses a common-source differential pair. For the differential pair, the feedback element (Q5) is made smaller than the input element (Q4) to allow for gain and still have high input impedance.

Design of the circuit began by first choosing the approximate sizes of the FETs (based on the IV curves) to handle the desired output power of +12 dBm. Then, since Q1 is to serve as a match to

50 Ohms, its gate size was chosen around 150  $\mu\text{m}$ . The diode chains seen in both the first and second stage take the place of inter-stage coupling capacitors and drop the DC level to zero volts for proper DC coupling at the ports. The feedback resistance ( $R_3$ ) in the first stage was chosen as a tradeoff between input match and gain. After setting all the initial values for each stage, the stages were designed independently for good input and output matching, high gain, and high third-order intercept. By changing the sizes of various FETs in the circuit it is possible to find values that make the gain large with little output power and also values with less gain and more output power. The chosen design values seem to be a good compromise between these extremes, with more emphasis on higher gain than on greater output power. If more output power is desired---and with similar gain---the best solution may be to simply increase the operating supplies a few volts. With the models available, we are unable to determine the noise figure of the amplifier, although we expect that it will be worse than a narrow-band conventional amplifier circuit due to the increased shot noise and high  $1/f$  noise of the active load current source components.

### 3. MODELED PERFORMANCE

Table 3-1 shows the specification compliance matrix for the amplifier design. The results were obtained from the LIBRA simulation of the Pre-Layout and Post-Layout configurations. Refer to

TABLE 3-1 Specification Compliance Matrix				
Specification Description	Requirement	Pre-Layout Simulation Result	Post-Layout Simulation Result	Compliance
Frequency	30 to 1500 MHz (2 GHz, Goal)	30 to 2000 MHz	30 to 2000 MHz	Meets Requirement
Gain	> 15 dB	> 20 dB	> 20 dB	Exceeds Requirement
Output Power	> 12 dB @ 1 dB Compression	≈ 8 dBm	≈ 8 dBm	Below Requirement
Output IP3	+25 dBm (Goal)	25.8 dBm	24.96 dBm	Meets Requirement
VSWR, 50 ohms	< 1.5:1 Input / Output (Goal)	< 1.32:1	< 1.32:1	Exceeds Requirement
Supply Voltage	± 5V (Goal)	± 5V	± 5V	Meets Requirement
Layout Size	60 x 60 mil. ANACHIP	NA	60 x 60 mil. ANACHIP	Meets Requirement

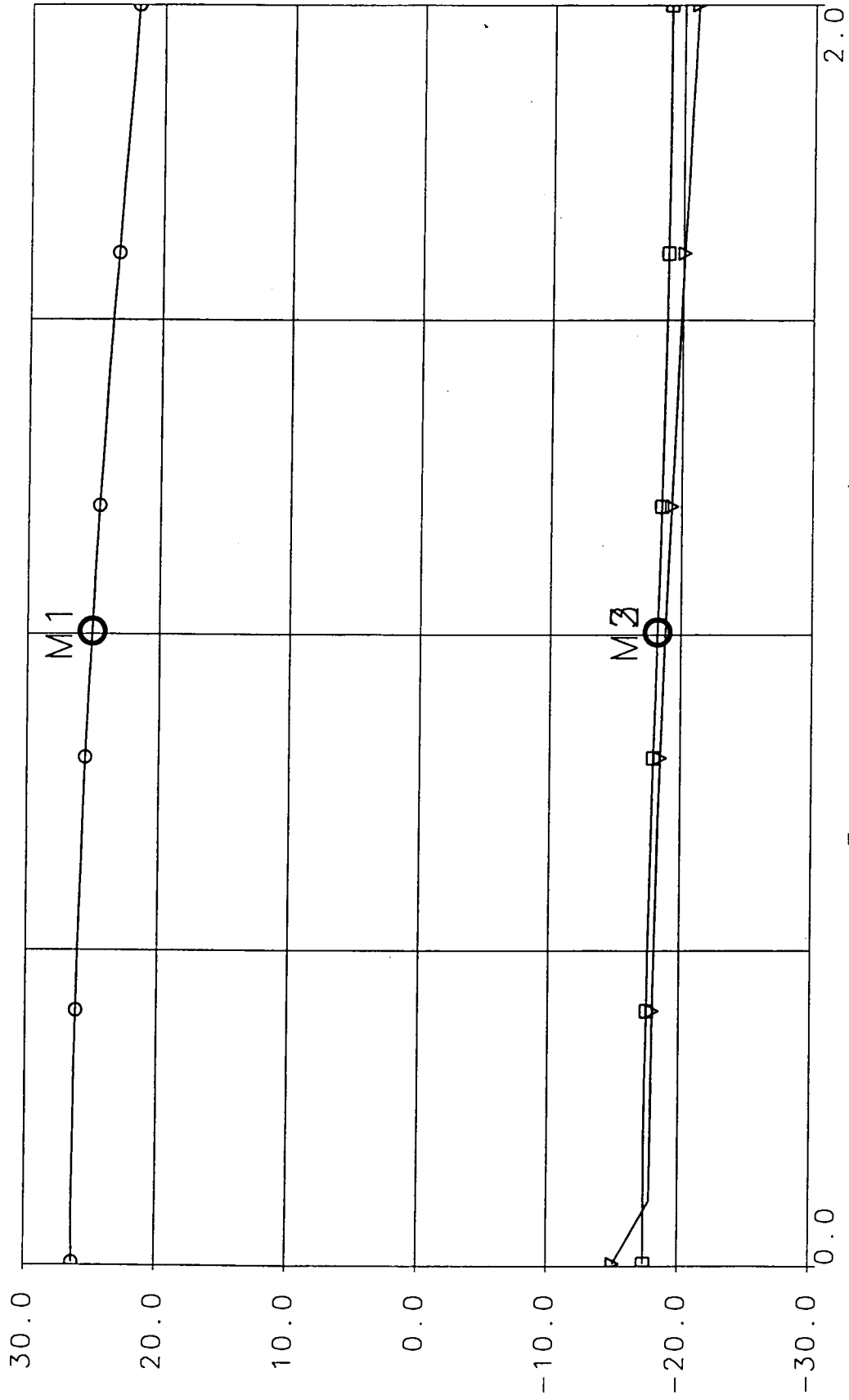
Figures 3-1 through 3-4 for the pre-layout modeled circuit simulation results and Figures 3-5 through 3-8 for the post-layout modeled circuit simulation results. All of the requirements were either met or exceeded with the exception of the output power. The output power requirement will be re-evaluated during chip testing by attempting to increase the DC bias voltage with the intentions of yielding a higher output power.

FIGURE 3-1 FRE-LAYOUT S11, S21, and S22

final\_project\_tb  
 SMAT1  
 final\_project  
 S[1,1]  
 dB

final\_project\_tb  
 SMAT1  
 final\_project  
 S[2,1]  
 dB

final\_project\_tb  
 SMAT1  
 final\_project  
 S[2,2]  
 dB

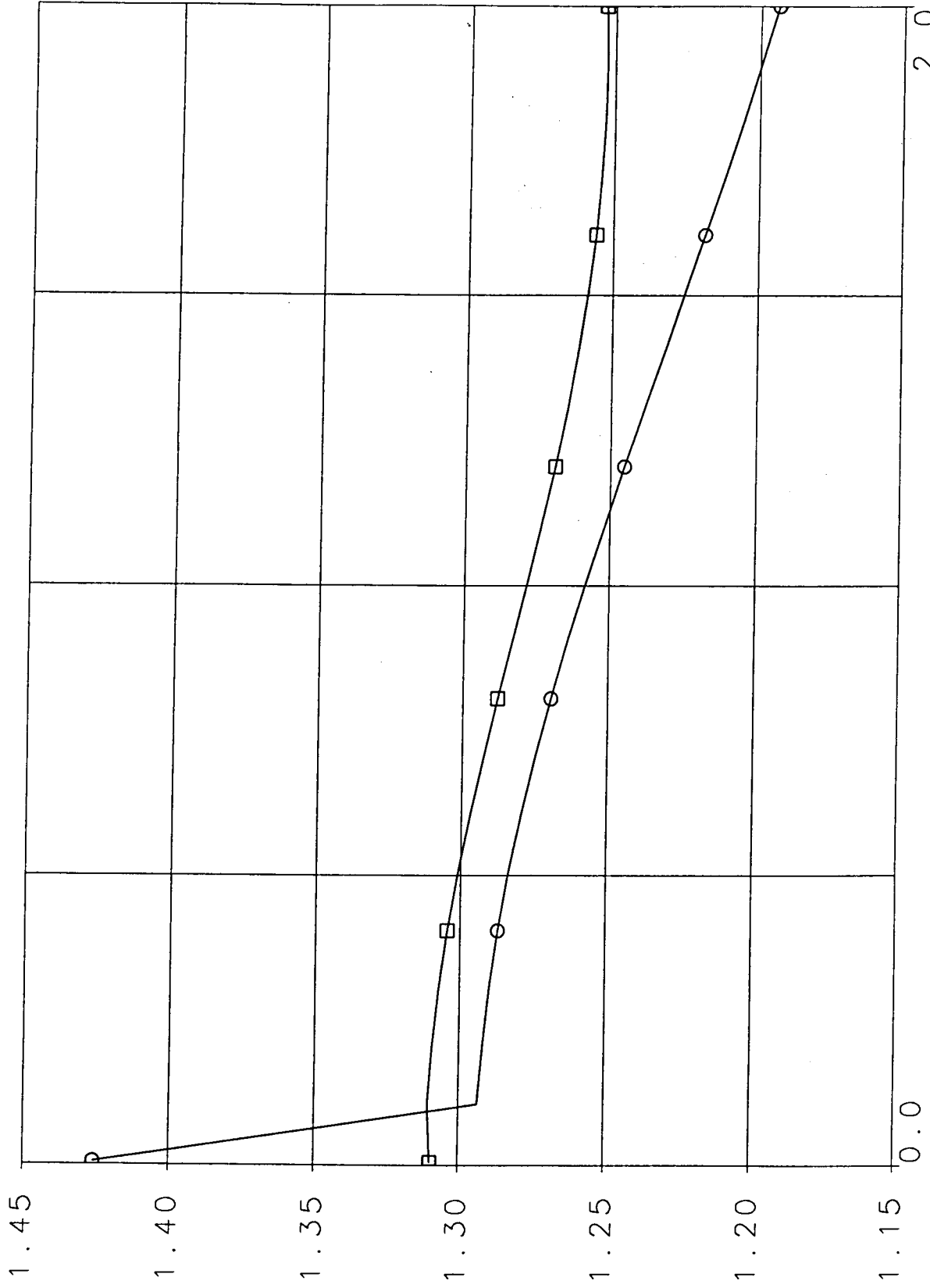


Frequency 0.5 GHz/DIV

M1 Frequency=1.00500000 value=25.1248293  
 M2 Frequency=1.00500000 value=-18.2545060  
 M3 Frequency=1.00500000 value=-18.2545060

□ final\_project\_tb  
VSWR1  
final\_project  
VSWR[1]

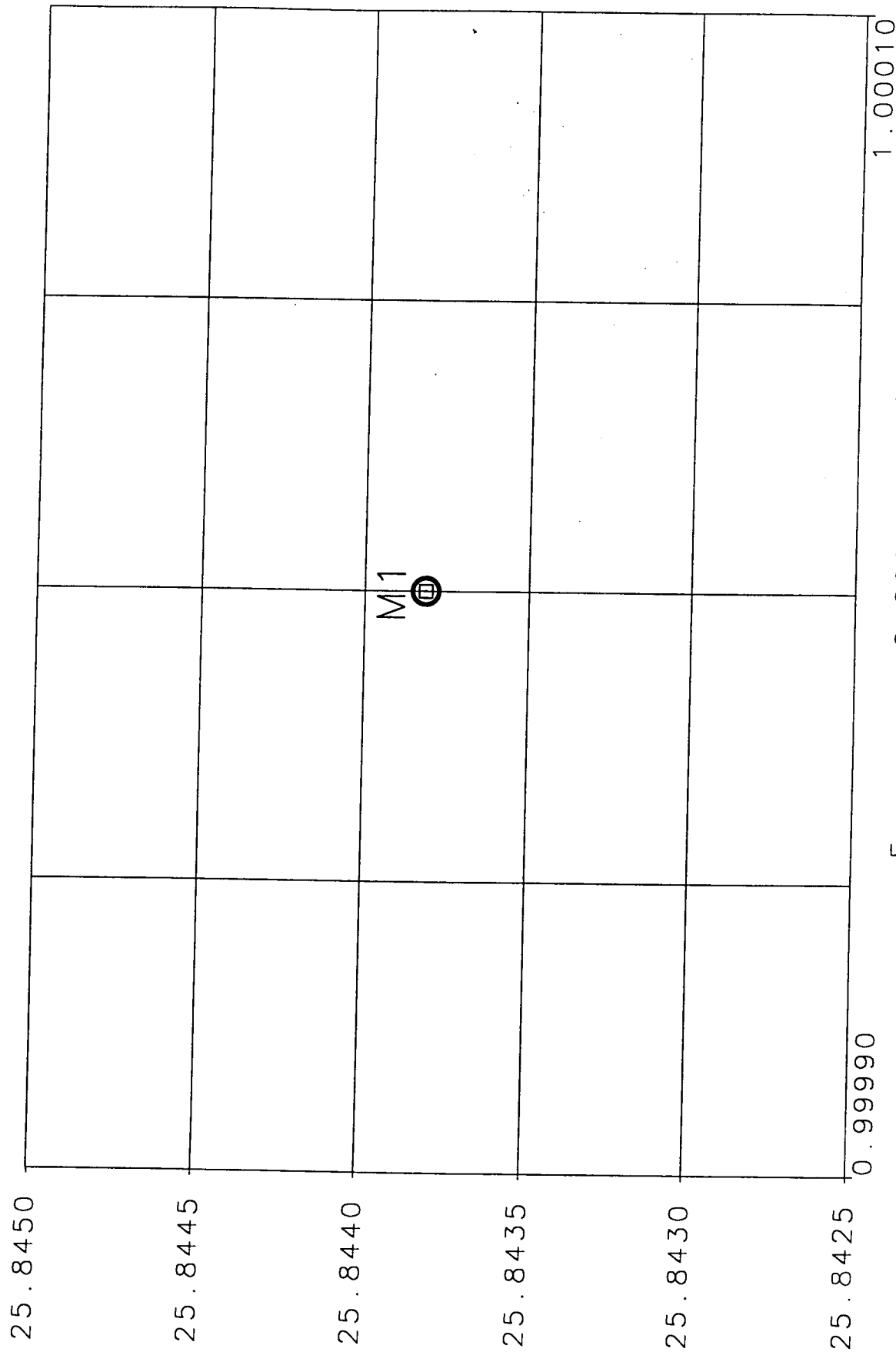
○ final\_project\_tb  
VSWR2  
final\_project  
VSWR[2]



Frequency 0.5 GHz/DIV

FIGURE 3-3 PRE-LAYOUT LFS

finalproject\_hb\_tb  
IP1  
final\_projec  
IP  
dBm



M1 Frequency=1.00000000 value=25.8438145  
Frequency 0.00005 GHz/DIV

□ finalproject\_hb\_tb  
PF2  
final\_projec  
PF  
dBm

○ finalproject\_hb\_tb  
PF1  
final\_projec  
PF  
dBm

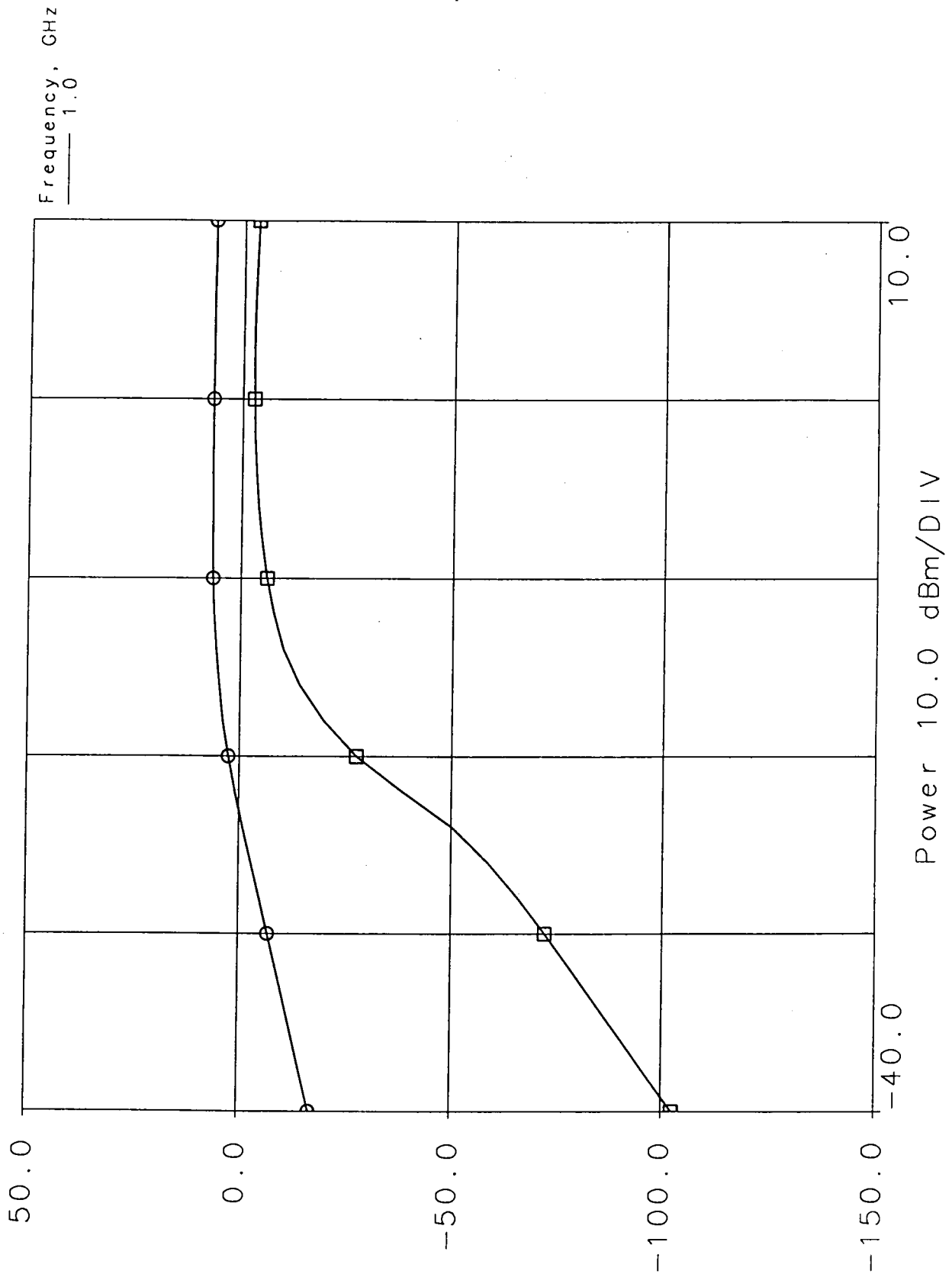
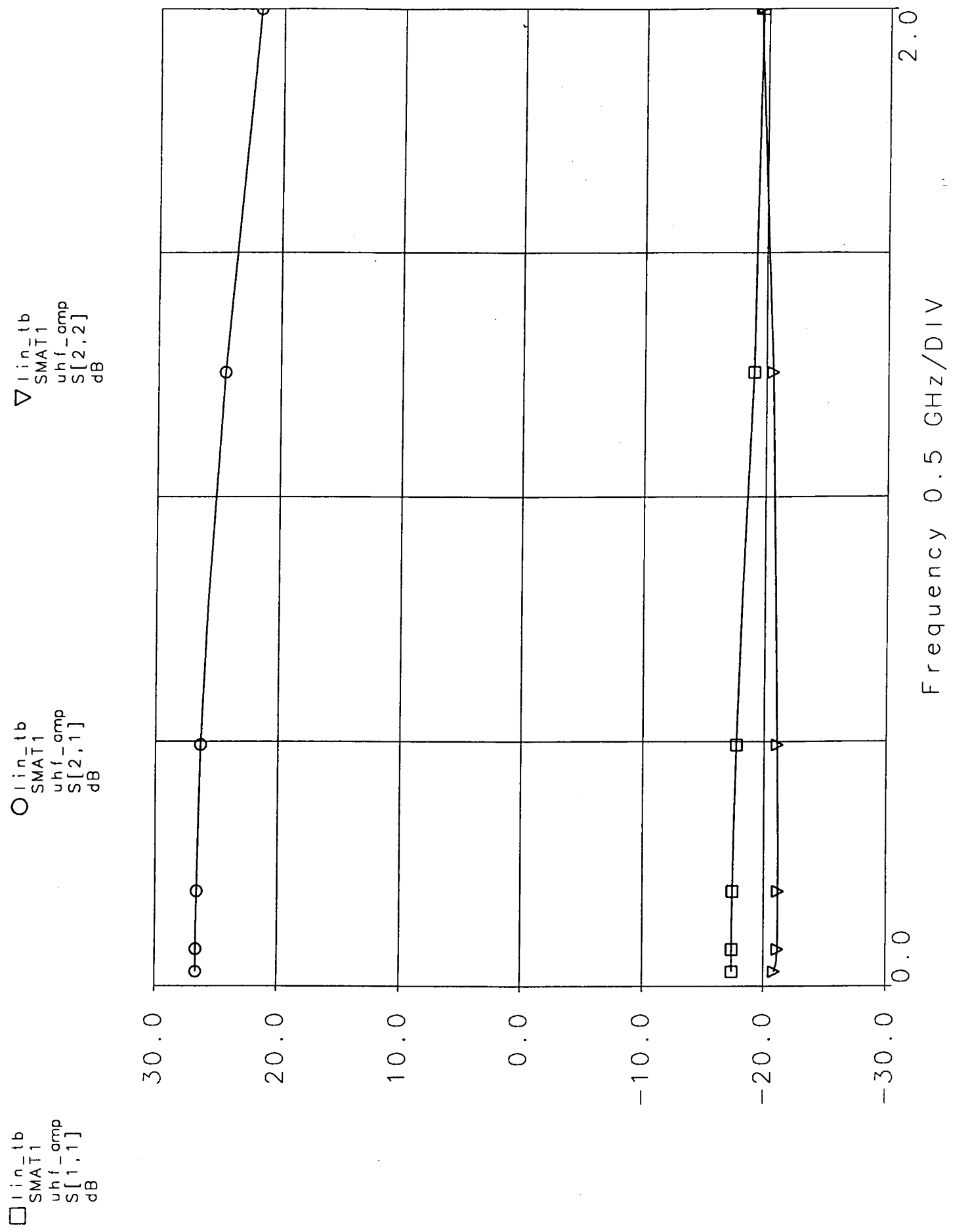




FIGURE 5-3 POST-LAYOUT S11, S21, S22



lin\_tb  
VSWR1  
uhf\_amp  
VSWR[1]

lin\_tb  
VSWR2  
uhf\_amp  
VSWR[2]

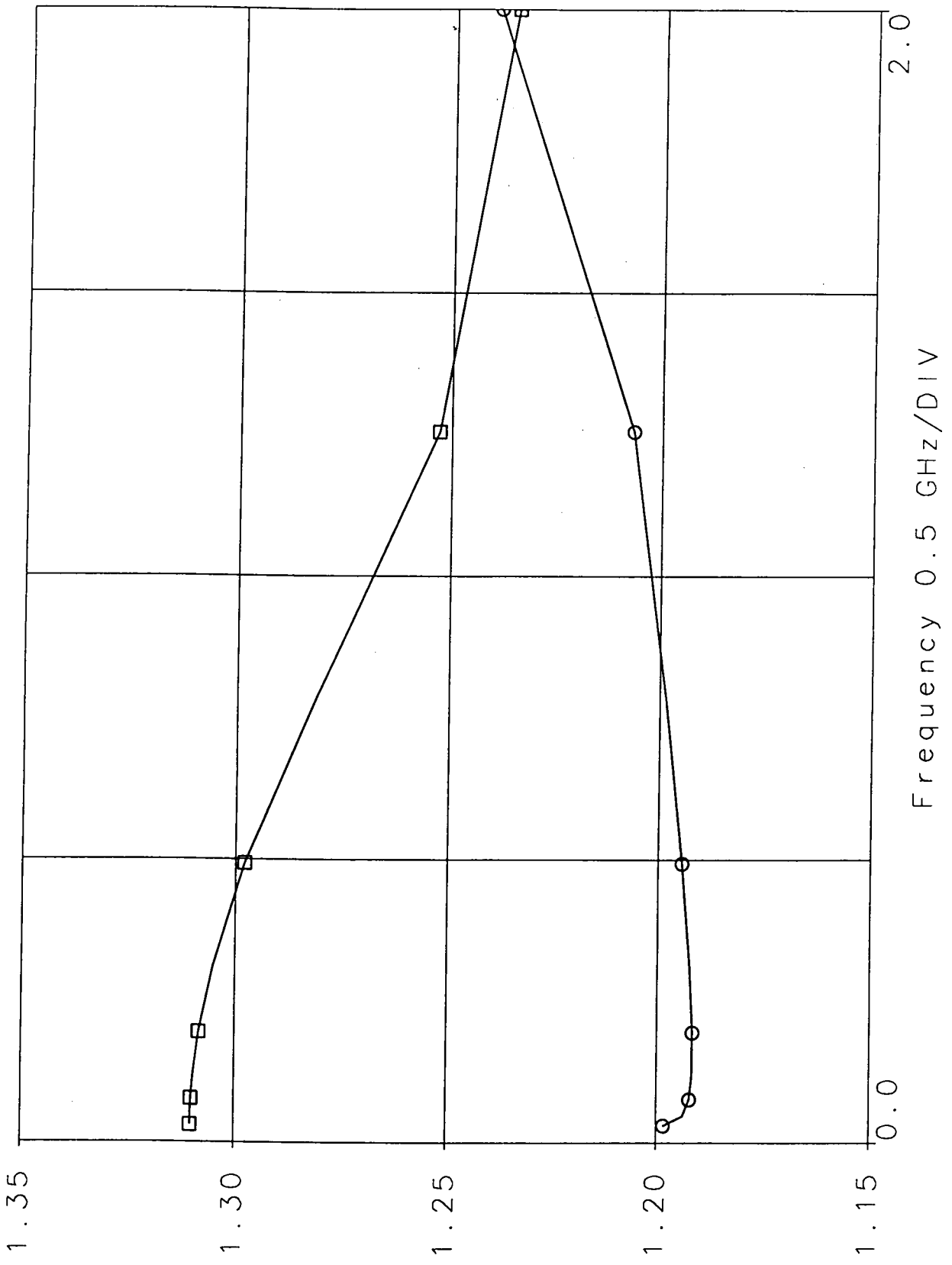
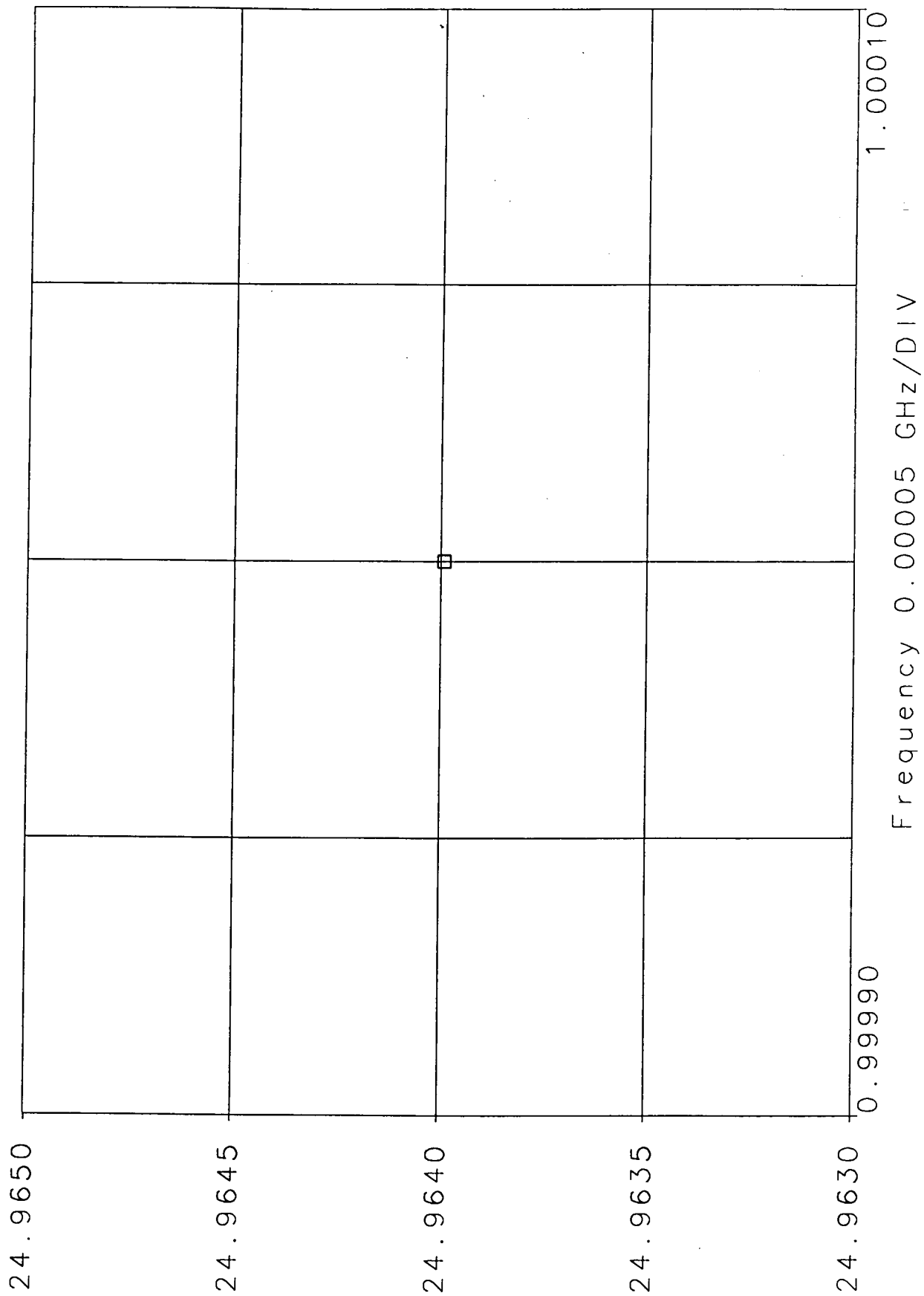


FIGURE 5-1 TEST-LAYOUT #10

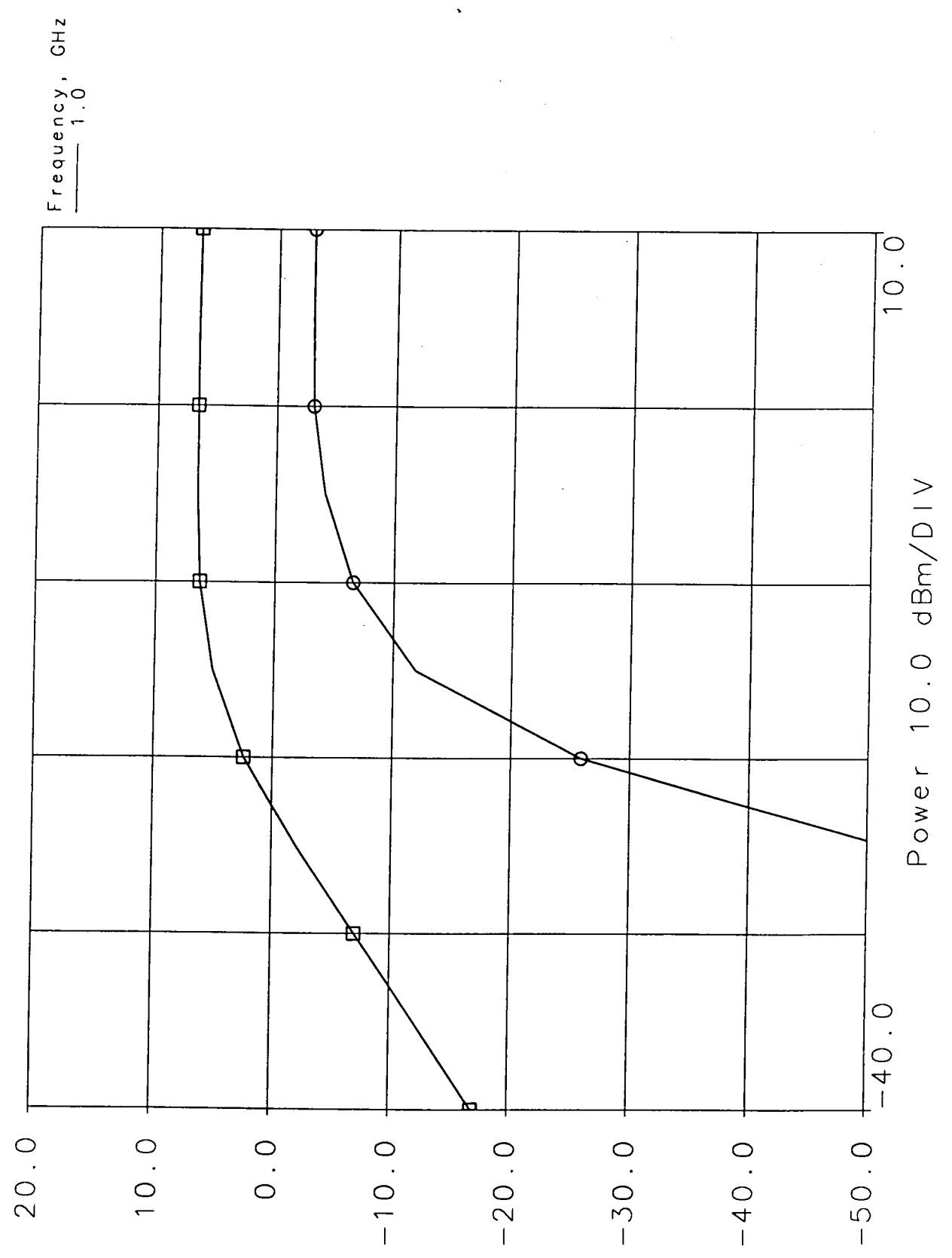
□ nonlin\_tb  
IP1  
uhf\_omp  
IP  
dBm



PF1 - 40.0 dBm  
PF2 - 10.0 dBm  
uhf\_omp  
nonlin\_tb

□ nonlin\_tb  
PF1  
uhf\_omp  
PF  
dBm

○ nonlin\_tb  
PF2  
uhf\_omp  
PF  
dBm



#### 4. SCHEMATIC DIAGRAMS

Figure 4-1 shows the schematic diagram used in the pre-layout simulations. It also gives a representation of some of the off chip components that are required to make the circuit work. These components include the input 50 ohm terminating resistor (designated as R1 in the schematic), supply line decoupling capacitors, and DC power supplies. The simulation was performed with large decoupling capacitors due to the frequency of interest. Capacitors of this magnitude can not be implemented on chip due to the physical size of the capacitor and the layout size design constraints. Figure 4-2 shows the on chip layout. Smaller decoupling capacitors were implemented on chip. External decoupling capacitors mounted in parallel on chip capacitance will be implemented during testing to make up for the additional capacitance.

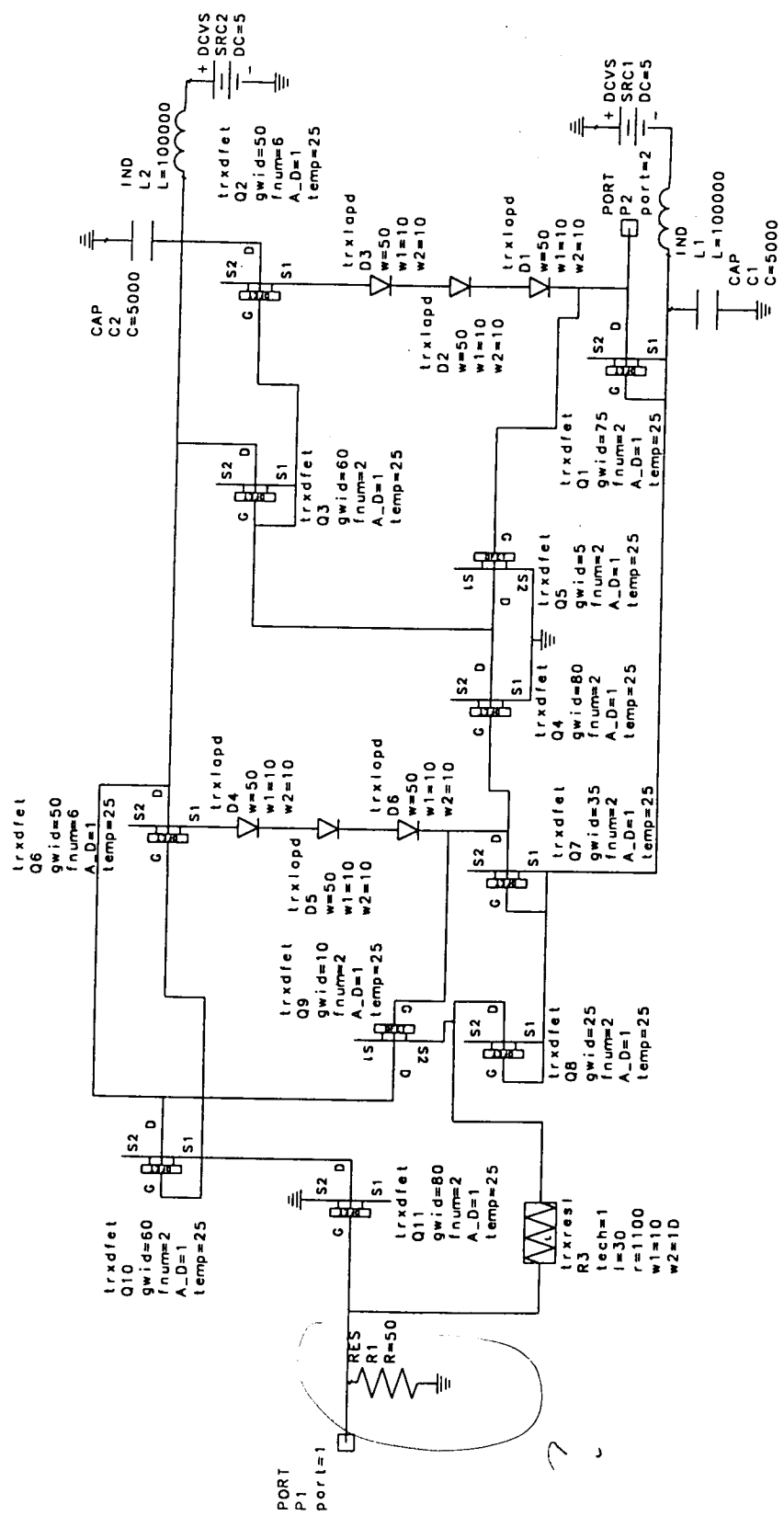
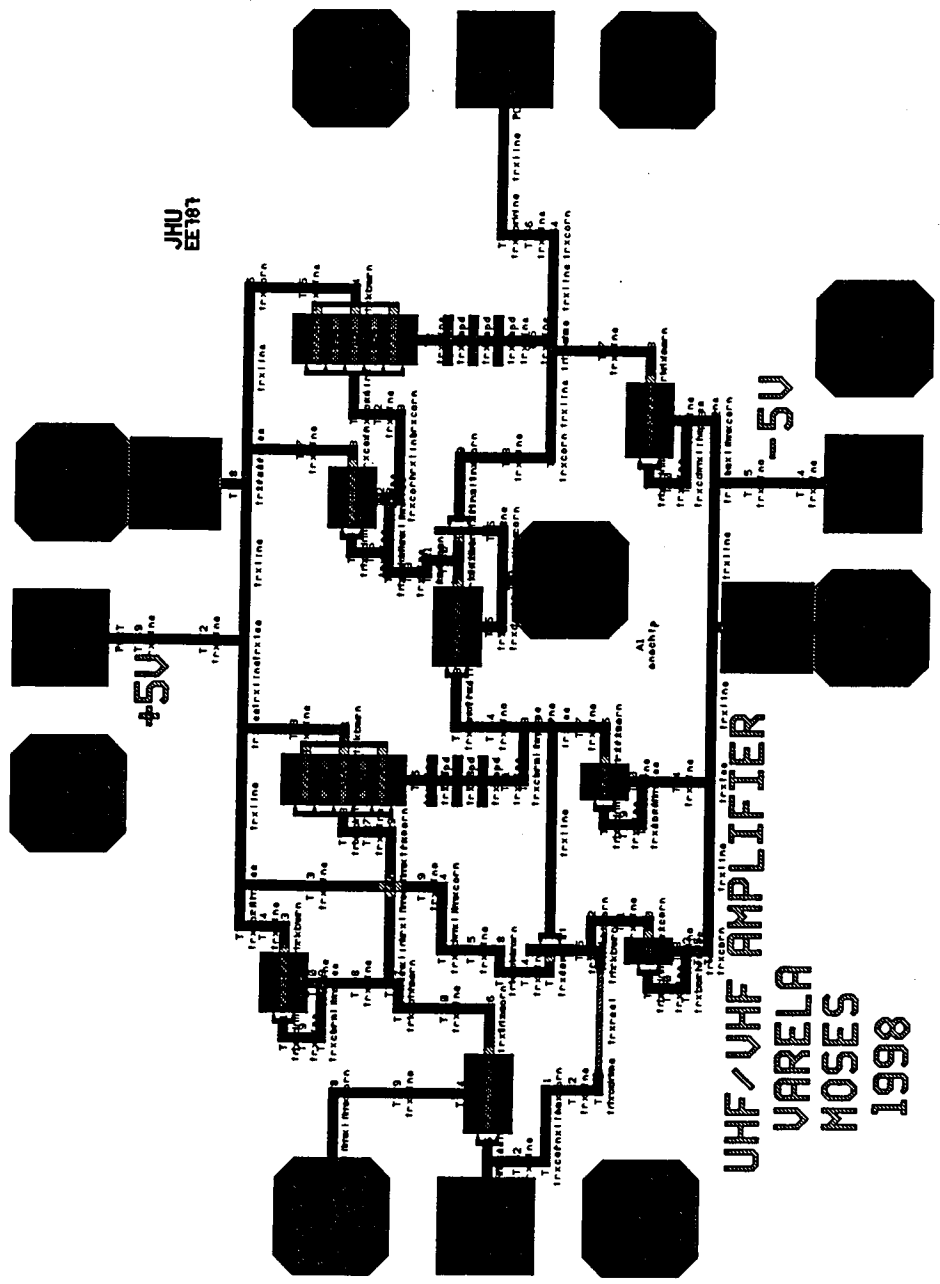


FIGURE 4-1 SIMULATION SCHEMATIC DIAGRAM

alph



alph

FIGURE 4-2 ON-CHIP COMPONENT LAYOUT

## 5. TEST PLAN

The following parameters will be evaluated under the test plan:

- Frequency Range
- Gain
- Output Power
- Output IP<sup>3</sup>
- VSWR

The following outlines the test configurations and test procedures that will be used to verify the performance of the amplifier against the modeled simulations.

### 5.1 Frequency Range

Figure 5-1 shows the test equipment configuration for measuring the frequency range.

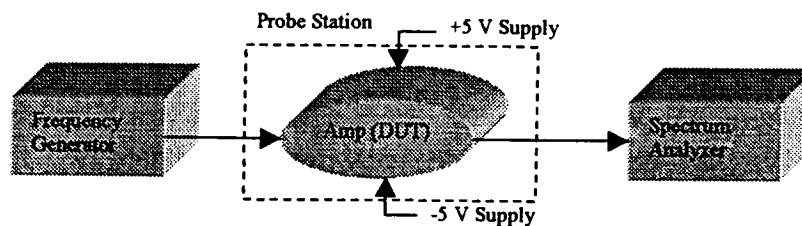


Figure 5-1 Frequency Measurement Configuration

The following outlines the procedure for performing the measurement:

1. Setup the Signal Generator to step the frequency in 100 MHz steps (approximately 20 measurements) from 30 MHz to 2000 MHz .
2. Set the output power of the signal generator to -20 dBm.
3. Step the generator frequency and note the output power level on the spectrum analyzer.  
Record the results and continue increasing the frequency until the -3 dB point is measured.
4. Graph results and compare to simulated data.



## 5.2 Gain

1. Using the graph from 5.1 calculate the mid band gain (at approximately 1000 MHz) by subtracting the input power level from the measured output power at the particular frequency.
2. Compare to simulated data.

## 5.3 Output Power

1. Using the same test configuration as Figure 5-1, set the generator to a nominal frequency of 1000 MHz.
2. Setup the frequency generator to step its output power from  $-60$  dBm to  $+20$  dBm in  $+5$  dBm steps.
3. Step the generator power and record the power level at the spectrum analyzer for each step. Note the point at which the amplifier output power is compressed by 1 dB.
4. Graph  $P_{out}$  vs.  $P_{in}$  and compare with the simulated results.

## 5.4 $IP^3$

Figure 5-2 shows the test equipment configuration for measuring the  $IP^3$ .

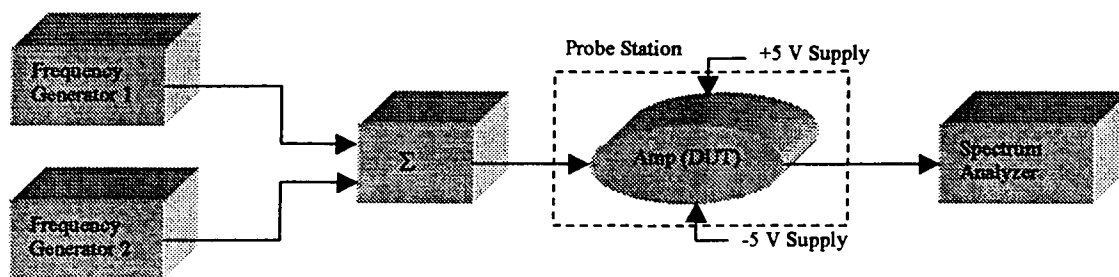


Figure 5-2  $IP^3$  Measurement Configuration

The following outlines the procedure for performing the measurement:

1. Select frequency 1 and frequency 2 to perform the two-tone 3<sup>rd</sup> order intermodulation distortion measurement. The frequencies should be selected close enough together so that the intermodulation terms fall within the passband of the amplifier.
2. Setup frequency generator #1 to step its output power from -60 dBm to +20 dBm in +5 dBm steps.
3. Set Frequency 1 to 1000MHz.
4. Setup frequency generator #2 to step its output power from -60 dBm to +20 dBm in +5 dBm steps.
5. Set Frequency 2 to 1000 MHz + (0.01)1000 MHz.
6. Step the generator powers simultaneously and record the power level at the spectrum analyzer, for each step, for the fundamental frequency and the 3<sup>rd</sup> order term. Plot, on the same graph, Pout vs. Pin for the fundamental and Pout vs. Pin for the 3<sup>rd</sup> order term.
7. On the graph, extend the linear region of the two measurements and note the corresponding value of the intersection.

## 5.5 VSWR

Figures 5-5.1 and 5-5.2 shows the test equipment configuration for measuring the VSWR.

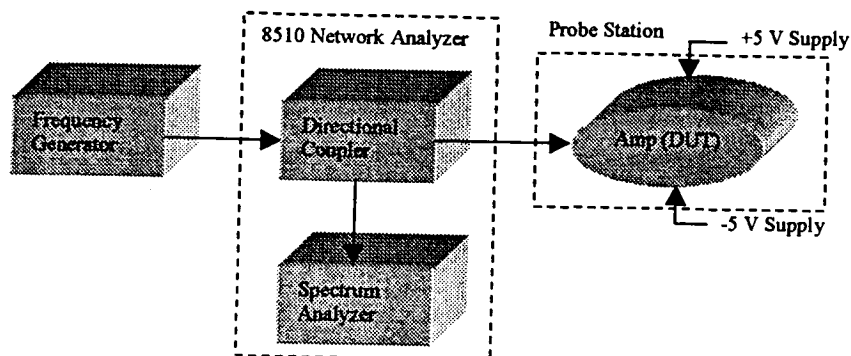


Figure 5-5.1 Input VSWR Measurement Configuration

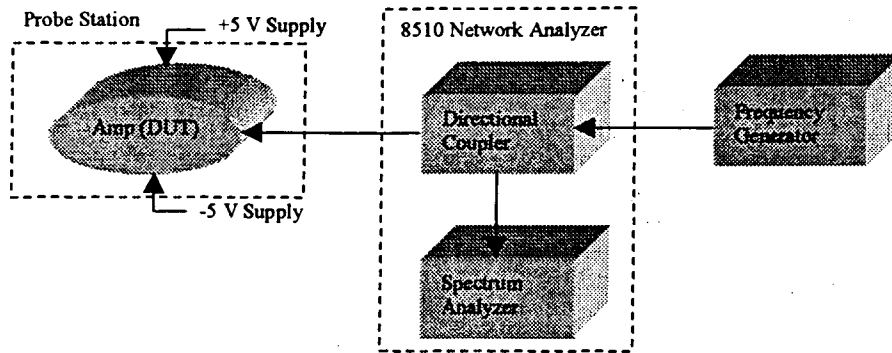


Figure 5-5.2 Output VSWR Measurement Configuration

The following outlines the procedure for performing the measurement:

1. Configure the 8510 Network Analyzer.
2. Measure S11 and S22 and determine the input and output VSWR.
3. Compare with simulated results.

## 6. CONCLUSIONS

The MMIC general-purpose amplifier design presented in this report can serve as the IF amplifier for a broad range of wireless products; one application is as a part of a wireless chip-set designed for C band. With no tunable elements and small size, this chip offers a very attractive solution for providing low cost elements for hand-held and portable communications products. Our design met all but one of the requirements set forth in the specifications; we were unable to provide the specified output power using the suggested supply voltages. As a recommendation, if increased IF power is required, the supply operating voltages can be increased. Additionally, it would be interesting to consider a design of this amplifier using a single ten or twelve volt supply to relieve the burden of having two supplies.

! Libra(R) 6.1 300 Dec 5 1996  
! Mon Dec 7 19:28:23 1998 lin\_tb\uhf\_amp  
# GHz S MA R 50.0000

! SCATTERING PARAMETERS :

0.03000	0.13431	178.845	21.6024	-3.33846	0.00013	-78.1760	0.09021	162.193
0.03130	0.13431	178.887	21.6024	-3.37005	0.00013	-77.5118	0.08995	162.810
0.03266	0.13431	178.927	21.6023	-3.40869	0.00012	-76.8265	0.08971	163.388
0.03407	0.13431	178.964	21.6022	-3.45434	0.00012	-76.1190	0.08949	163.929
0.03555	0.13431	178.999	21.6020	-3.50696	0.00011	-75.3879	0.08929	164.436
0.03709	0.13431	179.032	21.6017	-3.56654	0.00011	-74.6322	0.08911	164.910
0.03870	0.13431	179.062	21.6014	-3.63311	0.00010	-73.8506	0.08895	165.353
0.04037	0.13431	179.090	21.6010	-3.70672	0.00010	-73.0418	0.08880	165.765
0.04212	0.13431	179.116	21.6006	-3.78744	0.00009	-72.2047	0.08867	166.148
0.04395	0.13430	179.141	21.6000	-3.87535	0.00009	-71.3380	0.08854	166.503
0.04585	0.13430	179.163	21.5995	-3.97057	0.00009	-70.4404	0.08843	166.831
0.04784	0.13430	179.184	21.5988	-4.07322	0.00008	-69.5108	0.08833	167.134
0.04991	0.13429	179.203	21.5981	-4.18345	0.00008	-68.5479	0.08824	167.411
0.05207	0.13429	179.220	21.5973	-4.30144	0.00008	-67.5504	0.08815	167.663
0.05433	0.13429	179.236	21.5964	-4.42736	0.00007	-66.5171	0.08807	167.892
0.05669	0.13428	179.250	21.5954	-4.56142	0.00007	-65.4468	0.08800	168.098
0.05914	0.13428	179.263	21.5944	-4.70384	0.00007	-64.3383	0.08794	168.281
0.06170	0.13427	179.275	21.5932	-4.85485	0.00007	-63.1903	0.08788	168.442
0.06438	0.13426	179.285	21.5919	-5.01470	0.00006	-62.0019	0.08782	168.581
0.06717	0.13426	179.294	21.5905	-5.18369	0.00006	-60.7718	0.08777	168.699
0.07008	0.13425	179.301	21.5890	-5.36208	0.00006	-59.4989	0.08773	168.796
0.07312	0.13424	179.307	21.5874	-5.55019	0.00006	-58.1822	0.08769	168.872
0.07628	0.13423	179.312	21.5856	-5.74835	0.00005	-56.8207	0.08765	168.928
0.07959	0.13422	179.316	21.5836	-5.95692	0.00005	-55.4135	0.08762	168.963
0.08304	0.13421	179.318	21.5815	-6.17624	0.00005	-53.9597	0.08759	168.978
0.08664	0.13420	179.319	21.5792	-6.40671	0.00005	-52.4586	0.08756	168.972
0.09039	0.13418	179.319	21.5767	-6.64875	0.00005	-50.9094	0.08753	168.947
0.09431	0.13417	179.317	21.5739	-6.90276	0.00005	-49.3114	0.08751	168.901
0.09840	0.13415	179.315	21.5710	-7.16921	0.00004	-47.6642	0.08749	168.835
0.10266	0.13414	179.311	21.5678	-7.44858	0.00004	-45.9671	0.08747	168.749
0.10711	0.13412	179.306	21.5643	-7.74134	0.00004	-44.2199	0.08746	168.643
0.11175	0.13410	179.300	21.5605	-8.04803	0.00004	-42.4221	0.08745	168.516
0.11659	0.13407	179.293	21.5564	-8.36919	0.00004	-40.5736	0.08743	168.369
0.12164	0.13405	179.284	21.5519	-8.70539	0.00004	-38.6741	0.08743	168.200
0.12692	0.13402	179.275	21.5470	-9.05724	0.00004	-36.7233	0.08742	168.010
0.13242	0.13399	179.264	21.5417	-9.42534	0.00004	-34.7213	0.08741	167.799
0.13815	0.13396	179.252	21.5360	-9.81036	0.00004	-32.6678	0.08741	167.566
0.14414	0.13393	179.238	21.5298	-10.2130	0.00003	-30.5626	0.08741	167.311
0.15039	0.13389	179.224	21.5230	-10.6339	0.00003	-28.4057	0.08741	167.033
0.15690	0.13385	179.208	21.5157	-11.0739	0.00003	-26.1966	0.08741	166.732
0.16370	0.13380	179.191	21.5077	-11.5337	0.00003	-23.9351	0.08741	166.407
0.17080	0.13376	179.173	21.4990	-12.0142	0.00003	-21.6207	0.08741	166.059
0.17820	0.13370	179.154	21.4896	-12.5162	0.00003	-19.2528	0.08742	165.685
0.18592	0.13365	179.134	21.4793	-13.0406	0.00003	-16.8305	0.08743	165.287
0.19398	0.13358	179.112	21.4682	-13.5882	0.00003	-14.3527	0.08744	164.862
0.20238	0.13352	179.089	21.4561	-14.1602	0.00003	-11.8184	0.08745	164.411
0.21115	0.13344	179.066	21.4430	-14.7574	0.00003	-9.22598	0.08747	163.933
0.22030	0.13336	179.041	21.4287	-15.3809	0.00003	-6.57381	0.08749	163.427
0.22985	0.13328	179.015	21.4132	-16.0318	0.00003	-3.86001	0.08751	162.892
0.23981	0.13318	178.988	21.3963	-16.7113	0.00003	-1.08253	0.08753	162.328
0.25020	0.13308	178.960	21.3780	-17.4205	0.00003	1.76080	0.08755	161.733
0.26104	0.13297	178.931	21.3581	-18.1606	0.00003	4.67217	0.08758	161.106
0.27235	0.13285	178.901	21.3365	-18.9329	0.00003	7.65371	0.08761	160.448
0.28416	0.13272	178.871	21.3131	-19.7387	0.00003	10.7073	0.08765	159.756
0.29647	0.13258	178.840	21.2876	-20.5795	0.00003	13.8345	0.08769	159.031
0.30932	0.13242	178.808	21.2599	-21.4565	0.00003	17.0362	0.08773	158.270

0.32272	0.13226	178.776	21.2299	-22.3715	0.00003	20.3125	0.08778	157.473
0.33671	0.13207	178.744	21.1972	-23.3257	0.00003	23.6623	0.08783	156.639
0.35130	0.13188	178.713	21.1618	-24.3209	0.00003	27.0831	0.08788	155.767
0.36652	0.13167	178.681	21.1234	-25.3587	0.00003	30.5708	0.08794	154.856
0.38240	0.13144	178.650	21.0817	-26.4409	0.00003	34.1193	0.08801	153.905
0.39897	0.13119	178.621	21.0364	-27.5690	0.00003	37.7202	0.08808	152.912
0.41626	0.13092	178.593	20.9873	-28.7451	0.00003	41.3630	0.08816	151.878
0.43430	0.13063	178.566	20.9341	-29.9709	0.00003	45.0348	0.08824	150.800
0.45312	0.13031	178.542	20.8764	-31.2485	0.00003	48.7204	0.08833	149.677
0.47276	0.12998	178.521	20.8139	-32.5797	0.00003	52.4028	0.08843	148.510
0.49324	0.12961	178.505	20.7461	-33.9667	0.00003	56.0635	0.08853	147.296
0.51462	0.12922	178.492	20.6728	-35.4116	0.00003	59.6831	0.08865	146.036
0.53692	0.12879	178.485	20.5934	-36.9165	0.00004	63.2418	0.08877	144.728
0.56018	0.12834	178.485	20.5075	-38.4836	0.00004	66.7203	0.08890	143.371
0.58446	0.12785	178.493	20.4146	-40.1152	0.00004	70.1000	0.08904	141.966
0.60979	0.12732	178.510	20.3142	-41.8135	0.00004	73.3643	0.08919	140.512
0.63621	0.12676	178.538	20.2058	-43.5809	0.00004	76.4982	0.08935	139.008
0.66378	0.12616	178.579	20.0888	-45.4197	0.00005	79.4892	0.08952	137.455
0.69254	0.12551	178.634	19.9627	-47.3324	0.00005	82.3272	0.08970	135.853
0.72255	0.12483	178.706	19.8267	-49.3212	0.00005	85.0045	0.08990	134.203
0.75387	0.12410	178.798	19.6803	-51.3886	0.00006	87.5156	0.09010	132.504
0.78653	0.12333	178.912	19.5229	-53.5370	0.00006	89.8573	0.09032	130.759
0.82062	0.12251	179.052	19.3537	-55.7687	0.00006	92.0280	0.09055	128.968
0.85618	0.12165	179.221	19.1722	-58.0860	0.00007	94.0279	0.09079	127.134
0.89328	0.12075	179.423	18.9776	-60.4912	0.00008	95.8583	0.09105	125.258
0.93199	0.11980	179.662	18.7694	-62.9865	0.00008	97.5216	0.09132	123.345
0.97237	0.11881	179.943	18.5469	-65.5741	0.00009	99.0210	0.09161	121.397
1.01451	0.11778	-179.730	18.3095	-68.2558	0.00010	100.360	0.09191	119.418
1.05847	0.11673	-179.350	18.0567	-71.0337	0.00010	101.543	0.09223	117.414
1.10434	0.11564	-178.912	17.7879	-73.9095	0.00011	102.574	0.09257	115.389
1.15220	0.11454	-178.410	17.5028	-76.8849	0.00012	103.458	0.09292	113.352
1.20213	0.11342	-177.838	17.2011	-79.9612	0.00013	104.198	0.09331	111.309
1.25422	0.11231	-177.191	16.8825	-83.1400	0.00014	104.800	0.09372	109.271
1.30857	0.11121	-176.462	16.5471	-86.4223	0.00016	105.266	0.09417	107.246
1.36527	0.11015	-175.646	16.1948	-89.8093	0.00017	105.599	0.09467	105.247
1.42444	0.10913	-174.740	15.8259	-93.3020	0.00019	105.802	0.09523	103.287
1.48616	0.10817	-173.739	15.4410	-96.9015	0.00020	105.877	0.09587	101.383
1.55057	0.10731	-172.644	15.0405	-100.609	0.00022	105.822	0.09661	99.5510
1.61776	0.10656	-171.454	14.6255	-104.426	0.00024	105.636	0.09749	97.8125
1.68786	0.10594	-170.174	14.1970	-108.356	0.00027	105.312	0.09857	96.1900
1.76100	0.10547	-168.811	13.7562	-112.400	0.00030	104.838	0.09991	94.7087
1.83731	0.10519	-167.376	13.3047	-116.565	0.00033	104.197	0.10163	93.3958
1.91693	0.10511	-165.886	12.8443	-120.860	0.00037	103.358	0.10388	92.2787
2.00000	0.10523	-164.363	12.3766	-125.297	0.00041	102.270	0.10692	91.3796

bias_bench_tb	bias_bench_tb
IDC2	IDC3
uhf_amp	uhf_amp

IDC	IDC
-----	-----

Bias1

0.000000000e+00	mA	60.6973	mA	35.0051
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**MMIC Transimpedance Amplifier**  
**FALL 1998**  
**Special Project I 525.801**  
**Daniel Judy**



## 1. Introduction

Optical communication requires a way to convert optical signals to electrical signals. This is typically done with PIN photodiode, which is essentially a high impedance current source. The long distances between transmitter and receiver often mean that the signals at the receiver are small and need amplification. Modern high-speed digital communication also requires large bandwidths to accommodate the information flow. These requirements are a good match to MMIC MESFET design that uses high-input-impedance active devices with large gain bandwidth products.

In this report I'll present a deterministic method to design a maximally flat transimpedance amplifier using FET width and feedback resistance as the only design parameters. I'll also present a method to indirectly measure the transimpedance using a vector network analyzer.

## 2. Design Examples and Simulation

The following sections discuss the design and simulation of two different amplifiers. Because there are no inductors in the circuit there was plenty of room on the  $1500 \times 1500 \mu\text{m}$  anachip for two amplifiers. I decided to put both a standard Van Tuyl-Hornbuckle based transimpedance amplifier and a common-source common-gate cascode based amplifier. Section 2.1 covers the Van Tuyl-Hornbuckle design and Section 2.2 covers the cascode design.

### 2.1. SA-1 Trans-impedance Amplifier

Figure 1 shows the schematic of the Van Tuyl-Hornbuckle transimpedance amplifier design. The amplifier consists of a common source FET (CSF) amplifier followed a source-follower buffer stage. Both stages have active loads that are nominally  $\frac{1}{2}$  the area of the respective FETs. The diodes provide a DC level shift so that the output node is approximately at ground potential and are bypassed by a capacitor to provide better high-frequency performance. I have also shown feedback resistor, which sets the transimpedance of the amplifier. An additional source-follower-buffer stage has been added as well as a biasing resistor to the gate of Q1. The additional source-follower buffers the feedback path from the  $50\Omega$  load impedance and is sized ( $124\mu\text{m}$ ) for an output-impedance of  $50\Omega$ . The biasing resistor ( $R_g$ ) has been added to provide a  $-0.2\text{V}$  gate bias to Q1 so only two bias voltages are required,  $V_{dd}$  which is  $+4\text{V}$ , and  $V_{ss}$  which is  $-2\text{V}$ .

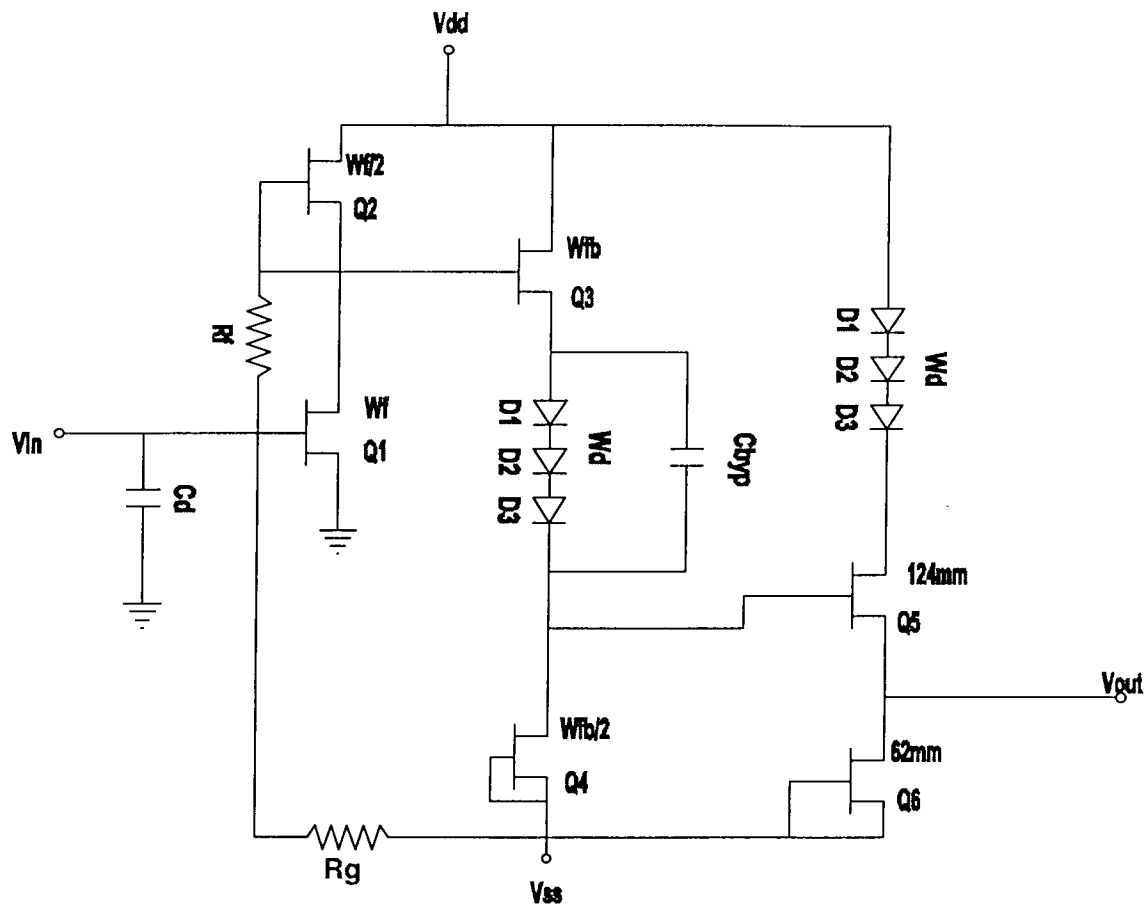


Figure 1 shows the schematic of the Van Tuyl-Hornbuckle transimpedance amplifier design.

### 2.1.1. Design Examples

I'll discuss three design examples using a maximally flat magnitude (MFM) design<sup>1</sup>. I'll present the design calculations and linear circuit simulator results. The MFM design procedure is very good for an amplifier followed by an ideal buffer amplifier that has high input impedance with only capacitive loading and an output impedance that is exactly  $50\Omega$  throughout the band of interest. Any practical source follower has output impedance that is  $50\Omega$  for only a portion of its useful band and thus will affect the flatness of the previous amplifier. What this means is that the MFM design gives a good starting point for the design and the middle FET (Q3) must be tuned (usually smaller in width) to re-flatten the response with the output buffer added. With this in mind, I'll show the transimpedance of only the first two stages and with the output buffer after tuning. Table 1 shows the design parameters of the various design examples. The first example is based on measurements of the photo diode I intend to use and the target transimpedance. This is the design I'll actually layout and submit for fabrication. The other two examples are only to illustrate the utility of the design equations.

<sup>1</sup> ARL technical report, A Maximally Flat Magnitude MMIC Transimpedance Amplifier, (not yet published)

Example	Transimpedance ( $Z_{i0}$ )	Diode Capacitance ( $C_d$ )
1	2500 $\Omega$	27.5fF
2	1000 $\Omega$	27.5fF
3	2500 $\Omega$	50fF

Table 1 shows the design parameters of the various design examples.

Parameter	Design	Ideal Simulated	Tuned
$W_f$	9.673 $\mu\text{m}$	9.673 $\mu\text{m}$	9.673 $\mu\text{m}$
$W_{fb,MFM}$	31.883 $\mu\text{m}$	31.883 $\mu\text{m}$	21 $\mu\text{m}$
$R_f$	7416 $\Omega$	7416 $\Omega$	7616 $\Omega$
$f_{c,MFM}$	2.947 GHz	3.07 GHz	3.14 GHz

Table 2 shows the circuit values calculated using the MFM design procedure for Example 1.

Table 2 shows the circuit values calculated using the MFM design procedure for Example 1. and, Figure 2 shows the response of the circuit of Example 1. The case of the CSF amplifier followed by a single source-follower is shown in blue, while the case of the SA-1 gain block followed by a 50 $\Omega$  source follower buffer is shown in red and brown. The red line shows the SA-1 with buffer circuit with the circuit parameters from the design equations and the brown line shows the response after tuning the middle FET width from 32 $\mu\text{m}$  to 21 $\mu\text{m}$  and  $R_f$  from 7416 $\Omega$  to 7616 $\Omega$ . The results are summarized in Table 2. Table 3 and Figure 3 give similar results for the Example 2 design parameters.

Parameter	Design	Ideal Simulated	Tuned
$W_f$	15.75 $\mu\text{m}$	15.75 $\mu\text{m}$	15.75 $\mu\text{m}$
$W_{fb,MFM}$	33.776 $\mu\text{m}$	33.776 $\mu\text{m}$	27 $\mu\text{m}$
$R_f$	3112 $\Omega$	3112 $\Omega$	3200 $\Omega$
$f_{c,MFM}$	4.659GHz	4.85GHz	4.45GHz

Table 3 shows the circuit values calculated using the MFM design procedure for example 2.

The simulation results for example three are shown in Table 4 and Figure 4.

Parameter	Design	Ideal Simulated	Tuned
$W_f$	12.8 $\mu\text{m}$	12.8 $\mu\text{m}$	12.8 $\mu\text{m}$
$W_{fb,MFM}$	59.111 $\mu\text{m}$	59.111 $\mu\text{m}$	54 $\mu\text{m}$
$R_f$	7250 $\Omega$	7250 $\Omega$	7450 $\Omega$
$f_{c,MFM}$	2.081GHz	2.14GHz	2.44GHz

Table 4 shows the design for example 3.

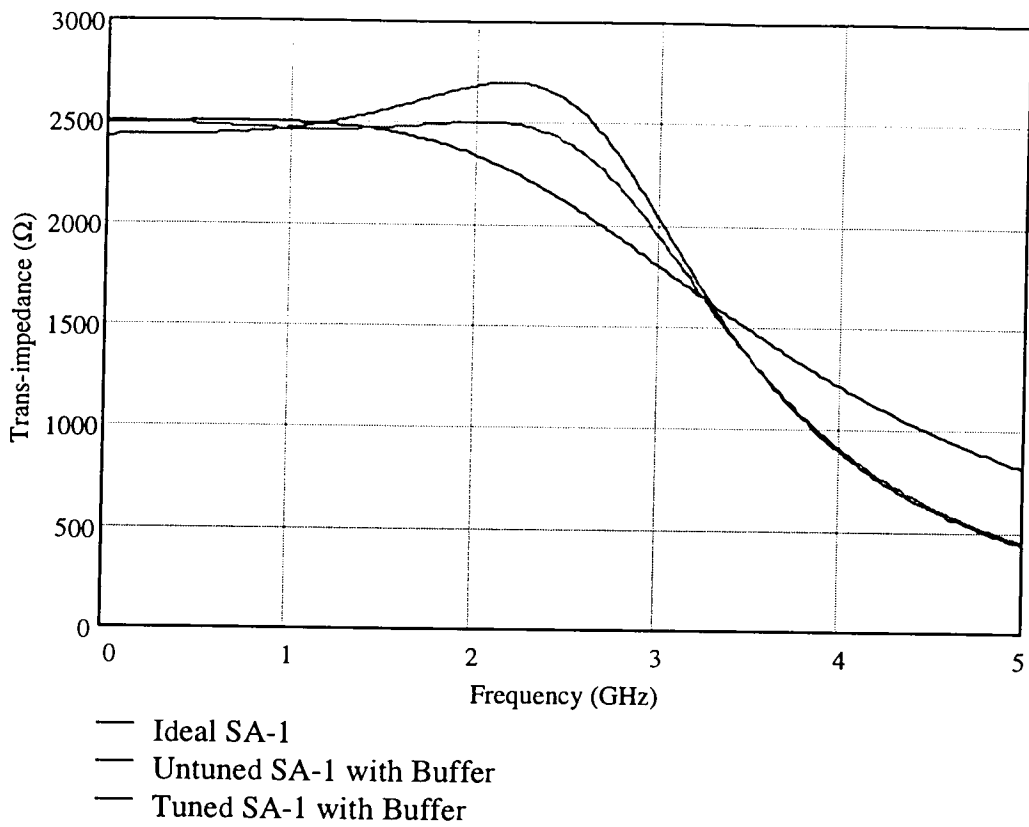


Figure 2 shows the response of the circuit of Example 1.

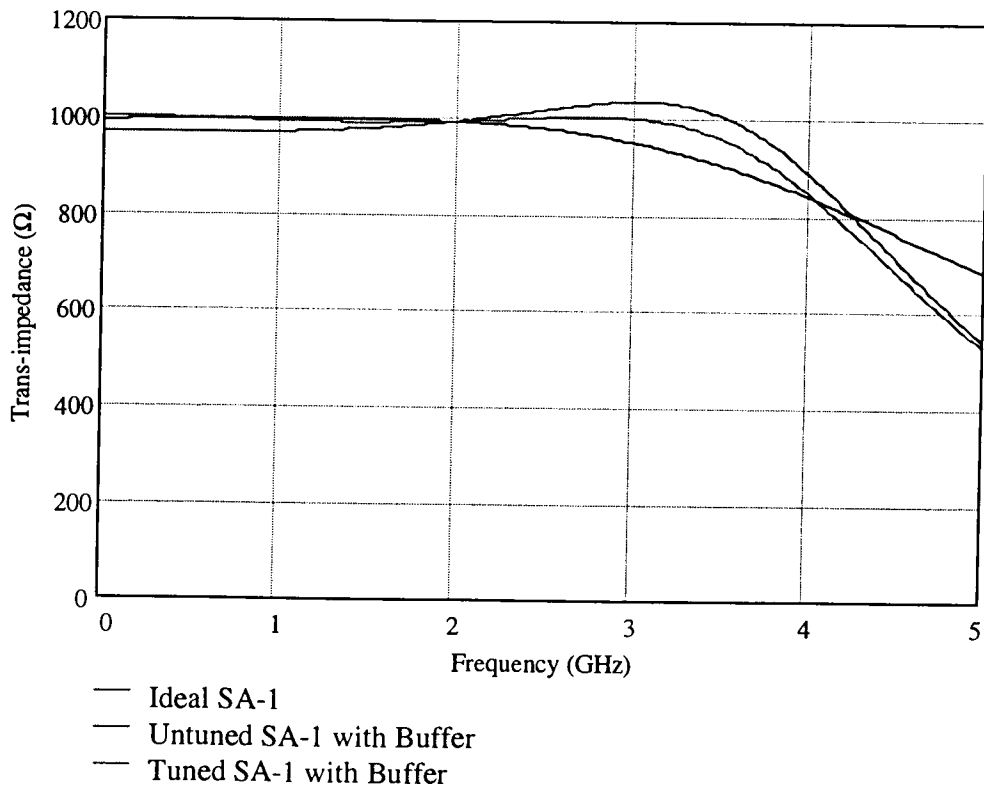


Figure 3 shows the circuit simulator results of example 2.

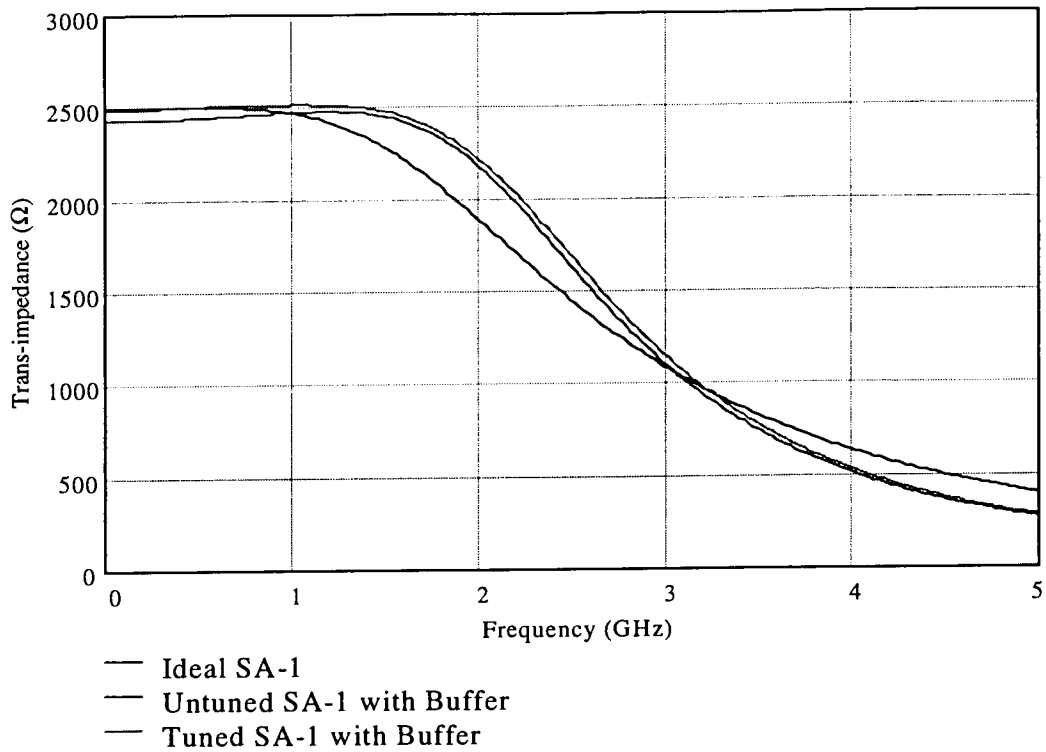


Figure 4 shows the circuit simulator results of example 3.

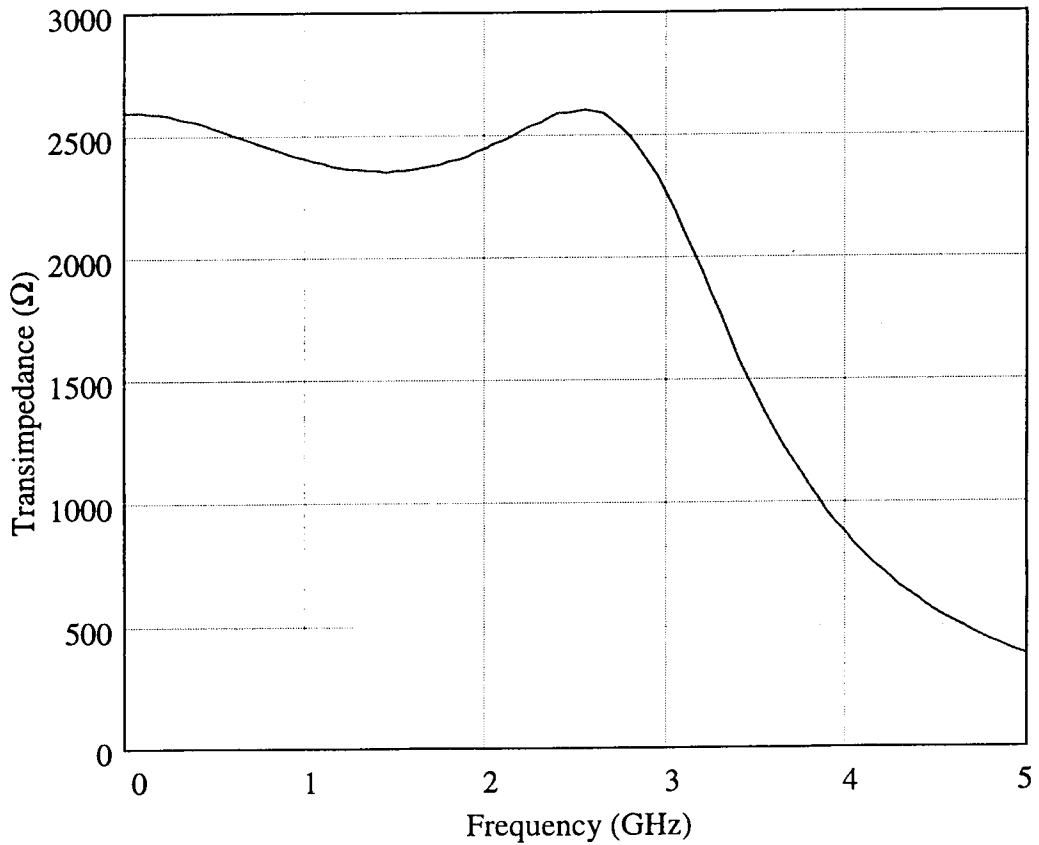


Figure 5 shows the transimpedance of the circuit in Figure 10.

## 2.2. Cascode Transimpedance Amplifier

Figure 10 shows the schematic of the cascode transimpedance amplifier. A common-gate FET (Q2) has been added to the drain of Q1 to extend the bandwidth of the circuit. The FETs Q1 and Q2 are both  $13\mu\text{m}$  and the active load Q3 is  $7\mu\text{m}$ . Each FET has been biased for a drain-to-source voltage of 2V and, except in the case of the active load, a gate-to-source voltage of  $-2\text{V}$ . FET Q9 and diodes D13-D18 provide the gate bias of the cascode FET (Q1). Diodes D4-D5 and D9-D11 have been added to adjust the bias of the source-follower stages for  $+6\text{V } V_{dd}$ .

The behavior of the circuit is similar to that of the previous design. That is, by tuning  $R_f$  I can adjust the DC transimpedance and by tuning  $C_f$  I can adjust the high-frequency transimpedance. Figure 5 shows the transimpedance of the circuit in Figure 10. The bandwidth of the circuit has been extended to 3.4GHz compared to 2.9GHz for the previous circuit. Also there is about a  $\pm 100\text{W}$  (0.7dB) ripple that is not present in the previous circuit. I have no explanation for the ripple at this time.

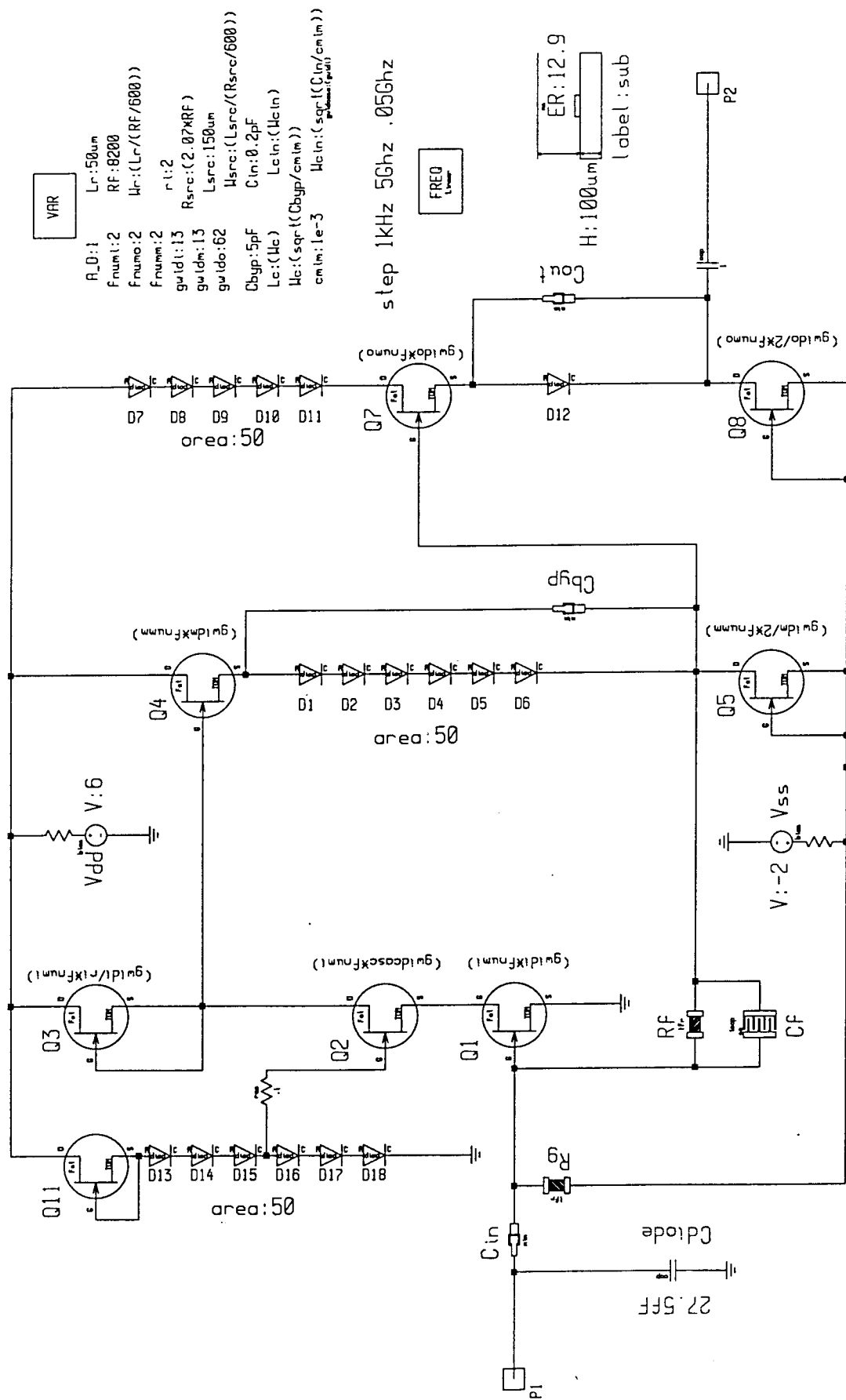


Figure 10 shows the schematic of the cascode transimpedance amplifier.

### 3. Layout

Figure 7 shows the final layout of the circuit. The SA-1 based design is in the upper right corner of the chip and the cascode based design is in the lower left corner. The SA-1 based design is marked as TIAMP and the cascode-based design is marked as TIAMP CASC. The input and output ports are marked on the chip as are the bias voltages for each amplifier.

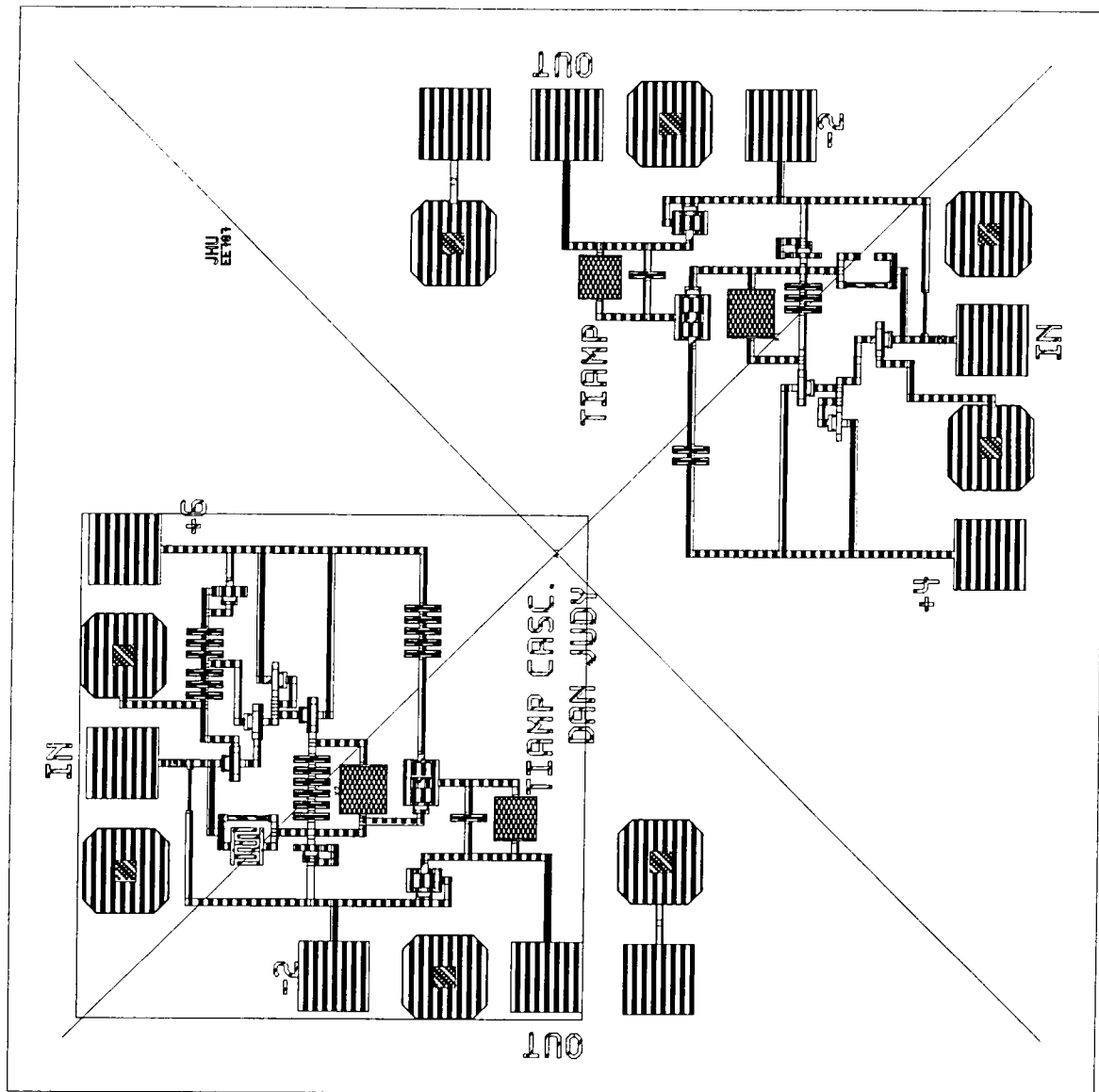


Figure 7 shows the final layout of the circuit.



## 4. Test Plan

### 4.1. SA-1 Trans-impedance Amplifier

#### 4.1.1. Bias Connections

Connect +4V and -2V bias voltages to the pads marked on the chip using needle probes.

##### 4.1.1.1. Measure Output Voltage

Place a GSG probe on with the signal electrode on the pad marked OUT. Measure the output voltage using a multi-meter. The voltage should be within a few tenths of a volt of ground potential. If this is not the case the bias circuit is faulty and a spare needle probe should be used to check the bias at several key positions to troubleshoot the circuit.

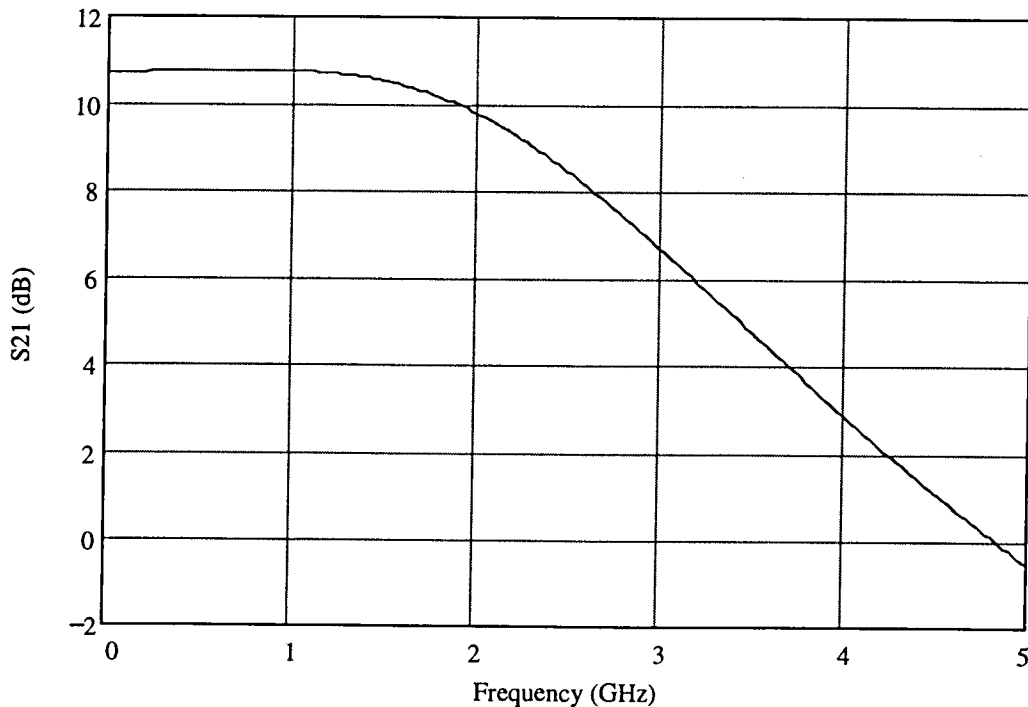
#### 4.1.2. S Parameter Measurement

##### 4.1.2.1. Calibrate

Remove the transimpedance amplifier and place a calibration substrate on the probe station. Calibrate the probes for a frequency range of 45MHz to 5045MHz using an SOLT calibration. Check the calibration by observing that there is a dot at the short and open locations on the Smith chart view when the appropriate standard is connected.

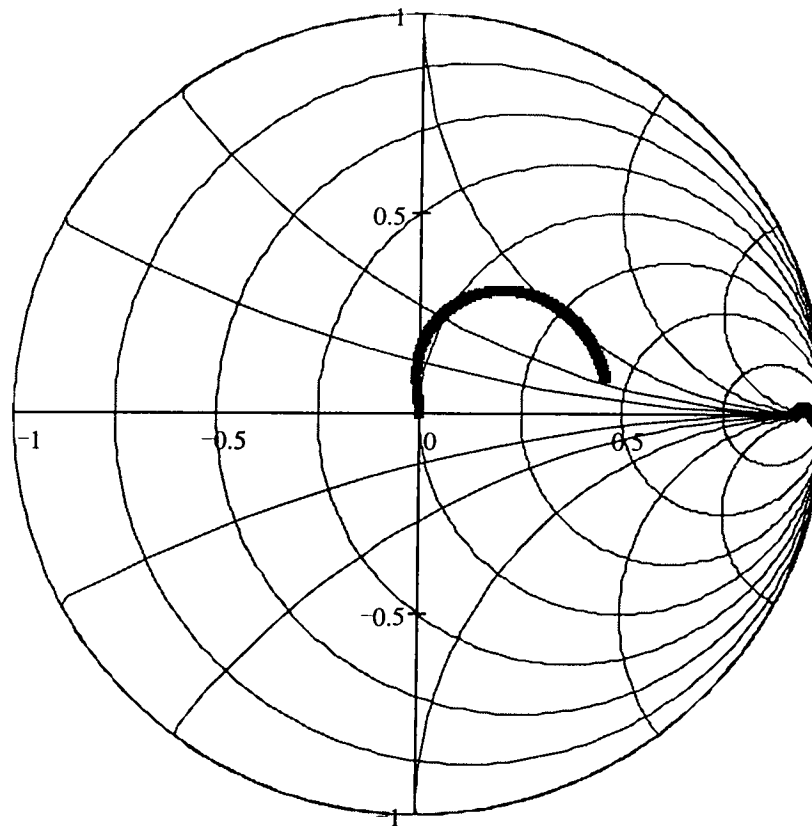
##### 4.1.2.2. Measure S Parameters

Remove the calibration substrate and place the transimpedance amp back on the probe station. Connect the +4V and -2V to appropriate pads on the chip. Connect the port 1 GSG probe to the pad marked in and the port 2 GSG probe to the pad marked out. Observe that the S21 magnitude response is similar to that displayed in Figure 8.



**Figure 8 unloaded S21 magnitude response of the transimpedance amplifier.**

Set up the network analyzer to display S11 and S22 on the Smith chart view. Observe that the response is similar to that displayed in Figure 9.



- Smith Chart
- ◇ S11
- S22

Figure 9 unload S11 and S22 response of the transimpedance amplifier.

#### 4.1.3. Download S Parameters and Calculate the Transimpedance.

If the S parameters are as expected, download the full S parameter matrix to an instrument controller or to the floppy disk. Import the data into Mathcad, Matlab, or a spreadsheet program and calculate the Y matrix using the following equation.

$$Y = Y_0(I - S)(I + S)^{-1}$$

Load the Y parameter matrix with a virtual capacitor of the same value as the diode capacitor as follows.

$$\vec{Y}_{loaded} = \vec{Y} + j \cdot 2 \cdot \pi \cdot f \cdot C_d \cdot \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}$$

Calculate the transimpedance of the loaded circuit using the following equation.

$$Z_t = \frac{-y_{loaded, 21}}{\det(\vec{Y}_{loaded}) + y_{loaded, 11} \cdot Y_l}$$

