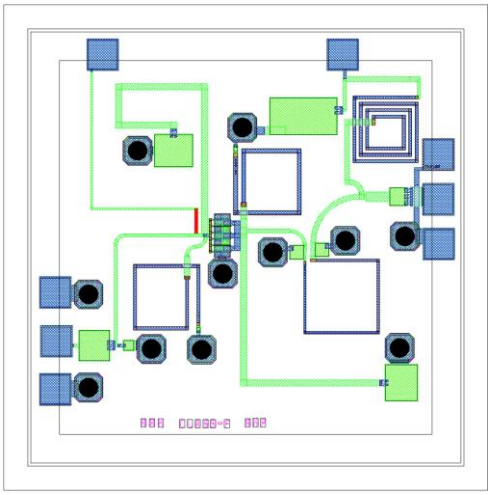
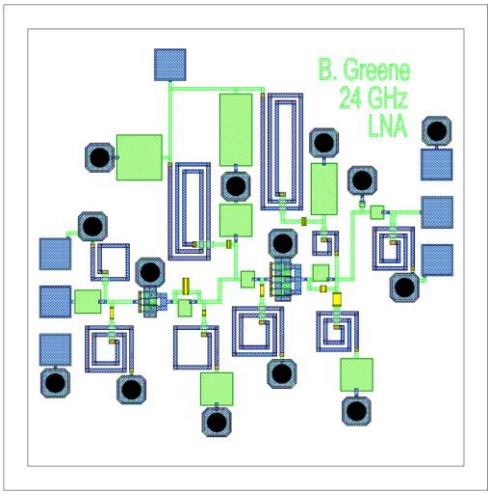
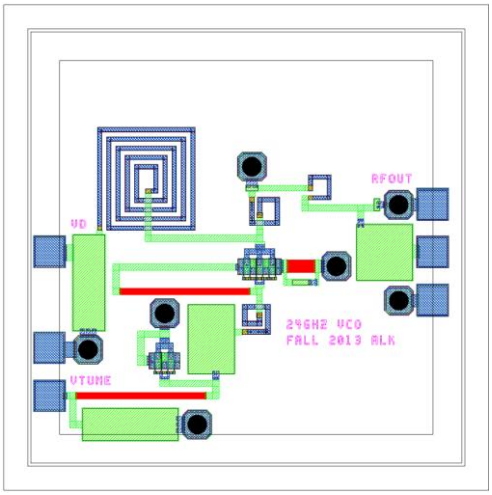
Fall 2013 JHU EE787 MMIC Design Student Projects
Supported by TriQuint, Applied Wave Research, and Agilent
Professors John Penn and Dr. Willie Thompson



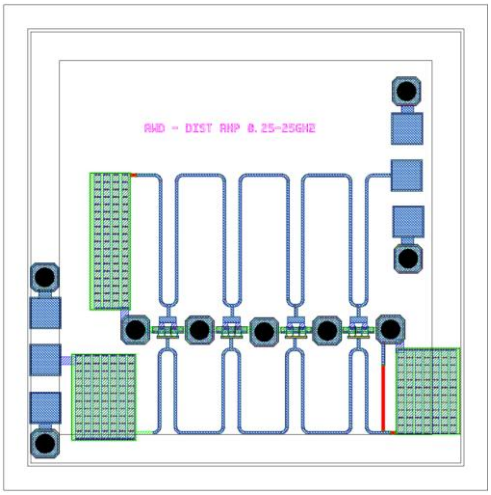
Class-F Power Amplifier—Rajesh Madhavan



Low Noise Amplifier—Brad Greene



Voltage Controlled Oscillator—Amy Kordovski



Distributed Amplifier—Alan Doucette

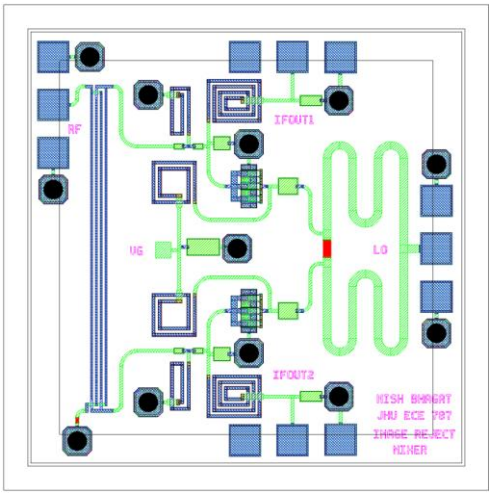
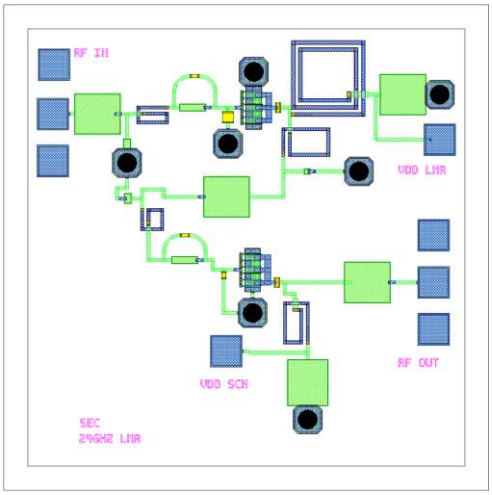


Image Reject Mixer—Nish Bhagat



Low Noise Amplifier—Shaynee Contee

MMIC Design

(Fall 2013)

Class Project

Class-F Amplifier at 10GHz

Rajesh Madhavan

Abstract: This report details the design of a Class-F Amplifier at 10GHz. The design uses one 50 X 6 device from the Triquint TQP13 Library to achieve a medium output power and high efficiency. The Amplifier is biased at 3.7V at the Drain and -0.1V at the Gate. The design is fit inside a 60Mil X 60Mils Anachip carrier.

Introduction: Class-F Amplifiers are reduced angle Amplifiers with Harmonic terminations to shape the Drain voltage and current such that the peak of Drain Current and Voltage do not coincide (i.e.) having a 180 Degree relation between the Voltage and current. This in turn makes the energy dissipated in the device to a minimum which improves the efficiency. If all the Harmonics are considered, it is possible to get a theoretical efficiency close to 100%. This also assumes that the device has an infinite Ft. Since this is not possible, we consider at least 3 harmonics. The Class F Amplifier has an open at odd order Harmonics and a short at even order harmonics. The terminations are presented at the Drain plane of the device to achieve maximum efficiency. It was found that having the harmonic terminations in the input also improves the efficiency. Since the Drain voltage in Class-F Amplifiers can reach high values, it is necessary to make sure that it does not reach the maximum ratings of the device. Normally Class-F Amplifiers are attempted with high voltage devices like GaN. Attempt has been made with TQP13 process here to find out how much efficiency we can achieve. Since this Amplifier is designed to be a medium power amplifier suitable as a driver Amplifier, It does not have to be unconditionally stable for all impedances at the input and output. However, care should be taken to make the Amplifier reasonably stable.

Specifications:

Gain	7dB to 10dB
Stability	Conditionally Stable
Output Power	+20dBm Nominal
Drain Efficiency	50%
Power added Efficiency	45%
VDD	3.5V to 4V
VGS,IDS	-0.3 to 0V,10mA to 20mA

Design Goal and Modifications:

The Original goal of the project was to design a Class-F Amplifier at 26GHz ISM Band. As stated before, the device has to have a reasonable gain and Ft up to at least 3 Harmonics, (78GHz) for a Class-F amplifier to provide high efficiency. Since the device did not provide such Gain at higher frequencies, the design goal was modified and a frequency of 10GHz was chosen.

Design and simulations:

Step 1: The first step is to find out how much output power and Efficiency can be achieved with the device by having an ideal matching in the input and output of the device. This is as shown in Fig-1.

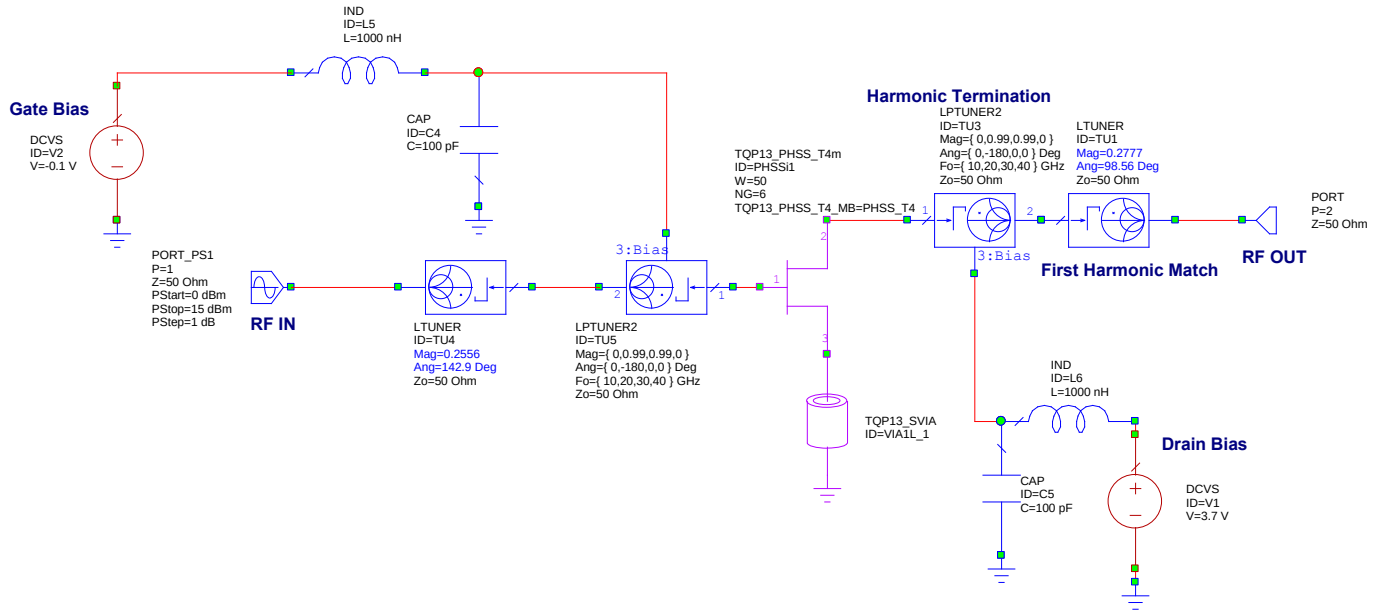


Fig-1 (Ideal Matching with TQP13 Device)

The second harmonic at 20GHz was provided a short (Mag 0.99, Phase of-180Deg) and the third harmonic at 30GHz was provided an open (Mag 0.99, Phase of 0Deg). The Amplifier was then conjugate matched at the input and output to achieve the necessary output power and efficiency. The Efficiency, Output power and the Drain efficiency was as shown in Fig-2 when the input power is swept from 0dBm to +15dBm at 10GHz.

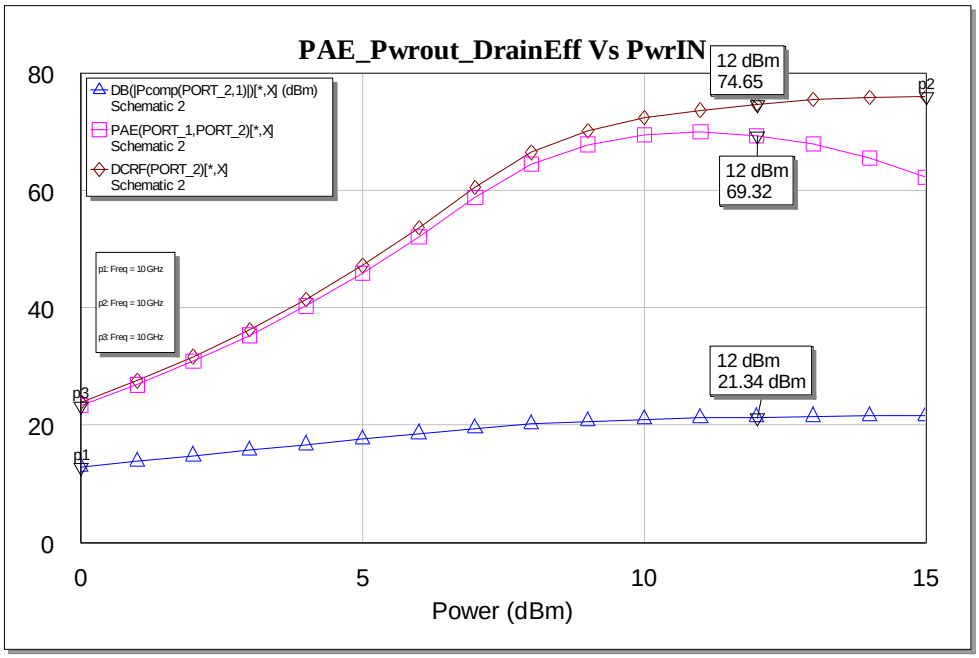


Fig-2 (Performance with Ideal Matching of a TQP13 Device)

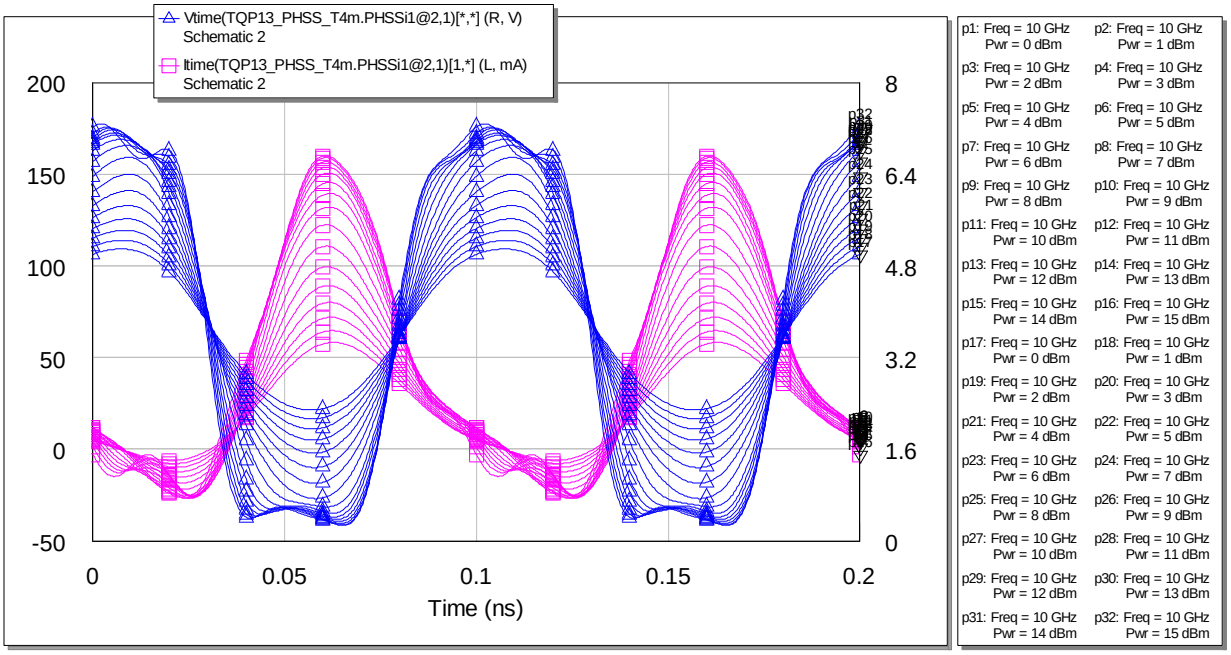


Fig-2A (Voltage and Current Waveforms at the Drain Terminal with Ideal Match)

The Power added Efficiency is around 70% for an output power is in excess of 20dBm. The Gain is 9dB when driven at +12dBm. The Drain Efficiency is close to 75%.

Step 2: The next step is to tune the harmonic terminations choosing the components from the TQP13 component library. This is shown in Fig-3.

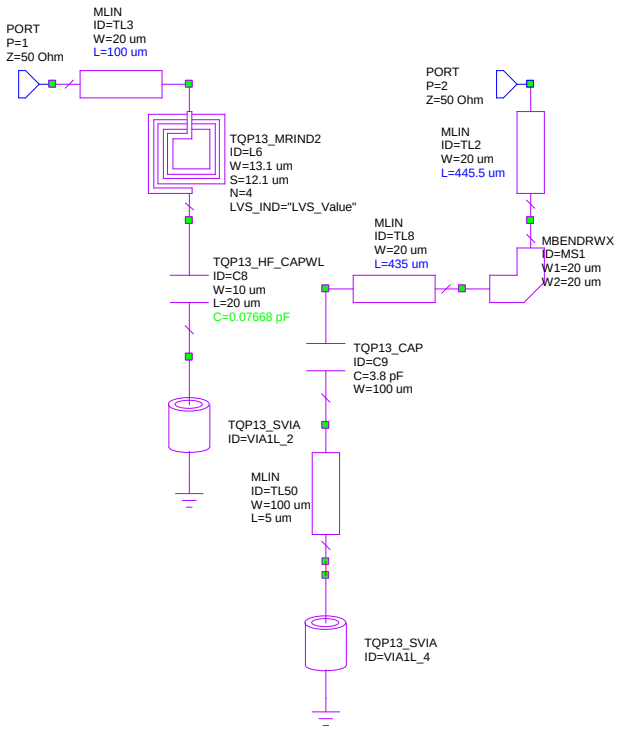


Fig-3 (Harmonic Terminations-Initial Values)

The reflection coefficients of the harmonic terminations at the first, second and third harmonics are as shown in Fig-4.

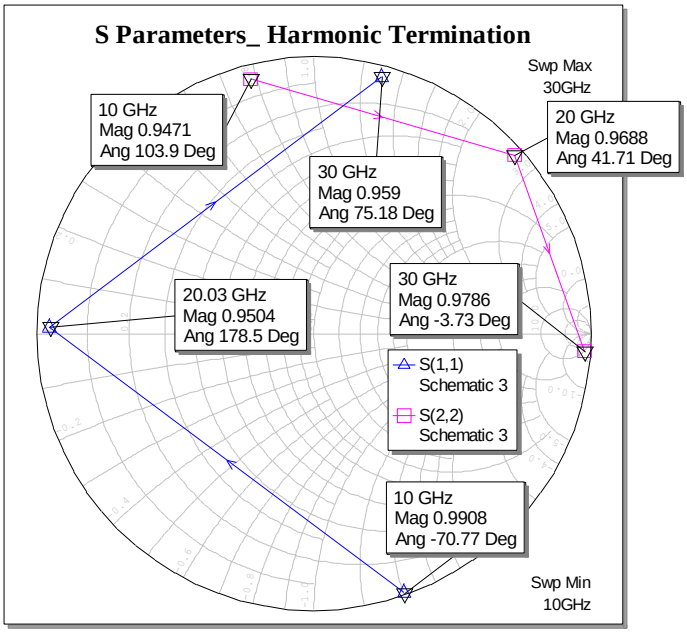


Fig-4 (Harmonic Terminations at 1st,2nd and 3rd Harmonics)

Step 3: The combined network and its response of both the resonators is as shown in Fig-5 and Fig-6 respectively.

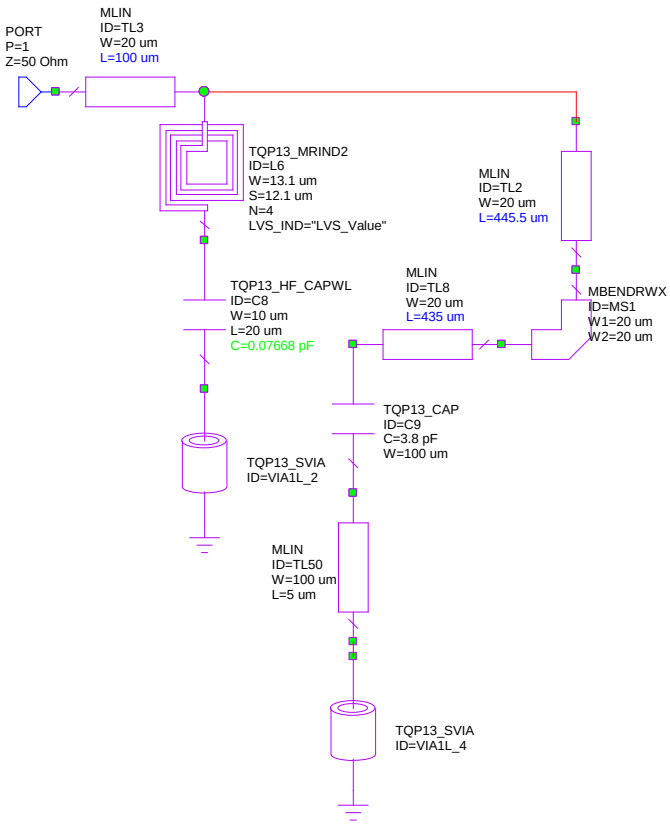


Fig-5

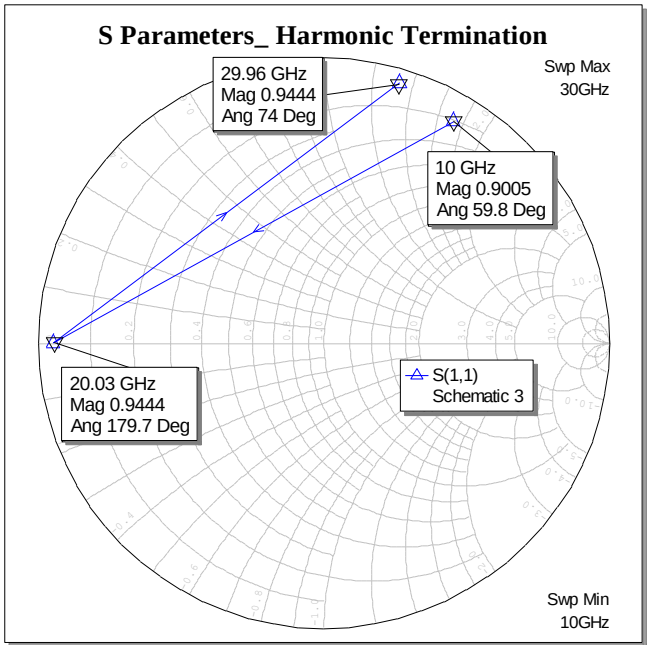


Fig-6

The reflection coefficient at 30GHz has shifted away from the phase of zero degrees. The values are considered initial values and can be optimized in the final circuit. The value at the first harmonic of 10GHz has also changed and the loaded value will be used for conjugate matching.

Step 4: The harmonic terminations are added and the input and output matched and optimized for power and efficiency. This schematic is as shown in Fig-7.

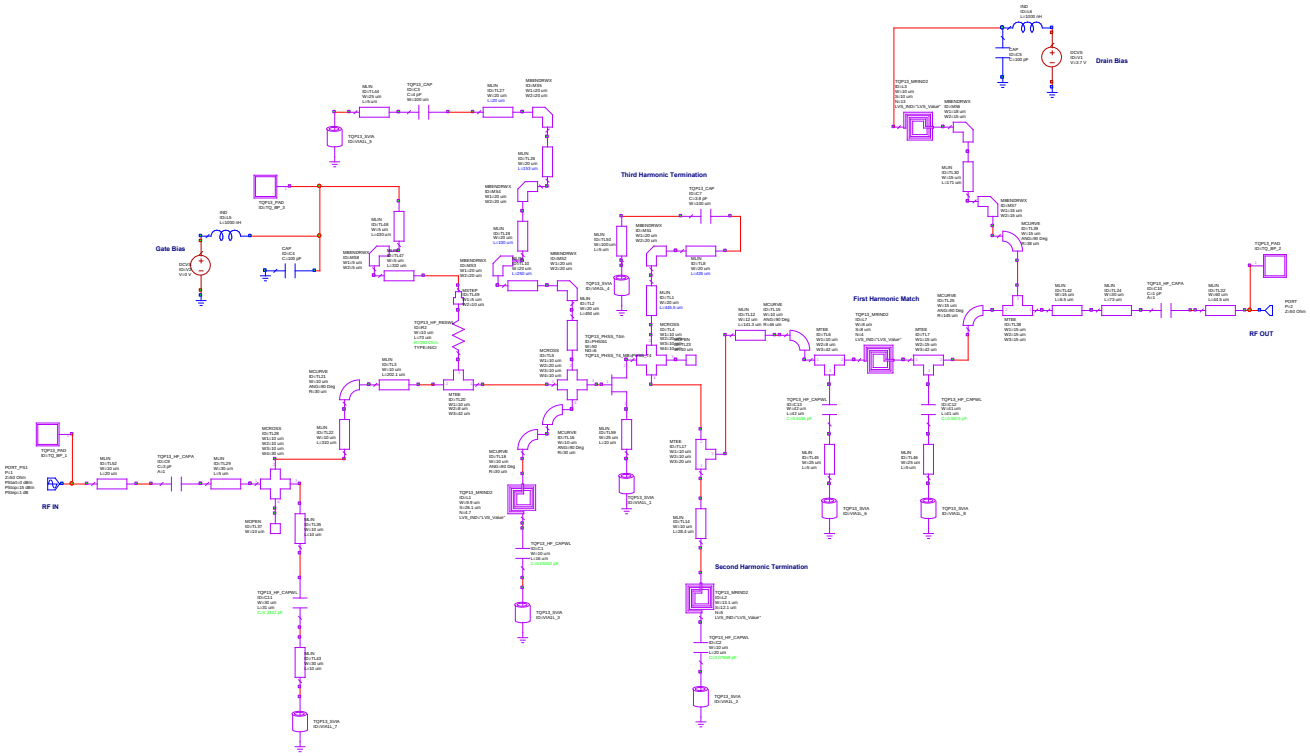


Fig-7(Schematic of the Amplifier with Matching and Bias)

Step 5:
Simulation Performance and analysis:
Linear Simulation: The S parameters of the circuit are plotted in Fig-8.

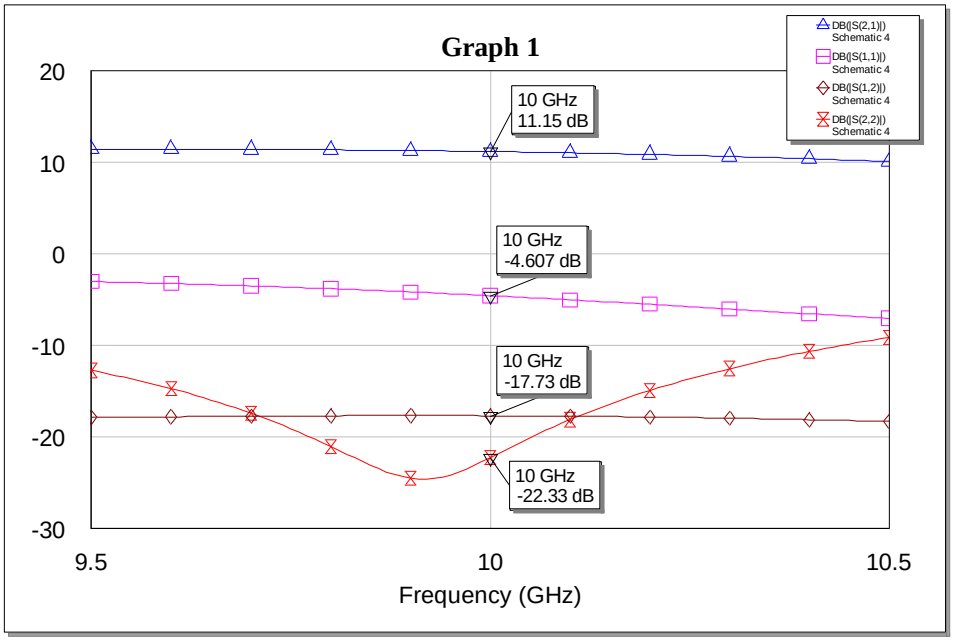


Fig-8(Linear Performance of the Amplifier)

The Linear Gain is 11dB. The input RL is poor as it is optimized for power and efficiency.
The stability of the circuit is plotted in Fig-9.

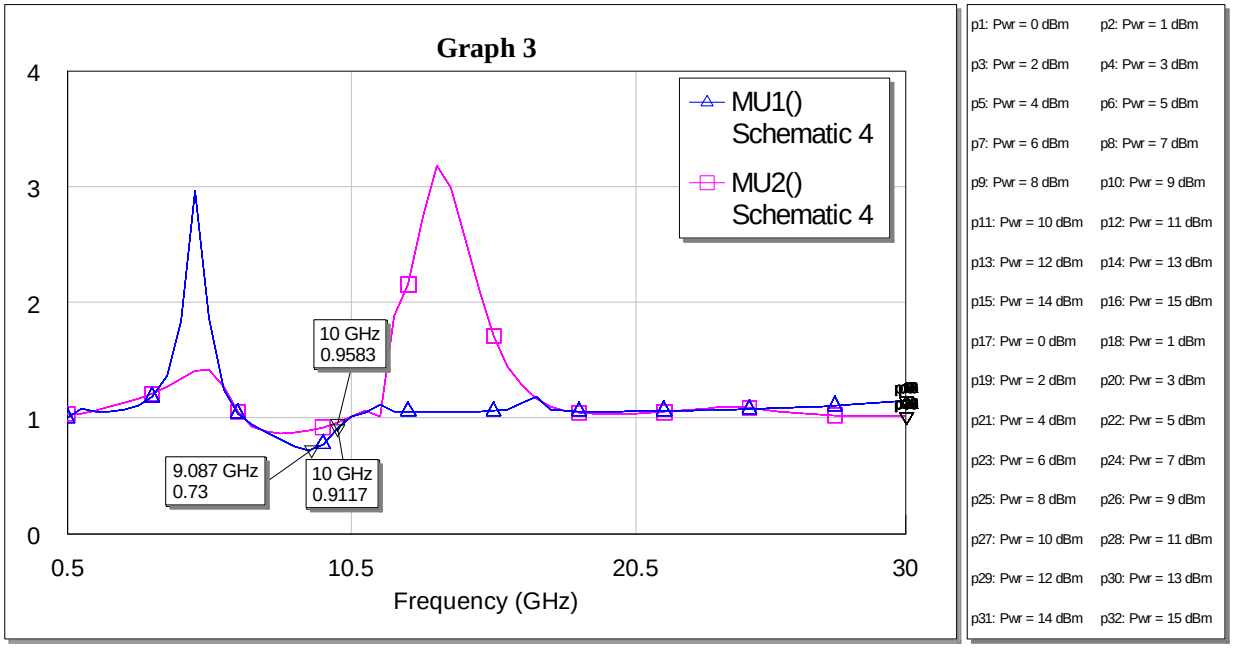


Fig-9(Linear Stability of the Amplifier)

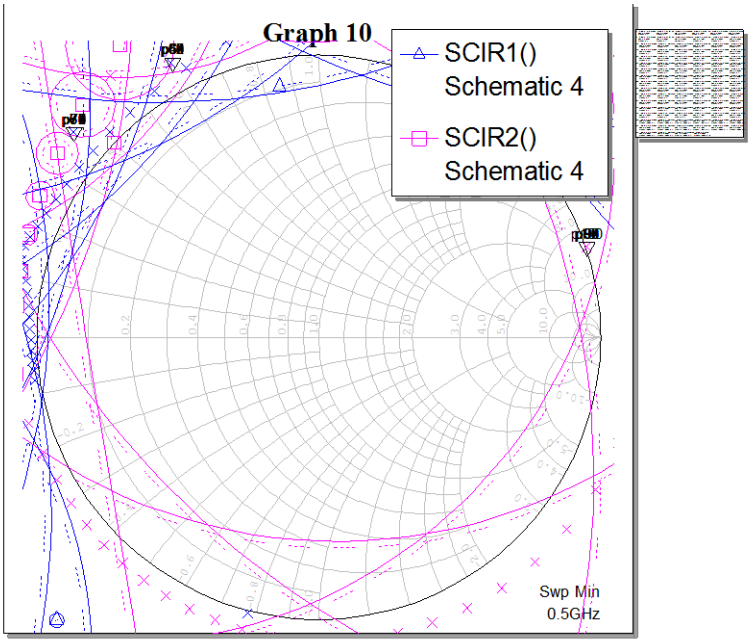


Fig-9-A(Linear Stability of the Amplifier)

The circuit is conditionally stable at certain frequencies. Since this is designed as a medium power driver amplifier, it is assumed that the amplifier is not going to be subjected to loads of poor VSWR. Also, as the plot indicates, the lowest value of MU is around 0.7. This means that the circuit should be stable for all the loads better than 3dB RL.

Non-Linear Simulation: The Non-Linear Gain, PAE, Drain Efficiency and Output power is shown in Fig-10.

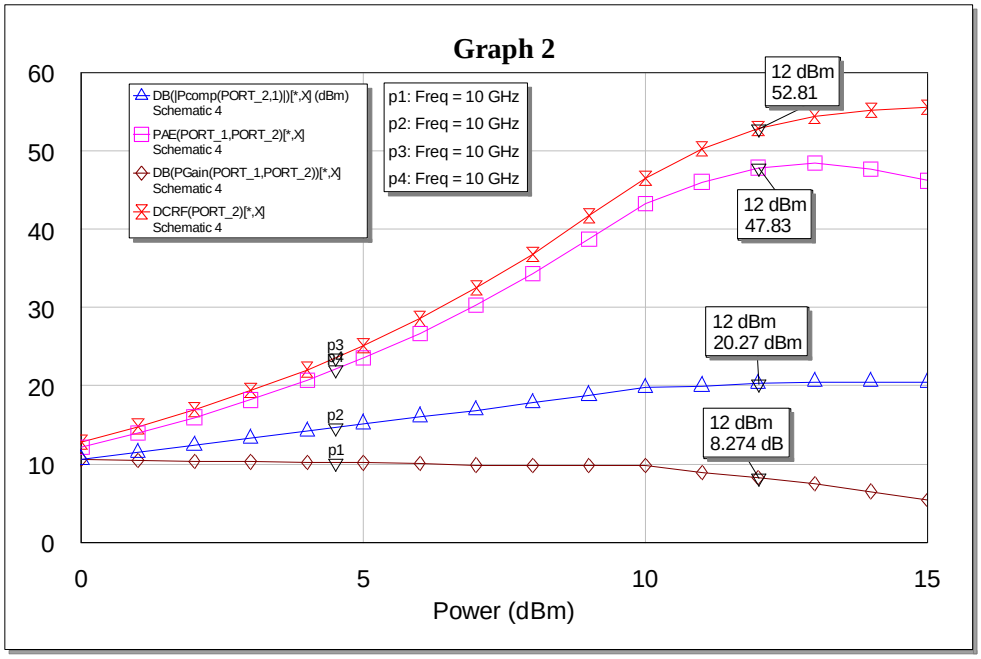


Fig-10(PAE, Output Power, Gain, Drain Efficiency of the Amplifier)

While the output power is as desired, the efficiency is not. This may be due to the fact that the physical elements of the TQP13 process have lesser Q at higher frequencies. Also as the next plot would indicate, the output peak voltage was limited to a value less than 8.5V so as to prevent the transistor from being damaged. This also limits the efficiency.

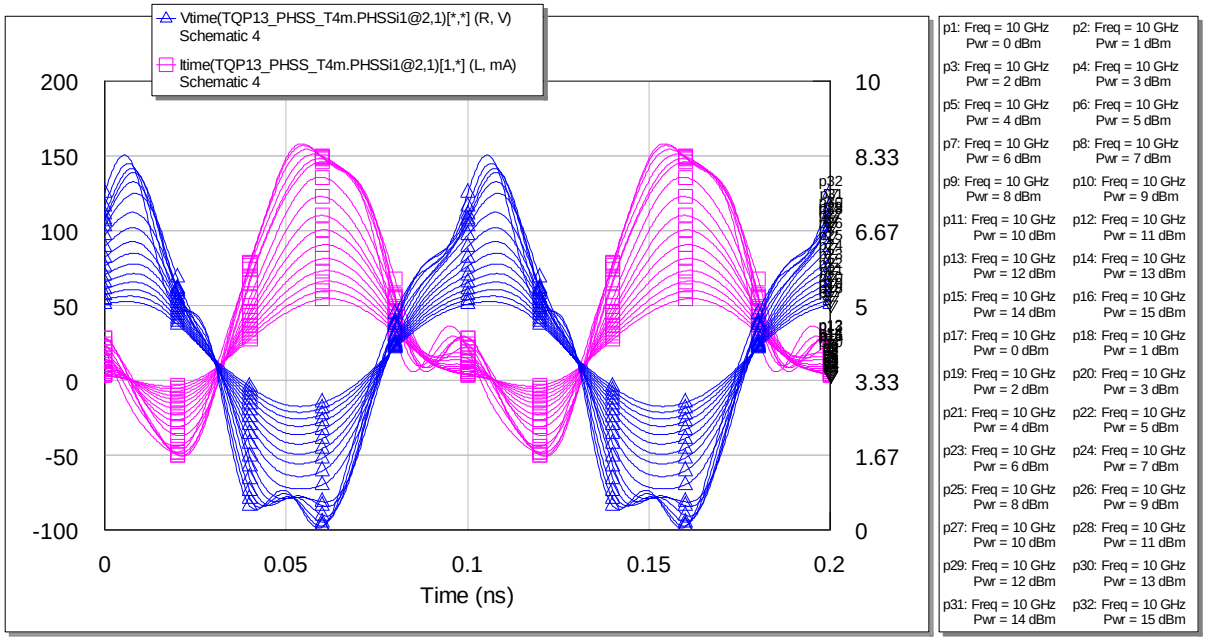


Fig-11 (Voltage and Current Waveforms at the Drain Terminal with Match Using TQP Elements)

The Voltage and current in a Class-F Amplifier are supposed to be half sine waves. The plots show that they resemble half sine waves. However with lesser losses (Higher Q) it would be a half sine.
The output power spectrum with an input power of 12dBm is as shown in Fig-12.

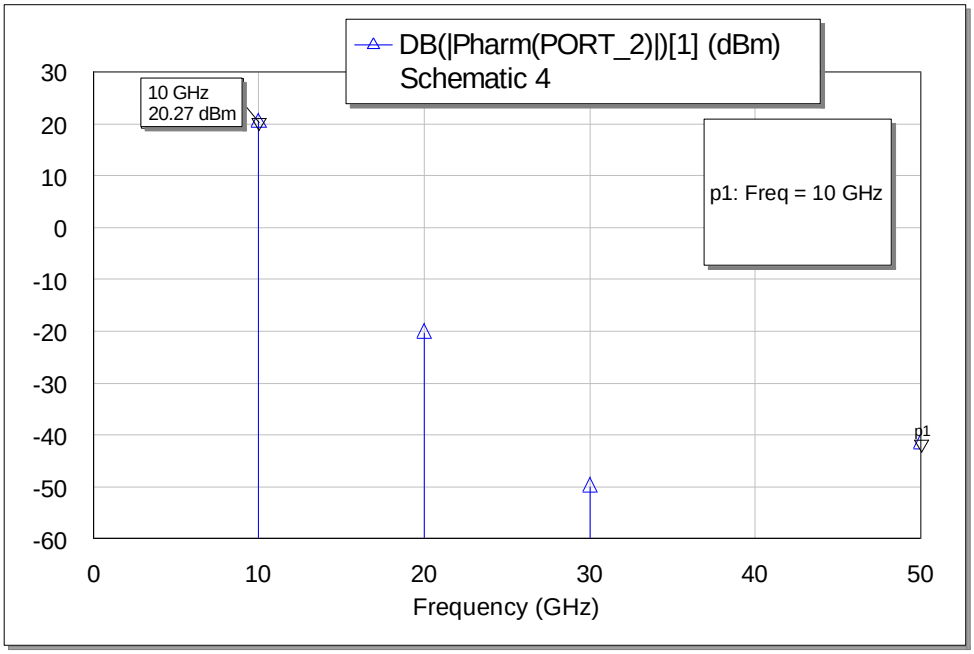


Fig-12(Output Power Spectrum)

Step 6:
DC analysis: The DC schematic with Voltage and current annotated is as shown in Fig-13.

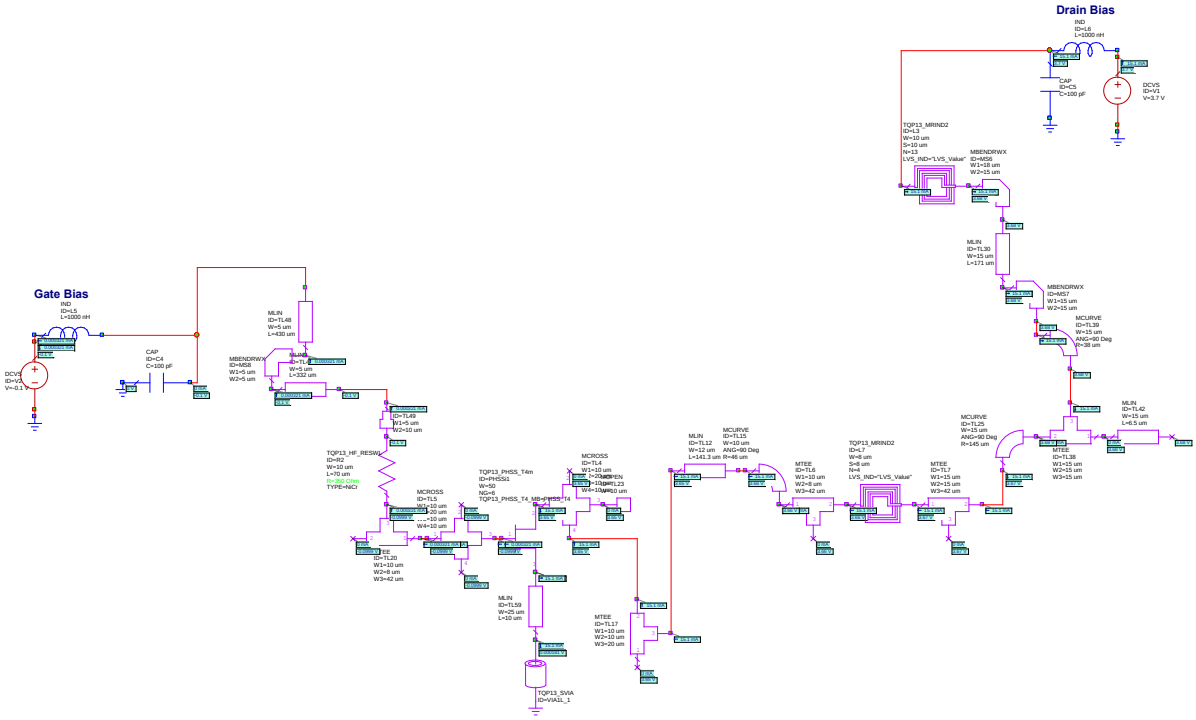


Fig-13(DC Bias Schematic)

From the Figure, the transistor is biased at 3.65V and 15mA. The DC bias for the Drain was introduced along with the output matching in the circuit. This was done so as the bias circuit to have a negligible effect on the matching. However, the width of the matching elements had to be increased which was non-optimal for the RF performance of the circuit.

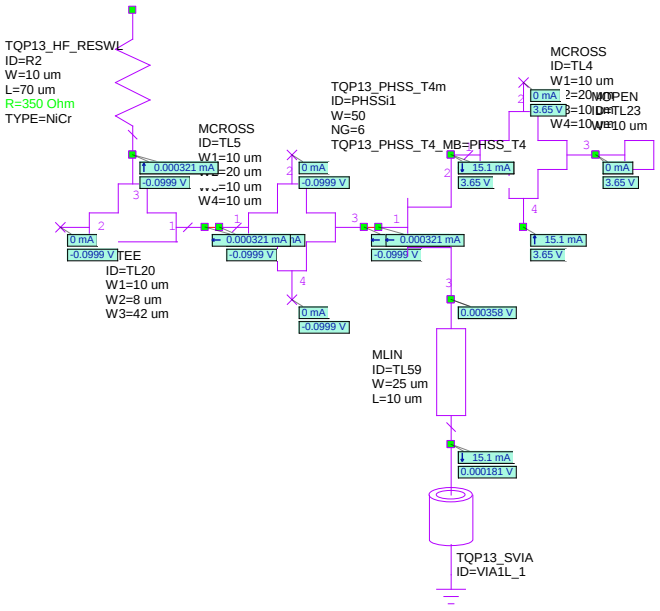


Fig-13-A(DC Bias Schematic)

Step 7:

Load Pull Analysis:

Load pull analysis was performed for best PAE and output power. The two graphs are as shown in Fig-14, Fig-15 respectively.

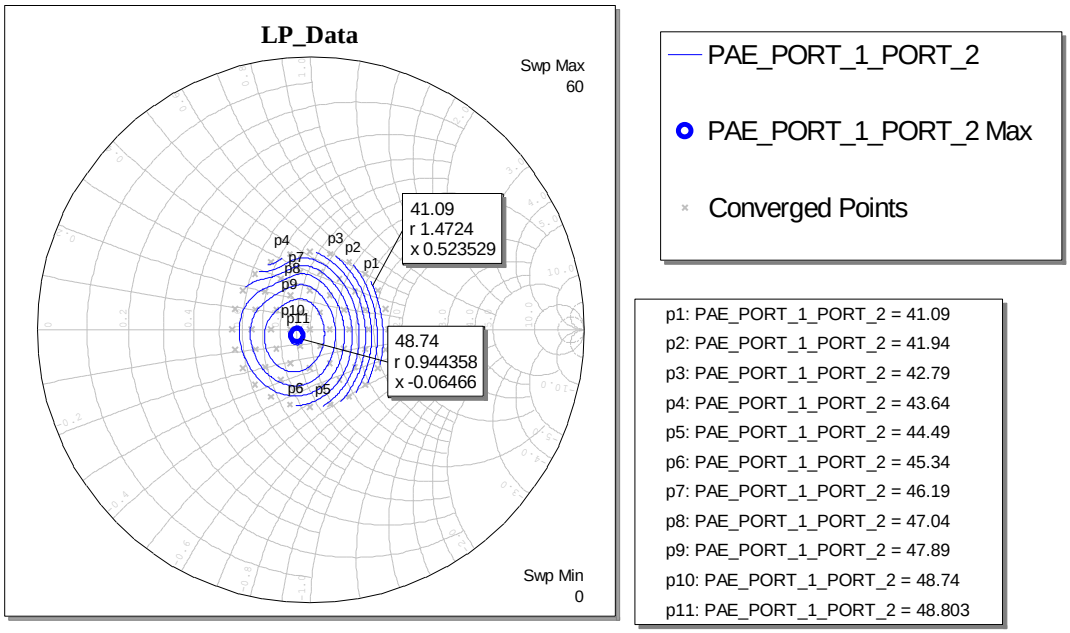


Fig-14(Load Pull Analysis-PAE)

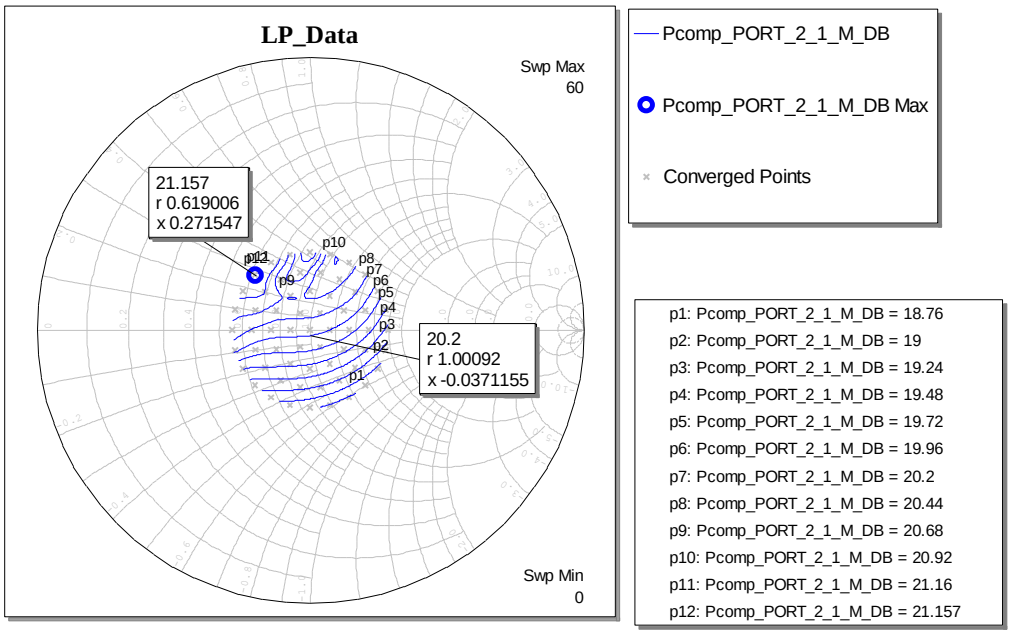


Fig-15(Load Pull Analysis-Output Power)

The Maximum PAE occurs at the center of the smith chart (Mag 0, Phase 0). However, the peak output power does not. The output power at the center is still greater than 20dBm.

Layout:

The layout of the circuit in TQP13 process is as shown in Fig-16.

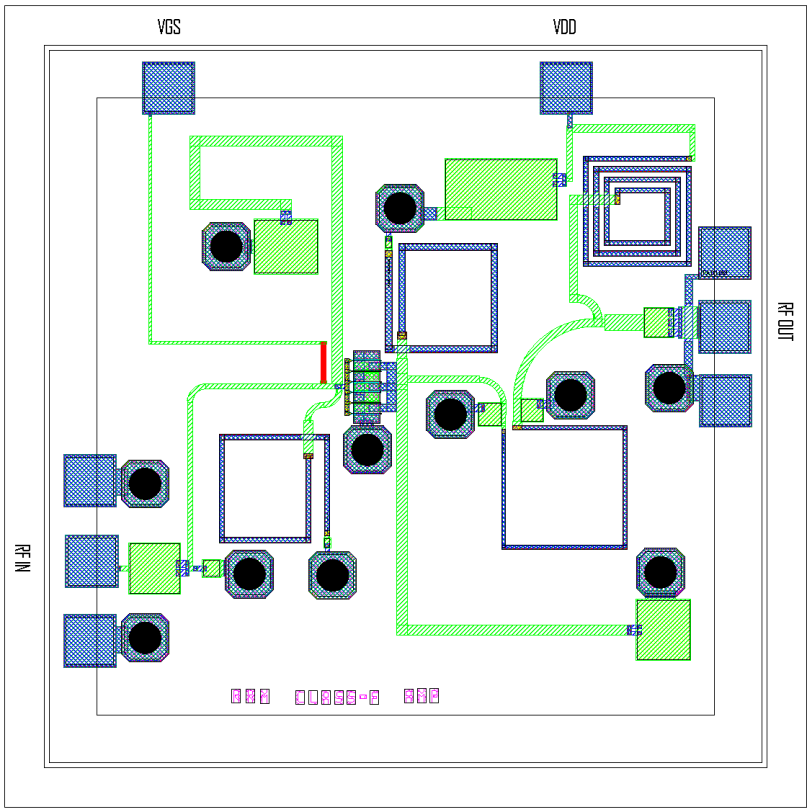


Fig-16(Layout)

Test Plan:

List of equipment needed:

1. 2 DC power supplies
2. Spectrum Analyzer
3. 2 DC probes
4. 2 RF Probes
5. Signal generator capable of providing at least 12dBm at 10GHz.

Testing:

1. Connect and energize the VGS supply and make it -2V.
2. Then energize VDS supply and bring it to 3.7V.
3. Increase VGS supply to -0.1V. Observe ID such that it is near 15mA.
4. Slowly sweep 10GHz input from 0dBm to 12dBm. Measure output power.

Conclusions:

A Class-F Amplifier design has been attempted in TQP13 at 10GHz. As stated before, the operational frequency was chosen to fit the design in the 60 Mils X 60Mils package. The Efficiency is not as good as some designs that use GaN or LDMOS. But, this design uses far smaller Drain voltages when compared to those semiconductors. However, the efficiency could be better if,

1. We had chosen a transmission line matching for the harmonic terminations instead of using an Inductor. This will require a larger carrier size.
2. Inductors have a higher Q at higher frequencies.

24 GHz Two-Stage LNA

Bradley Greene
Johns Hopkins University
December 8, 2013

Abstract

The Triquint TQP13 MMIC processed was utilized to create a 2-stage low noise amplifier for operation in the 24 GHz ISM band. The primary design goal was to achieve optimum noise figure and high gain at 24 GHz. While the design was optimized for a center frequency of 24 GHz the bandwidth of the design was maximized to provide a goal operating frequency range of one octave.

Introduction

A low noise amplifier (LNA) is a critical building block in wireless receiver systems. Having a low noise figure is critical to providing maximum dynamic range. A lower noise figure will improve the system's ability to intercept extremely low power signals. This is critical to system specifications like range and bit error rate. Optimum noise figure is achieved in a system by placing an amplifier with low noise figure and adequate gain at the antenna.

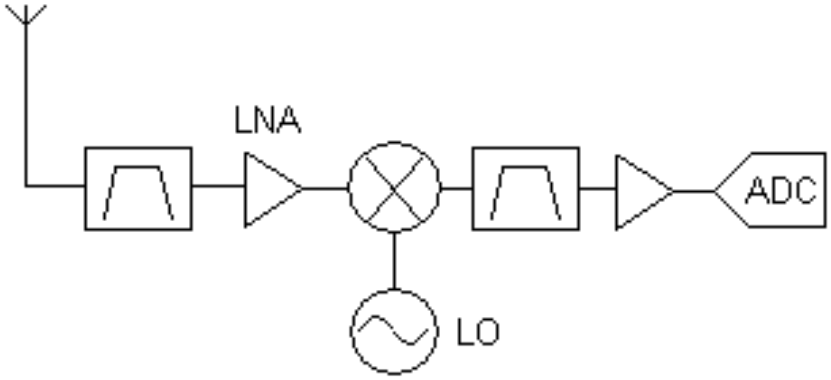


Figure 1: Example Receiver Block Diagram.

$$F_{Cascade} = F_1 + (F_2 - 1)/G_1$$

Equation 1: Cascaded Noise Figure of a System.

Low noise amplifiers are designed by matching the input of a transistor to the optimum noise parameters of the device. Next the output of the device is matched for best return loss. By matching the output for best return loss, the gain of the device is maximized.

Design

Because of the relatively low associated gain of the device at 24 GHz, two FET stages were used to improve the gain of the amplifier. A smaller device, 4x40 µm, was used for the first stage to reduce the device parasitics. This helped improve the device gain and bandwidth. A 6x50 µm device was used for the second stage with a goal of improving the intercept point of the amplifier.

The following list outlines the basic design approach:

1. Add stabilizing networks to the 1st and 2nd FET. Care was taken not to degrade the noise performance of the device and to maximize the gain.
2. Match the first FET input for optimum noise figure.
3. Create an inter-stage match between the 1st and 2nd FET.
4. Match the output of the combined 1st and 2nd stages.

Parameter	Specification	Conditions
Gain	15 dB	24 GHz
Output Return Loss	15 dB	18 – 30 GHz
Noise Figure	1.2 dB	24 GHz

Table 1: Design Performance Goals

An iterative design process was taken and several trades-offs were considered. The final design is a result of all these considerations. In general, noise figure was prioritized first, followed by gain second and return loss third.

Source inductance can be used to improve the input return loss of a FET used with an optimum noise match. This strategy could not be employed because it reduced the gain of the device to a point that it became unusable. For this reason the input return loss of the device is not very good but this was required to maintain good gain and good noise figure.

Another trade-off involved the inter-stage matching network. Maximum gain would have been achieved by providing a conjugate match between the stages. However, this could not be utilized because it degraded the overall noise figure significantly. Instead the inter-stage match was designed to provide an optimum noise match to the 2nd stage. This sacrificed a few dB of gain in exchange for reducing the noise figure by about 1 dB.

Simulations

The following simulations were conducted using Microwave Office and the Triquint TQP13 library.

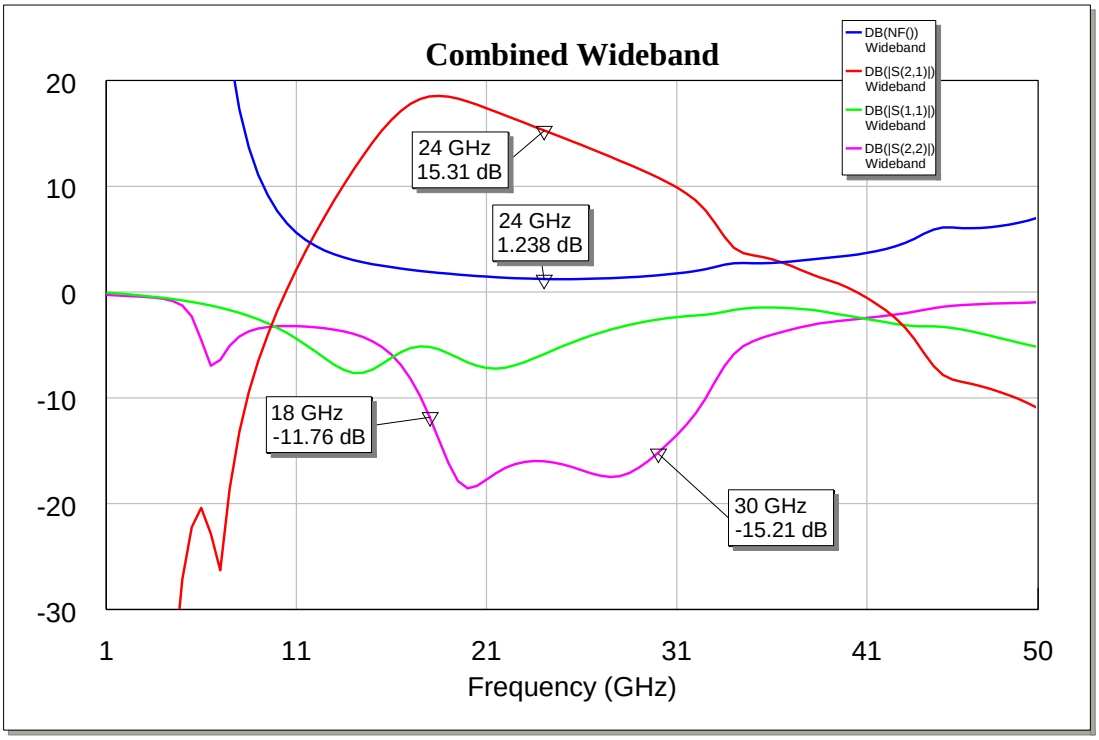


Figure 2: Gain, Return Loss, and Noise Figure Simulation Results 1-50 GHz

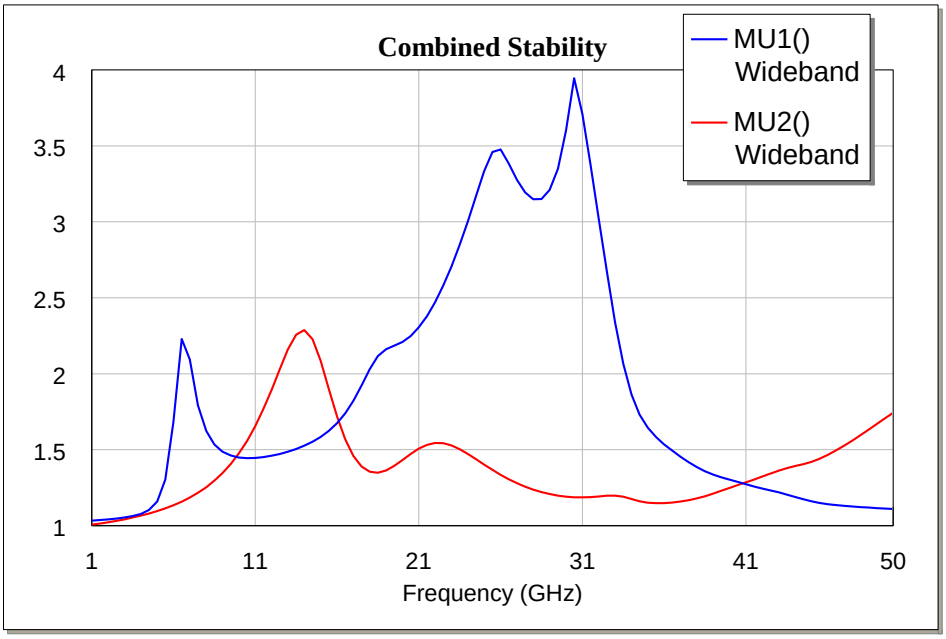


Figure 3: Stability Simulation Results 1-50 GHz

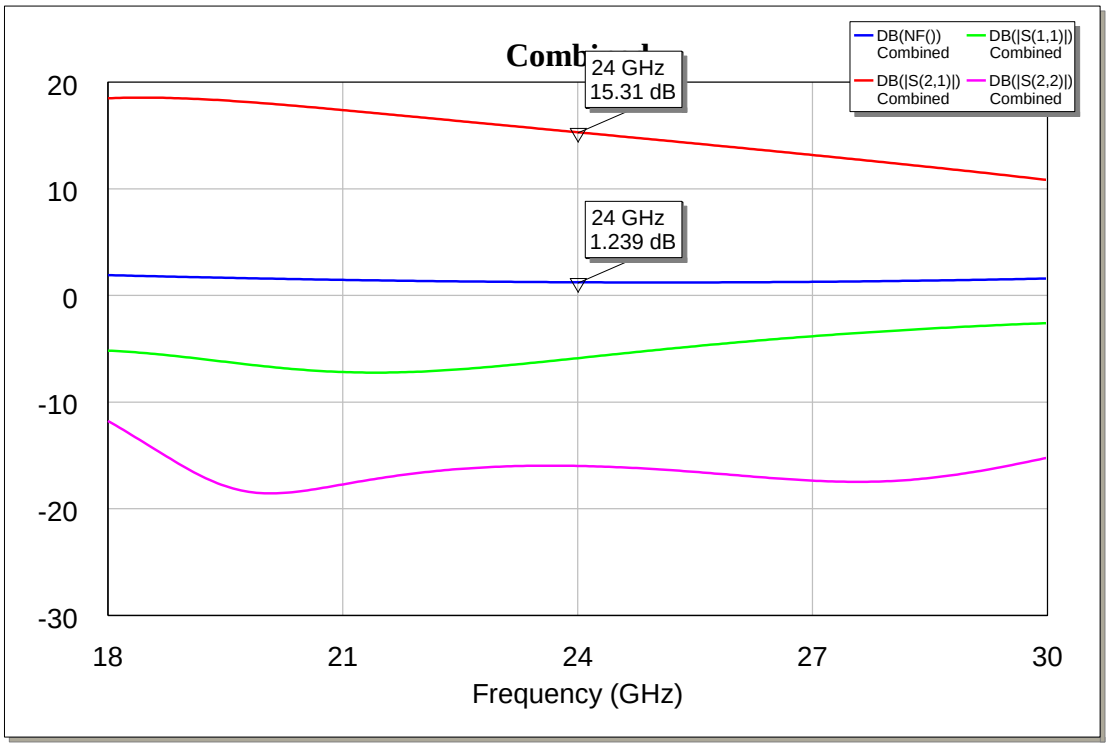


Figure 4: Gain, Return Loss, and Noise Figure Simulation Results 18-30 GHz

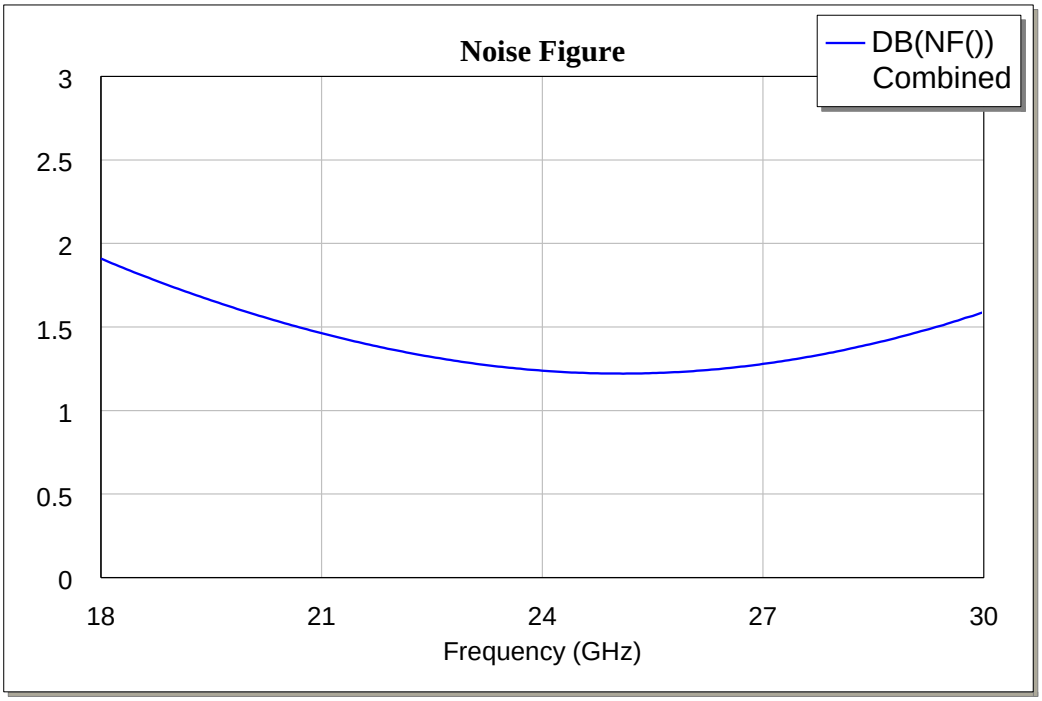


Figure 5: Noise Figure Simulation Results 18-30 GHz

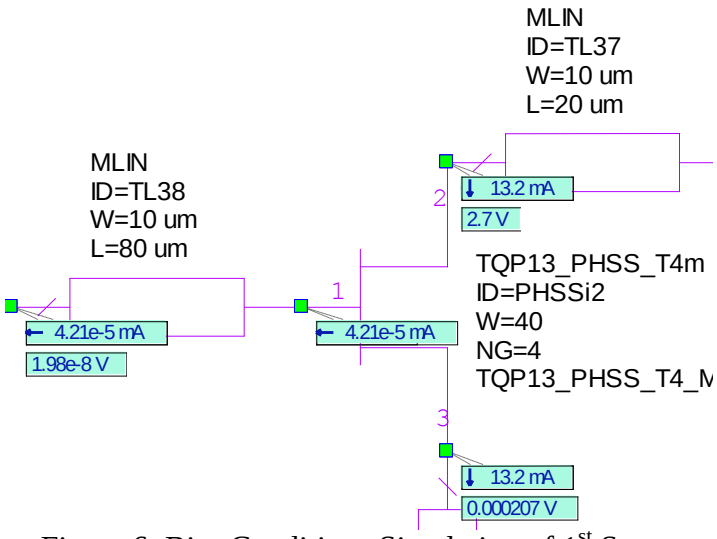


Figure 6: Bias Conditions Simulation of 1st Stage

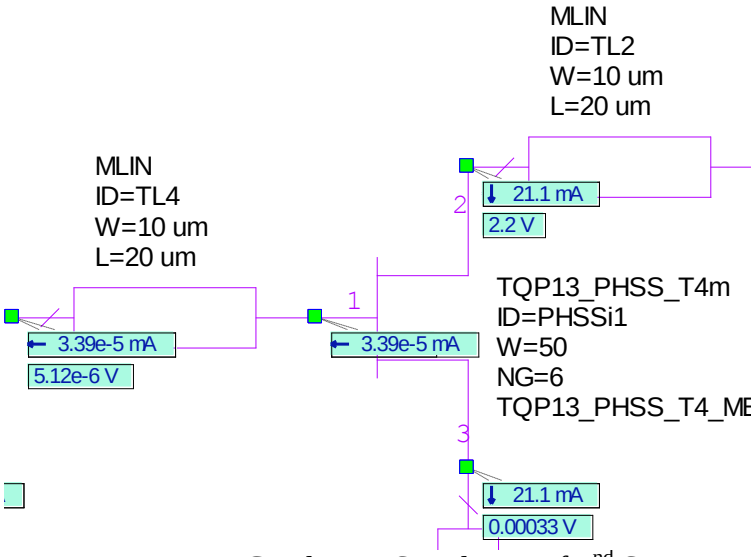


Figure 7: Bias Conditions Simulation of 2nd Stage

The circuit simulations show the LNA has a gain of about 15dB at 24 GHz and a noise figure of about 1.2 dB. Pretty good broadband performance was achieved with an output return loss better than about 12 dB from 18 to beyond 30 GHz. The noise over the 18-30 GHz spectrum is also decent at better than 2 dB. The simulations indicated that 34mA of current should be expected with a 3V bias voltage. The device is unconditionally stable with a μ1 and μ2 greater than 1 from 1 to 50 GHz. Although not shown, the individual devices were simulated for stability and were unconditionally stable as well.

Schematic

Several schematics representing the LNA are shown below. With the exception of the DC equivalent circuit, part values have been excluded as in practice they are not ideal components and therefore representative values do not make sense. The overall circuit schematic is shown first to provide a high-level picture of the circuit.

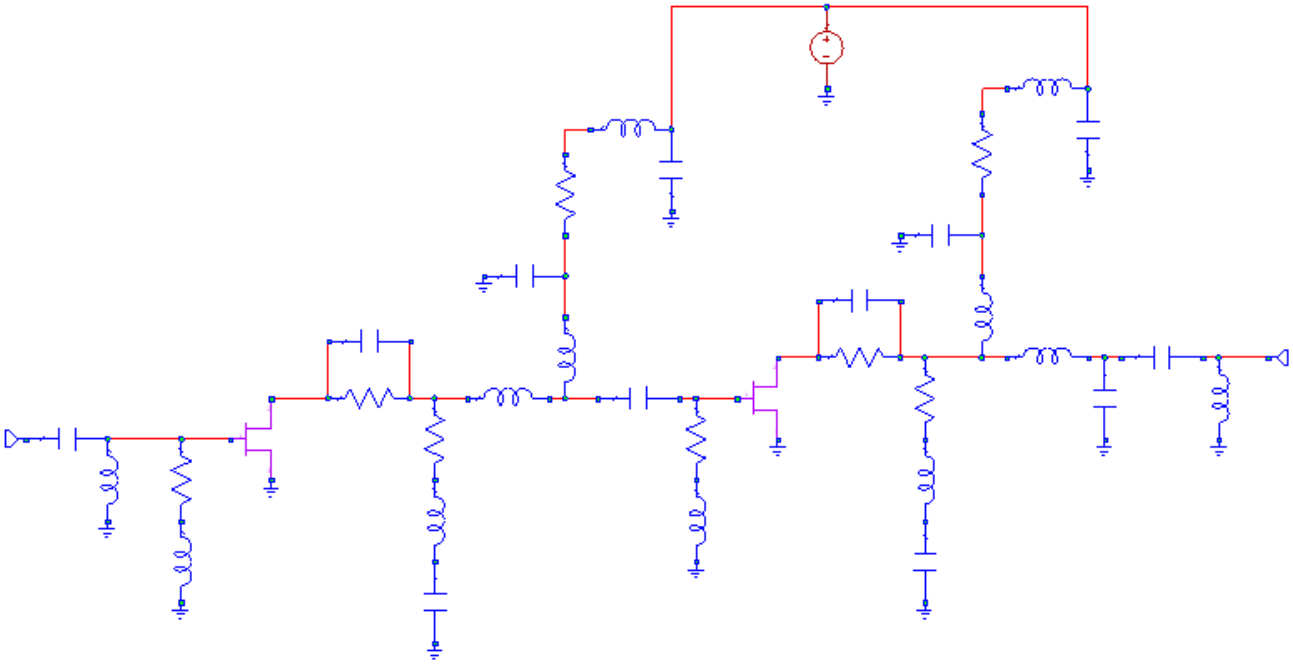


Figure 8: Equivalent Circuit of Entire IC

The stabilization network of the FET is shown below. The same circuit topology was used for both stages. The shunt inductor on the input stage was chosen so that it was high enough not to impact the NF of the device at the design frequency. Note that the input stability network provides $V_{GS} = 0$ for bias.

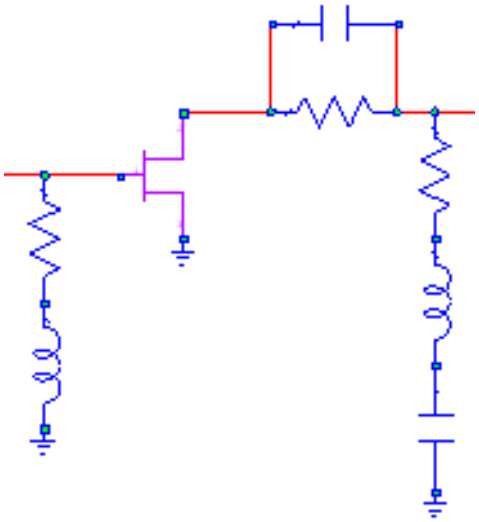


Figure 9: Equivalent Circuit of Stability Network Only

To simply the RF equivalent schematic, the stability networks were removed and included as part of the FET. Also the DC bias circuitry was excluded. The circuit below is meant to represent the matching circuitry only.

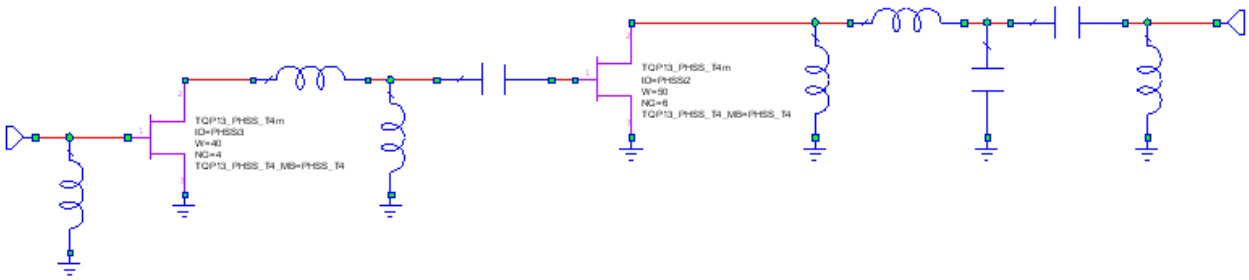


Figure 10: Equivalent Circuit of RF Matching Only

Finally, the schematic below shows the equivalent DC circuit schematic. All elements not relevant from a DC analysis perspective have been replaced with their DC equivalent.

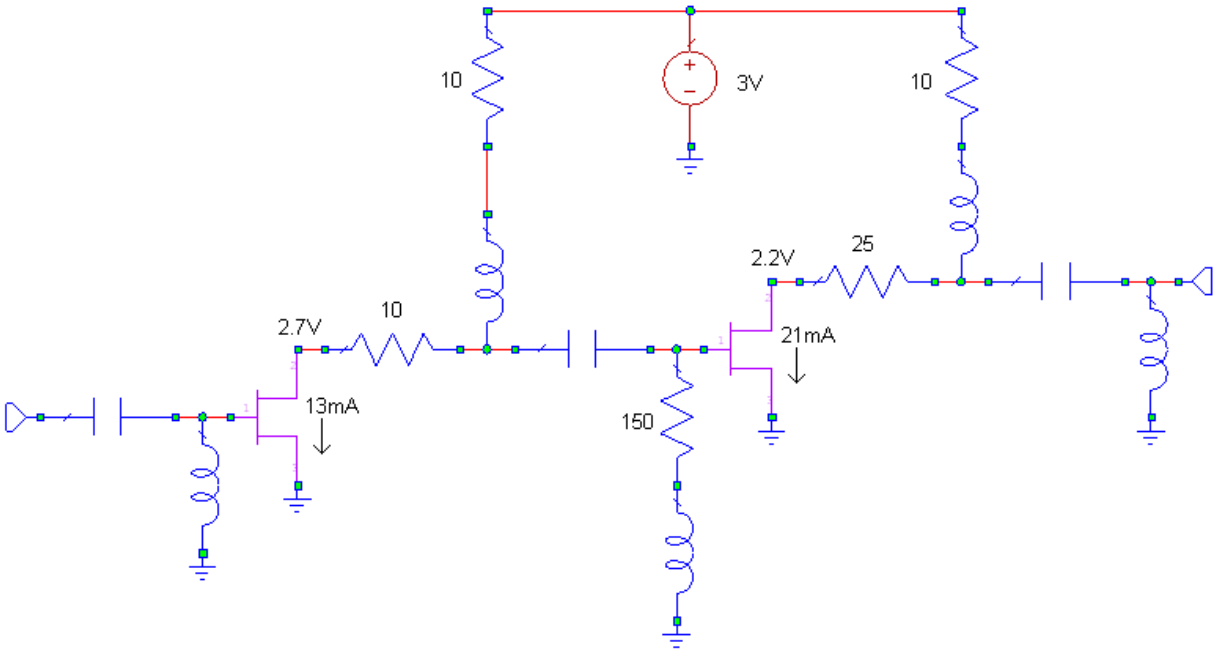


Figure 11: Equivalent Circuit of DC Bias Only

Layout

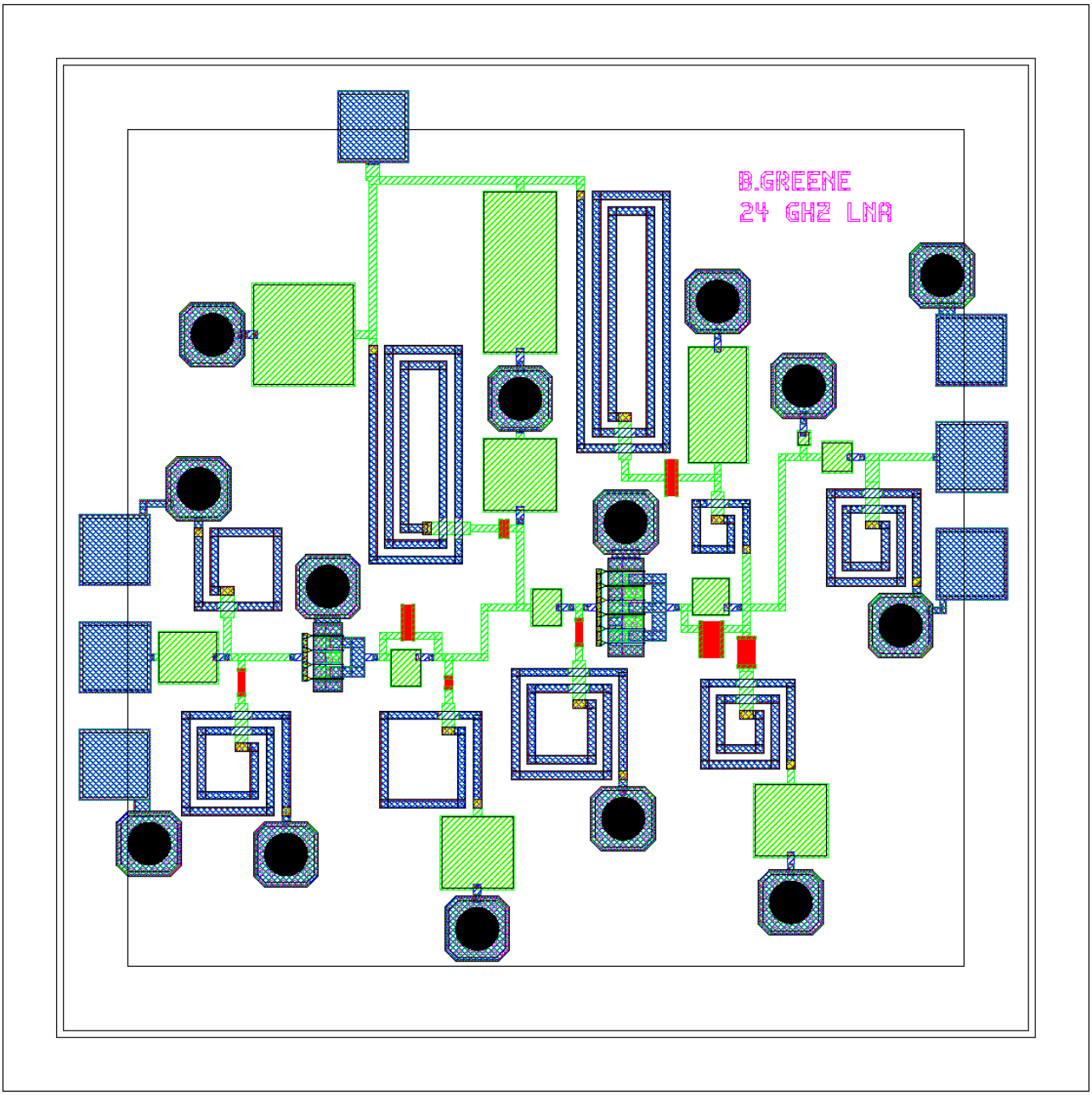


Figure 12: Plot of MMIC Layout

Test Plan

A step-by-step test plan is outlined below.

1. Apply DC voltage
    a. Slowly ramp voltage from 0-3V monitoring current.
    b. Adjust the voltage from 0.5V to 4.0V in 0.5 steps recording the associated DC current.
    c. Verify the nominal bias conditions of 3.0V @ 34mA.
2. Measure the s-parameters of the device at the 3V bias point.
    a. Verify there is approximately 15 dB of gain at 24 GHz.
    b. Verify good output return loss (>10 dB) from 18 to 30 GHz.
    c. Save s-parameter files to disk.
3. Measure the Noise Figure of the amplifier from 18 to 30 GHz using the noise figure test set.
4. Measure the P1dB of the circuit from 18 to 30 GHz in 3 GHz steps.
    a. Connect a signal generator to the input and spectrum analyzer to the output
    b. Step the input in 1dB steps from -20 dBm and record output power until the 1dB compression point is reached.
5. Measure the OIP3 of the circuit from 18 to 30 GHz in 3 GHz steps.
    a. Connect 2 signal generators to the split ports of a power combiner.
    b. Connect output of power combiner to the input of the LNA.
    c. Connect LNA output to a spectrum analyzer.
    d. Set input tones with 1 MHz spacing and adjust levels so that both output tones are located at 0 dBm.
    e. Record the dBc level of the 3^{rd} order inter-modulation tones.

Summary and Conclusions

The circuit met the performance goals established at the beginning of the design. With gain of better than 15 dB and a noise figure near 1 dB this amplifier would be an effective building block for use in the 24 GHz ISM band. With only about 100 mW of power consumption it is also a fairly power efficient device.

Parameter	Specification	Conditions
Gain	15 dB > 12 dB > 10 dB	24 GHz 18 – 28 GHz 18 – 30 GHz
Output Return Loss	< 12 dB < 10 dB	18.8 – 30 GHz 17.6 – 32.6 GHz
Noise Figure	1.2 dB < 2 dB	24 GHz 17.6 – 32 GHz
Bias Current	34 mA	V_{Supply} = 3V

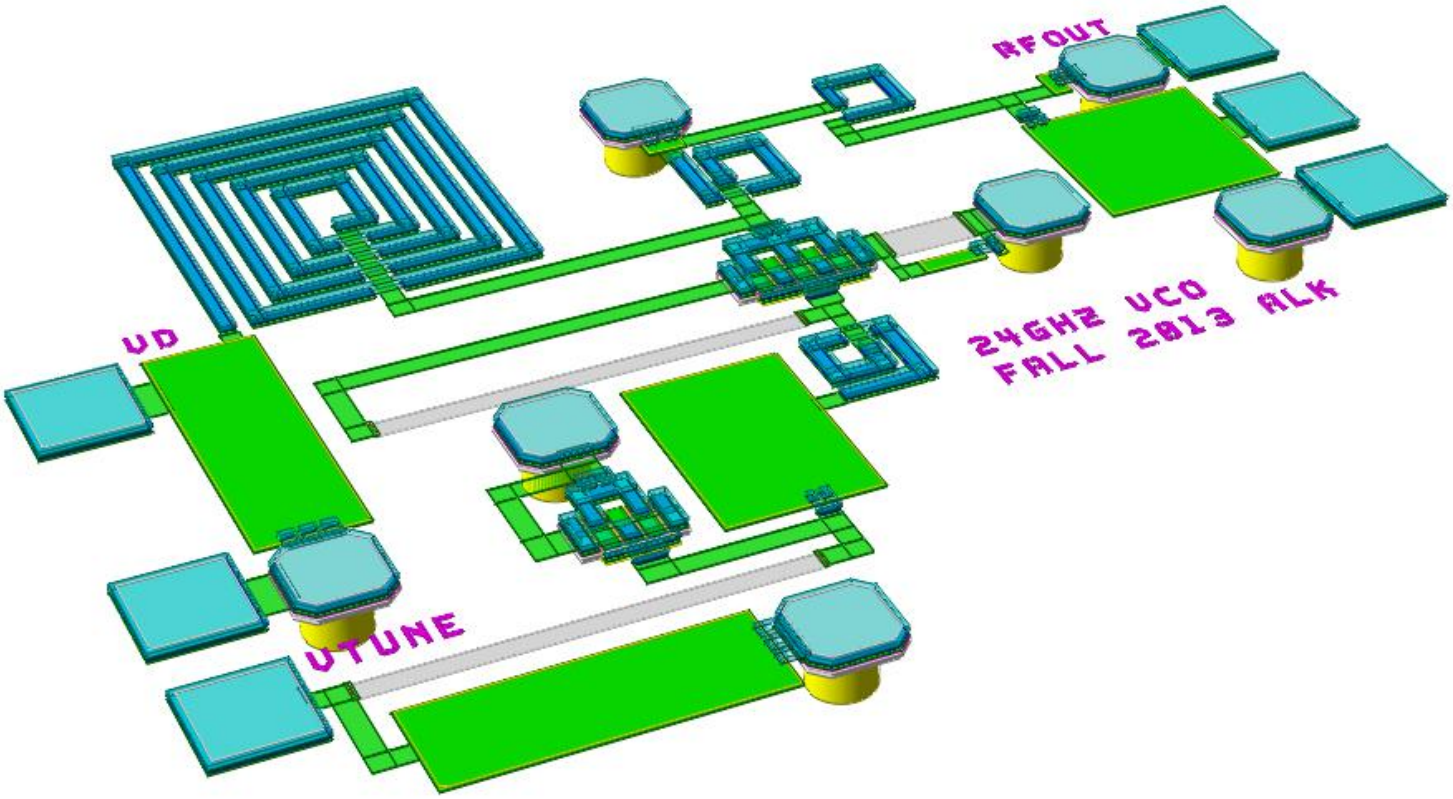
Table 2: Simulated LNA Performance

Johns Hopkins University

MMIC Design

525.787

A. Kordovski



Abstract
The purpose of this paper is to describe the design of a 24GHz Monolithic Microwave Integrated Circuit Voltage Controlled Oscillator using TriQuint lumped elements within the AWR Microwave Office design environment. The negative impedance method was used to design a series resonance oscillator and includes the following components which were layed out in a 60x60mil chip area:

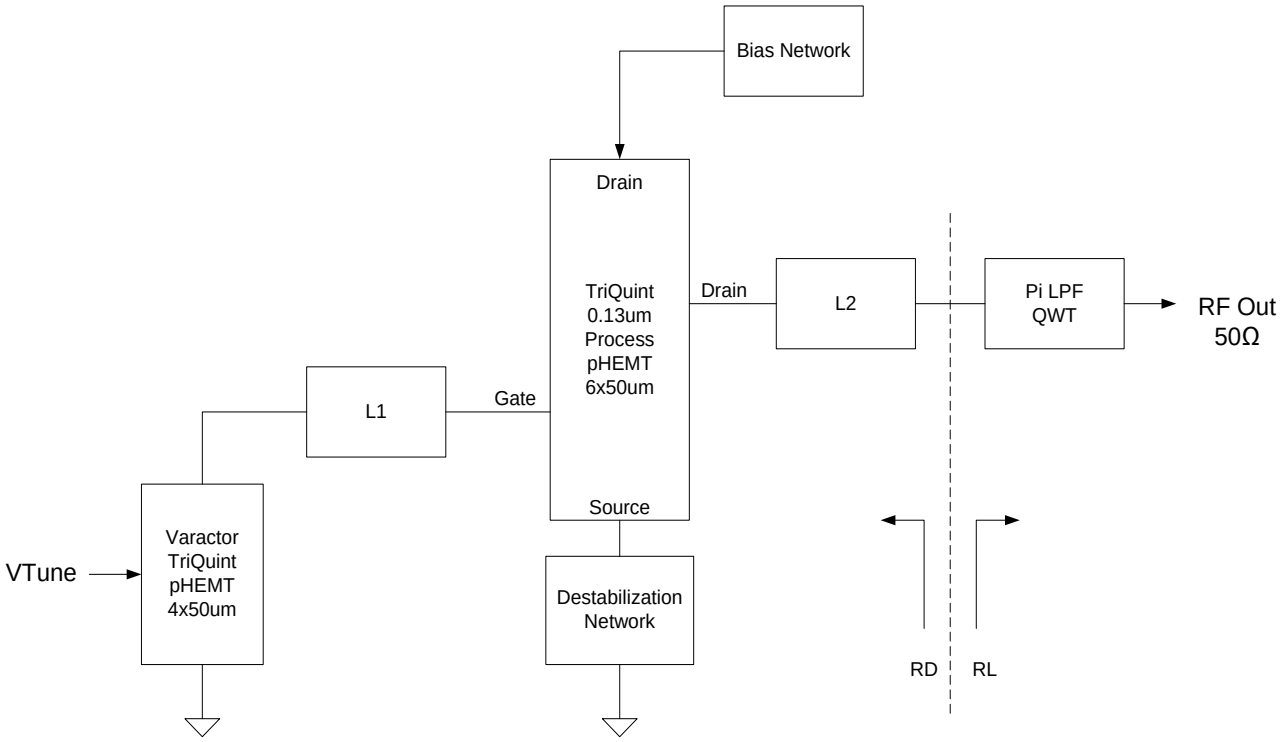


Figure 1

Introduction

The ideal VCO was designed to oscillate at 24GHz with Vtune =0V. After adding in MLINs to implement the layout, there were significant changes, and the design steps had to be repeated (and the design re-tuned) in order to ensure that the design would work at 24GHz, as shown by the simulations. The plot below shows the tuning limits and frequencies. At Vtune=0V, Fosc=23.64GHz. To achieve Fosc= 24GHz, Vtune=-0.17V. The voltage tuning range is limited, but provides a range of ~500MHz. No oscillation will occur below 23.26GHz (Vtune=+0.17V) or above 24.38GHz (Vtune=-0.34V).

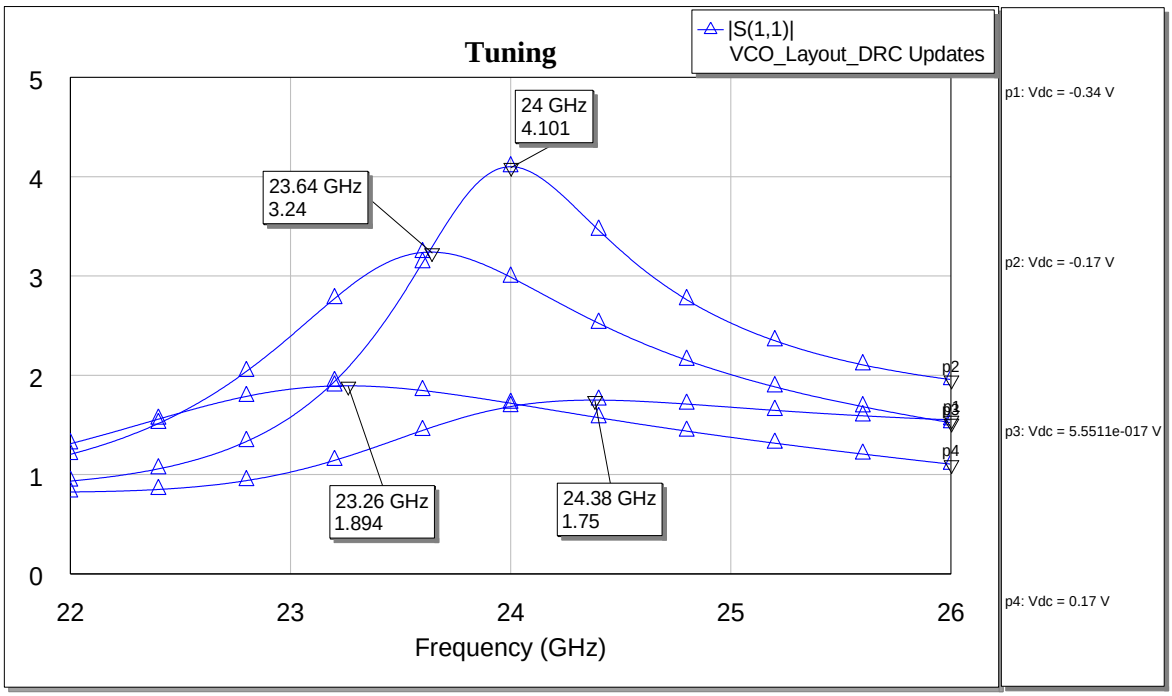


Figure 2

For the above design, the bias voltage Vdd is intended to be 4.5V (Id=21.5mA). Lowering the bias to Vdd=4.0V (Id=19.4mA) lowers Fosc ~100MHz overall and the magnitude ~0.12. So, there is an effect to changing the bias, but it is not overly significant. This effect can be quantified further during test. It is expected that Fosc may shift after fabrication, as well. Refer to **Figure 6** for Bias Check.

Design Approach & Simulations

The driving requirement for this design was to achieve Fosc=24GHz ± 0.2GHz and unconditional stability outside of this range. Since the primary goal of this design was basic functionality/proof of concept, performance measures such as output power and phase noise were not specified, but can be measured during test.

The basic design approach was the negative impedance method with the topology shown in **Figure 1**. It was deemed most efficient to do non-linear simulations upfront utilizing the actual device.

The first step was to destabilize the pHEMT. Generally, a source resistor is used (as shown below), but this was not enough to destabilize the device at 24GHz, so capacitive source feedback was employed.

L1 was set to center Fosc as close to 24GHz as possible while maintaining a magnitude of |Gamma|~3 as plotted on the compressed Smith Chart. The varactor was added in in place of the ideal 14pF capacitor and the feedback capacitor of the destabilizing network was slightly re-adjusted.

The varactor was designed to have a "reasonable" range around 24GHz. Refer to **Figures 3** and **3.1**.

Then, L2 was added and adjusted to set to shift the Fosc phase to 180° while maintaining |Gamma|~3. It was at this point the negative resistance looking into L2 was checked.

Figure 4 represents original (pre-layout) RD = -25.9Ω value and shows the zero phase crossing for Vtune=0V. For |RD|>3RL, this yielded an RL=8.63Ω. Thus, Zt = (8.63Ω*50Ω)^0.5 = 20.78Ω, from which the Low Pass Pi Filter Quarter Wave Transformer values were calculated. However, after the layout, the calculated values did not yield the expected results. The QWT had to be removed and re-tuned separately inclusive of the microstrip lines.

Figure 4.1 represents the checkout of the final layout looking into L2 (with the updated QWT disabled) for Vtune=-0.17V. This plot indicates that the oscillation frequency will be ~25GHz which is different from the **Figure 1**. Also, the slope of the impedance is slightly negative, instead of positive, as expected for a series oscillation scenario.

After adding in the QWT, **Figures 5** and **5.1** show the final results for Vtune=-0.18V (Fosc=24.03GHz) and Vtune=0V (Fosc=23.65GHz). All other frequencies from 1GHz to 30GHz appear to be stable.

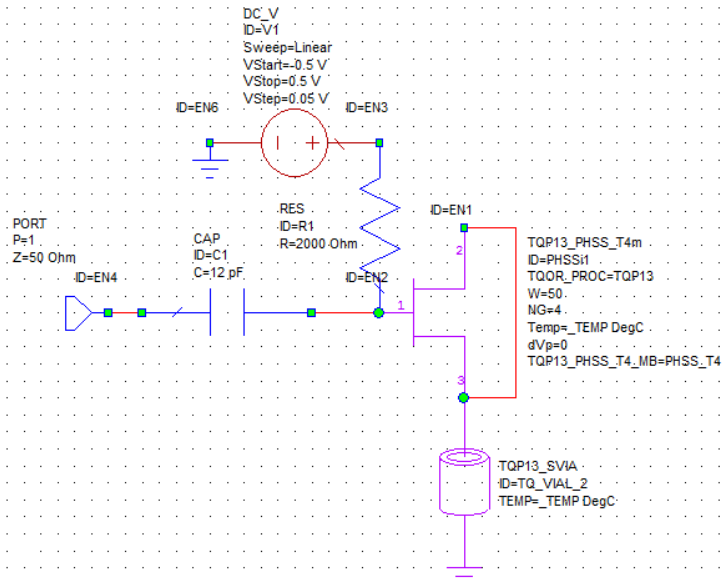
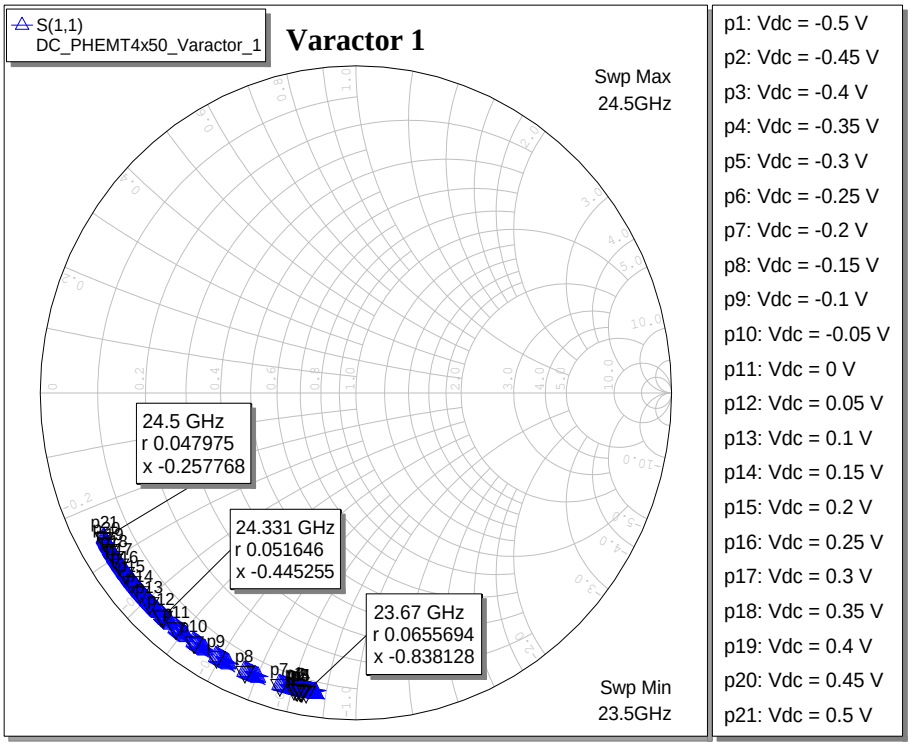


Figure 3



@-0.5V, C = 7.9pF @0V, C = 14.9pF @+0.5V, C = 25.7pF

Figure 3.1

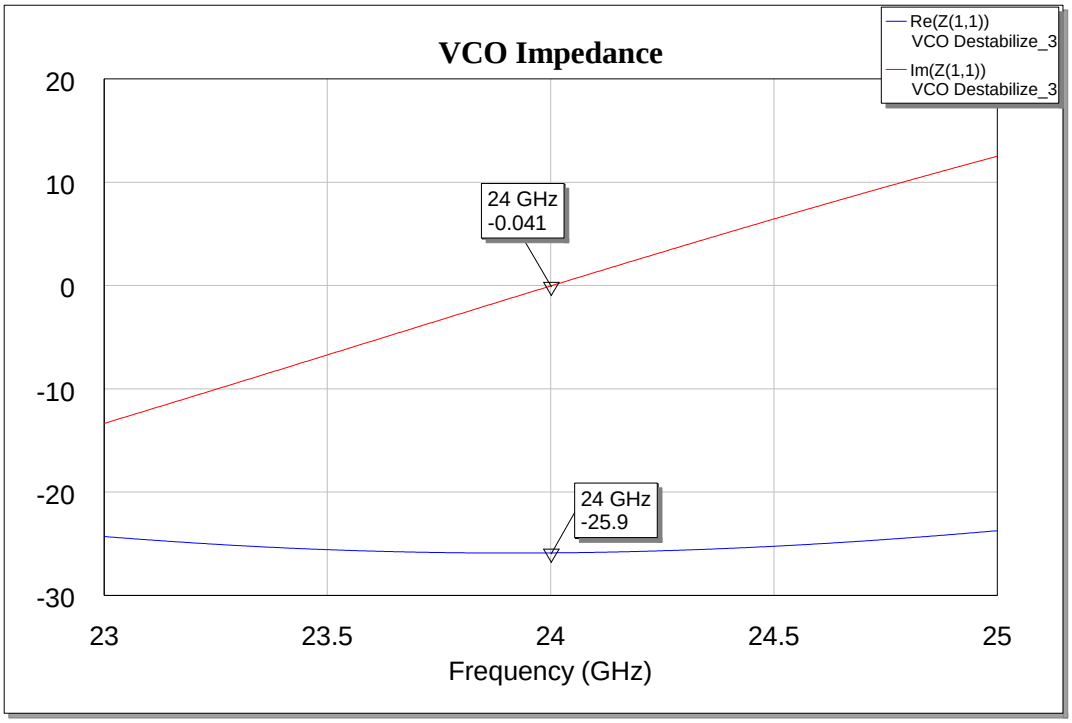


Figure 4

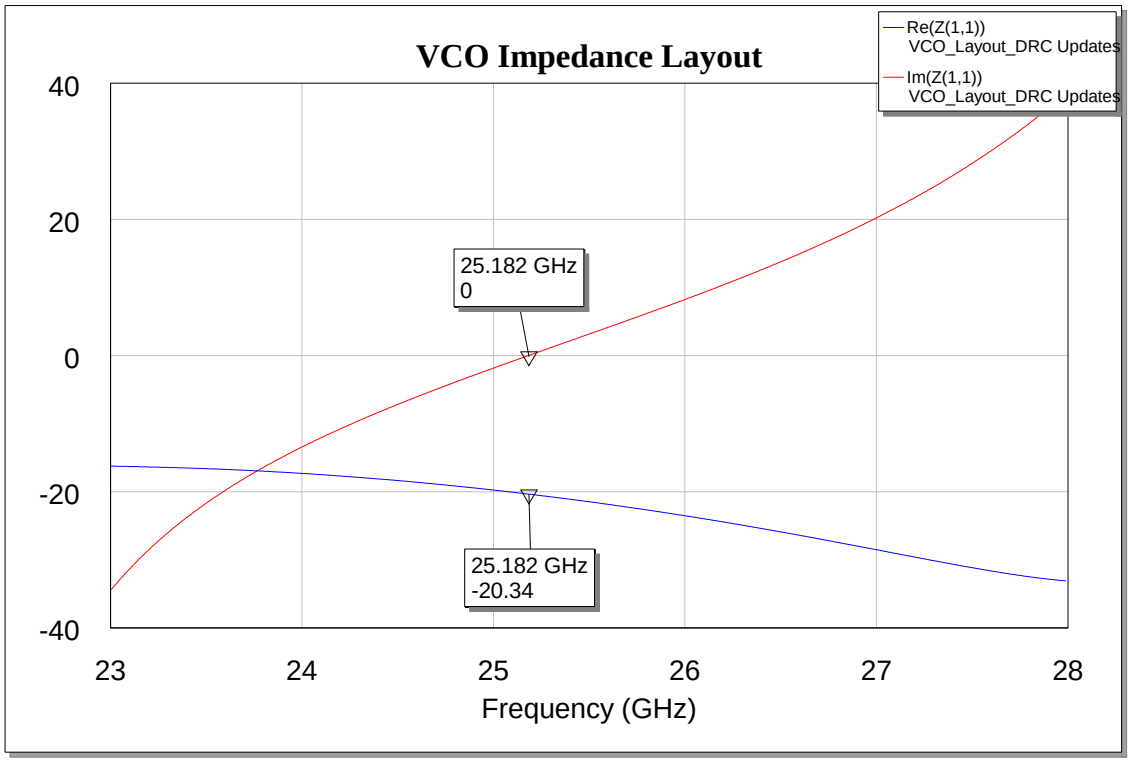


Figure 4.1

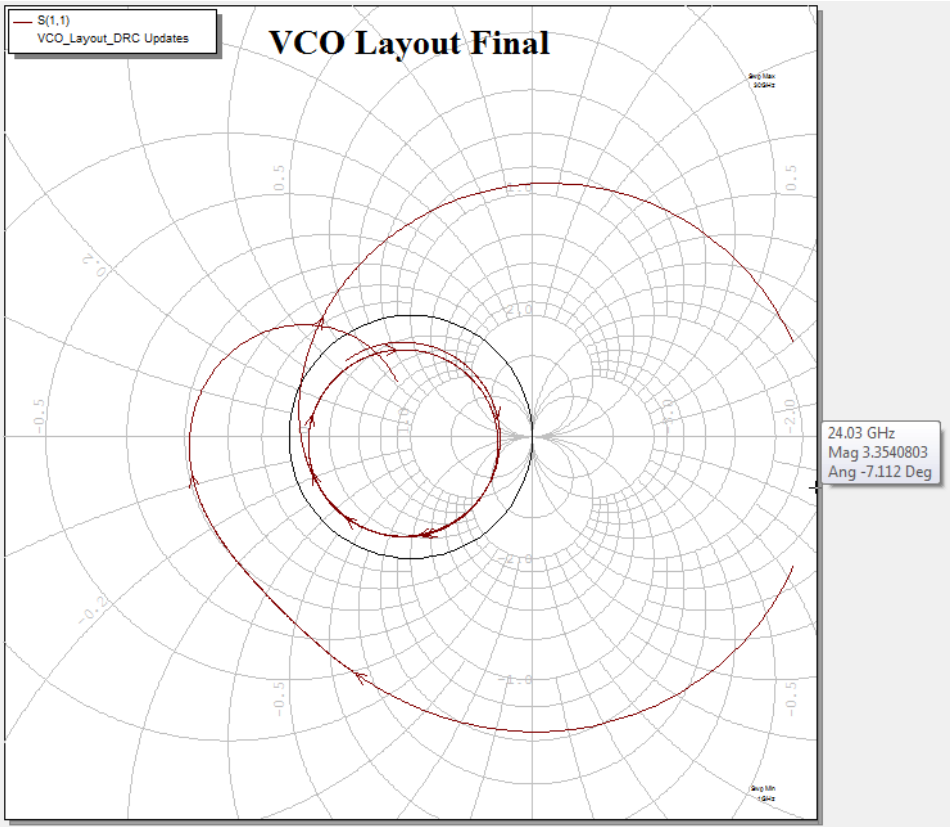


Figure 5 (Vtune=-0.18V)

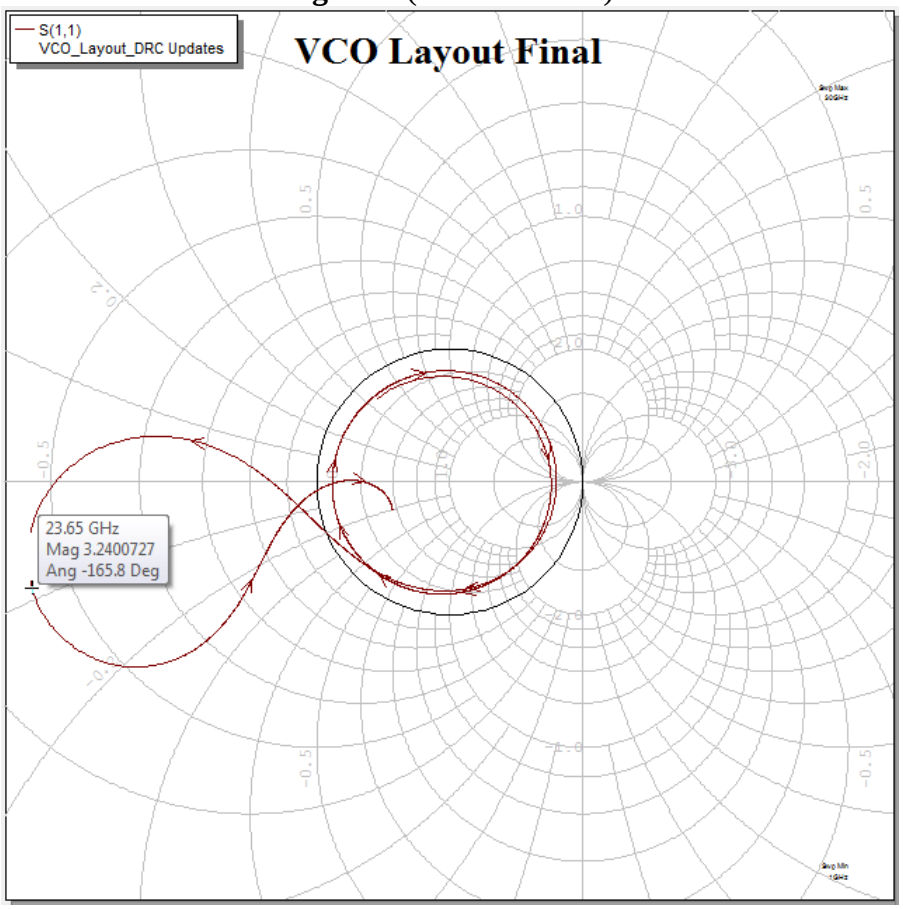


Figure 5.1 (Vtune=0V)

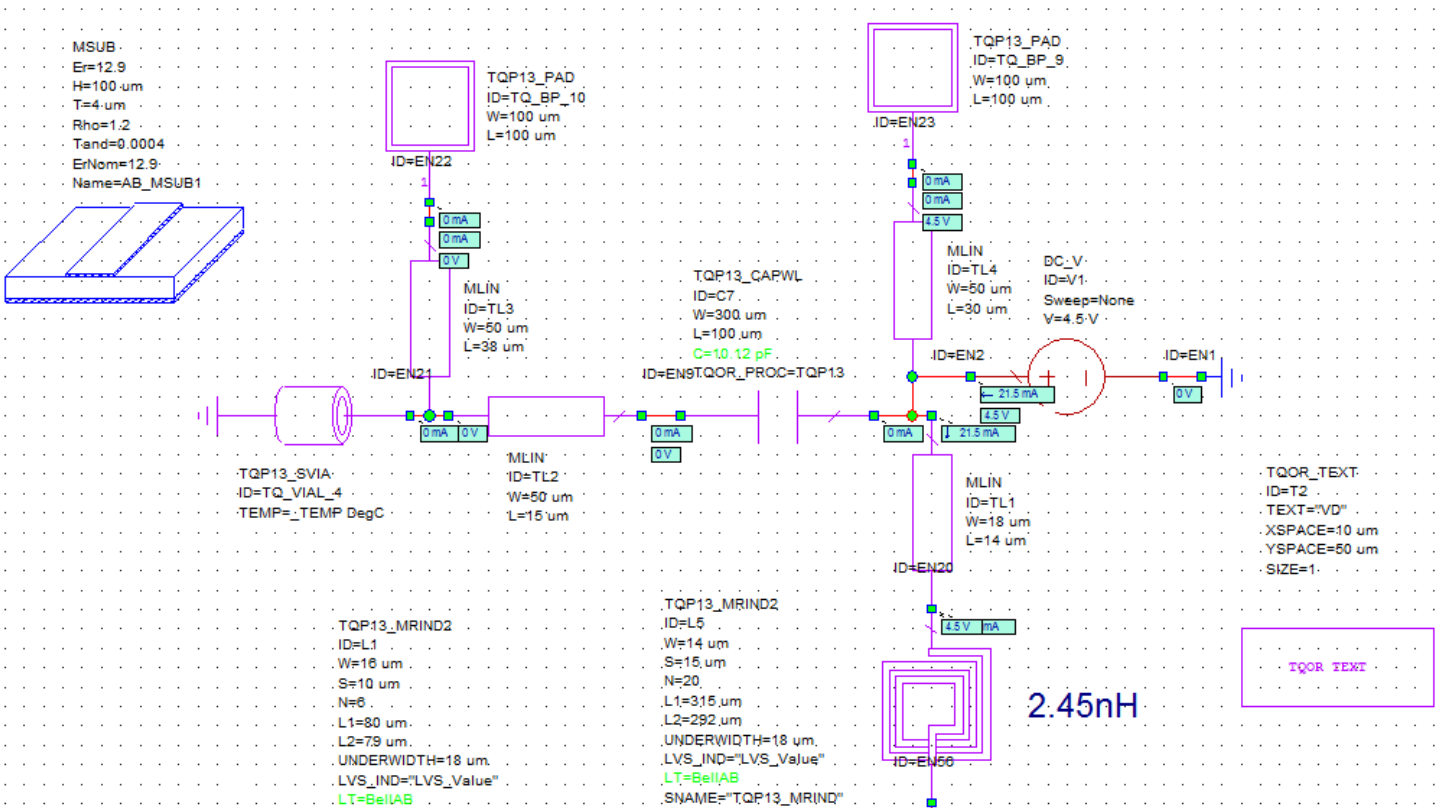
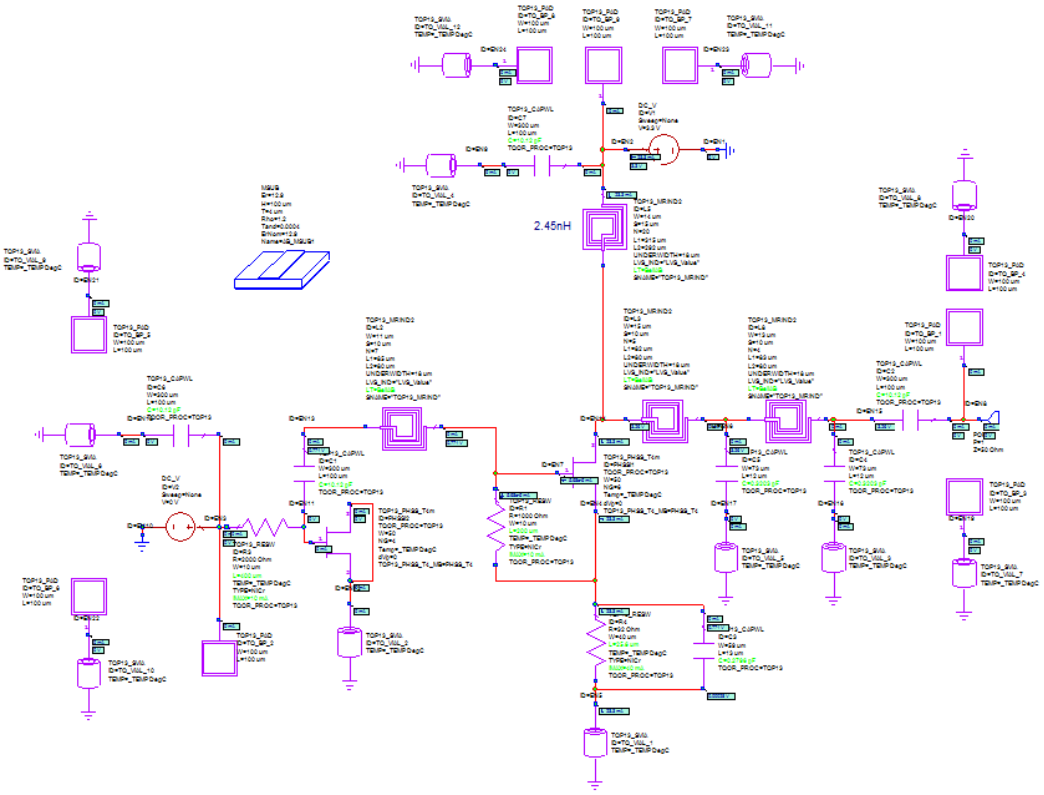
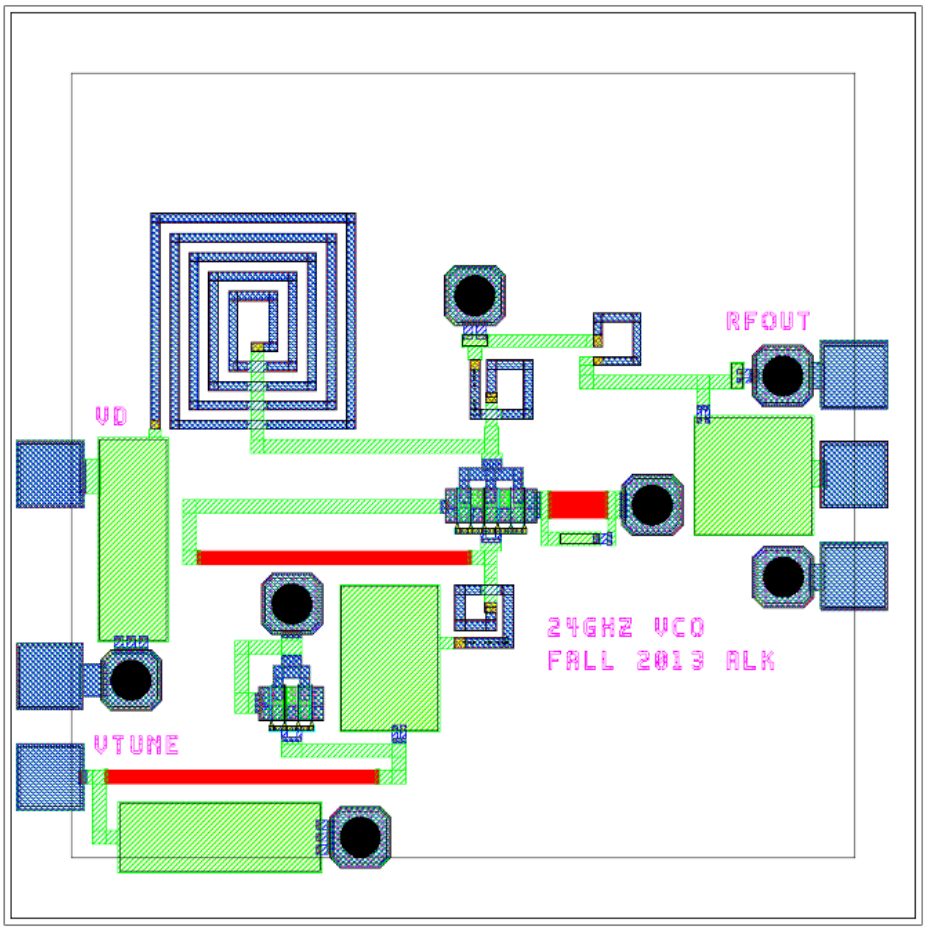


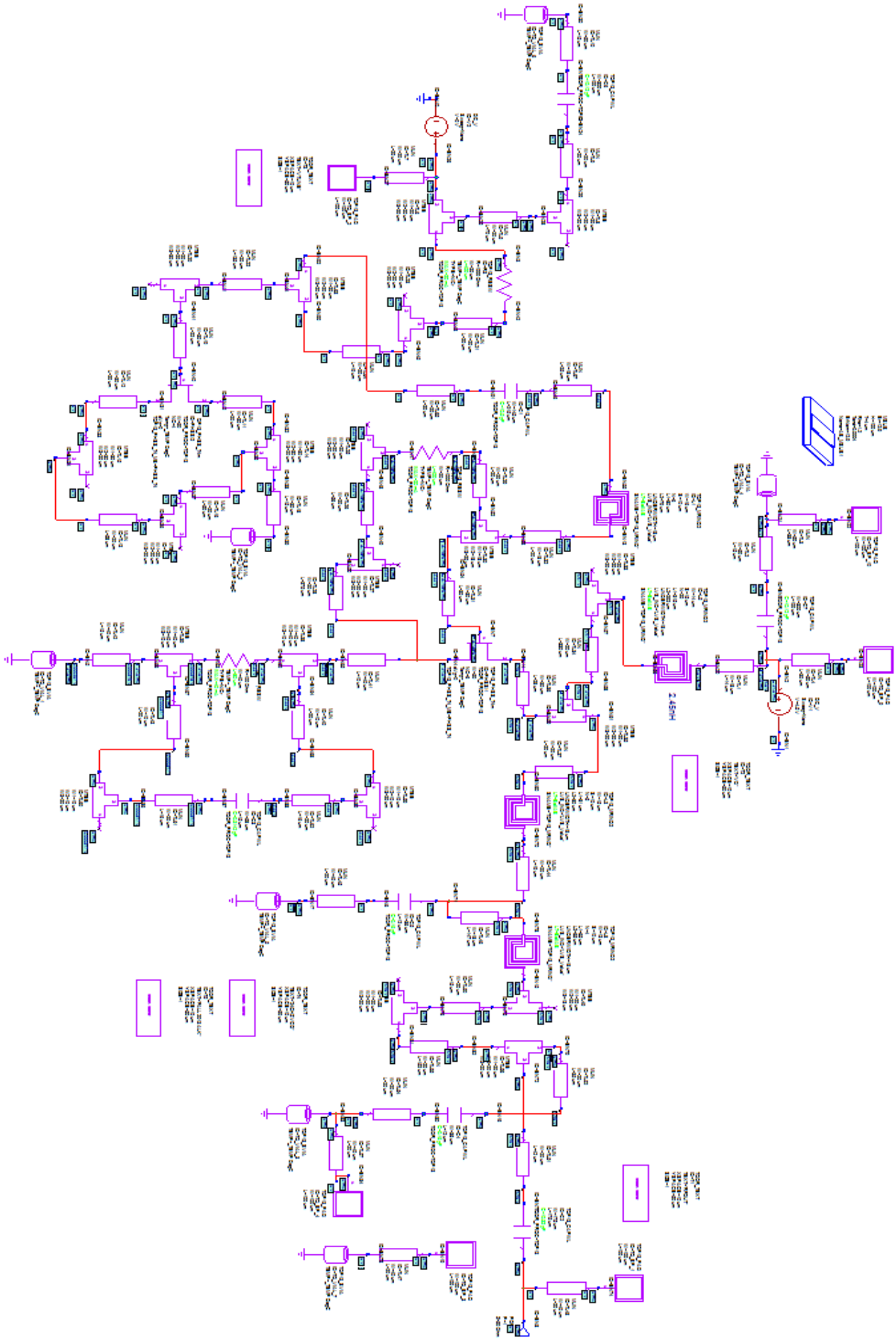
Figure 6.0 (Bias Check)

Schematic & Layout

The values in the schematic below had to be adjusted after the microstrip line interconnects were added for the final layout.







Test Plan

Required Equipment:

- Power supply and probe for bias voltage
- Power supply and probe for tuning voltage
- Spectrum Analyzer and RF probe for output signal

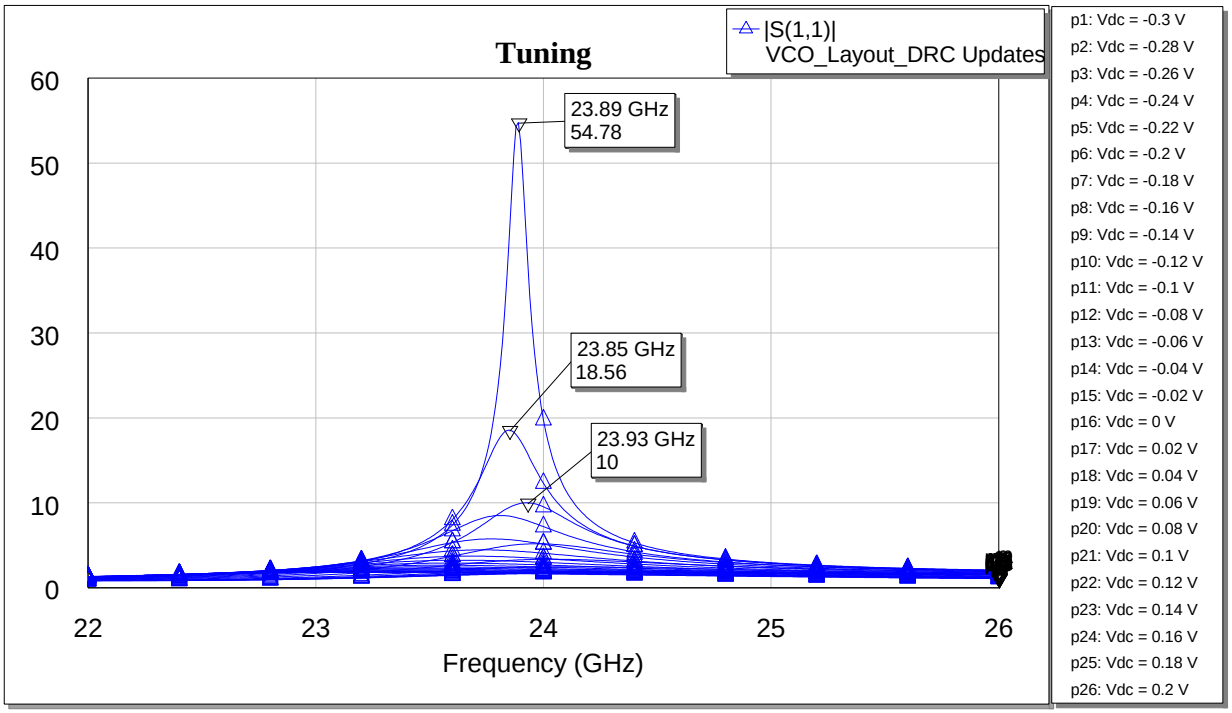
Procedure:

- Ensure power supplies are off
- Connect power supplies to VD and Vtune pads
- Characterize any RF interconnect losses
- Connect spectrum analyzer to RF Out pad
- Set VD power supply to 4.5V (Id=21.5mA)
- Set Vtune to 0V
- On spectrum analyzer, check circuit is oscillating at ~23.6GHz
- Adjust Vtune to -0.17 to -0.18V, and check circuit is oscillating at 24GHz
- Adjust Vtune from +0.2V to -0.3V in 0.02V steps and record oscillation frequency and output power; at each step, re-set VD to 4.0V (Id=19.4mA) and 5.0V, and observe any difference(s) in results and record oscillation frequency and output power for each bias voltage

Summary & Conclusions

The primary lesson learned with this MMIC VCO design was the drastic property shift after the MLINs and the design was layed out. It not only affected the Pi LPF QWT, but Fosc collapsed. The various parts of the circuit had to be disabled and the design process had to be stepped through again in order to compensate for the line length inductances and capacitances.

From the final simulations it appears that the design will oscillate at or near 24GHz. However, a more detailed check across the tuning range reveals an unusually high resonant peak within the tuning range. Whether oscillation is sustained for the peak remains to be characterized during test. An electromagnetic simulation may yield further insight into this potential phenomenon prior to test.



Despite this, however, the Smith Chart simulations of the final design show conditional stability for the 1GHz to 30GHz range, excluding the 23GHz-25GHz range.

Once the design is characterized through test, further design improvements and refinements can be investigated before it is incorporated as part of a PLL circuit for use as a local oscillator.

It will be interesting to see if the fabrication process shifts Fosc significantly compared to the simulations.

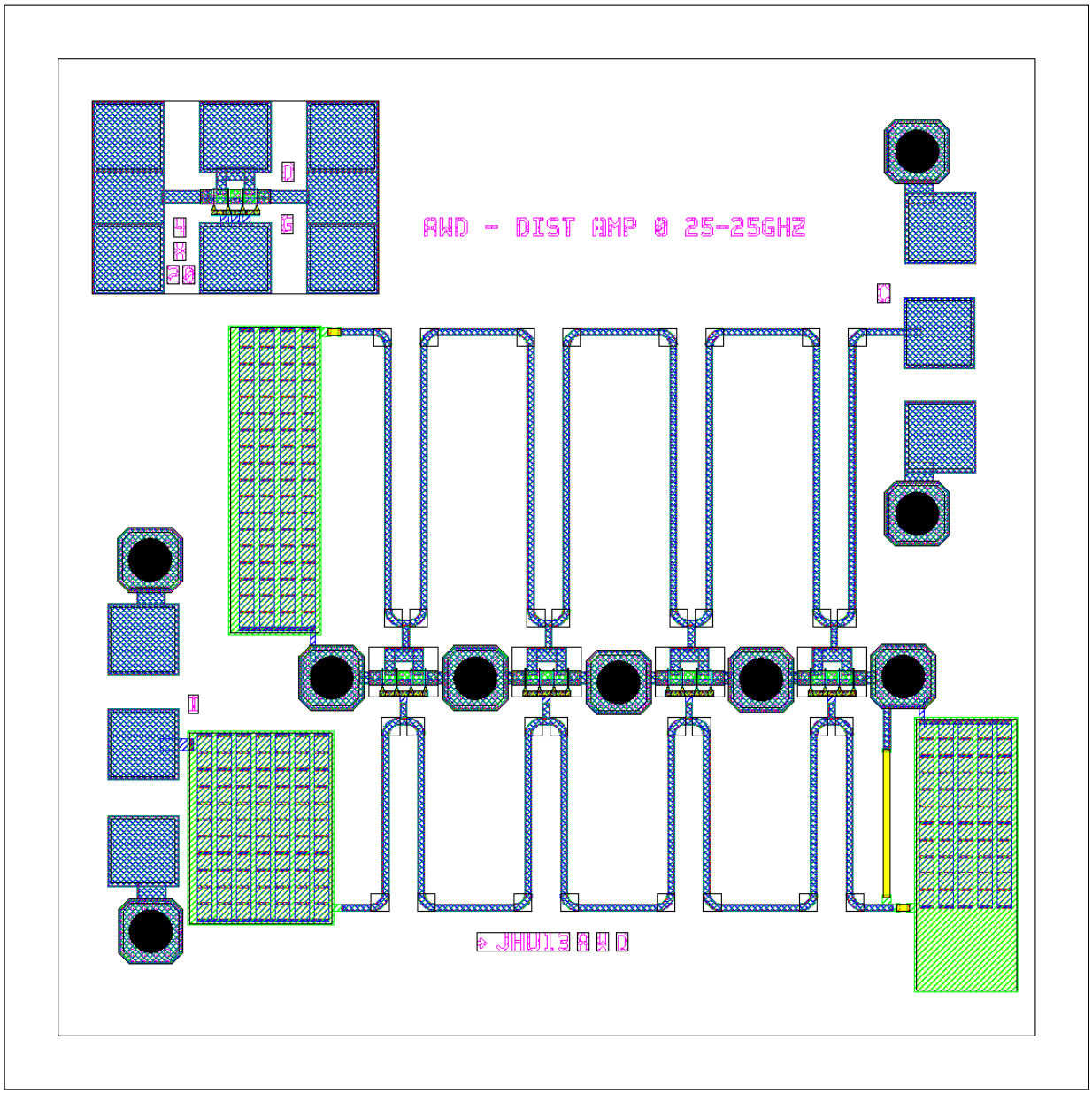
References

[1] *gEE-CAD Tutorial, Part D, Voltage Controlled Oscillator (VCO)*, Dr. Lee Edwards

[2] *Voltage Controlled Oscillator (VCO) Design Notes*, John Penn

[3] *Practical MMIC Design*, Steve Marsh

0.25 to 25 GHz Distributed Amplifier



Alan Doucette
December 2013

Abstract
This Distributed Amplifier design uses TQT-.13um technology on a 100x100 um chip to create a 10dB amplifier from 0.25 to 25 GHz with 3v supply. The gain band was designed to be flat within 2 dB. Noise was less than 3 dB down to 4 GHz and reached a maximum value of 6dB at 250MHz. Return loss is 14dB or better.

Introduction
In developing this distributed amplifier, the goal was to achieve 2 decades worth of usable bandwidth. Another specific goal was to be able to be fed by 3 volts—a value achievable by batteries or other low voltage sources. The other goals of 10dB gain and 2 dB gain flatness were of secondary importance. Next, return loss was targeted so that a good match could be insured. The last figure of merit, noise figure, was of reviewed but not optimized. The original intended purpose of this amplifier was as a wideband LNA, but in chasing that much bandwidth the noise figure got too large. Instead, now the device would most properly function as a low voltage wide band gain block amplifier. Per Triquint's homepage as of December 2013, they do not currently offer a gain block amplifier that operates at 3v.

Design Approach
The approach to meet the specified design criteria was to use a distributed amplifier topology. The theory behind the distributed amplifier is that a lumped element 50 ohm transmission line can be replicated two repeating elements. The first is the shunt Cgs capacitance inherent in the FET structure. The second structure is to use the specific inductance of the gate microstrip line to match that of the Cgs value. Because impedance equals (L/C)^.5, as long as L and C are picked such that this equation equals 50 ohms, then the response is independent of frequency as a first order approximation. In actual implementation, parasitics are introduced that end up degrading ideal performance.
In laying out the actual design, C is a function of each particular PHEMT FET structure. As a rough approximation, Cgs depends on the product of the number of FET fingers and size of FET fingers. An early trade was performed by looking at several combinations of both fingers count and sizes. It was determined that 4x20um was a good value for a flat broadband response. Enlarging the FET, either by increasing the number of fingers or size of fingers, caused the Cgs capacitance to dominate at lower and lower frequencies. This also had the effect of mandating longer and longer inductive traces between each sequential FET stage. So not only did performance suffer but the practicality of implementation got harder and harder on the given chip size.
One thing to note is that due to the architecture of distributed amplifiers these PHEMT stages are not terribly efficient or high gain as a single stage. Therefore, by placing four in parallel, the overall gain requirement of the amplifier is met. Note that because the PHEMT FET stages are in parallel and not in series that the gain sums linearly, not multiplicatively.
The original design goals were two decades of bandwidth from 0.3 to 30 GHz with 10+ dB of gain. The design started off meeting the 30 GHz high end with ideal elements, but as they were replaced with microstrip and TQT elements, the high end began to suffer. Since there an ISM band at 24 GHz, the decision to back off the 25 GHz was made. At the same time, certain measures had to be undertaken in order to recover 50 MHz on the low end to maintain 2 decades of bandwidth. As mentioned in the Introduction section, the goal of 2 dB gain flatness was next on the list. This was deemed important because high end gain could always be increased by adding resonances in the inductive gate feeds, but that defeated the fundamental philosophy of the design approach. These high end resonances were also thought to be potential destabilizers of the overall amplifier.
The last sought-after goal was a 3dB noise figure across the design bandwidth. This was a nice goal, if not ultimately impractical. The problem was that in order to decrease the NF at low frequencies the on-chip capacitors had to be made larger. Since there are three main on-chip blocking capacitors in the final layout that all effectively target the same frequency, increasing one meant increasing three. Ultimately, a practical size limitation was reached. In addition, the low end gain would rise, which would knock the design out of the 2 dB gain flatness window.
The design was originally planned to be biased with .1v for Vgs, but after layout considerations it was decided that 0v bias would be best. That way no extra voltage need be brought onto the chip. The gates for each PHEMT were tied to ground via a large 1K resistor. This was chosen because it was able to set the DC Vgs bias

point, but the 1K value did not have much impact on the overall match. Since the design consisted of replicating structures, thick metal was used for almost all traces to keep line resistance as low as possible.
Table 1 shows that except for noise figure, the design met all specified criteria. Figure 1 is an ideal component schematic.

Parameter	Requirement/Goal	Expected Performance
Die Size	.100x.100	.100x.100
Drain Voltage	3v	3v
Bandwidth	2 decades	.25-25GHz
Minimum Gain	10dB	9.97dB
Gain flatness	<2dB	1.89dB
Return Loss	>10dB	13.91dB
Noise Figure	<3dB	6.21dB worst case

Table 1: Summary of design goal and expected performance

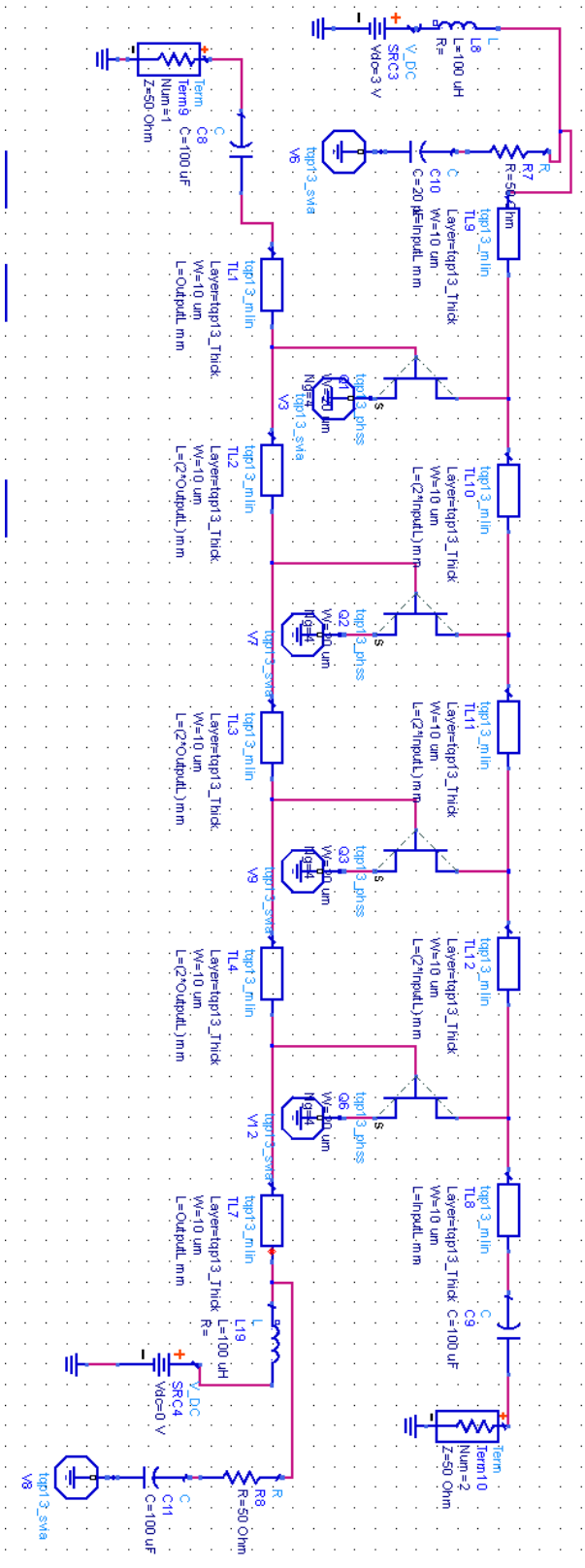


Figure 1: Ideal Circuit Schematic

Simulations

Figure 2 and Figure 3 show the simulated results of the ideal circuit compared the final layout circuit.

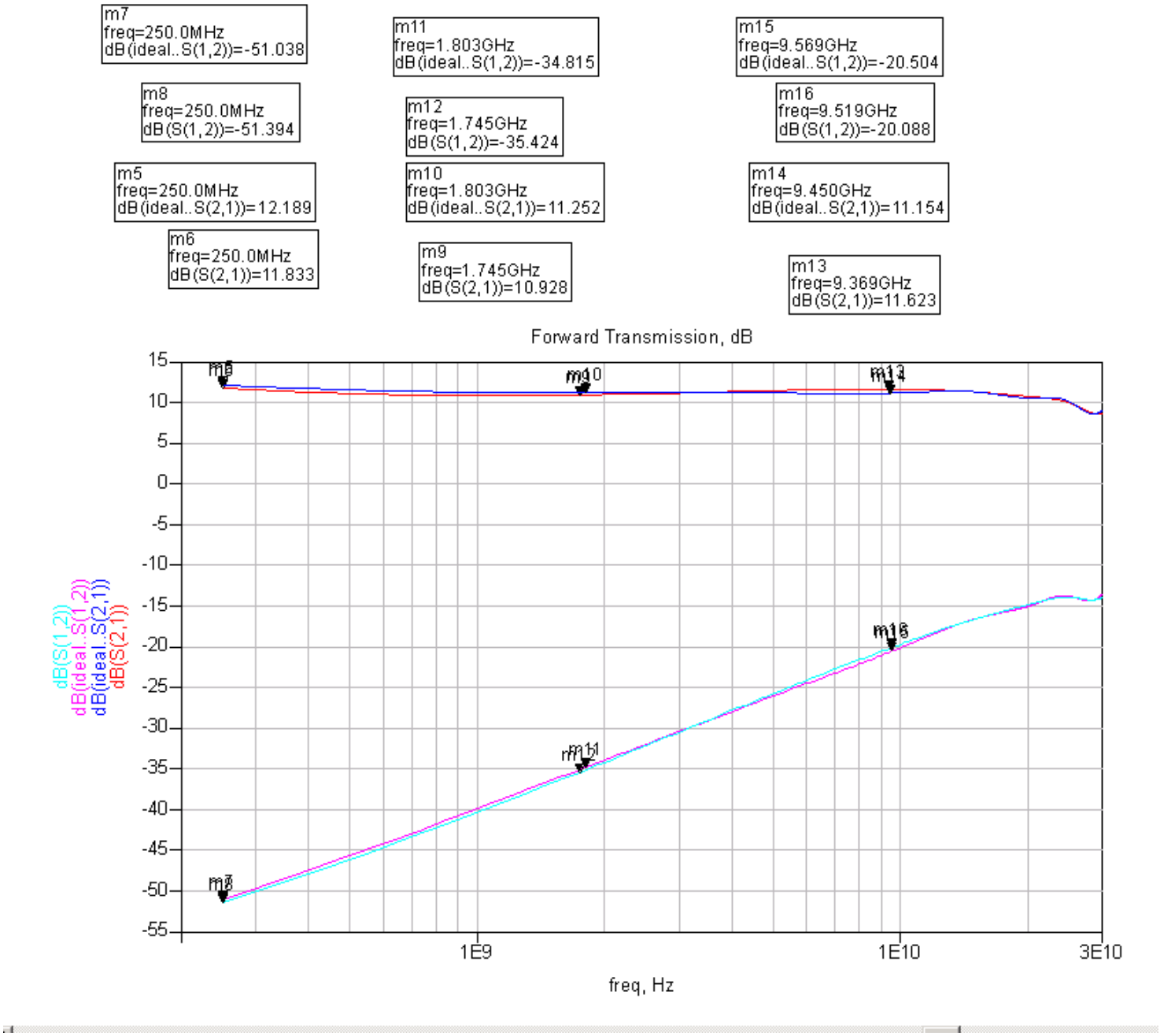


Figure 2: Performance vs Frequency (Log scale)

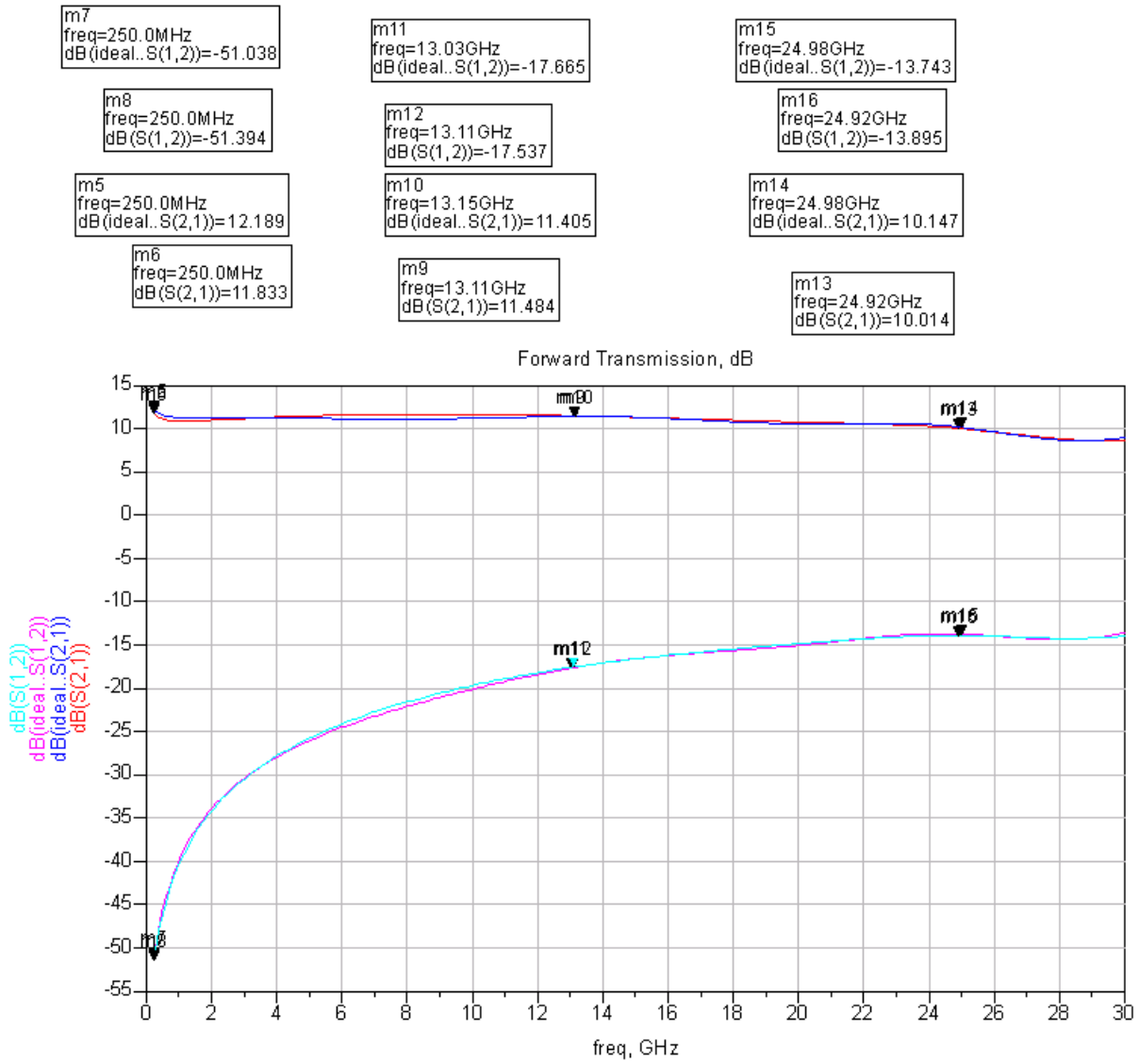


Figure 3: Performance vs Frequency (Linear scale)

This shows that the performance of the final layout closely tracks an ideal circuit, but there are noticable differences due to parasitics. Figure 4 shows input and output match. The complex plots show qualitatively how good the match it, while the linearized output match plot shows the magnitude of the match for the final, realized circuit. Figure 5 shows stability of the final, realized circuit. This is more marginal than originally intended, but stability can be increased by just increasing the drain voltage. Figure 6 shows NF performance across the bandwidth of interest. Figure shows a DC Bias simulation of the realized circuit.

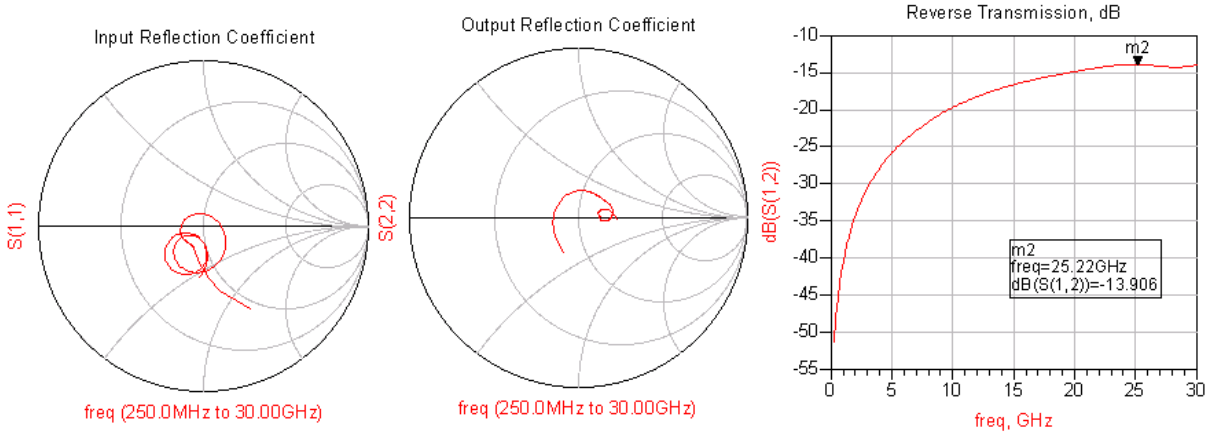


Figure 4: Simulated Input and Output Match of Realized Circuit

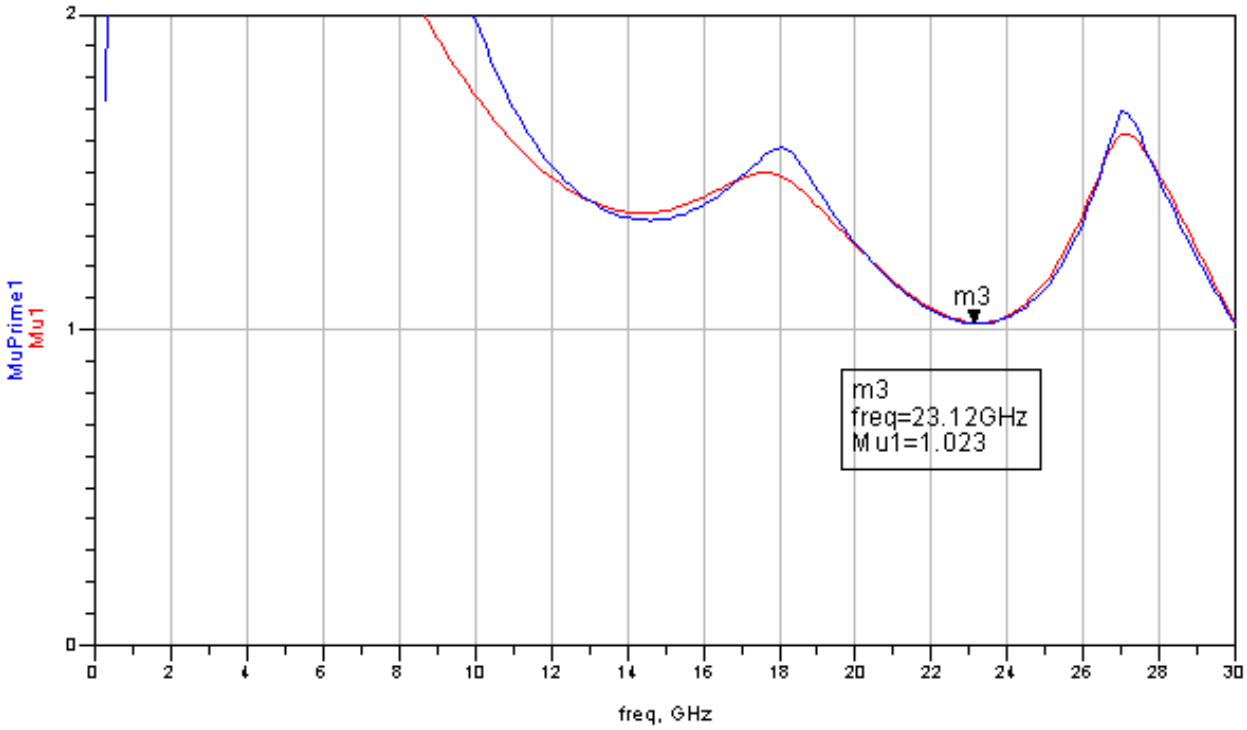


Figure 5: Simulated Stability of Realized Circuit

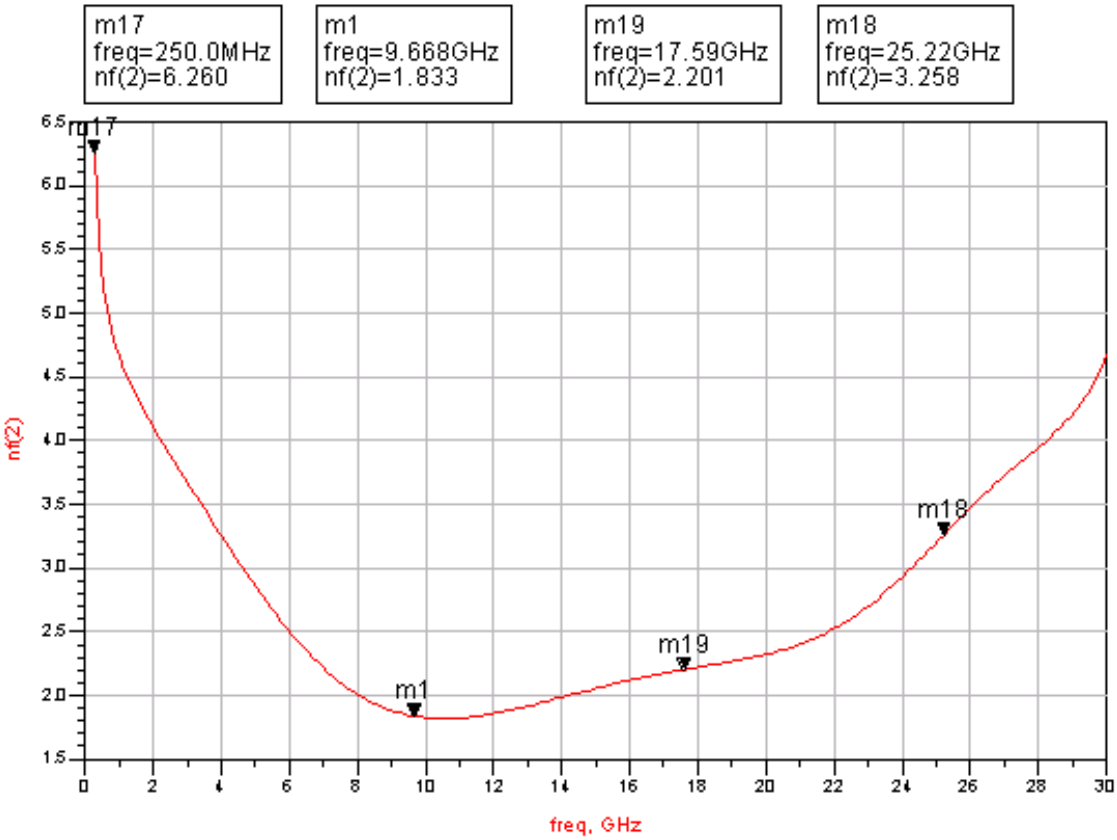


Figure 6: Simulated Noise Performance of Realized Circuit

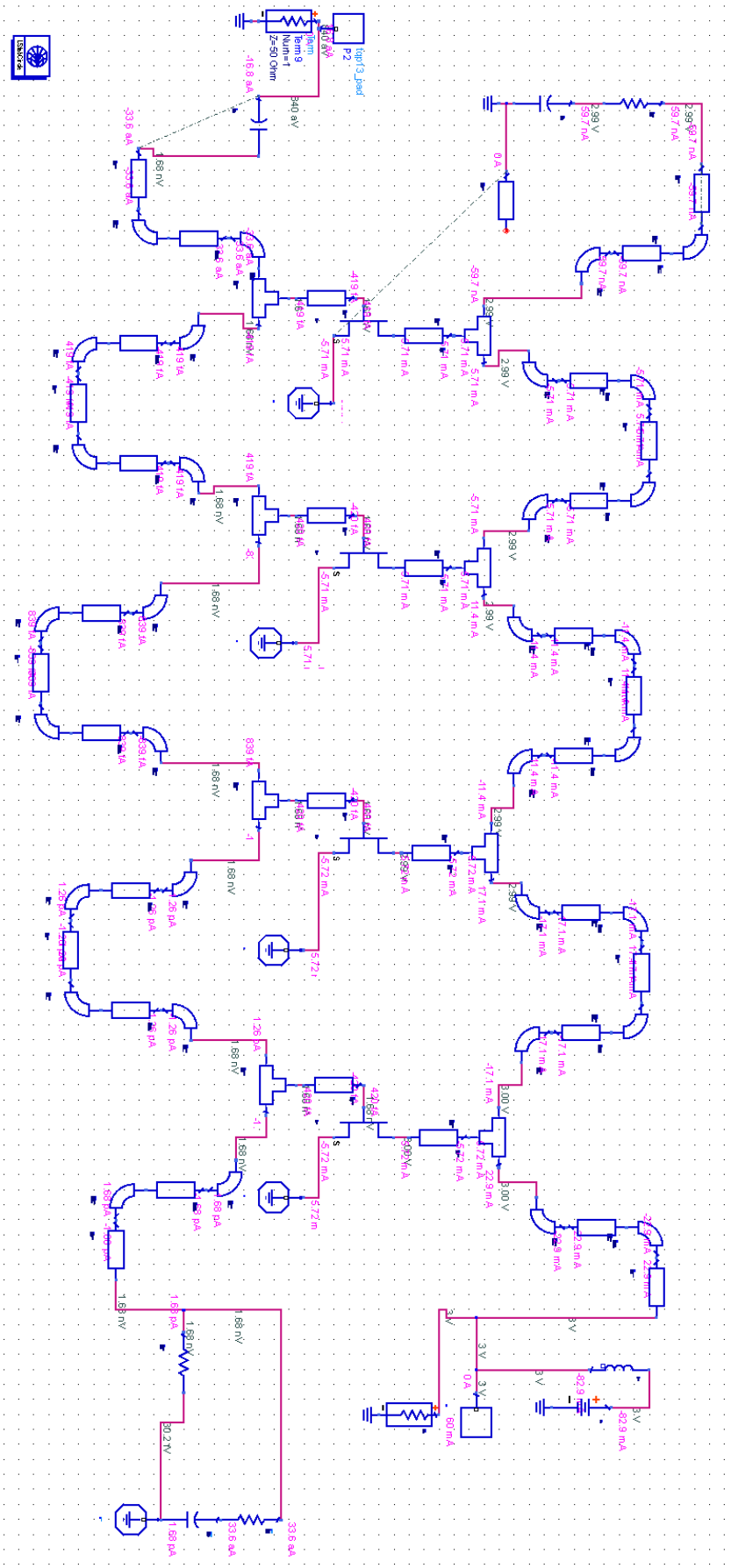
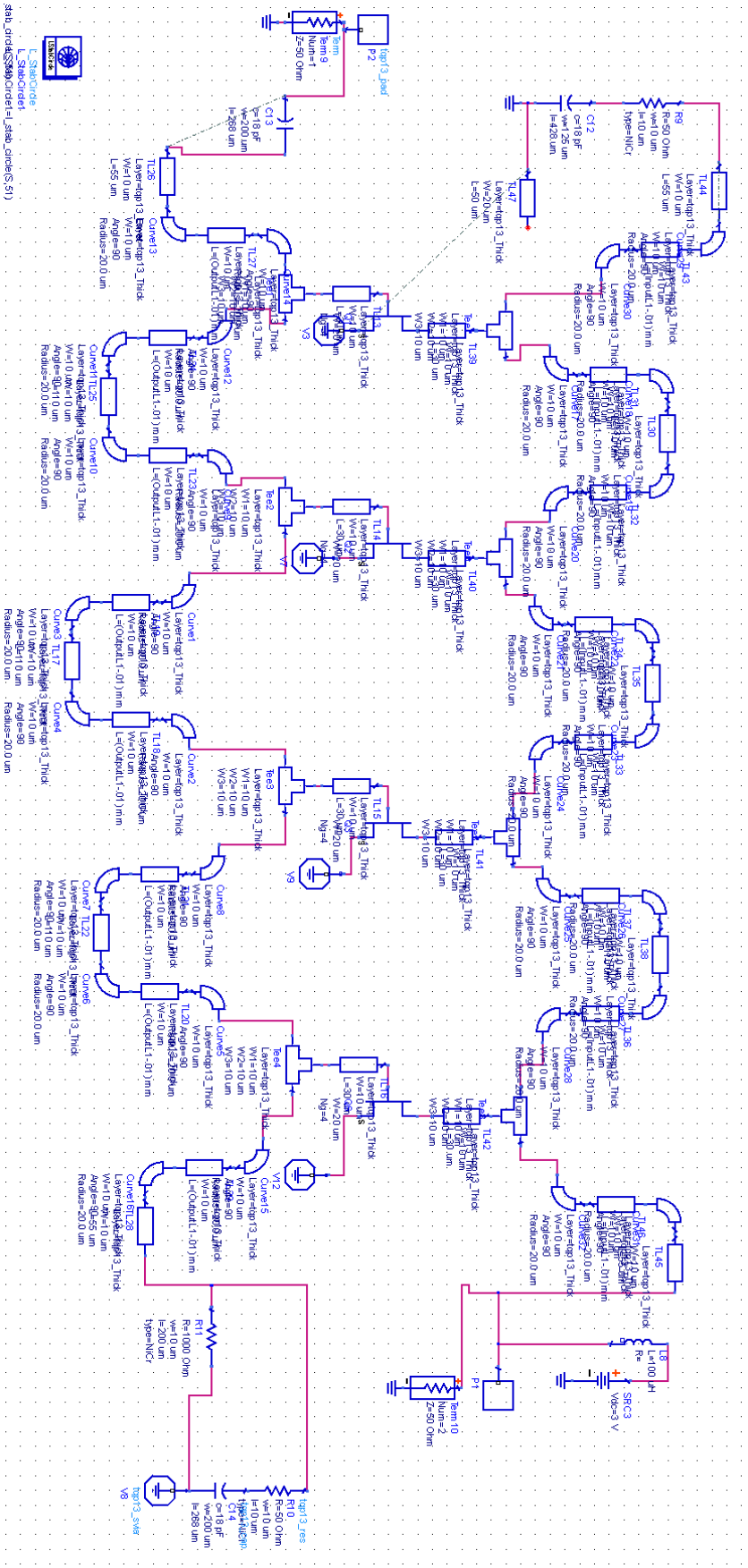
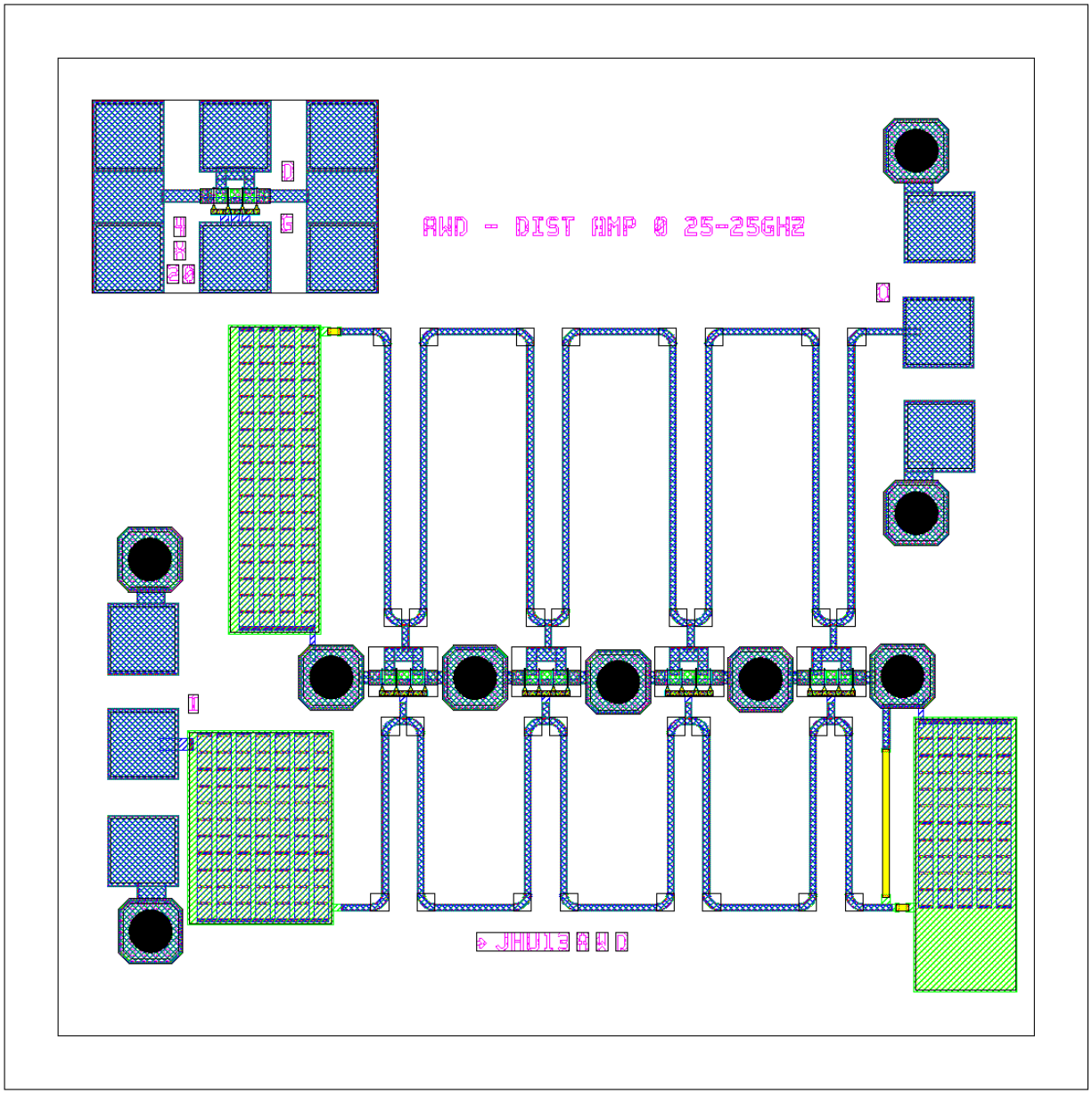


Figure 7: Simulated DC Analysis of Realized Circuit

Final Layout Schematic:



Layout Plot:



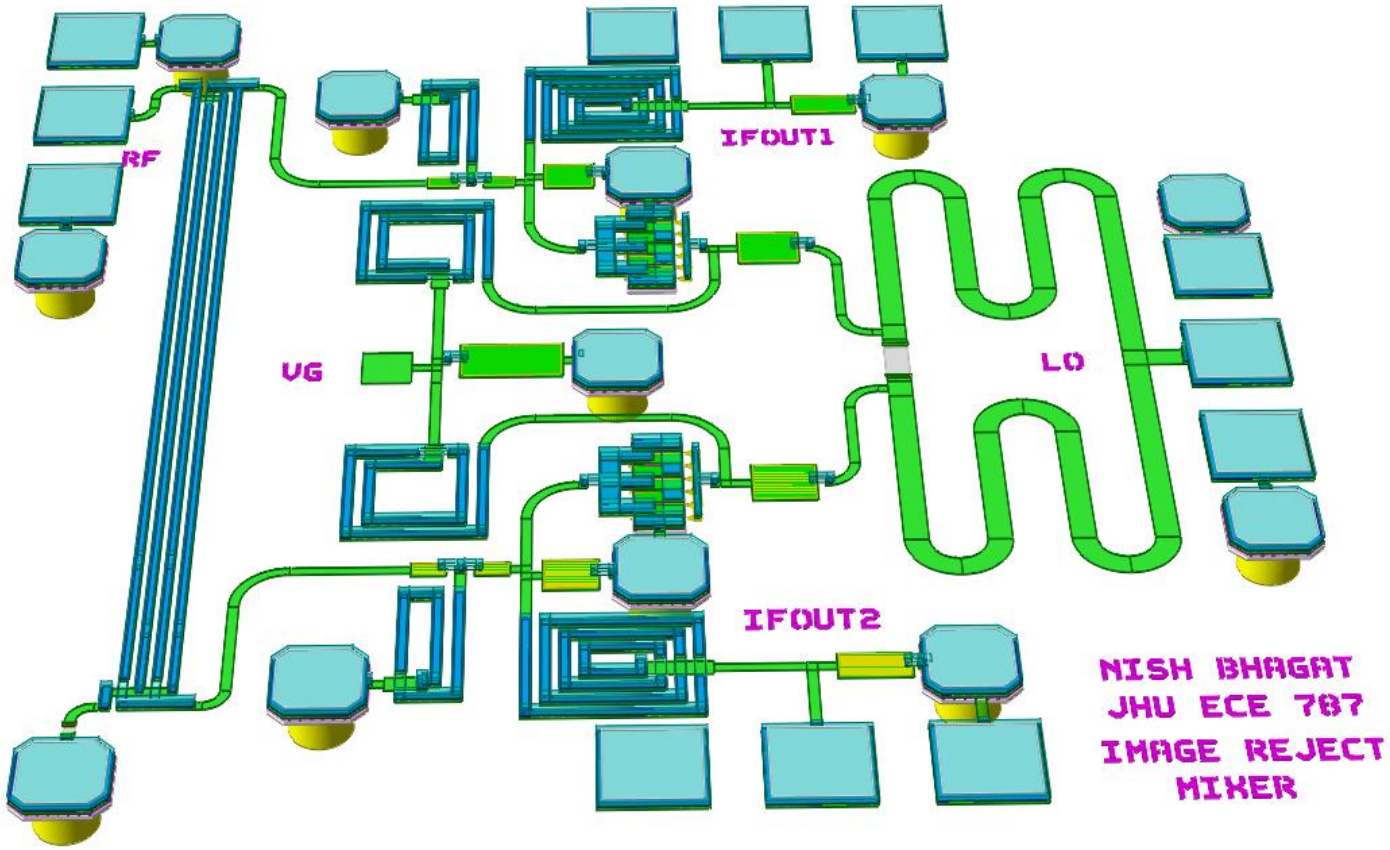
Test Plan:

1. Connect 3Vpower supply (power off) to network analyzer bias tee to bring power onto the chip.
2. Connect a network analyzer (signal off) to the ground-signal-ground pads for “I” and “O” on probe station
3. Set a current limit on the power supply to around 90 mA. The DC annotation says that the circuit should only draw 83 mA—60mA of which goes to the 50 ohm load of the network analyzer.
4. Set the power supply to 3V and turn on the output.
5. Expect gain between 9 and 12 dB and return loss better than 10 dB on the Network Analyzer.

Conclusion

Large gain bandwidths are achievable by using a Distributed Amplifier architecture. Simulations show this design has 10+ dB of gain from .25 to 25 GHz—two decades of bandwidth. Simulated gain flatness of 1.89dB was achieved for an input drain voltage of 3v. The design should be stable from DC to 30 GHz and shows good input and output match. Given the high noise figure of the amplifier, this design would most appropriately be used as a large bandwidth gain block amplifier. The area I am most concerned about is stability above 30 GHz. I did not focus on this because the test equipment cannot measure performance above 30 GHz. Given the outlined test protocol, measured performance of the device should be easily attained and can be compared to simulations.

24GHz Image Rejection Mixer



Nish Bhagat
ECE 525.787 – MMIC Design
JHU EP Fall 2013

Abstract:

This is an Image Reject Mixer implemented in GaAs technology using TriQuint's 0.13um pHEMT process. It is designed for a RF input of 24GHz and a Local Oscillator (LO) input of 23GHz. This is designed as a low side inject mixer giving an output Intermediate Frequency (IF) of 1GHz. The design has 4 main parts. The first part is the 90° Hybrid Coupler that is implemented as a Lange Coupler to save space. Then, the two 90° phase offset outputs go to the second and third parts; the mirrored Mixers. These mixers are implemented as Resistive FETs to, again, save space and keep the voltage and amperage required low. These mixers are also fed by a distributive Wilkinson Coupler that splits the incoming LO signal evenly, which is the last part. Ideally, there would be an IF 90° Hybrid Coupler to bring back the offset IF outputs to get the image rejection. However, due to space and time constraints that portion has been omitted.

Introduction

An Image Reject Mixer gets rid of the unwanted mixer result, which sometimes can be very close and hard to remove with narrowband filters. Due to the image rejection properties of the mixer, it also reduces the noise figure by at least 3dB.
This technology was originally developed by NASA for the Cassini Probe Mission sent to Saturn. They wanted a way to be able to communicate with the spacecraft over long distances without having to worry about the probe getting the signals mixed up. This technology has manifested itself in all sorts of modern day adaptions; from cell phones to navigation radar receivers.

Design Approach

This MMIC chip has been designed for GaAs using TriQuint's 0.13um pHEMT process. We were given a design frequency goal of 24GHz and a physical size of 60 x 60 mils. Beyond that we were not given any other hard constraints.
I chose this design because I got to design, build, and test a simpler version of this, designed for 2.4GHz on Rodgers material. That design was for a previous class with Professor Chris Fazi (ECE 525.791).
This design has 4 main parts:

1. First part is a 90° Hybrid Coupler that is implemented as a Lange Coupler to save space.

2. Then, the two 90° phase offset outputs go to the second and third parts; the mirrored Mixers. These mixers are implemented as Resistive FETs to, again, save space and keep the voltage and amperage required low. The mixing actually happens with a low pass filter and a high pass filter on the drain of the FET (see figure 1), while the LO is on the gate.

3. (Same as #2).

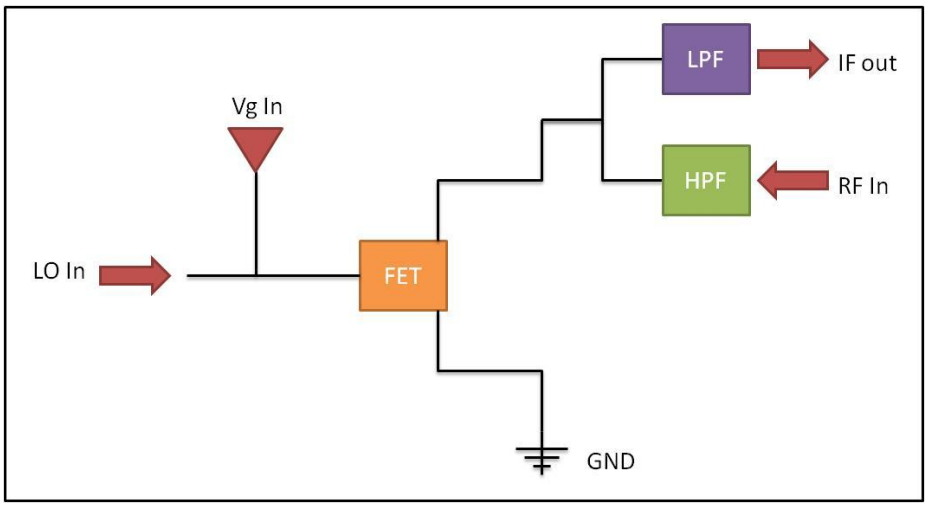


Figure 1: Resistive FET Mixer

4. These mixers are also fed by a distributive Wilkinson Coupler that splits the incoming LO signal evenly, which is the last part.

Ideally, there would be an IF 90° Hybrid Coupler to bring back the offset IF outputs to get the image rejection. However, due to space and time constraints that portion has been omitted. Below shows the a concept of the layout including all the major components.

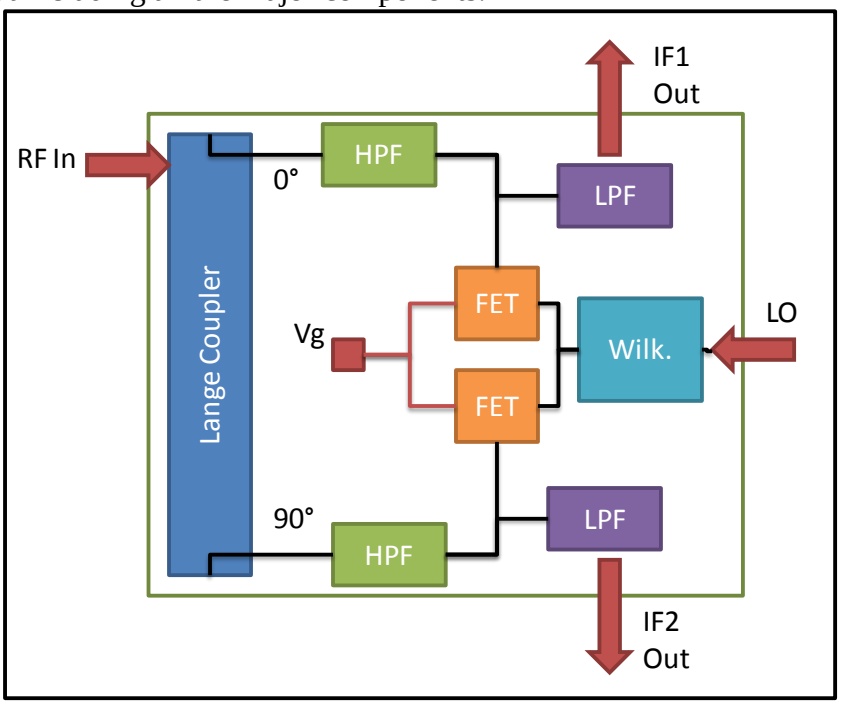


Figure 2: Concept of Layout

The 90° Hybrid Coupler can be implemented in a couple different ways. The first and most familiar one is an a branchline coupler. A branchline can be done with distributive elements (transmission line) or lumped elements (inductors and capacitors to mimic a transmission line).

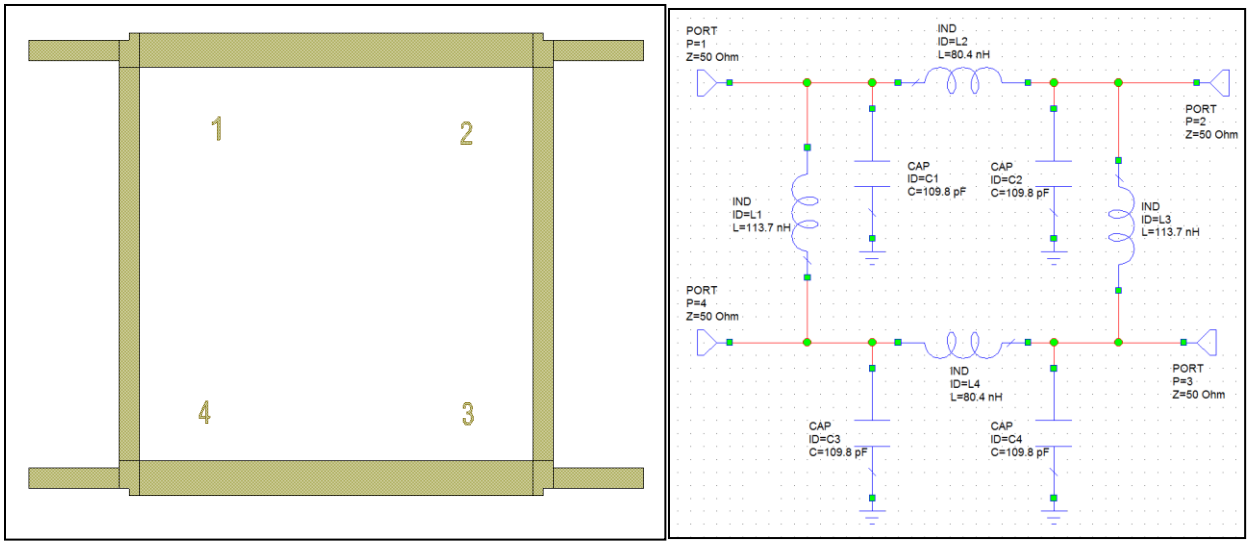


Figure 3: Two different implementations of a branchline coupler

But both of these can be quite large and take up valuable space. So the implementation that I chose was a Lange coupler, which is essentially a coupled line filter that has multiple lines close enough to each other that causing coupling to occur (giving the even split) and is long enough to give a phase offset of 90° (see figure 4).

Figure 4: Lange Coupler

For the mixer I could have used something very similar to the branchline with diodes on the output to create a diode mixer, but again that would have taken quite a bit of space. I went with an idea that was suggested to me where I use a FET but I run it close to pinchoff. The mixing actually happens on the drain side as the gate gets pulsed with the LO signal. Thus the RF comes in and the IF goes out on the drain (see figure 5 for a DC schematic view or figure 1 for a conceptual view). The High Pass Filter (HPF) was designed with a cutoff frequency of 20GHz, while the Low Pass Filter (LPF) was designed with a cutoff frequency of 4GHz. On the HPF the design frequency doesn't really matter, but on the LPF I used the 4GHz because it allowed some of the components to be smaller which made it easier to create the required elements.

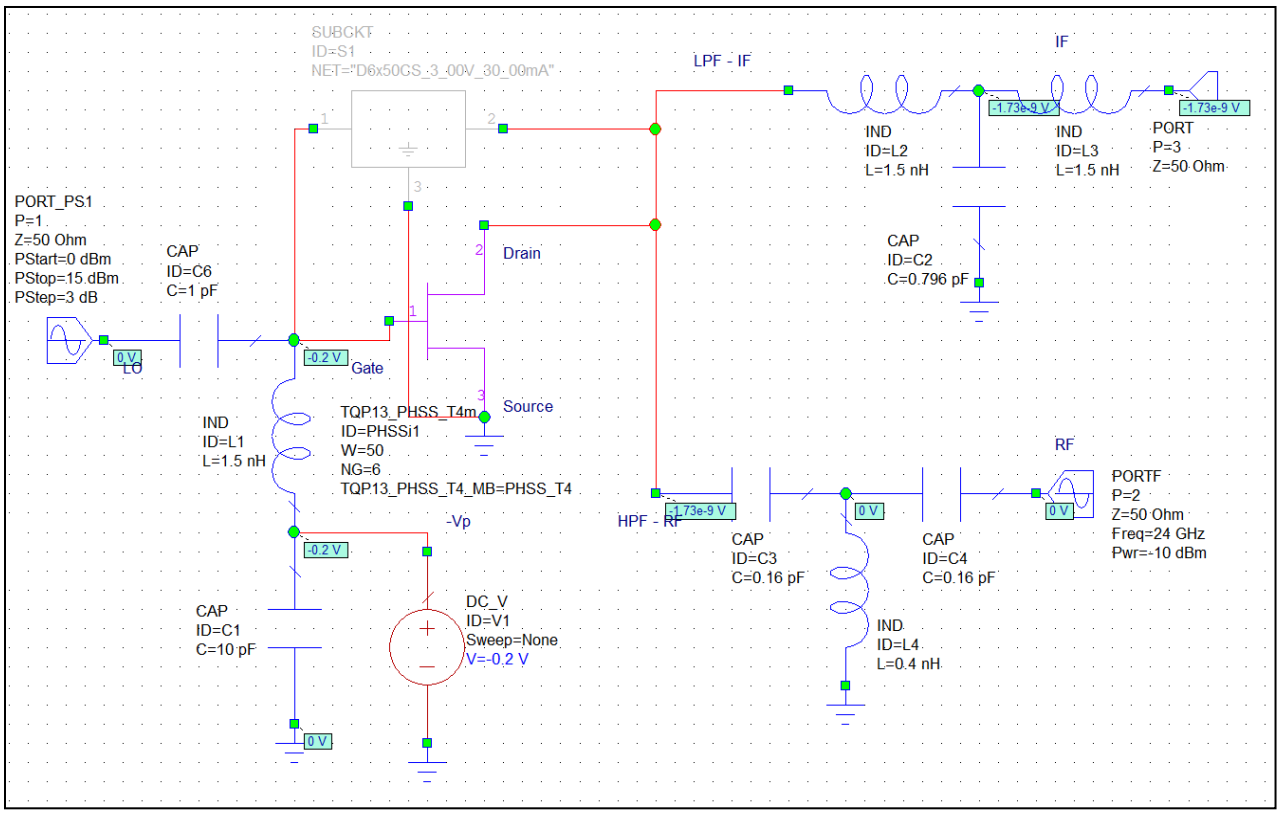


Figure 5: Schematic for an Ideal Resistive FET Mixer

I went with the Wilkinson Coupler as a way to divide the LO into two equal amplitude and phase paths for the mixer. I am familiar with the Wilkinson since we had used it in a previous class with Professor John Penn. The Wilkinson was easy to implement as a distributed element because of the design frequency.

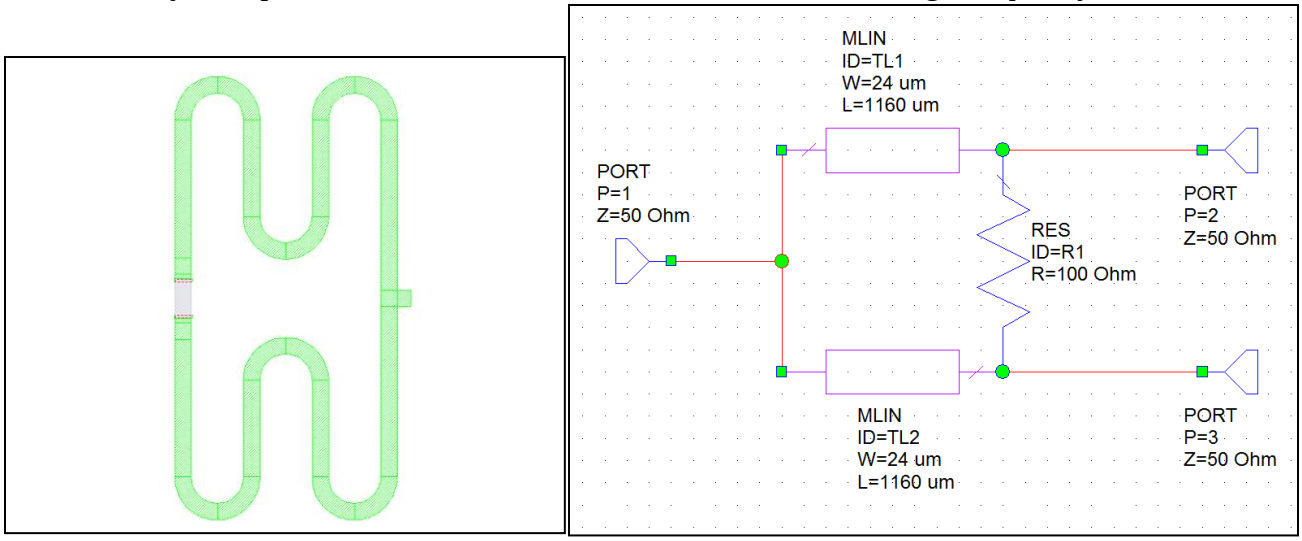


Figure 6: Layout view of Wilkinson Coupler and circuit view of an Ideal Wilkinson

Simulations

90° Hybrid Coupler

The Lange coupler had a very even split on the output within 0.01dB and the phase difference was about 91.7° (see figure 7). It is more important to have the outputs be more balanced than the phase to be balanced so this is ok.

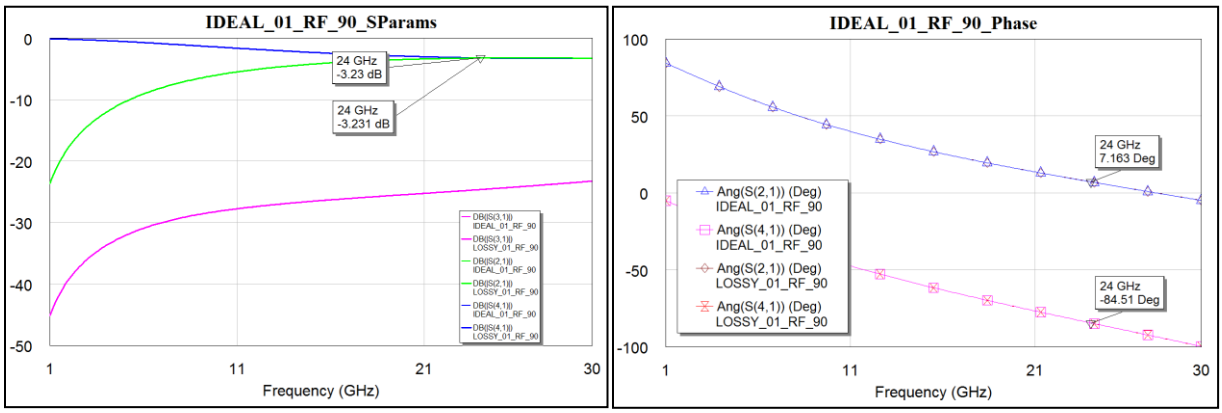


Figure 7: Plots showing Ideal performance vs TriQuint (Lossy) elements

Resistive FET Mixer

The Resistive FET mixer was an interesting design and had a couple of design quarks. One of which was for the Low Pass Filter (LPF). The pi network that was designed for it ideally led to great results, however upon using TriQuint element the high end of the LPF started to kick up. The solution was a simple one, but took quite a bit of time to figure out; each leg going to ground needed its own via. For some reason MWO showed the kick up that you can see in figure 8 when both legs were connected to the same ground. There is still a little bit of kick up, but not as strong as it was before.

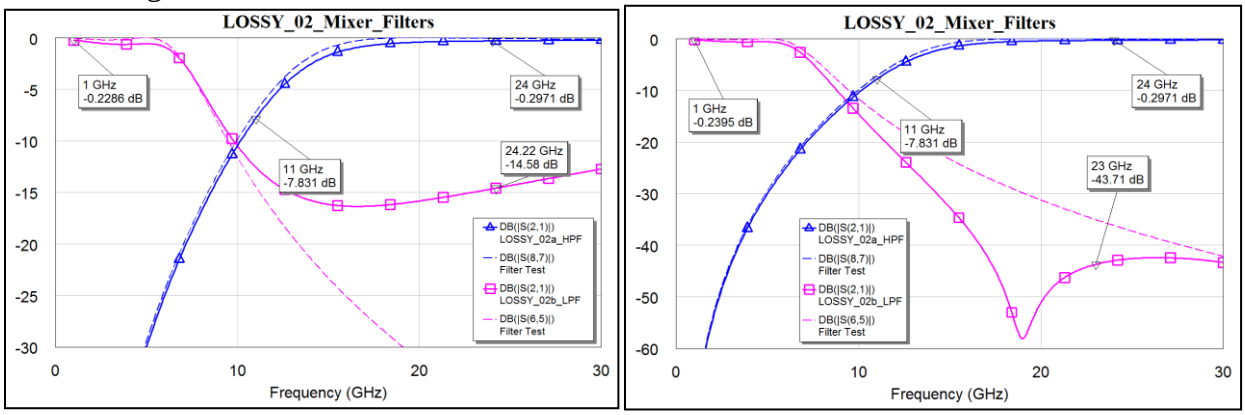


Figure 8: Single via results compared to Individual via results

The High Pass Filter (HPF) simulated exactly like the ideal circuit. When everything was put together for the mixer it performed reasonably as compared to the ideal version. There was about 4dB of loss through it, but the LO leakage was reduced by about 10dB (see figure 9).

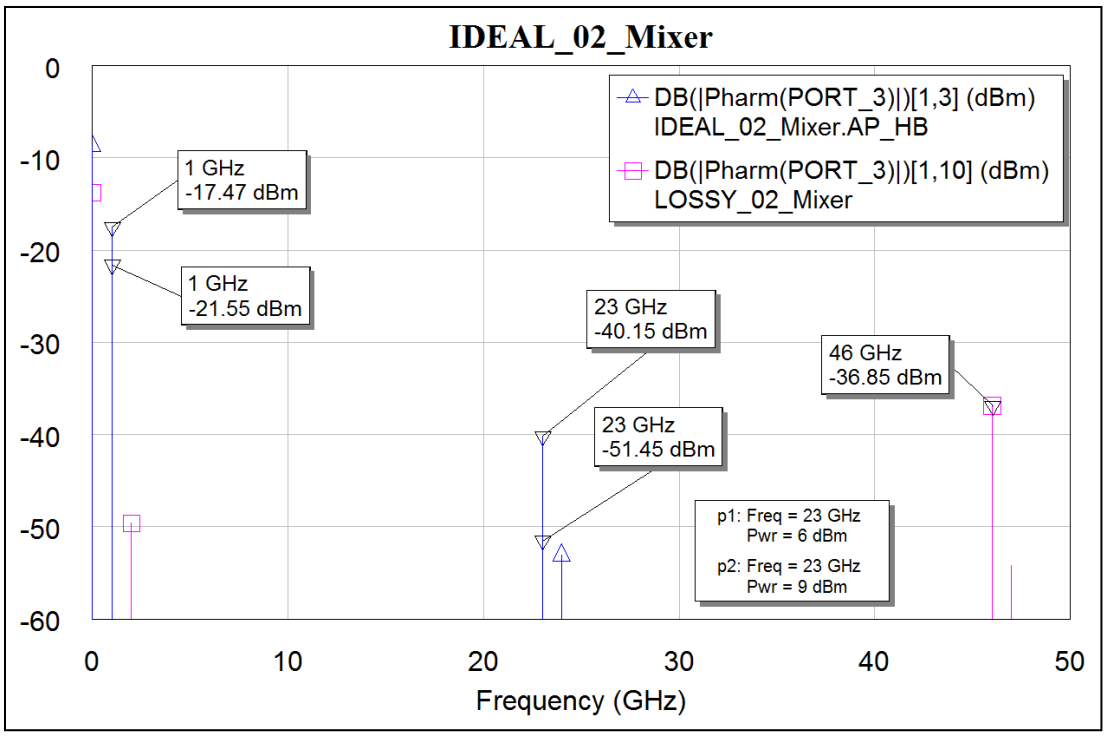


Figure 9: Mixer results, Ideal vs Lossy

Wilkinson Coupler for LO

The Wilkinson Coupler was very straight forward and the results match the ideal version of it.

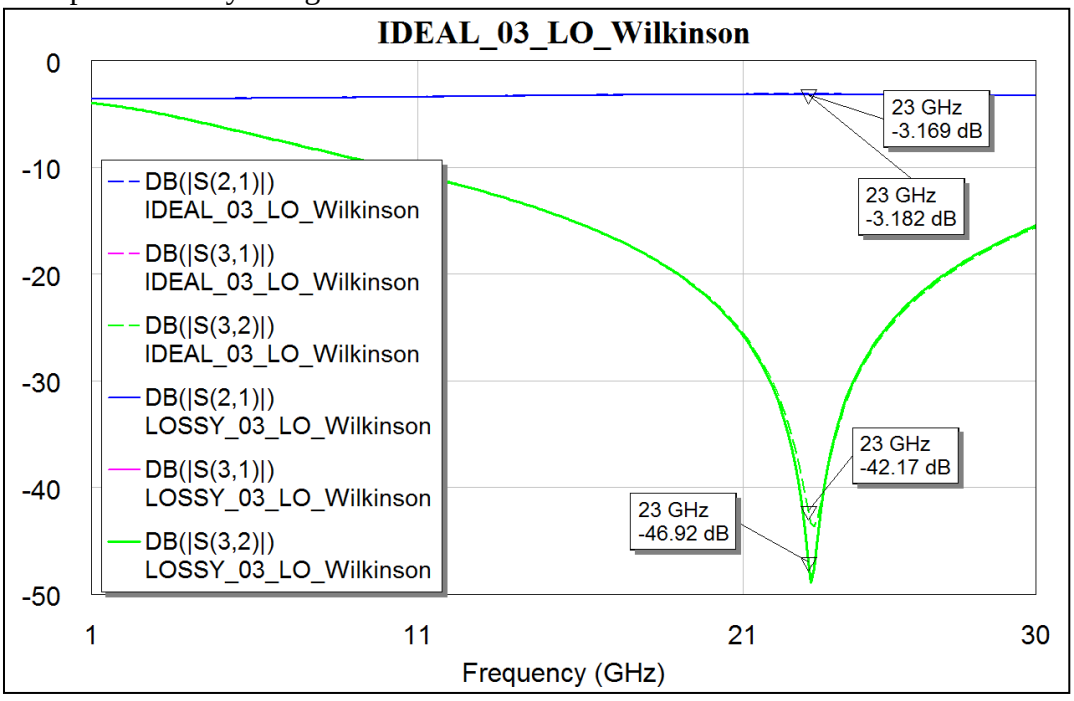


Figure 10: Wilkinson Coupler results, Ideal vs Lossy

Full Circuit

When all the elements were put together the overall circuit seemed to perform quite well as compared to the Ideal version (see figure 11).

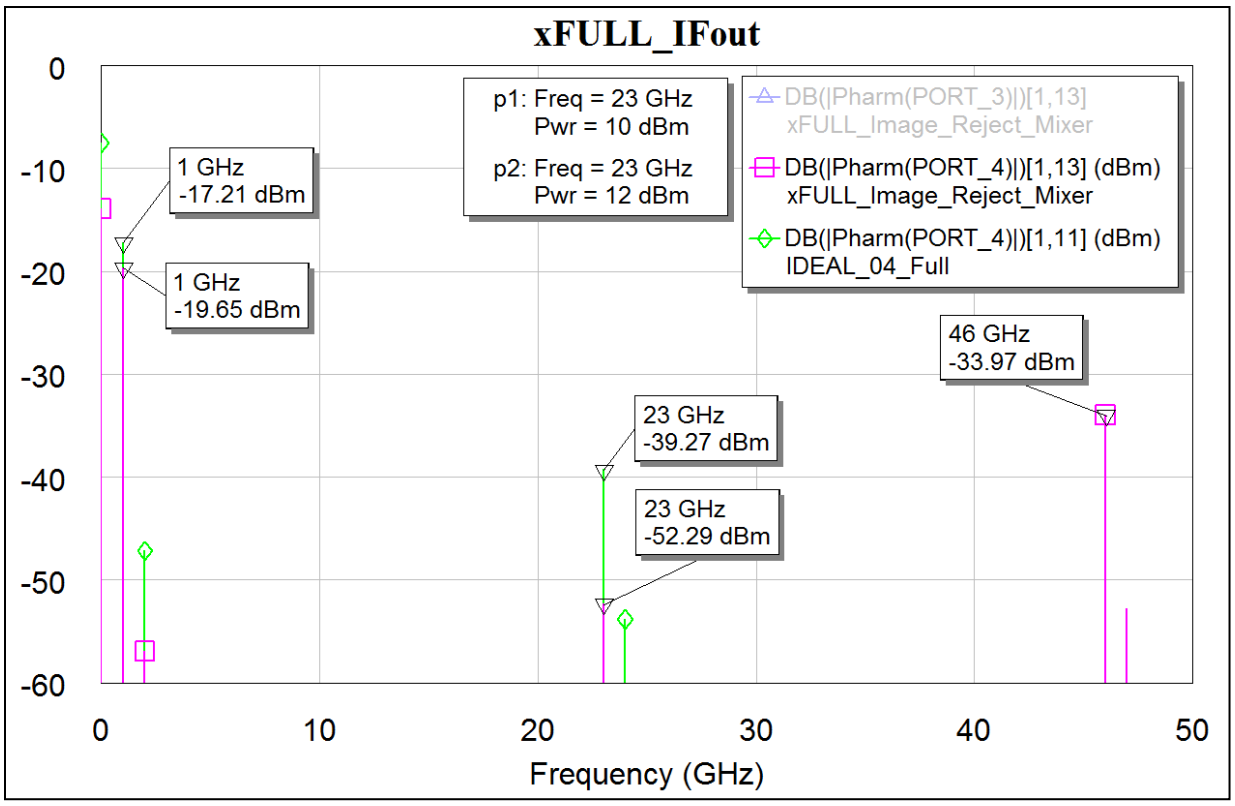


Figure 11: Performance of full circuit, Lossy vs Ideal

There was another thing that made the design more interesting. Despite the symmetry in the mixers there was a 3dB difference in two Intermediate Frequency (IF) outputs and the convergence loss (see figure 12). The good thing was that difference was only caused by the placement of the 50Ω termination for the Lange Coupler, which was corrected for during the Design Rule Checks.

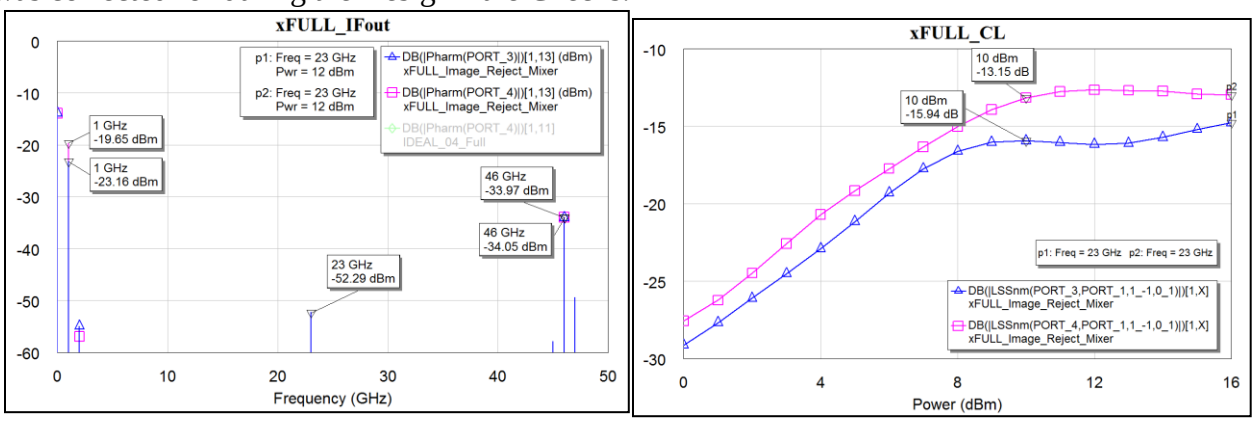


Figure 12: Performance of full circuit and convergence loss, IF output 1 vs IF output 2

Overall, the performance of the Image Reject Mixer seems to be on par with the results of the Ideal version. We will know how the actual results compare once we get the chips fabricated so we can test them.

Schematic

One additional challenge to this project was to get the circuit to fit within a 60 x 60 mil layout. Using some creative approaches this was possible. The figure below shows the RF Schematic.

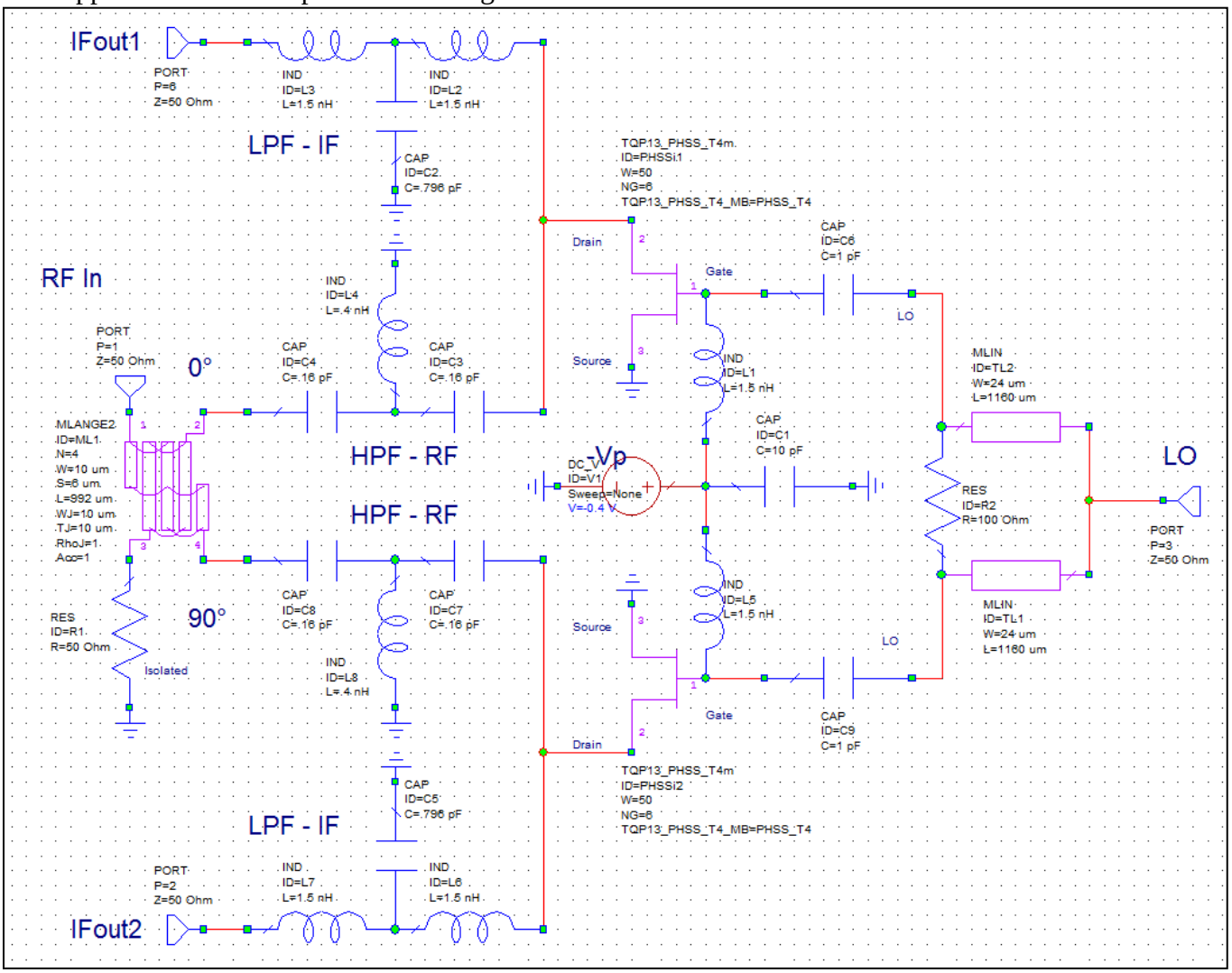


Figure 13: RF Schematic of Image Reject Filter

Below is the DC Schematic of the circuit. In the DC circuit all inductor have gone to shorts and most capacitors have gone to opens (the few capacitors left allow for the circuit to remain complete). The gate voltage does not travel anywhere else in the circuit, besides the gate of the FET.

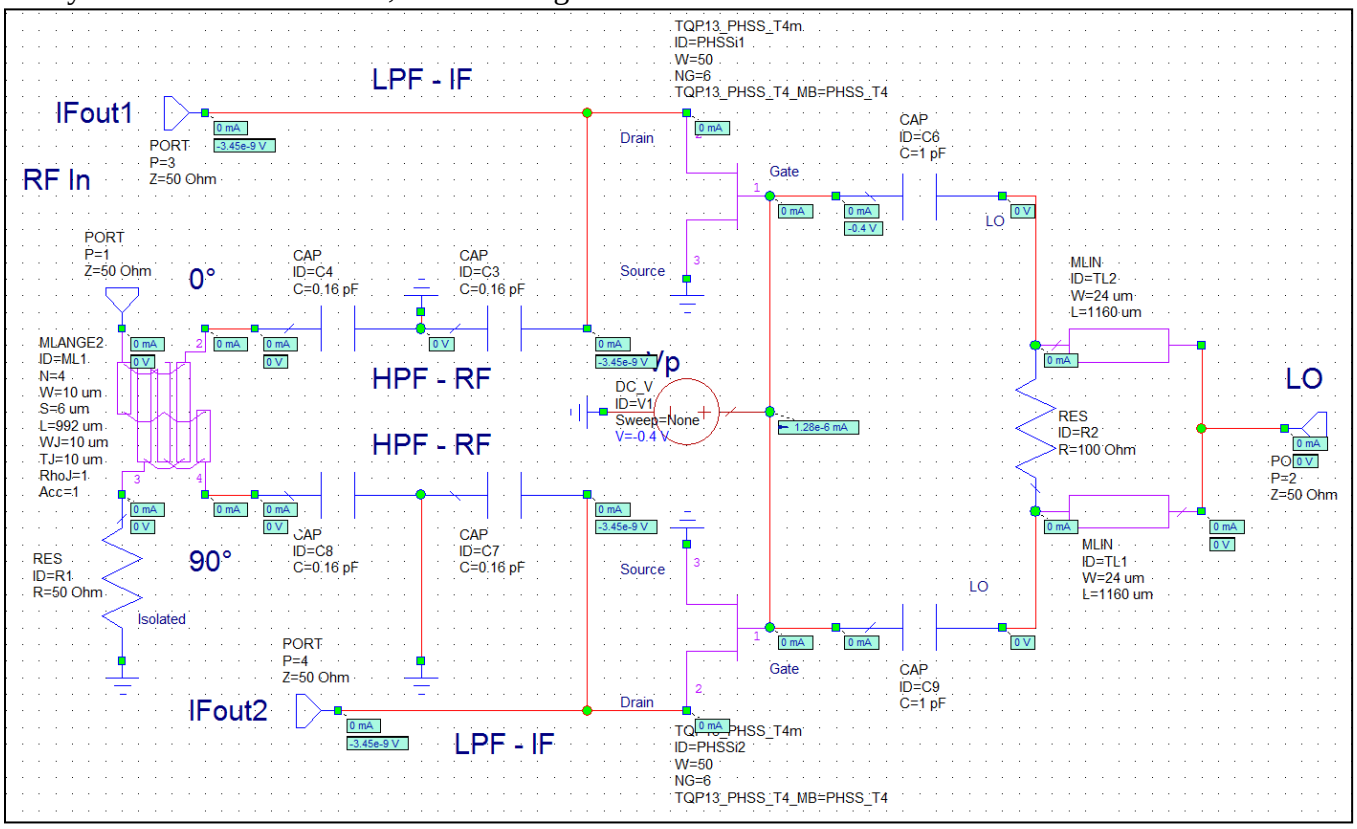


Figure 14: DC Schematic of Image Reject Filter

Layout

Below is the layout for the Image Reject Mixer before the DRC checks.

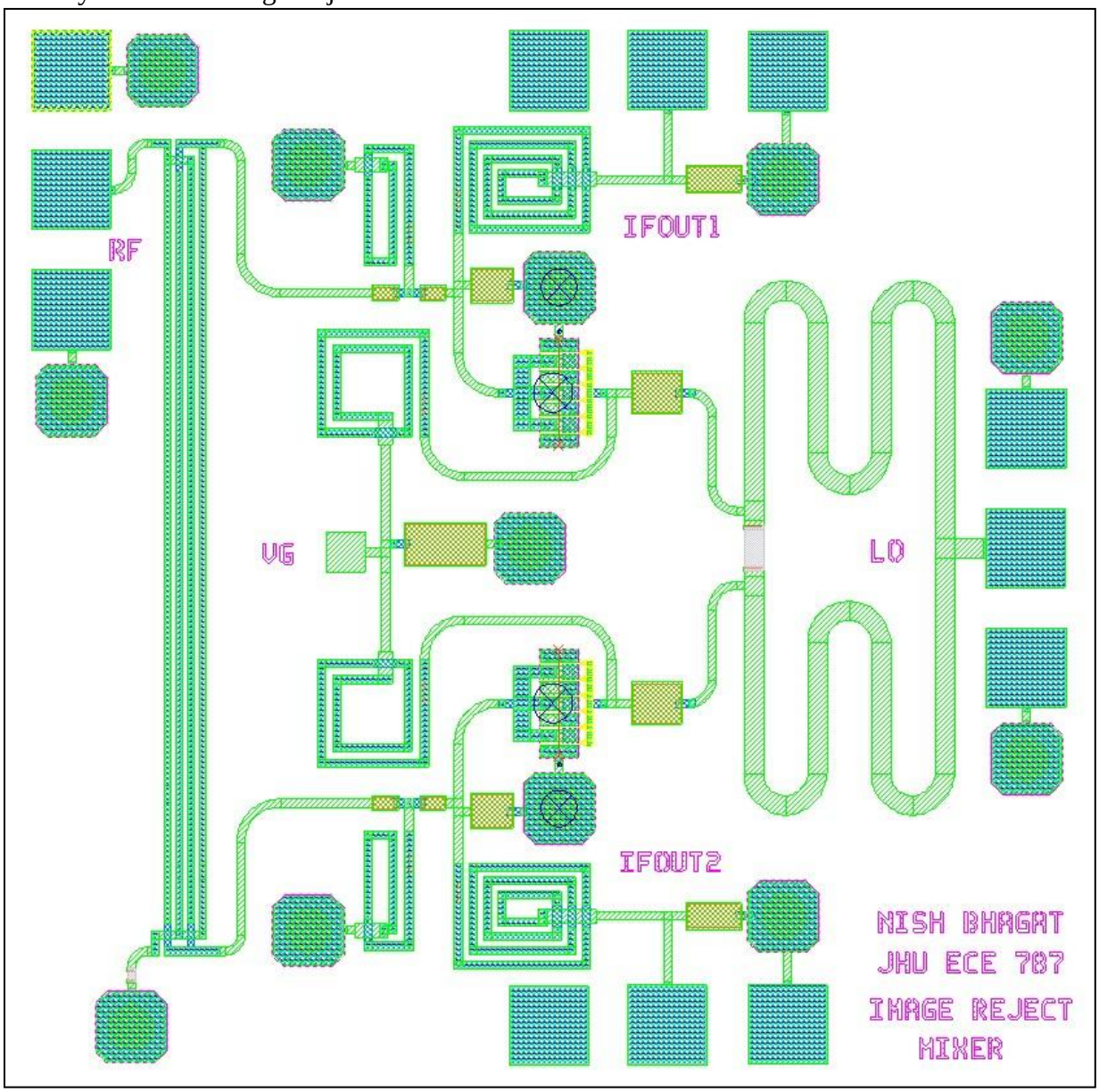


Figure 15: Image Reject Mixer Layout

Test Plan

Once the circuit gets fabricated by TriQuint the following would be the order of operation to test it:

1. Put a Ground-Signal-Ground (GSG) Probe on the RF input and connect it to a signal generator set up at 24GHz and power at -7dB of power.
2. Put a GSG Probe on the LO input (across from the RF Input) and connect it to a signal generator set up at 23GHz and power at +12dB of power.
3. Put a GSG Probe on the first (top) IF output and connect it to a spectrum analyzer.
4. Put the last GSG Probe on the second (bottom) IF output and leave it unconnected until you are ready to measure it on the spectrum analyzer.
5. Finally, place a Voltage Probe on the Vg pad and set the voltage at -0.4V.
6. Check both IF outputs on the spectrum analyzer to see what the levels are at for 1GHz.
7. Sweep the voltage from 0V to -0.8V in 0.1V steps to find the optimum voltage level (**Table 1**).
8. Now you can sweep the LO from 0dB to +14dB in 1dB increments to see the effect on the IF (**Table 2**).
9. Putting the LO at +12dB again, sweep the RF from -60dB to 0dB in 5dB steps to get results at IF for a varying RF input (**Table 3**).
10. OPTIONAL: Try to swap the LO and RF signals to see if the circuit still works.

Vg (V)	IFout1 (dB)	IFout2 (dB)
0		
-0.1		
-0.2		
-0.3		
-0.4		
-0.5		
-0.6		
-0.7		
-0.8		

Table 1: Varying Vg

LO (dB)	IFout1 (dB)	IFout2 (dB)
0		
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		

Table 2: Varying LO

RF (dB)	IFout1 (dB)	IFout2 (dB)
-60		
-55		
-50		
-45		
-40		
-35		
-30		
-25		
-20		
-15		
-10		
-5		
0		

Table 3: Varying RF

Conclusion

This was a fun project to work on and design. There are still adjustments and fine tuning that can still happen to slightly improve performance and save additional space. However, this would require more time and would need to be looked over by someone with industry experience. I would have loved to add the final IF 90° Hybrid to make this into the full Image Reject Mixer, but for now we will have to assume that will happen off chip. The chips should be fabricated early next year (2014) and tested in March of the same year. The performance and design goals for this project have been roughly met. Running an electromagnetic simulation of this circuit would reveal insight into the placement of the routes and their effects. A second iteration of this design would include the final stage and be designed to be more broadband. An interesting idea could be to add a Voltage Controlled Oscillator (VCO) to the design that could switch from 23GHz to 25GHz, which would allow the mixer to do low/high side injection. Or allow the IF to be at something other than 1GHz.

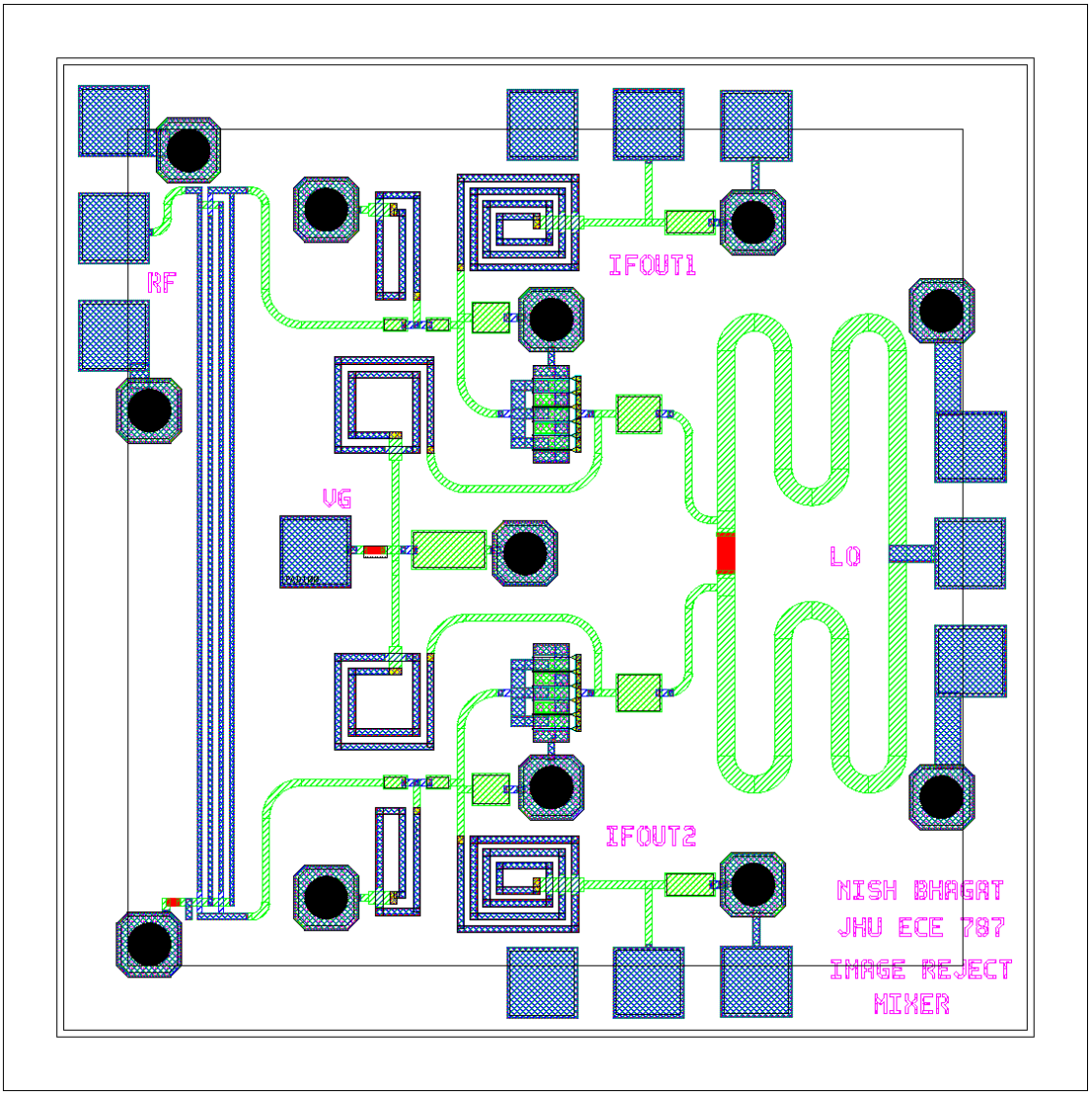
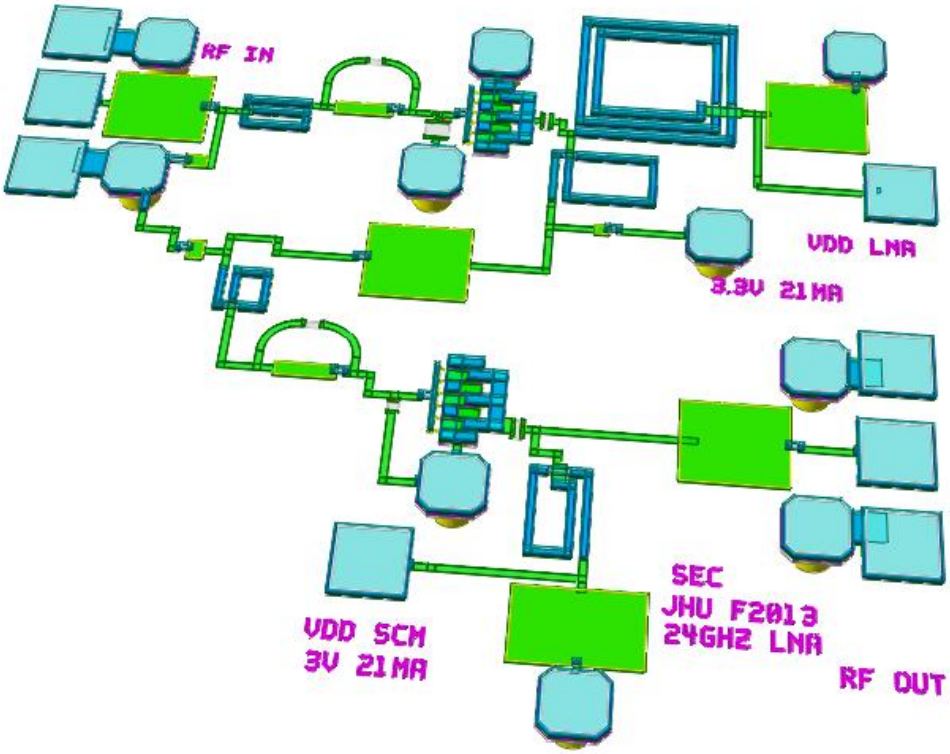


Figure 16: Final Layout after DRC checks

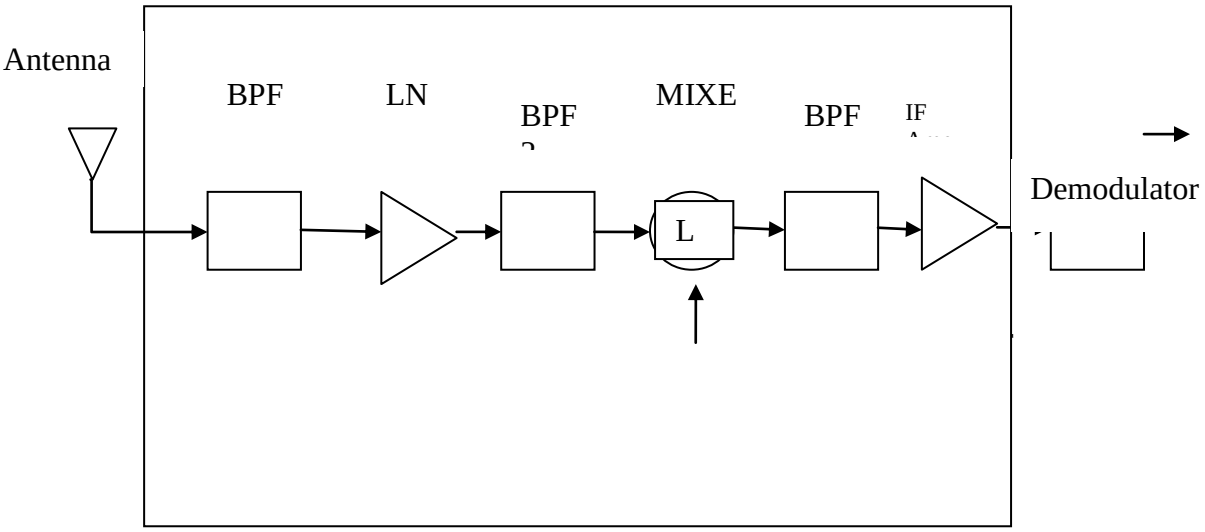


Shaynee Contee
December 11, 2013
EN.525.787 FA13 MMIC Design
Professor Penn – Dr. Thompson

Design of a 24 GHz Low Noise Amplifier

Abstract
This paper describes the design of a two-stage low noise amplifier operating at 24 GHz. The design utilizes TriQuint's TQP13 process and was simulated primarily using AWR's Microwave Office. Agilent's ADS was also used for simulations. The final layout is to be processed on a 54 by 54 mil GaAs substrate that is 85 microns thick.

Introduction
Low noise amplifiers play an important role in a communication system and are usually found in a receiver. Figure 1 shows an example block diagram of a receiver. An example of a communication system is shown in Figure 2 that displays the desired responses for each component of the system. The desired characteristic of a low noise amplifier (LNA) is that it amplifies a weak input signal while minimizing its' noise contribution to the system. The design of an LNA requires high gain, low noise figure, unconditional stability and good input and output matching with a minimal output current. When designing a LNA there is an expected trade-off among the gain, noise figure and stability. This trade-off or compromise exists because it's difficult to meet these requirements simultaneously.



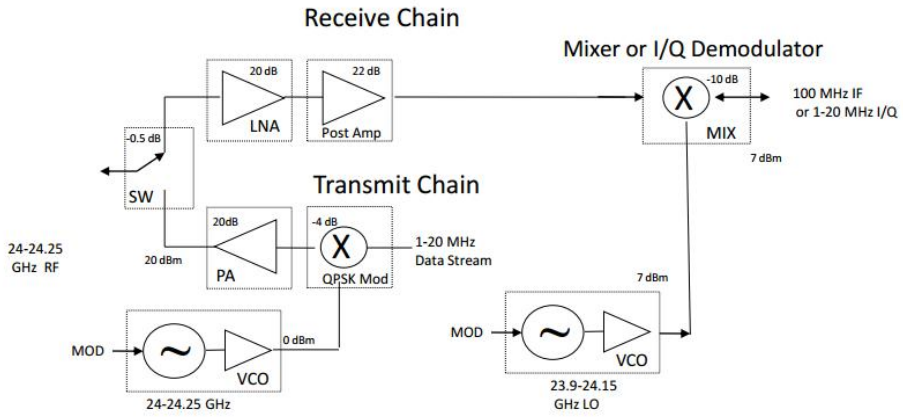


Figure 2 24 – 24.25 GHz ISM bands Communication System

Design Specifications
Frequency: 24GHz
Current: ≤ 30mA
Gain: 20dB
Return Loss: < -10dB for S11, < -15dB for S22
Noise Figure: < 3

Design Approach
To begin designing the LNA, the small signal parameters of the 6x50 µm pHEMT (Vds=3V, Ids = 30mA) are used to stabilize the transistor at 24 GHz. Figure 3 shows the final schematic used to stabilize the transistor. A shunt RC combination was placed in series at the input of the transistor to improve stability at lower frequencies. The plots of the stability and noise figure of the stabilized pHEMT are shown in Figures 4 and 5 respectively. To determine the input match for the LNA, the noise and gain circles of the stabilized pHEMT were used (these were obtained using Agilent's ADS).

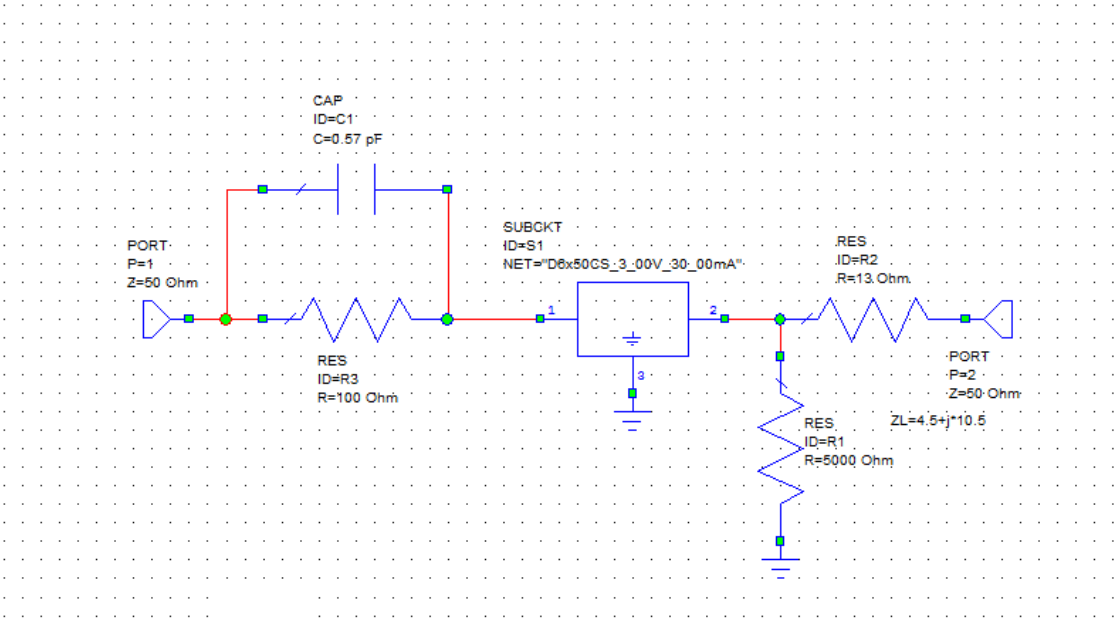


Figure 3 Circuit used to stabilize pHEMT

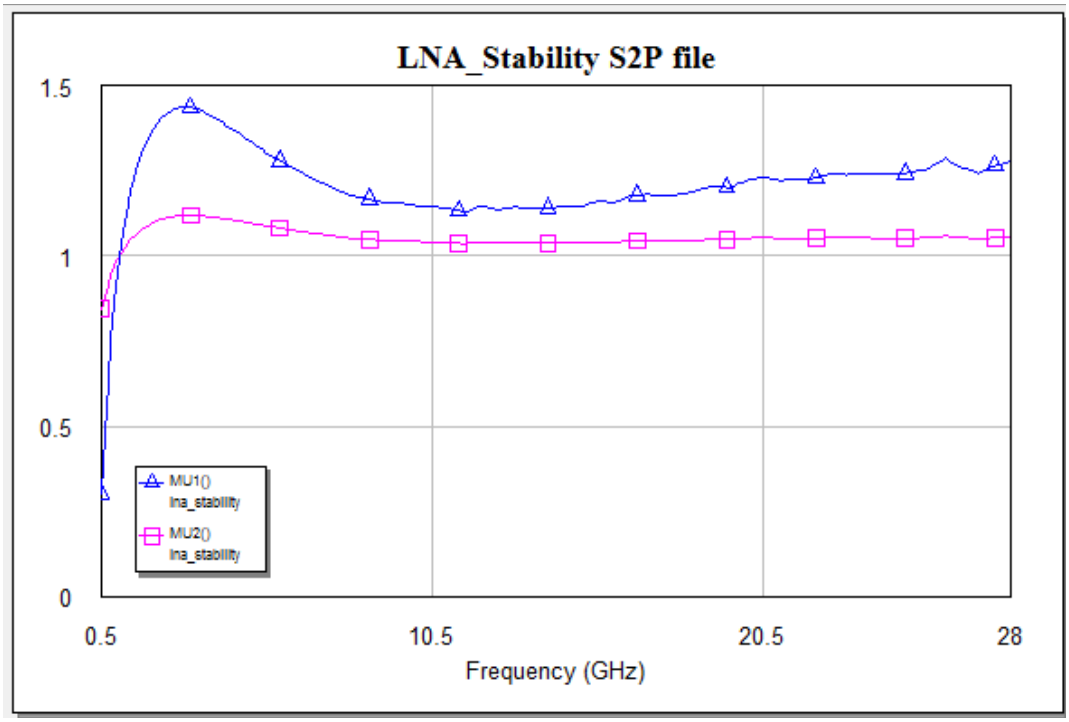


Figure 4 Stability of stable pHEMT

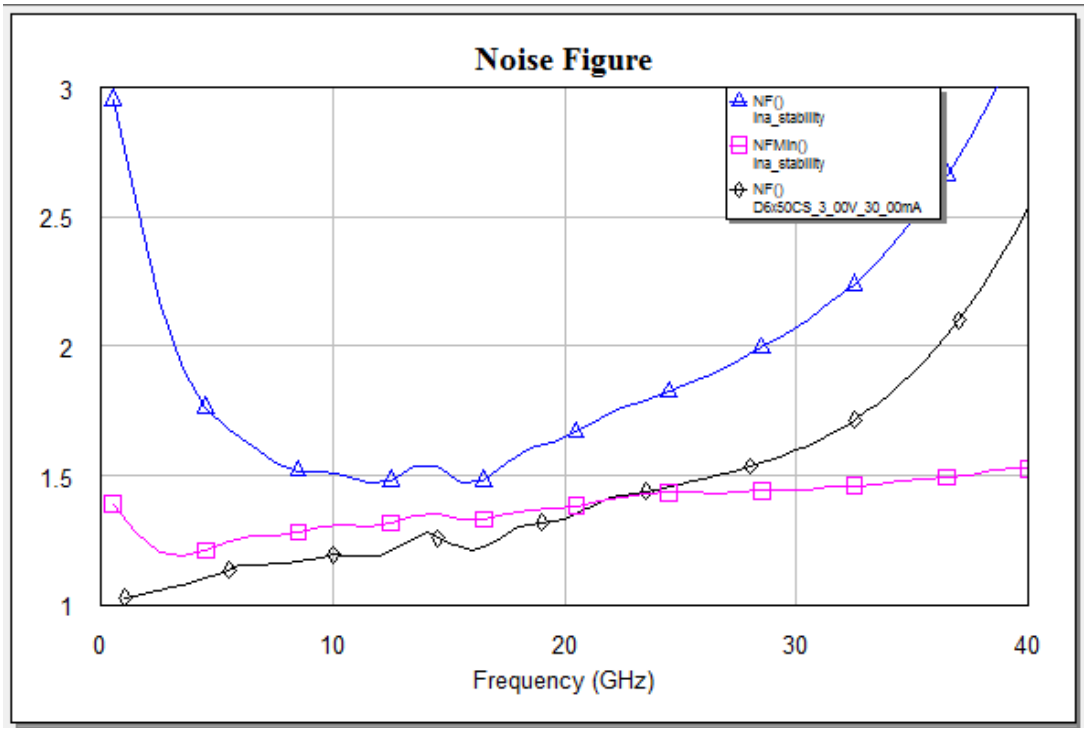


Figure 5 Noise Figure of Stabilized pHEMT

A point intersecting the gain circle of 8dB and the noise circle of 1.7dB was used to determine the input matching network. The impedance of this point is 6.27+ j15.232 Ω. The resulting circuit (input match and stable pHEMT) was used to obtain the output matching network. The conjugate of this circuit's S22 was used to design the output match (S22* = 25.17+ j16.48). Figure 6 shows the resulting low noise amplifier using the S-parameter data at a bias of Vds =3V and Ids = 30mA.

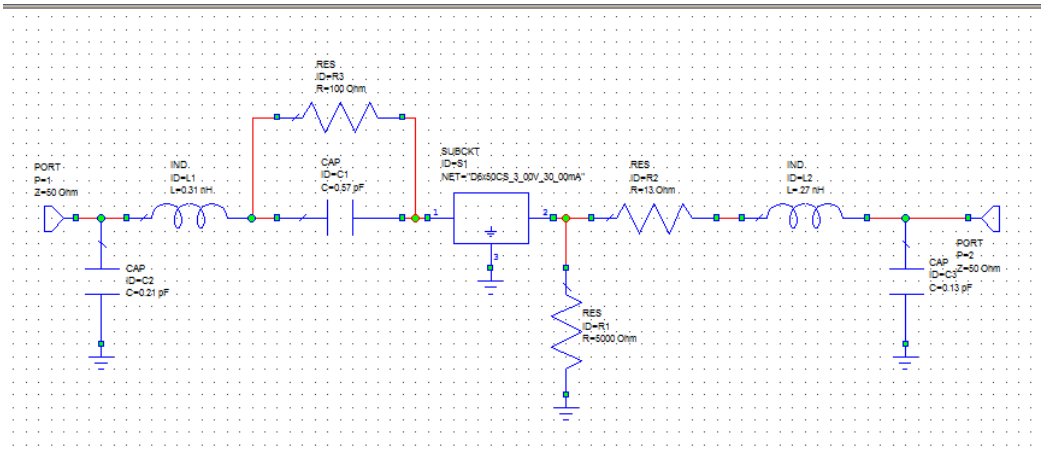


Figure 6 Low Noise Amplifier

Because the gain of this LNA was low (6.9 dB), a simultaneously conjugate match (SCM) amplifier was designed as a second stage to increase the gain. The non-linear low noise amplifier was later implemented using the TOM3 model of the transistor that is a part of the TQOR_TQP13 library. The SCM amplifier also uses a 6x50 µm pHEMT. Figure 7 shows the final schematic for the SCM amplifier that has a gain of 7.3dB. The impedances used to obtain the input and output matching networks for the SCM amplifier are 3.845 + j21.175Ω and 17.318 +j24.29Ω respectively. A decoupling capacitor (6pF) was placed between the LNA and SCM amplifiers. It was expected that the gain would have been closer to 13dB, but as the ideal circuit elements were changed to TriQuint elements using an iterative tuning process the resulting gain at 24GHz is 10.9dB. Figure 8 shows the circuit using TriQuint elements and Figure 9 shows a plot of the gain and return loss at ports one and two. Figure 10 shows a plot of the noise figure in comparison with the noise measurements of the transistor at the bias of 3V, 30mA (brown trace).

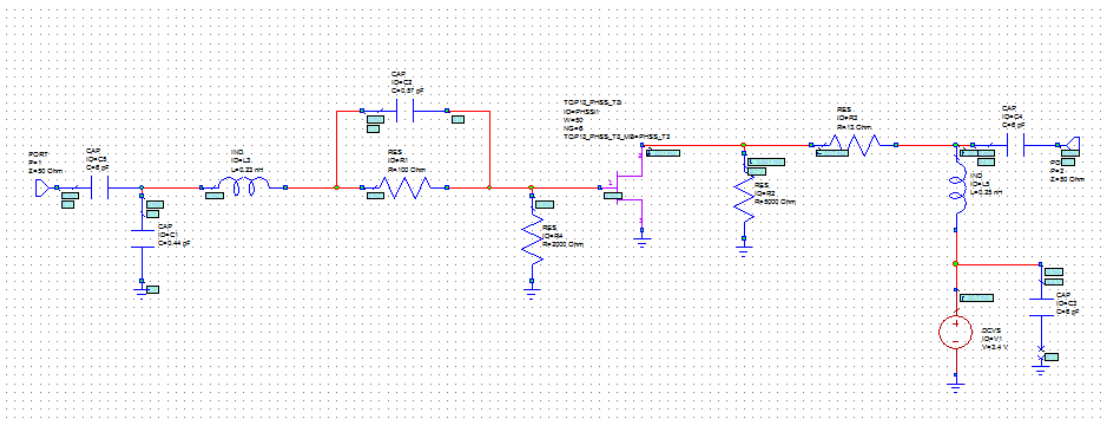


Figure 7 Simultaneously Conjugate Matched Amplifier

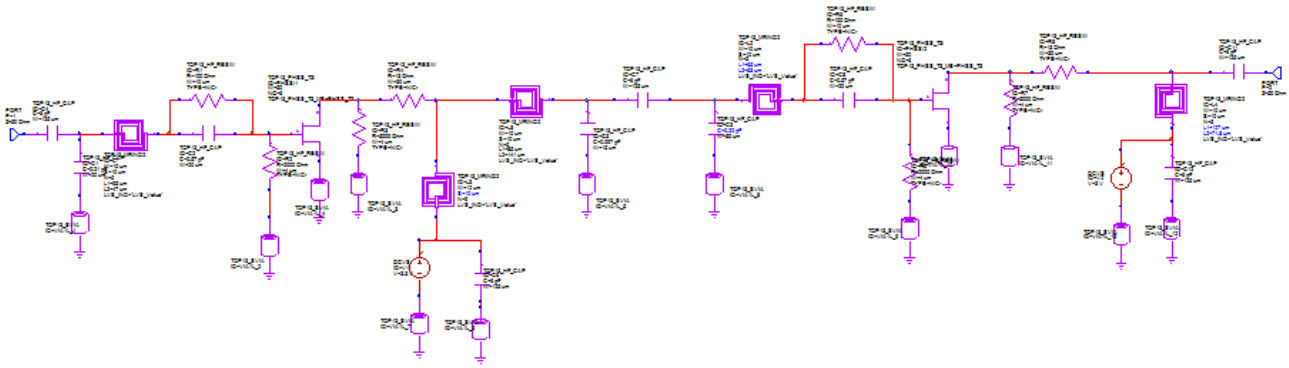


Figure 8 LNA cascaded with a SCM amplifier using TriQuint elements

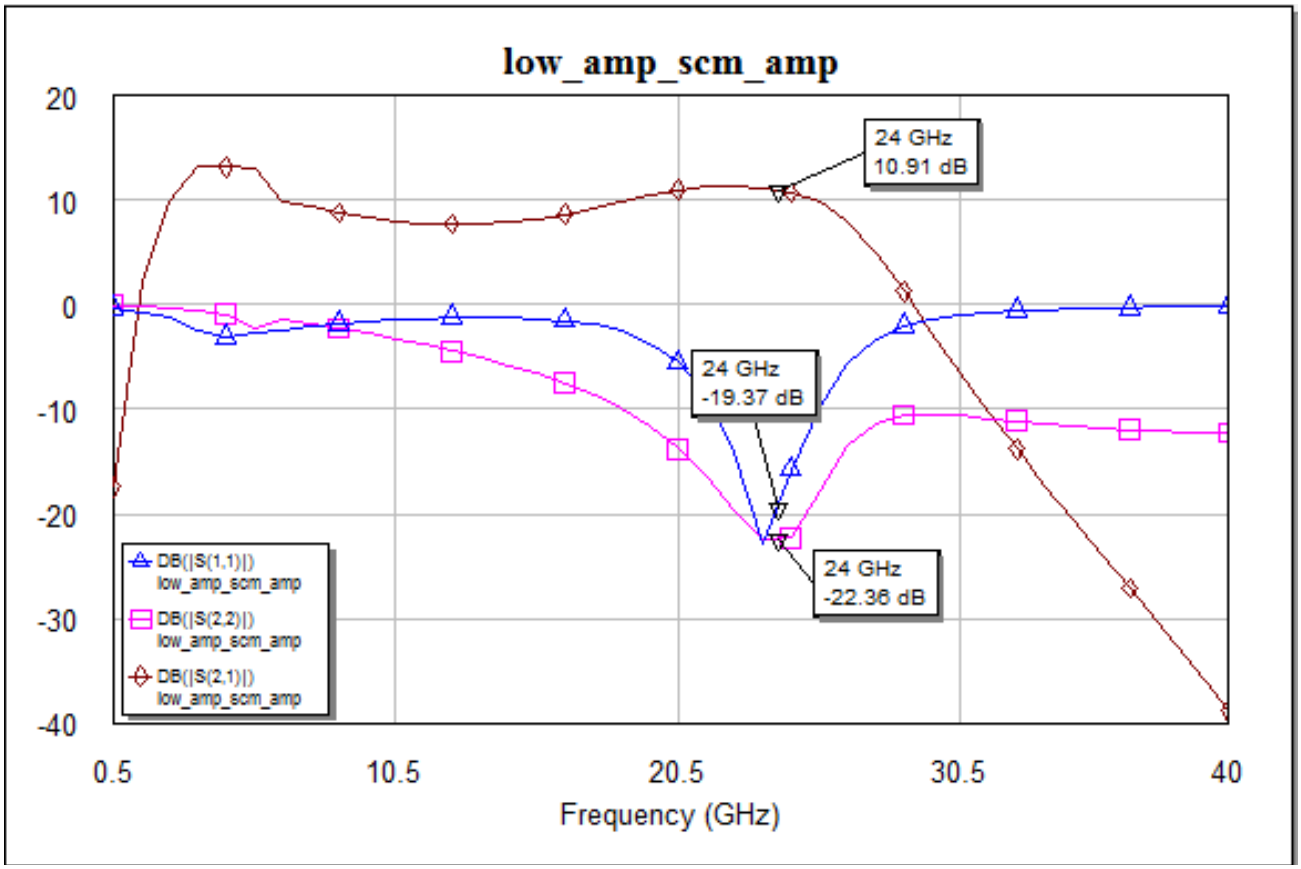


Figure 9 S-parameters of LNA cascaded with a SCM amplifier using TriQuint elements

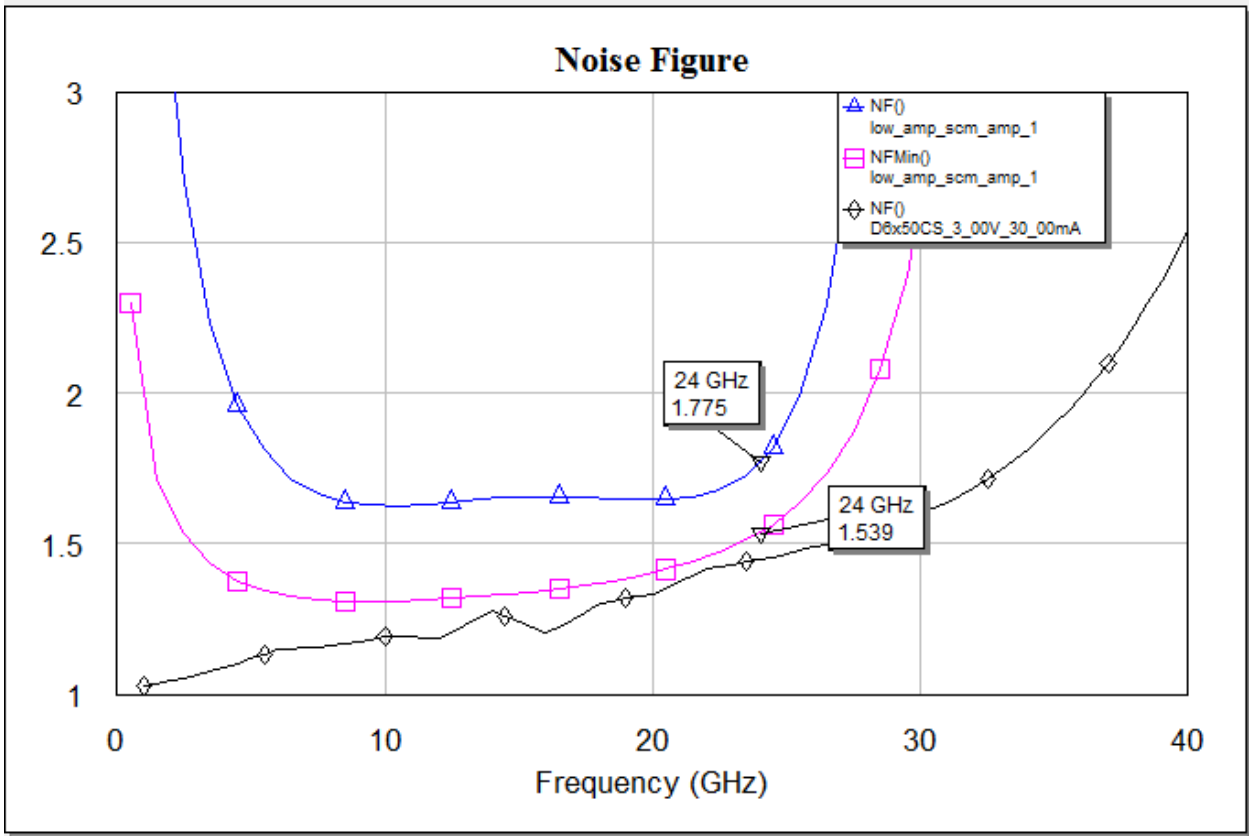


Figure 10 Noise Figure of LNA cascaded with a SCM amplifier using TriQuint elements

Simulations

Biasing for the LNA includes a large resistor (2kΩ) at the gate so that Vgs = 0V. The drain of the LNA is biased at Vdd=3.3V with an expected 21.5mA at the drain. The gate of the pHEMT used for the SCM amplifier is also biased using a large resistor (2kΩ) at the gate so that Vgs = 0V. The drain of the SCM amplifier is biased at Vdd=3V with an expected 20mA at the drain. A DC annotation was performed on the final circuit using the previously mentioned values of Vdd. The intent was to get a current of 30mA at the drain of each transistor; however larger values of Vdd were not helpful in reaching this goal due to the series resistor that is a part of the stability circuit. Figure 10 shows the schematic of the two-stage amplifier circuit that was used for layout; note that the shunt 5kΩ resistor at the drain of each transistor has been removed.

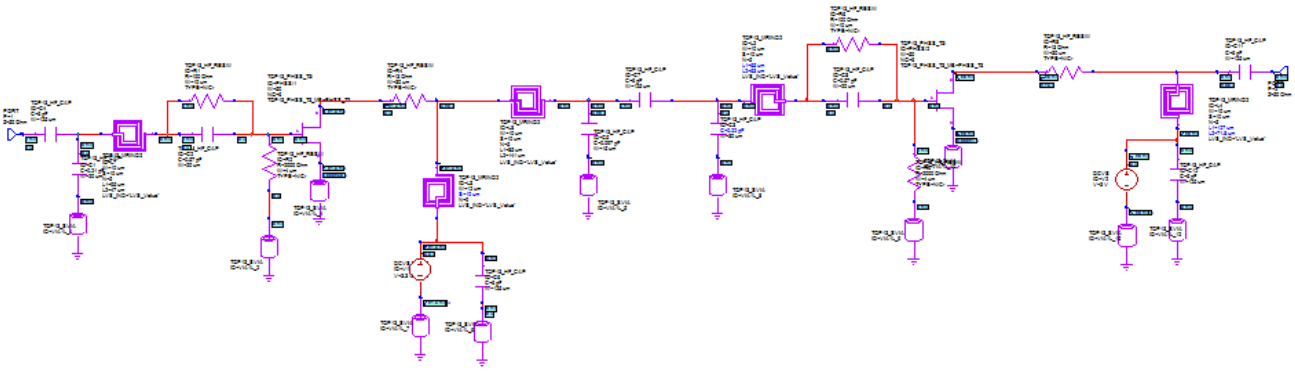


Figure 10 Two-stage Amplifier using TriQuint Elements

The Dynamic Load Line of the amplifier was plotted (Figure 11) and it was observed that the resulting contours extend outside of the IV curves. The IV curves were plotted using the provided S-parameter data for a bias of 3V and 30mA at the drain. The current used to obtain the plot is the drain current of the SCM amplifier. The one dB compression point of the circuit was also simulated. The simulated results plotted in Figure 12 show that an output power of 13.72dBm (0.02W) can be obtained when the input power is 3.772dBm. The output power versus the input power was also plotted and can be seen in Figure 13. This plot shows that the circuit behaves linearly at 24 GHz when the input power is between 1.148 and 8.223 dBm.

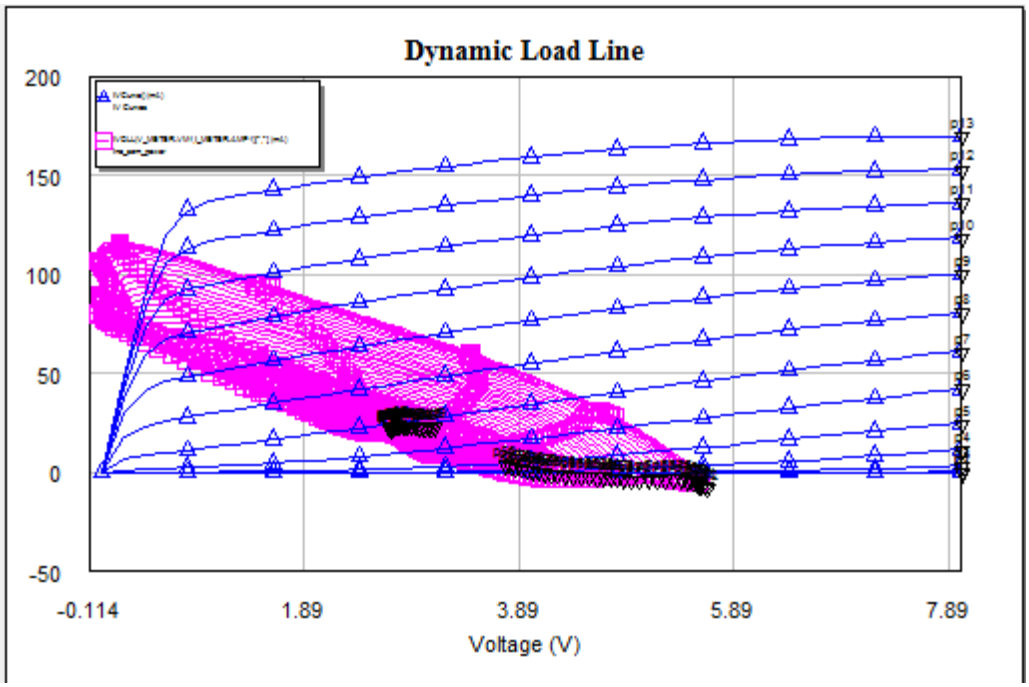


Figure 11 Dynamic Load Line

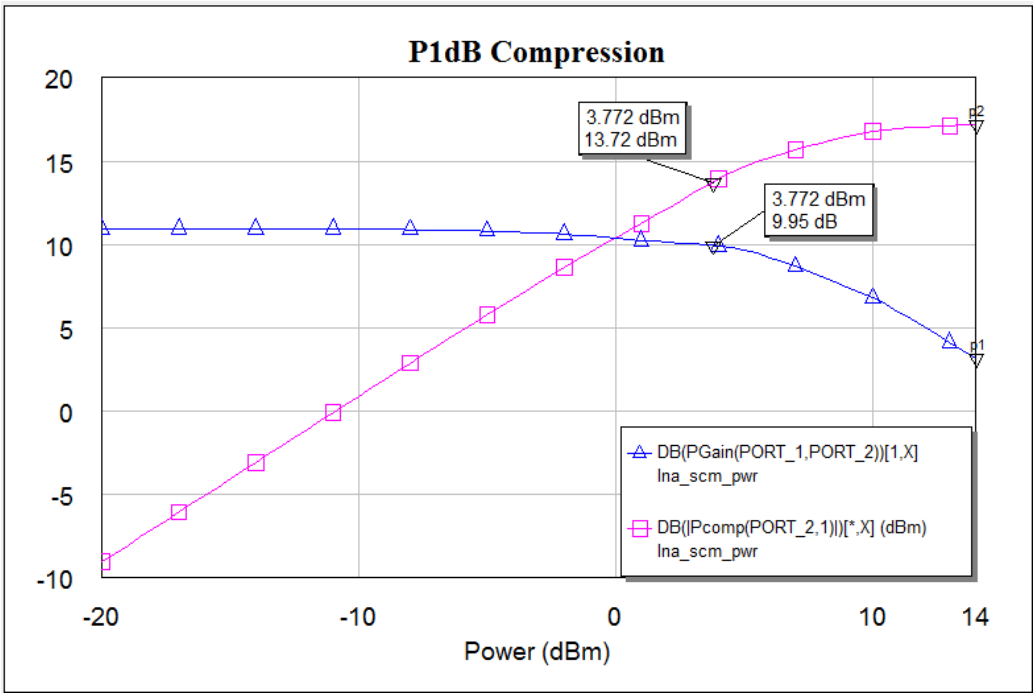


Figure 12 P1dB of LNA

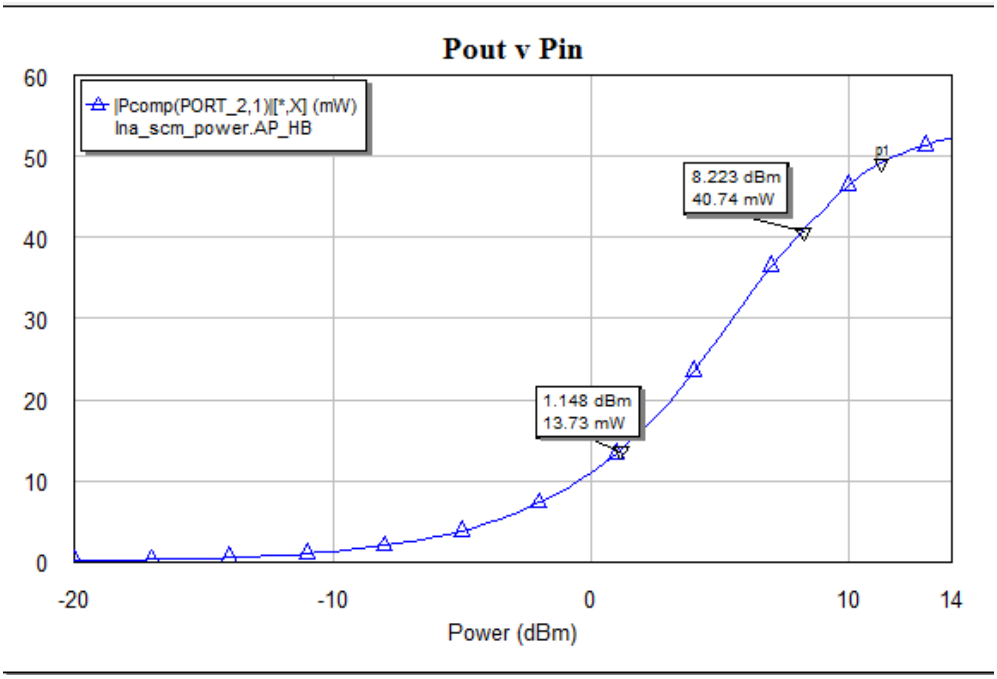


Figure 13 Pout vs Pin of LNA

Schematic

The microstrip components (MLINs, MTEEs and MCURVEs) were added to the circuit in Figure 8 to obtain a final circuit for layout. Preparing the circuit for final layout resulted in a loss of gain and a shift in the return loss as shown in Figure 14. Figure 15 shows that the final circuit is unconditionally stable. Figure 16 shows the simulated noise parameters of the LNA. At 24 GHz, the noise figure is 2.329. Figure 17a shows the final schematic for layout and Figure 17b shows the DC schematic for the same circuit.

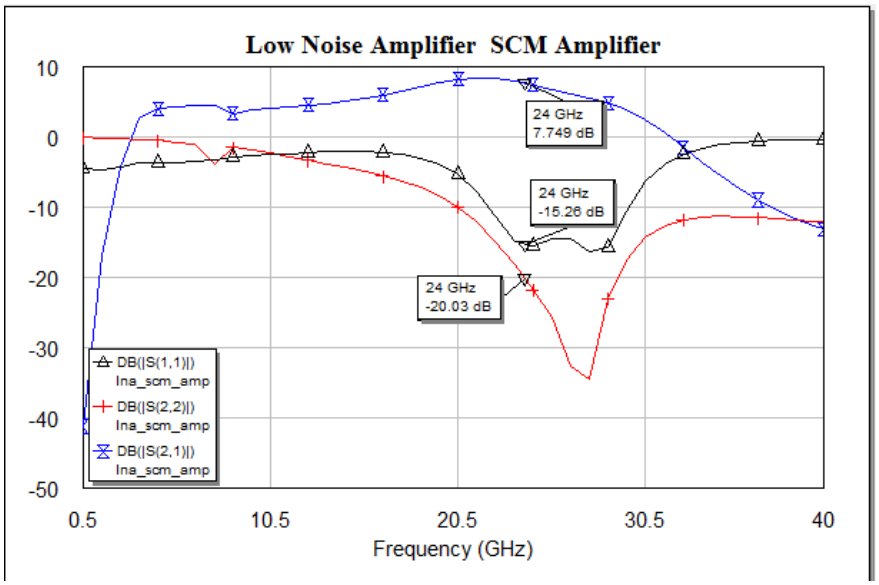


Figure 14 Simulated S-parameters of LNA

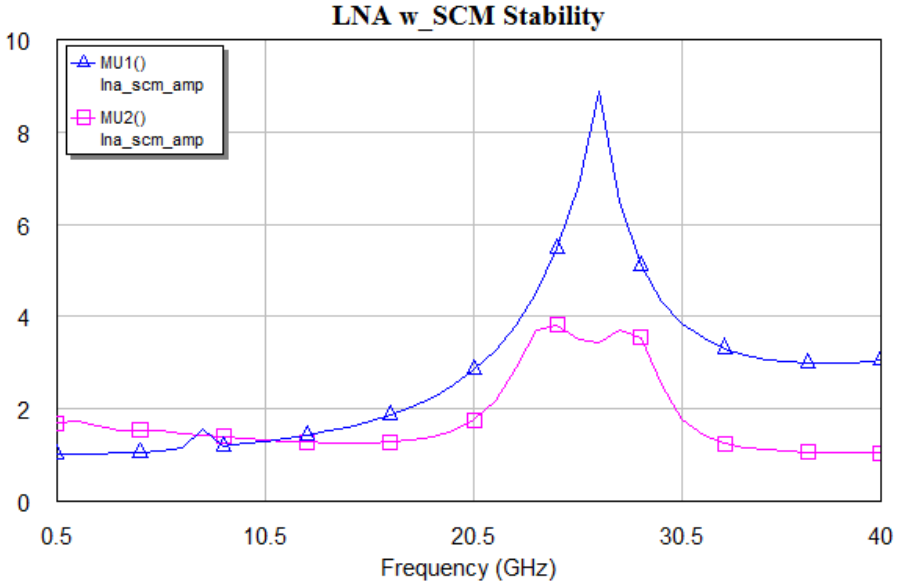


Figure 15 Stability of LNA

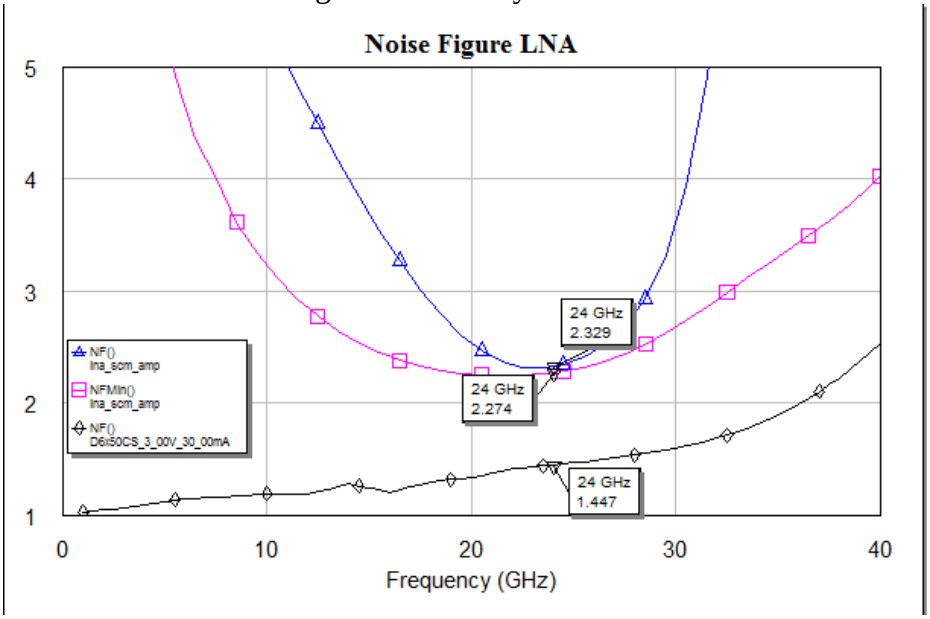


Figure 16 Noise Figure of LNA

The table below shows a comparison of the desired design specifications and the actual results.

Specification	Goal	Actual w/TQ elements	Actual w/Interconnect
Gain	20dB	10.4dB	7.7dB
Current	≤ 30mA	LNA:21.5mA, SCM:20mA	LNA:21.5mA, SCM:20mA
S11	< -10dB	-19.37dB	-15.26dB
S22	< - 15dB	-22.36dB	-20.03dB
Noise Figure min	< 3	1.54	2.27

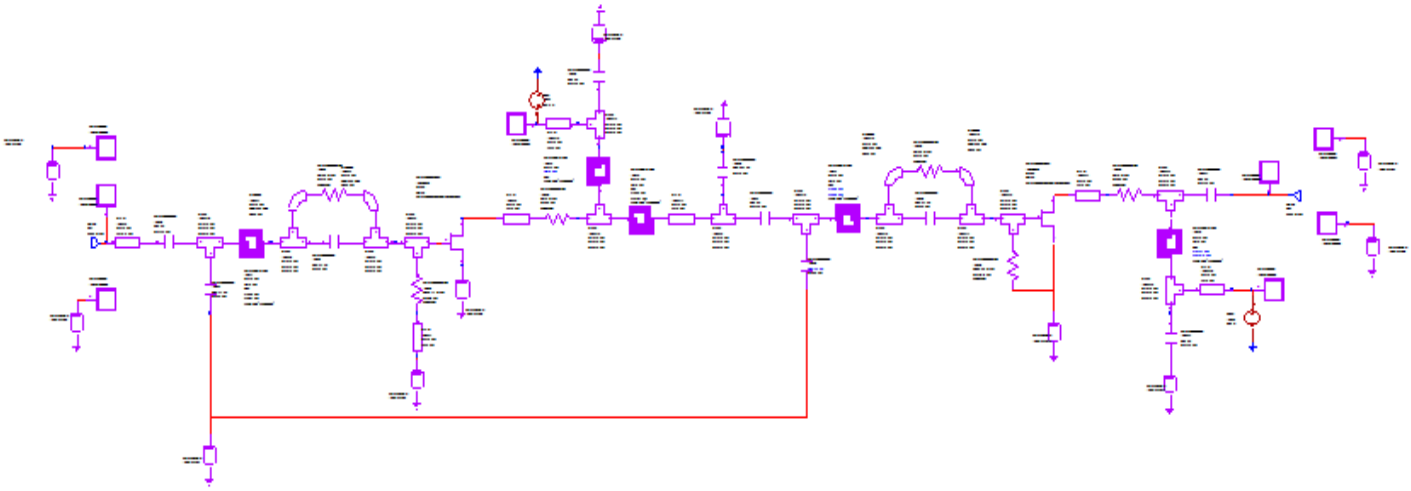


Figure 17a Schematic of Final LNA w/ Microstrip Interconnect

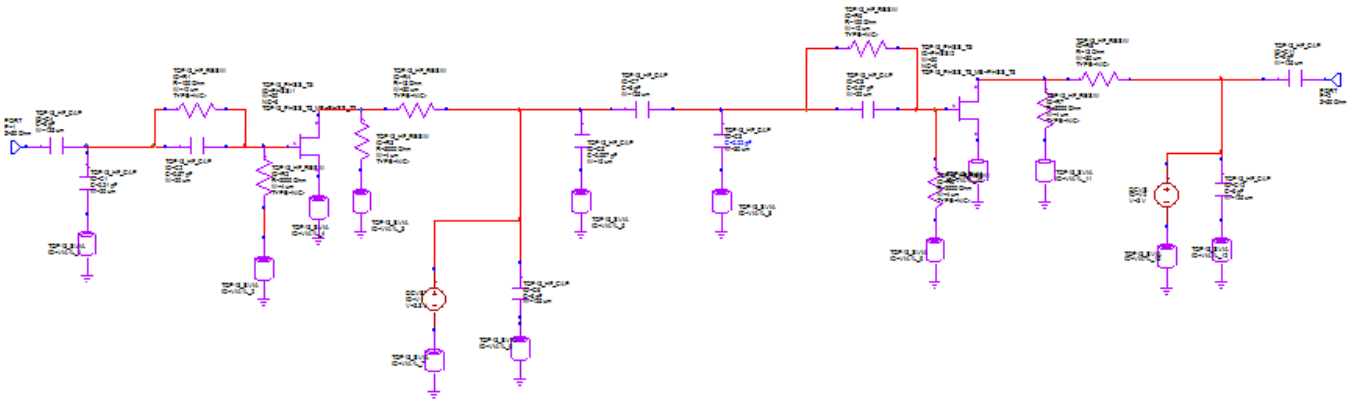


Figure 17b DC Schematic of Final LNA

Layout Plot

The schematic shown in Figure 17a was used for the final layout that is shown in Figure 18. The layout was to fit within the 54mil x 54mil ANACHIP layout that was provided in class. The initial layout did not have the fingers of the devices oriented properly and had to be rotated as shown in Figure 19.

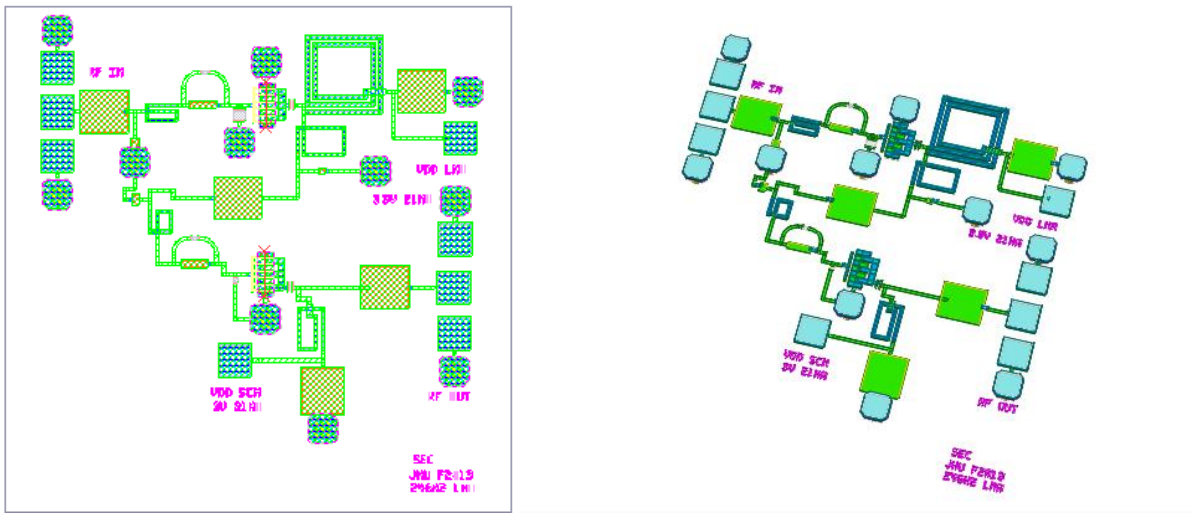


Figure 18 2D and 3D plots of LNA Layout

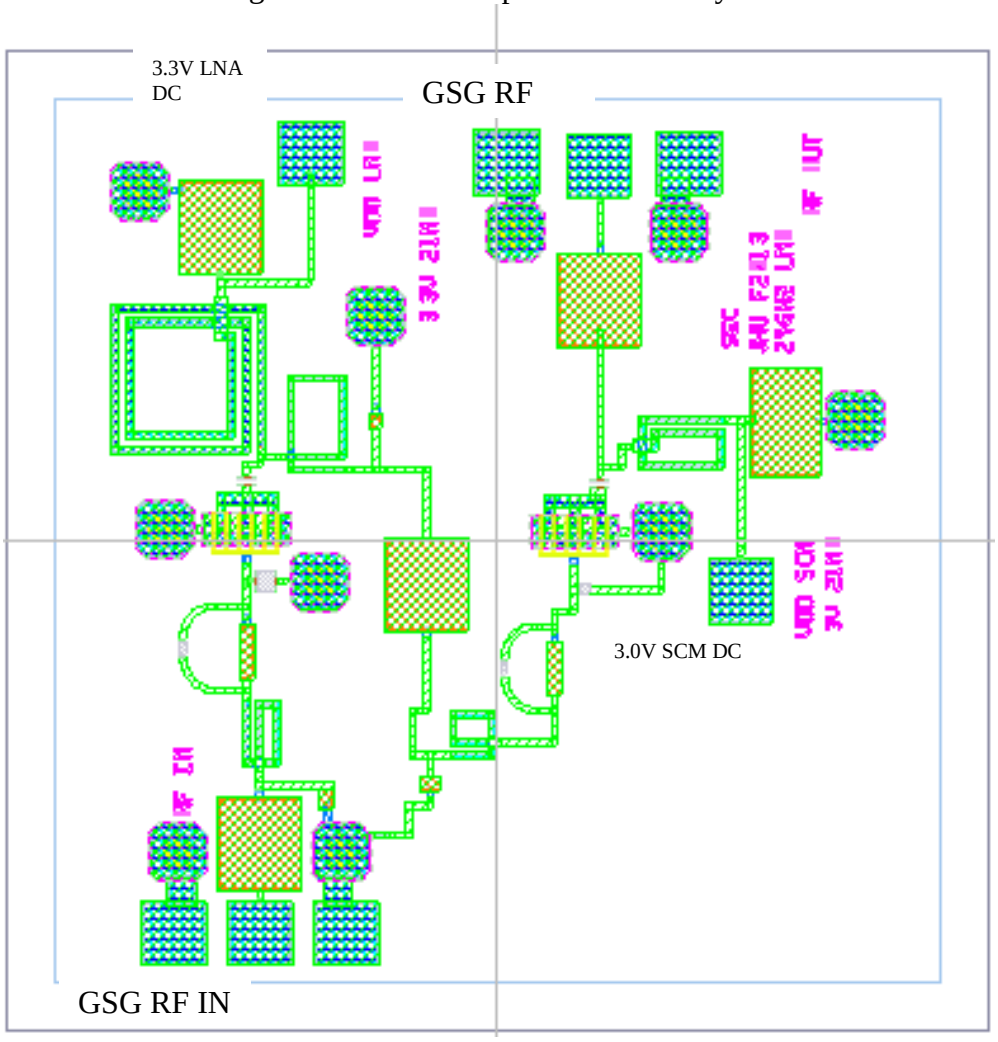


Figure 19 Correct Orientation of Layout

Test Plan

To perform measurements of the LNA the following equipment will be needed: two DC power supplies, network analyzer, RF signal generator, spectrum analyzer and a noise figure meter (if available).

S-parameter measurement

1. Connect DC power supplies to each drain (3.3V for LNA and 3V for SCM; maximum current for each based on DC annotation should be 21.5mA and 20mA respectively).
2. Turn power supplies on.
3. Calibrate Network Analyzer.
4. Connect Port 1 to GSG pads labeled RF IN and connect Port 2 to GSG pads labeled RF OUT.
5. Measure S11, S21 and S22 to compare with simulated results (Figure 14).

Power measurement

1. Connect the output of RF signal generator to input labeled RF IN.
2. Connect Spectrum Analyzer to output labeled RF OUT.
3. Beginning at -20dBm measure the output power in increments of 1dBm to 14dBm.
4. Compare measured data with Pout vs. Pin plot (Figure 13).

Noise Figure measurement

1. If a noise meter is available, connect the noise meter to the input and output.
2. Compare measured data with Noise Figure plot (Figure 16).

Conclusion

In conclusion, the design and layout of a 24 GHz LNA amplifier was completed using the design kit for the TriQuint TQOR_TQP13 process. The design process focused more on stability and minimum noise. It was difficult to meet the specification for gain with a single stage at the desired frequency. To increase the gain, it was thought that adding an amplifier with a higher gain in cascade (the simultaneously conjugate match amplifier) would increase the gain, but the associated losses from the TriQuint elements and interconnect resulted in a lower gain once the final circuit was implemented for layout. This decision to use only two stages did not meet the desired gain of 20dB. There was also an increase in the minimum noise figure as a result of using the SCM amplifier.

During the design process, different approaches to the design were presented during design review. If there had been more time to explore these approaches, the following would be examined: use of a smaller-sized pHEMT, use of several stages of only the LNA in cascade and use of the TOM4 model for non-linear simulations to see if there are significant differences between the models provided in the design kit.

Overall, completion of the design project provided an opportunity to learn how to work with design criteria that have to be taken into consideration when preparing a circuit for layout for a specific process; i.e. size. The design parameters of circuit elements, namely the spiral inductors, used for layout would also be watched more closely during the iterative process to potentially save time and prevent the unwanted need to begin a new design.