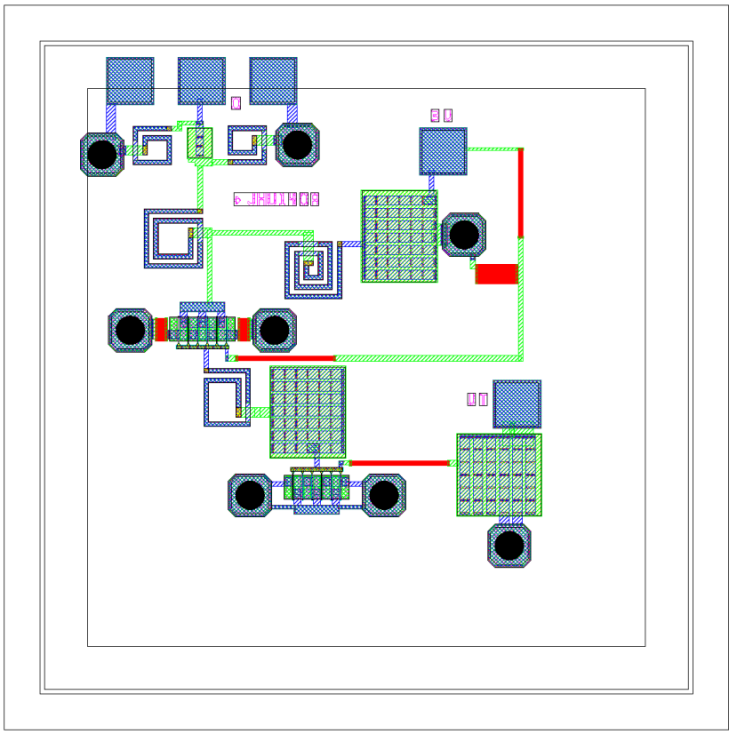
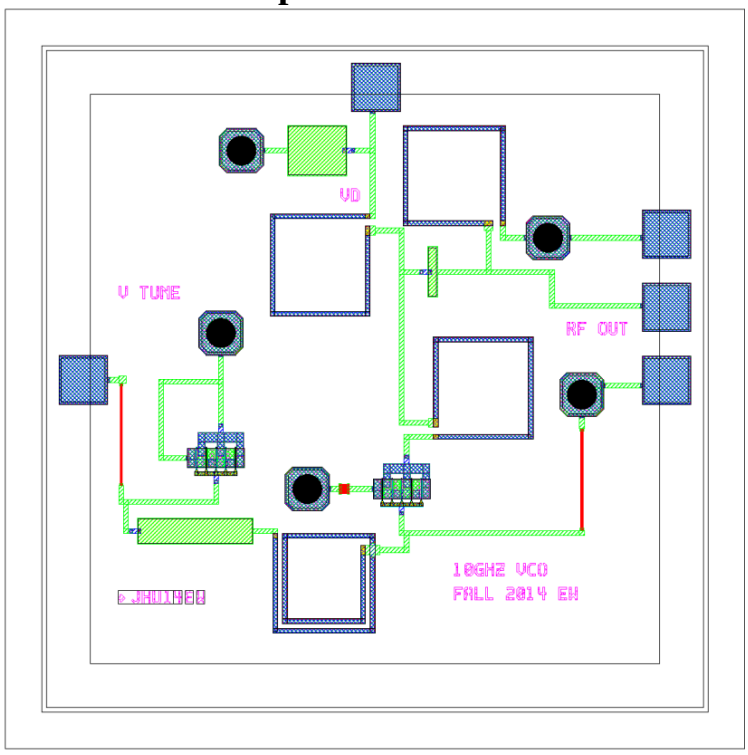
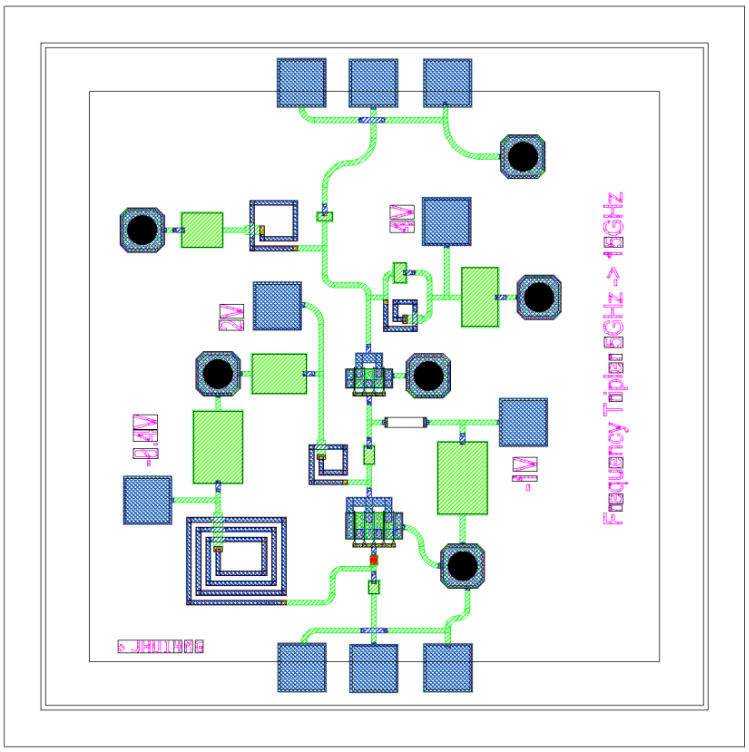
Fall 2014 JHU EE787 MMIC Design Student Projects
Supported by TriQuint, Applied Wave Research, and Agilent
Professors John Penn and Dr. Willie Thompson



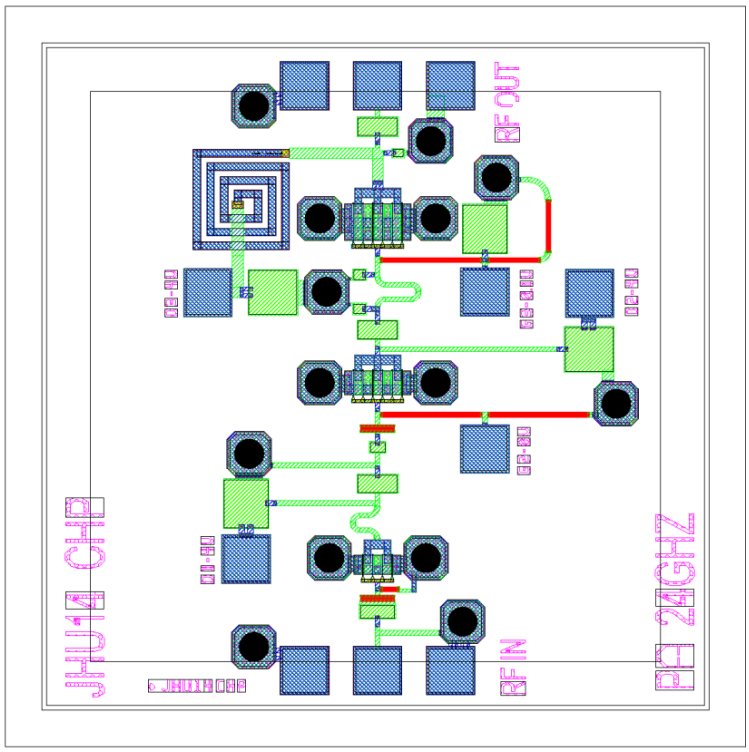
15 GHz Voltage Controlled Osc —Odeneho Anaman



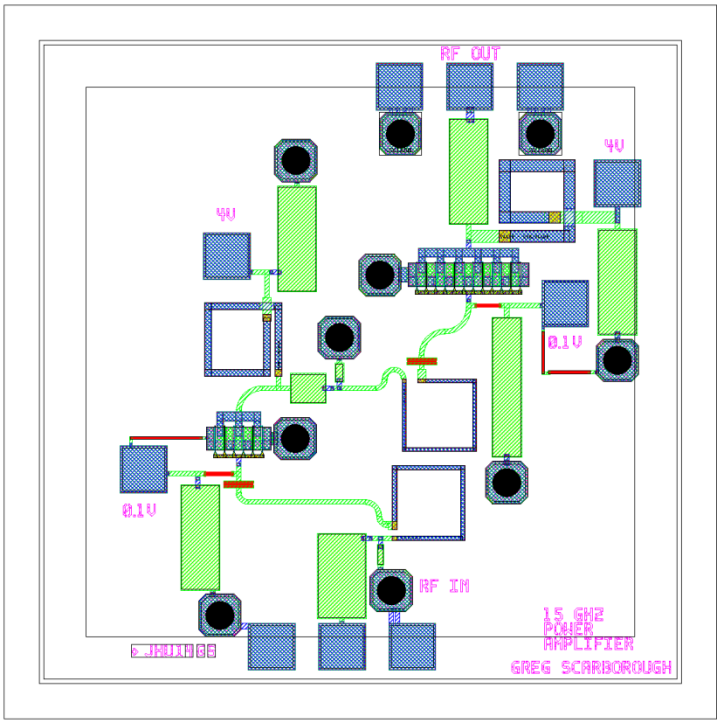
10 GHz Voltage Controlled Osc —Enoch Wong



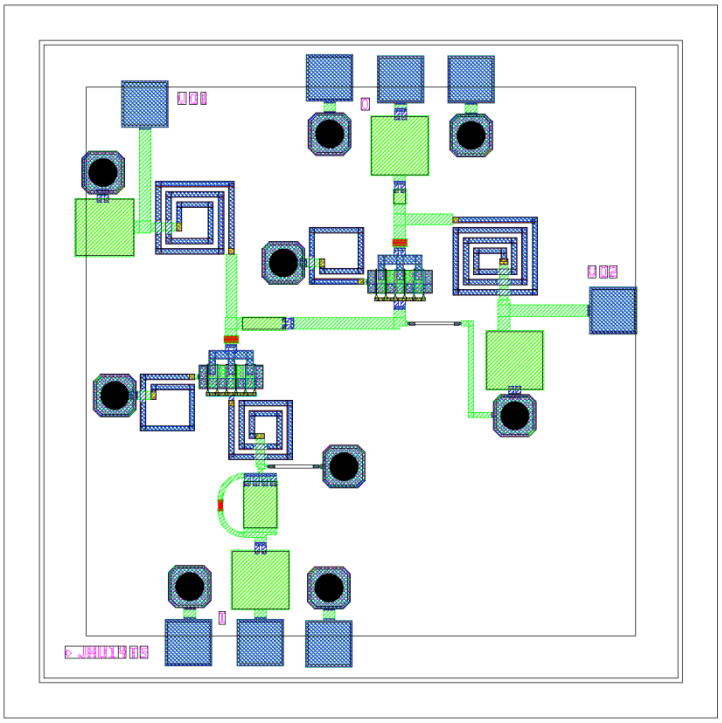
5 to 15 GHz Frequency Tripler -- Nick Gagliolo



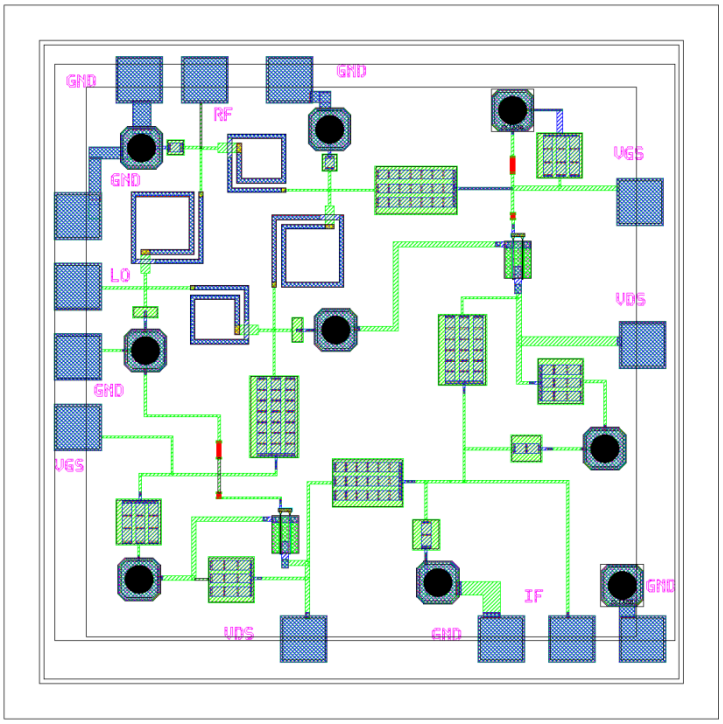
24 GHz Power Amplifier -- Chris Pickett



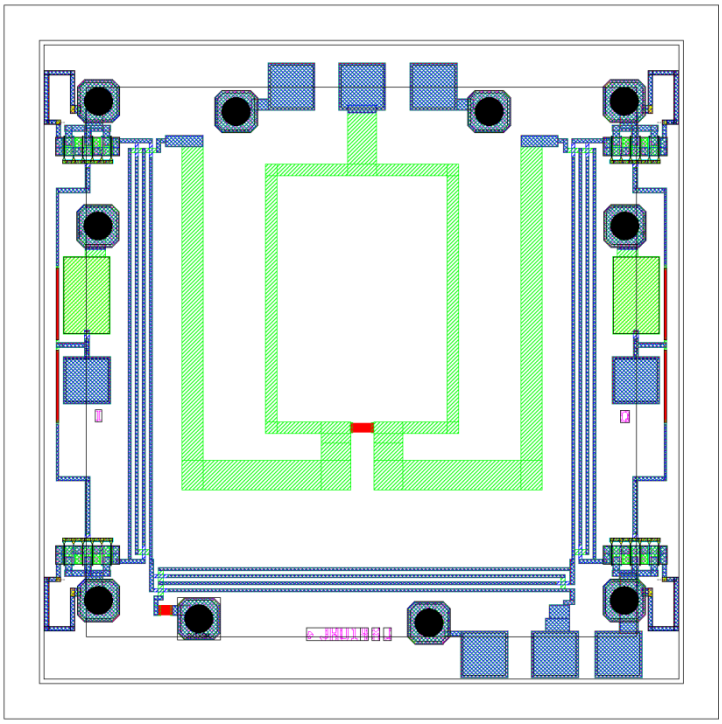
24 GHz Power Amplifier -- Greg Scarborough



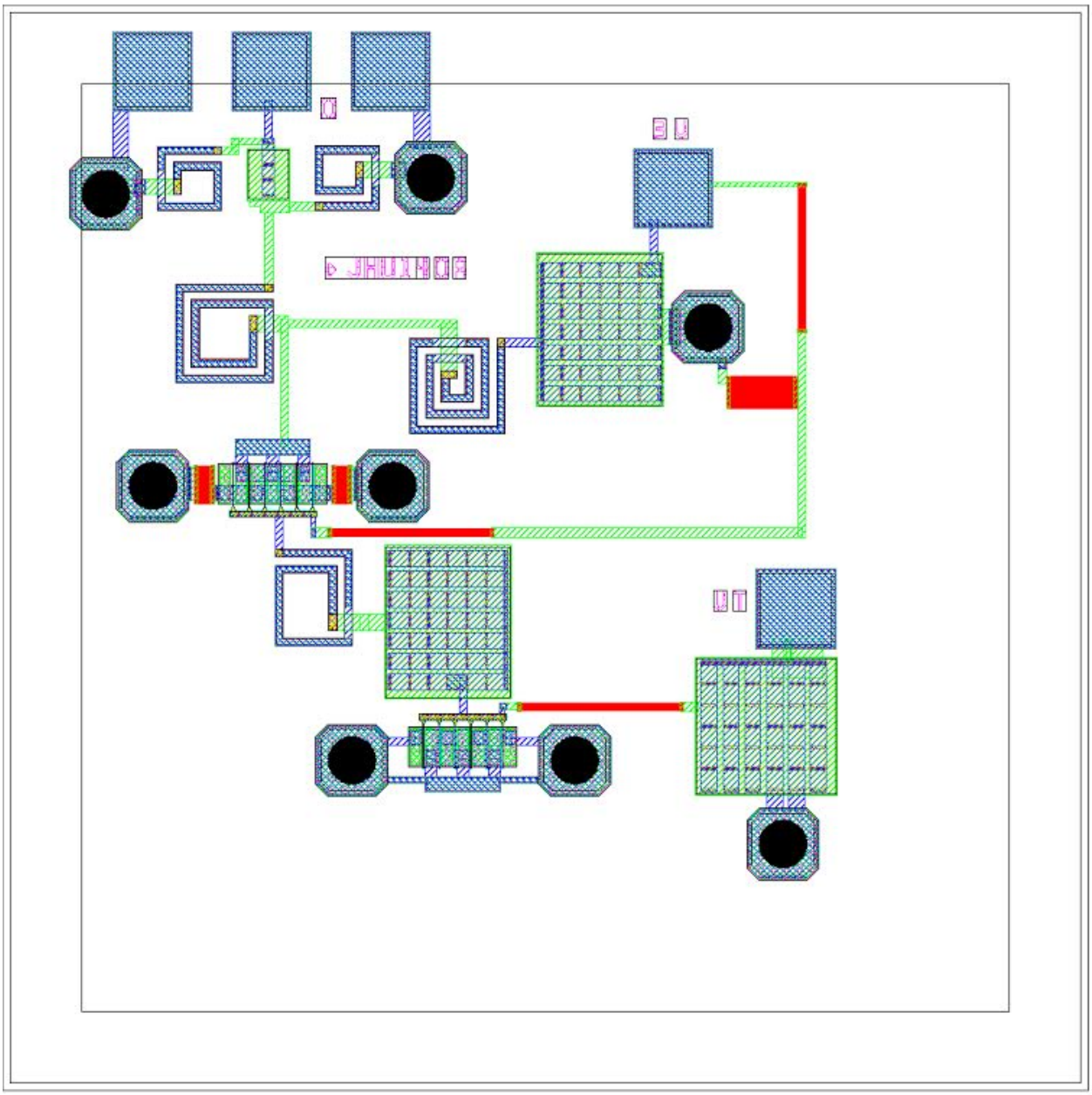
24 GHz Low Noise Amplifier -- Tom Summers



Active FET (PHEMT) Mixer—Asia Mason



34 GHz Vector Modulator—Mark Johnson



15 GHz Voltage Controlled Oscillator

Odeneho Anaman

Abstract

The purpose of this project is to design, fabricate and test 15 GHz Monolithic Microwave Integrated Circuit (MMIC) Voltage Controlled Oscillator (VCO) using Triquint lumped and distributed elements in Agilent's Advance Design System Software. The bias at the drain is 3 V and 0.3V for the Varactor bias. The real estate used for this design is the ANACHIP layout of 60 x 60 mil. To begin the design, the device must be destabilize. To ensure maximum destabilization, a series inductor and varactor are needed at the gate of the device. A series inductor at the drain will cancel out the reactance seen at the drain of the device. A quarter wave transformer is needed to connect the VCO to a 50 Ohm connection.

Introduction

The purpose of the oscillator is to convert a DC signal to an AC signal at a resonant frequency. Microwave Oscillators are one-port negative resistance devices that must have controlled destabilized device. They are used for frequency stabilization, harmonics, etc. Microwave and RF oscillators are used in frequency mixing for up-conversion and down-conversion.

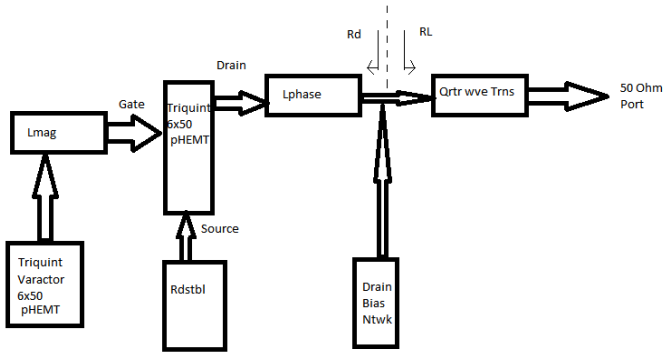


Figure 1 Diagram of VCO

Specifications	intial	Triquint results
Bandwidth, +/- MHz	NS	500
Pout, dBm	> 0dBm	9.5 @Pin=9 dBm
Phase noise	-	-

Design Approach

A. Destabilize device

De-stabilize the device with a source resistance of 15 Ω. Check for instability by using the input Stability Circle, for this project it will be the Load Stability component. Map2Circle component maps the source reflection coefficient magnitude to the unit smith chart. The goal is to have the magnitude of the output reflection coefficient for the mapping circle to be approximately 3.

B. Impement source inductor maximize output reflection coefficient

To provide an input impedance at the gate to ensure maximum or desired output reflection coefficient by adding a series inductor to ground on the gate. Shown in the figure below, the magnitude of the reflection coefficient is approximately 2.2.

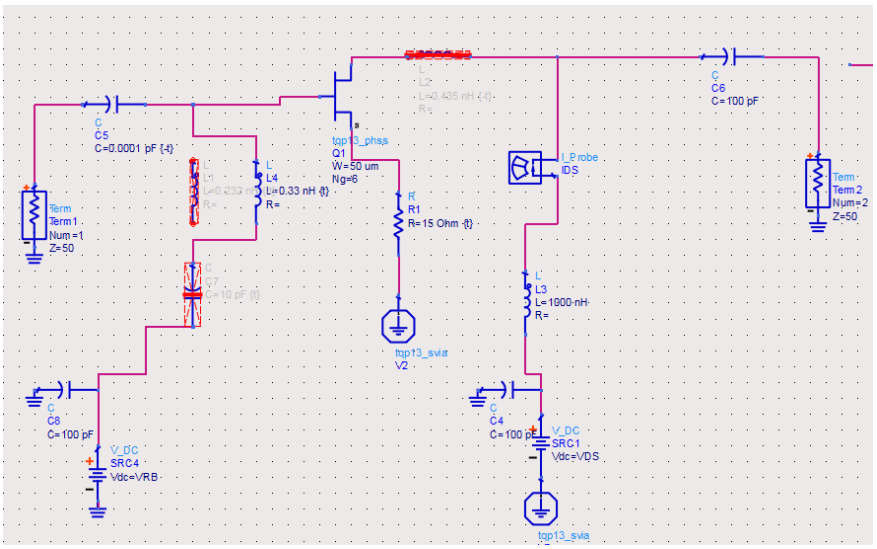


Figure 2 schematic of source inductor for maximum output reflection coefficient magnitude

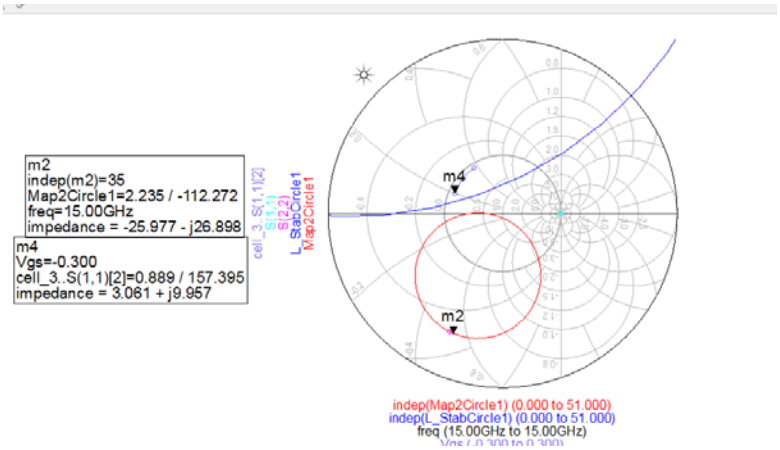


Figure 3 results maximum output reflection coeffient magnitude

C. Drain inductor for zero phase

To create an output matching network so that the phase can be set to have an ideal negative resistance of three. The output impedance is -25 Ω (purely resistive), and this is done by tuning the inductor at the drain.

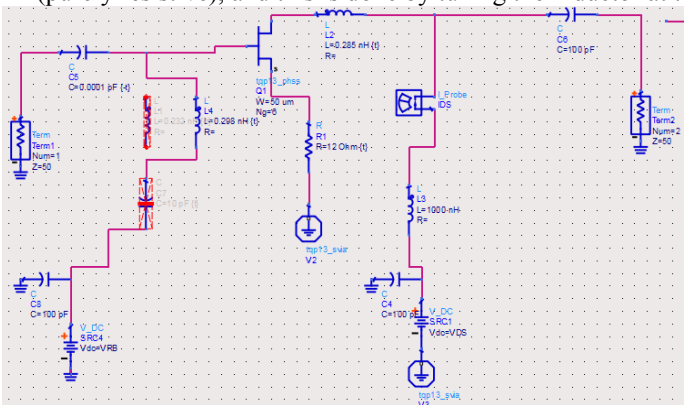


Figure 4 Schematic zero phase drain inductor

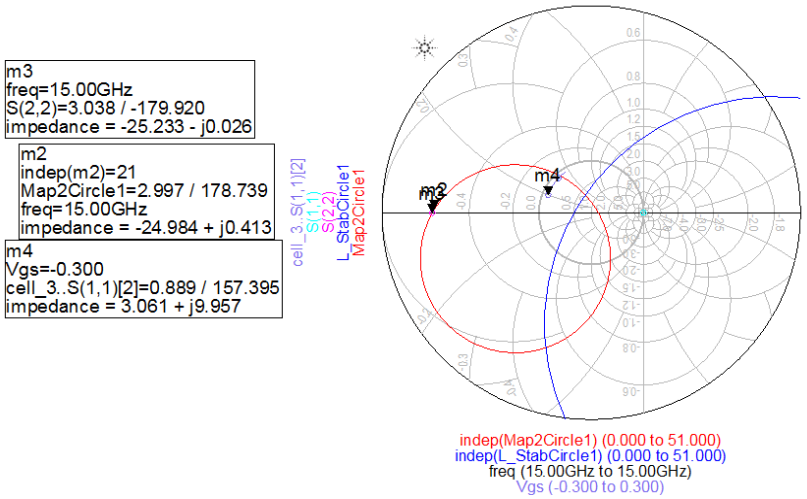


Figure 5 results for zero phase drain inductor

D. Varactor simulation

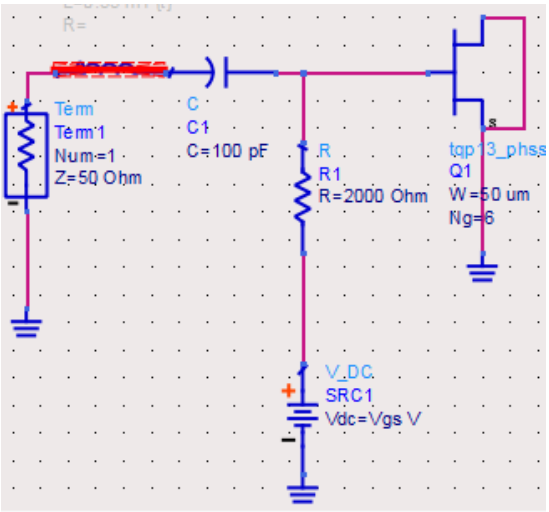


Figure 6 schematic of ideal varactor tune setup

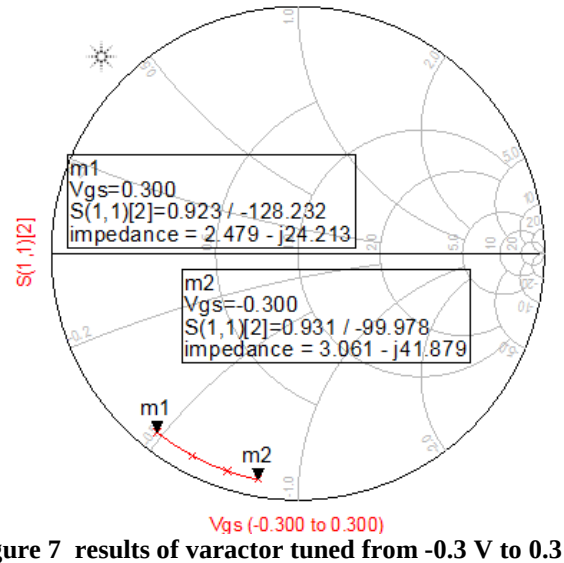


Figure 7 results of varactor tuned from -0.3 V to 0.3 V

E. Results without quarter wave

After obtaining the ideal VCO, the next step is to transform all ideal elements into Triquint elements. Figure below shows the schematic of the VCO with Triquint elements and no quarter wave transformer.

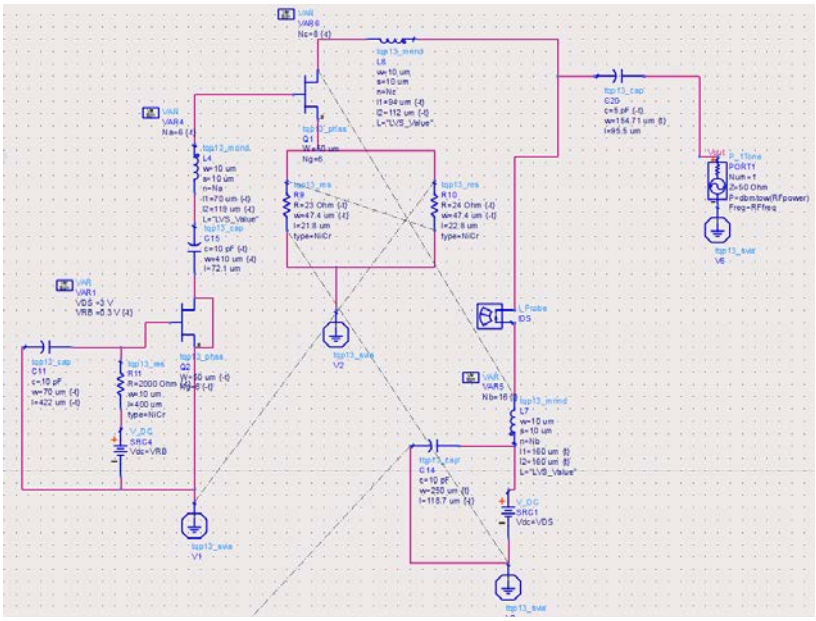


Figure 8 Nonideal VCO without quarter wave

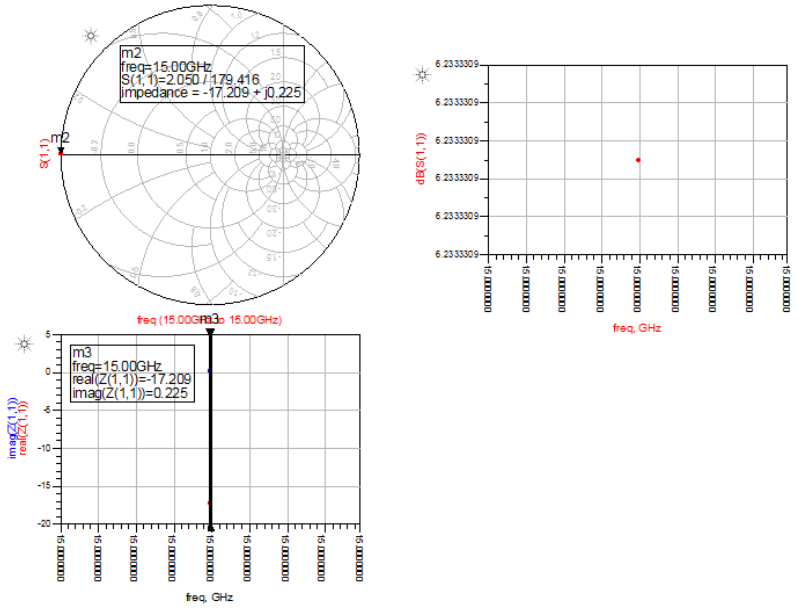


Figure 9 Nonideal VCO without quarterwave results

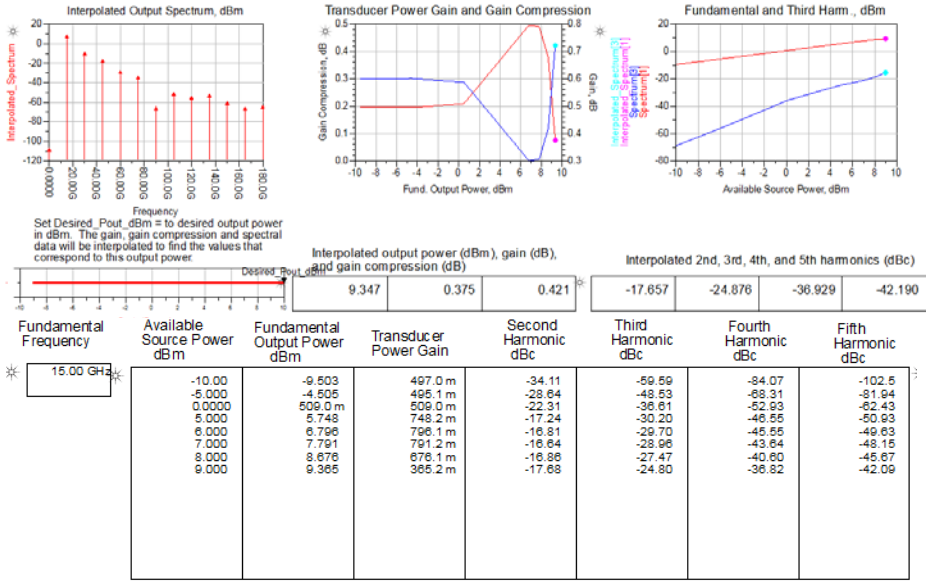


Figure 10 Nonideal VCO without quarter wave power results

F. Results with Triquint quarter wave

After obtaining output reflection of magnitude of approximately 2, with a phase of -179 degrees. The next step is to supply a quarter wave transformer at the drain to start up oscillation. The One-third of the magnitude of the output load impedance of the device at this stage should be matched to 50 Ω. The calculation for the quarter wave transformer is shown below:

$$|Rd|>3RL$$

$$Rd=-17.209 \Rightarrow RL=|Rd|/3 \approx 5.74$$

$$Zqw=\sqrt{(RL*ZL)} \approx \sqrt{(5.74*50)} \approx 16.94\ \Omega.$$

After obtaining the quarter wave characteristic impedance, ADS' Linecalc is used to calculate the transmission line. By using a High Pass filter design, the distributed element was converted into lumped elements.

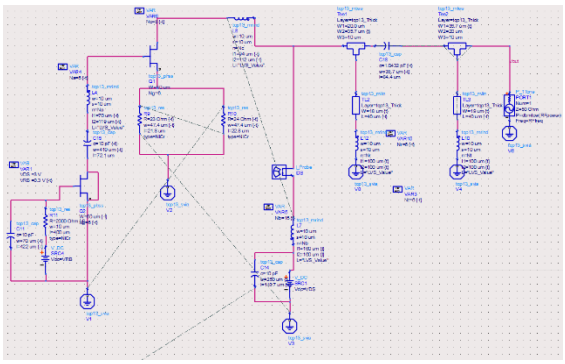


Figure 11 Nonideal VCO with quarter wave schematic

After implementing the quarter wave transformer, there is an issue of convergence for input powers of 5 and 6 dBm. The results are shown in the figure below.

Fundamental Frequency	Available Source Power dBm	Fundamental Output Power dBm	Transducer Power Gain	Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
15.00 GHz	-10.00	-14.50	-4.503	-42.83	-45.09	-68.51	-85.28
	-5.000	-9.286	-4.286	-35.43	-34.18	-52.15	-63.87
	0.0000	-1.863	-1.863	-10.93	-17.56	-42.96	-32.45
	5.000	<invalid>	<invalid>	<invalid>	<invalid>	<invalid>	<invalid>
	6.000	<invalid>	<invalid>	<invalid>	<invalid>	<invalid>	<invalid>
	7.000	7.444	443.9 m	-34.04	-39.15	-51.67	-62.83
	8.000	8.399	398.8 m	-34.72	-39.46	-51.13	-60.63
	9.000	9.358	357.8 m	-35.44	-39.80	-50.70	-58.65

Figure 12 Nonideal VCO with quarter wave power results

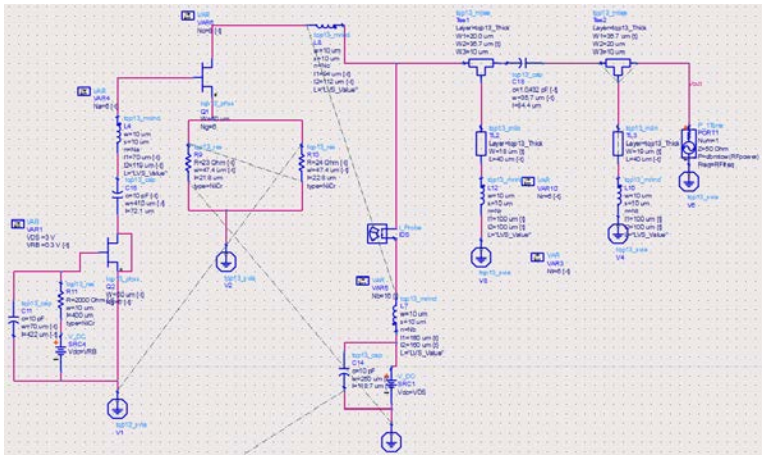


Figure 13 Triquint VCO with quarter wave transformer and swept varactor bias schematic

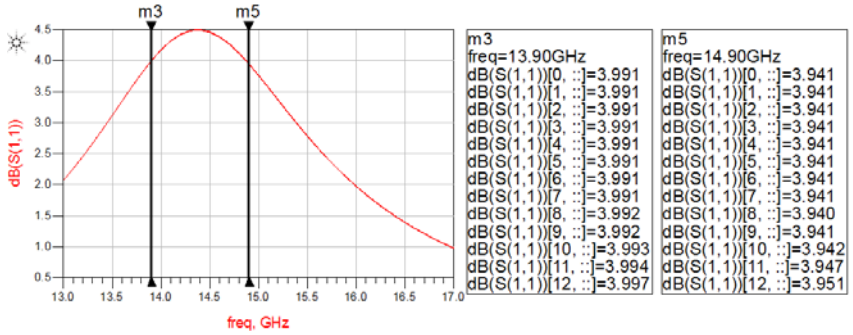


Figure 14 Triquint VCO with quarter wave transformer and swept varactor bias results

II. SCHEMATIC AND LAYOUT

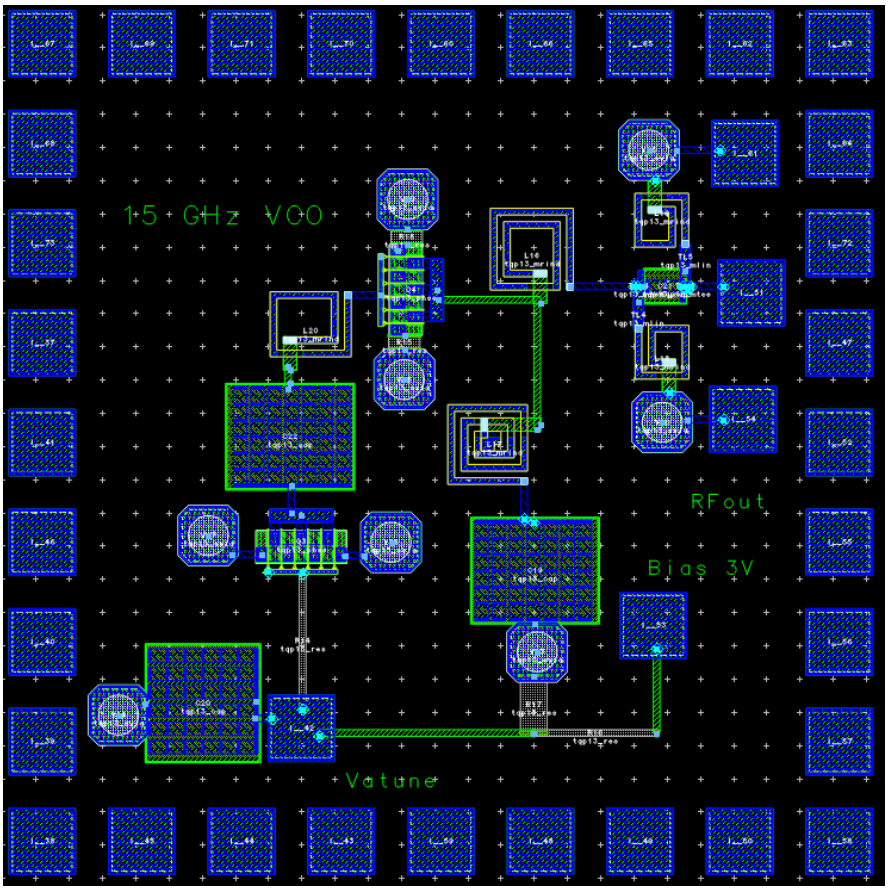


Figure 15 Layout without tuning the Varactor at bias 0.3 V

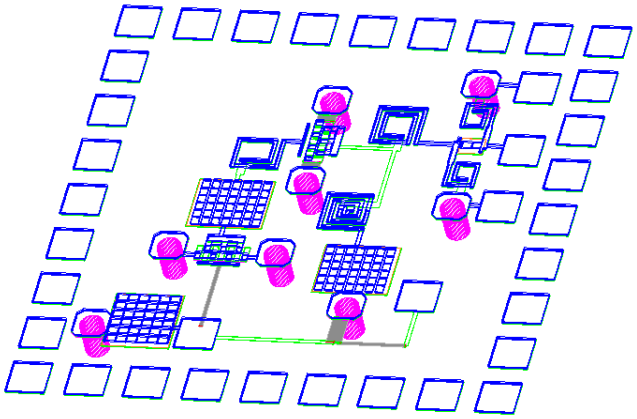


Figure 16 layout of VCO before modification

Conclusion

From looking at figure 12, the frequency of operation was moved to 14.4 GHz. Further optimization is needed in order to shift the frequency of operation to 15 GHz. From the Triquint final schematic, the bias inductor is not needed because the shunt inductor of the high pass filter can be used as part of the bias network at the drain. An EM simulation is needed to see how the device performs. Another method to designing the VCO is to start off with ideal transmission lines at the gate and source and optimize for desired -25 Ω, then transform each ideal section into the corresponding Triquint elements and interconnects.

Test Plan

Equiptmen:

- Power Supply and probes for bias
- Power Supply and probes for Varactor tuning (Vatune)
- Spectrum Analyzer (SA) and RF probe for VCO port

Procedure:

1. Power supplies off
2. Connect power supplies to Varactor and Bias pads
3. Connect SA to VCO port
4. Set bias to 3V
5. Set Vatune to 0.5 V
6. Cheack the SA to see if circuit is oscillating at 15 GHz
7. Sweep input power from -10 dBm to 9 dBm and take note of the output power
8. Adjust Vatune from 0.3 Vto -0.3 V in steps of 0.1 V, record output power

References

[1] Penn, John. “Voltage Controlled Oscillator Design Approach in MMICS.”

[2] Kordovski, A. “24 GHz VCO Fall 2013.” MMICFall13Reports.pdf.

[3] Pozar, David. “Microwave Engineering, Third Edition.

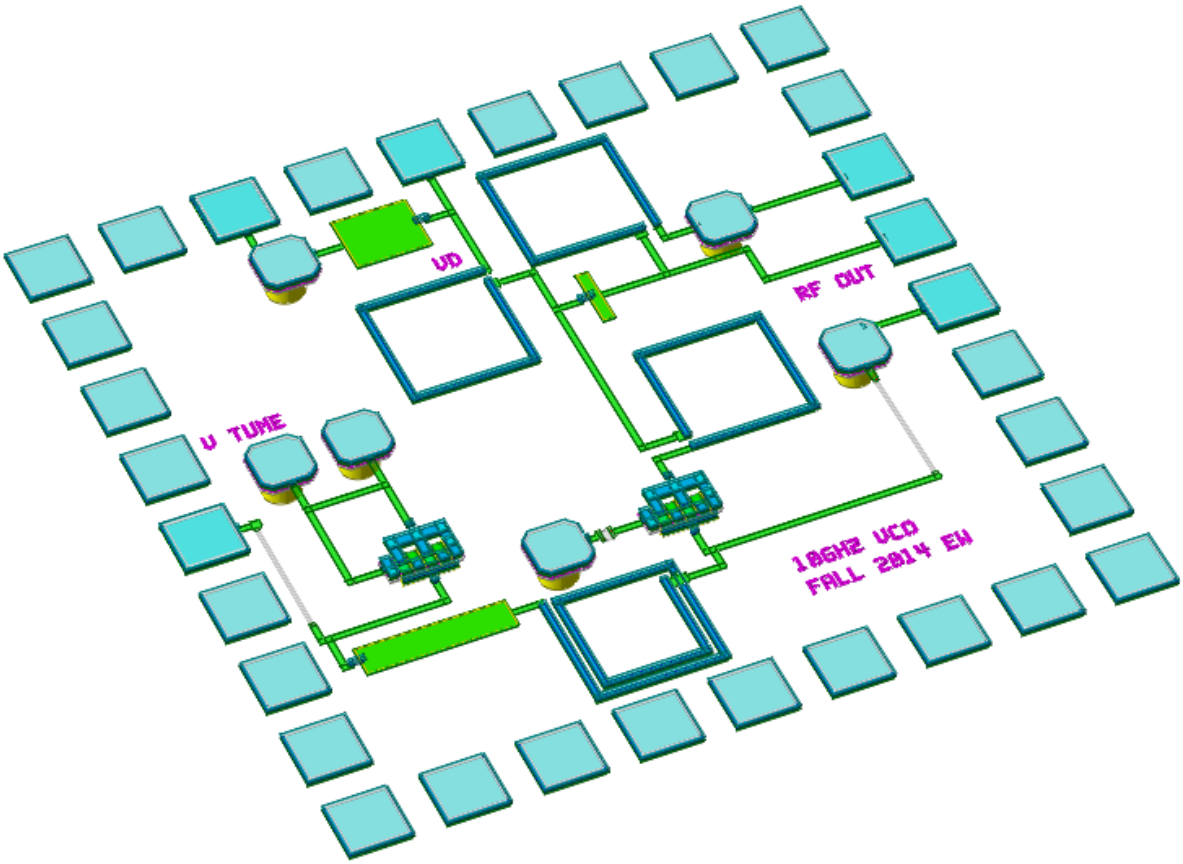
John Hopkins University

EN.525.787.91.FA14

MMIC Design

10GHz VCO

Enoch Wong



Abstract

The purpose of this project was to design a 10GHz Monolithic Microwave Integrated Circuit Voltage Controlled Oscillator (VCO) using Triquint elements. The design would be done using the AWR Microwave Office software. The FET was first destabilized before using the negative impedance method by adding a series resonance oscillator to the gate of the FET. Tuning an inductor at the output of the drain, the ideal phase at the output should be 0. Finally, using a high pass filter quarter wave transformer, we get the impedance transform so that we have a match to the 50 Ohm output port.

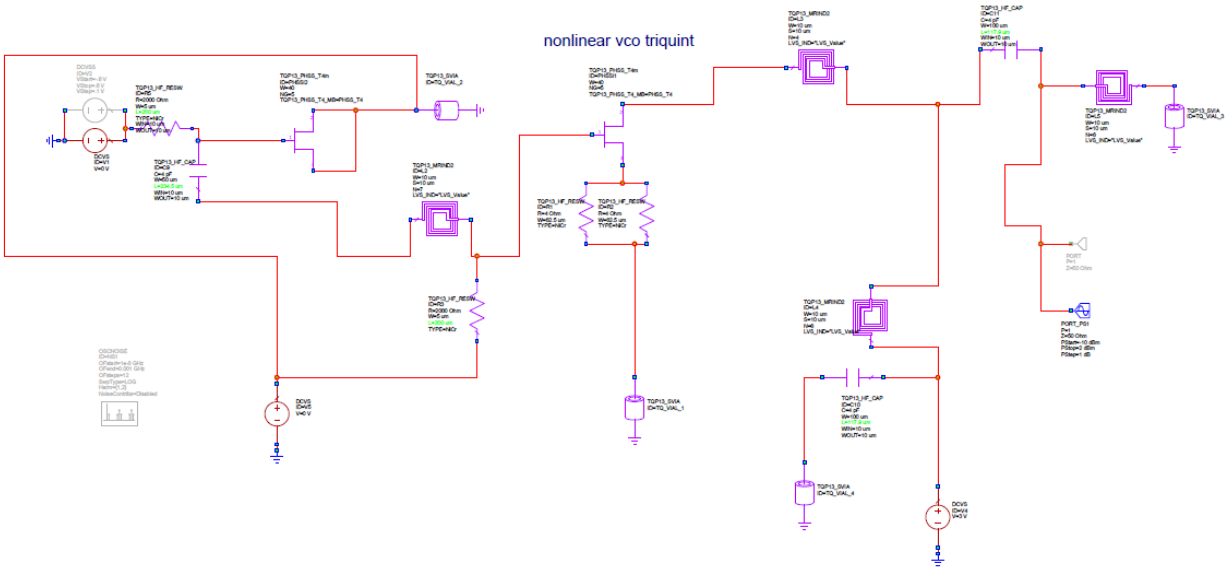


Figure 1. Initial design of VCO

Introduction

A voltage controlled oscillator is an oscillator that primarily uses a varactor as the tuning element. In this case, the FET's drain and source were both tied to ground so that it would act like a varactor diode. Using this varactor, a DC voltage can be applied to vary the total capacitance of the tuning portion of the design.

To start with, one needs to first destabilize the FET to cause it to oscillate. This is typically done by adding source resistors that make it go unstable. Then, the series inductor and capacitor at the gate will maximize the output. An inductor is added to the drain to get close to zero phase. Finally, the high pass filter quarter wave transformer is used to match the impedance of the design output to the impedance of the output port.

Design approach

As mentioned before, the negative impedance method was used to design this 10GHz VCO. For this design, signal strength, power out, and stable voltage output in time were the main concerns. The tradeoff in focusing on this is that the phase at the output and the phase noise was not taken into account.

First, the FET is un-stabilized using the source resistors.

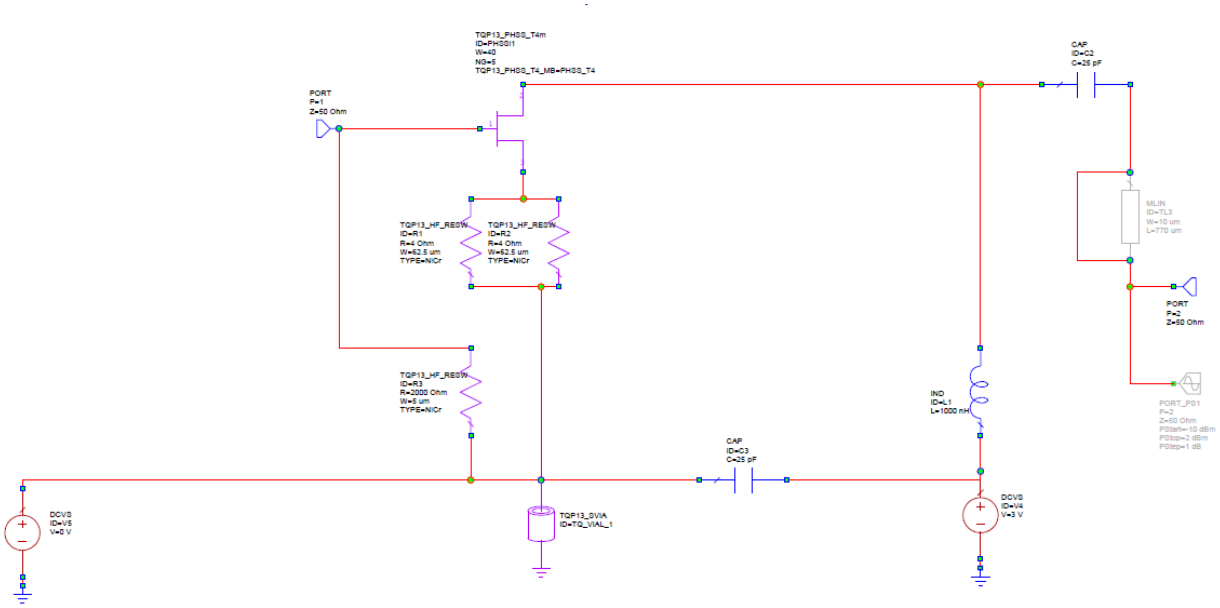


Figure 2. Schematic used for destabilizing FET

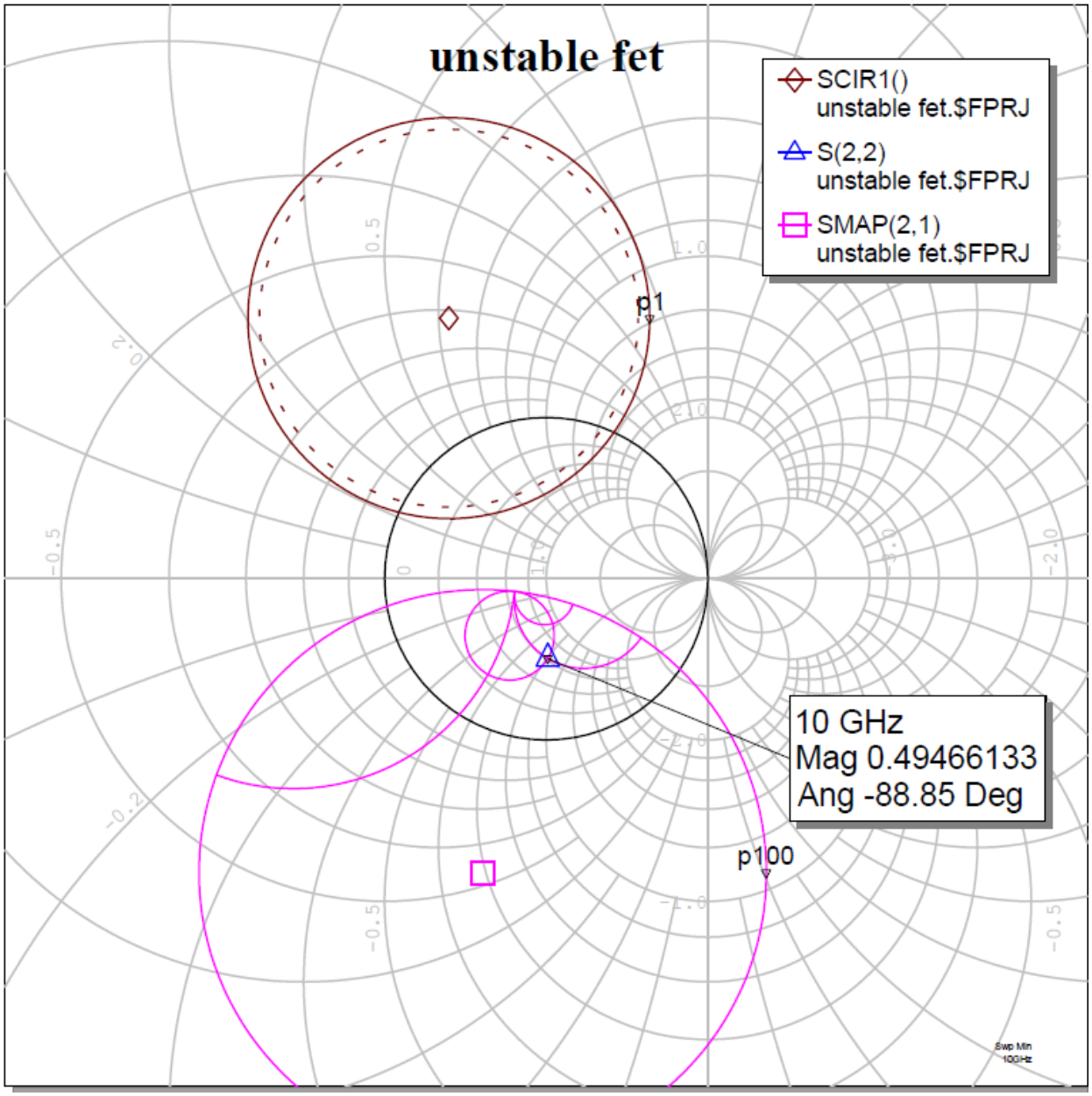


Figure 3. Smith chart showing the de-stabilization

Next, the series resonator is tuned to maximize the output. Then the series inductor at the drain is tuned to get a phase of zero. The varactor is tuned to get a decent frequency range.

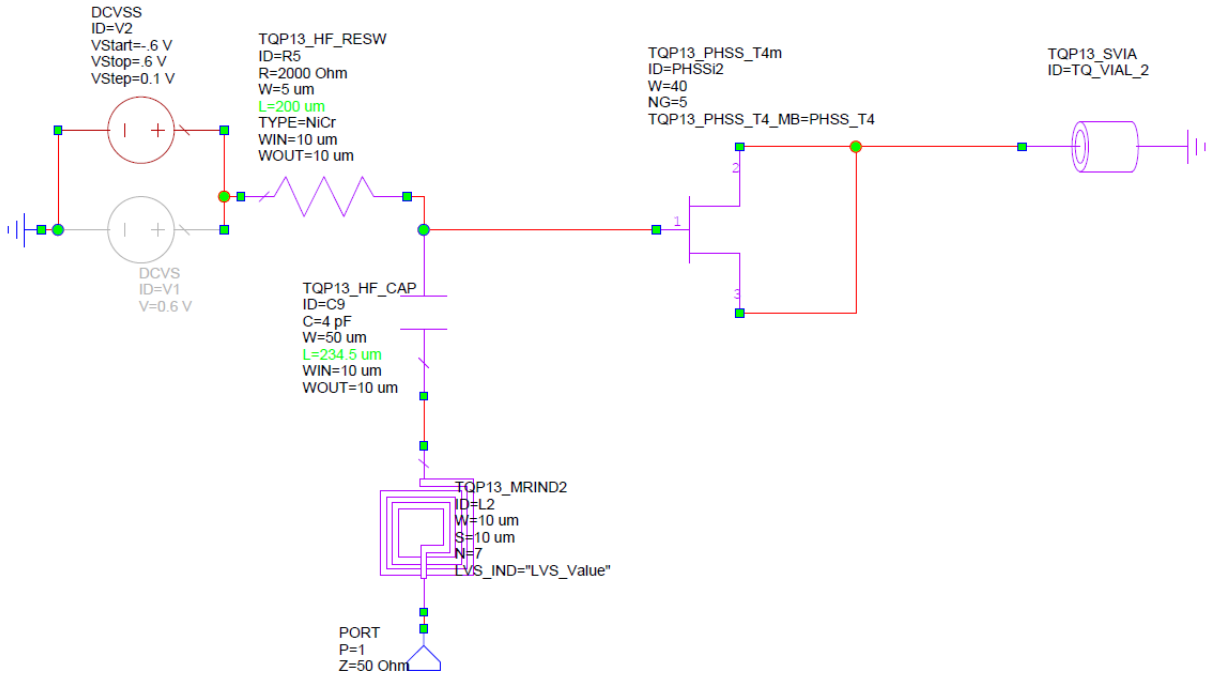


Figure 4. Varactor tuning circuit

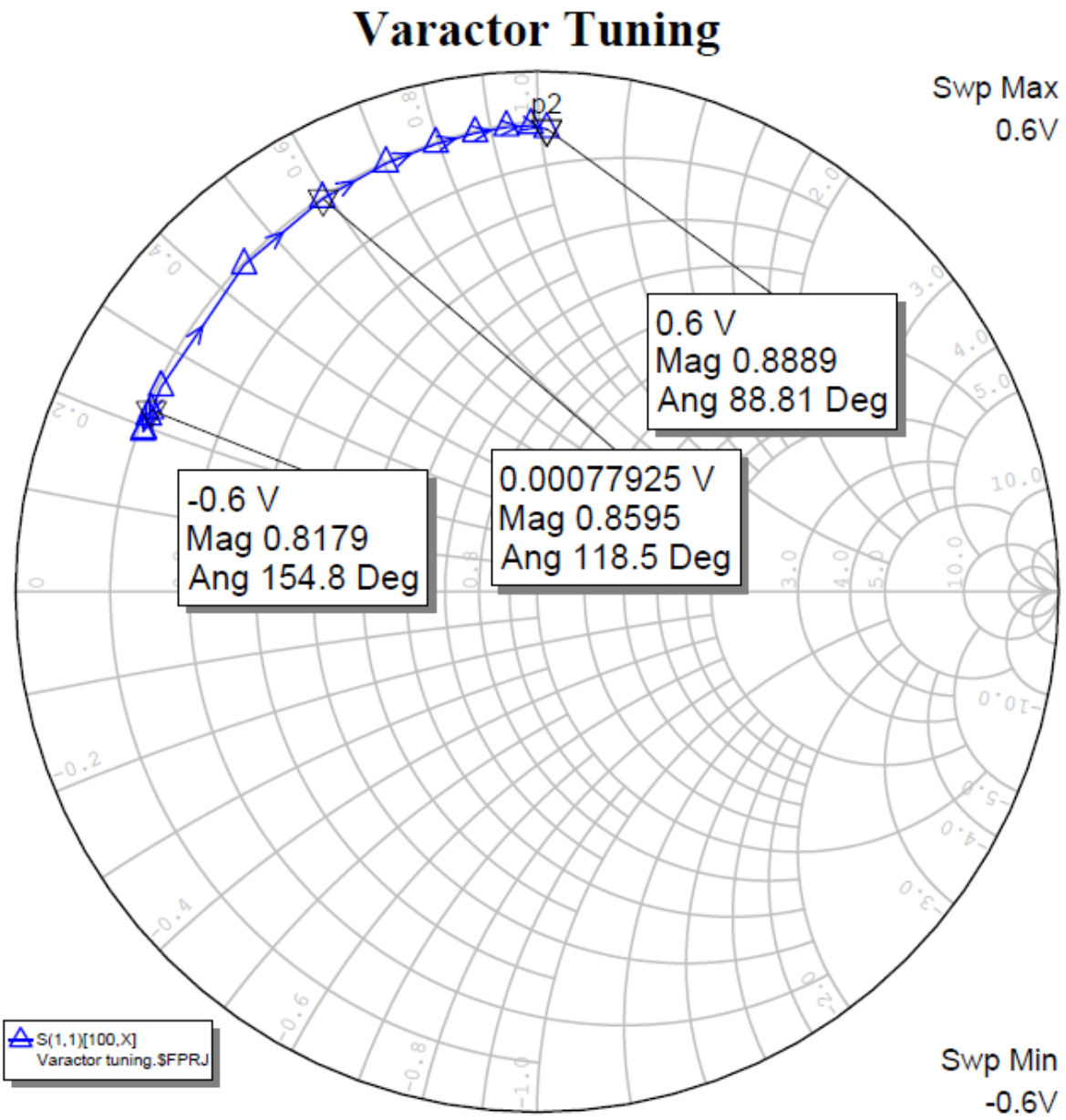


Figure 5. Varactor tuning - Smith chart depicts the varying capacitance

Simulations

The S11 from the VCO shows great promise. The tuning range is about +/- 0.6GHz with the center frequency at 10GHz.

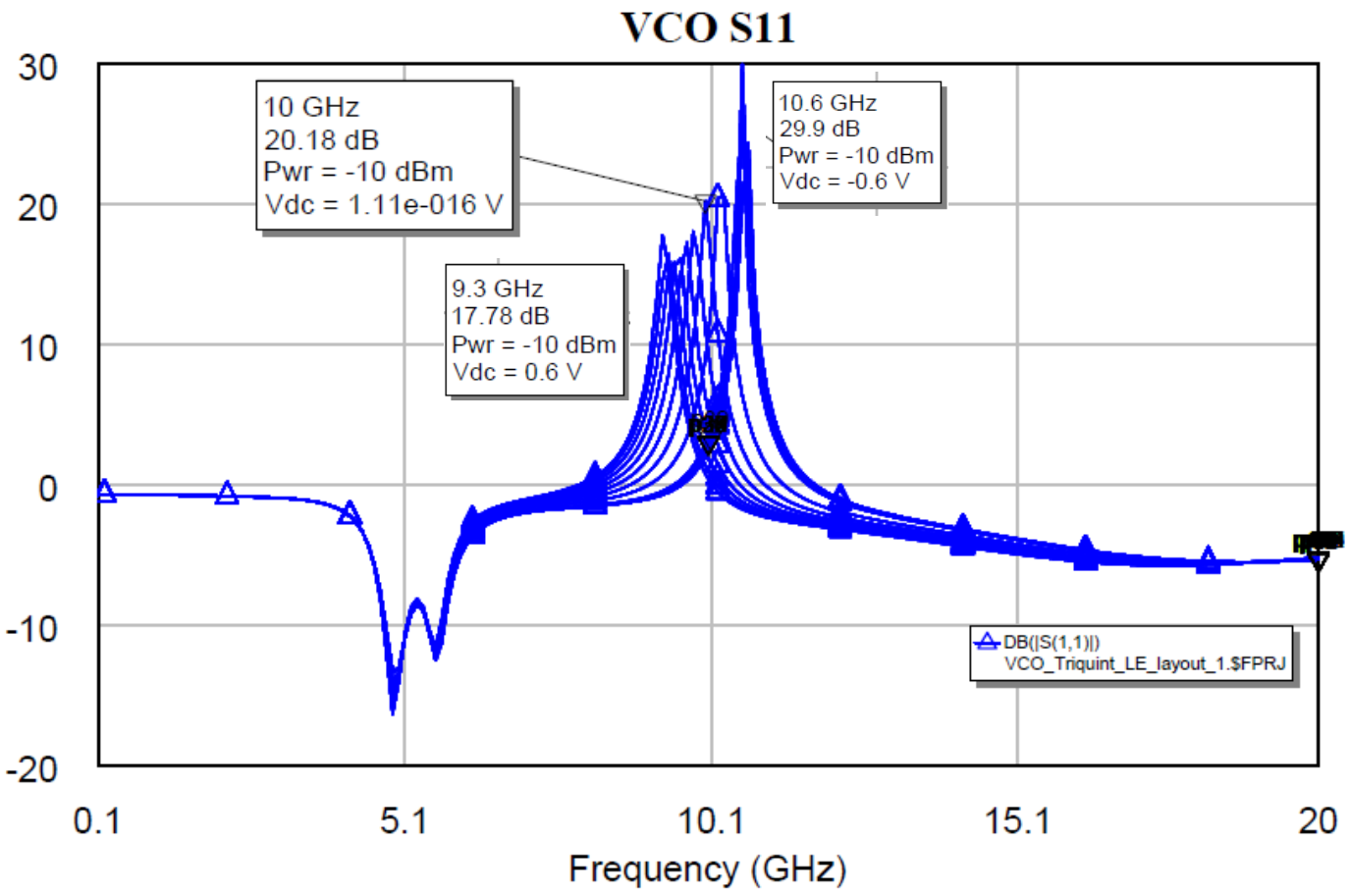


Figure 6. S11 of the layout

The impedance of the design matches to the impedance of the output port. In this way, there the power efficiency should be higher as there is less power loss due to impedance mismatch.

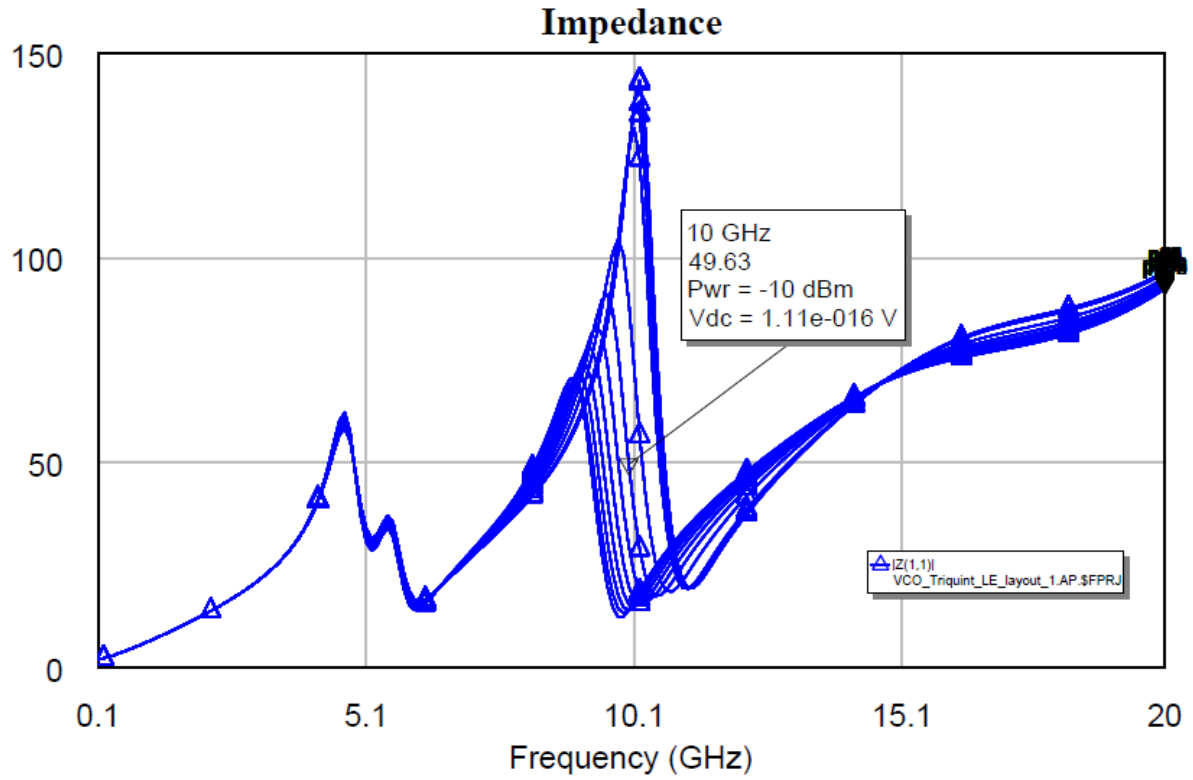


Figure . Impedance of the layout

The power out of the VCO is relatively linear. If there is a need for it, once can always add a power amplifier stage after the VCO to boost the signal.

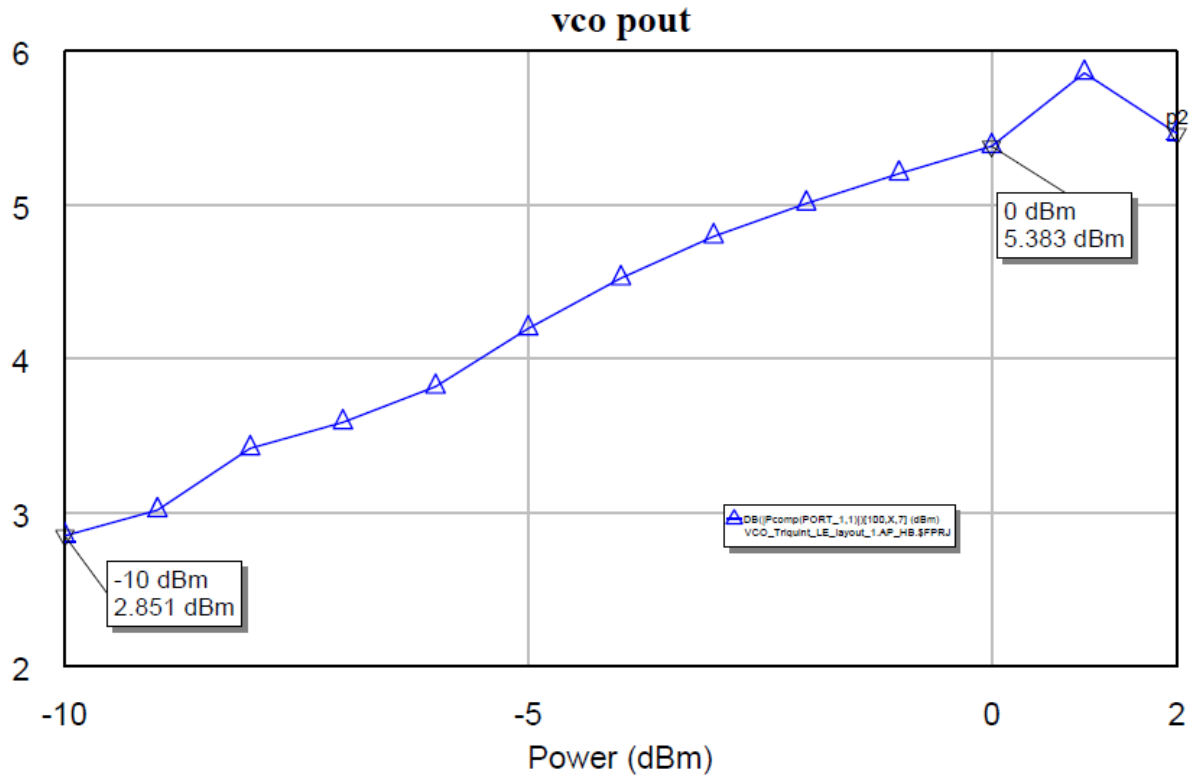


Figure . Power out at the VCO

The harmonics of the VCO look okay. Low pass filtering is definitely recommended to reduce the first harmonic.

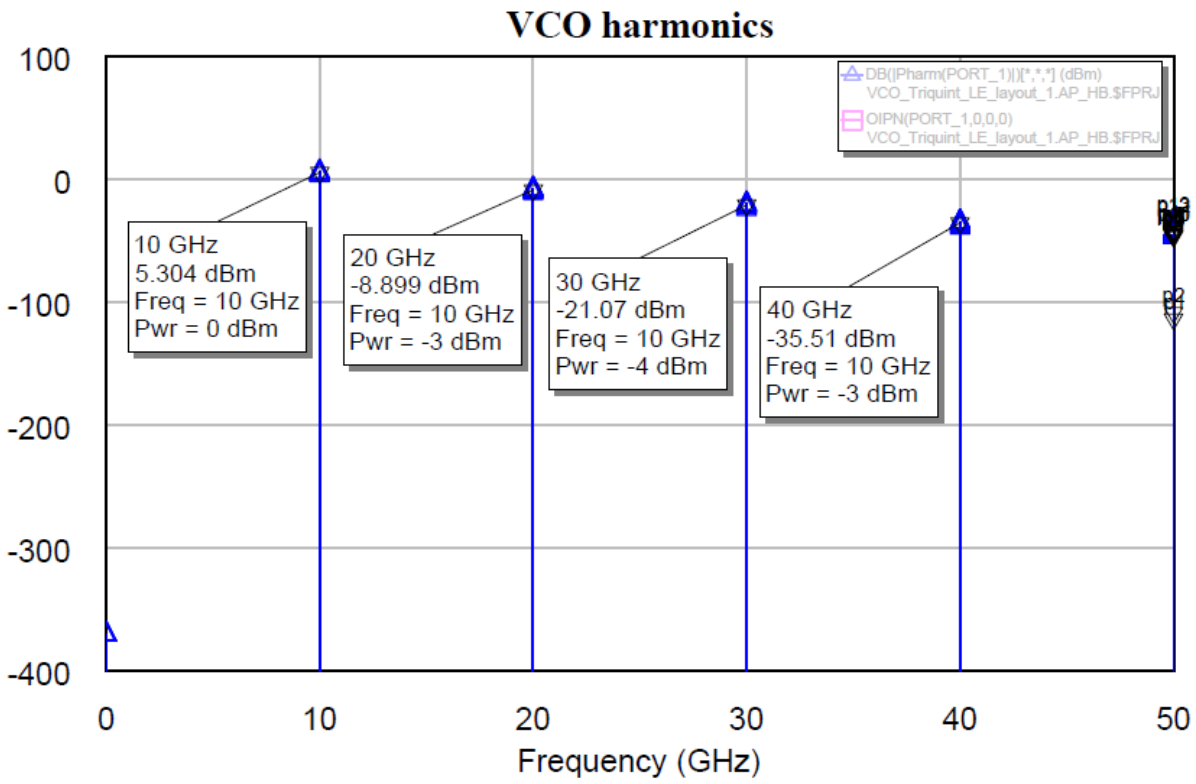


Figure . Harmonics at 10GHz

Finally, the voltage out in time looks consistently stable at 10GHz.

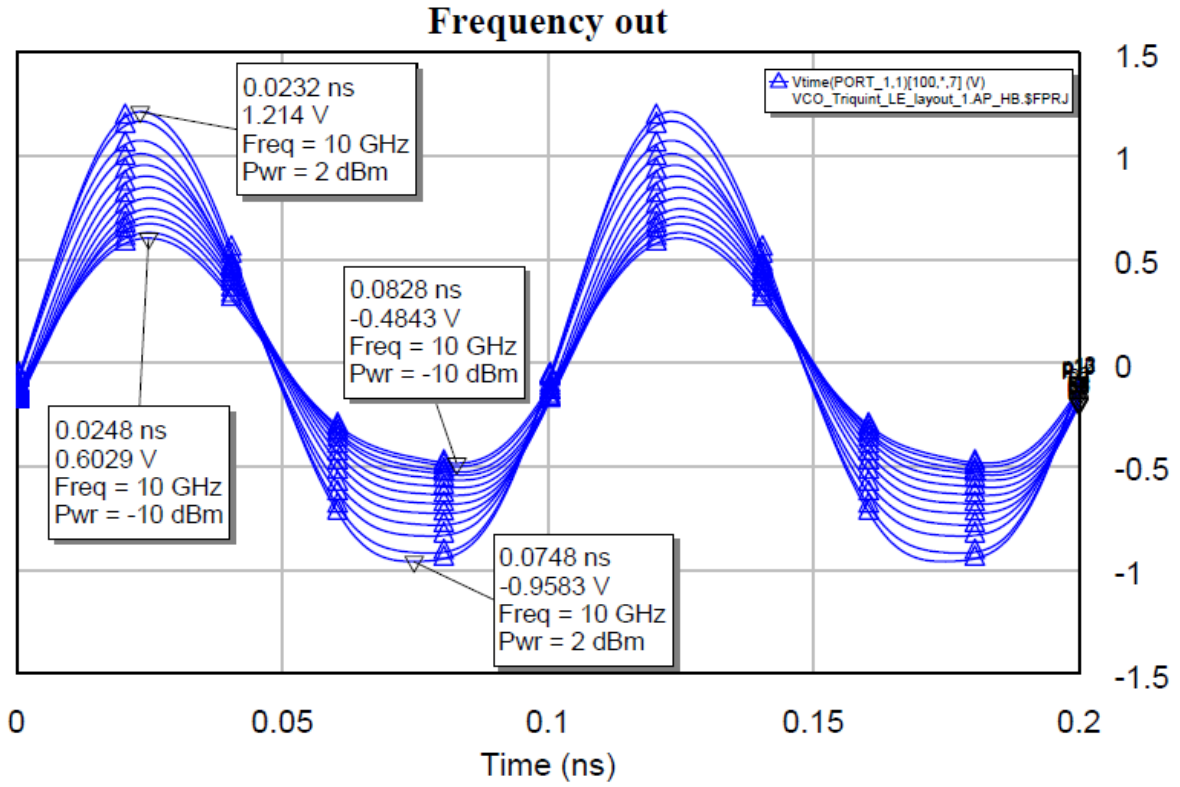


Figure . 10GHz Voltage out in time

Schematic

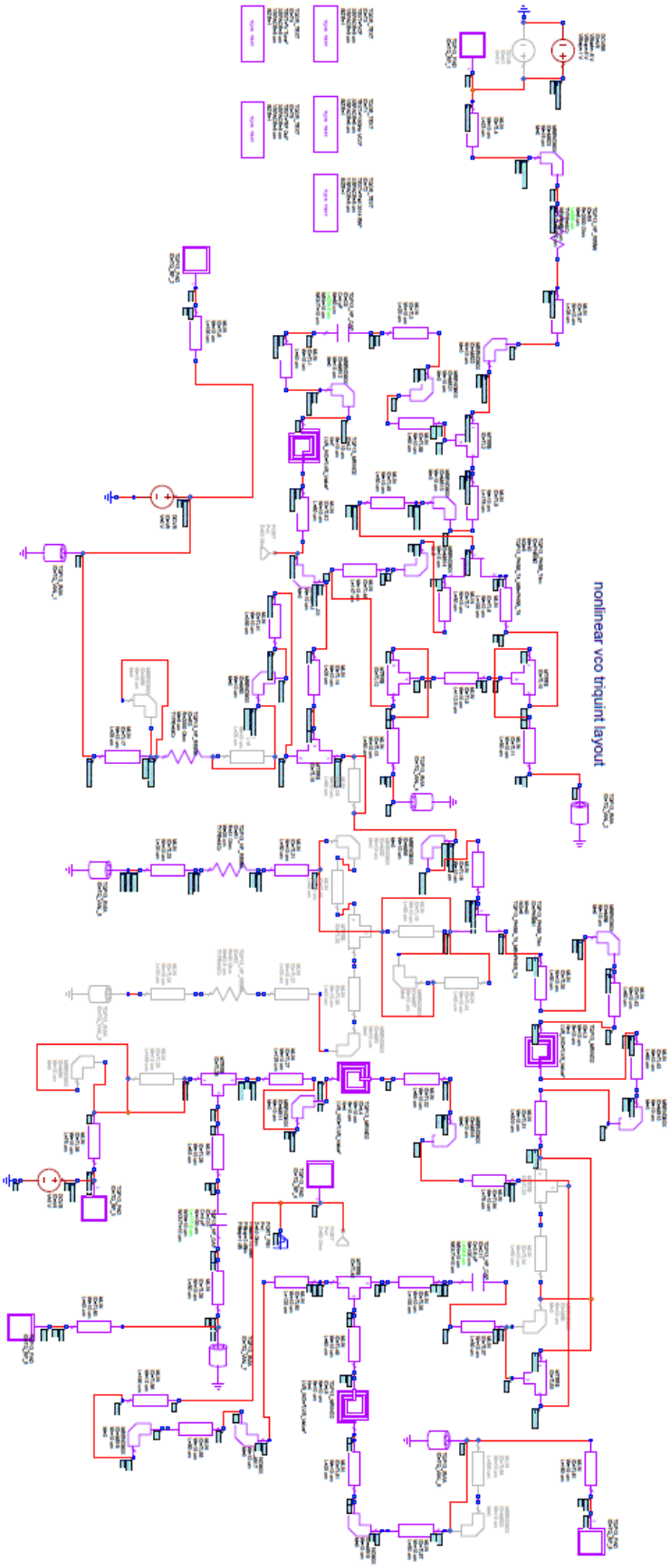


Figure . This schematic shows the interconnects as well as the changes from the initial design. Annotations are also done as well.

Layout

This is the final layout that was submitted. The VD pad is 3V and the other unnamed pads are just ground.

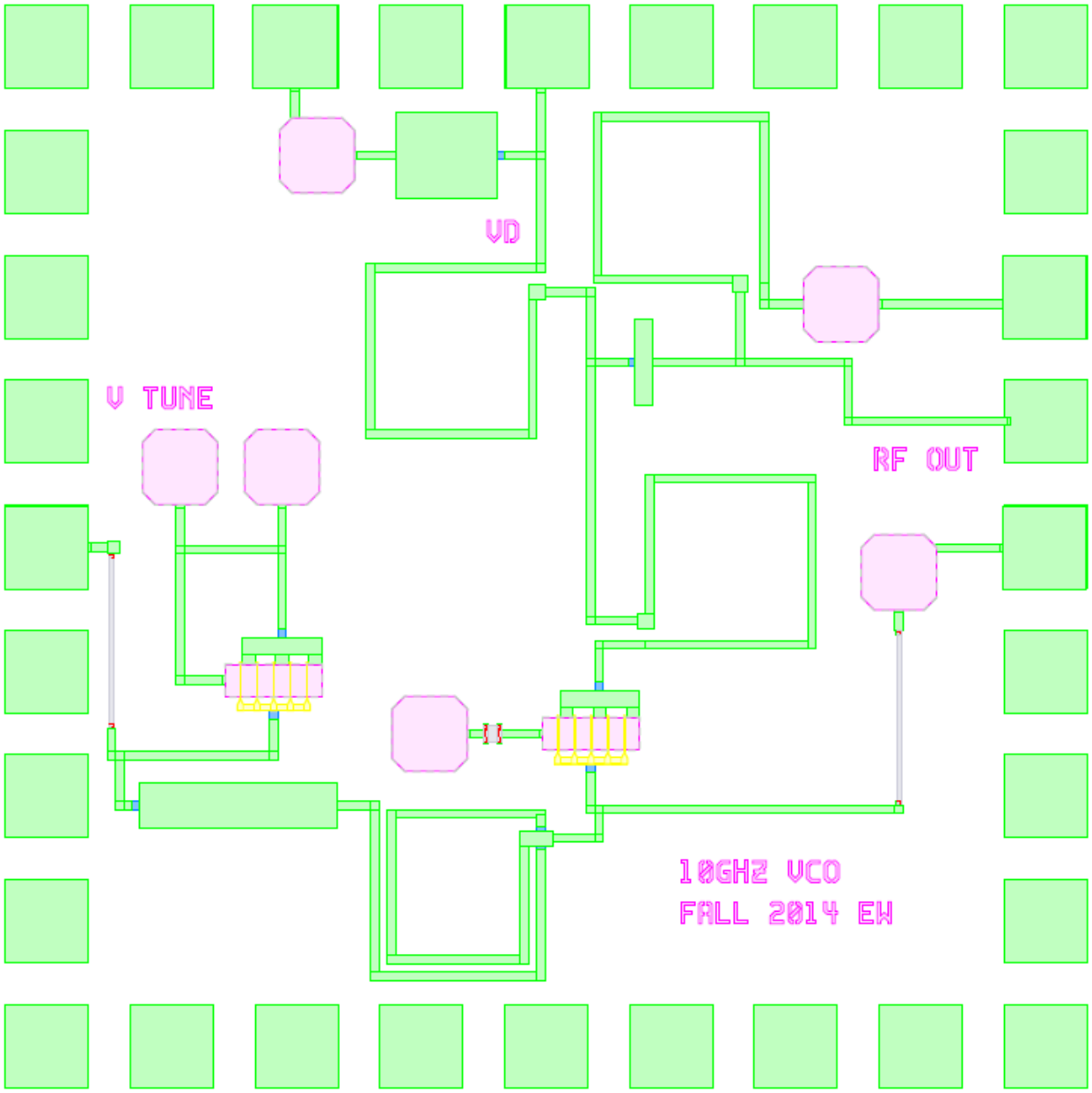


Figure . Final layout design of VCO

Test Plan

Once the fabrication of the VCO design is done, the following equipment will be needed to test the VCO design.

- Spectrum Analyzer

- Probes for VD, V Tune, RF out, and Ground

- DC power supplies for VD and V Tune

Procedure

1. Connect a 3V DC power supply to the pad labeled VD using a probe.

2. Connect a sweeping DC power supply from -0.6V to 0.6V to the pad labeled V Tune using a probe.

3. Connect the grounds of the DC power supply and the spectrum analyzer and have the ground line attached to probe. Have the probe connected to one of the pads connected to a ground via.

4. Connect the spectrum analyzer input to the RF out pad using a probe.

5. Turn the DC power supplies on. You should see an oscillation between 9.3GHz to 10.6GHz

6. Measure the power and each of the different frequencies.

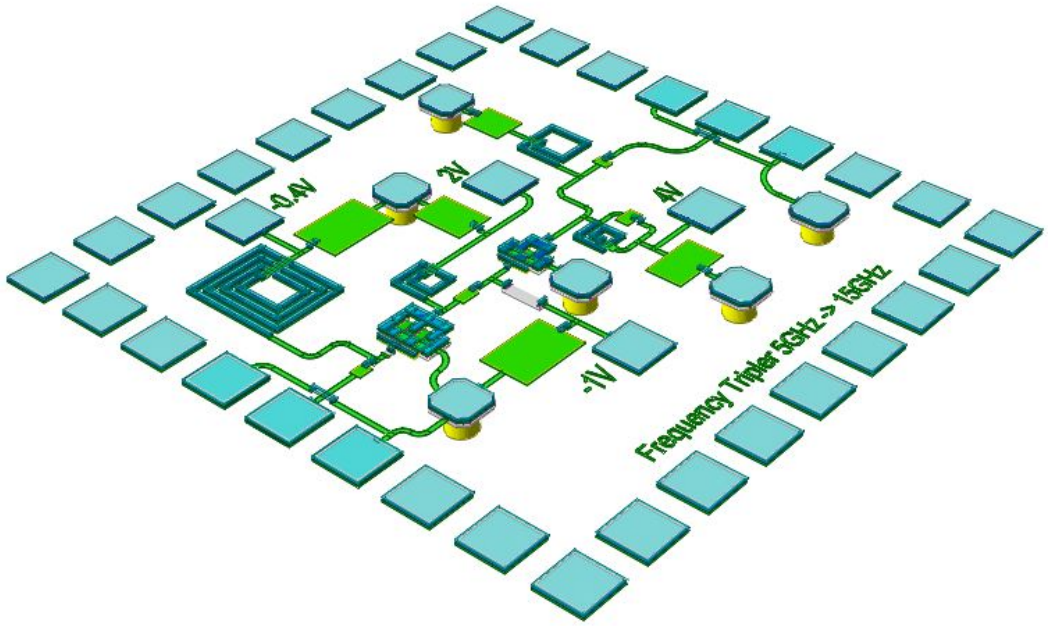
Summary and Conclusion

This report goes over the design thought process of a 10GHz VCO that will be fabricated using the Triquint GaAs process. By using the negative impedance method, we designed a VCO with a center frequency of 10GHz and a tuning range of about +/- 0.6GHz. Further investigation can be done to determine the phase noise and well as additional filtering to dampen the harmonics.

From this design, it becomes very apparent that the length of the traces for the source resistor used for stabilization become very critical when we take a look at how much the design can vary. It was needed to match the impedance at the output to make sure that the maximum power from the VCO gets delivered. Also, there were many issues running the software as it lead to errors causing the program to crash or even corrupt the files.

In the future, it would be very interesting to properly characterize the phase noise and see which method would best reduce it.

EN.525.787 MMIC Design
Fall 2014 Final Project
5GHz Frequency Tripler



Nicolas Gagliolo

Abstract:

This paper details the design and simulated results of a two-stage frequency tripler designed using the Triquint 0.13um pHEMT TQP13 process on a 100um x 100um die. The circuit is designed to function at an input frequency of 5GHz and create an output at 15GHz. The simulated results show a conversion gain greater than -3dB for input power levels of 4.377dBm and up, and greater than 20dB isolation between the 2nd harmonic (15GHz) and both the fundamental (5GHz) and 1st harmonic (10GHz). The simulations also show a total DC consumption of 0.015mW.

Introduction:

Frequency multipliers have a multitude of uses, and are most often used in transceivers to produce a high frequency LO signal for the mixer. While passive frequency multipliers exist and are used, they suffer from high conversion loss and typically require higher input power. It is therefore useful to design and use active multipliers, which can produce conversion gain and require less input power. Active multipliers typically rely upon a transistor biased near cutoff to produce a harmonic-rich output, which is then filtered to obtain the desired output frequency.

In their 2014 paper[1], Mingquan Bao et al detail a novel approach to designing a frequency tripler in which they first use a transistor biased in class-B operation to produce the harmonic-rich output. The design then takes advantage of the non-linear characteristics of a transistor biased in class-C operation to produce the 2nd harmonic from the inter-modulation terms that occur when mixing the fundamental, 1st, and 2nd harmonics, in addition to the usual amplified terms and harmonics generated from the non-linear operation. This topology produces strong conversion gain and state-of-the-art peak power efficiency, and serves as the basis for the design outlined in this paper.

The original design was designed for use in the D-band (110 – 170GHz), and used 0.25um InP DHBT technology, but the overall topology (class-B stage followed by a class-C stage) is used in the Triquint 0.13um pHEMT TQP13 process to produce a 5GHz frequency tripler (15GHz output).

Design Specifications:

The proposed specifications for the 5GHz – 15GHz frequency tripler are shown below, in Table I:

Table I: Design Specification for Frequency Tripler

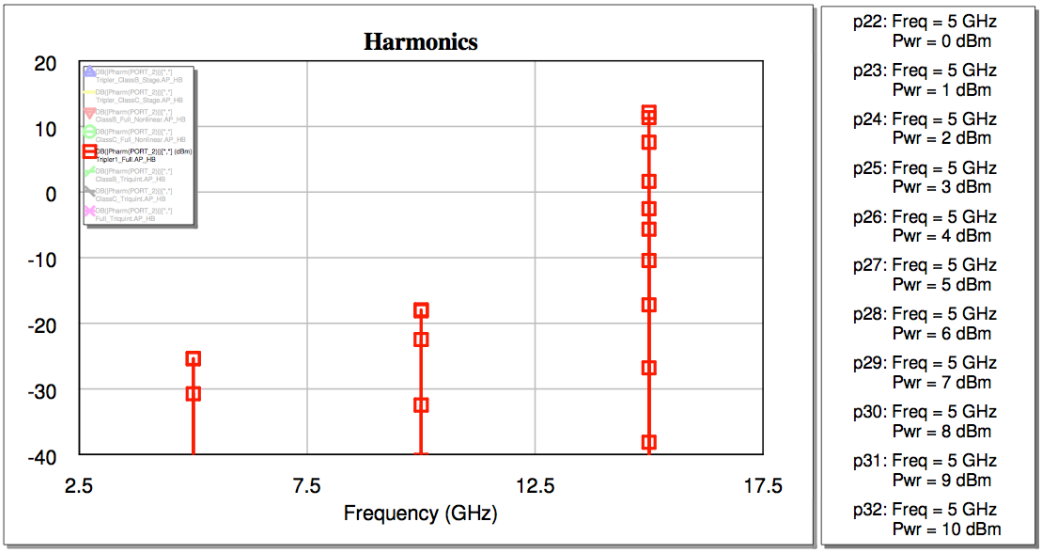
Conversion Gain	> -3dB
2nd Harmonic – Fundamental Isolation	> 20dB
2nd Harmonic – 1st Harmonic Isolation	> 20 dB
Stability	Unconditionally Stable

[1] Mingquan Bao, Rumen Kozhuharov, Herbert Zirath, *A High Power-Efficiency D-Band Frequency Tripler MMIC With Gain Up to 7dB* (IEEE Microwave and Wireless Components Letters, Vol. 24, No. 2, Feb 2014)

Design Approach:

Initially, a simple harmonic balance simulation was run with a pair of 4x50um FETs. The first stage was biased in a class-B configuration with V_{GS1} = -0.8, V_{DS1} = 1V, and was unconditionally stabilized with a series resistor of 120 ohms and a shunt resistor of 500 ohms. The second stage was biased in a class-C configuration with V_{GS2} = -1.0V, V_{DS2} = 4.0V, and was already unconditionally stable. In addition, an LC resonator at the output of the class-C stage was constructed using ideal elements, with L = 0.05nH and C = 2.25pF. This initial design contained no input or output matching networks, but still produced strong results that served as a benchmark to meet when introducing the non-ideal elements and the transmission line interconnects. The results of this initial simulation are shown below:

Figure I: Initial Harmonic Simulation Results



The initial simulation provides a conversion gain of 1.7dB for a 10dBm input (P_{3f0} = 11.7dBm), and has greater than 20dB isolation from the 2nd harmonic to both the 1st harmonic (P_{2f0} = -18.8dBm) and to the fundamental (P_{f0} = -26.2dBm). The isolation values are also measured for an input of 10dBm.

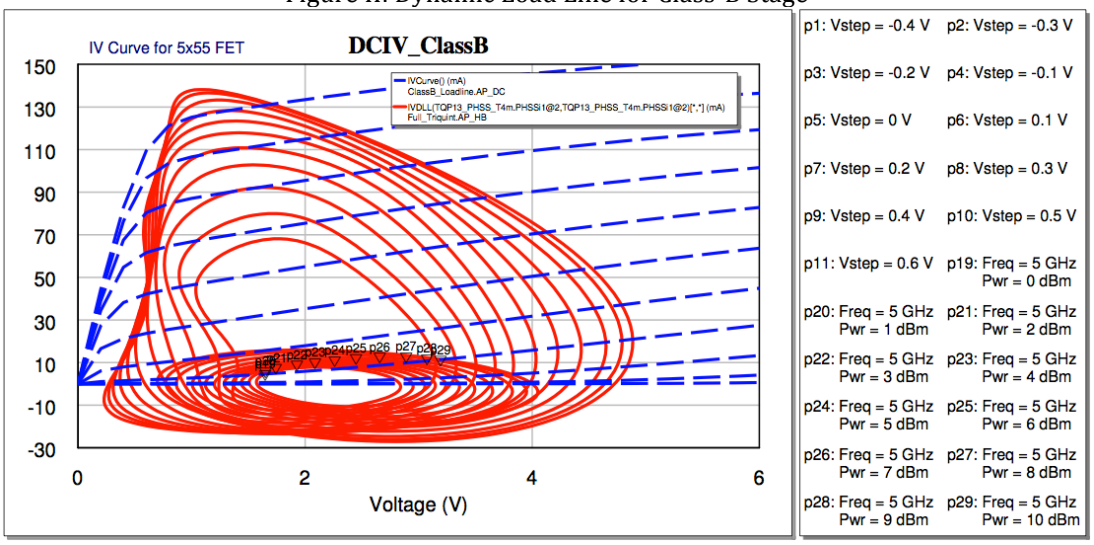
Once this initial design was tested and the performance verified, the non-ideal components were added and the physical layout began to take shape. The class-B and class-C stages were first designed and tested separately, while attempting to match the performances of the individual stages in the initial simulations. Once the non-ideal components were installed and the matching networks were completed, the two stages were combined and the inter-stage matching network was simplified. Finally, the physical interconnects were designed in an iterative fashion, so that each change to the physical layout was met with a change in component sizing to maintain the desired performance. During this process, the transistor sizing and bias were also altered to optimize performance due to the non-idealities introduced by the Triquint components and physical layout.

Class-B Stage Design:

The input stage of the frequency tripler is designed to take in a 5GHz signal, and, using a bias at or near the cutoff of the FET, produce a harmonic-rich output. Since the desired 2nd harmonic is far weaker than the fundamental, this stage needs to produce a fair amount of gain, and the input should be designed to match 50 ohms at 5GHz. I found that, as expected, adding non-linear Triquint components helped improve stability, so I was able to reduce the size of the stabilizing resistor down to a single series resistor of 35 ohms. This in turn increased the gain, which had the drawback of saturating the output of this stage. As the output of the 1st stage saturates, it becomes harder to maintain the isolation between the 2nd harmonic and the other frequency components. To mitigate this, I increased the size of the FET from 4x50 to 5x55, and increased V_{DS1} from 1V to 2V. In turn, this allowed me to increase V_{GS1} from -0.8V to -0.4V and still stay biased in a class-B configuration.

The dynamic load line for the class-B stage of the tripler is shown below in Figure II.

Figure II: Dynamic Load Line for Class-B Stage



Class-C Stage Design:

The output stage of the frequency tripler is biased in class-C to increase the non-linear effects of the FET, so that it both amplifies the 2nd harmonic, creates 2nd harmonic components from the fundamental and 1st harmonic, and also creates inter-modulation components from the lower harmonics at the 2nd harmonic. The input match is therefore designed to be fairly broadband, but the output match is designed to be narrowband around 15GHz.

The most critical portion of this stage is the resonant LC tank circuit at the output, which is designed to resonate at the desired frequency of 15GHz. In the initial design, this was constructed using a 0.05nH inductor and a 2.25pF capacitor (both ideal). However, creating a physical inductor at that value with the TQP13 components is impossible due to the physical constraints, and using a simple piece of transmission line proved to be difficult. It was therefore necessary to redesign

the resonant circuit, which had to be realizable in layout and provide a parallel resonance (ie cross the Smith Chart's real axis) at 15GHz. The finalized resonator layout and simulation are shown below in Figures III and IV.

Figure III: Finalized Resonator Layout

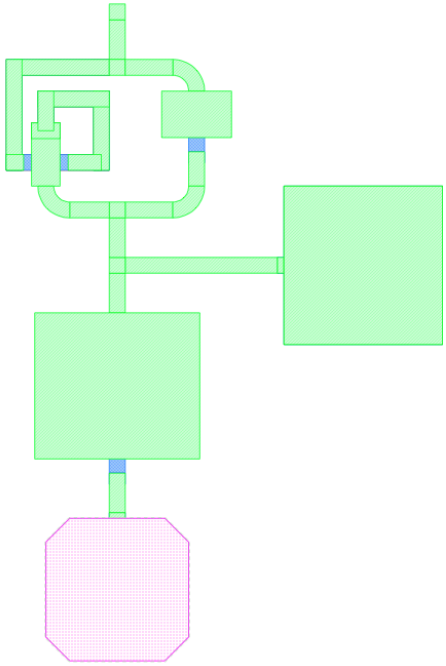
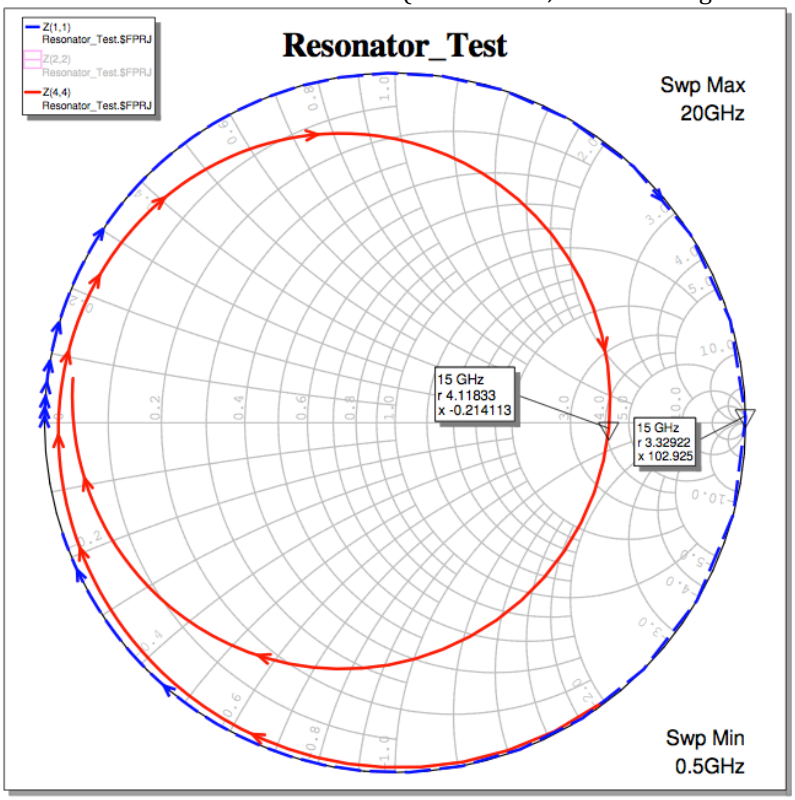


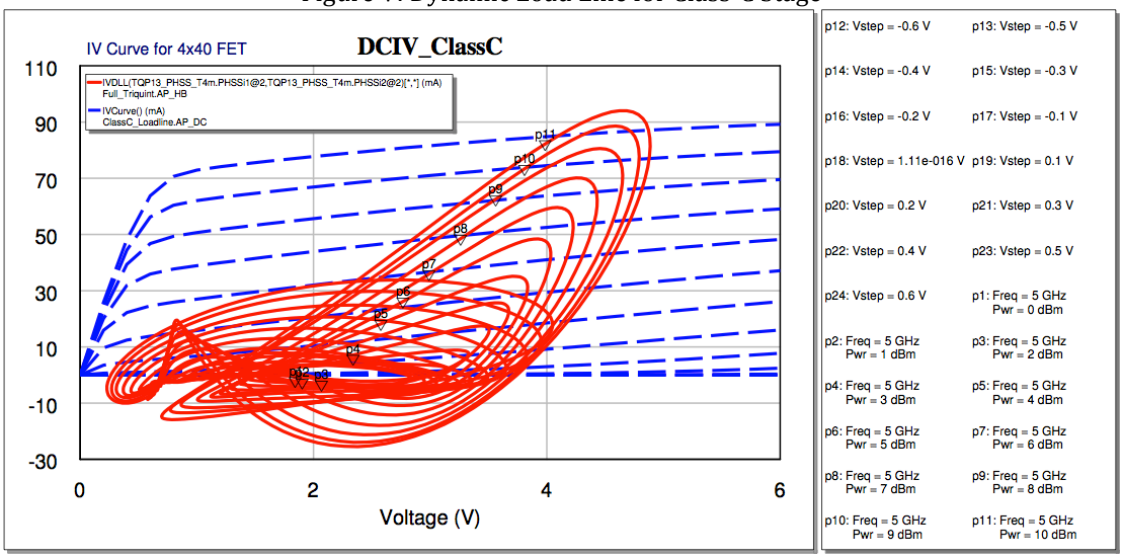
Figure IV: Finalized Resonator Smith Chart (blue is ideal, red is redesigned resonator)



Due to the alterations in the resonator, as well as losses introduced by the non-ideal Triquint elements, the FET sizing for the second stage was changed from 4x50 to 4x40 to introduce a bit more gain. Due to the changes in the inter-stage match, a 400ohm shunt resistor was installed to introduce and isolate the DC bias at V_{GS2} from the RF signal. The bias conditions stayed almost identical, as the only alteration was changing V_{GS} to -1.0V from -1.1V. The output match was designed to provide a high-pass resistor with a cutoff frequency around 12-14 GHz (this value changed as I tuned for the output match), and the output match is quite strong, with S_{22} = -25.55 at 15GHz.

The dynamic load line for the class-C stage of the tripler is shown below in Figure V.

Figure V: Dynamic Load Line for Class-C Stage



Simulated Results:

The simulated results for the full circuit are shown below in Figures VI-X. The simulations were run in Microwave Office using the TQP13 library from Triquint. The figures below show a linear simulation to determine the S-Parameters of the tripler (Figure VI), and harmonic balance simulations to determine the output harmonic components (Figures VII and VIII) and to determine the conversion gain (Figure IX). The dashed lines show the results of the initial simulations (ideal components), and the solid lines denote the simulations run with the TQP13 components. Figure X shows the stability of the overall circuit for the given bias values. The circuit was also proven unconditionally stable for V_{GS} = 0, to ensure stability even give some bias drift.

Figure VI: S-Parameters for Full Frequency Tripler

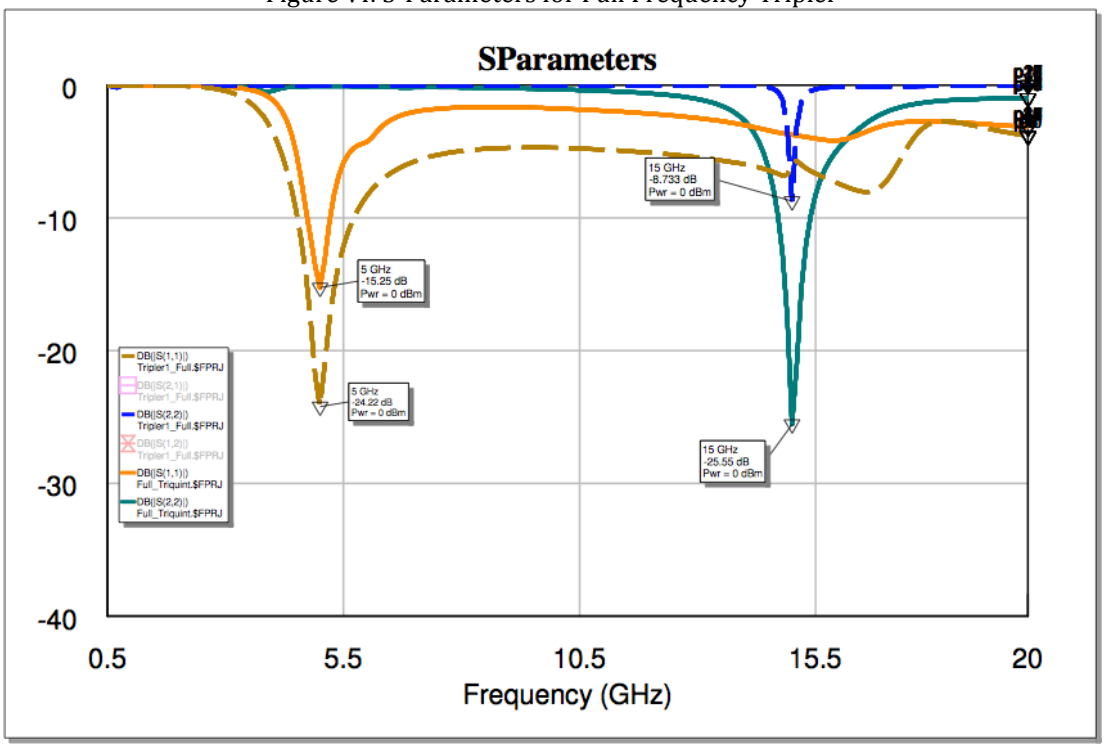


Figure VII: Output Harmonic Components

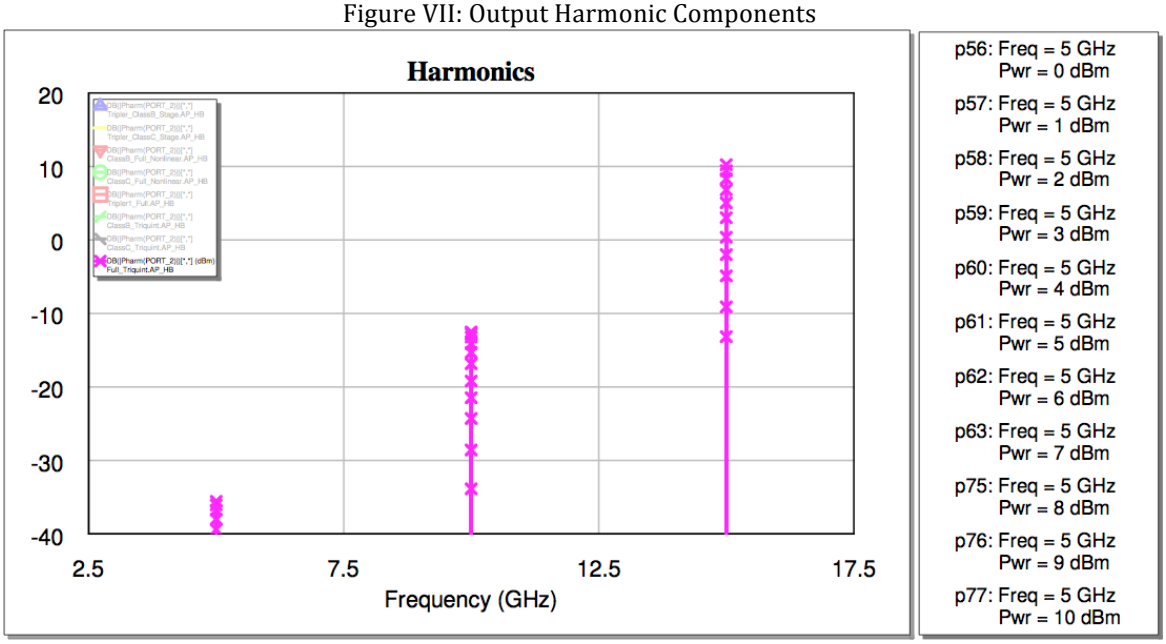


Figure VIII: Pout vs Pin for f_0, $2f_0$, $3f_0$

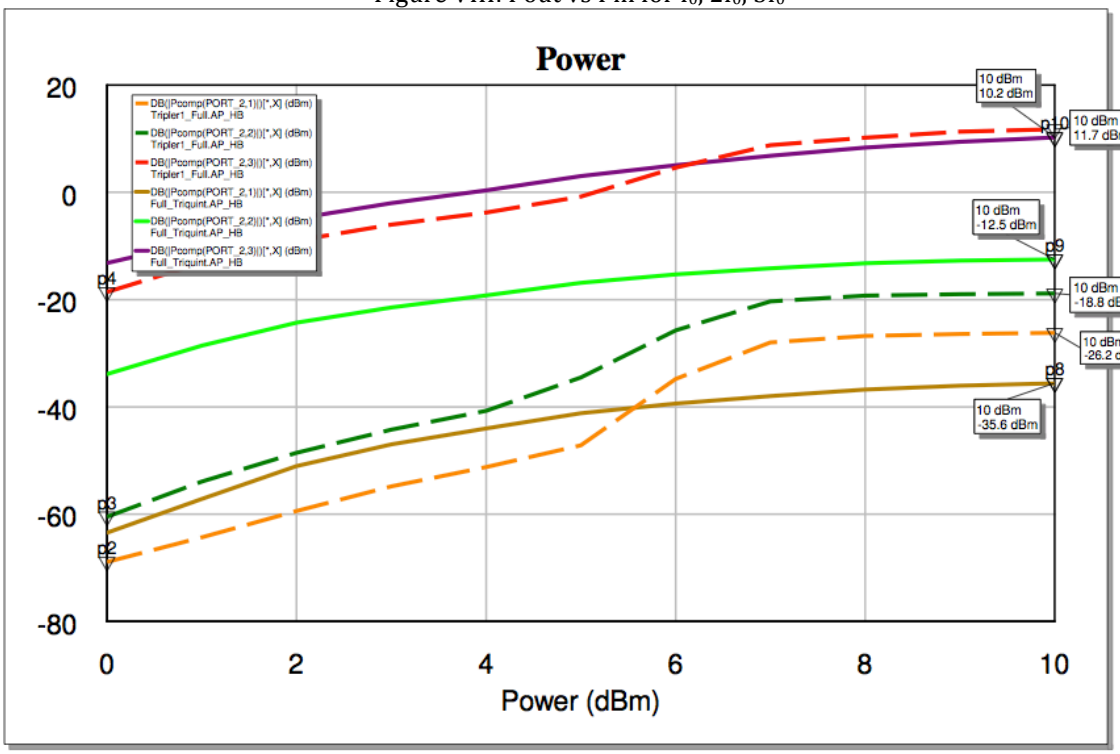


Figure IX: Conversion Gain for f_0, $2f_0$, $3f_0$ vs Pin

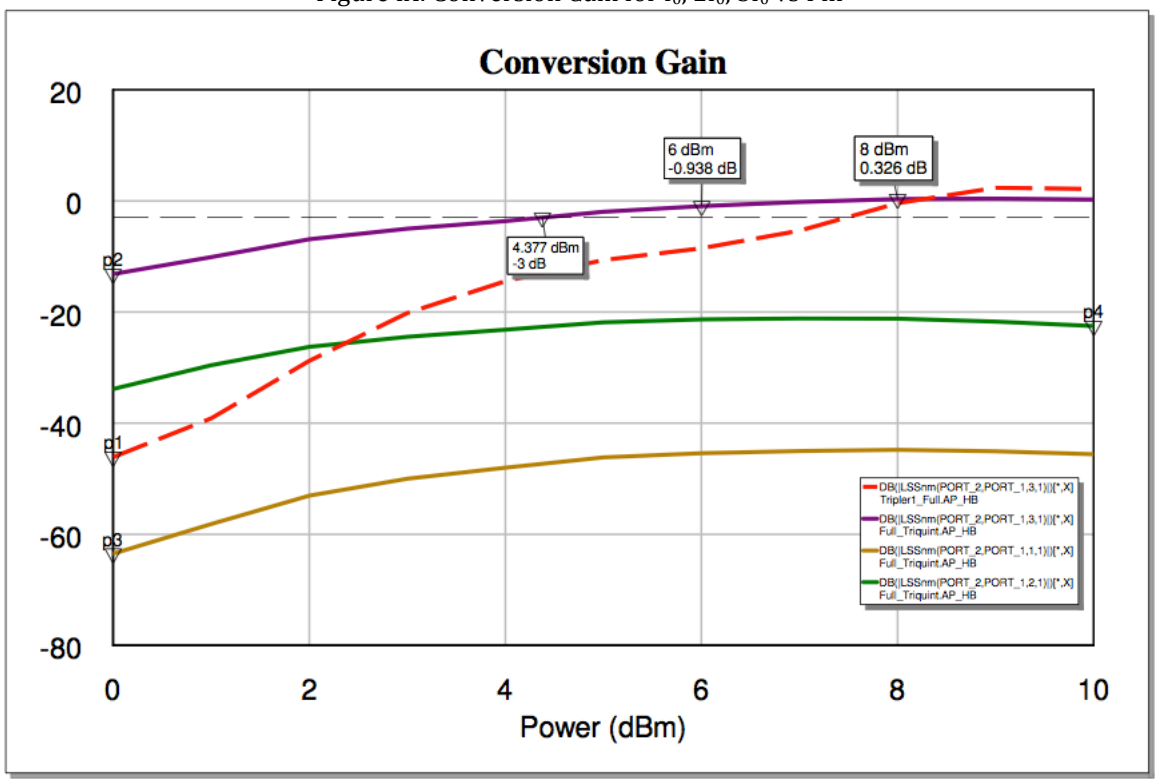
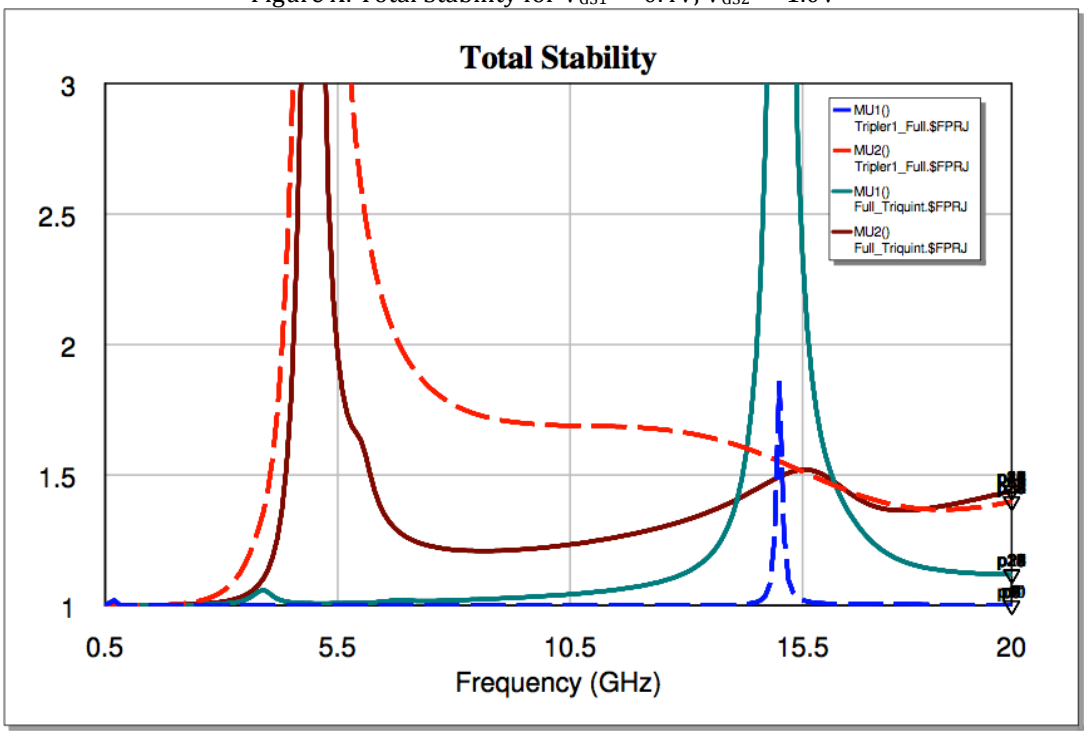


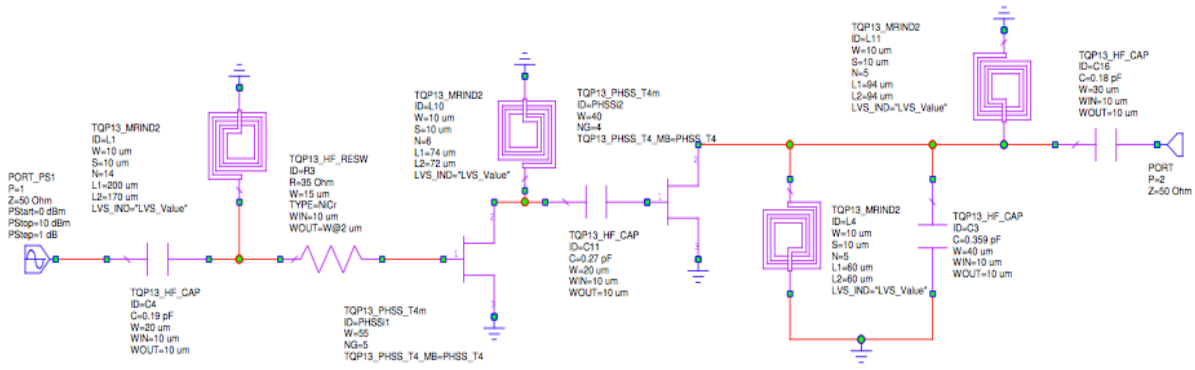
Figure X: Total Stability for V_{GS1} = -0.4V, V_{GS2} = -1.0V



RF Schematic:

Shown below in Figure XI is a simplified RF schematic of the frequency tripler, with the interconnects and the DC bias components removed.

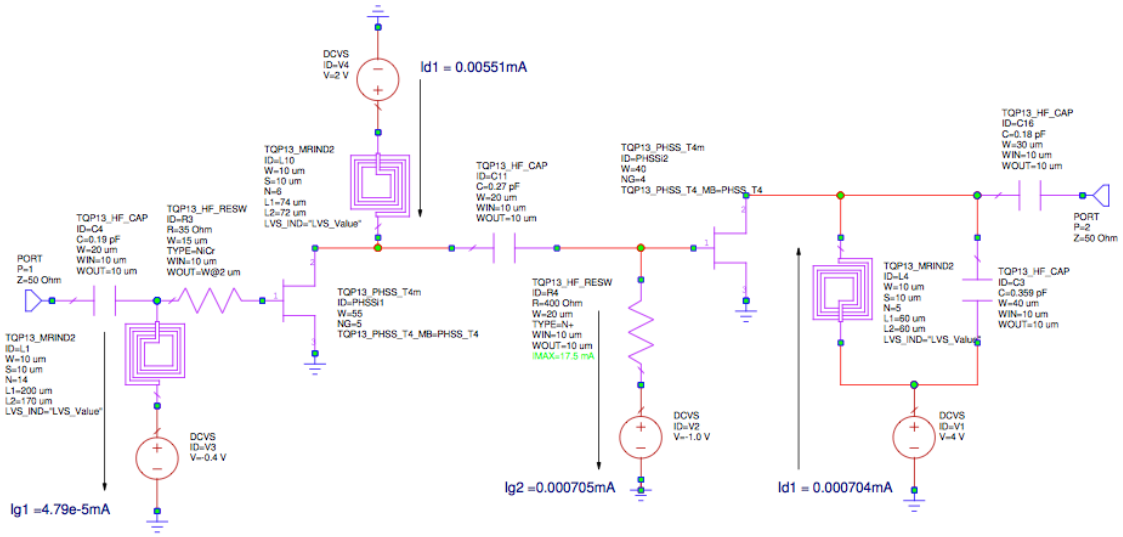
Figure XI: RF Schematic of Frequency Tripler



DC Schematic:

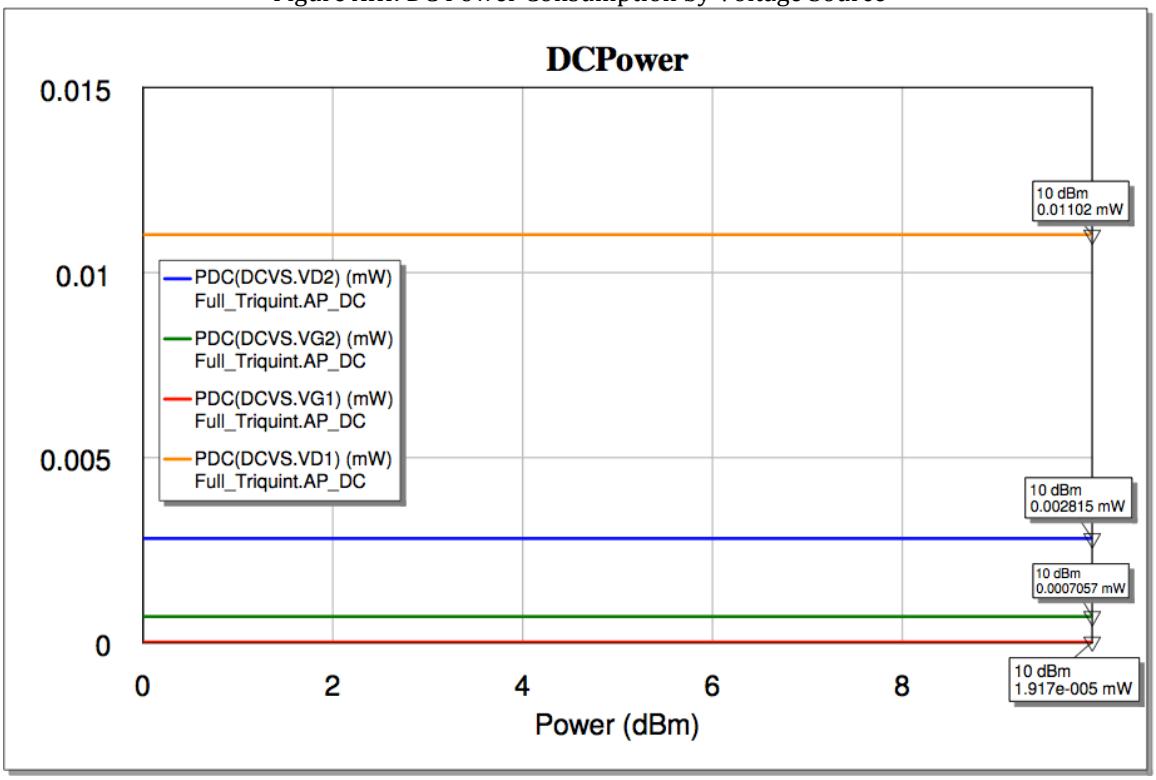
Shown below in Figure XII is a simplified DC schematic of the full circuit, which shows the DC bias components. The interconnects and matching elements that are not used for DC biasing have been removed.

Figure XII: DC Schematic for Frequency Tripler



The DC currents are copied from the annotated version of the full tripler (with TQP13 components and interconnects). The total DC consumption is 0.015mW (-18.2dBm), and the breakdown of DC power consumption is shown in Figure XIII below.

Figure XIII: DC Power Consumption by Voltage Source



Full Schematic and Layout:

The finalized schematic and layout are shown below, in Figures XIV and XV.

Figure XIV: Finalized Schematic of 5GHz Frequency Tripler (Input at Top)

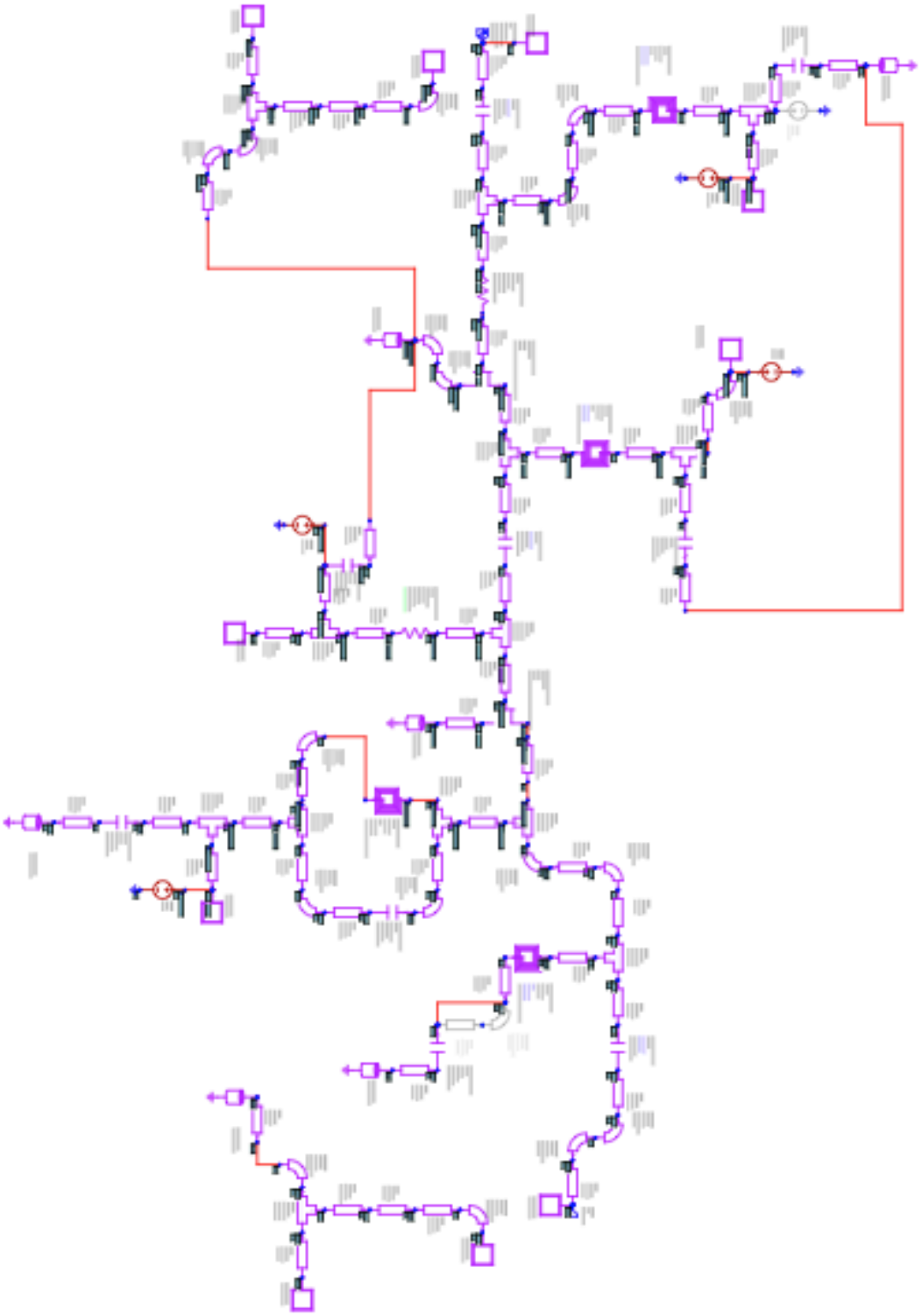
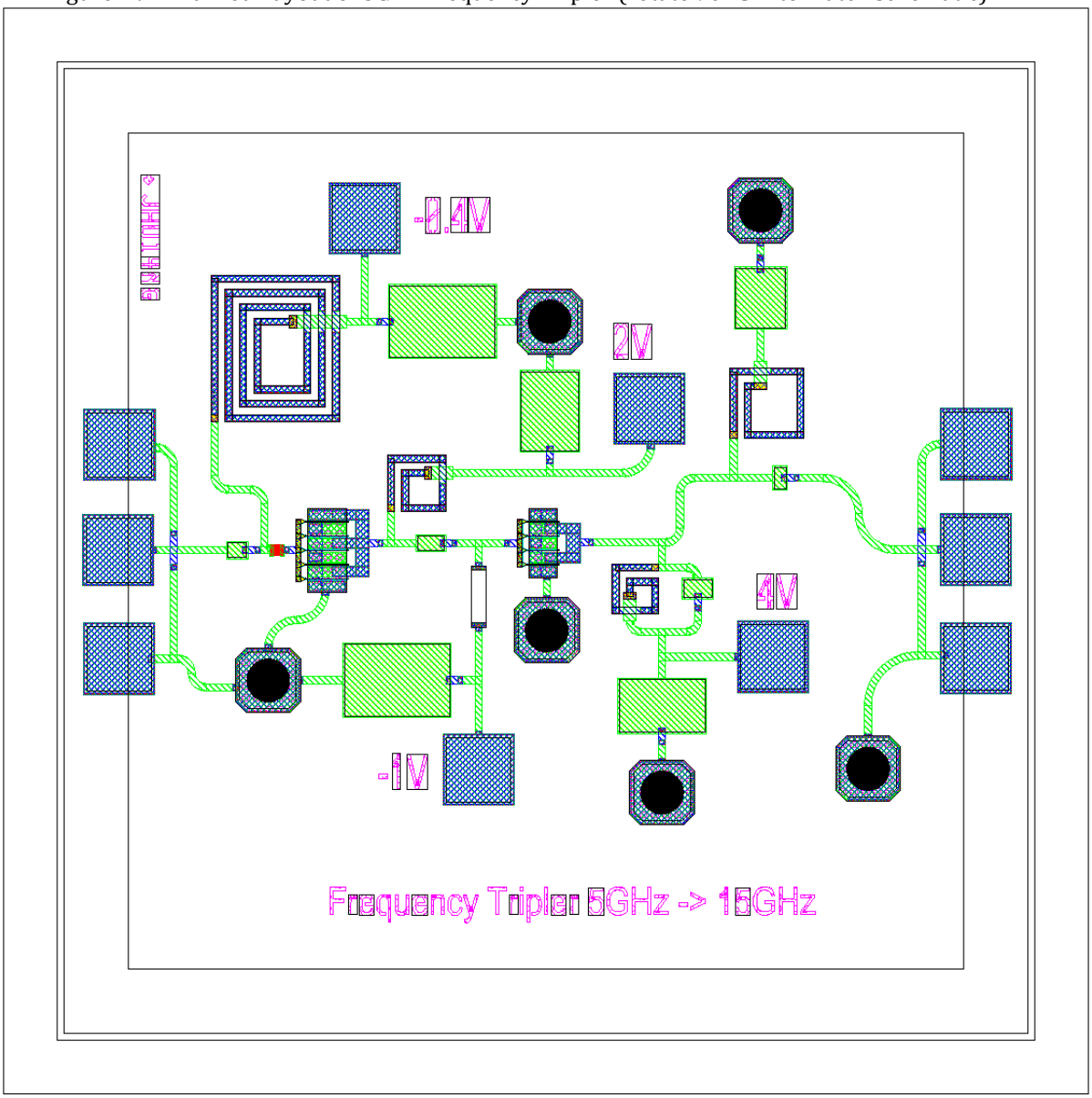


Figure XV: Finalized Layout of 5GHz Frequency Tripler (rotate 90° CW to match schematic)



Test Plan:

In order to test the frequency tripler, the following equipment is necessary: four DC power supplies, a network analyzer, and a spectrum analyzer (which should also have an RF signal generator).

Determining the S-Parameters:

1. Apply V_{G1} = -0.4V, V_{G2} = -1.0V to the appropriate gate pads.
2. Apply V_{D1} = 2.0V, V_{D2} = 4.0V to the appropriate drain pads and monitor the current on the drain supplies. The current draw should be minimal.
3. Calibrate the network analyzer.
4. Connect the GSG probes out of the network analyzer to the RF input and RF output.

5. Measure S_{11} and S_{22} and compare to the simulated data.

Testing the Tripling Effect

1. Leave the gate and drain voltages connected as before.
2. Connect the output of the RF signal generator to the RF input of the design and set the frequency to 5GHz.
3. Connect the input of the signal spectrum analyzer to the RF output of the design.
4. Sweep the input power from -10dBm to +10dBm in 1dBm steps, and compare to the simulated results.
5. Fill in the table below (Table II).

Table II: Test Plan for 5GHz Frequency Tripler

Pin (dBm)	Pout (dBm)	Adj. Pin (dBm)	Adj. Pout (dBm)	Gain (dB)
-10				
-9				
-8				
-7				
-6				
-5				
-4				
-3				
-2				
-1				
0				
+1				
+2				
+3				
+4				
+5				
+6				
+7				
+8				
+9				
+10				

Summary and Conclusions:

A two-stage 5GHz frequency tripler was designed and laid out using the Triquint process. The most challenging part of the design was dealing with the introduction of the TQP13 components and physical interconnects, especially in the resonator. However, these obstacles were overcome, and the design meets the specifications laid out at the beginning of the paper. The simulated results are summarized and compared to the desired specifications in Table III below.

Table III: Simulated Results vs Specifications

Parameter	*Desired Specification*	*Final Simulated Result*
Conversion Gain	> -3dB	0.2 dB for P_{in} = 10dBm. > -3dB for P_{in} > 4.377dBm

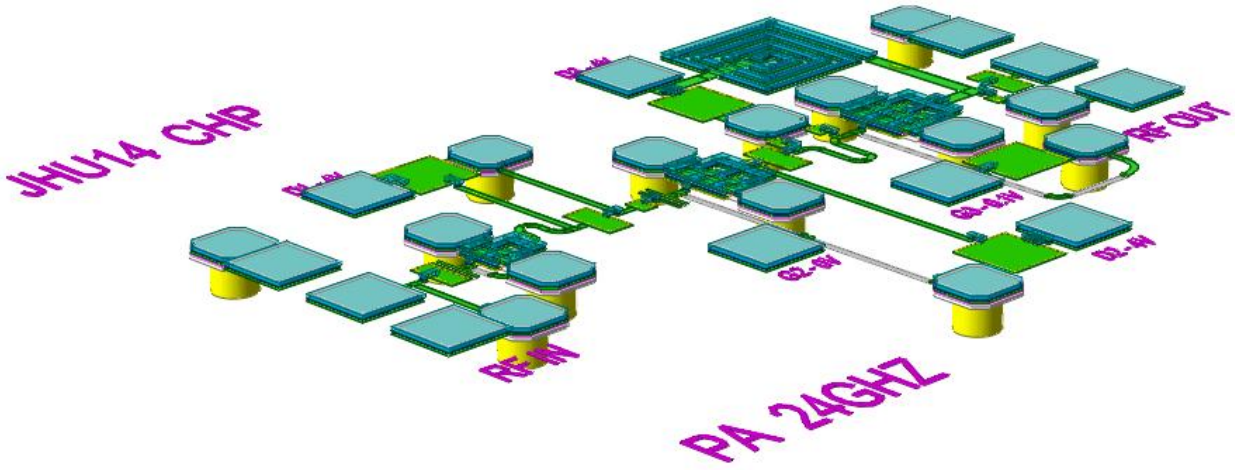
2^{nd} Harmonic – Fundamental Isolation	> 20dB	22.7dB for P_{in} = 10dBm
2^{nd} Harmonic – 1^{st} Harmonic Isolation	> 20 dB	45.8dB for P_{in} = 10dBm
Stability	Unconditionally Stable	Unconditionally Stable

24 GHz Three-Stage Power Amplifier

Chris Pickett

Johns Hopkins University

525.787 MMIC Design, Fall 2014



Abstract

The Triquint TQP13, 0.13um pHEMT process is used to create a three stage amplifier operating at 24GHz. The amplifier is designed for operation in the ISM band, 24-24.25GHz. Three stages give the amplifier 20dB of gain and 20dBm of output power using a 4V supply. Nonlinear simulations show that this design meets the requirements. A layout was designed to fit the circuit on a 1500 x 1500um GaAs MMIC.

Introduction

The goal of this design is to create a power gain block that can be used in 24GHz ISM band applications. The primary design goal is 20dBm P1dB, which makes this amplifier a good power stage for any low power system operating at 24GHz. The design goal of 20dB small signal gain allows this amplifier to be used without a driver stage. Input and output return loss goals are 20dB and 10dB, respectively. The output return loss is going to be a function of the transistor's optimum power match, so meeting the specification is less critical. The input return loss is more critical to present a good match to the previous element in the system. Other parameters, such as noise figure and efficiency, do not have design goals and will not be optimized in this design.

Design Approach

Triquint's TQP13 process defines a default 300um (6x50um) depletion-mode pHEMT, but the device size (number of gate fingers and finger length) can be changed to suit different applications. Decreasing the device size decreases the drain bias current, which is advantageous in low noise applications. Conversely, this decreases the available output power. However, decreasing the size typically results in higher available gain, due to reduced parasitic capacitance. AWR's Microwave Office (MWO) and Triquint's TOM4 pHEMT model were used to simulate and evaluate different size devices for their use in gain and power stage applications. The overall design process for a single stage is summarized below.

1. Using MWO, plot DCIV and Gain curves for various size transistors. Select a transistor size that meets the gain and output power requirements for the stage.
2. Assess stability by plotting Mu1 and Mu2 over the frequency range 1-30GHz.
3. Add series and/or shunt resistors to the gate to increase stability. Weigh stability vs. gain tradeoff.
4. Add input and output matching circuits.
5. Verify and tune the design using ideal elements and ideal interconnect.
6. Replace ideal elements with Triquint elements. Retune and verify design still operates as desired.

In the design process, various device sizes and matching techniques were tested in order to arrive at a final configuration of device size, matching, and number of stages required to achieve the design goals. This report details only the three stages used in the final cascade design. The following sections detail each stage individually to show how each stage contributes to the overall circuit.

Gain Stage Design

For the first stage in the amplifier, high gain, and good match on the input and output are most important. Higher gain on the first stage will allow later stages to sacrifice gain for output power. For the first stage a 160um (4x40um) device was used. The smaller device provides higher gain at the expense of output power. Figure 1 shows the DCIV curves and the DC bias point for this stage.

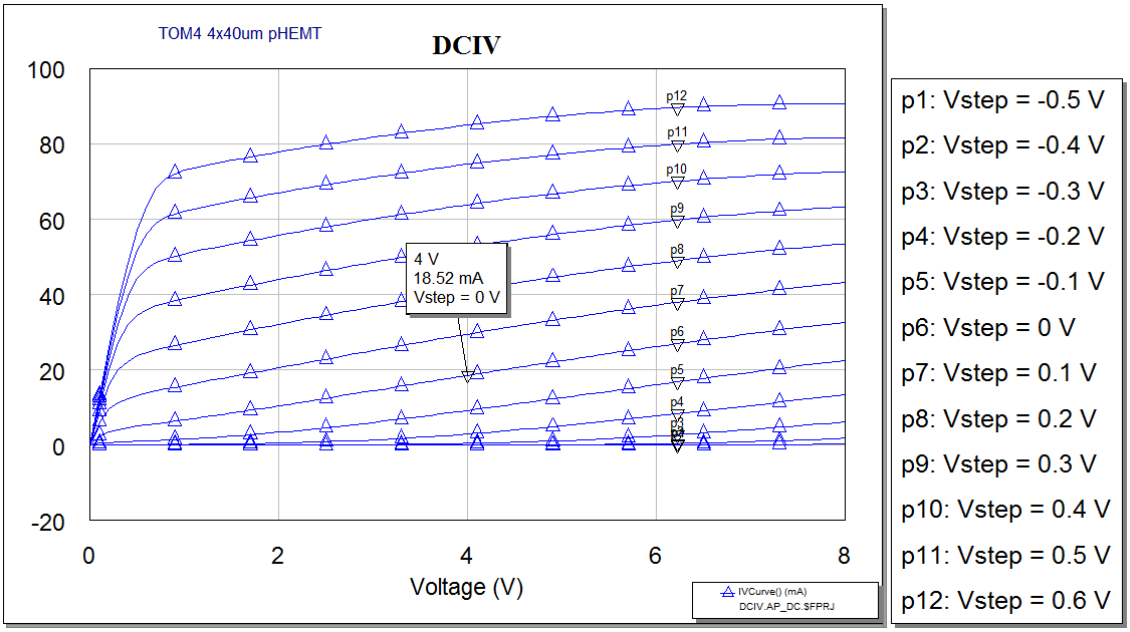


Figure 1. 4x40um pHEMT IV Curves and DC Bias Point

A simultaneous conjugate match (SCM) technique was used to get maximum gain out of the device with good input and output match. Stabilization of the device across a wide frequency range, 0 – 30 GHz, was achieved with a series and shunt resistor on the gate. A low shunt resistance was required to achieve unconditional stability across the full range of frequency, due to the high gain of the device. However, this caused an undesirable loss in gain. As a result, conditional stability was accepted at the lower frequencies in exchange for higher gain. The reasoning is that the loss added by using Triquint elements instead of ideal elements and microstrip lines instead of ideal interconnects will stabilize the amplifier across all frequencies. After the device was stabilized, input and output gain circles were plotted on a Smith chart. These circles gave the impedance that the input and output matching circuits should present to the device for maximum gain. A Smith chart program was used to design simple two-element matching circuits, as this is a narrowband application. Ideal inductors and capacitors were used for initial verification, and then Triquint elements were substituted. The inductance values were so small that microstrip lines were employed instead of spiral inductors. Lengths were calculated using the rule of thumb 1ph/um of 10um wide microstrip line. The substrate vias have about 25pH of inductance so those had to be accounted for where used. Figure 2 shows the schematic of this stage with Triquint elements and ideal interconnect.

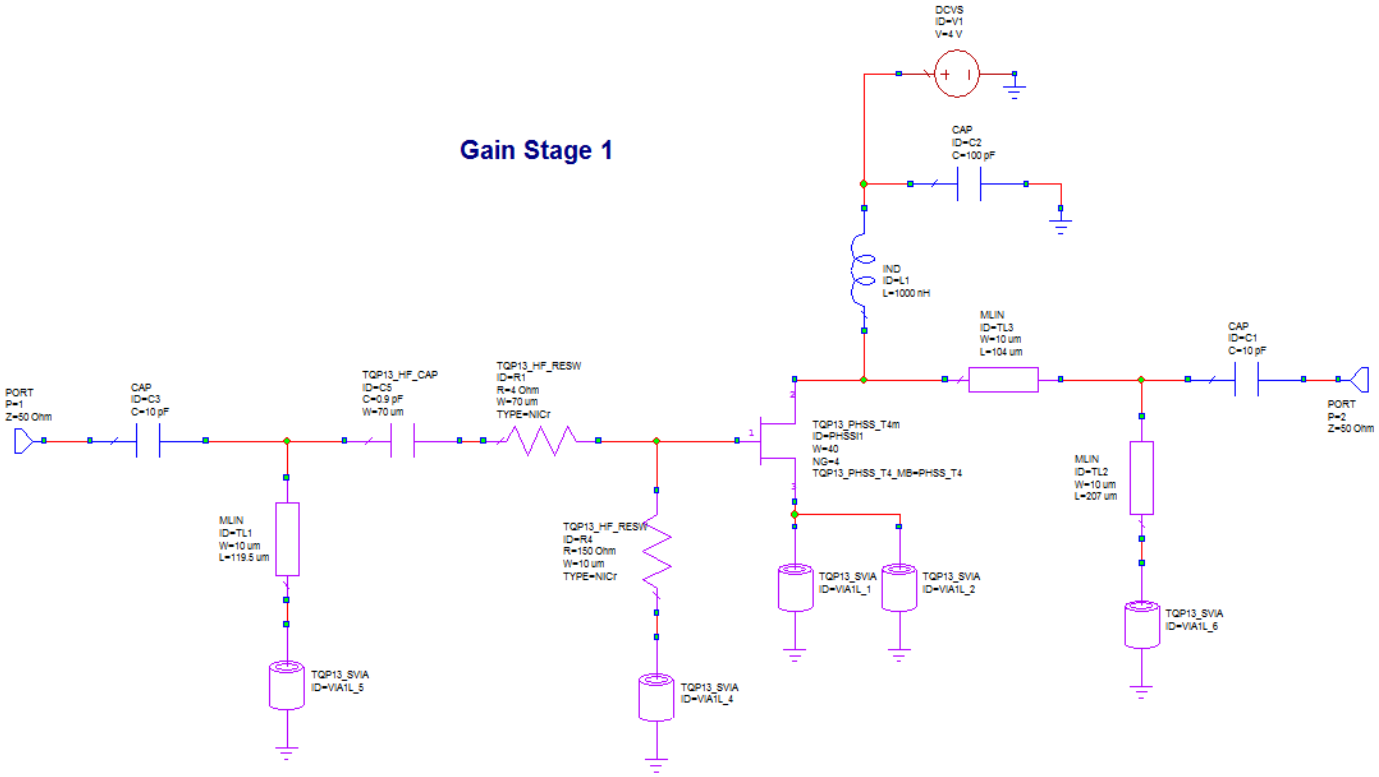


Figure 2. Schematic, Gain Stage, Triquint Elements

Figure 3 shows good input and output match, and a gain of 10dB at 24GHz. The dotted lines are the match and gain of the circuit using ideal elements. The solid line shows the gain and match of the circuit using Triquint elements.

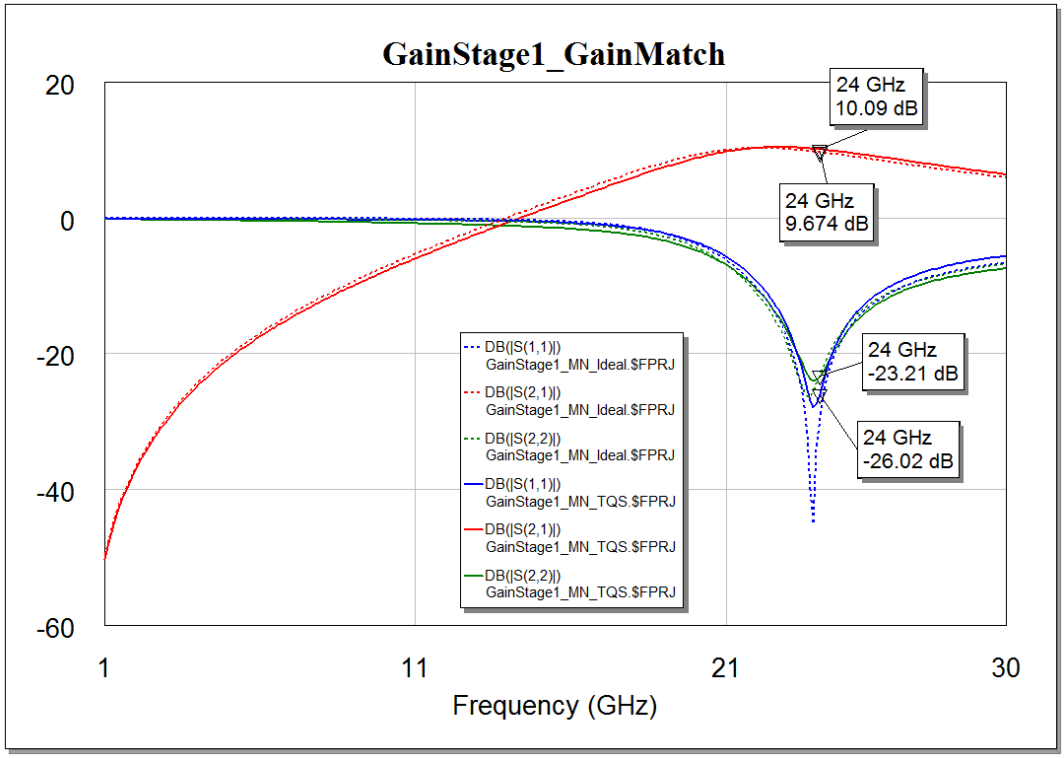


Figure 3. Small Signal Gain, Input Return Loss, Output Return Loss

Figure 4 shows that while the circuit was conditionally stable initially, the circuit is unconditionally stable using Triquint elements. This shows that no excess gain was wasted in the initial stabilization.

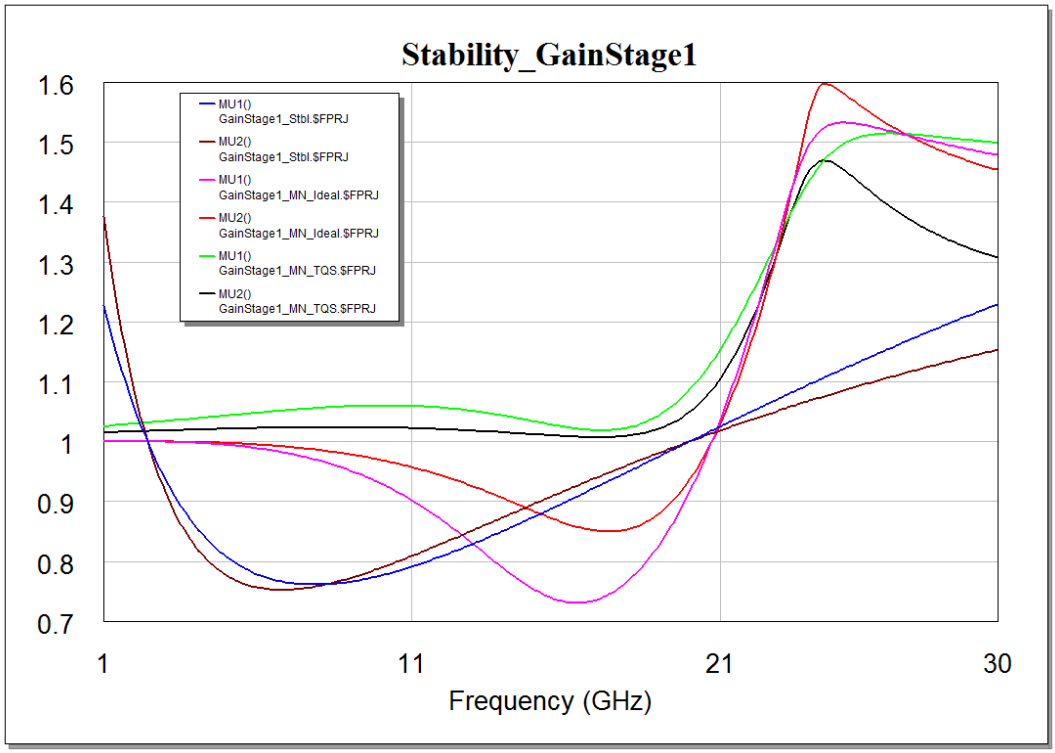


Figure 4. Stability, Gain Stage

Figure 5 shows the output power and gain of the device with input power levels from -20 to +20dBm. The approximate 1dB compression points are marked.

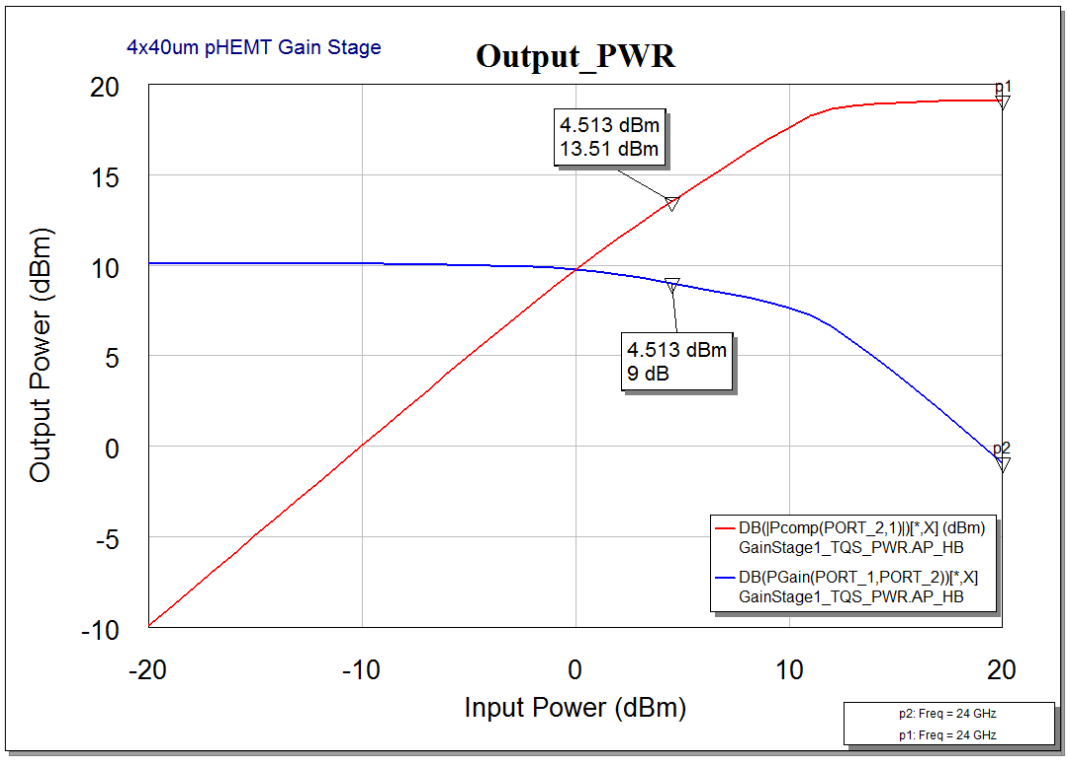


Figure 5. Output Power, Gain Stage

Power Stage 1 Design

For the second stage, a larger device was used in order to provide more output power. IV curves and a load line were used to approximate output power for various device sizes and bias points. The default 300um (6x50um) device was used, and the Cripps' method was used to match the output for maximum power. Figure 6 shows the IV curves and DC bias point for the device. The load line is shown in red. The Cripps resistance is calculated from the slope of the load line to be ~51.5Ω. This is the resistance for the output match. The reactance is given by measuring S_{22} of the stabilized and biased device. Once the output matching circuit is connected, the input is conjugate matched.

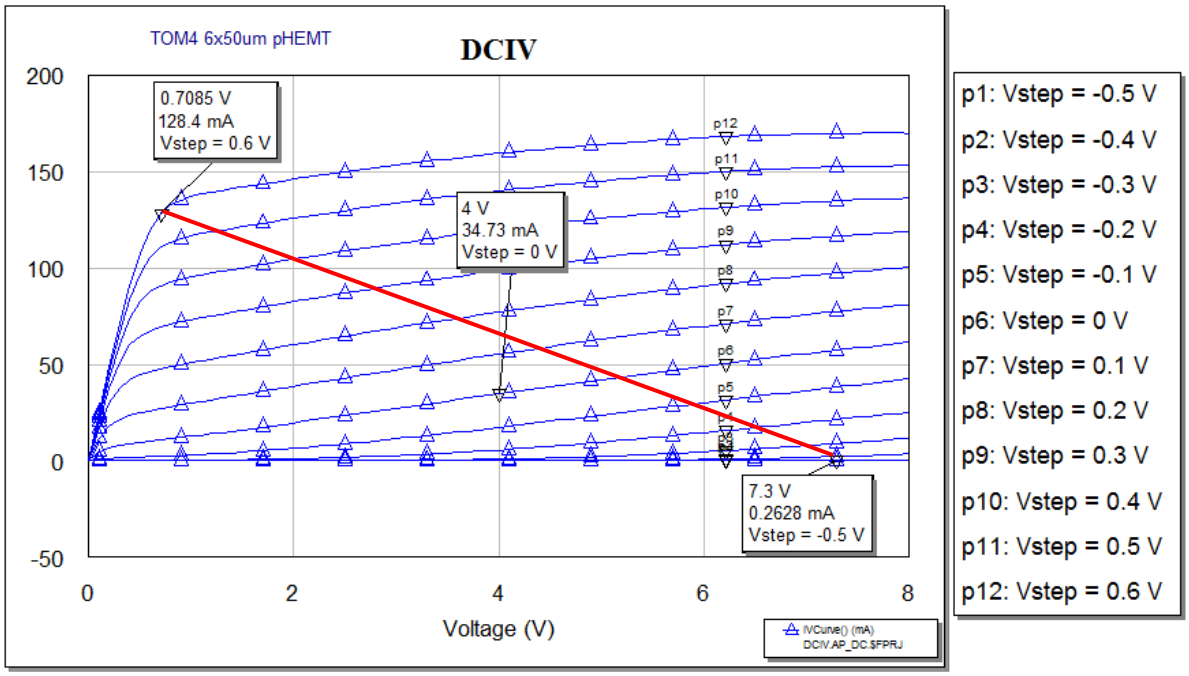


Figure 6. 6x50um pHEMT IV Curves and DC Bias Point

Figure 7 shows the schematic of this stage using Triquint elements and ideal interconnect.

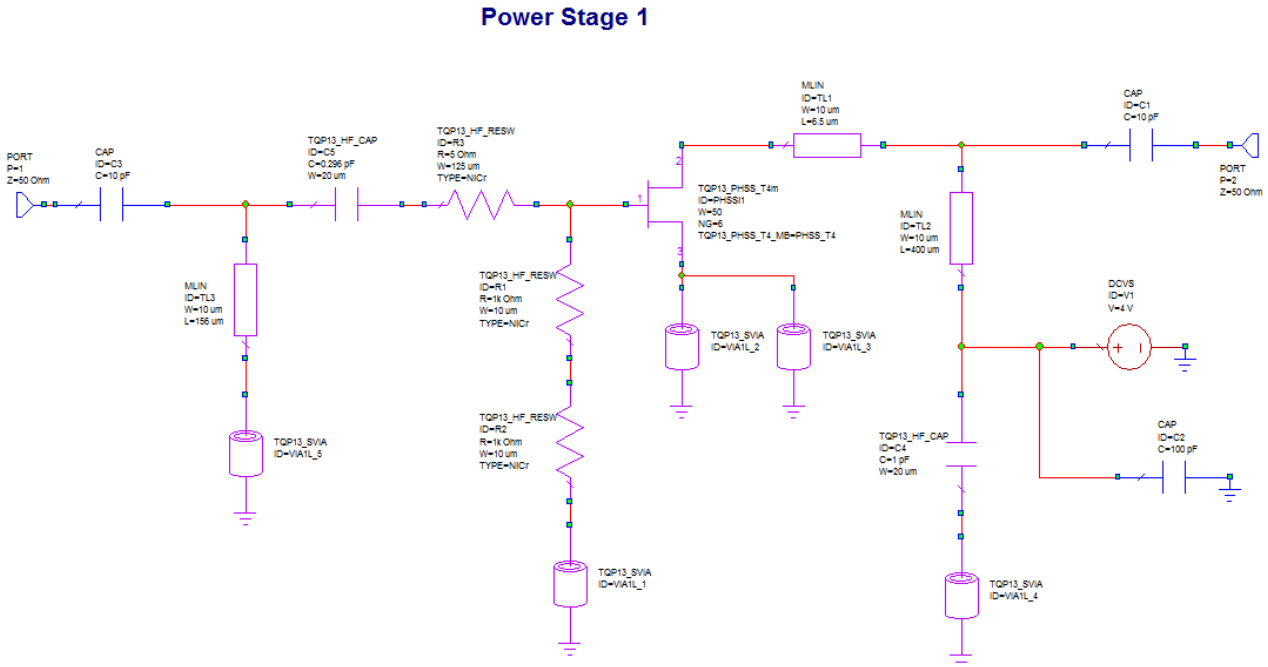


Figure 7. Schematic, Power Stage 1

Figure 8 shows the gain, input return loss, and output return loss. The small signal gain is lower than the first stage, but that is expected because of the larger device and the match for power. The output match is not great, but not bad considering that the device was matched for power.

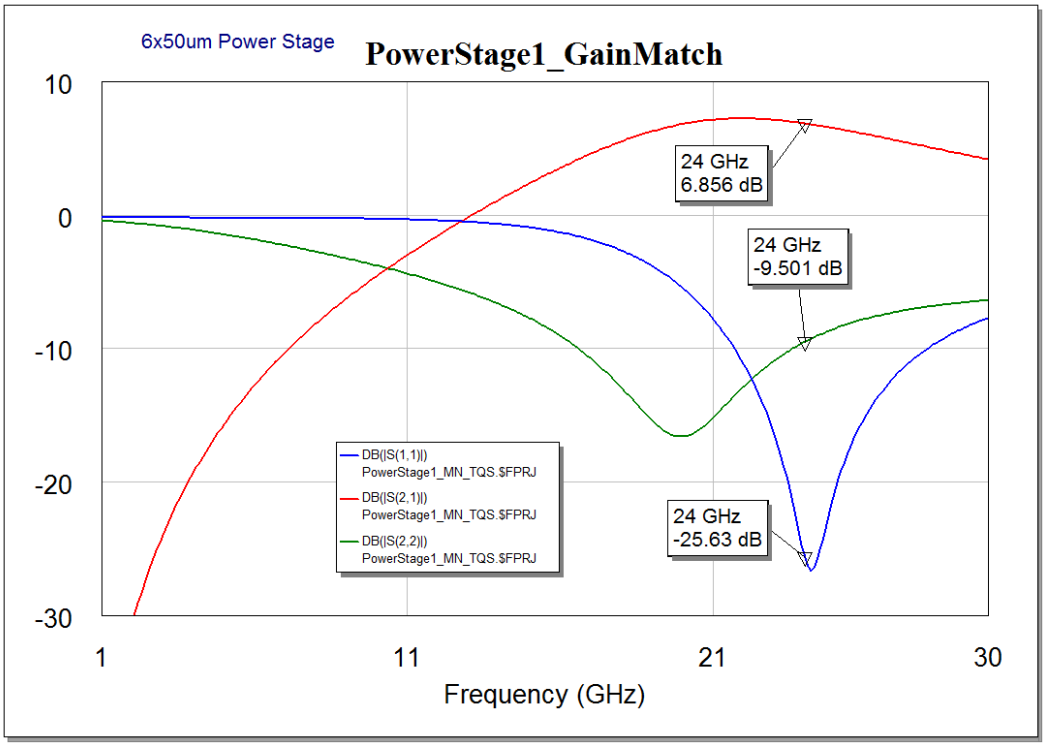


Figure 8. Small Signal Gain, Input Return Loss, Output Return Loss, Power Stage 1

Figure 9 shows that while the design was conditionally stable using ideal elements, once Triquint elements were substituted, unconditional stability was achieved.

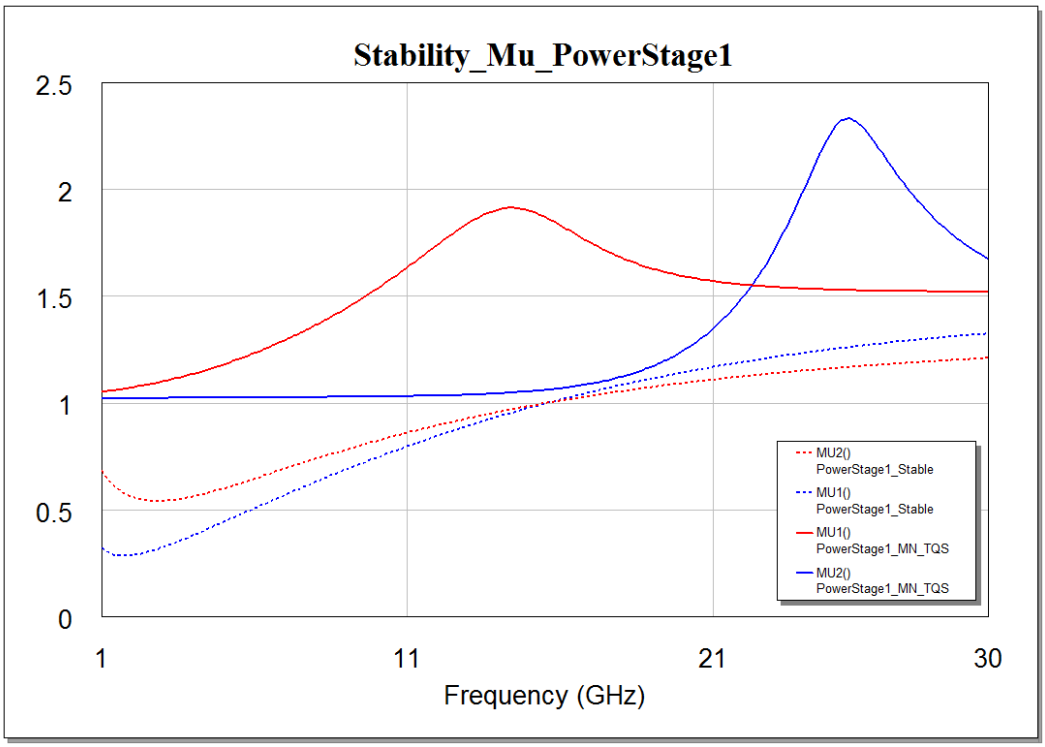


Figure 9. Stability, Power Stage 1

Figure 10 shows the output power and gain of the with input power levels from -20 to +20dBm. The simulation appears to have trouble converging between 15 and 16dBm input levels, which is, incidentally where the 1dB compression point seems to be. The approximate P1dB points are marked. This stage should operate in the linear region so the convergence error is not a large concern at this point.

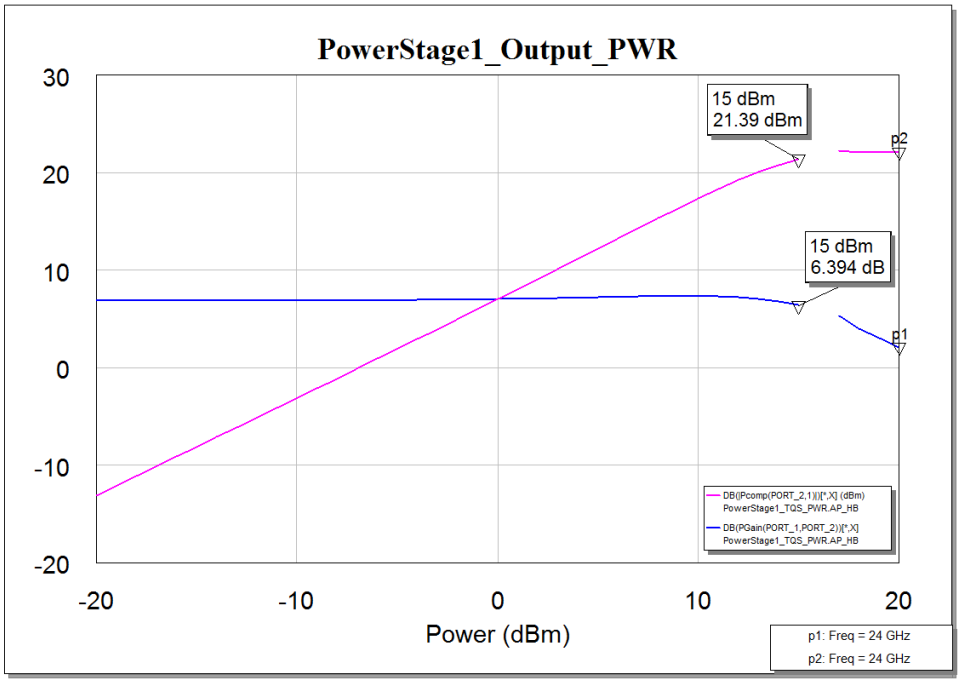


Figure 10. Output Power, Power Stage 1

Power Stage 2 Design

While the previous stage meets the requirement for 20dBm P1dB, the cascade gain of the first two stages is not high enough to meet the specifications, so a third stage is necessary. The cascade gain of the first two stages is about 17dB, so the last stage needs a minimum of 3dB to meet the requirement. With such a low gain requirement, a larger device can be used to get more output power without worrying about the consequent gain reduction. For the third stage a 450um (6x75um) device was chosen. Figure 11 shows the IV curves and DC bias point for the final stage. Notice the gate is biased at 0.1V to push the bias point closer to Class A operation and get a little more power out of this stage. The two previous stages used V_{GS} = 0V for ease of biasing. Again, the Cripps' method was used to match the output for power. The Cripps resistance is calculated to be approximately 34.4Ω as shown by the load line in figure 11. The final schematic using Triquint elements is shown in figure 12.

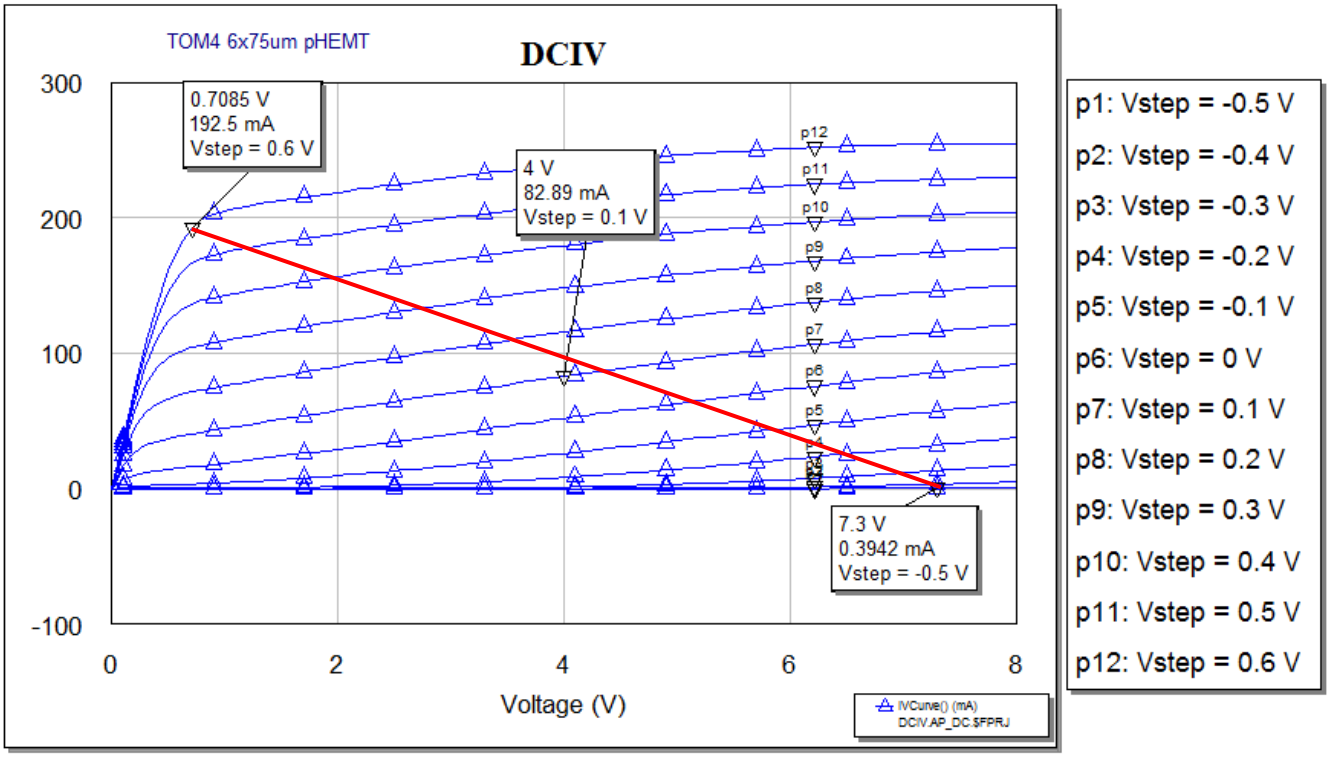


Figure 11. 6x75um pHEMT, IV Curves and DC Bias Point

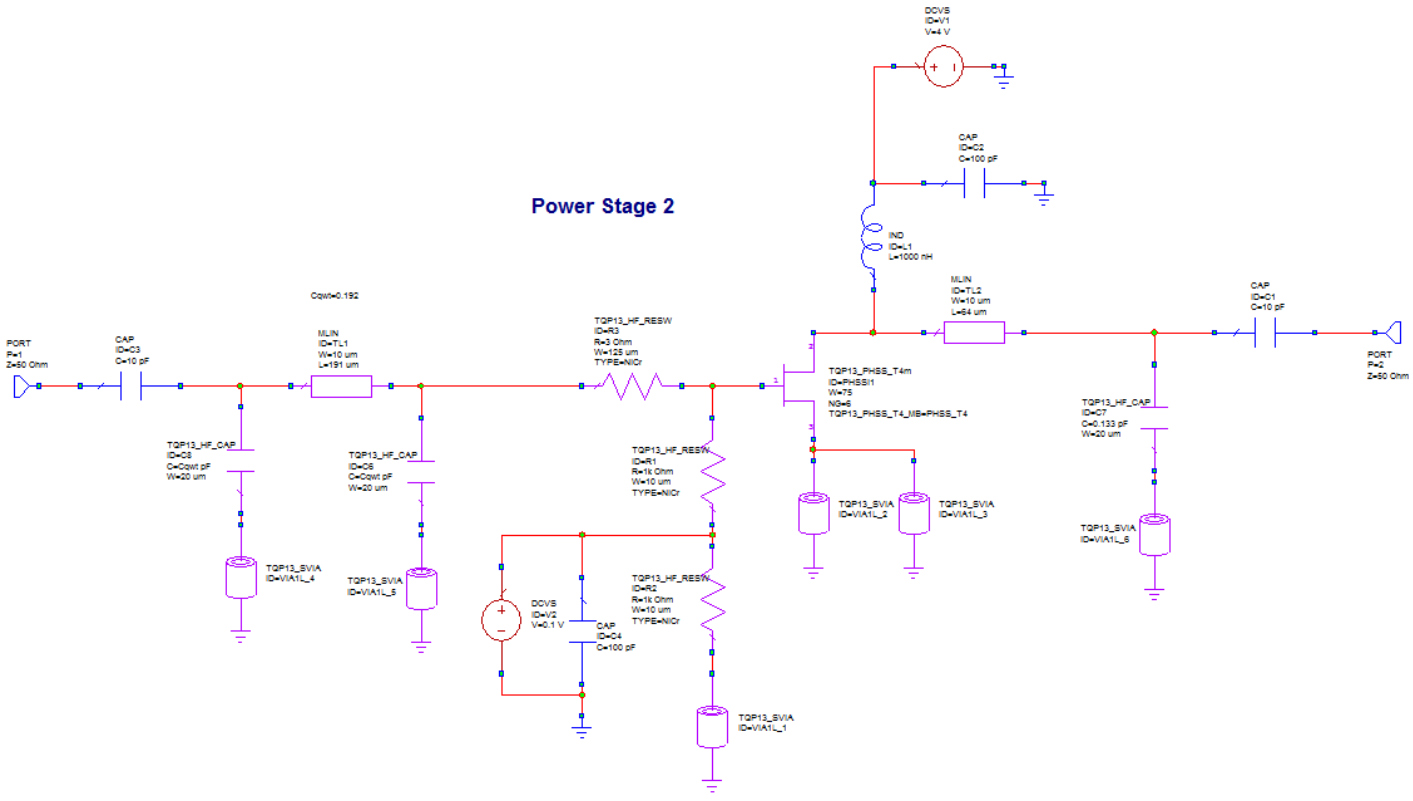


Figure 12. Schematic, Power Stage 2

Figure 13 below shows the small signal gain, input return loss, and output return loss. While the gain is low it meets the 3dB minimum requirement. The input presents a good match to the previous stage, and while the output match is not great, it is acceptable for this application.

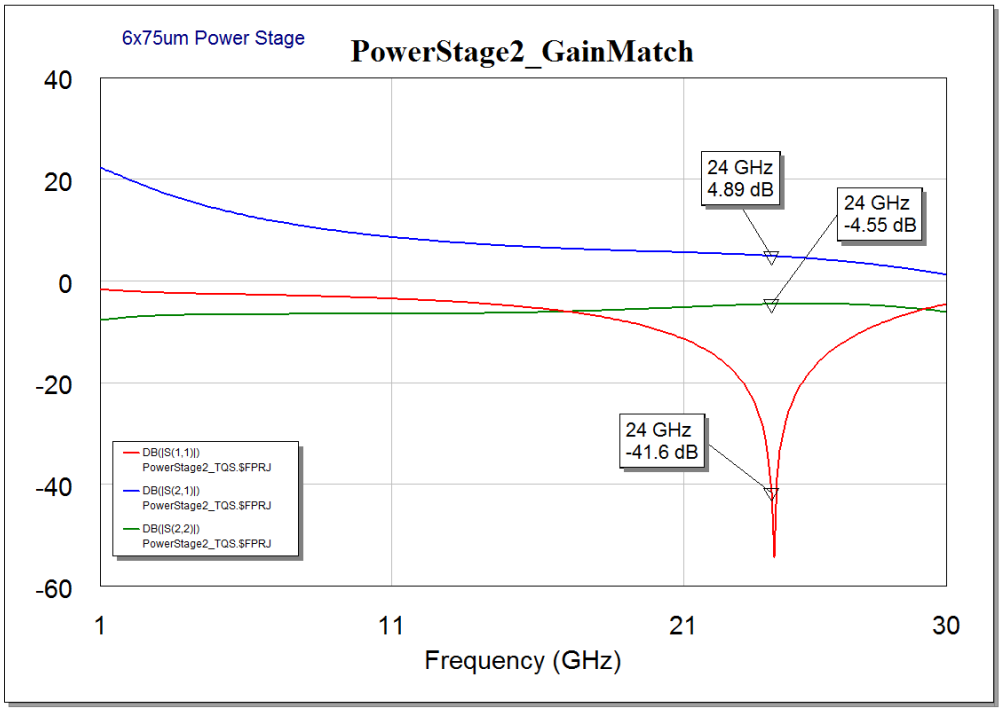


Figure 13. Small Signal Gain, Input Return Loss, Output Return Loss

Figure 14 shows that this stage is only conditionally stable even with Triquint elements. The assumption is that the addition of lossy microstrip interconnect will increase the stability at the lower frequencies. While this stage is not unconditionally stable, S_{11} and S_{22} do not go positive at any point, which reduces concerns about inadvertent oscillation.

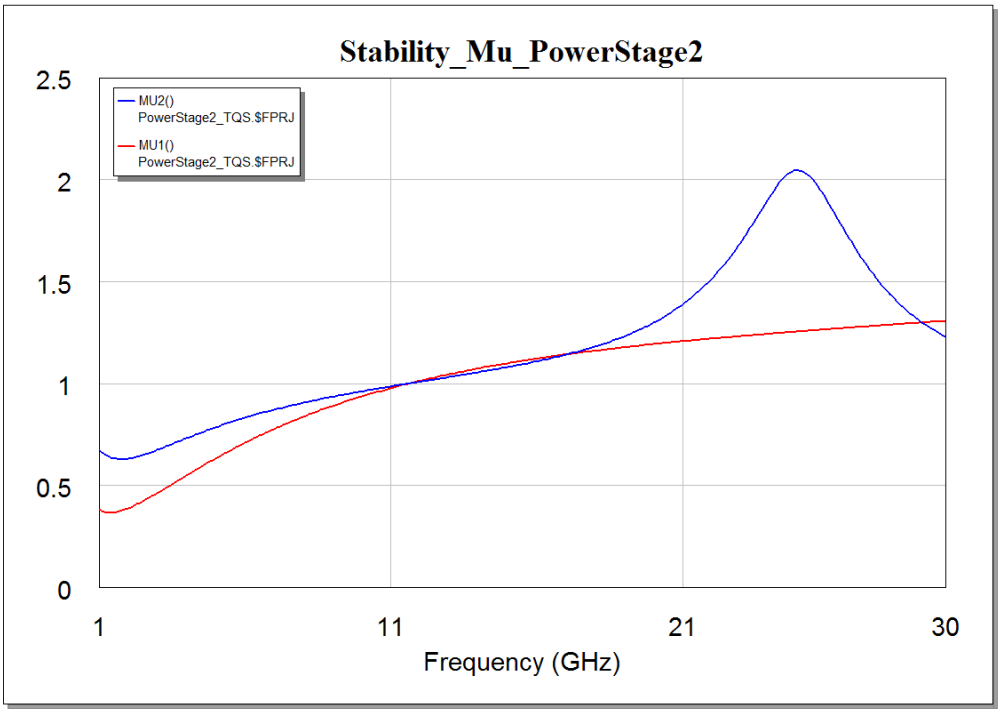


Figure 14. Stability, Power Stage 2

Figure 15 shows the output power and gain plotted as a function of input power. The approximate 1dB compression points are marked.

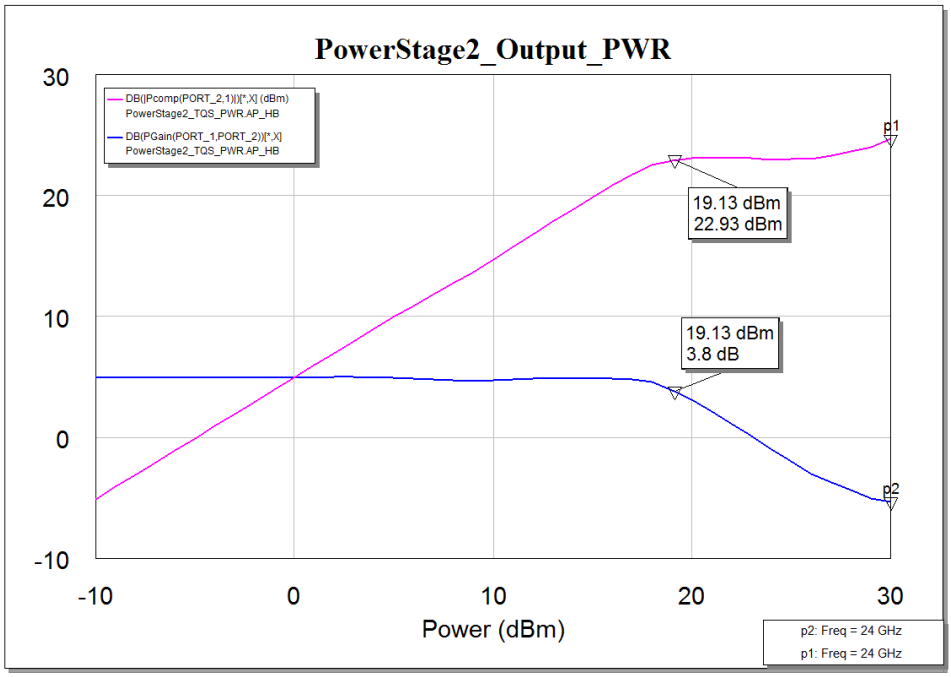


Figure 15. Output Power, Power Stage 2

Cascade Circuit

The next step is to take the three independently designed stages and connect them in cascade. The schematic of the cascade circuit is shown in figure 20 on page 14. The circuit still has ideal interconnect and ideal biasing at this point. Figure 16 shows the gain, input return loss, and output return loss of the circuit. The output return loss is driven by the output return loss of the last stage, so it is no surprise that it is low.

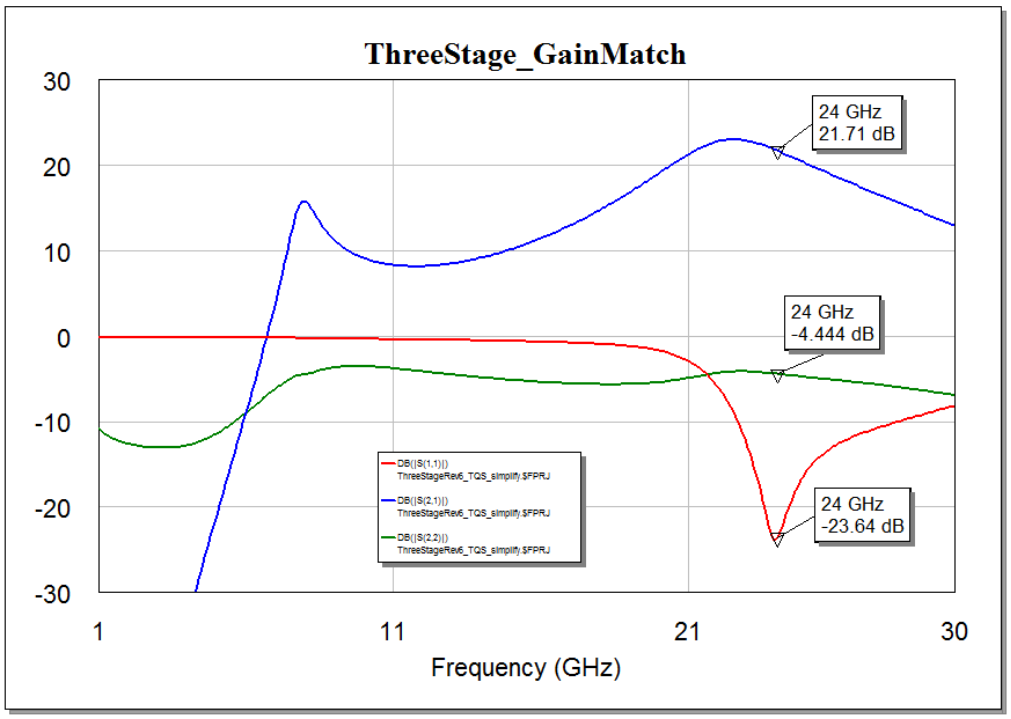


Figure 16. Cascade Gain, Input Return Loss, Output Return Loss

Figure 17 shows the cascade design is unconditionally stable across the frequency range 1-30GHz.

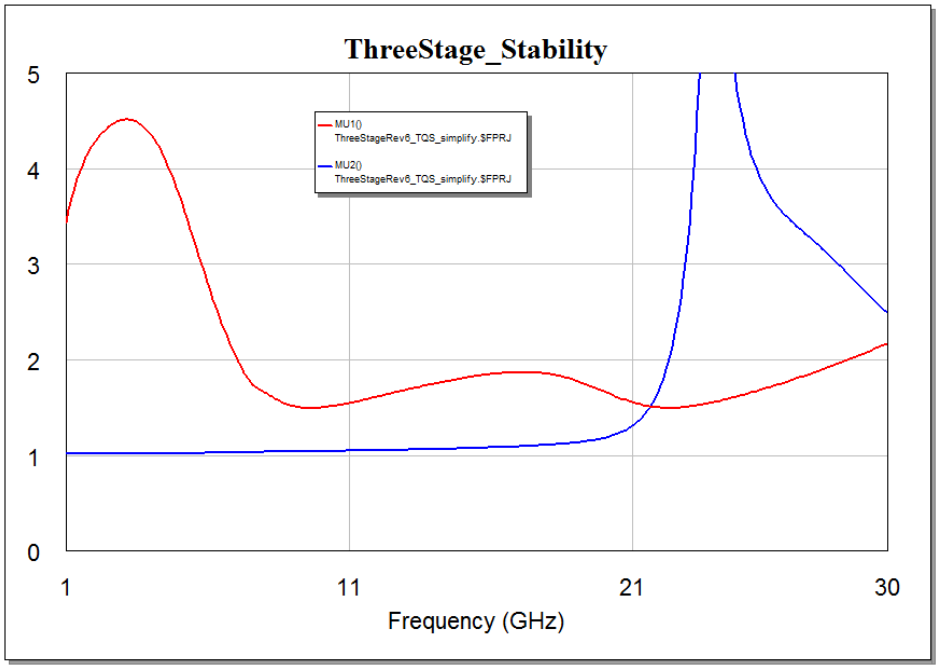


Figure 17. Stability, Cascade Design

The output power and gain is shown in figure 18 below. The approximate P1dB point is marked. It is interesting that the simulation was unable to converge at 6dBm input power, but ran fine elsewhere. The power added efficiency (PAE) is also plotted in green. MWO calculated a PAE of 13.86% at the P1dB point, although back of the envelope calculations place the PAE closer to 30%, this discrepancy was unable to be resolved by the project due date. The measurement is shown here for completeness.

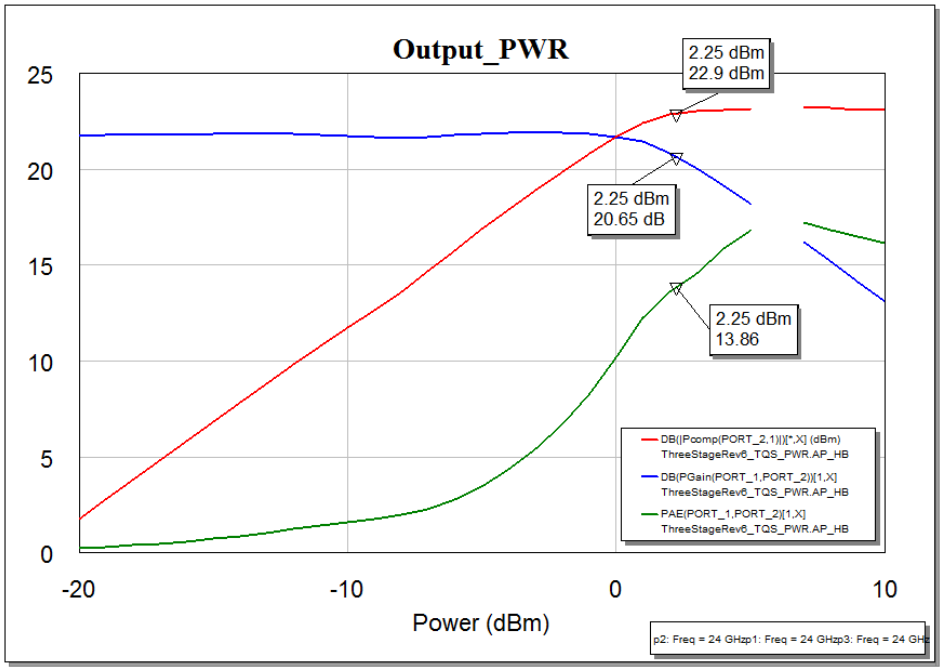


Figure 18. Output Power, Cascade Circuit

Layout

Transforming the schematic shown in figure 20 into a full layout was a slow, iterative process. The first step was to orient and place the layout cells according to the schematic. Then, slowly proceeding from the input to output, each connection was replaced with a microstrip line, bend, or tee that would allow the elements to physically connect. The inductance of each section of microstrip interconnect has a significant impact on the matching network elements, due to the high operating frequency. This required compensation for each section of interconnect. Once a first pass layout was completed, its size was compared to the Anachip layout to determine how much compacting would be necessary. Bends and curves were added to straight lines where possible, and vias combined where possible. Eventually the circuit was able to fit within the Anachip layout and input and output bond pads were connected. Bias inductors and bypass capacitors were maximized to the available space left in order to maximize the RF isolation of the circuit from the bias points. Given more time, the drain bias connections can be tied together to allow for a single 4V supply instead of 3 separate. The gate bias can be generated using a voltage divider off of the 4V, if desired. The final layout is shown in figure 19 below. Just for reference, the complete schematic is shown in figure 21.

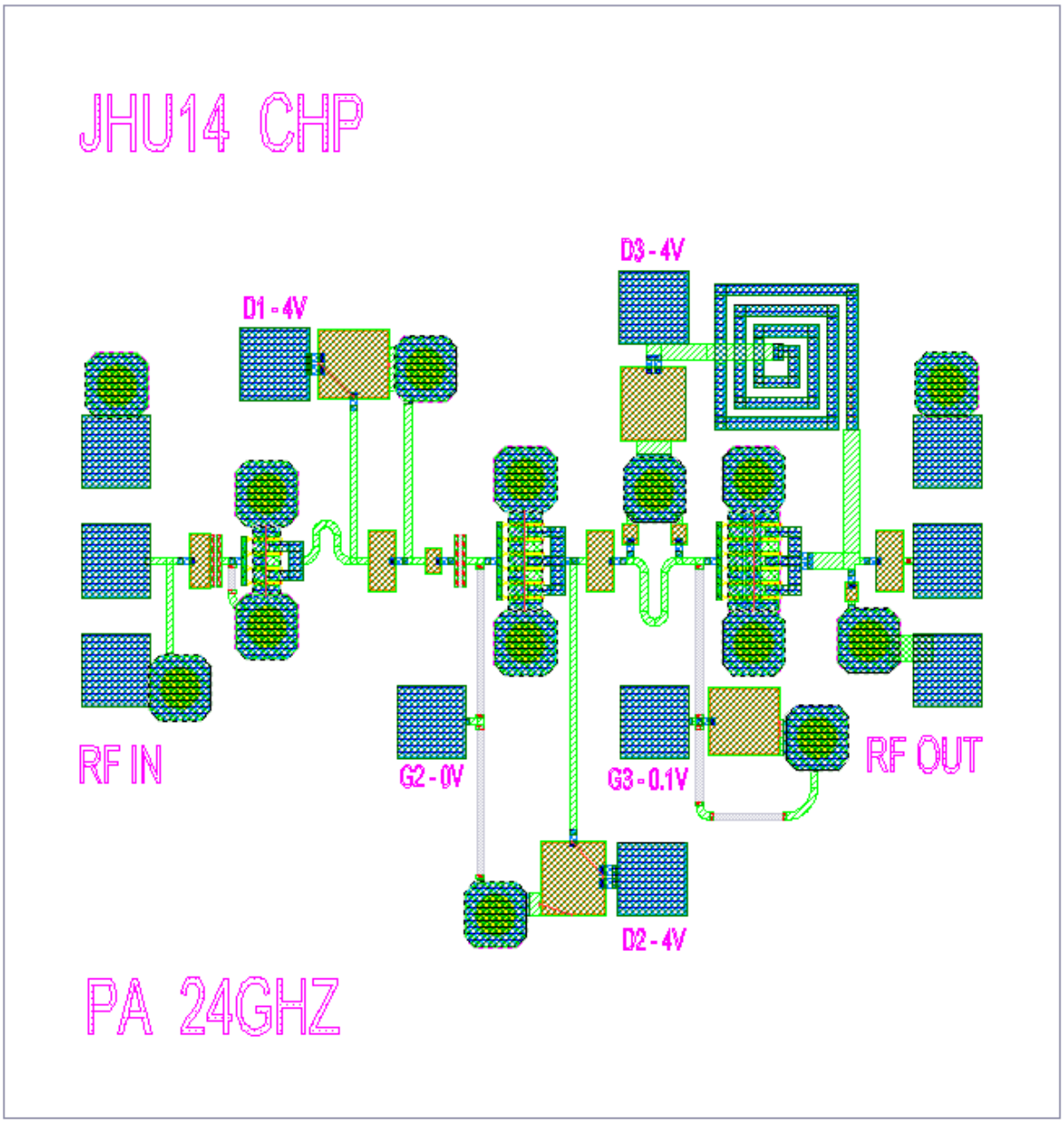


Figure 19. Final Layout

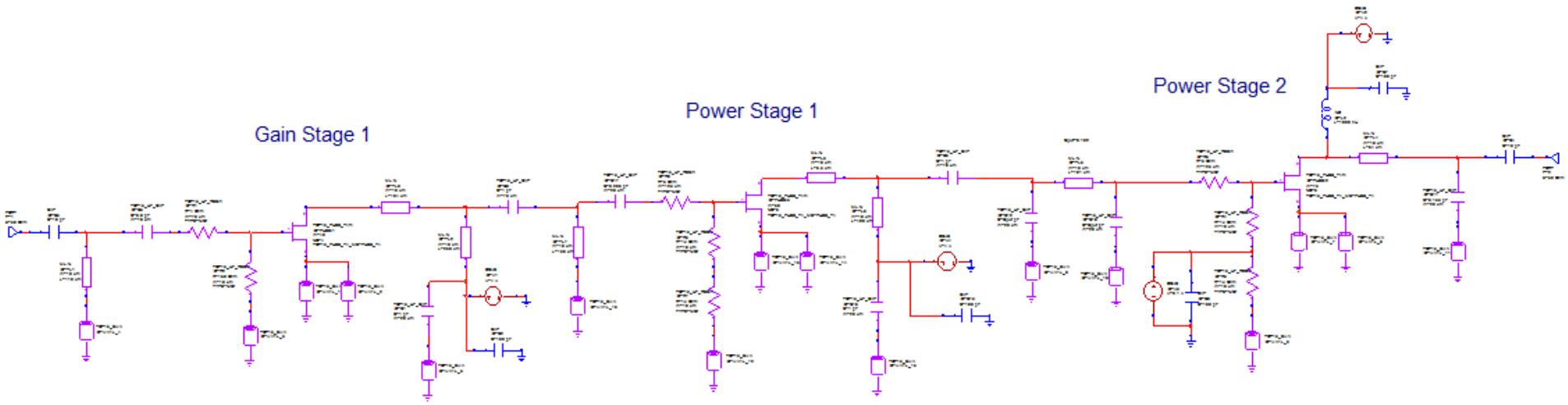


Figure 20. Cascade Schematic, Ideal Interconnect

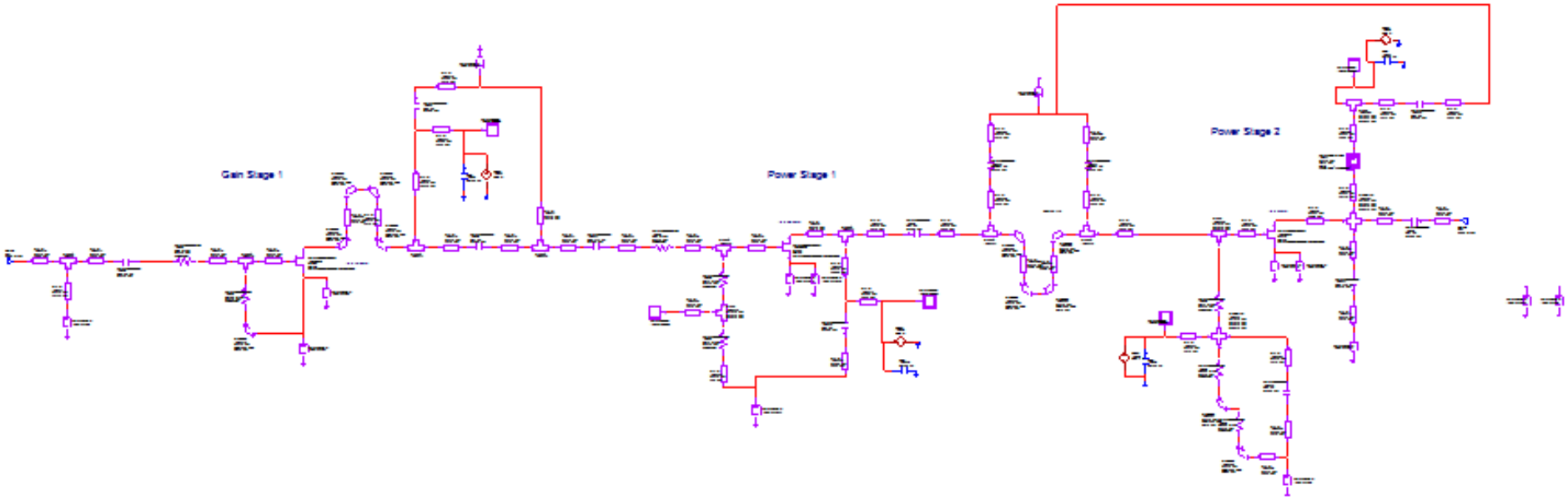


Figure 21. Complete Schematic, Microstrip Interconnect

Test Plan

The procedure to test the fabricated MMIC is presented below.

Required Equipment

1. 4 DC Probes (V_{D1}, V_{D2}, V_{D3}, V_{G3})
2. Two RF Probes (Input, Output)
3. Network Analyzer
4. Spectrum Analyzer
5. Signal Generator

The first measurement will be to check the small signal S-Parameters using the network analyzer. Then the output power and compression will be checked using a signal generator and spectrum analyzer. Efficiency can be checked by recording the DC power consumption while measuring the output power.

Biasing Procedure

All three transistors are DC biased at V_{GS} = 0V, so it is safe to apply 4V to each drain bias pad. The third transistor needs a gate bias of V_{GS} = 0.1V to operate as designed. The bias currents should be similar to those listed below:

a. I_{D1} = 19mA
b. I_{D2} = 35mA
c. I_{D3} = 83mA

S-Parameter Measurements

Calibrate the network analyzer across the frequency range 1 – 30GHz. Set the test power level to -10dBm or less to ensure small signal operation. Measure S_{11}, S_{22}, S_{21}, S_{12} and save for later comparison against simulated measurements.

Output Power Measurements

Connect a signal generator to the input and set the frequency to 24GHz, and the power to -10dBm. Connect the spectrum analyzer to the output and measure the output power at 24GHz. Record the output power and DC currents. Increase the input power to +3dB in 1dB steps. Record the output power and DC currents for each input power step.

Alternate Testing

Once the above tests are run at the designed bias point, some experimentation can be done to check limits of the design. The above tests can be run at slightly higher or lower drain voltages. The third stage gate bias can be removed, and it can be run at V_{GS} = 0V. A small gate voltage can be injected into the middle stage via the G2 bias pad.

Conclusion

The initial design goals and the final simulation results are shown in the table below. The nonlinear simulations performed in Microwave Office using the TQP14 library show that it is possible to achieve 20dB gain and 20dBm output power at 24GHz in a relatively small 1500 x 1500um GaAs MMIC. Each design goal was met with the exception of the output return loss, which was deemed acceptable. To fully qualify the design, additional parameters can be measured, such as efficiency. This design was not designed with efficiency in mind, but for compact, portable applications, efficiency is a larger concern. A load pull can be performed to verify the output match. Dynamic load lines can be plotted to verify each device is operated in the intended region. With additional time available, an electromagnetic (EM) simulation can be performed to verify the layout and account for interaction between elements in close physical proximity. Robustness of the design can be verified by running Monte Carlo simulations using process variation data. The ultimate verification of the design, measuring an actual MMIC, will have to wait a few months.

Design Parameter	Design Goal	Design Performance
Gain (S_{21})	20dB	21.7dB
P1dB (output)	20dBm	22.8dBm
Input Return Loss (S_{11})	-20dB	-23.6dB
Output Return Loss (S_{22})	-10dB	-4.4dB

Figure 22. Design Goals vs. Achieved

Two- Stage, Ku-Band Power Amplifier

Greg Scarborough

MMIC Design

EE 787

Johns Hopkins

12/10/14

Abstract

This report describes the design process and simulated performance of a two-stage power amplifier tuned for Ku-band operation using a GaAs MMIC process. The design was simulated using Microwave Office with Triquint's TQP design kit. Layout for the design used Triquint's 0.13 um process.

Introduction

Power amplifiers serve as an integral component in a communication system. A frequency of 15 GHz was chosen due to its usage in the UAV and SATCOM markets. A Class A power amplifier was chosen for this project due to its characteristics of high output power and ease of implementation, while having a lower efficiency compared to other amplifiers classes. The goal of this power amplifier was to produce as much power as possible, bounded by the design process and substrate size. To achieve the maximum amount of output power, a two stage design was chosen, with the first stage of the amplifier being a high gain element and the second stage of the amplifier being a maximum output power component. Table 1 details the design goals for this two stage power amplifier design.

Table 1: Design Goals

Parameter	Goal
Frequency	15 GHz
Gain	15 dB
Pout	20 dBm
PAE	25%

Design Approach

The design approach was to design each stage of the amplifier individually, then to combine them and tune the matching inductor and capacitor elements for maximum output power. The first stage will be referred to as the driver stage and the second stage will be referred to as the power stage. The TOM4 model of the Triquint library was first simulated to determine the IV curves. A DC source was connected to the depletion mode pHEMT TOM4 model and swept. The results are shown in Figure 1. Figure 1 shows the load line and if biased with a VGS of 0.1 V and a VDS of 4 V would provide the maximum current swing and maximum output power. At 4 V VDS and 55mA, the Cripps resistance would be approximately 73Ω.

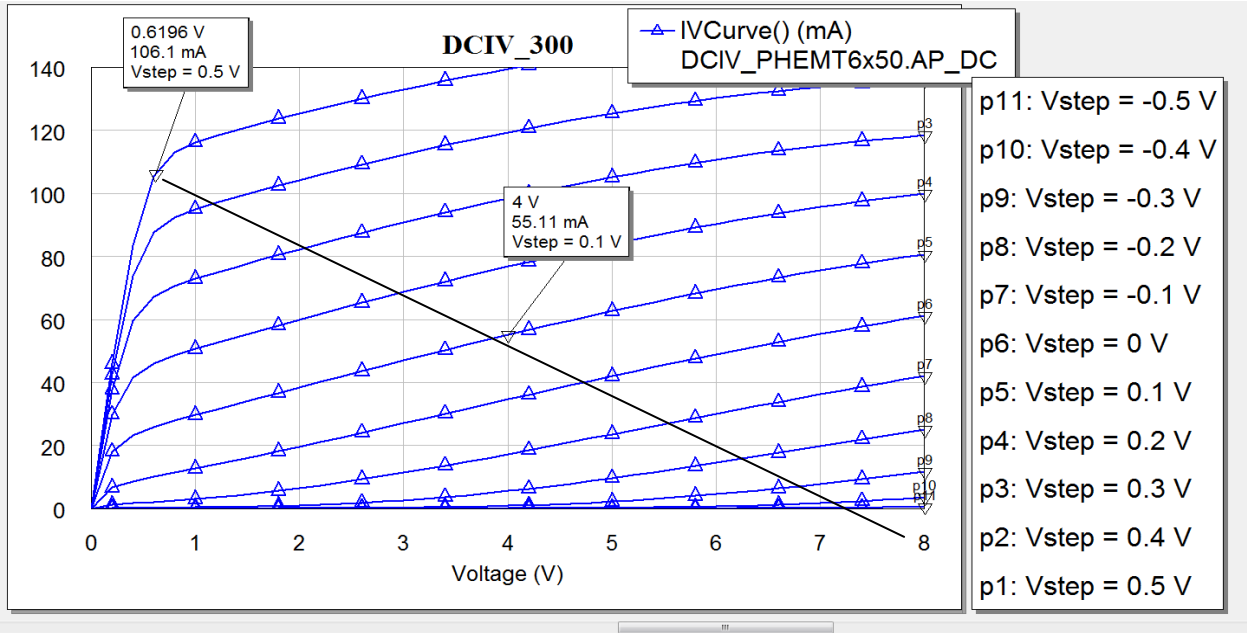


Figure 1: Triquint TOM4 IV Curves

After the TOM4 IV curve was modeled, GAC_MAX and GPC_MAX circles were simulated for the TOM4 model at 15 GHz. These measurements show the available gain contours in the input and output reflection planes. The point highlighted in Figure 2, shows the impedance that the output of the transistor wants to see for maximum gain in relation to the input of the transistor. The conjugate match will then be designed on the input of the transistor.

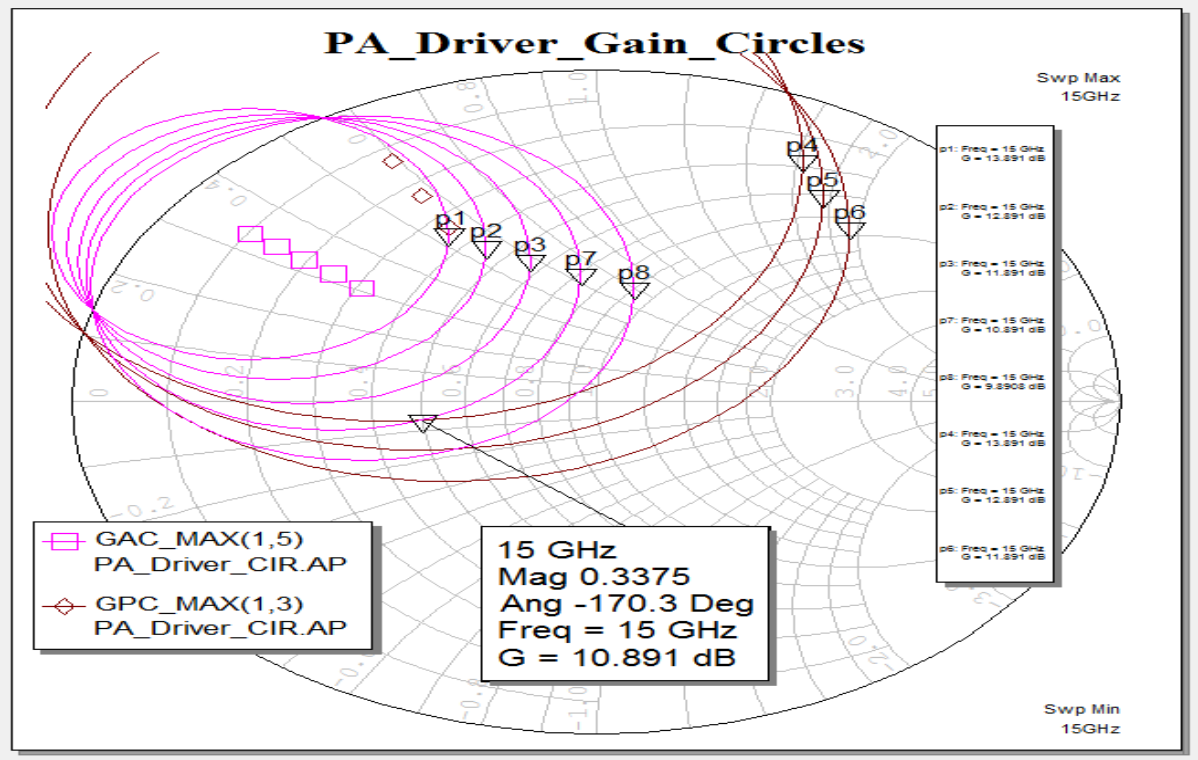


Figure 2: Triquint TOM4 Gain Circles at 15 GHz

Using the smith chart utility, an output impedance match was then calculated using the datapoint established in Figure 2. Figure 3 details the impedance matching process which resulted in a shunt inductor of 0.545 pH and a series capacitor of 0.489 pF.

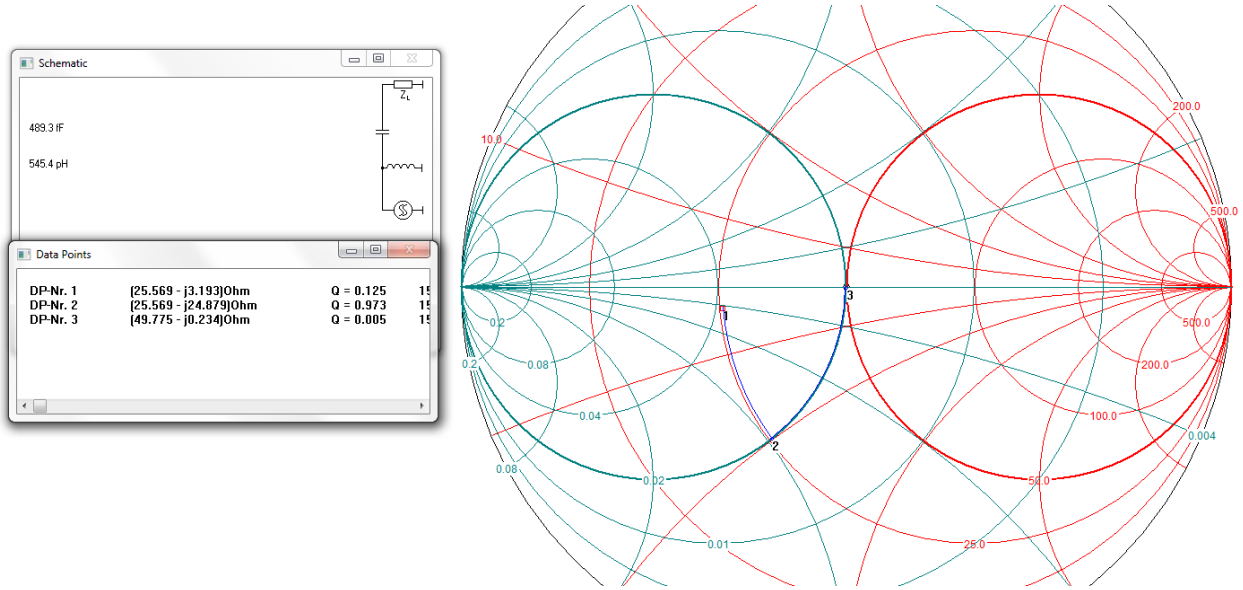


Figure 3: Drive Stage Matching Network on the Smith Chart

The impedance match established in Figure 3 and its conjugate match were then added to the transistor model. A series and shunt resistor were added on the base of the transistor to provide stability. DC biasing was added to the circuit to bias drain at 4 V. DC blocking capacitors of 10 pF were added to prevent the RF and DC from mixing. All elements added were ideal and this is shown in Figure 4.

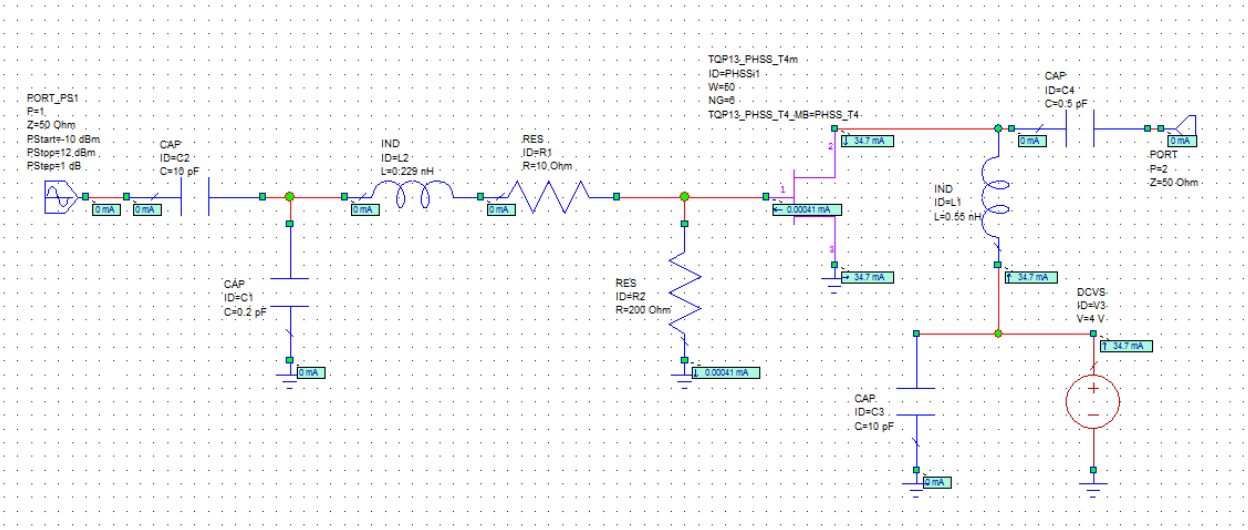


Figure 4: Ideal Schematic of Driver Amplifier

The circuit in Figure 4 was then simulated using a non linear simulation in Microwave Office. This was done as a sanity check to ensure that the circuit functioned before progressing the design. Figure 5 shows the non linear simulation with an input power of 0.783 dBm and output power of 9.485 dBm.

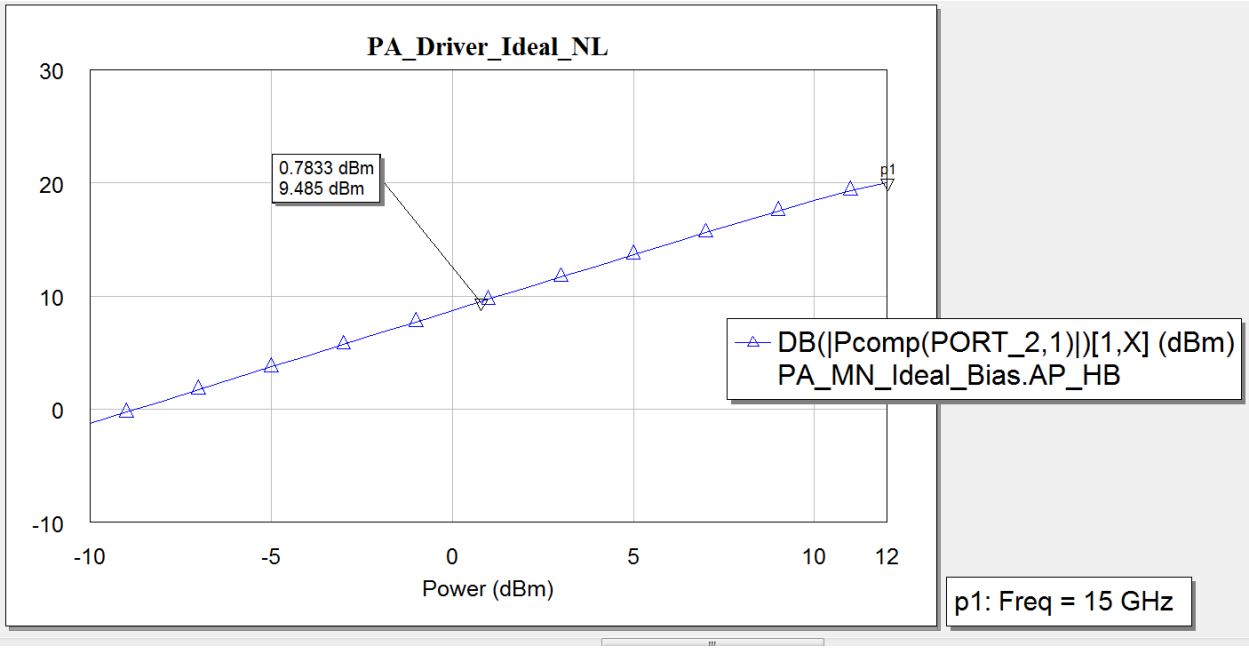


Figure 5: Non Linear Simulation of Driver Amp Using Ideal Elements

The ideal elements were replaced with Triquint elements. Microstrip was added for the layout and a substrate was added for simulation purposes. This circuit schematic is shown in Figure 6.

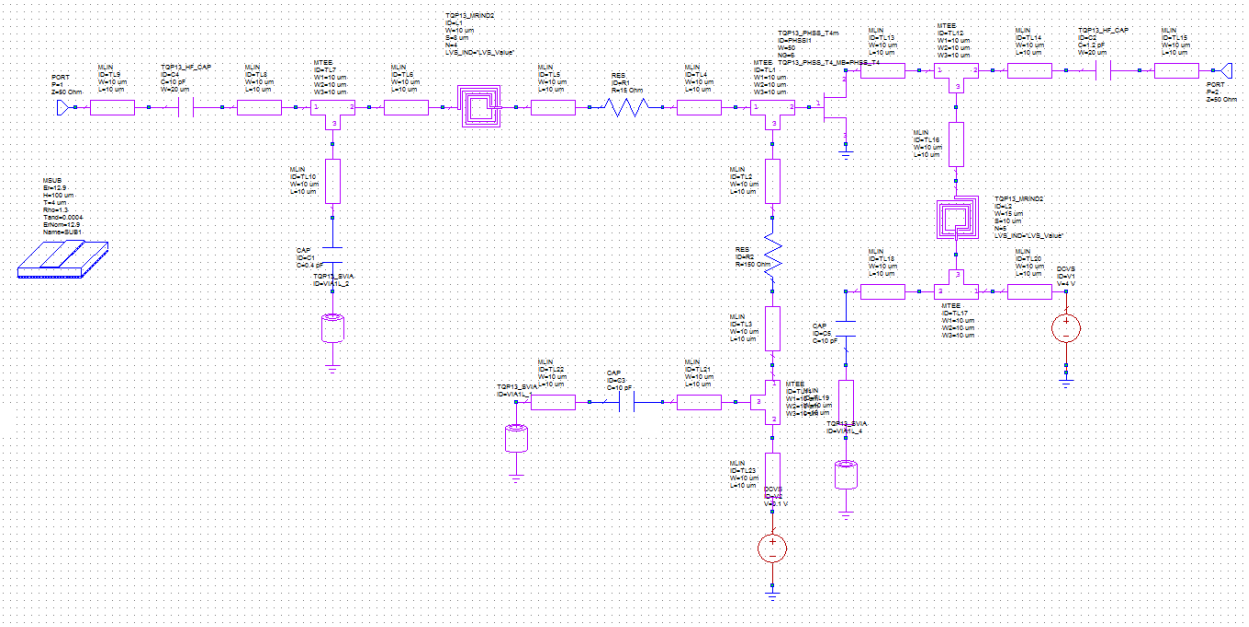


Figure 6: Triquint Schematic of Driver Amplifier

The circuit in Figure 6 was then simulated using a linear simulation. Inductors and capacitors were tuned to achieve the highest possible gain. S parameters of the circuit are shown in Figure 7. Figure 7 shows a gain of approximately 8 dB, which was the maximum possible gain for this circuit at 15 GHz. The Figure 8 shows the stability of the transistor circuit. The resistors were tuned to increase the gain and maintain a Mu1 greater than 1 across the entire frequency band to ensure no oscillations in the circuit.

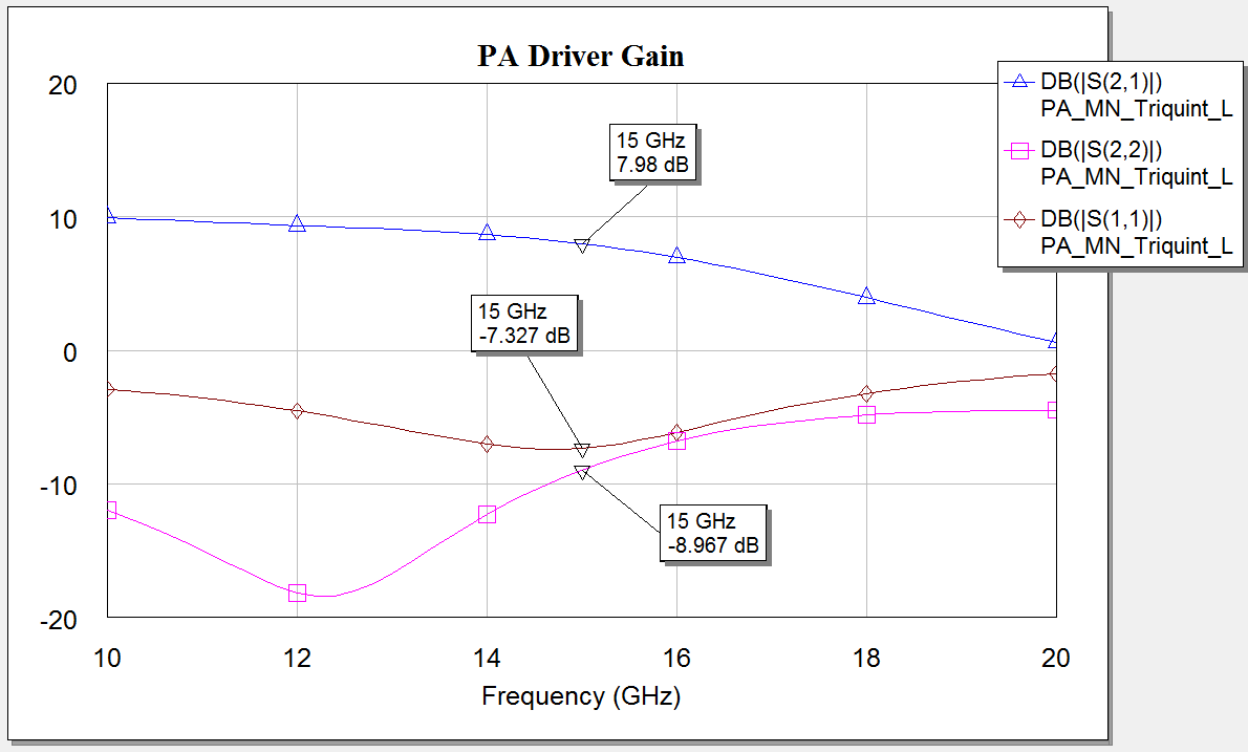


Figure 7: S Parameters of Final Driver Amp

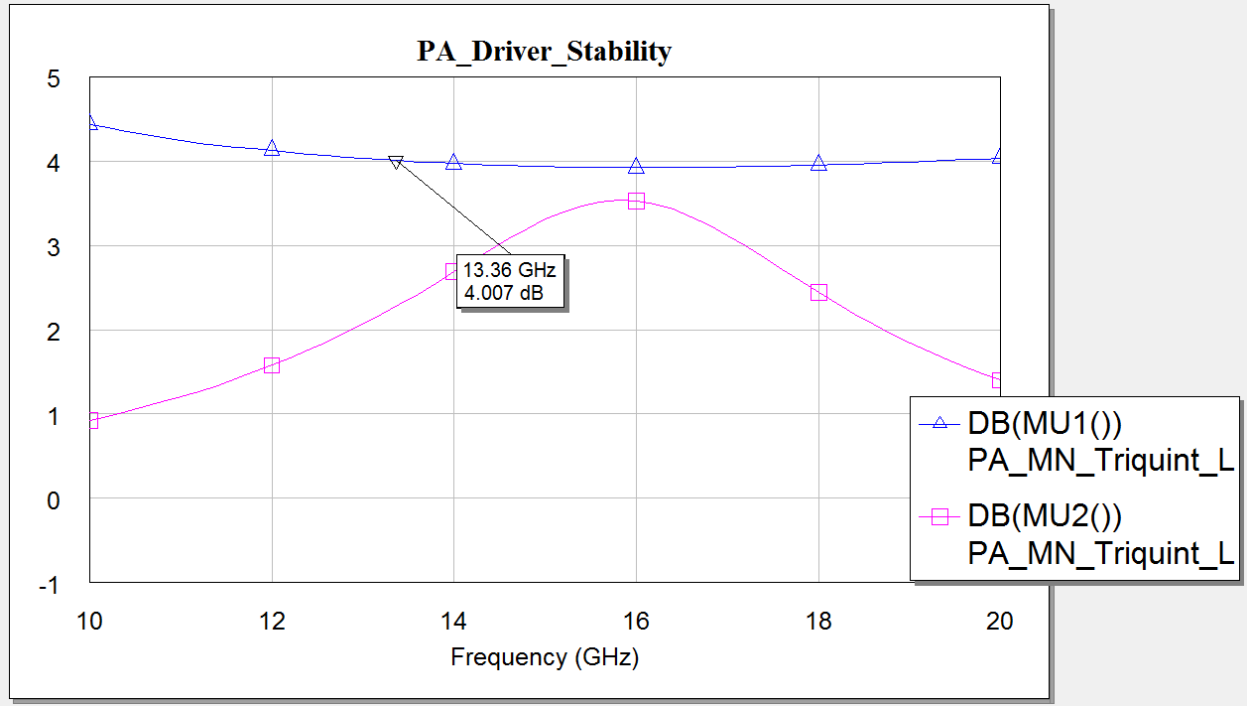


Figure 8: Stability of Final Driver Amp

Figure 9 shows the non linear simulation of the driver amp. With an input power of 8 dBm the circuit shows an output power of 16.76 dBm with a PAE of 19.2%. These parameters were acceptable for the driver amp to meet the overall design goals.

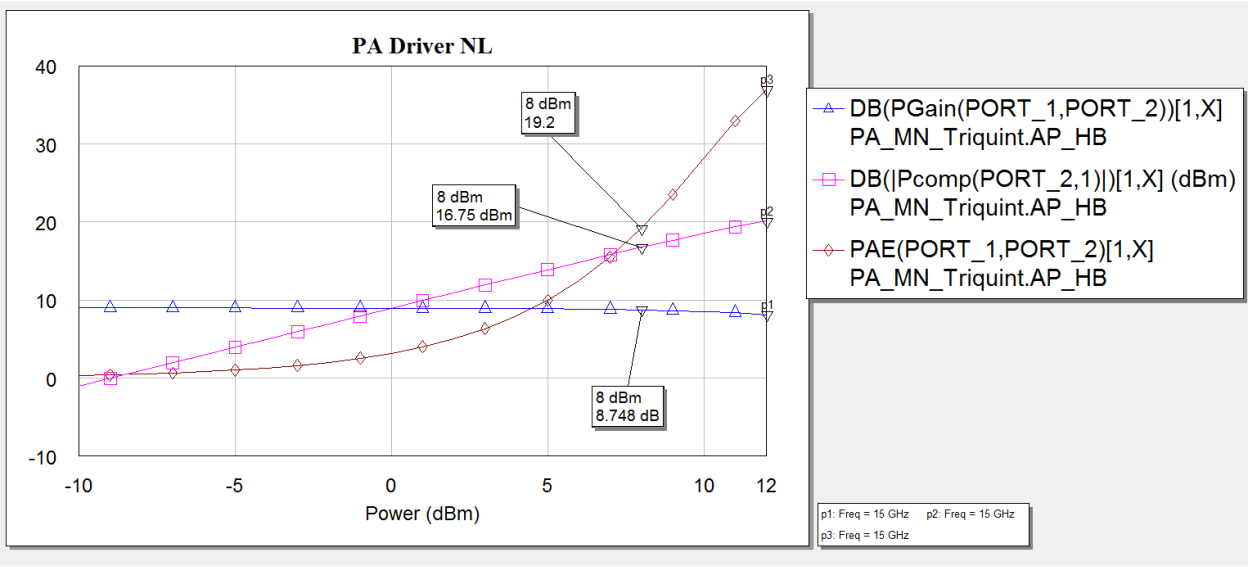


Figure 9: Non Linear Simulation of Final Driver Amp

Figure 10 shows S22 of the TOM4 Triquint model at 15Ghz. This value was used to calculate the parallel resistor and capacitor that showed this impedance on the drain and source of the model. Figure 11 details this.

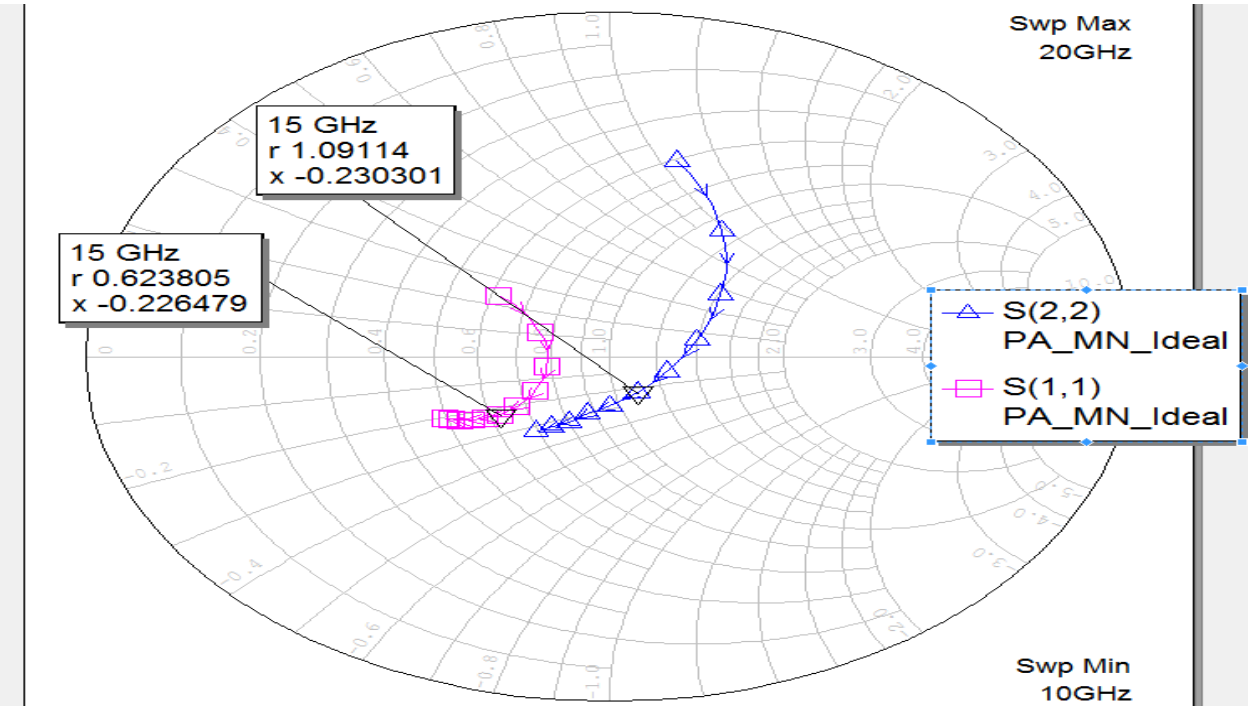


Figure 10: TOM4 Triquint S Parameters

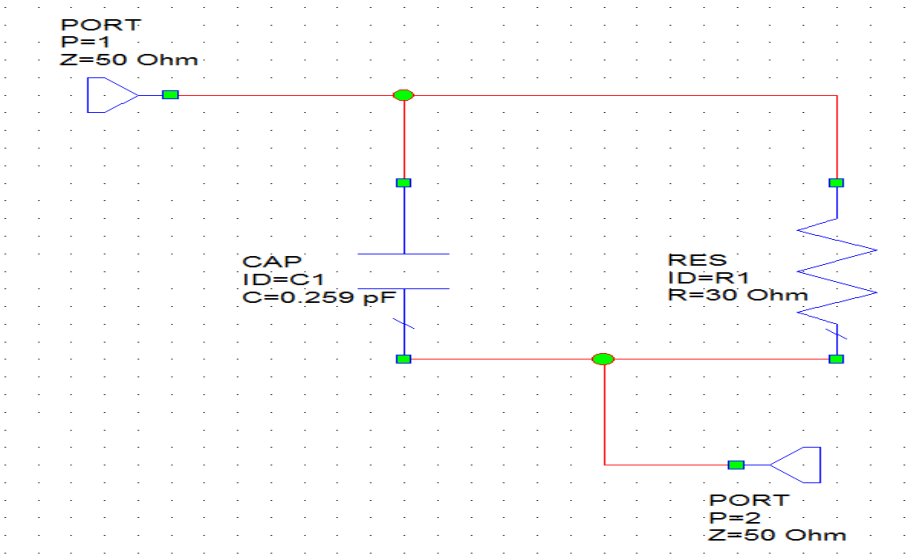


Figure 11: Cds and Rds of TOM4 Model

The resistor in Figure 11 was replaced with the Cripps resistor calculated from Figure 1. The output of the transistor was then impedance matched to these values and the conjugate match was applied to the input of transistor. This impedance matching technique for the second stage of the power amplifier will provide the maximum amount of output power. This circuit was created using ideal elements and is shown in Figure 12. A series and shunt resistor were added on the base of the transistor to provide stability. DC biasing was added to the circuit to bias drain at 4 V. DC blocking capacitors of 10 pF were added to prevent the RF and DC from mixing.

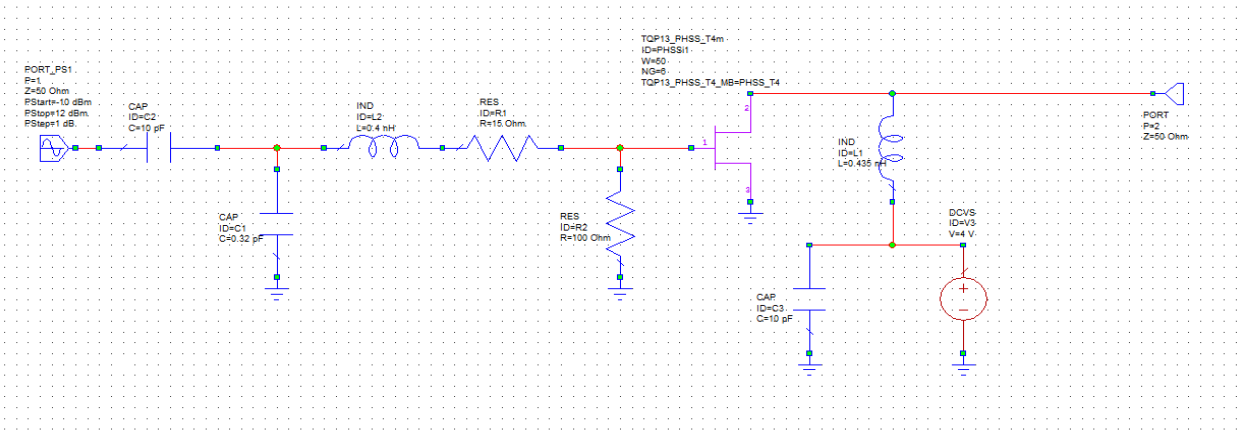


Figure 12: Power Stage Amplifier Using Ideal Elements

The circuit in Figure 12 was then simulated using a non linear simulation in Microwave Office. The inductor and capacitor elements were tuned to provide the maximum amount of output power. This was done as a sanity check to ensure that the circuit functioned before progressing the design. Figure 13 shows the non linear simulation with an input power of 0.527 dBm and output power of 9.555 dBm.

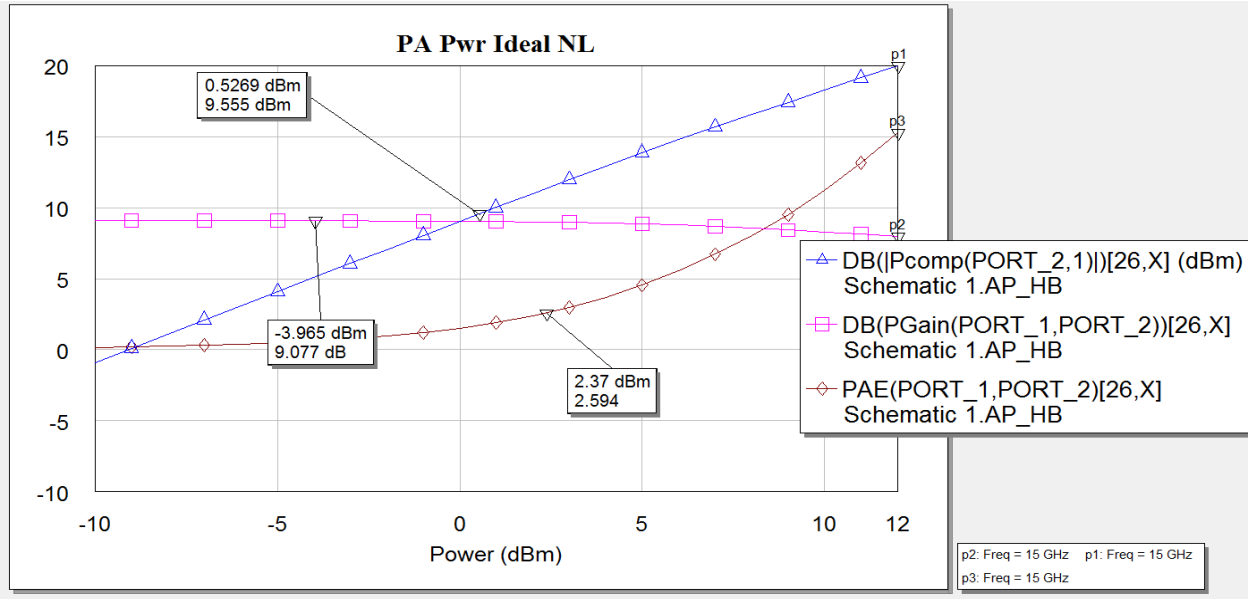


Figure 13: Power Stage Amplifier Non Linear Simulation Using Ideal Elements

The ideal elements were replaced with Triquint elements. Microstrip was added for the layout and a substrate was added for simulation purposes. This circuit schematic is shown in Figure 14.

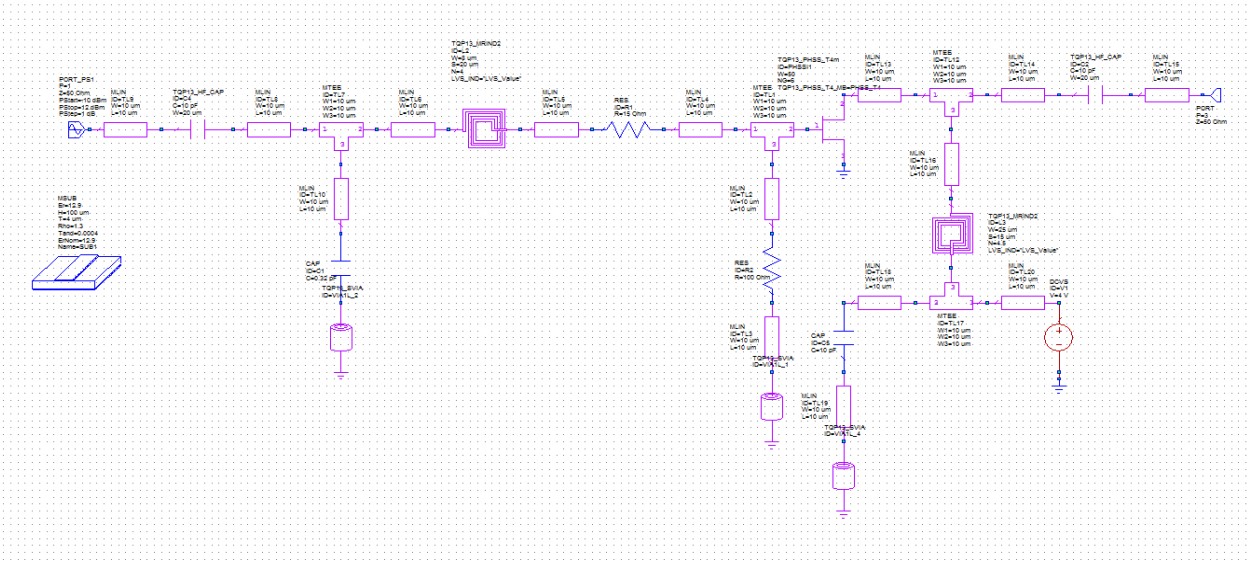


Figure 14: Power Stage Amplifier Schematic

The circuit in Figure 14 was then simulated using a linear and non linear simulation. Inductors and capacitors were tuned to achieve the maximum possible output power. S parameters of the circuit are shown in Figure 15. Figure 15 shows a gain of approximately 7.139 dB, which was the maximum possible output power for this circuit at 15 GHz. Figure 15 shows the stability of the transistor circuit. The resistors were tuned to increase the maximum possible output power and maintain a Mu1 greater than 1 across the entire frequency band to ensure no oscillations in the circuit.

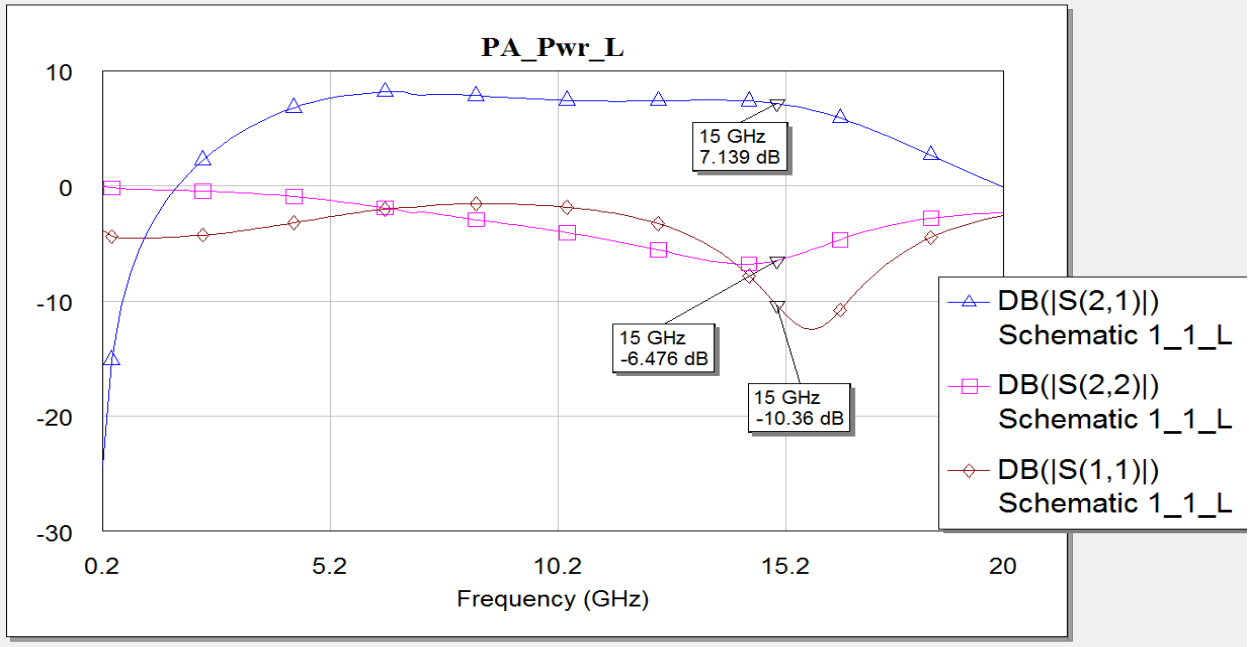


Figure 15: Power Stage Amplifier Linear Simulation

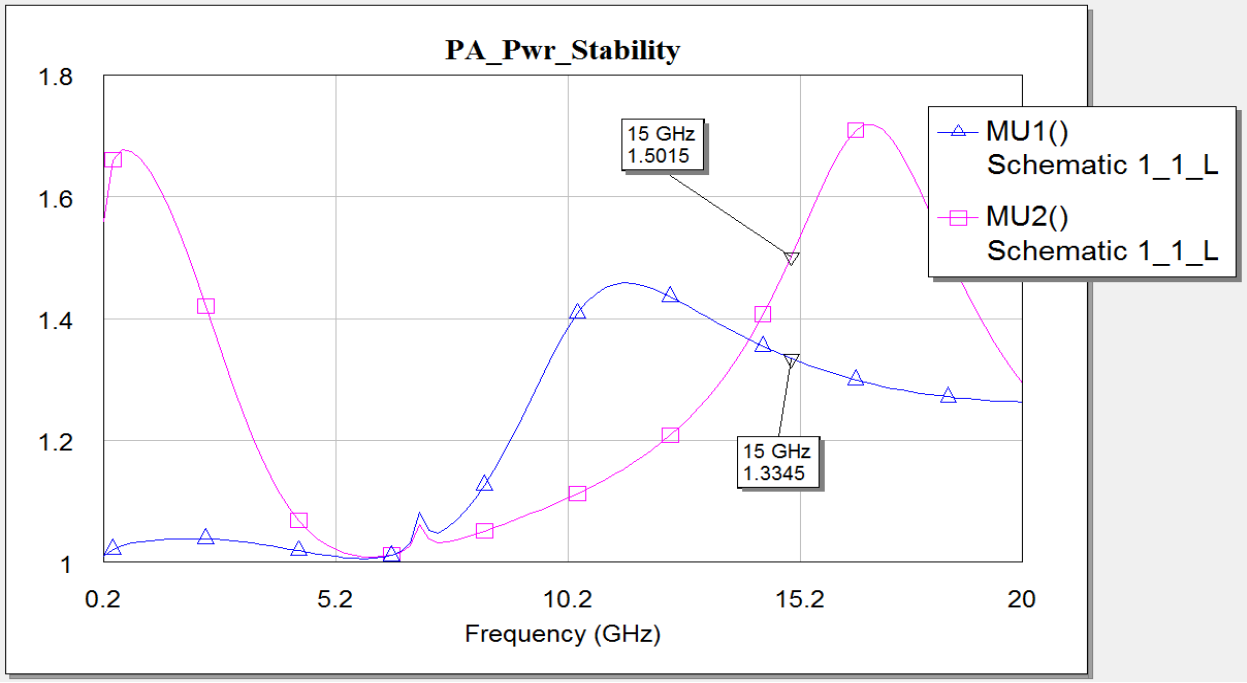


Figure 16: Power Stage Amplifier Stability

Figure 17 shows the non linear simulation of the power stage of the amplifier. With an input power of 8 dBm the circuit shows an output power of 14.48 dBm with a PAE of 14.9%. These parameters were acceptable for the power stage of the amplifier to meet the overall design goals.

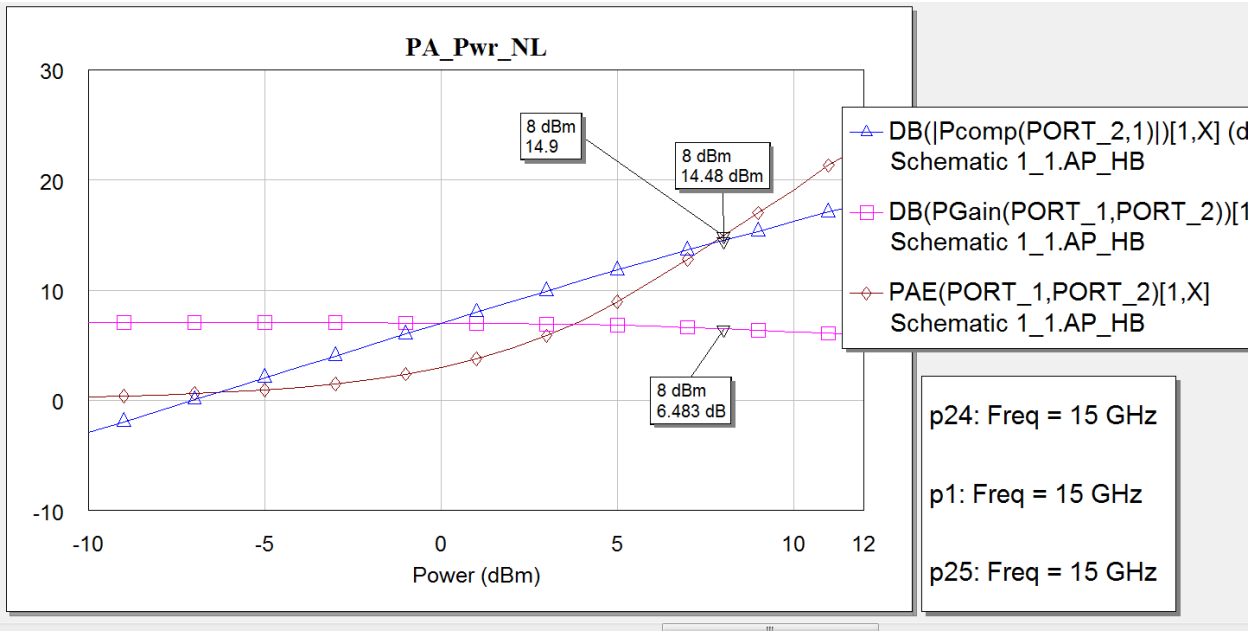


Figure 17: Power Stage Amplifier Non Linear Simulation

The first and second stage amplifiers were then combined into one schematic. The blocking capacitor from the input of the second stage of the amplifier was removed, due to the blocking capacitor on the output of the first stage providing the same function. At this point, concentration was then spent on the layout. This is detailed in the next section. After the layout was complete, the fingers of the second stage of the amplifier were increased to 12 to increase the maximum amount of output power. It was found that increasing the fingers beyond that threshold greatly reduced the PAE. Capacitors were then tuned to provide the maximum amount of output power. Resistors were tuned to increase the maximum amount of output power, while maintain a Mu1 of greater than 1 across the frequency band.

The circuit in Figure 18 was then simulated using a linear and non linear simulation. S parameters of the circuit are shown in Figure 19. Figure 19 shows a gain of approximately 13.2 dB at 15 GHz. Figure 20 shows the stability of the transistor circuit. A Mu1 of greater than 1 across the entire frequency band was achieved to ensure no oscillations in the circuit.

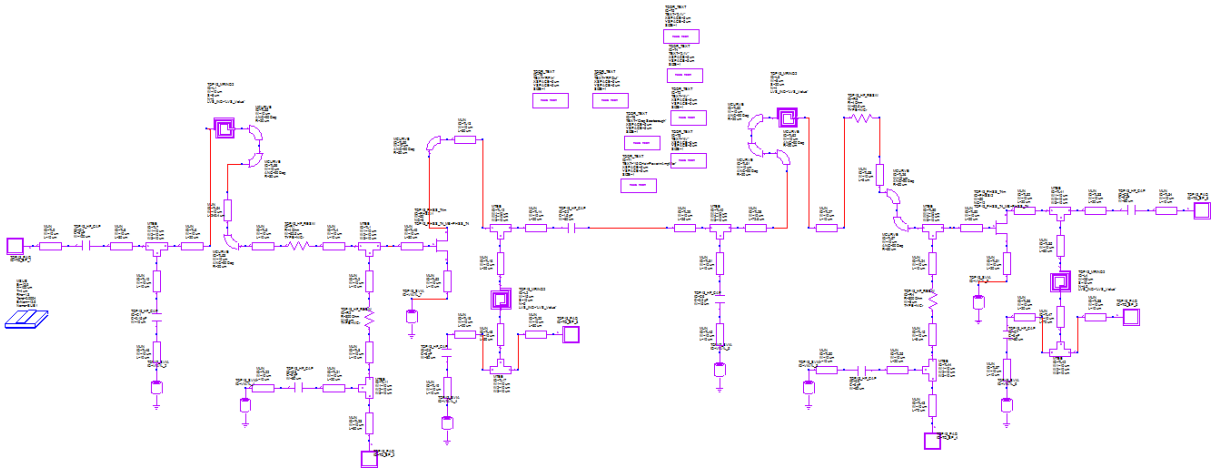


Figure 18: Power Amplifier Schematic

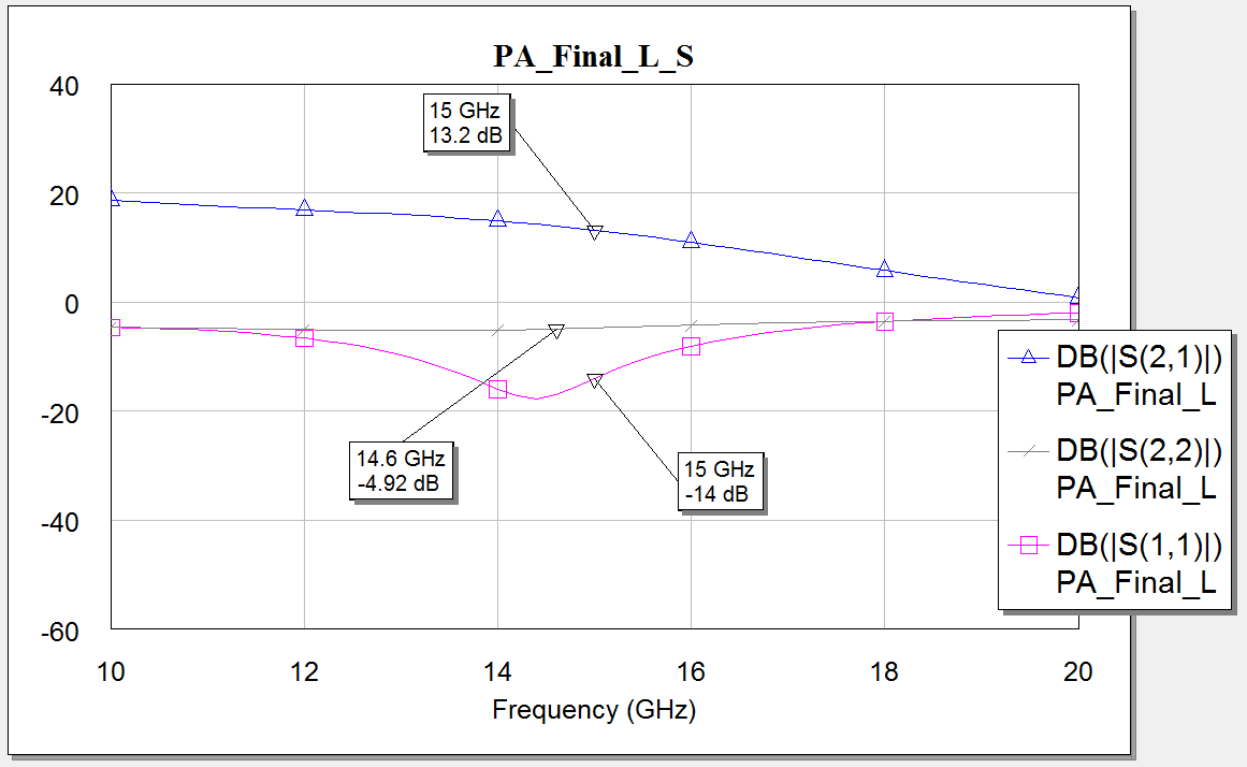


Figure 19: Power Amplifier Linear Simulation

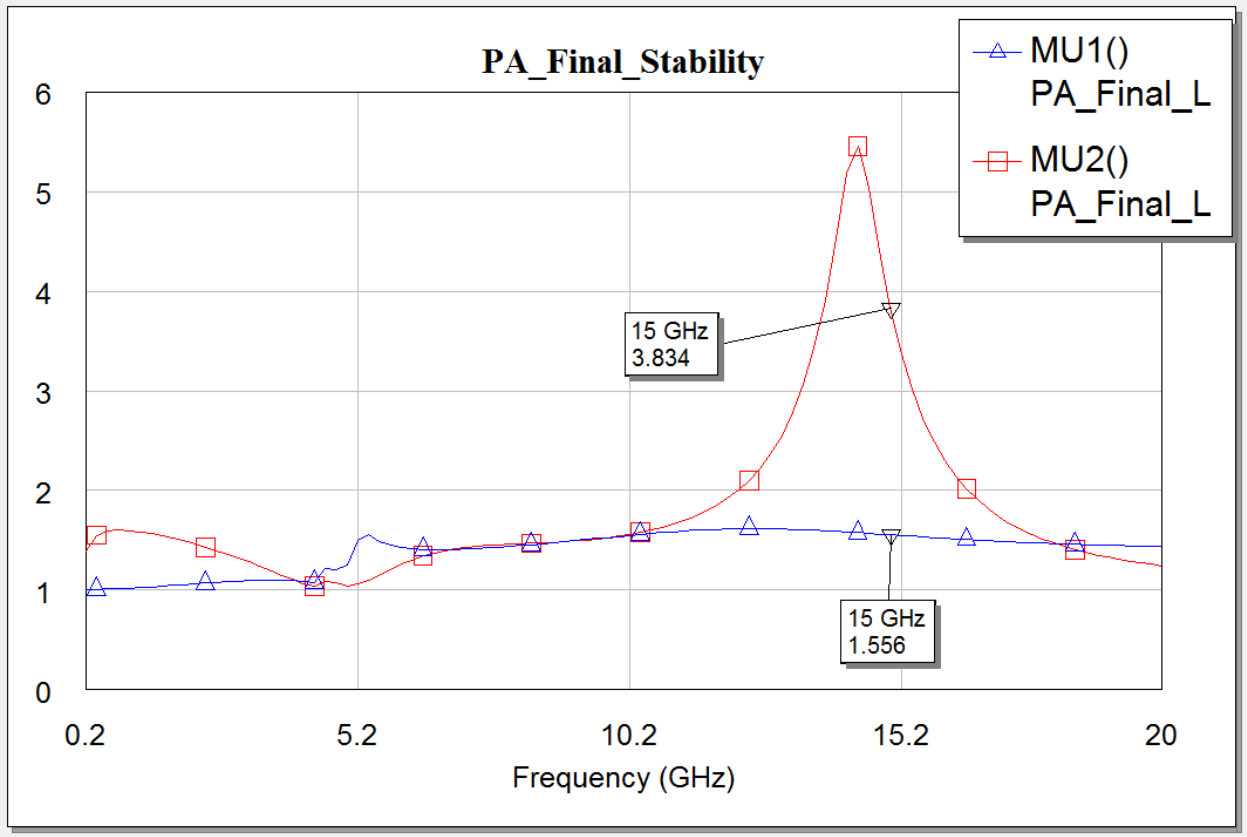


Figure 20: Power Amplifier Stability

Figure 21 shows the non linear simulation of the power amplifier. With an input power of 10.38 dBm the circuit shows an output power of 22.8 dBm with a PAE of 26.45%.

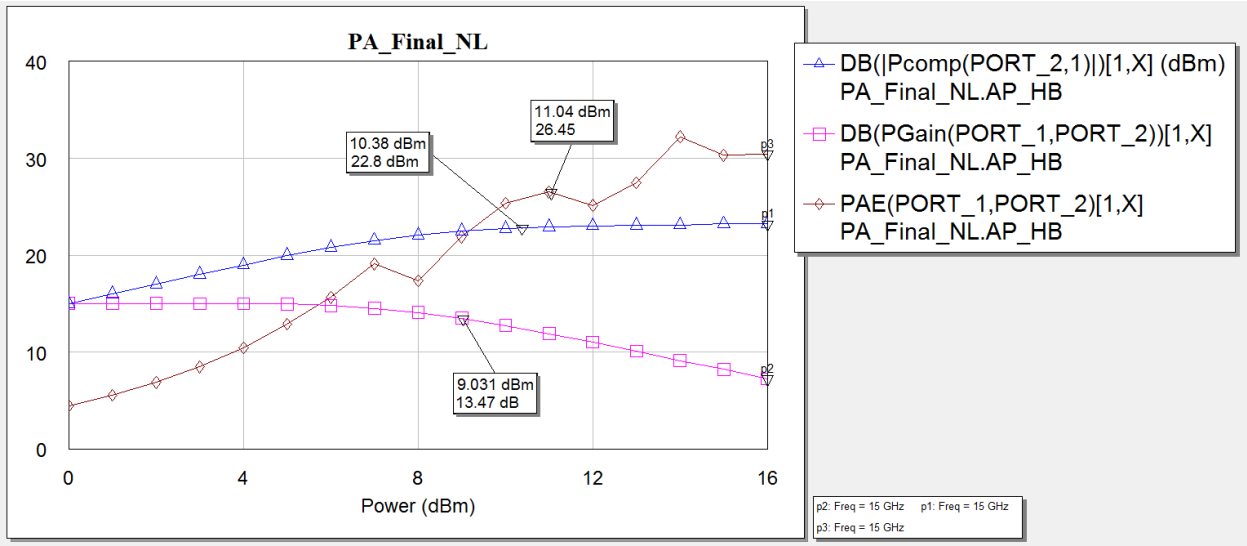


Figure 21: Power Amplifier Non Linear Simulation

Layout

Figures 22 and 23 show the final power amplifier in 2D and 3D form. Several microstrip bends were added to ensure proper distance between components to prevent coupling. Capacitor width was tuned for sizing efficiency. All inputs were labeled.

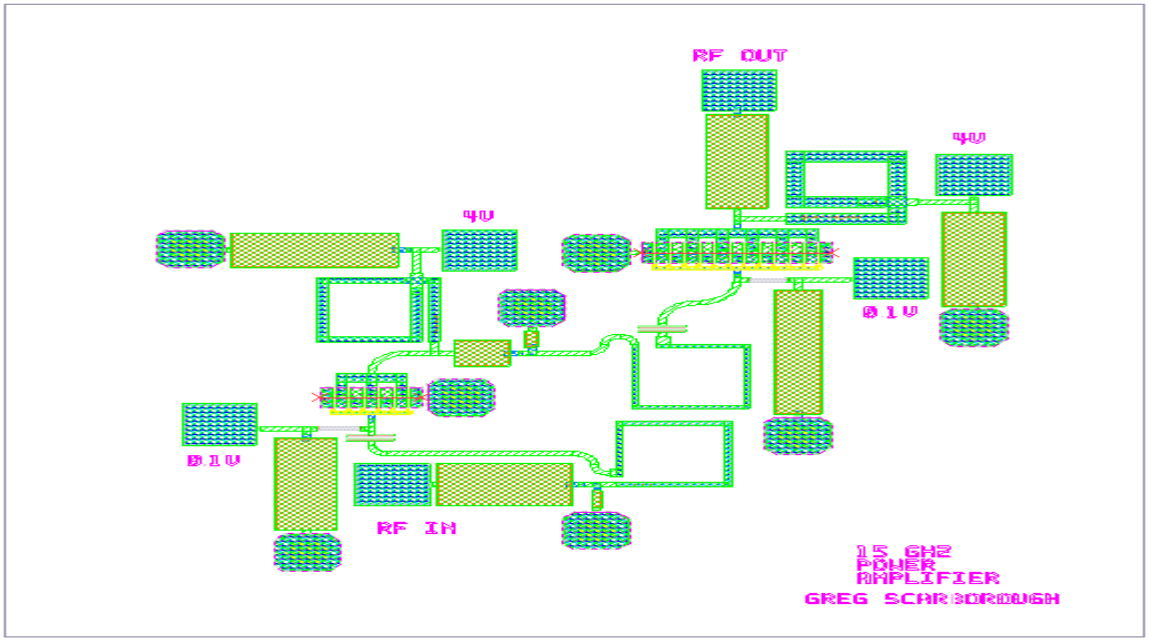


Figure 22: 2D Layout of Final Power Amplifier Circuit

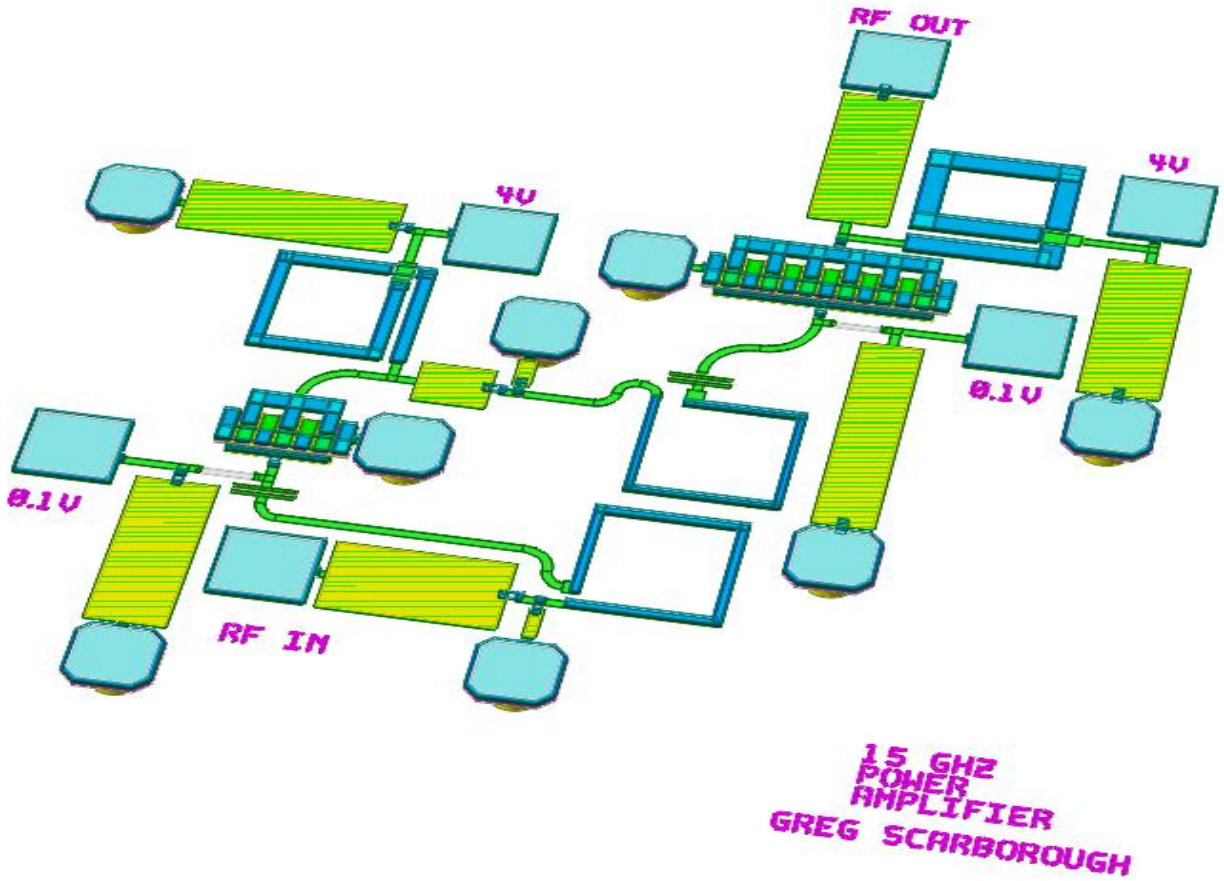


Figure 23: 3D Layout of Final Power Amplifier Circuit

Test Plan

Test Equipment:
DC power supply (2)
Spectrum Analyzer
Signal Generator
DC Probe (2)
RF Probe (2)

Test Setup:
Set the DC power supplies to 0.1 V and 4 V. Connect the DC probes to the power supplies and insert the probes onto the labeled pads of the die. Connect the first RF probe to the signal generator and insert the probe onto the RF IN pad. Connect the second RF probe to the spectrum analyzer. Set the signal generator to 15 GHz and sweep from 0 – 12 dBm. Record the results in the table.

Input Power (dBm)	Output Power (dBm)
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	

Summary & Conclusions

Table 2 details the design goals versus the simulated results for the power amplifier.

Table 2: Design Goals vs. Simulated Results

Parameter	Design Goal	Predicted Results
Frequency	15 GHz	15 GHz
Gain	15 dB	13.2 dB
Pout	20 dBm	23 dBm @ 11 dBm
PAE	25%	26% @ 11 dBm

The simulated results showed that the frequency, power out and power added efficiency goals were met. The gain goal was short by 1.8 dB. At a frequency of 15 GHz it was very challenging to achieve a high gain, but the overall goal of the project was to meet the power out goal. This goal was met mainly by increasing the size of the second, power transistor in the design, but the simulated power added efficiency showed that it had acceptable efficiency for a class A design. If more time was available, inductors could have been tuned in the layout stage to meet the gain goal and increase the other parameters. Overall, this design was a success and once fabricated, the measured results should be consistent with the simulated results.

X-Band Low Noise Amplifier MMIC Design

Thomas Summers

Fall Semester 2014

Abstract

The Triquint TQP13 MMIC process was used to design a two stage low noise amplifier for operation in the X-band military satcom bands. The primary objective of the design was to minimize noise figure while maintaining high enough gain to set system noise figure. This project utilized AWR's Microwave office for simulation and layout.

Introduction

A low noise amplifier (LNA) is an important component in communication systems. Low noise amplifiers are used on the input of receivers to set the noise figure of the receiver chain (See Figure 1). To set the noise figure of the communication system there are two important parameters to low noise amplifiers, gain and noise figure. Noise figure is a measure of degradation of the signal to noise ratio that the receiver components cause. In a LNA it is important to try and get this parameter as low as possible but there is a tradeoff between gain and noise figure. Gain is also important to a LNA in order to set the system noise figure there must be sufficient gain as to make the LNA noise figure dominate the other elements in the receiver chain. Looking at the equation for cascaded noise figure in Figure 2 below one can see that the higher the gain of the first element the more the noise figure of that element dominates the system noise. Understanding these two criteria is important in LNA design as the designer must take these factors into consideration when trading noise figure and gain.

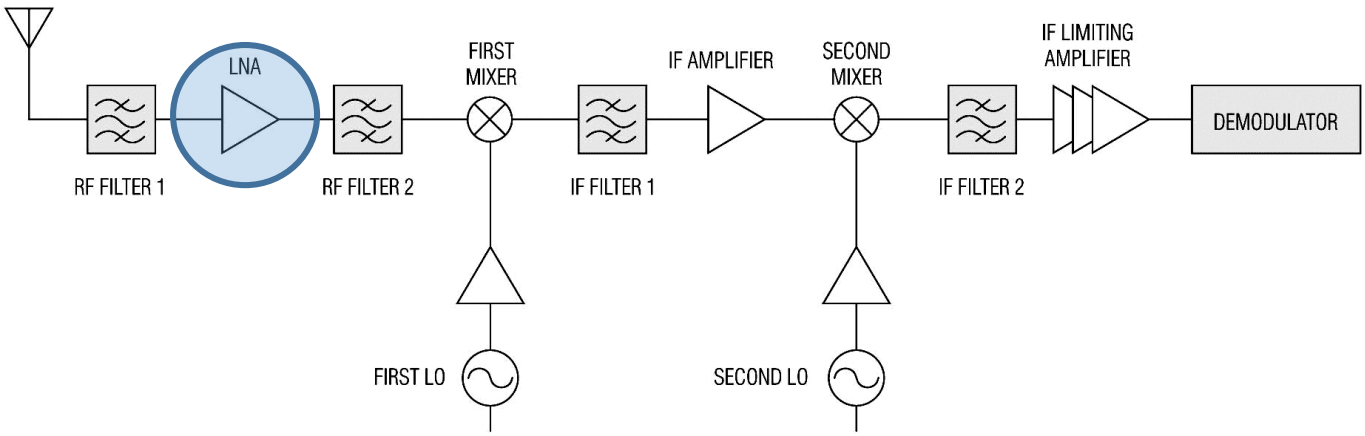


Figure 1. Receiver Block Diagram

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_{n-1}},$$

Figure 2. Cascaded Noise Figure Equation

Design Specifications

Frequency: 7.25-7.75 GHz and 7.9-8.4 GHz

Noise Figure: ~1dB

Gain: >15dB

Return loss: <-15dB for both S11 and S22

Biasing: Single voltage

Design Approach

To begin the design the first step taken was to determine how much transistor size affected minimum noise figure. Beginning with the S-parameter files provided by Triquint it looking at the 4x50 um pHEMT and 6x50 um pHEMT devices there was little improvement in the noise figure at the frequencies of concern. It was decided to go with the 6x50 um pHEMT as it was thought that the larger device would yield a better 1dB compression point.

First Stage Design

After deciding upon using the 6x50 device the next step was to design the first stage of the amplifier. Since the first stage's noise figure would dominate the following stages the decision was made to focus on matching for minimum noise figure. Next biasing had to be considered, to simplify the design it was decided to provide a V_{GS} = 0V and a V_{DS} = 3V. This was chosen for two reasons, first this biases the device in at a good level for low noise applications. Second there already existed measurement files from Triquint with the device biased in this manner giving a high degree of confidence in the linear simulations. Next the device was stabilized, after many iterations it was determined that drain stabilization would not be enough to ensure stabilization at the lower frequencies. To get around this a resistor was added to the gate side in parallel with a bypass capacitor to short the resistor out for higher frequencies. The input match was then designed to provide the lowest noise figure and finally the output was conjugate matched. When at all possible in this design when matching the drain side the decision was made to have an inductor to ground and a capacitor in series, this allows for biasing without having to add more inductors and bypass caps. The final design of the first stage can be seen in Figure X.

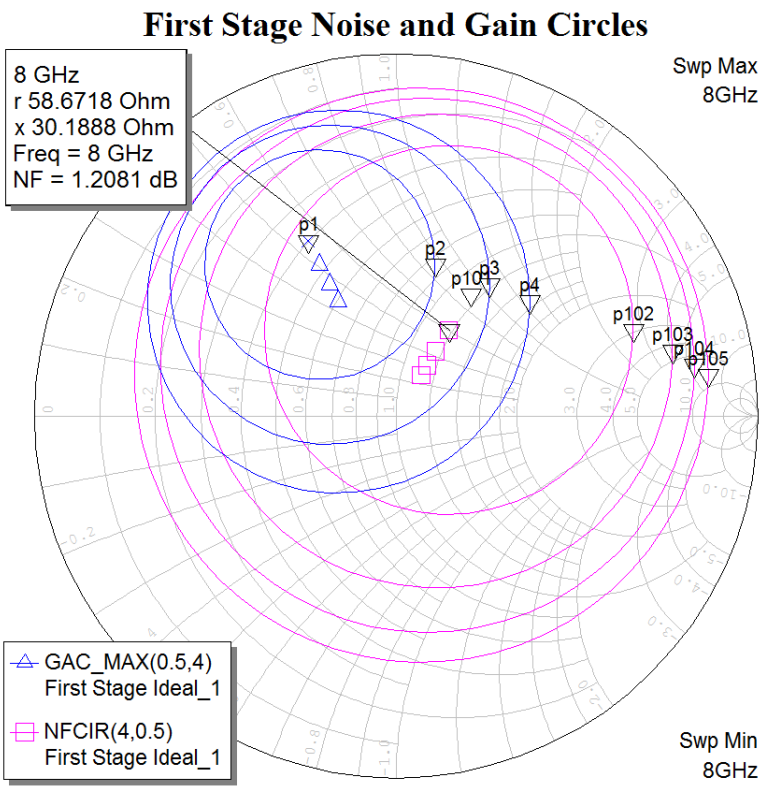


Figure 3. Noise and Gain Circles

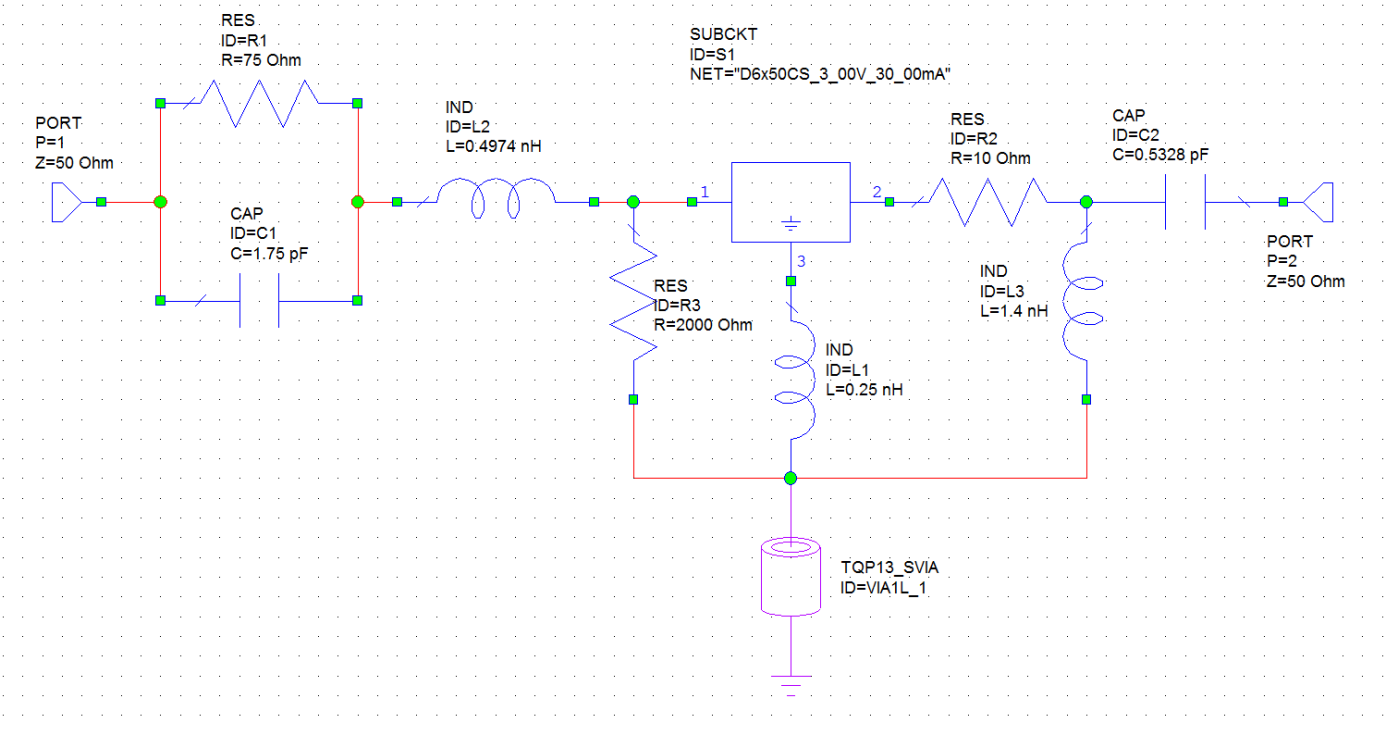


Figure 4. First Stage Ideal Schematic

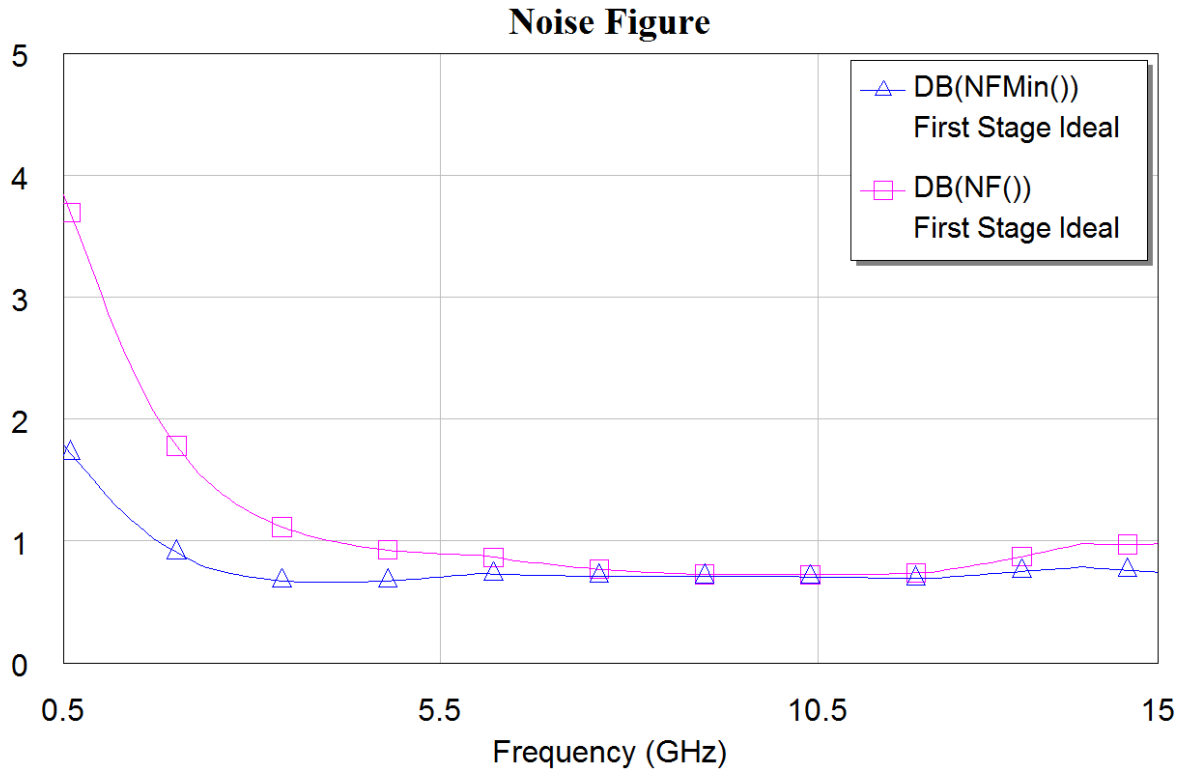


Figure 5. First Stage Ideal Noise Figure

Second Stage

The second stage was originally designed to have the highest gain possible while providing decent noise figure. After several iterations it was determined that to keep the total LNA noise figure at about 1 dB that the second stage would need a noise figure of less than 1.5 dB. This decision lead to a similar design to the first stage, the biggest difference in the second stage was that the gate resistor was removed. In the end the second stage had similar performance to the first stage but with improvement to S22.

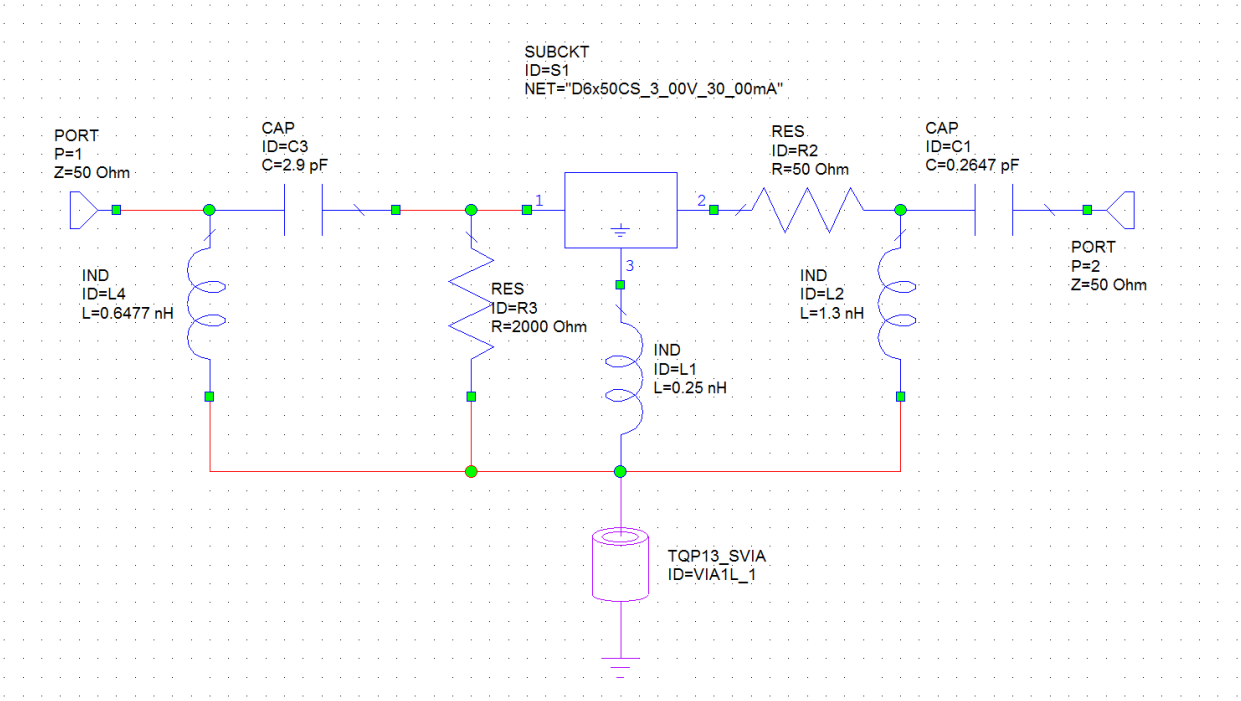


Figure 6. Second Stage Ideal Schematic

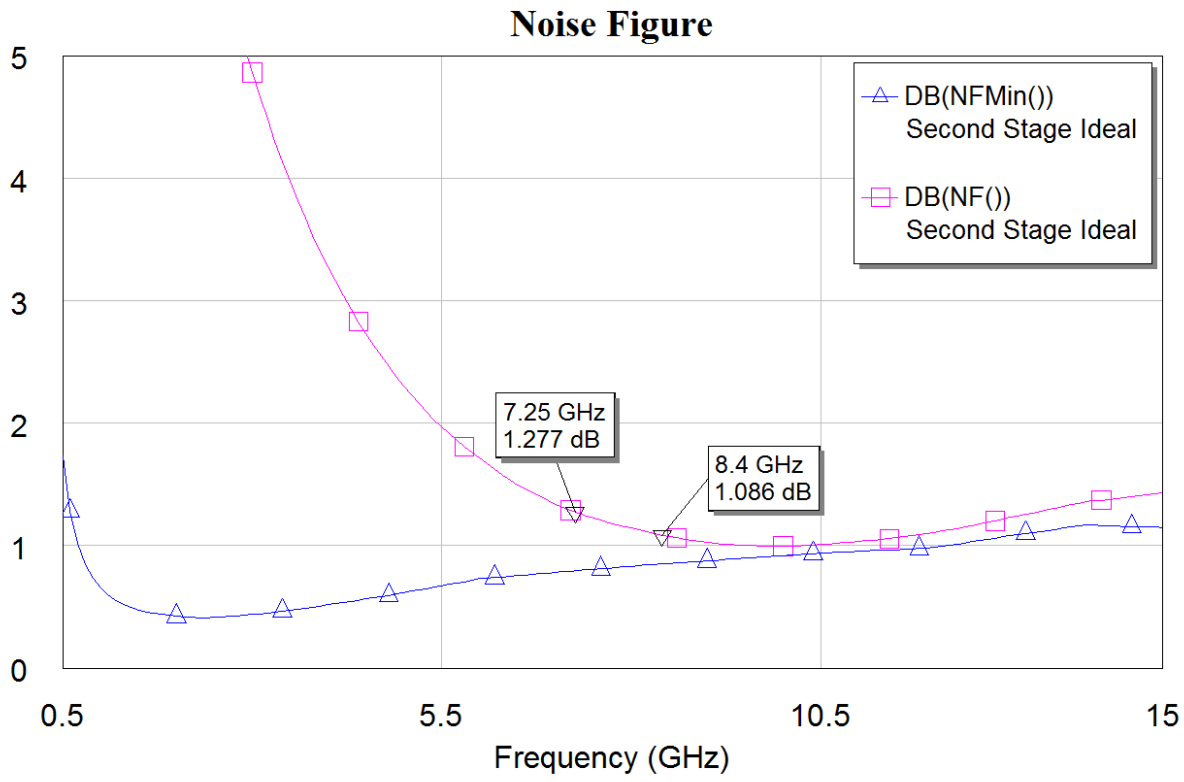


Figure 7. Second Stage Ideal Noise Figure

Combined LNA

In combining the two LNA stages the interconnecting stages can be simplified. By combining the output matching of stage 1 and the input matching of stage 2 it was possible to eliminate the need of an inductor and a capacitor reducing the total size of the MMIC. The final combined schematic can be seen in Figure X.

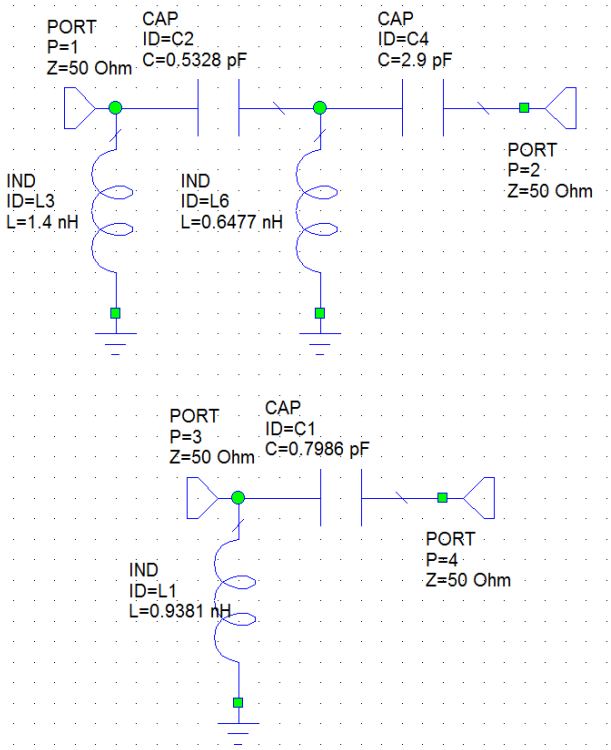


Figure 8. Interstage Match (Top: Initial Bottom: Simplified)

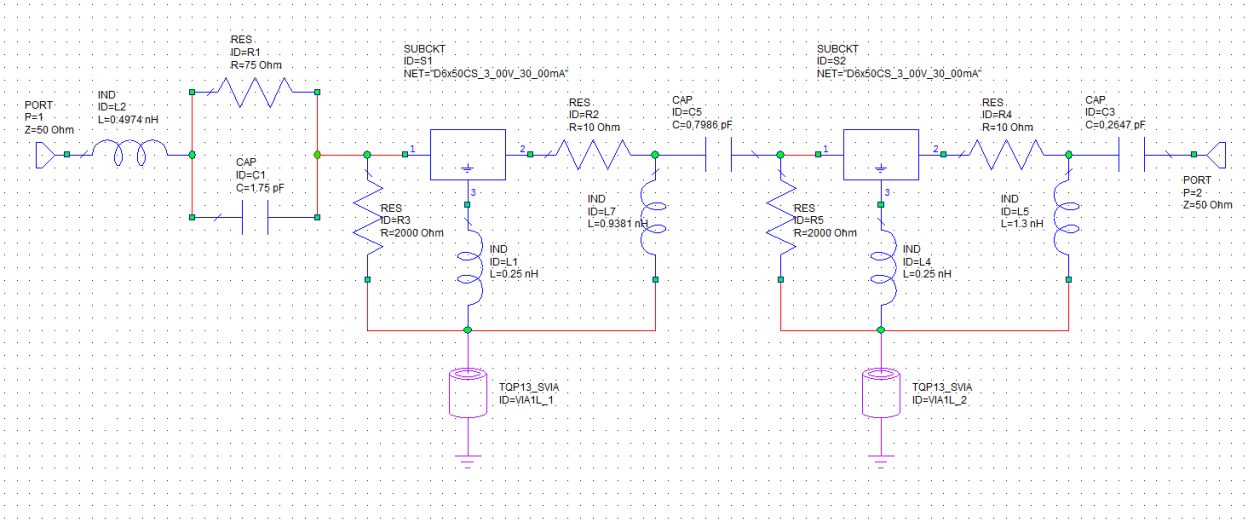


Figure 9. Final Design Ideal Schematic

Simulations

After combining the two ideal stages and simplifying the interstage match the combined performance was simulated to ensure that the goals of the design were still being met. Figures 10-11 show the S-parameters and noise figure of the combined ideal design respectively. As can be seen from the simulations the majority of design parameters were met. The only exception was the input and output matching but the only way to improve these parameters degraded noise figure. Since noise figure was the primary goal of this design it was decided to accept the return loss.

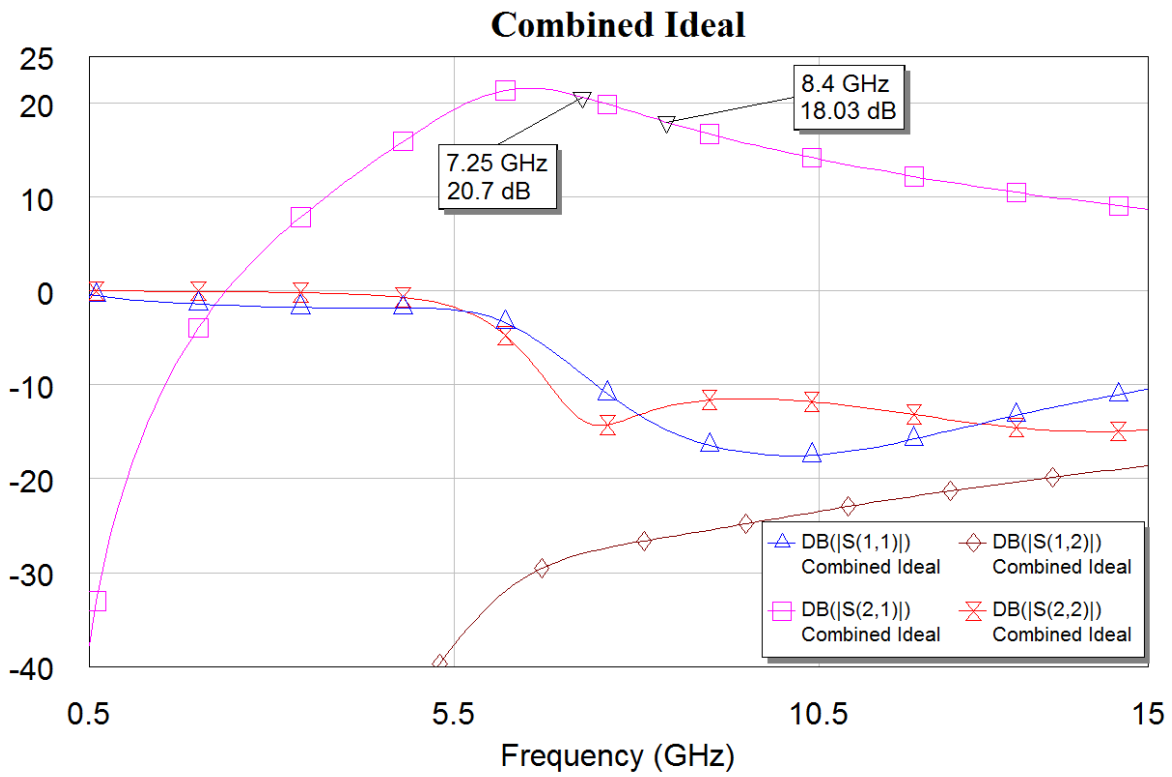


Figure 10. Ideal S-Parameters

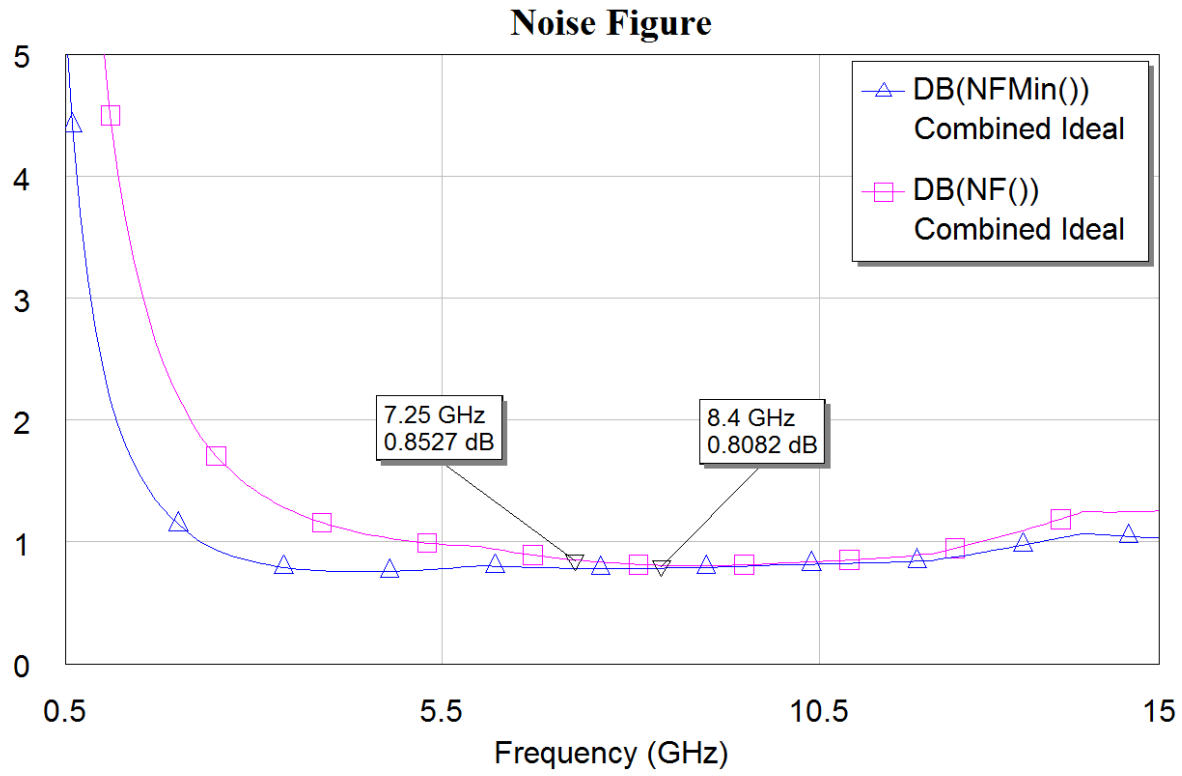


Figure 11. Ideal Noise Figure

After determining the performance of the combined ideal design the next step was to replace the ideal components with Triquint elements and layout the design. Figures 12-15 show the S-parameters, noise figure, stability and power compression of the final design with Triquint elements and interconnecting lines.

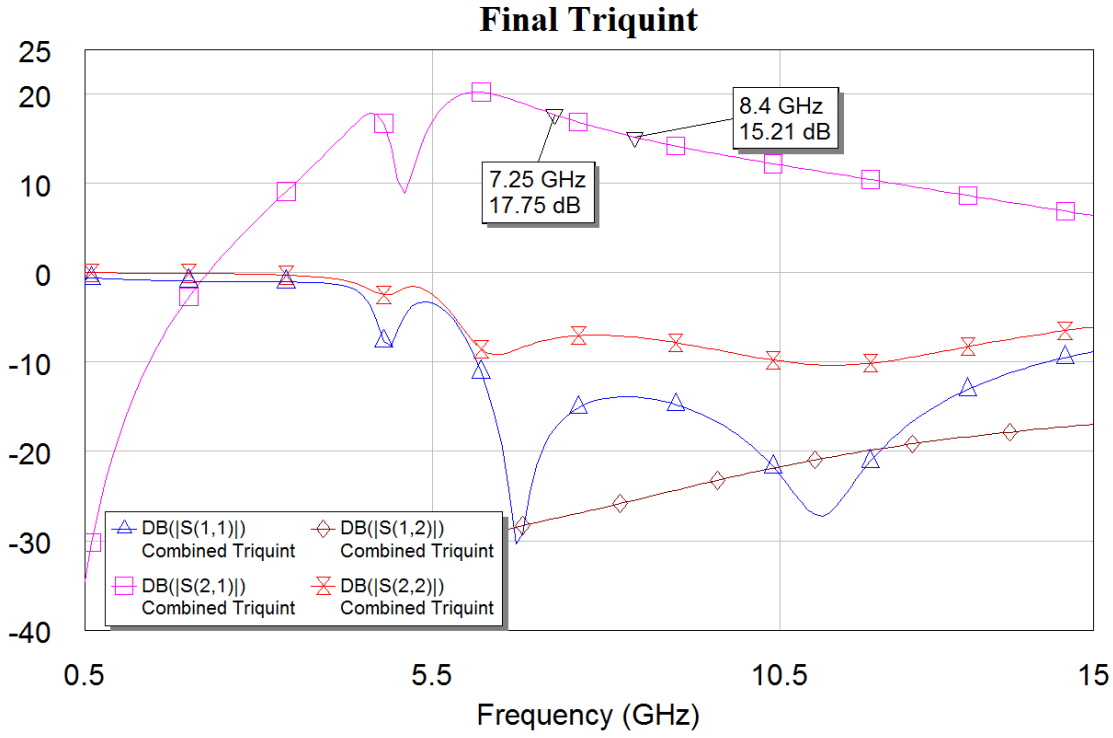


Figure 12. Final S-Parameters

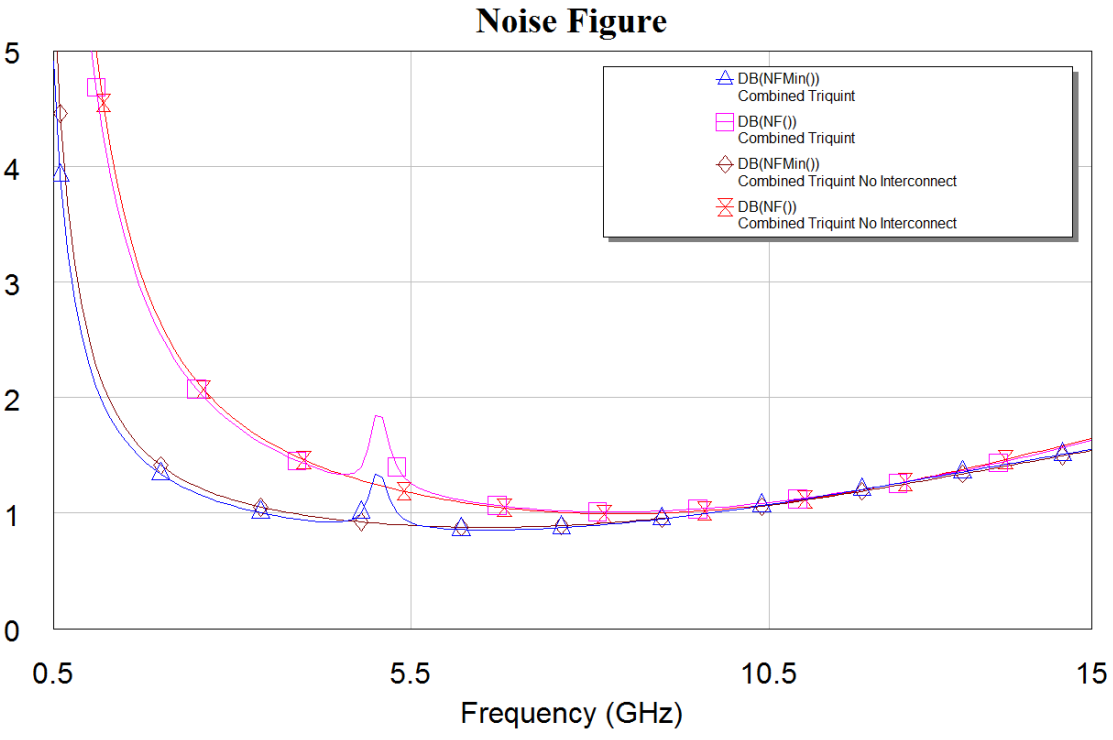


Figure 13. FInal Noise Figure

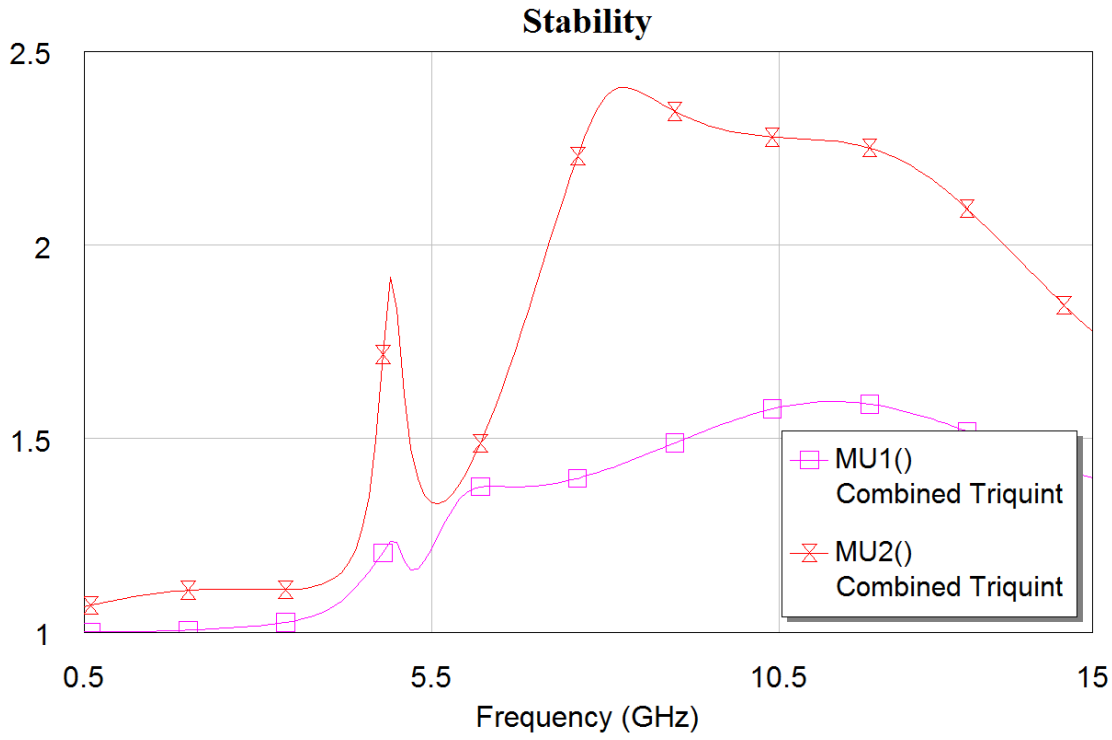


Figure 14. Final Stability

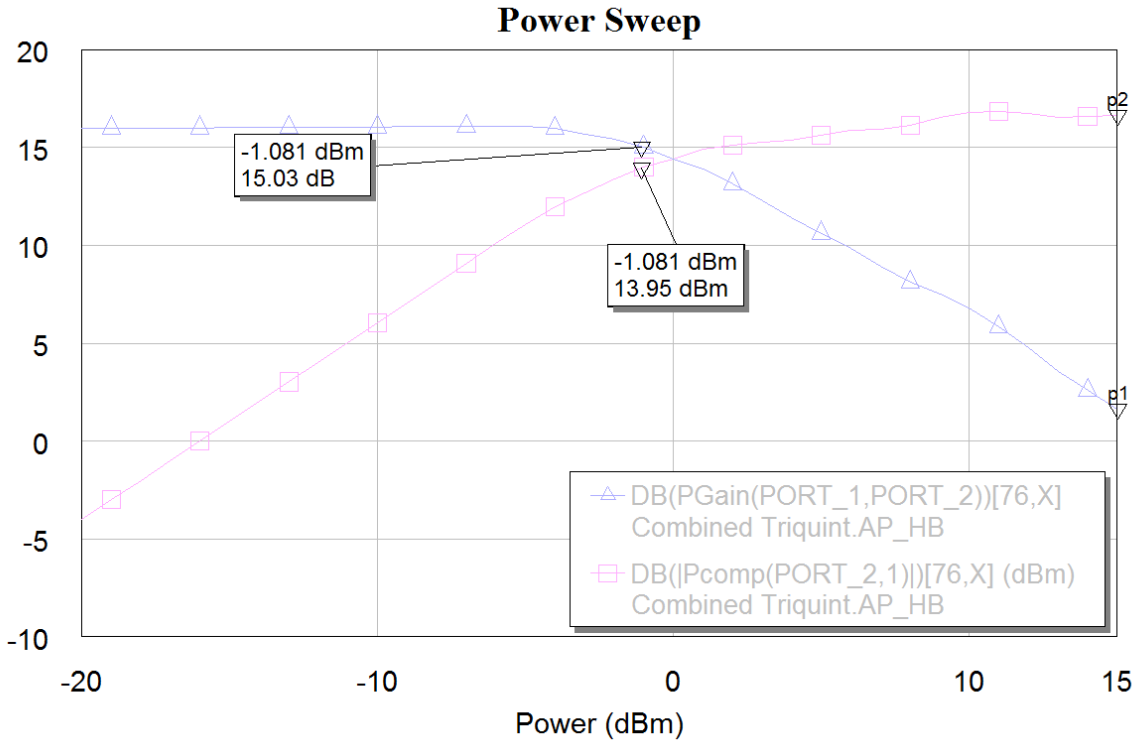


Figure 15. Final Input Compression Point

Schematics

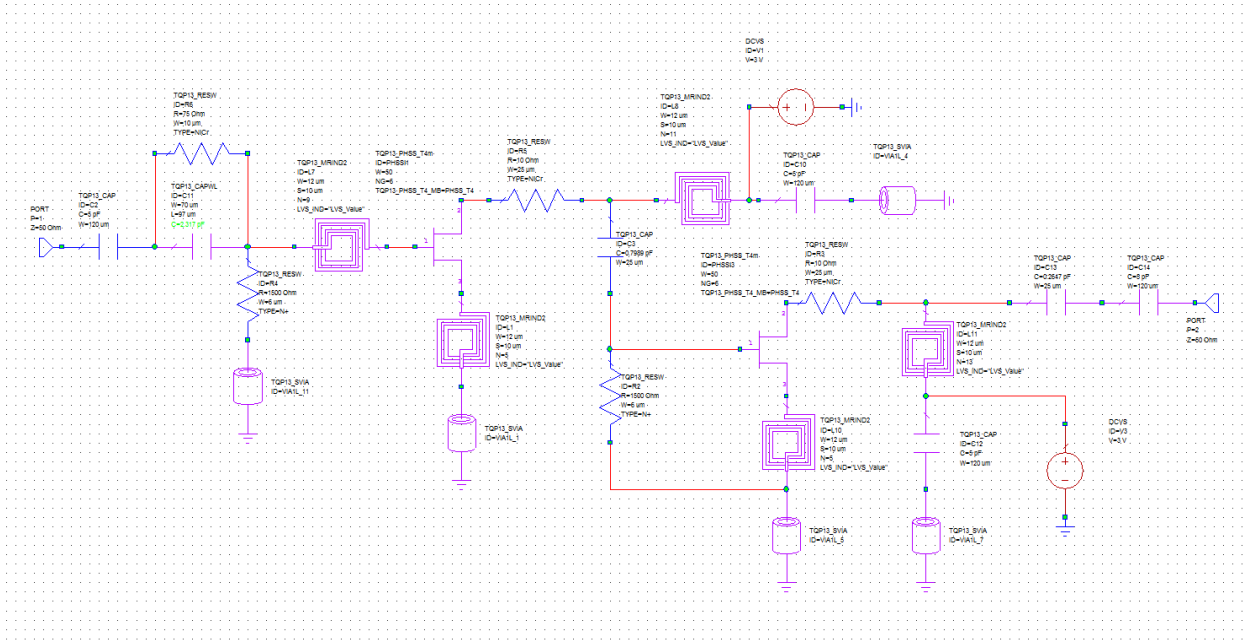


Figure 17. FInal Schematic No Interconnects

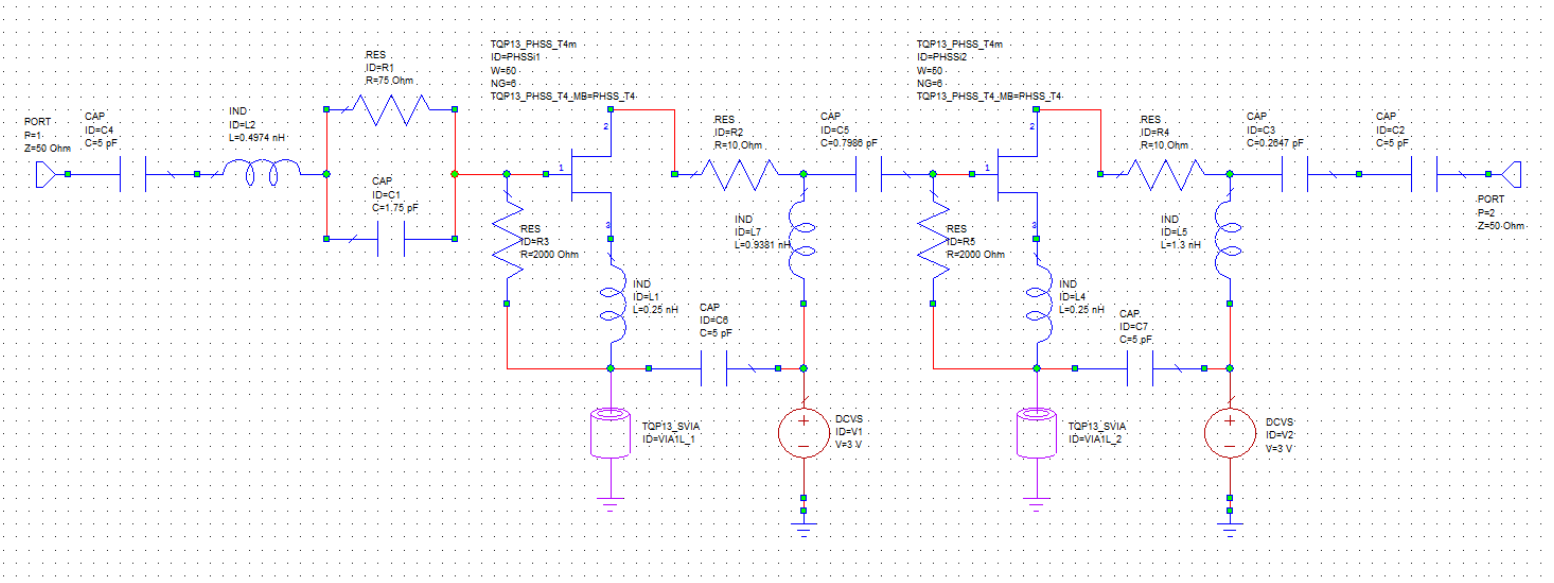


Figure 16. Final DC Schematic

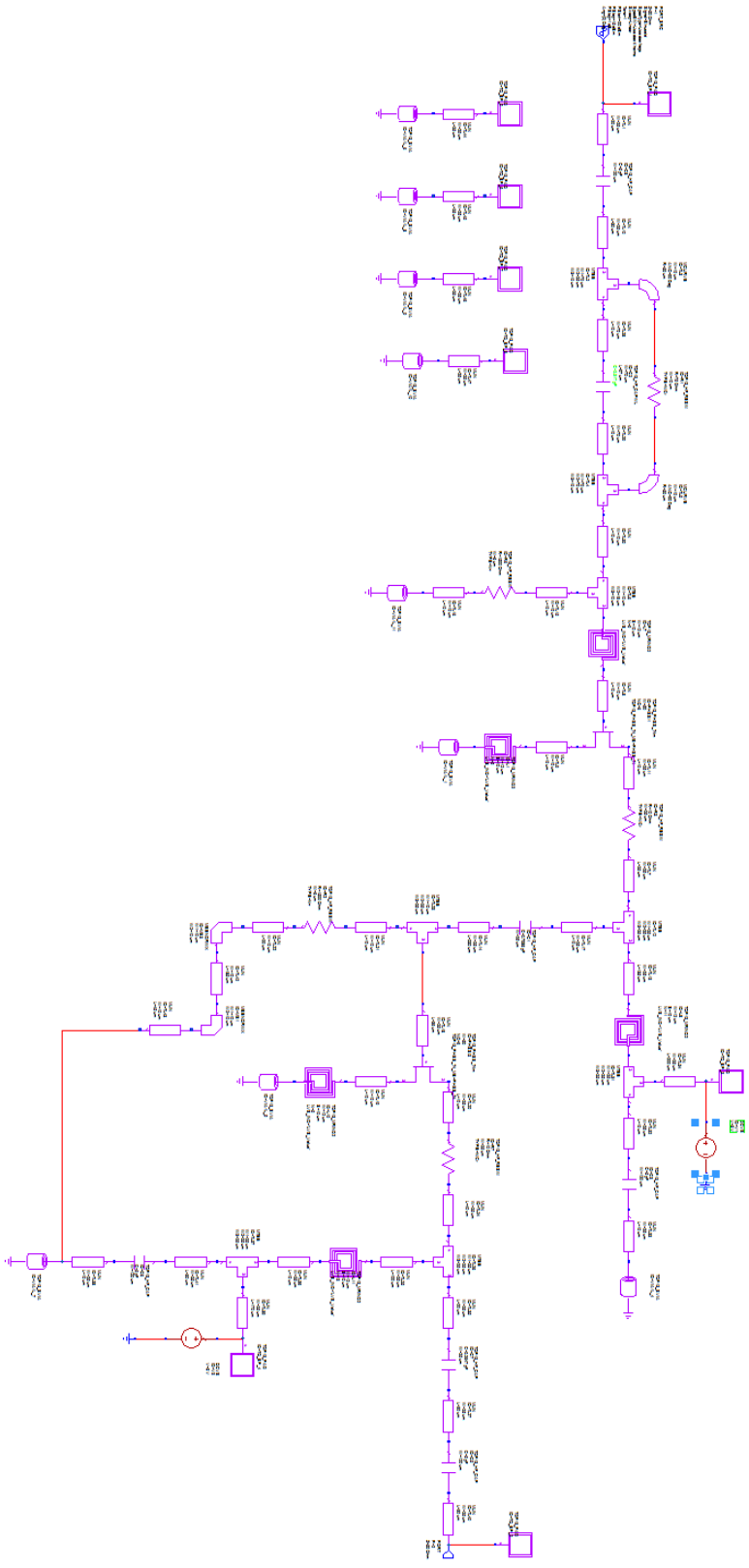


Figure 18. Final Schematic with interconnects

Layout

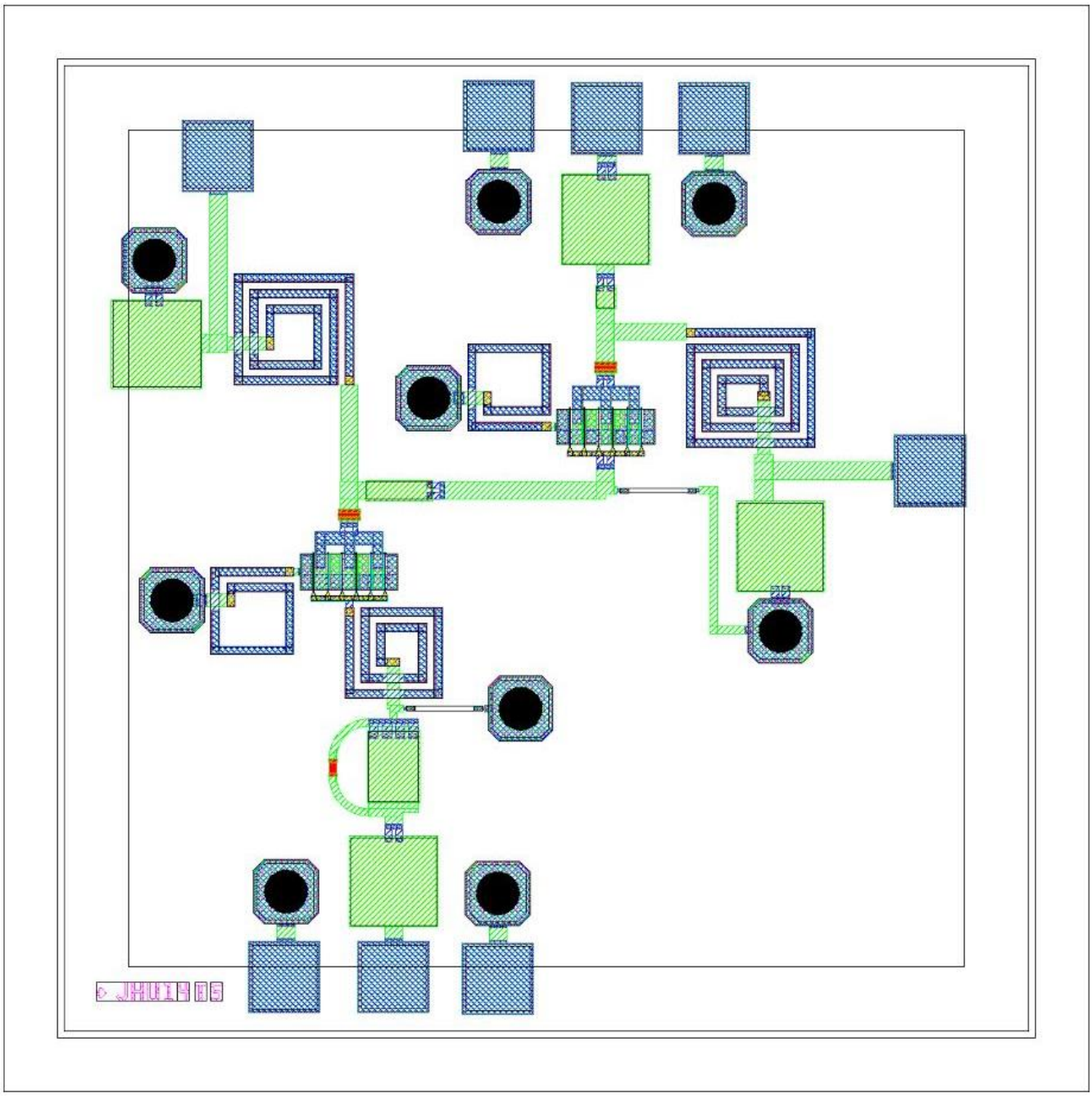


Figure 19. Final Layout

Test Plan

Test Equipment:

1. Two DC Power Supplies
2. Probes (RF and DC)
3. Network Analyzer
4. RF Signal Generator
5. Spectrum Analyzer
6. Noise Source
7. Noise Figure Meter

S-parameter Measurement

1. Connect each DC power supply to each drain pad and verify current (approximately 27mA)
2. Calibrate network analyzer
3. Connect RF probes to MMIC input and output
4. Measure S-parameters and verify results with simulated data

Power measurement

1. Connect RF signal generator to input of LNA
2. Connect output of LNA to spectrum analyzer
3. Starting at -20 dBm increment RF power by 1 dB until reaching 15 dBm
4. Compare measured results with simulation

Noise Figure Measurement

1. Calibrate noise figure meter
2. Attach noise source to input of LNA
3. Attach out of LNA to noise figure meter
4. Compare results with simulated data

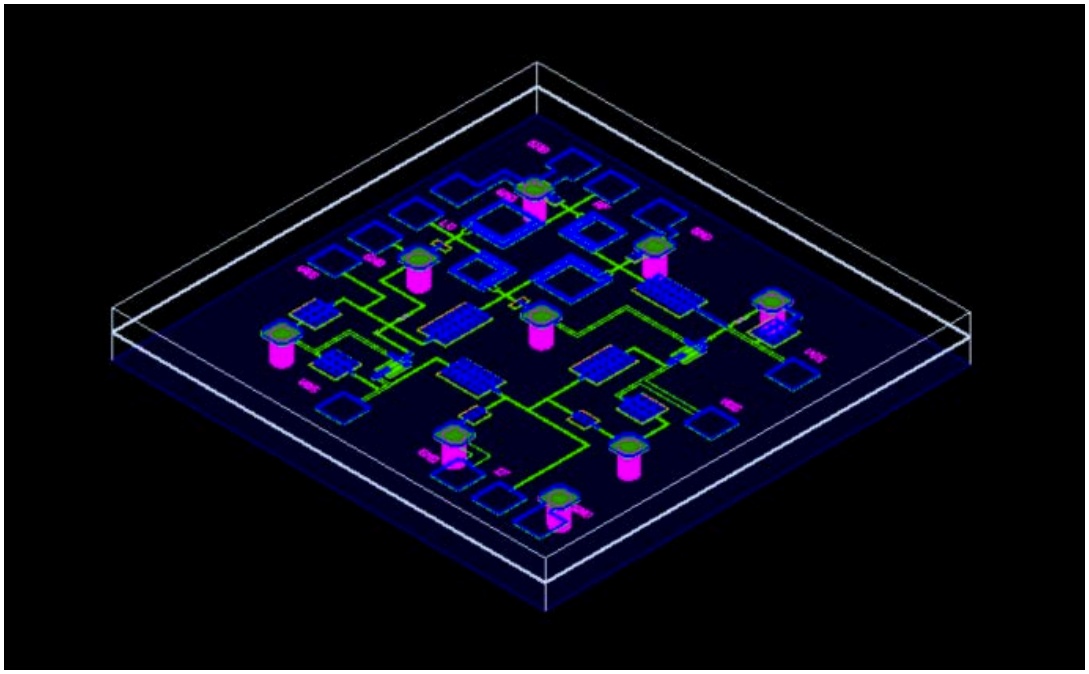
Summary

Summary of goals and simulated results

	Goal	**Simulated**
Noise Figure	**~1 dB**	**1.18 dB**
Gain	**15 dB**	**15.21 dB**
S11	**-15 dB**	**-13.9 dB**
S22	**-15 dB**	**-6.9 dB**

In conclusion using Microwave Office and techniques learned in the MMIC design course I was successfully able to design and layout a low noise amplifier in the X-band military satcom frequencies while meeting a majority of the goals set at the beginning of the design.

Single Balanced FET Mixer



MMIC Design
Fall 2014
Asia Mason

I. Abstract

The purpose of this design is to create a balanced FET mixer using TriQuint's process. The mixer will be producing a high side injection down conversion and has a RF frequency of 21 GHz. The IF frequency is 1.5 GHz and the LO is 22.5 GHz. The design approach in this paper analyzes FET mixers that incorporate a branch-line coupler, Wilkinson power divider, and low pass filter. The responses that will be analyzed are the S-parameters, conversion loss, and power levels. The final design successfully met all of the design goals.

II. Introduction

A mixer is a device used for frequency conversion. It has three ports, two for input signals and one for an output signal. Mixing takes place by multiplying a RF/IF signal with an LO and taking the sums and differences of their frequencies. A nonlinear device such as a FET, or a time-varying device such as a switch is used for converting the input signals. The two types of mixer conversions are up-conversion and down-conversion. With up conversion, a low frequency is converted to a larger frequency while down conversion converts a high frequency to a lower frequency. In a transceiver chain, transmitter use up-conversion mixers and receivers use down conversion mixers. The FET mixer in this design is a down conversion.

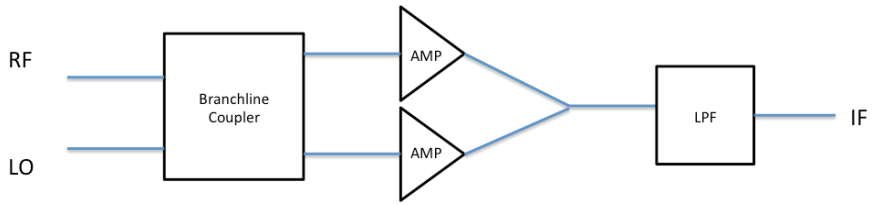


Figure 1: Single Balanced FET Mixer

III. Design

A. Design Goals

- RF= 21 GHz
- LO= 22.5 GHz
- IF= 1.5 GHz
- RF power < 0 dBm
- LO power <11 dBm
- Conversion Loss< 10 dB

B. Single Ended FET Mixer

To begin the process, it was decided that a single ended FET mixer should be designed using ideal components in order to ensure that the FET portion of the design is working properly. The analysis of a smaller design is simpler to trouble shoot than the fully cascaded design. A Wilkinson combiner is the first circuit in the design, and is created at 21 GHz.

Next, the FET curve tracer was used to view the IV curves for the pHEMT. From there, the bias point chosen was Vgs=-0.2 V and Vds=2 V. The transistor was then biased and the load

and source stability circles as well as the stability factor were plotted to establish that a stability network was needed. A series 30-ohm resistor and a shunt 150-ohm resistor at the gate were used to form the stability network for unconditional stability. Input and output matching networks were then created using a simultaneously conjugate match at IF 1.5 GHz. The input-matching network has a series 1.1 pF capacitor and a shunt 6.1 nH inductor. The output-matching network has a series 0.325pF capacitor and a shunt 19.8 nH inductor.

An ideal low pass filter is at the output of the mixer in order to filter out harmonics at higher frequencies. The low pass filter design has a capacitor and inductor pi network topology. After the Wilkinson, FET circuit, and low pass filter were cascaded, a RF power of -20 dBm and LO power of 5 dBm were applied at the inputs of the design. The IF output displayed a power of -22.583 dB. The conversion loss for the design was -2.583 dB.

C. Tuned Values

The ideal lumped components were replaced with TriQuint elements and tuning was needed to achieve results closer to the ideal response. The components that were optimized included the capacitors and inductors for the input and output matching networks. The inductors were replaced with high impedance lines because the inductance values were so large that there would be a spacing issue. The widths of the high impedance lines were tuned to 1.185nm at the input and 0.755nm at the output. The capacitor at the input was tuned to 5.8 pF and the output was 5 pF. Next, the drain voltage and the input power levels were optimized. The drain voltage became 3 V, RF increased to -10dBm, and LO increased to 10 dBm. The inductor for the low pass filter was also replaced with a high impedance line with a width of 1.2 um, and the capacitors were decreased to 1.15 pF. Another parameter that was optimized in order to improve the conversion loss was the size of the device. It was changed from 6x50 um to 2x80um.

D. Single Balanced FET Mixer

For the Balanced FET Mixer, the topology begins with the design of a branchline coupler at RF frequency 21 GHz. The FET along with its biasing, stability, and matching networks were attached to ports 2 and 3 of the branchline coupler. The FET circuits connected to branchline ports were identical. The output of the FET circuits were both connected to the low pass filter at the IF port. The conversion loss of the final cascade was about 7.45 dB, which is lower than the design goal of <10 dB. When the circuit was converted to layout, the capacitors appeared to be long such that those dimensions would be seen as a microstrip line as opposed to a capacitor. The lengths and widths were optimized to obtain a more square shaped capacitor and the final conversion loss became 8.314 dB when the RF input powere is -10 dBm and the LO input power is 10 dBm. This value still fell below the design spec of no more than 10 dB of loss.

E. Tradeoffs:

A few trade offs were made during the design process. The decision to create a single balanced FET mixer instead of a single ended FET mixer because it has the ability to provide better isolation and matching depending which four port coupler is used at in the topology. A design the uses a rat-race coupler has improved isolation, while the design that uses the branchline coupler had improved matching. Due to the amount of stage in the full design, the branchline was chosen to assist with matching.

Single balanced mixers also have the option to use either FETs or diode to create mixing. The device chosen was a FET because it is expected to provide a smaller conversion loss than a diode, and sometimes even a gain. When the final cascading the final design, it was noticed that the higher frequency harmonics were not filtered out very well. However, as the filter was tuned to suppress the harmonics more, the conversion loss increased. The conversion loss was a higher concern so the filter was returned to its previous value.

IV. Schematic/ Simulations

A. Single Ended FET

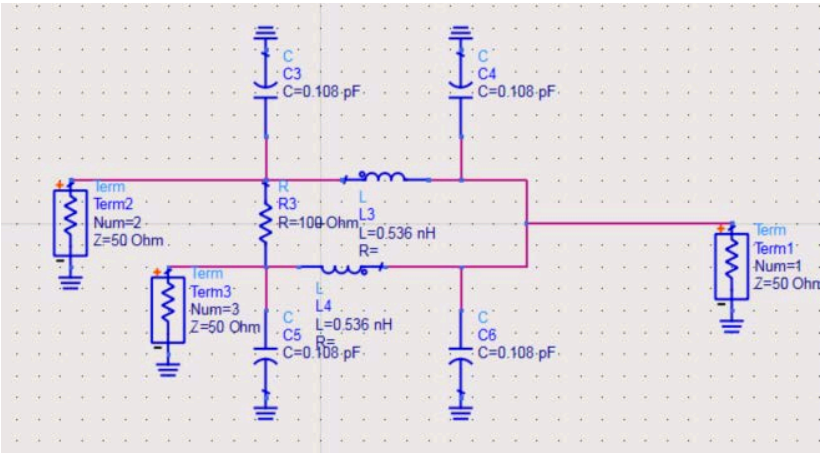


Figure 2: Wilkinson combiner

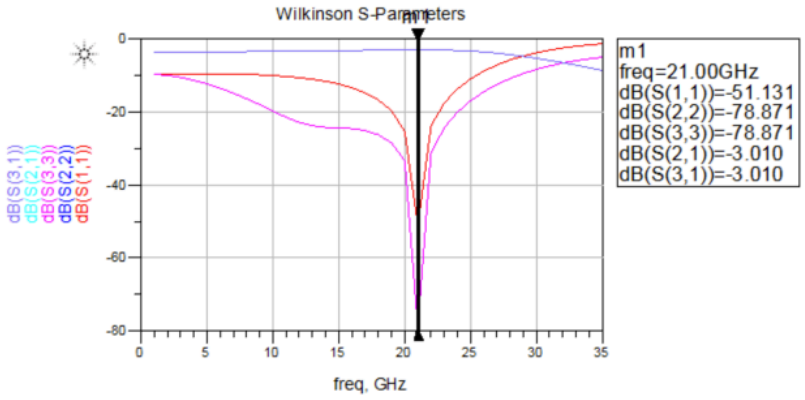


Figure 3: Wilkinson combiner S-Parameter response

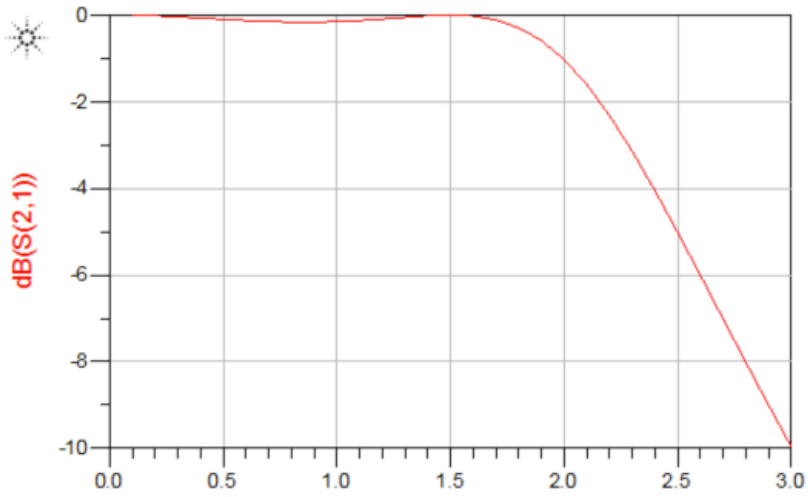


Figure 4: Low pass filter response

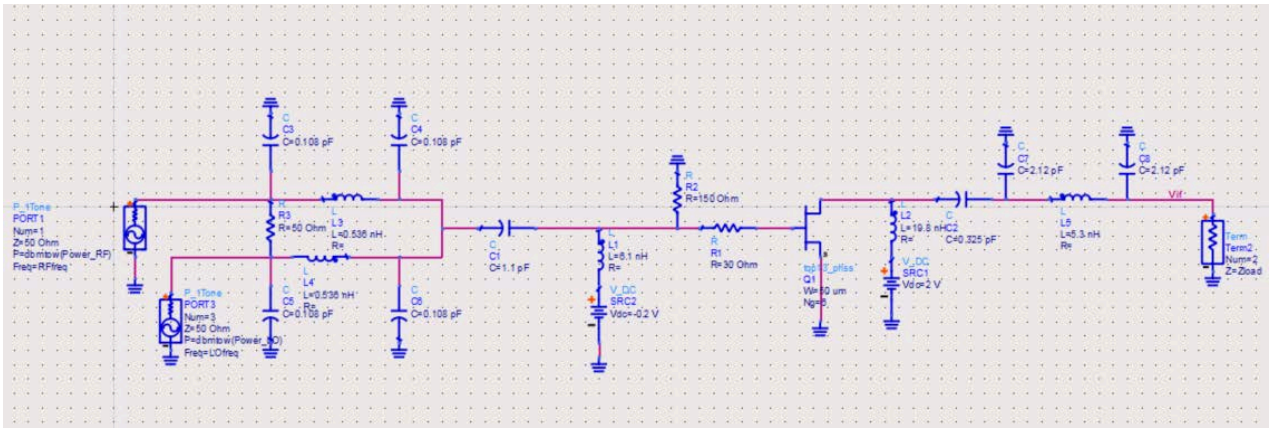


Figure 5: Ideal Single Ended FET Mixer

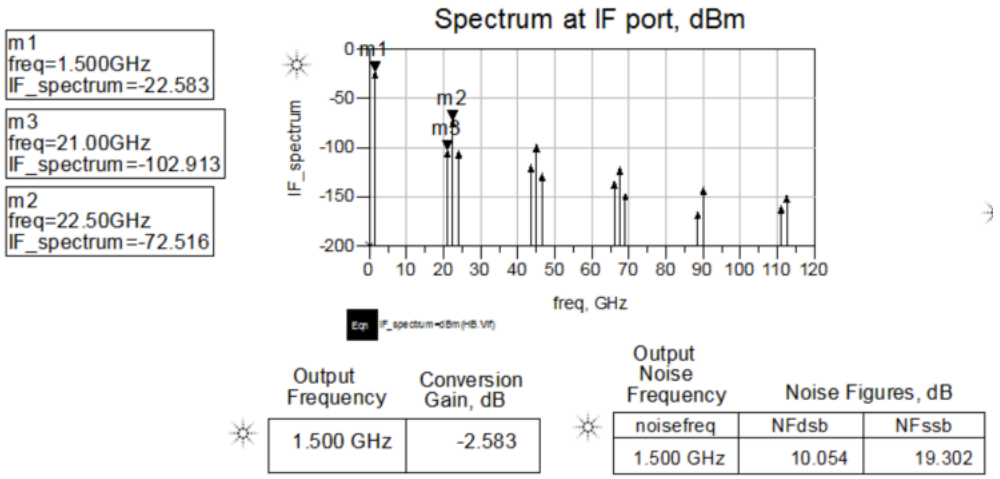


Figure 6: Ideal Single Ended FET response when RF=-20 dBm, LO= 5dBm

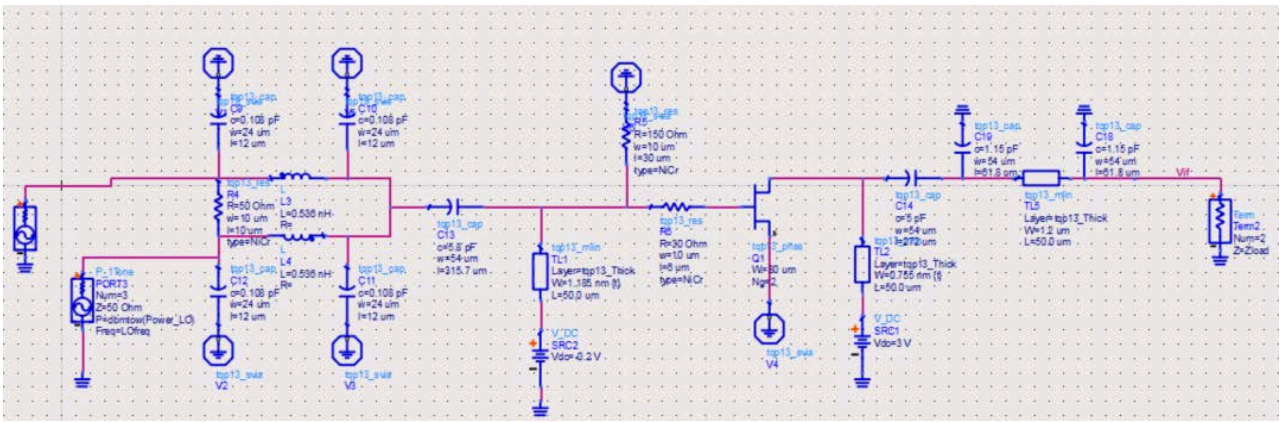


Figure 7: Non-Ideal Single Ended FET Mixer

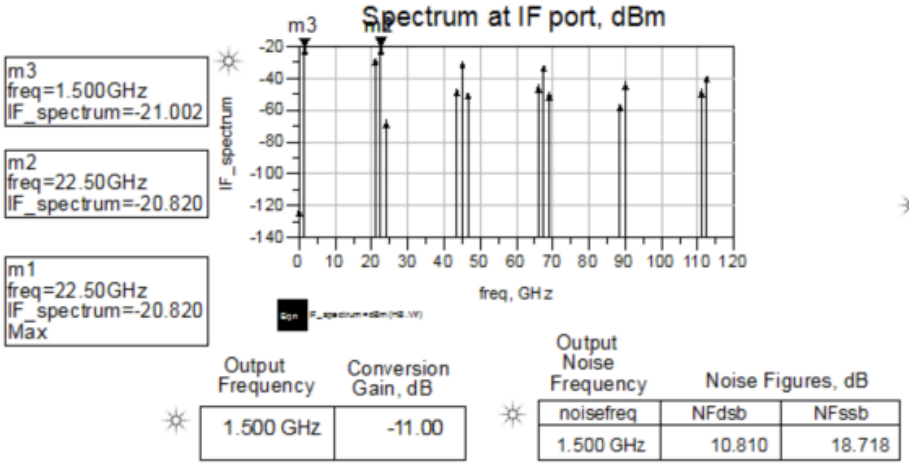


Figure 8: Non-Ideal response when RF=-10 dBm, LO=10 dBm

B. Single Balanced FET Mixer

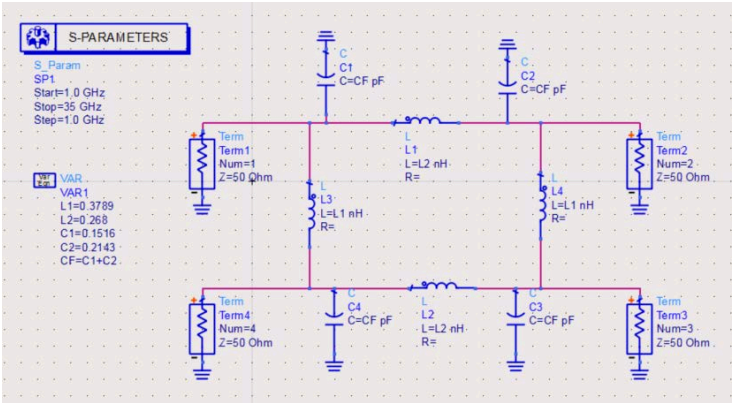


Figure 9: Branchline coupler designed at 21 GHz

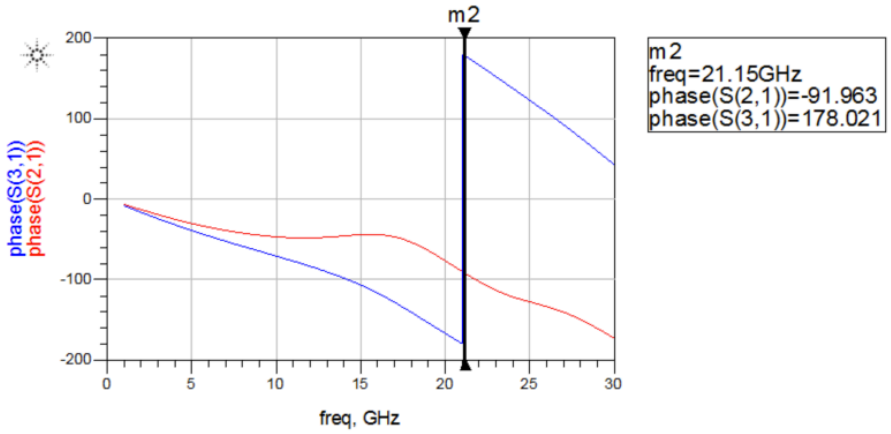


Figure 10: Display of 90-degree phase for branchline

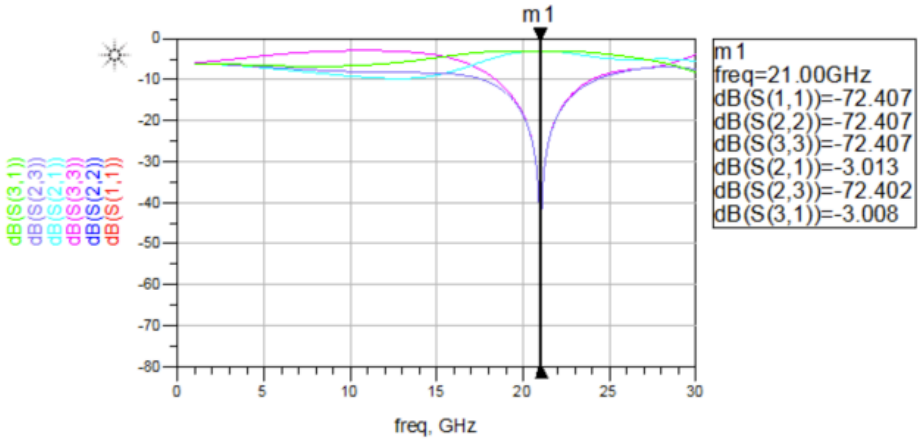


Figure 11: S-Parameters of branchline

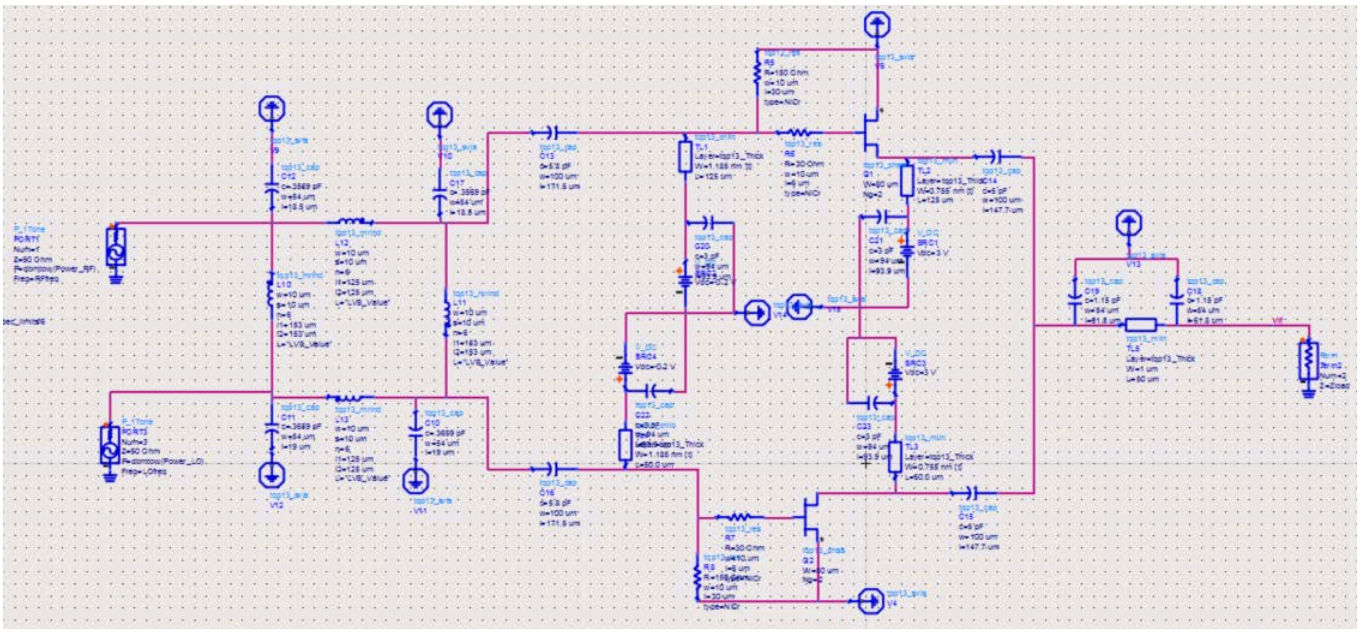
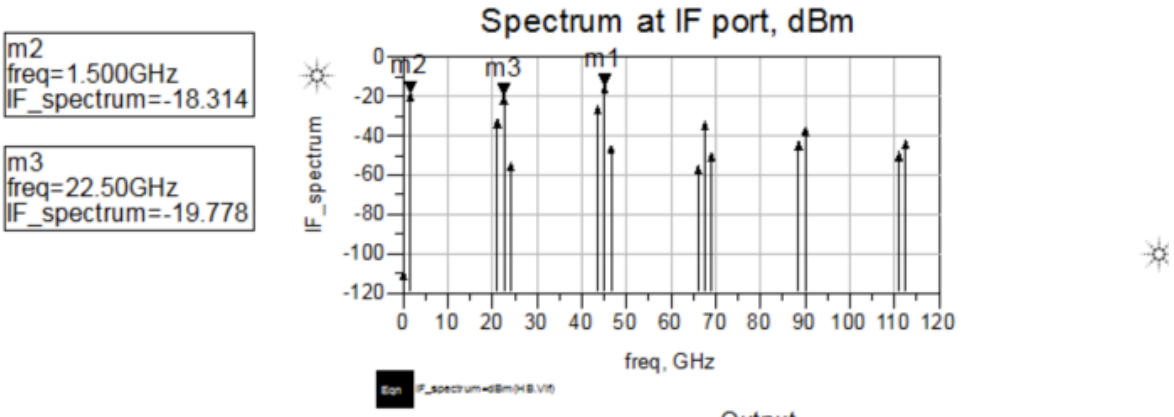


Figure 12: Final Single Balance FET Mixer Schematic



Output Frequency	Conversion Gain, dB
1.500 GHz	-8.314

Output Noise Frequency	Noise Figures, dB	
noisefreq	NFdsb	NFssb
1.500 GHz	9.441	20.335

Figure 13: Final Circuit Harmonic Balance Simulation

A sweep of the LO power was completed and plotted vs. conversion gain for several set RF values. The RF values included -10 dBm, -20 dBm, -40 dBm, -45 dBm, and -50 dBm. For RF input powers from -10 dBm to -40 dBm, the best conversion gain loss was between 8 dB and 9 dB at LO power of 10 dBm. At RF of -45 dBm and -50 dBm, the best conversion loss was at an LO power of about 19 dBm, which is well above the design goal of being less than 11 dBm.

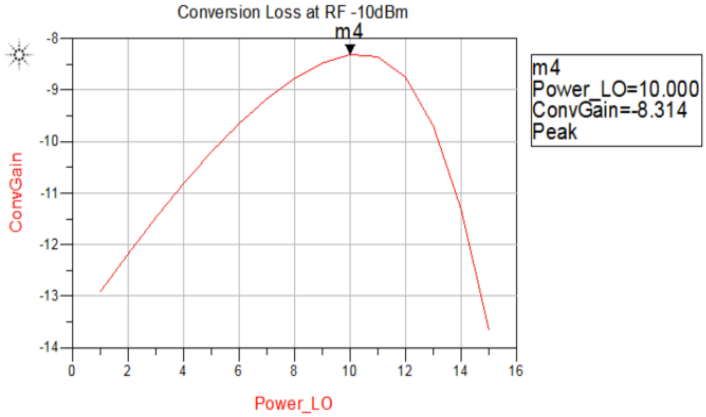


Figure 14: LO Power Sweep for RF =-10 dBm

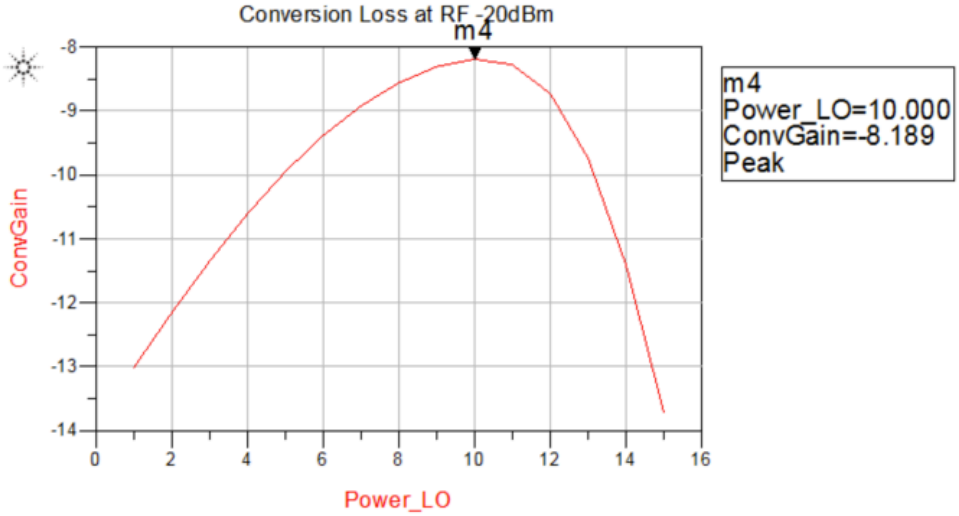


Figure 15: LO Power Sweep for RF =-20 dBm

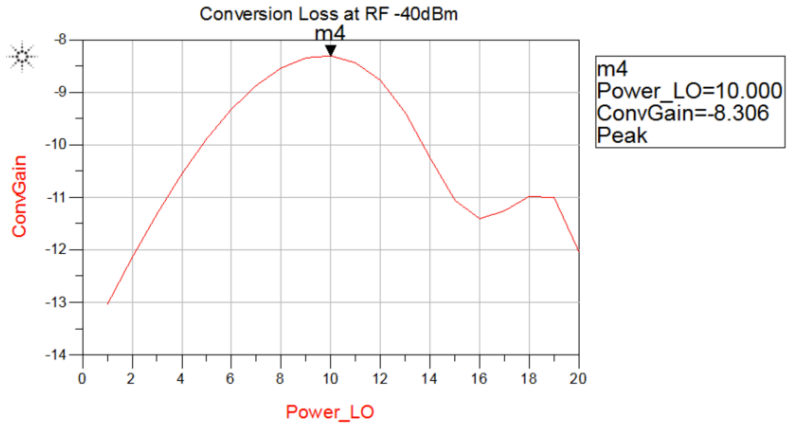


Figure 16: LO Power Sweep for RF =-40 dBm

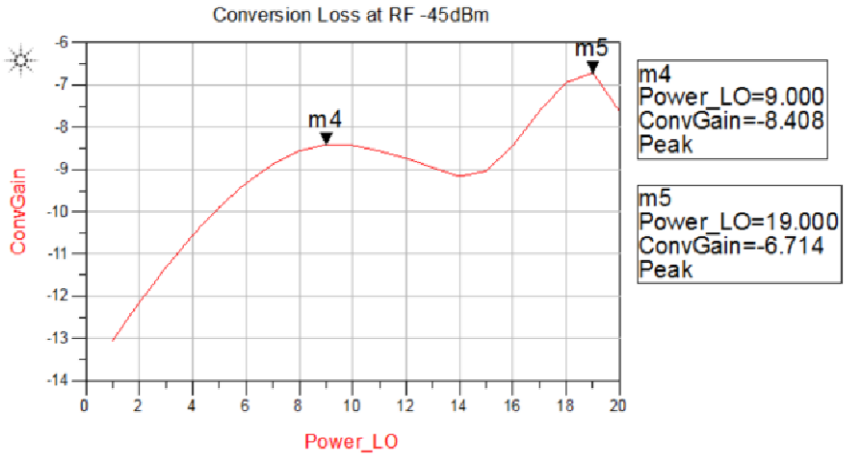


Figure 17: LO Power Sweep for RF =-45 dBm

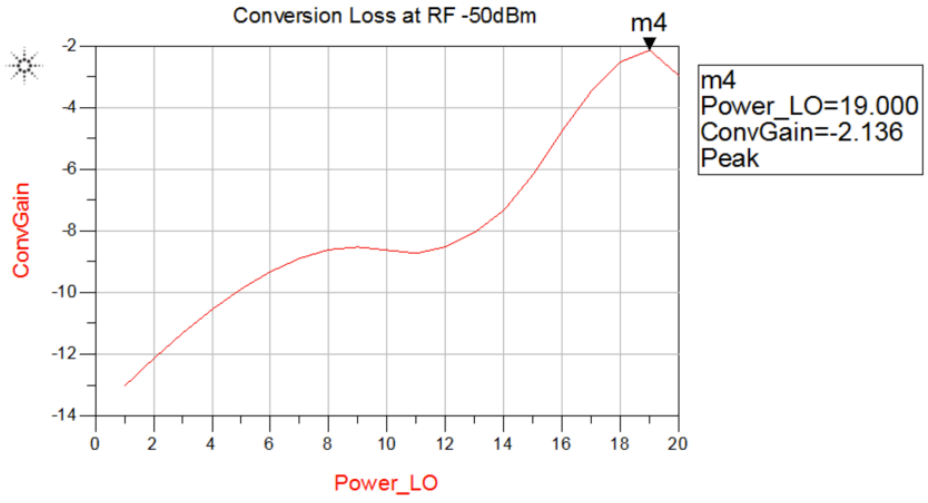


Figure 18: LO Power Sweep for RF =-50 dBm

V. Layout

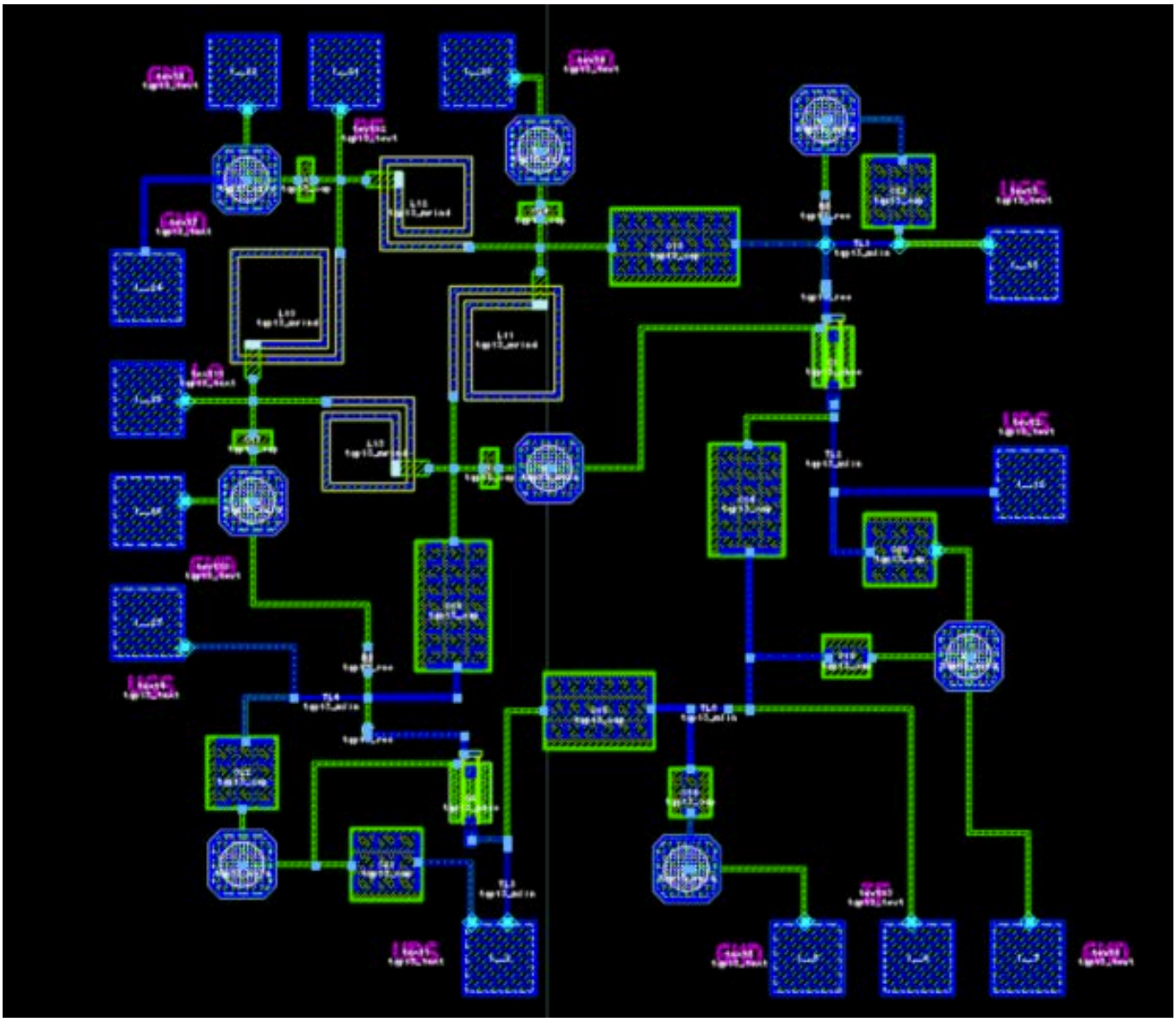


Figure 19: Layout before DRC checks

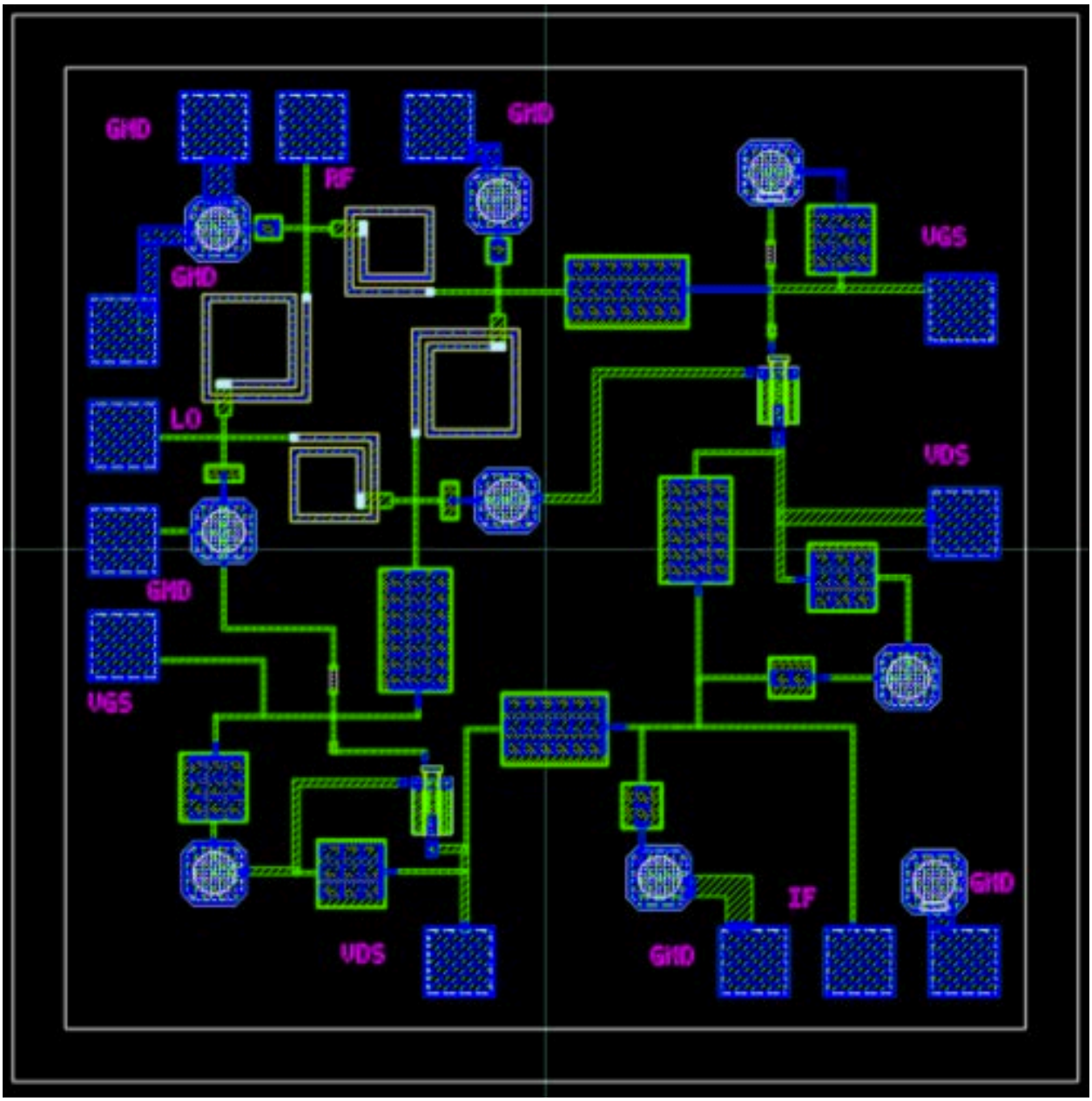


Figure 20: Final layout after DRC and LVS checks

VII. Test Plan

1) Properly connect all grounds.
2) Apply -0.2 V to the gate of the FETs
3) Apply 3 V to the drain of the FETS
4) Connect GSG probes to RF, LO, and IF ports
5) Apply RF--10 dBm and LO=10 dBm
6) Measure conversion loss at IF port (expect between 8 dB and 9 dB)
7) Remember to account for cable loss
8) LO sweep from 1-20 dBm vs. conversion gain for the following RF values: -10 dBm, -20 dBm, -40 dBm, -45 dBm, and -50 dBm.

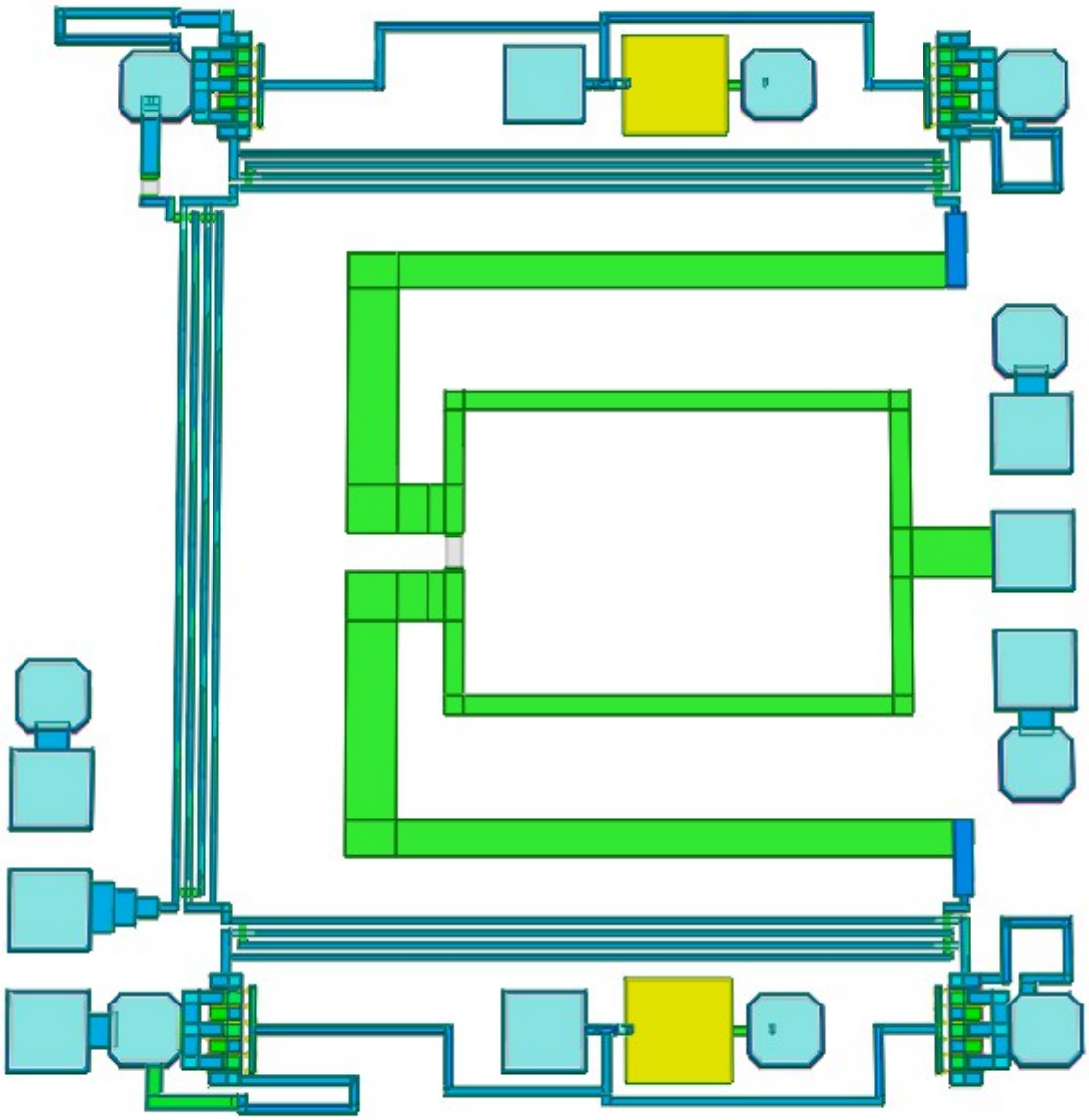
VIII. Summary/ Conclusion

This paper discussed the design of a Single Balanced FET Mixer. Table 1 displays a comparison between the design goals and the values achieved. The topology used for this mixer proved to be a good choice for the design as all of the goals were met. Also, the conversion loss was lower than other single balanced mixer designs found during research that used a diode configuration. Though the design goals were met, there is still room for improvement. Future work will include optimizing the design to filter out the high frequency harmonics a lot better while maintaining an acceptable conversion loss value. Overall, this was a successful MMIC Mixer design. This project provided the opportunity to practice MMIC design and learn what parameters need to be taken into account when converting from schematic to layout so that design rules are followed.

Parameter	Goal	Achieved
RF frequency	21 GHz	21 GHz
LO frequency	22.5 GHz	22.5 GHz
IF frequency	1.5 GHz	1.5 GHz
RF Power	<0 dBm	-10 dBm
LO Power	<12 dBm	10 dBm
Conversion Loss	<10 dB	-8.314 dB

Table 1: Results Comparison

34 GHz Ka-band IQ Vector Modulator



Mark Johnson
MMIC Design
Johns Hopkins University
Fall 2014

1 Abstract

The purpose of this project was to design a vector modulator capable of generating QPSK (quadrature phase-shift keying) signals in the Ka-band. This was accomplished by splitting an incoming RF tone and using reflective attenuators to control the phase of the split signals before recombining and transmitting them. The vector modulator was designed to fit on a 60x60 mil chip using TriQuint's 0.13 um pHEMT process.

2 Introduction

The purpose of a vector modulator is to encode digital data for transmission. This is accomplished by varying the phase and/or amplitude of one or more signals before combining them and transmitting them simultaneously. A quadrature phase modulator (such as the one designed in this project) is capable of sending two bits of information simultaneously by varying the I and Q inputs to control the phase of the output signals.

This vector modulator uses a Lange coupler to split the incoming RF tone into two signals, which are sent to the I and the Q reflective attenuators. The attenuators are each composed of another Lange coupler as well as two transistors. The drain and the source of the transistors are connected between the Lange ports and ground, and their gates are connected to the I and Q input voltages. When the I and Q voltages are set to either +1 or -1, the transistor functions as either a short circuit or an open circuit, altering the phase of the signal by changing the manner in which it is reflected.

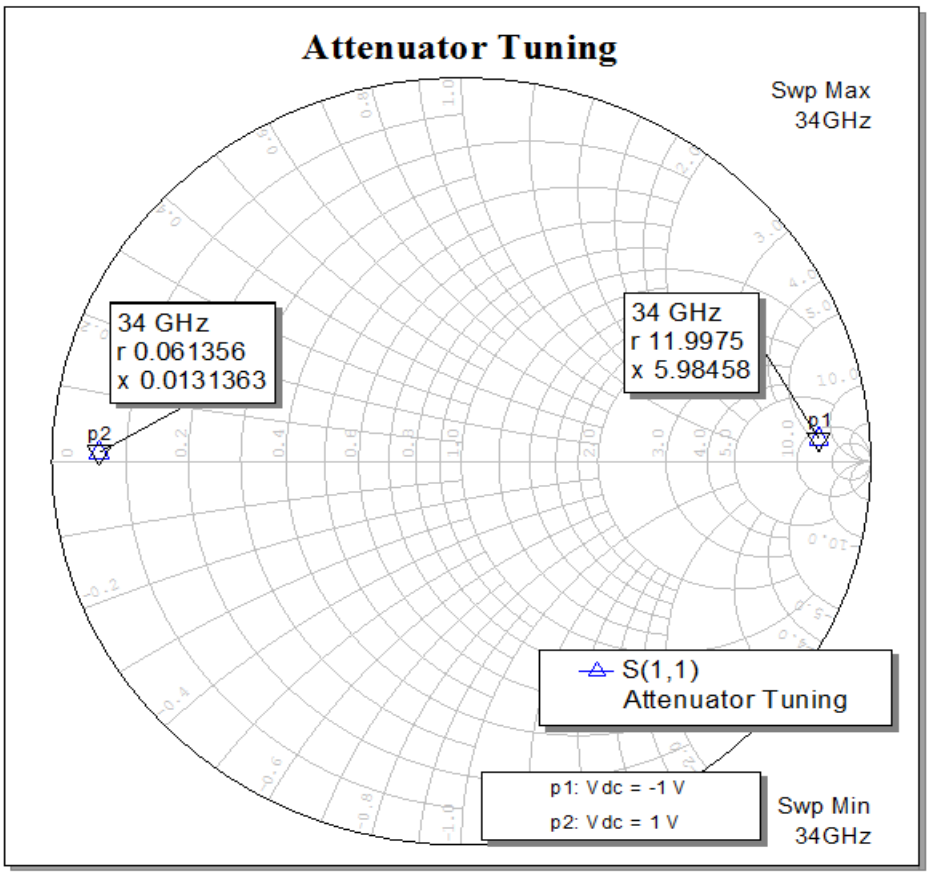
3 Design Approach

3.1 Lange Coupler

Several initial Lange coupler designs were done, but none of them were really satisfactory, and at least one of them wouldn't have passed a design rule check. However, the professor shared a Lange design for 26 GHz, which was then modified to operate at 34 GHz instead. This involved a lot of trial-and-error of adjusting trace lengths and re-running EM simulations until a satisfactory result was achieved. The final design has approximately a 3 dB split between the outgoing ports, and there is very little coupling between those ports.

3.2 Attenuator Tuning

One of the most important parts of the design was tuning the attenuators so they produced a balanced output. This required adjusting the size of the transistors so that they could produce both a good short-circuit as well as a good open-circuit. This was crucial to producing an output constellation that would be centered on a polar graph. However, this was not an easy task. Any transistor capable of operating with low resistance when it is turned on will also have a lot of capacitance, which is very bad for creating a balanced output for the attenuators. Fortunately, the capacitance was able to be resonated out by placing a carefully-tuned inductor in parallel with the transistor. This task involved a lot of tuning, adjustment, and re-simulation in order to create an attenuator that had a balanced output.



3.3 Wilkinson Combiner

The Wilkinson combiner was relatively easy compared to the other design tasks. The only issue was that the transmission lines everywhere else on the chip were very thin, and a Wilkinson combiner is supposed to be composed of transmission lines that are thinner than the input lines, so the traces feeding into the Wilkinson coupler were gradually increased in size until the proper size input line was achieved.

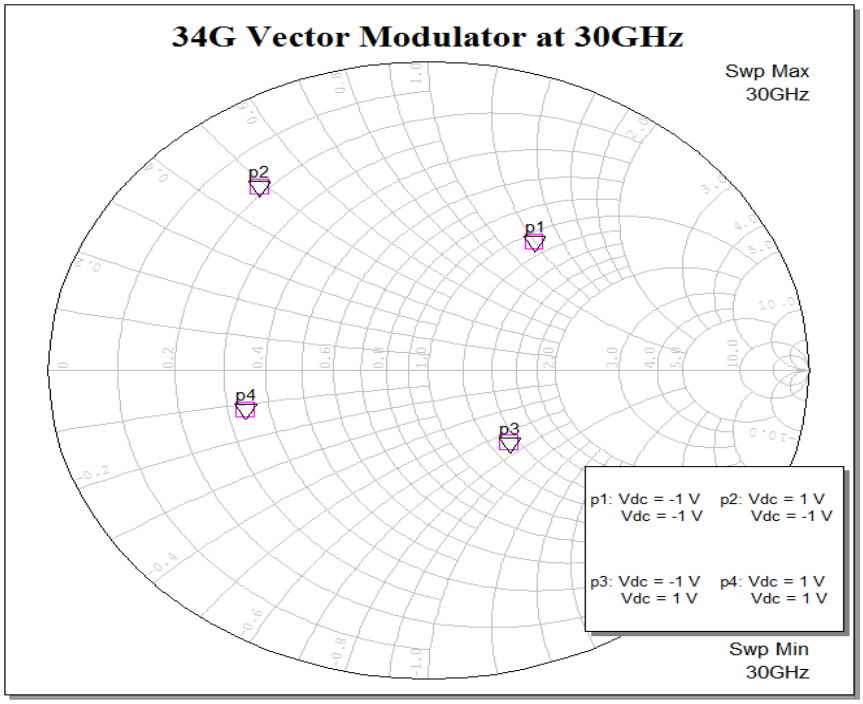
3.4 Output Phase Adjustment

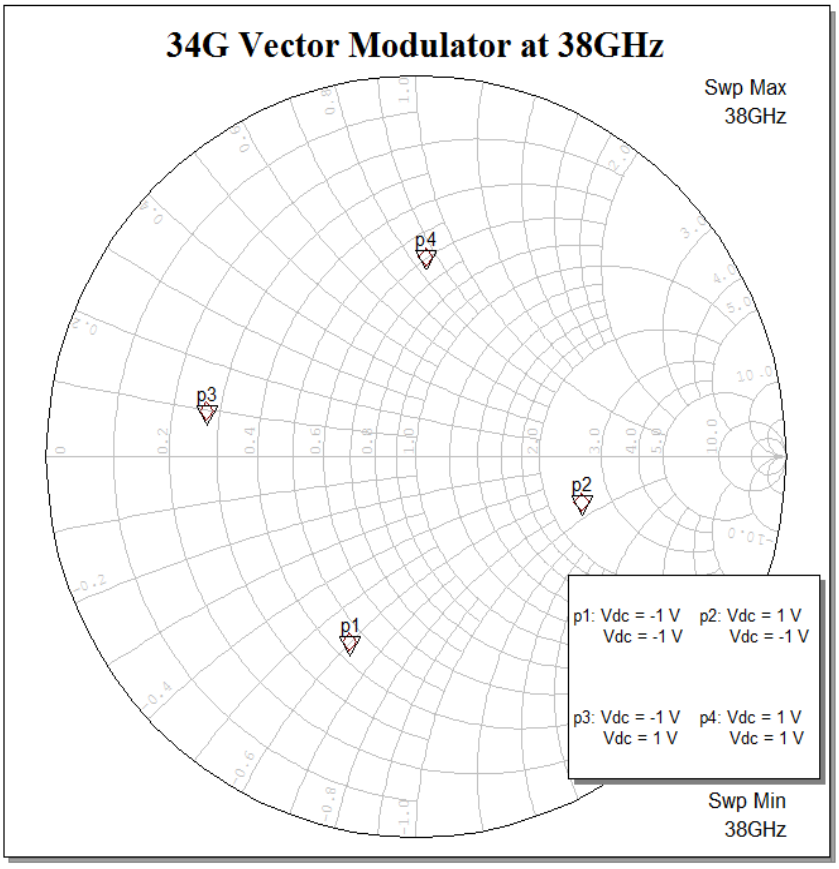
Originally, there had been plans to add identical capacitors in series with the output of each reflective attenuator to rotate the output constellation so that it would appear square on a polar graph. Unfortunately, the Triquint 0.13 um process does not allow capacitors to be made small enough to achieve this. Several capacitors were placed in series in an attempt to achieve a lower total capacitance, but the addition of so many capacitors resulted in an unacceptable degradation of the output signal quality. This idea was abandoned in order to preserve the output signal integrity.

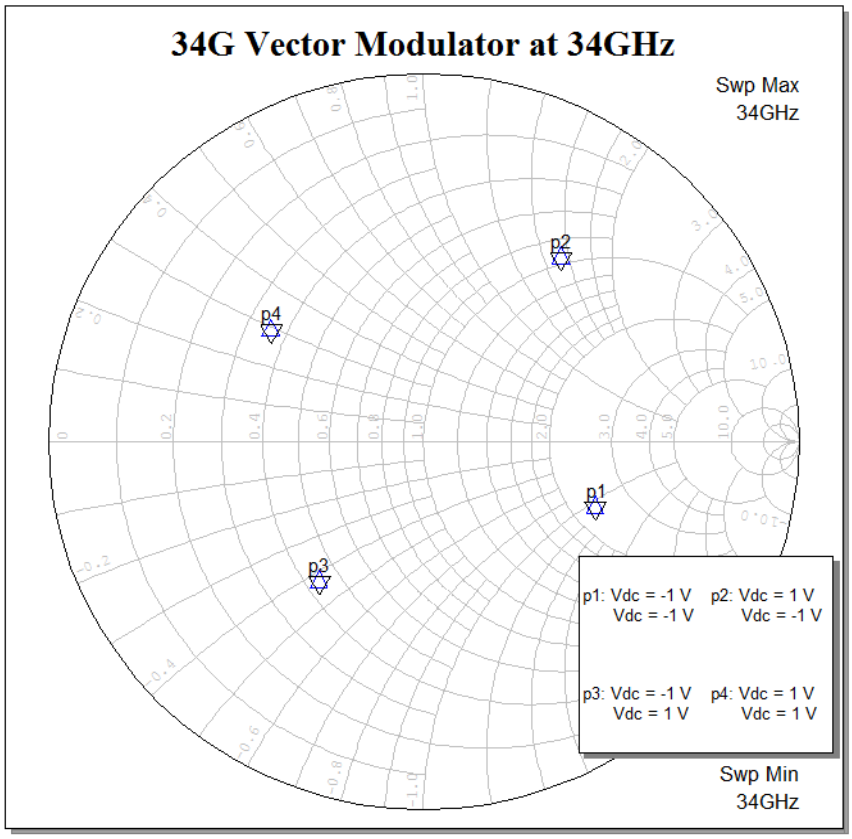
4 Simulations

4.1 Vector Modulator

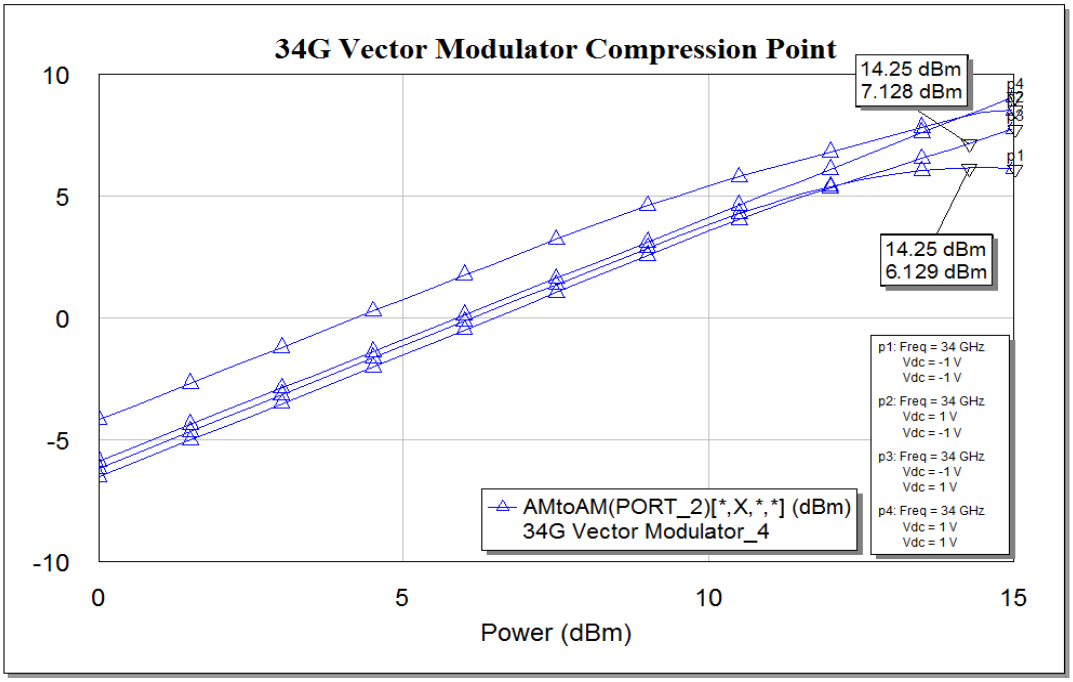
4.1.1 Constellations



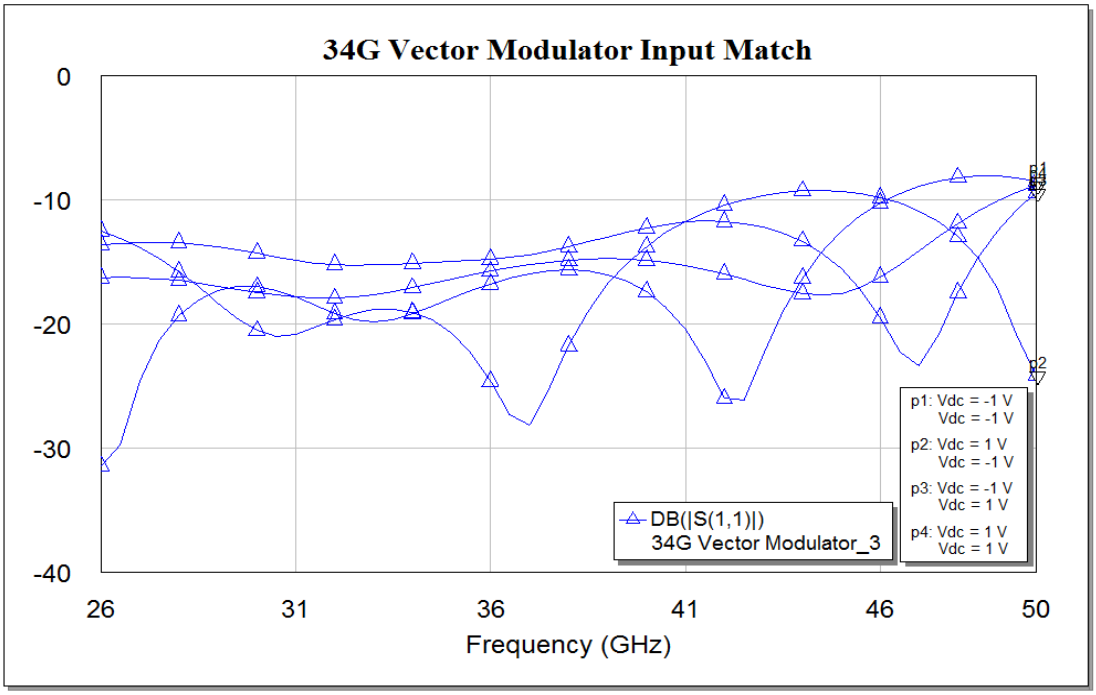




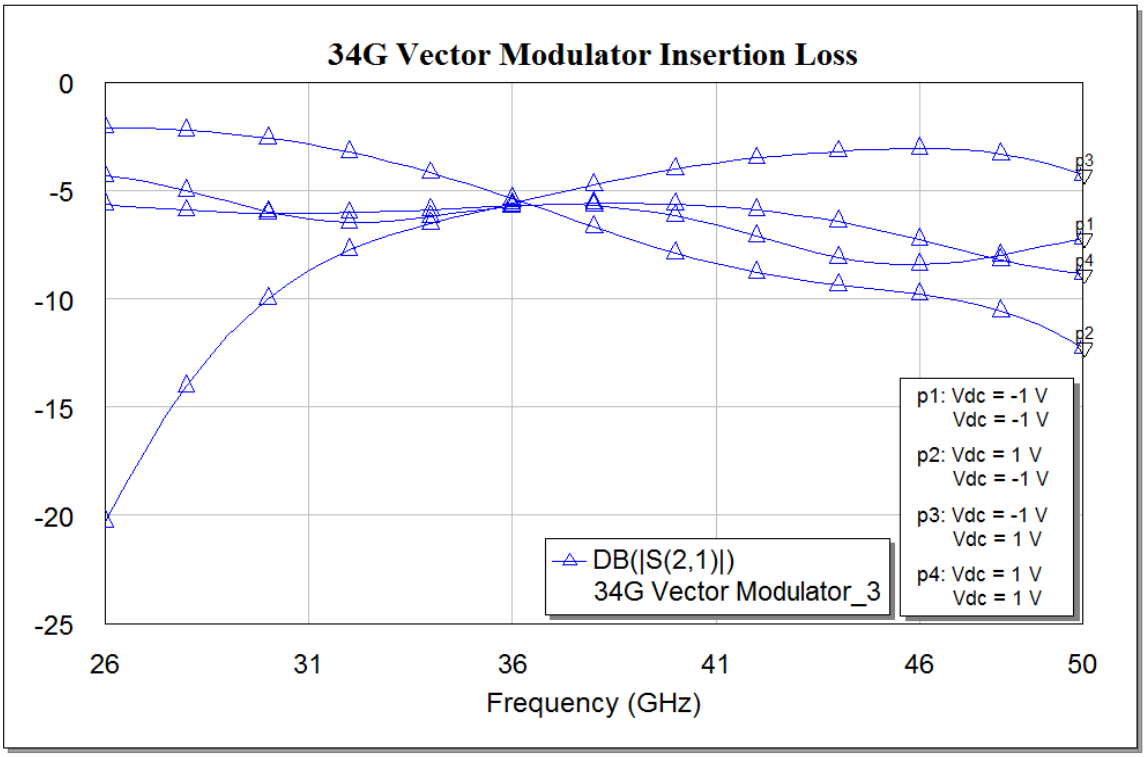
4.1.2 Compression Point



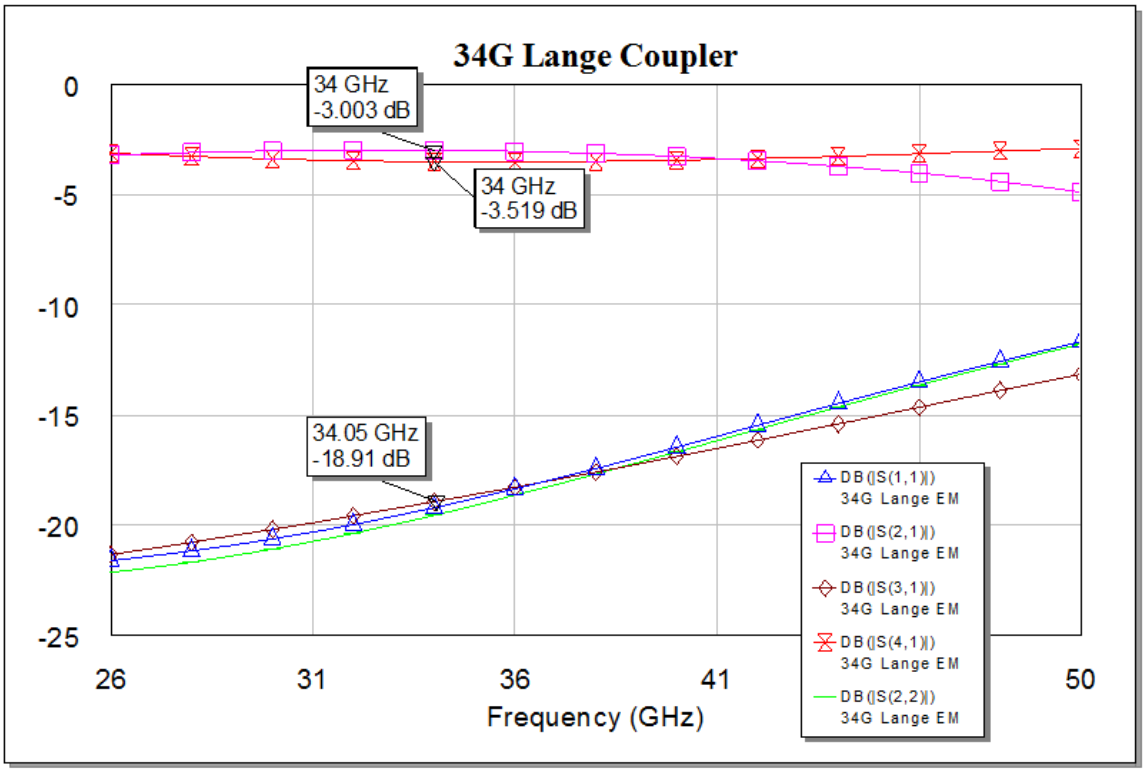
4.1.3 Input Match



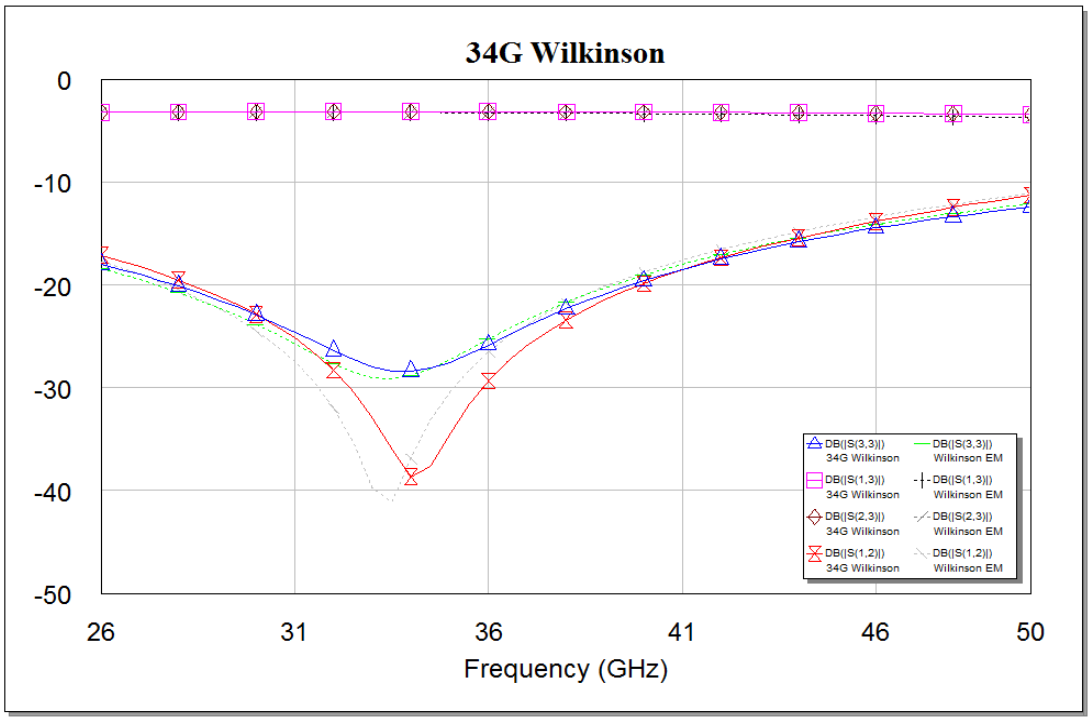
4.1.4 Insertion Loss



4.2 Lange Coupler

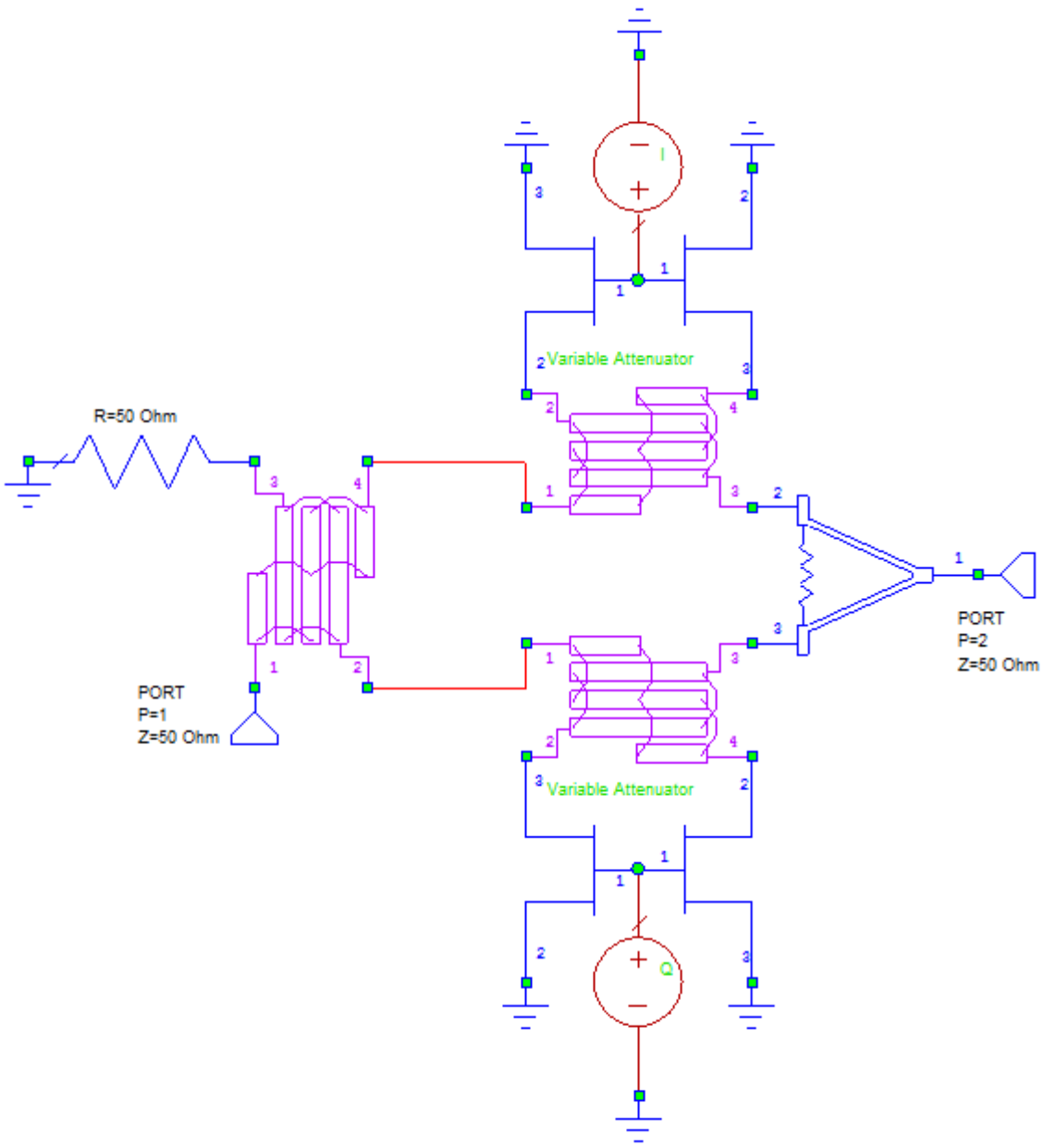


4.3 Wilkinson Combiner

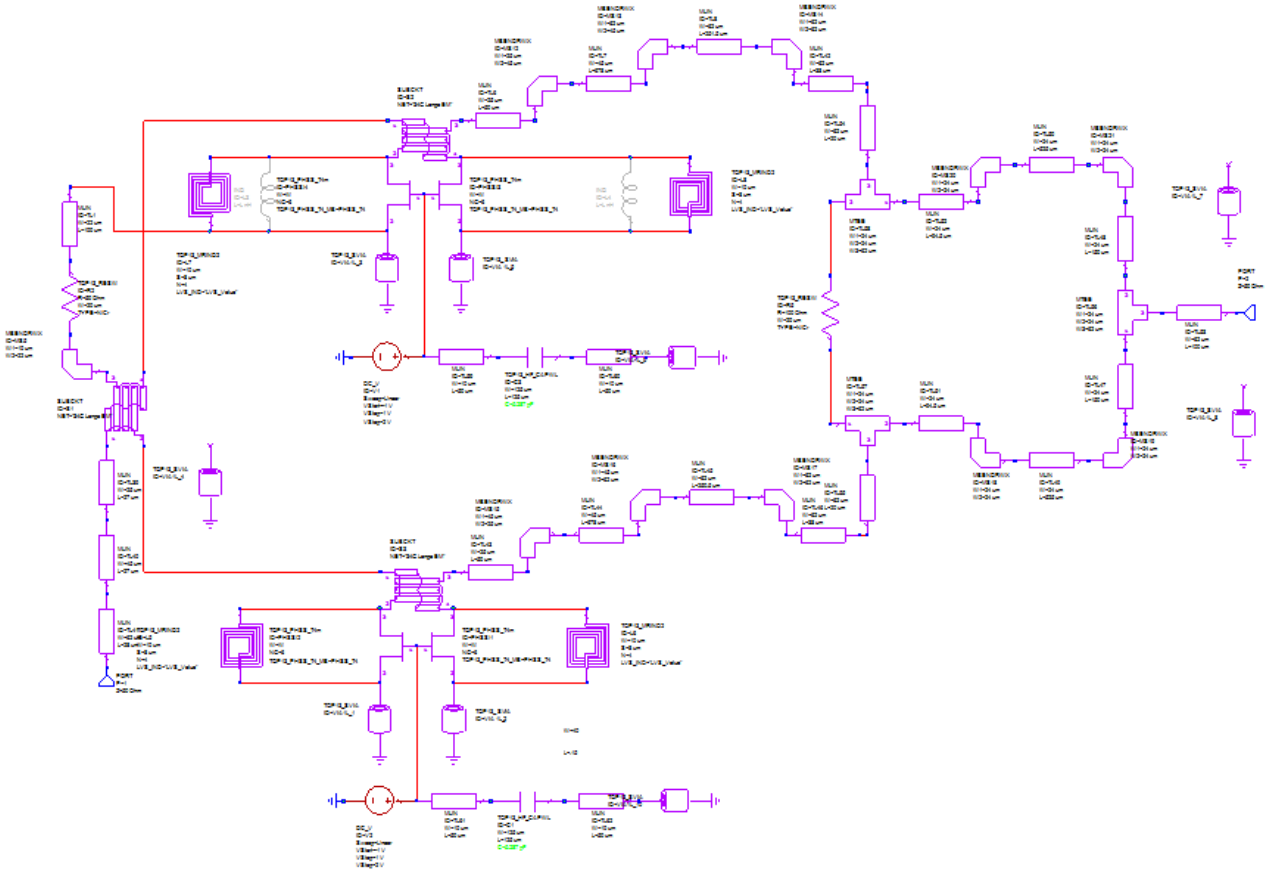


5 Schematic

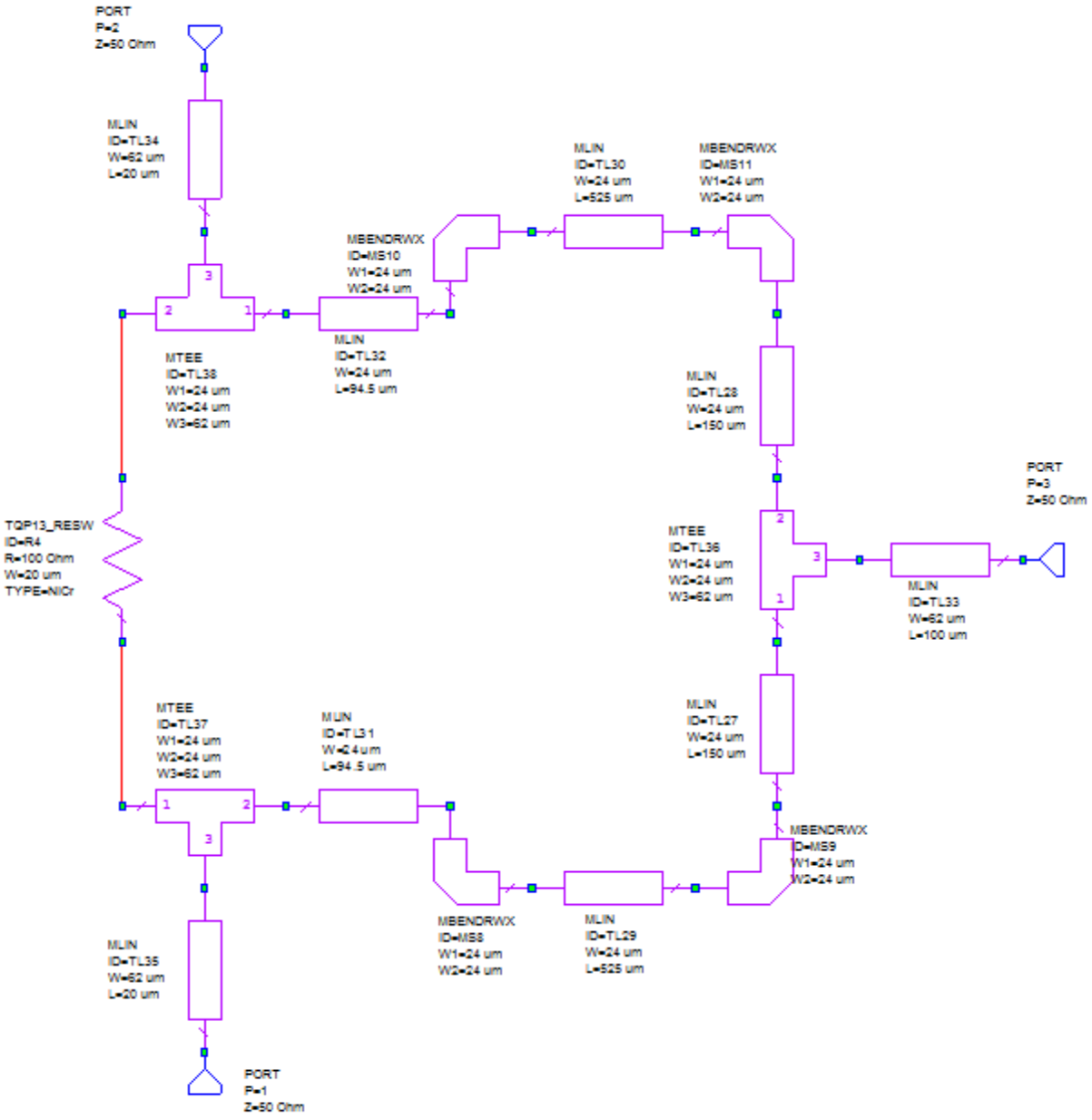
5.1 Vector Modulator Block Diagram



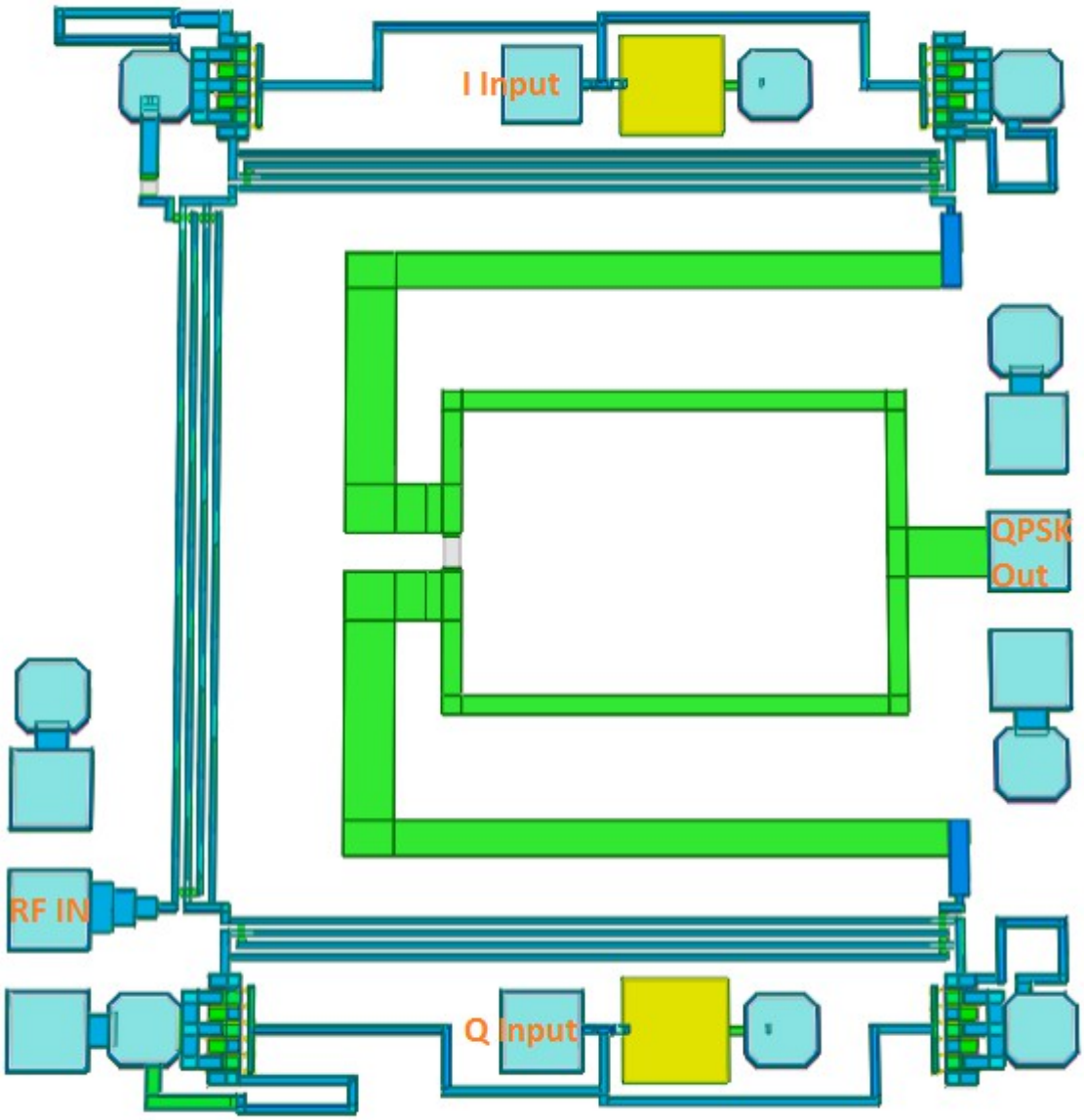
5.2 Vector Modulator Schematic



5.3 Wilkinson Coupler



6 Layout



7 Test Plan

7.1 Test Equipment

- Network analyzer
- DC power supply
- Spectrum Analyzer

7.2 Test Procedure

The s-parameters of the device will be measured four times (+1V and -1V for both the I and Q inputs) at several different frequencies within the Ka-band. These s-parameters will then be plotted on polar plots to confirm the device's ability to generate a good constellation at each frequency. The return loss, insertion loss, and 1 dB compression point will also be measured.

8 Summary & Conclusions

The vector modulator simulates quite well and performs as expected. However, one of the professors noticed that there aren't any current-limiting resistors between the DC inputs and the transistor gates. Upon adding those resistors, the output IQ constellation shifted dramatically upwards. In order to fix this, the transistors will need to be re-tuned to re-balance the reflective attenuators. However, if changes are made to the transistors, the inductors will need to be adjusted as well in order to maintain the square shape of the constellation. In general, the vector modulator is close to being complete, but it needs a couple more tweaks before it will be ready for fabrication.

A lot more experience with mesh analysis was gained while completing this project. Many problems were encountered with the software generating mesh sizes and shapes that were either inappropriate or unable to be simulated due to the way the EM simulation algorithm operates. After much research (and trial-and error), the problems were overcome by adjusting some settings that control how the software creates its meshes. Although these problems created a somewhat frustrating experience, the knowledge gained will be useful in the future.