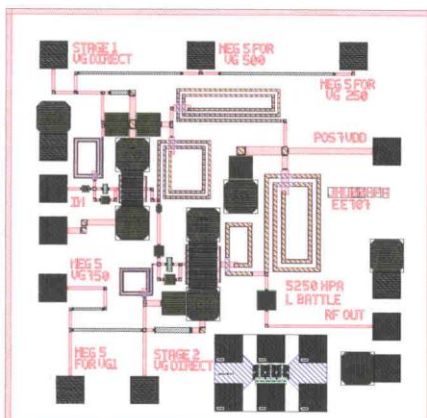


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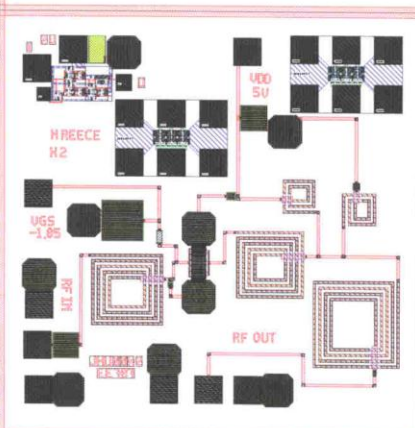
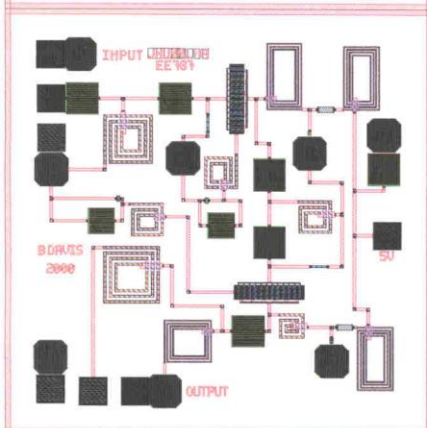
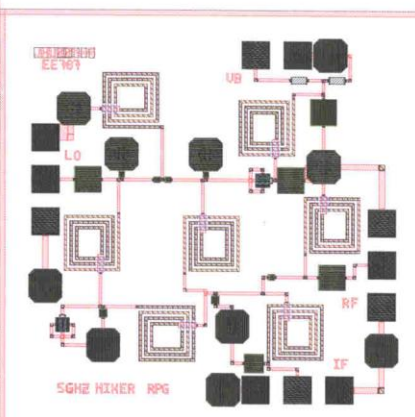
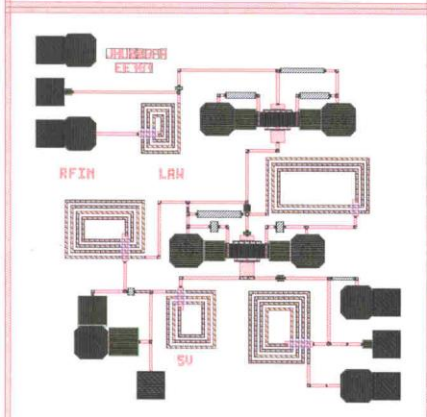
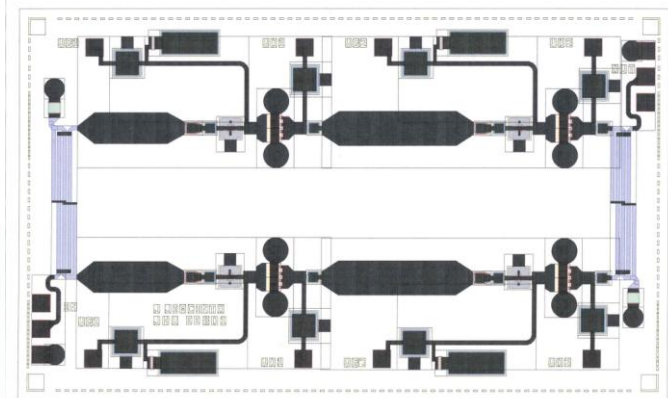
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SUPPORT FROM TRIQUINT AND AGILENT



# 5.25 GHz Low Noise Amplifier Using Triquint MMIC Process

Ben Davis  
December 11, 2000  
MMIC Design  
Fall 2000

Instructors: John Penn, Craig Moore

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## Summary

This report documents the design of a low-noise amplifier designed at 5.25 GHz using the Triquint TQS TRx process. The design was produced as a part of the MMIC Design course taught at Johns Hopkins University during the Fall 2000 semester.

The LNA was designed for use in a C-band HYPERLAN transceiver. Other designs produced in the course were to be used alongside this design as parts of this transceiver.

The design software used to design the LNA was Agilent Advanced Design System 1.3 (ADS). The elements used were custom model elements based on the Triquint process. The design was laid out on a 60 x 60 mil chip by Anachip. The final MMIC design will be fabricated and tested over the course of the first six months of 2001.

# Introduction

## ***Circuit Description***

The circuit topology chosen for the design was a simple cascaded two-stage amplifier layout with self-biasing networks implemented. Matching networks were employed using lumped element topology.

## ***Design Philosophy***

In designing low-noise amplifiers, the primary goal is to maintain the lowest possible noise figure while attaining useable gain. For this design, the Triquint DFET was chosen as the transistor due to its low-noise and gain characteristics. In order to achieve the goal of 15 dB gain, a 600  $\mu\text{m}$  DFET was chosen over the 300  $\mu\text{m}$  device.

The first step in designing the LNA was to analyze the performance of the device. The DFET transistor models were nonlinear, however, they did not include noise performance. So the measured noise parameters had to be implemented in a linear model and that linear model, which provided the noise data, was used alongside the nonlinear model throughout the design process. Considering that the noise data was only taken at certain bias points, the Q-point was chosen based on the available data. The bias point chosen was

$$V_d = 2V \quad V_g = -0.225V \quad I_{ds} = 20.85mA$$

After choosing the bias point, the S parameters, noise figure, minimum noise figure, stability, and stability circles were simulated for both the linear and nonlinear models. From this point, stabilizing inductors were added to achieve desired broadband stability.

The next point was to produce an input matching network for the first stage. This was done by matching to  $\Gamma_{\text{opt}}$ . Again, the nonlinear and linear models were both simulated with the matching network to verify that they were in agreement.

The second stage was identical to the first stage so the interstage matching network was derived by using the output of the first stage and the input of the first stage without the input matching network. Once again, the linear and nonlinear models were simulated in tandem.

Finally, the output matching network was derived with both stages and interstage networks in place. Initially, ideal lumped elements were used in the matching networks for quicker simulation and tweaking. Once the performance was optimized, the ideal elements were replaced with Triquint elements and re-tuned for optimum performance.

After the simplified schematic was optimized to desired performance, the layout process was initiated. For ease of layout design, all of the elements from the schematic were placed on the layout grid singly without any connection. This method made it easier to figure out spacing and routing options. Once the elements were placed on the chip in the desired locations, they were interconnected with microstrip. After the layout completion, the schematic was updated to include all of the interconnections.

As a final tweaking step, the new schematic that included the microstrip interconnects was further optimized by way of the matching networks. This was done to reclaim any performance lost during the layout generation. Any changes made after the optimization were then translated back to the layout to produce the final design.

## Trade-offs

Though the DFET provided decent noise figure for the design, the stability was not within the desired range for a broadband of frequencies. Therefore, stabilization inductors had to be used on the source to provide better stability. As a consequence, the maximum gain of the device suffered.

## Modeled Performance

### Specification Compliance Matrix

The following table summarizes the design specifications and the corresponding simulated performance. Both the simplified schematic's and the layout schematic's performance are included in the table.

**Table 1 - Specification Matrix**

	<b>Specification Goal</b>	<b>Simplified Schematic</b>	<b>Layout Schematic</b>
Frequency Bandwidth	5150 – 5350 MHz	5150 – 5350 MHz	5150 – 5350 MHz
Gain	> 15 dB	12 dB	10.9 dB
Gain Ripple	± 0.5 dB max	± 0.05 dB	± 0.25 dB
Noise Figure	> 5 dB, 3 dB opt	2.1 dB	2.1 dB
Input IP3	> 5 dBm	-	-
VSWR, 50 ohm	< 1.5:1 input < 1.5:1 output	1.3:1 input 2.0:1 output	1.5:1 input 1.3:1 output
Supply Voltage	± 5 V, +5 only opt	+5 V	+5 V

### Predicted Performance

The following plots show the performance of the design at the simplified and layout stages. Figures 1a through 1d illustrate the performance of the simplified schematic. Figures 2a through 2d illustrate the performance of the final layout schematic.

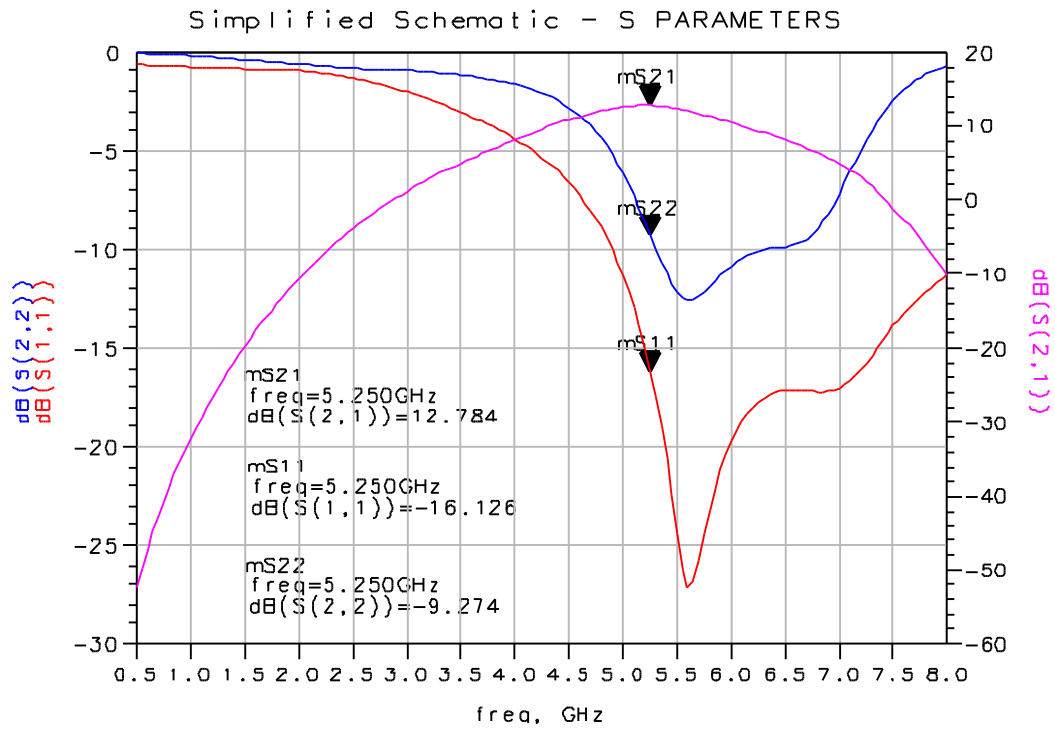


Figure 1 - simplified schematic S parameters

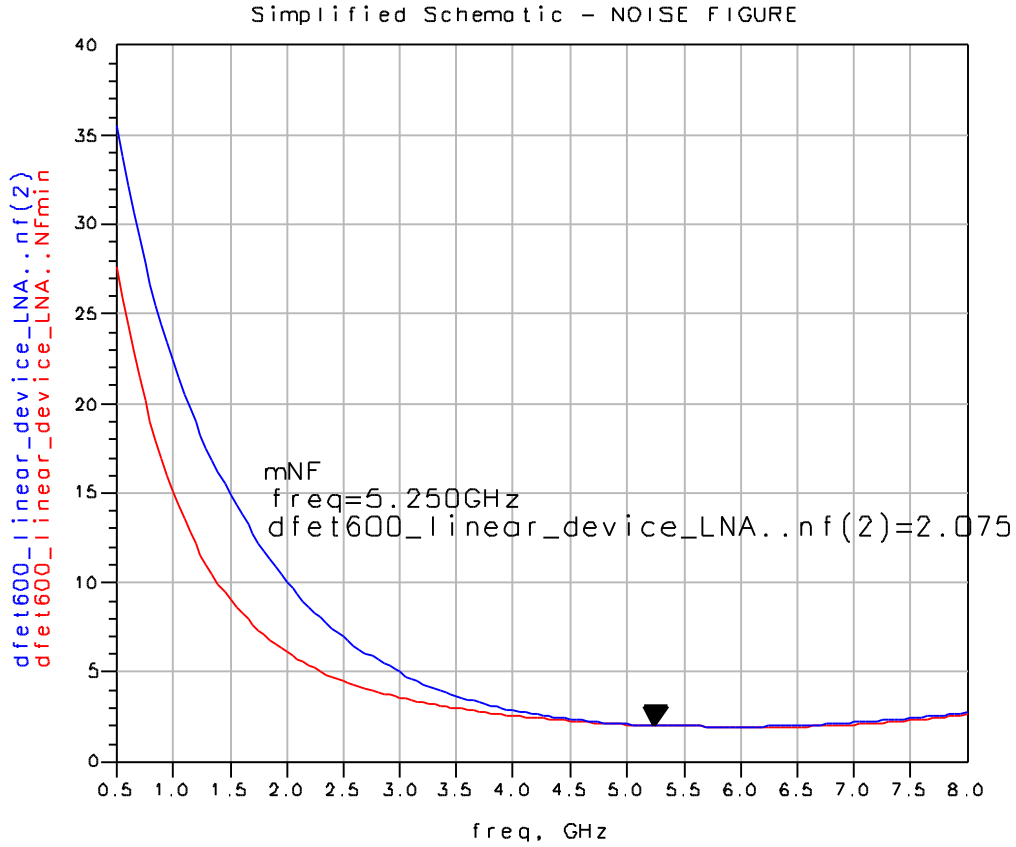


Figure 2 - simplified schematic noise figure

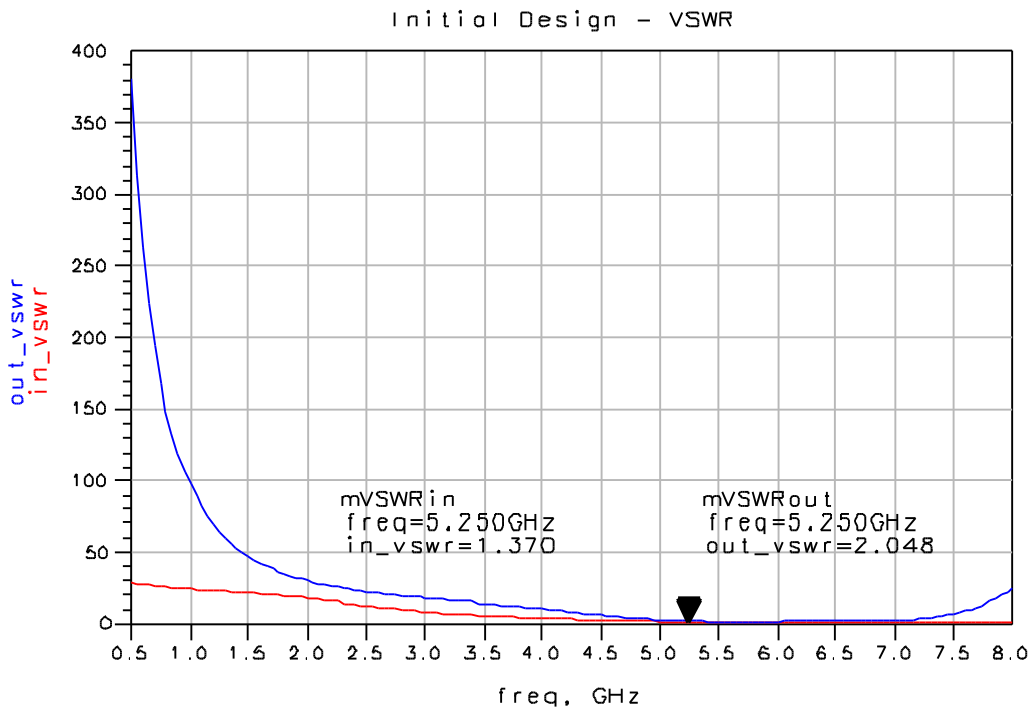


Figure 3 - simplified schematic VSWR



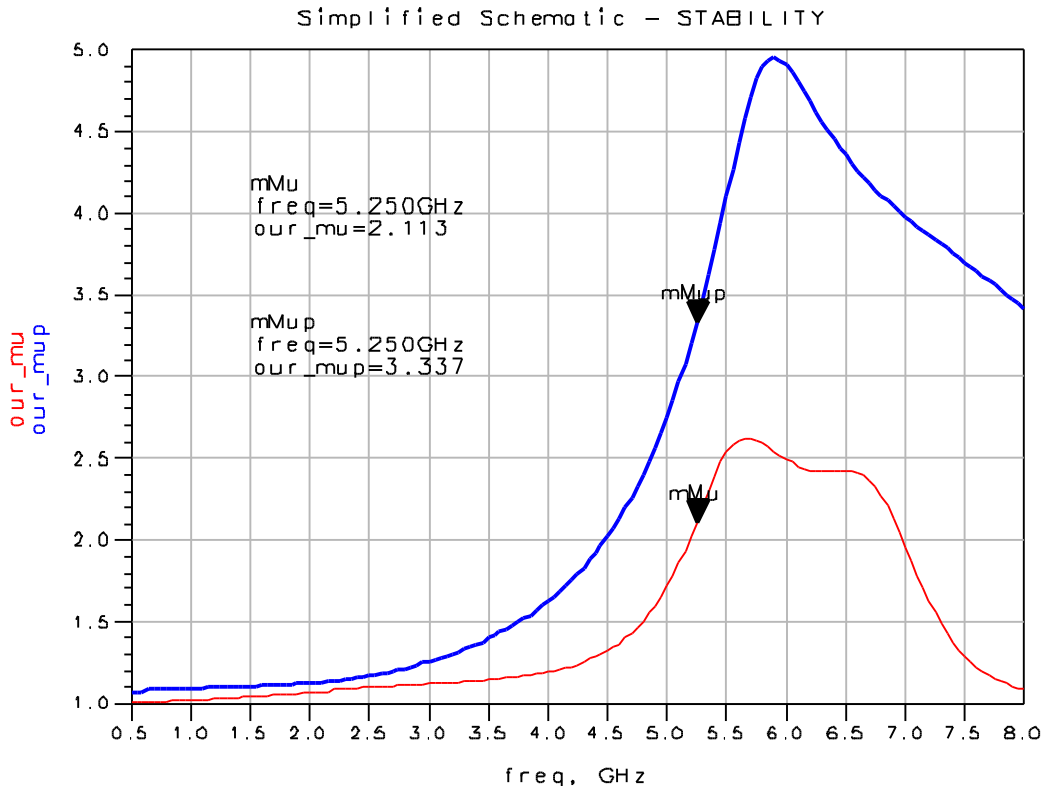


Figure 4 - simplified schematic stability

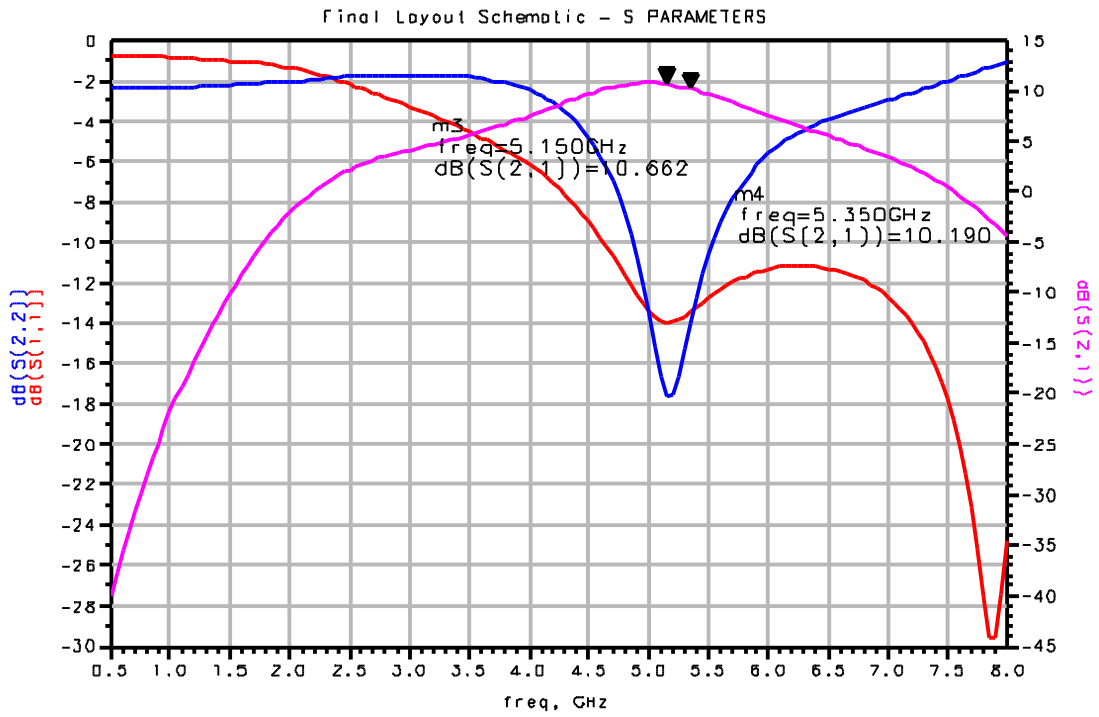


Figure 5 - final layout schematic S parameters

Final Layout Schematic - NOISE FIGURE

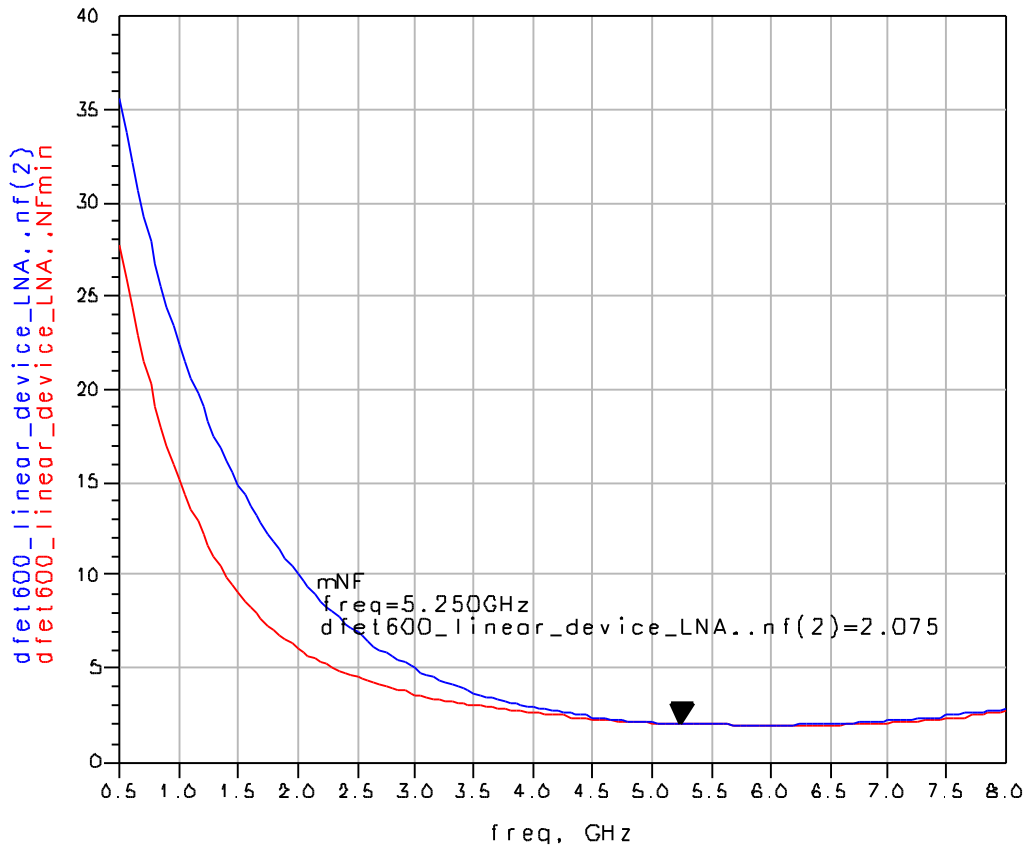


Figure 6 - final layout schematic noise figure

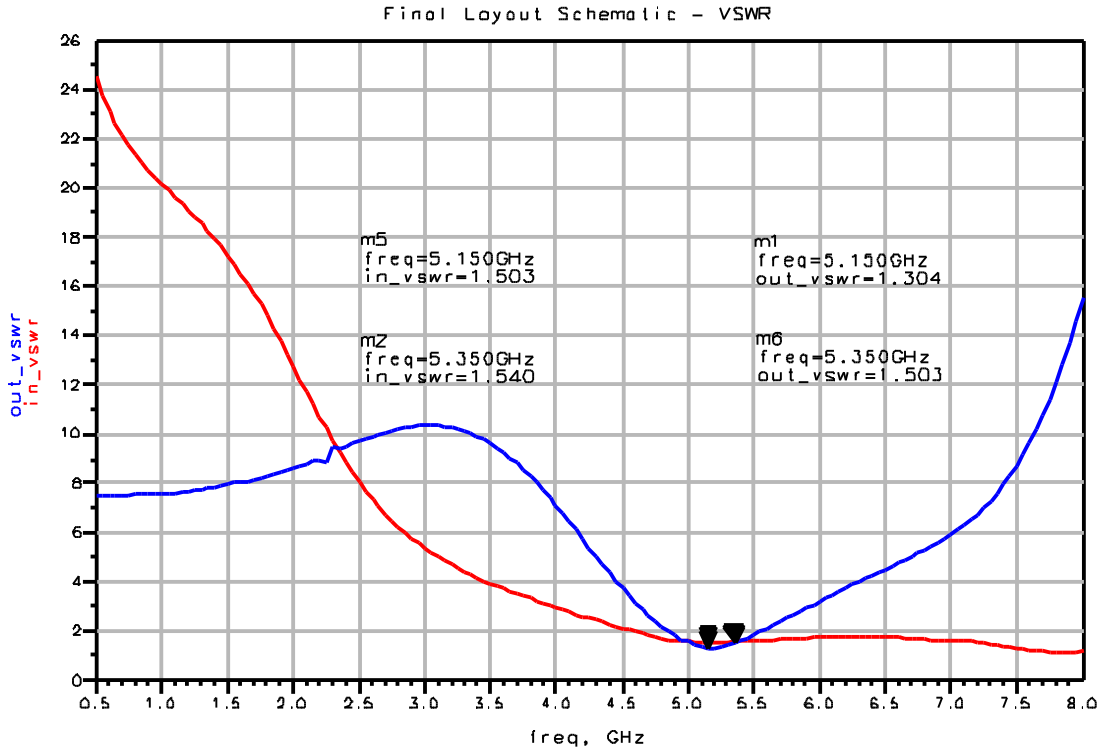


Figure 7 - final layout schematic VSWR

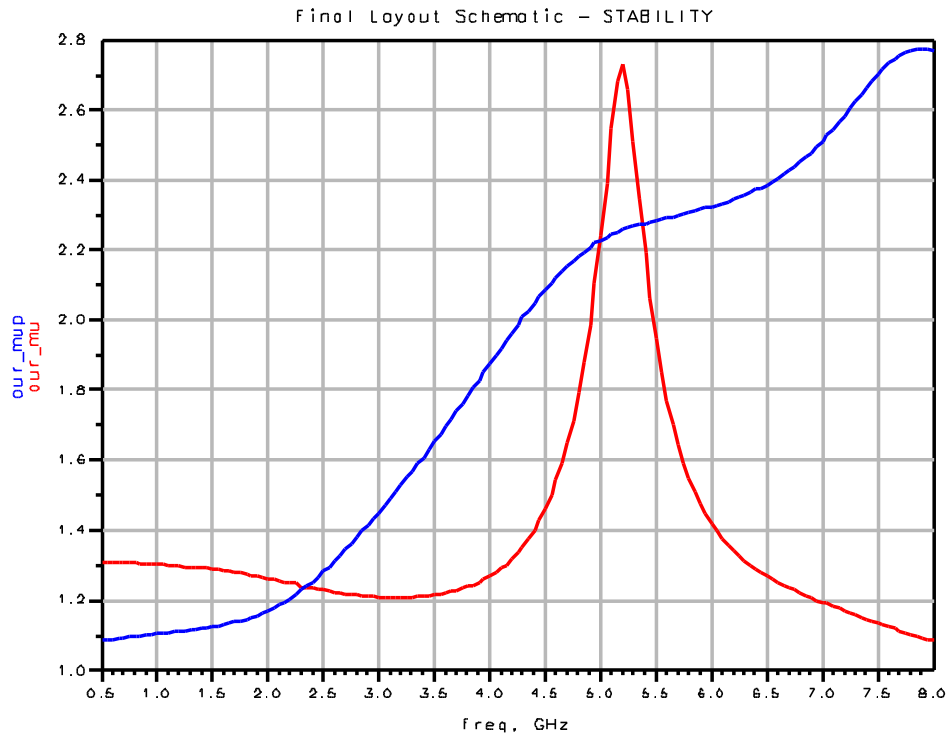


Figure 8 - final layout schematic stability

## **Schematic Diagrams**

The following pages illustrate the final schematics used for both the simplified and layout designs.

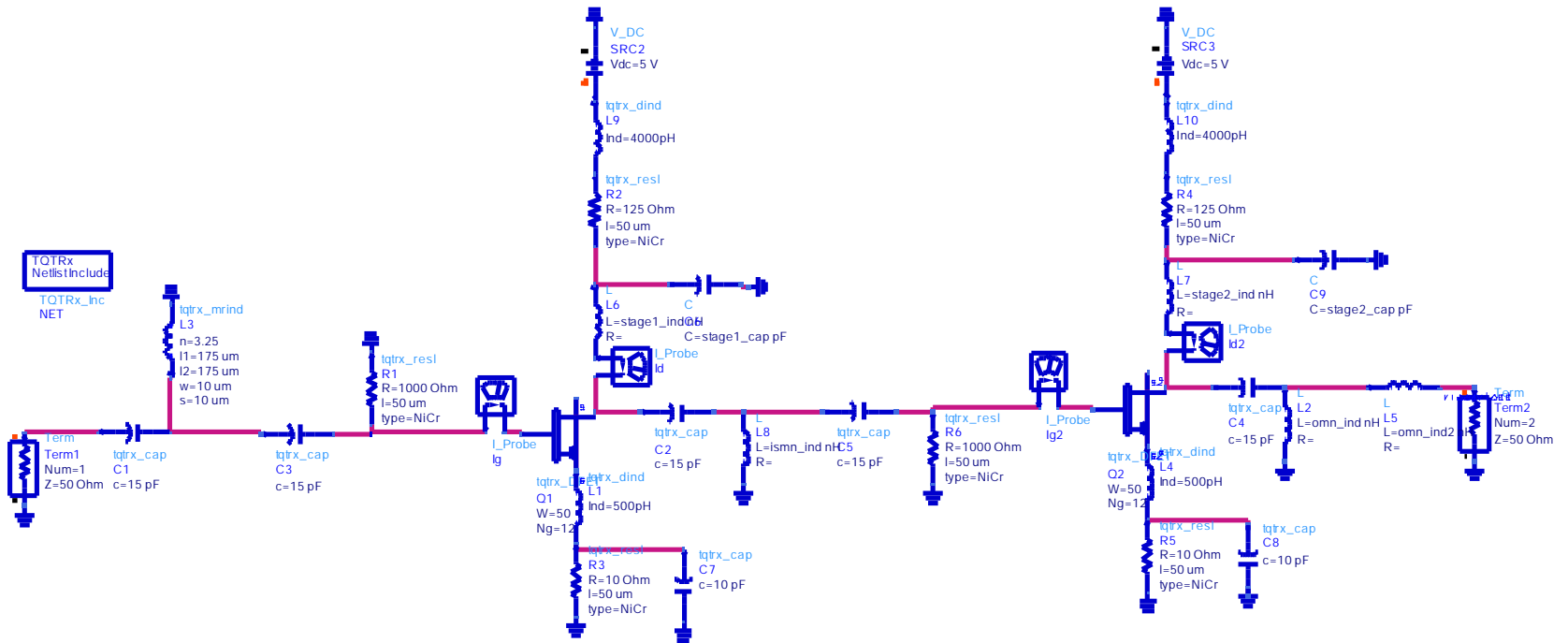


Figure 9 - simplified schematic design

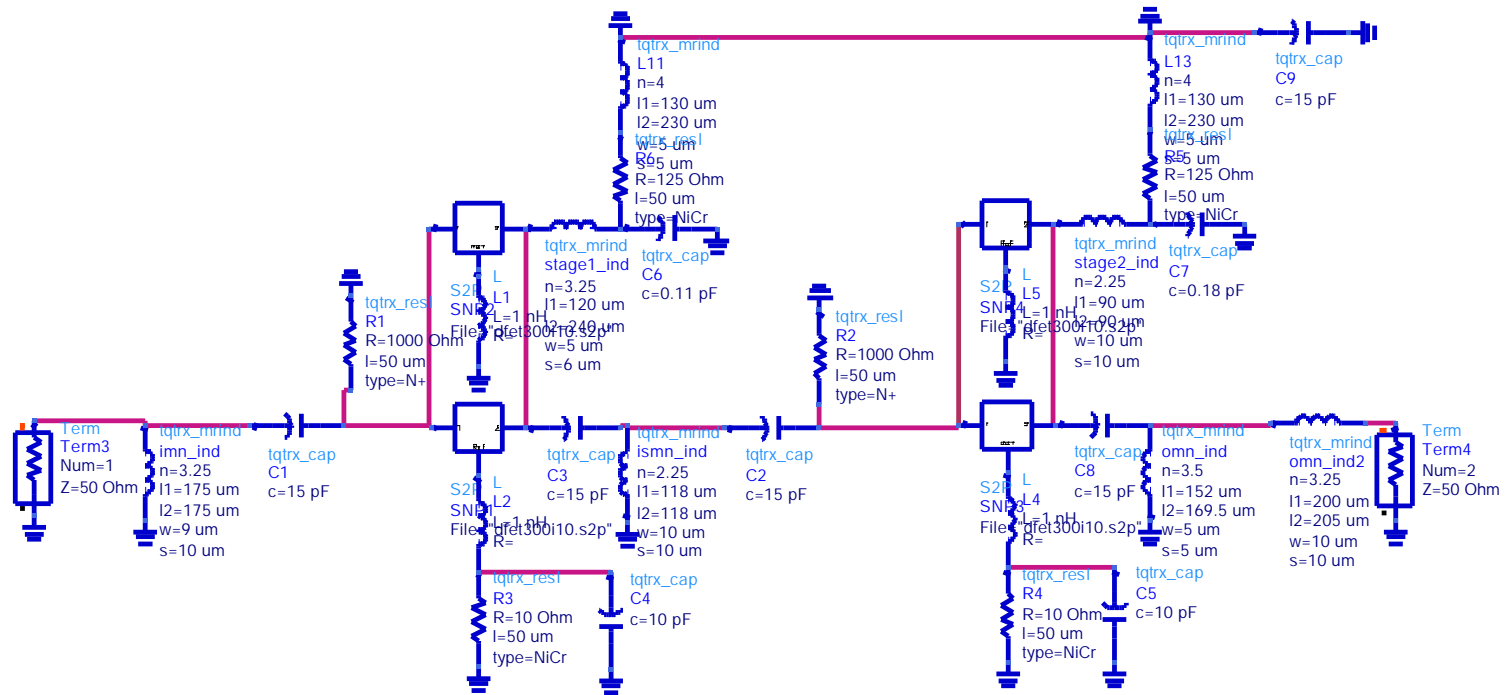


Figure 10 - linear model schematic

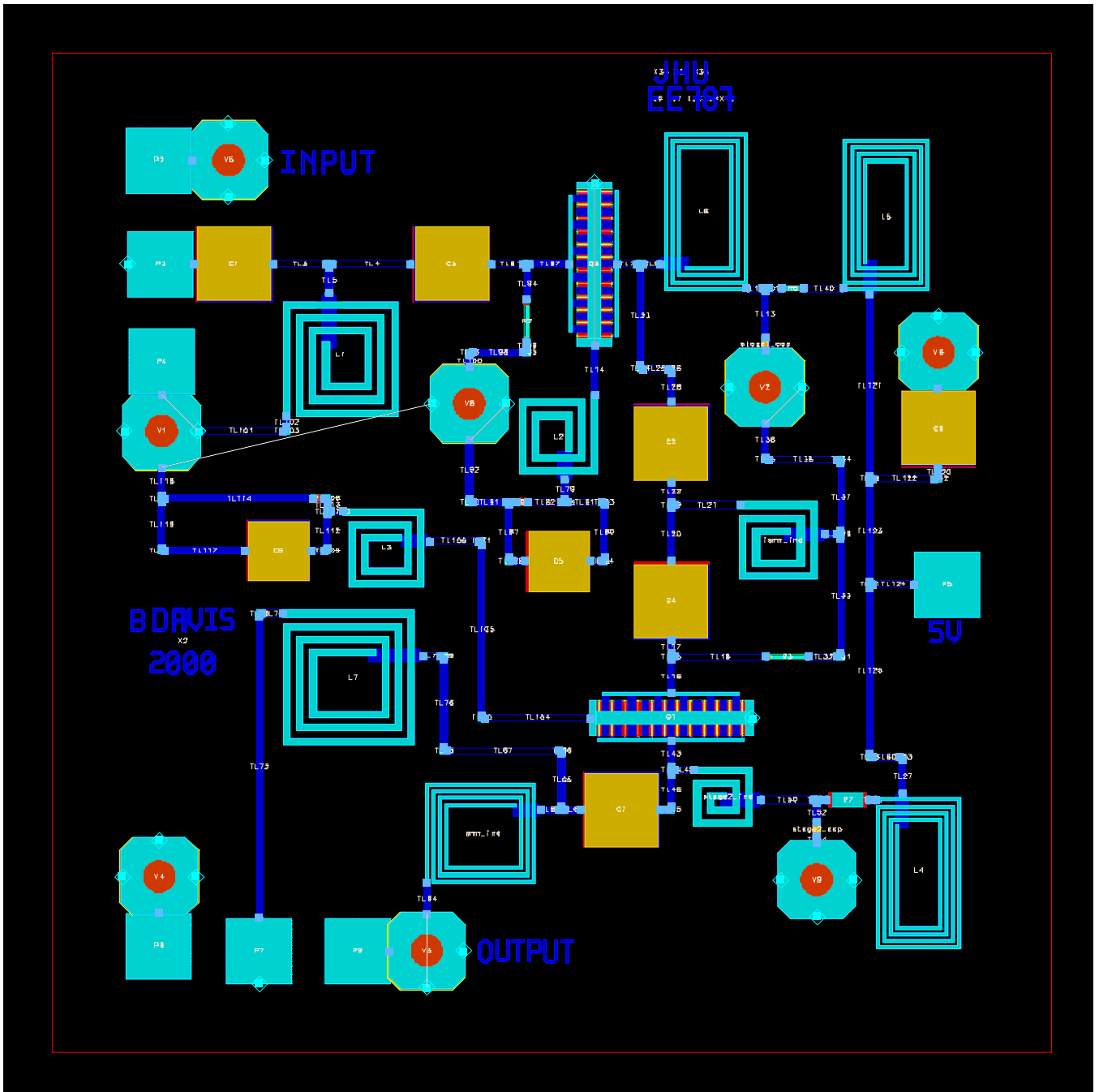


Figure 11 - final layout design





## Test Plan

To test the chip after fabrication, the following test plans are suggested.

### ***Linear Parameters***

To measure the S parameters, a vector network analyzer is needed along with extraction software, preferably Agilent ICCAP. This test plan assumes you have both.

- Calibrate the network analyzer from 0.45 to 10 GHz.
- Using ICCAP, create an extraction module to sweep frequency from 0.5 to 8 GHz in steps of 50 MHz while supplying a bias voltage of 5 volts to the DUT.
- Place the bias probe on the chip's pad that is next to the "5V" indicator.
- Place the probe tips on the appropriate pads. The input port is located on the upper left of the chip and is marked by "INPUT". The output port is located on the bottom left of the chip and is marked by "OUTPUT".
- Begin the ICCAP extraction routine that you have created to measure S parameters and store the data.

### ***Noise Figure***

To measure the noise figure, a noise figure meter is needed along with extraction software, preferably Agilent ICCAP. This test plan assumes you have both.

- Calibrate the noise figure meter from 0.45 to 10 GHz.
- Using ICCAP, create an extraction module to sweep frequency from 0.5 to 8 GHz in steps of 50 MHz while supplying a bias voltage of 5 volts to the DUT.
- Place the bias probe on the chip's pad that is next to the "5V" indicator.
- Place the probe tips on the appropriate pads. The input port is located on the upper left of the chip and is marked by "INPUT". The output port is located on the bottom left of the chip and is marked by "OUTPUT".
- Begin the ICCAP extraction routine that you have created to measure noise figure parameters and store the data.

## **Conclusion and Recommendations**

The design was successful and passed all design goals except for gain. In retrospect, the second stage of the amplifier would be redesigned for maximum gain instead of lowest noise figure. The first stage provided a low enough minimum noise figure such that a compromise on the second stage noise figure would have been acceptable and still meet specifications.

The third-order intercept power could not be simulated due to the failure of the harmonic balance simulations. Further investigation into the reason why the design would not simulate is needed.

## **Appendix – ADS Project File**

On the attached floppy diskette is an ADS archive project containing all of the design schematics, plots and layouts used for the design. The file “readme.dsn” describes the various schematics.

## **Appendix – GDSII (CALMA) Layout File**

On the attached floppy diskette is a GDSII layout file for generating the MMIC chip.

# C-Band General Purpose Amplifier



*Lawrence A. Walker Jr.*

*Doctoral Candidate, Morgan State University  
School of Engineering*



December 11, 2000



Johns Hopkins University  
Professors: Craig Moore and John Penn

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*Abstract* - A single-supply 12dB MMIC C-band general-purpose amplifier for the HYPERLAN wireless local area network frequencies has been designed based on well-known small-signal s-parameter techniques and the Cripps method. The amplifier is packaged on a 60x60 mil ANACHIP realized using Triquint's foundry process. The design is capable of producing in excess of +13dBm of power with good input and output VSWR (50 $\Omega$ ). Also, the design features DC blocking capacitors at the input and output. The schematic and layout were simulated using Agilent's Advanced Design System (ADS). Simulated results show that all design specifications were met.

---

# C-Band General Purpose Amplifier

## 1. Introduction

### 1.1. *Circuit Description*

The design is a two stage C-band general-purpose amplifier with on-chip bias network utilizing two 300um GFETs. The amplifier is intended to operate from 5150 to 5350 MHz on a single +5V supply. A simultaneously conjugate matched first stage is followed by a second power amplifier stage to provide 12 dB of gain across the band. The output power is typically 16 dBm at 1dB gain compression. The second stage is biased directly from the +5V supply. A resistive divider provides approximately 4V to the first stage. The resistive divider along with a 12 pF capacitor assists in isolating the two stages thereby suppressing instability. On-chip DC blocks allows *cascaability* with good input and output VSWR. The overall chip size is 60x60 mil.

### 1.2. *Design Philosophy*

The design is implemented using small-signal s-parameter techniques and the Cripp's method. The primary design strategy was to work with each stage separately. The secondary design strategy is to begin matching the 2<sup>nd</sup> stage output matching network (OMN) towards the 1<sup>st</sup> stage input matching network (IMN). Note that the stability of the individual and combined first and second stages was checked.

#### 1.2.1. Selection of transistors and operating point

Two 300um GFETs were selected. The 2<sup>nd</sup> stage GFET is suitable for meeting the output power requirements. However, the 1<sup>st</sup> stage GFET is sized for ease of matching between the 1<sup>st</sup> and 2<sup>nd</sup> stages. A simple interstage matching network (CMN) is desired because it uses less chip space. The 1<sup>st</sup> stage is biased to provide ample linear gain prior to the 2<sup>nd</sup> stage. The 2<sup>nd</sup> stage was biased at approximately  $\frac{1}{2} I_{DSS} = 50$  mA.

#### 1.2.2. Transistor stabilization

The utilization of series and shunt resistors at the gates suppresses instabilities at the high and low end, respectively.

### **1.2.3. Design of second stage output matching network**

The Cripps method was used to realize the 2<sup>nd</sup> stage OMN. The desired load line that the amplifier would like to see for maximum symmetrical swing is  $80\Omega$ . This then leads to a preliminary OMN that matches  $80\Omega$  to  $50\Omega$ . Also, a  $300\Omega$  shunt was added to provide improved output VSWR.

### **1.2.4. Design of second stage input matching network**

The input of the 2<sup>nd</sup> stage was simply conjugately matched to  $50\Omega$  with the OMN in place.

### **1.2.5. Design of first stage input and output matching network**

The 1<sup>st</sup> stage was simply simultaneously conjugate matched.

### **1.2.6. Design of interstage matching network**

It is straightforward to realize the interstage matching network (CMN) based on the 1<sup>st</sup> stage output and 2<sup>nd</sup> stage input impedances found previously.

### **1.2.7. Overall amplifier optimization**

The first and second stages were combined using the interstage matching network. The overall amplifier was then optimized. Further optimization was required after replacing the ideal elements with Triquint elements. The stability was checked.

### **1.2.8. Conversion to self-bias**

The drain and source bias resistors were selected to provide the desired bias (Figure 5).

### **1.2.9. Realization of the on-chip layout**

All elements contained in the self-bias schematic were placed strategically within the required area of the  $60\times 60$  mil ANACHIP. Next, interconnects were routed and the elements positioned as appropriate. Then, schematics of the first, interstage, and second stage matching networks were recreated from the layout. Subsequent optimization of each stage was used to recover the performance seen in the prelayout schematic (Figure 4).

Also, the RC shunt networks were affixed on both sides of the FET artwork to preserve electrical symmetry (Figure 1).

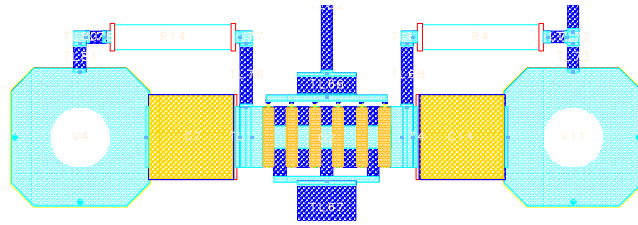


Figure 1: Layout - FET Symmetry

### 1.3. Trade-offs

In realizing a design that meet ALL specifications, the following were the trade-offs that were made.

- ◆ Gain & Power for output VSWR – the OMN network was readjusted slightly to improve VSWR.
- ◆ First stage transistor size for ease of developing interstage match - a smaller transistor makes matching difficult.
- ◆ Gain for stability – the stabilizing resistors taxed the gain
- ◆ Power for self-bias – the self-bias network pinched the output signal swing at high voltages and the operating point shifted from 5 to 4.3V.

## 2. Modeled Performance

### 2.1. Specification Compliance Matrix

Table 1: Specification Compliance Matrix

Requirements	Specification	Goal	Simulated	
			Pre-layout	Post-layout
Frequency	5150 to 5350 MHz	-	ACHIEVED	ACHIEVED
Bandwidth	> 200MHz	-	ACHIEVED	ACHIEVED
Gain (small-signal)	> 12dB	15dB	15	14
Gain ripple	$\pm 0.5$ dB	-	ACHIEVED	ACHIEVED
Output Power @ 1dB compression	> +13dBm	-	18	16
VSWR, 50 $\Omega$				
Input	< 1.5:1	-	1.46	1.46
Output	< 1.5:1	-	1.22	1.22
Supply Voltage	$\pm 5$ Volts	+5 Volts	ACHIEVED	ACHIEVED
Size	60x60mil ANACHIP	-	ACHIEVED	ACHIEVED



## 2.2. Predicted Performance

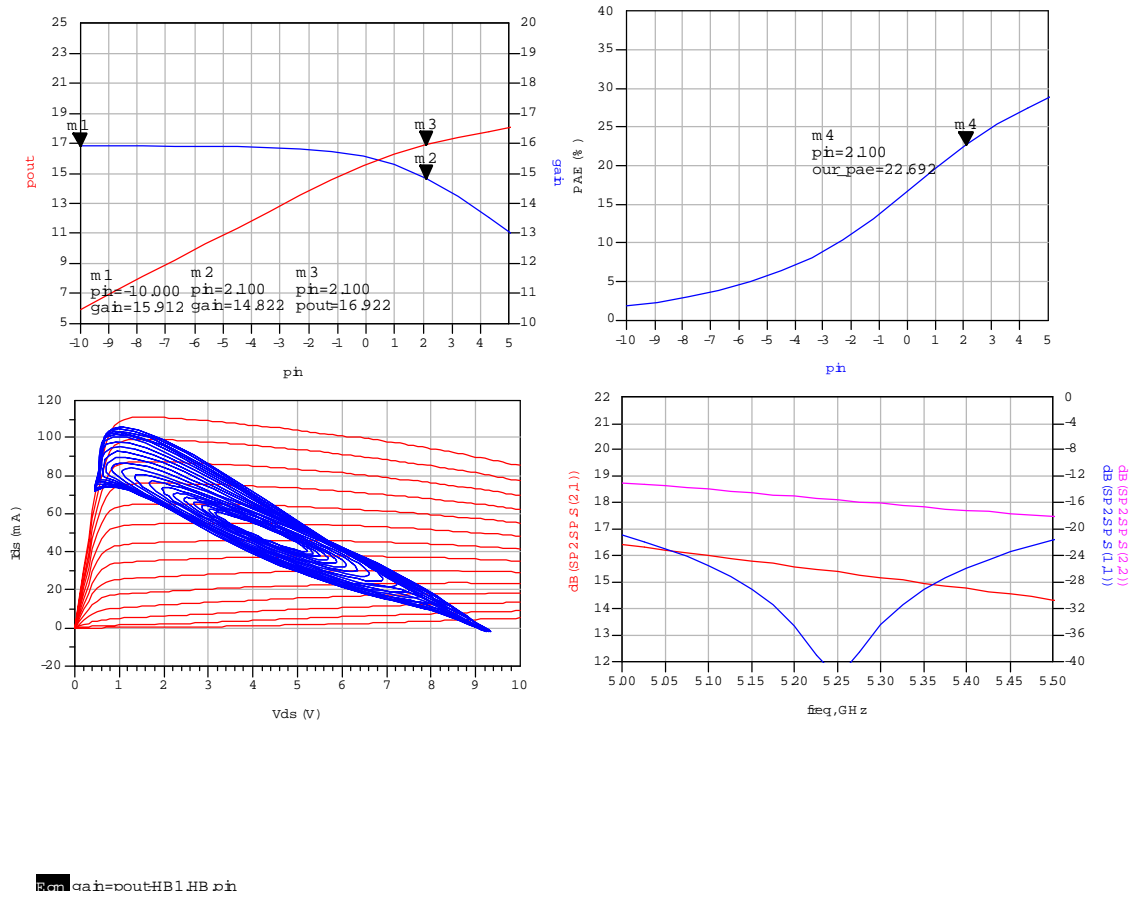
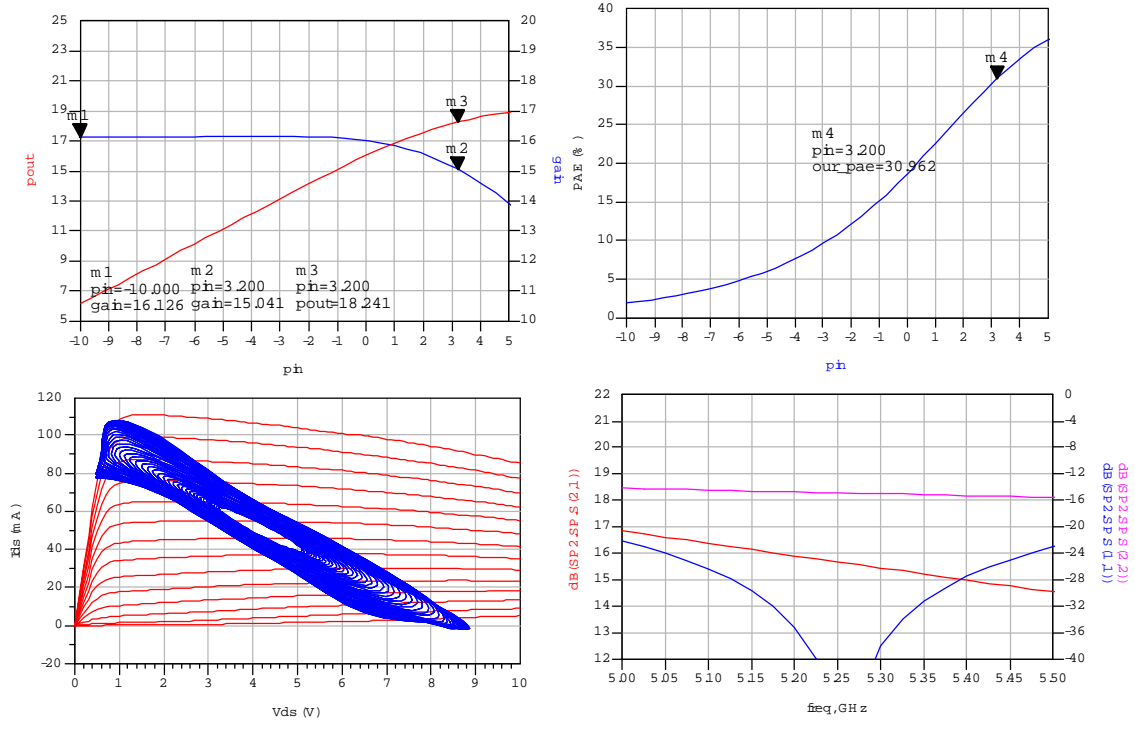


Figure 2: Overall Performance (Post-layout)



Sim: gain=pout-HR1\_HR.ph

Figure 3: Overall performance (Pre-layout)

# Schematic Diagrams

R1	24
R2	445
R3	114
R4	34
R5	300
R6	10
R7	14
R8	300
Vdd	5V
C1	0.46 pF
C2	12 pF
C3	12 pF
C4	0.13 pF
C5	0.66 pF
C6	12 pF
C7	12 pF
C8	0.71 pF
C9	1.64pF
L1	1840 pH
L2	5000 pH
L3	3000 pH
L4	3000 pH
L5	3500 pH
Q1	GFET 300um
Q2	GFET 300um

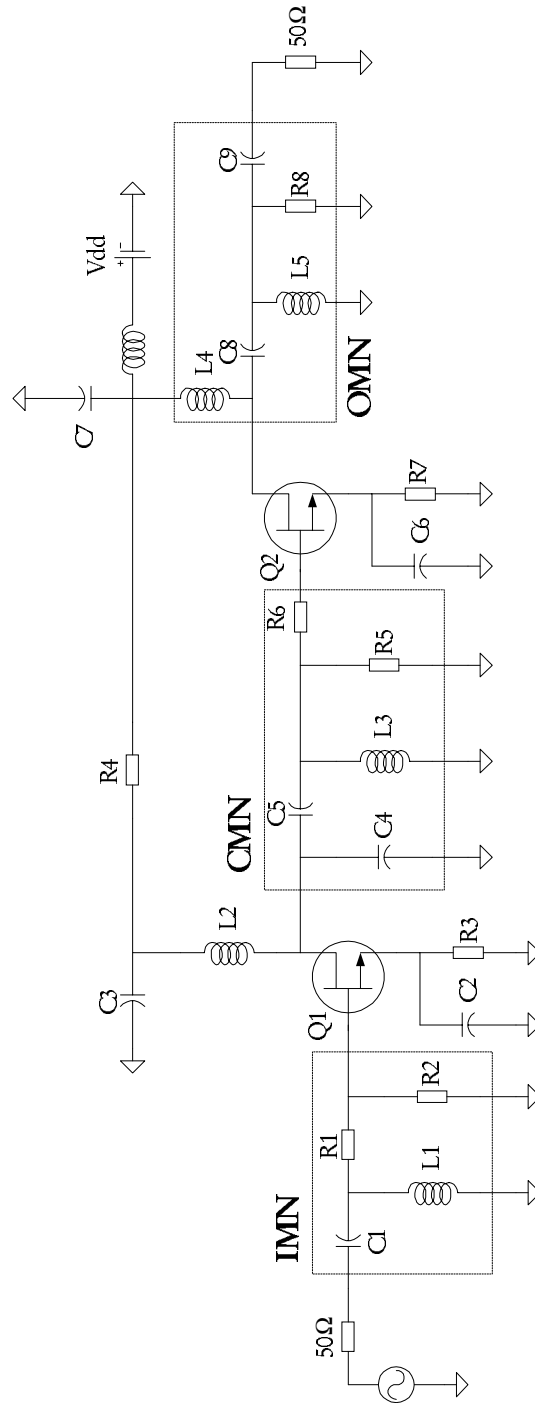


Figure 4: Self-bias Schematic (Pre-layout)

### 3. DC Analysis

#### 3.1. Simplified DC Schematic

R1	24
R2	445
R3	114
R4	34
R6	10
R7	14
Vdd	5V
Q1	GFET 300um
Q2	GFET 300um

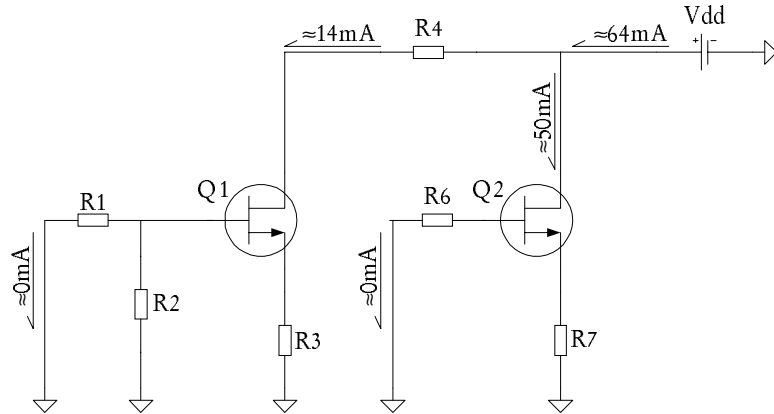


Figure 5: Simplified DC Schematic

#### 3.2. Bias Check

Both stages are biased from a single drain supply of +5V. This feature was achieved via a self-bias topology (Figure 5).

Table 2: Modeled DC Analysis (Pre-layout)

Stage	Vgs (V)	Vds (V)	Ids (mA)
1	-1.54	3	14
2	-0.7	4.3	50

#### 3.3. Interconnect and Component DC Current Stress

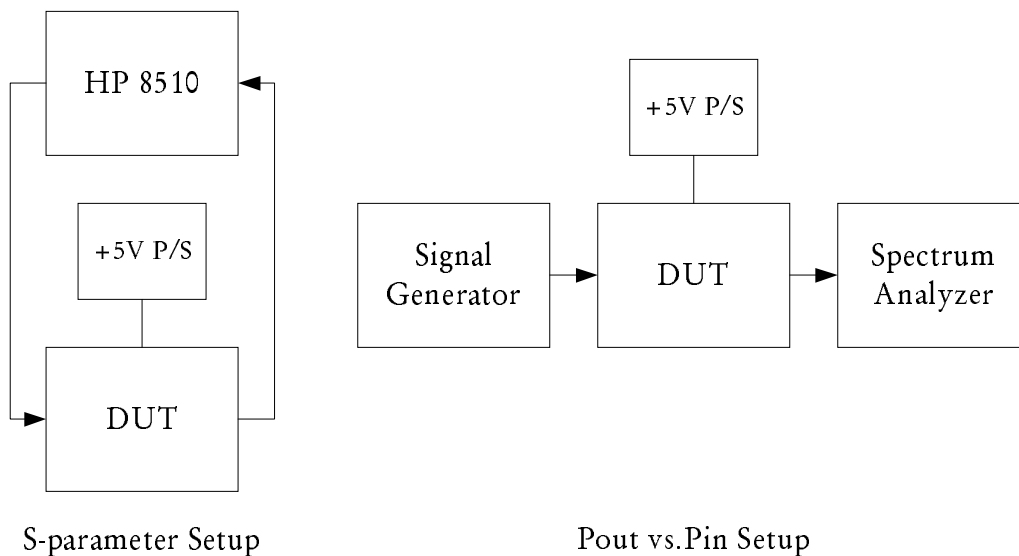
The NiCr resistors and all other interconnects used in the layout meets the current stress requirement. The resistors and the interconnects are specified to handle 1 and 18 mA per micron, respectively. A break-down of the current handling capability of the ‘high-risk’ resistors is summarized in Table 3. The maximum specified DC current stress rating is obtained by the following expression:  $I_{max} = (\text{Width} \times \text{Rating in mA per micron}) \times 150\%$ .

**Table 3: Resistor Current Stress Rating**

Resistor	Width (um)	Current (mA)		
		Max. spec.	Nominal	Worst-case
R3	50	50	14	21
R4	25	25	14	21
R7	76	76	50	75

## 4. Test Plan

- Setup test bench (Figure 6) to measure total current and s-parameters
- Apply bias – the total current should be approximately 64mA based on DC analysis.
- Measure s-parameters – chip level probe testing with the Wiltron VNA; the chip has one RF input and one RF output, and one DC input.
- Setup test bench (Figure 6) to measure 1dB gain compression
- Apply bias
- Measure power vs. pin at 5150, 5250, and 5350 MHz – increase the input incrementally while recording the output power.

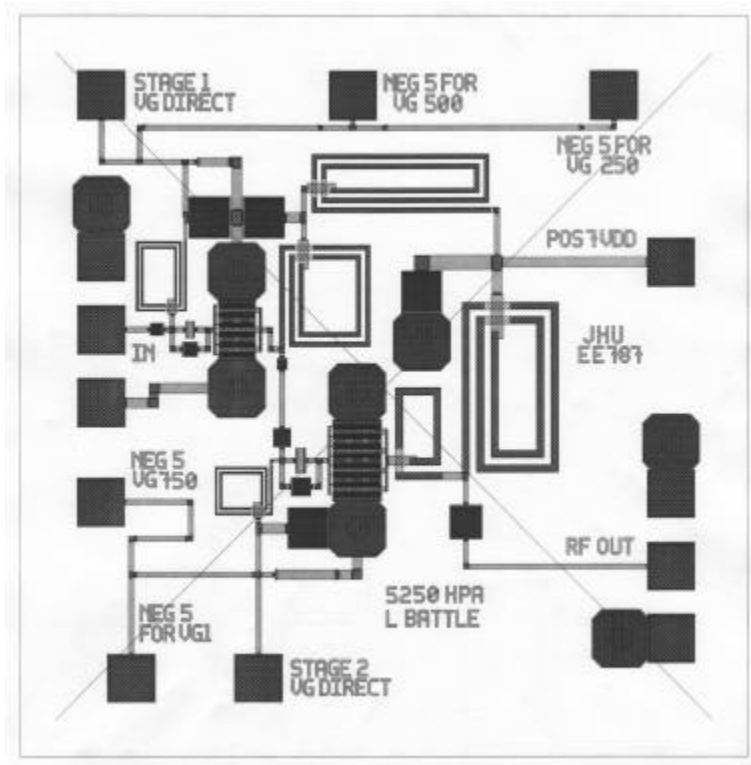


**Figure 6: Test set-up**

## 5. Conclusions & Recommendations

The two-stage general-purpose amplifier met all of its design specifications. I recommend tuning the output matching network if more margin on the output VSWR is desired. Also, I recommend checking performance based process variations. The process variations can be minimize by adding a resistor ladder.

# C Band Power Amplifier Design and Layout Using Agilent ADS and Triquint Element Library



Design and Report Prepared by Lee Battle  
EE525.787 MMIC Design  
Johns Hopkins University, Whiting School of Engineering  
December 13, 2000

## Abstract

The purpose of this exercise was to design a ¼ Watt C Band MMIC HPA utilizing Agilent/HP ADS software for eventual circuit fabrication by Triquint. Performance requirements were given for the design which included frequency range, gain, ripple, output power, and VSWR. Circuit layout was restricted to a standard 60x60 mil package. Class F operation was targeted for improved efficiency but was not realizable using standard Triquint elements within the allotted time. All other performance requirements were achieved using a two-stage design with Triquint GFET transistors. The complete design process included device selection, circuit design, circuit modeling and simulation, and physical layout. A test plan is included for testing of first unit to verify actual performance versus modeled performance.

## Introduction

Performance requirements for the design are listed in Table 1.

**Table 1 -- Design Requirements**

Parameter	Design Requirement/Goal
Operating Frequency Range:	5150 to 5350 MHz
Bandwidth:	> 200 MHz
Gain:	> 12 dB (15 dB Goal)
Gain Ripple over Frequency:	$\pm 0.5$ dB
Output Power (P1dB):	> +24 dBm
Efficiency (Power Added Efficiency):	> 20% @ P1dB (25% Goal)
Input and Output VSWR:	< 1.5:1
Supply Voltage:	+7 V and -5 V
Physical Layout:	60 x 60 mil ANACHIP package with standard Triquint elements

The most restrictive parameters in the design were the overall 60x60 mil size restriction and the limitation of devices to standard Triquint elements. This restricted the design to Triquint EFET, DFET, or GFET transistors and restricted other passive elements and interconnects to a size that would fit within the chip outline when physically laid out. Initially, the second stage output matching network to achieve the design goal of Class F operation was to be implemented towards the end of the design process. However, the component and size restrictions hindered achieving this goal.

The design assumed two stages of cascaded gain were required to achieve the required gain of 12dB (15 dB goal). The second (output) stage was designed to provide maximum power output while the first (input) stage was designed for maximum gain. The design of the second (output) stage was selected as the starting point due to its influence on the critical output power performance requirement.

The second (output) stage was designed using a Cripps output match approach to maximize output power. The Triquint GFET type power transistor was selected and a range of device sizes were DC simulated to create series of DC Characteristic Curves. A 800  $\mu\text{m}$  GFET (8 gate fingers x 100  $\mu\text{m}$  per gate finger) size was selected to give voltage swing of 12 volts p-p (based on drain bias supply of +7 V) and peak current of 300 mA to achieve device limited output power of 450 mW (+26.5 dBm). Setting the bias to  $I_{DS}=100$  mA was expected to yield an output power of 300 mW (+24.8 dBm). This operating point also had the advantage of requiring a  $Z_I=62 \Omega$  for a Cripps match output. This would allow for a good compromise between achieving a maximum output power match (62  $\Omega$ ) and a near ideal  $Z_o$  match (50  $\Omega$ ). The nonlinear model was biased and an S-parameter simulation was performed to model the  $R_{ds}$  and  $C_{ds}$  of the device. Input series resistance was used to achieve unconditional stability from 0.5 GHz to 10.5 GHz (approximately twice normal operating frequency). Parallel capacitance was added to the input resistance to recover gain at higher frequencies while still maintaining a  $\mu$  factor greater than one. Using the  $R_{ds}$  and  $C_{ds}$  model of the transistor and the required Cripps  $Z_I$  an output matching network (OMN) was designed with an integrated shunt inductance component for adding drain bias to the circuit. A new S-parameter simulation for the FET with OMN was used to generate a conjugate match input matching network (IMN) to maximize gain. A shunt inductor was also incorporated in the IMN for adding gate bias to the circuit. Simulation of the second (output) stage with ideal elements yielded 10.2 dB of gain and an output power (P1dB) of +26 dBm. Tuning of the circuit for improved performance was held until modeled Triquint elements were substituted for ideal elements for expediency in design.

Given the gain for the second stage of approximately 10 dB with a final target output power of +24 dBm for the cascaded circuit, a target minimum output power (P1dB) for the first (input) stage was determined



to be +14 dBm. In order to ensure that the first (input) stage would not compress before the second (output) stage and limit the overall amplifier, extra margin was added to the requirement for the device selection. A 450  $\mu\text{m}$  GFET (6 gate fingers x 75  $\mu\text{m}$  per gate finger) size was selected which had a device limited maximum output power of 250 mW or 24 dBm. Using the device with reduced bias ( $V_{gs}$ ) and conjugate match for maximum gain, a more reasonable output power (P1dB) of approximately 18-20 dBm was assumed. This would operate the first (input) stage at a reasonable 4 dB back-off point even if the second (output) stage gain was reduced once Triquint modeled elements were substituted for ideal. This over sizing of the first stage would be at the expense of overall efficiency with the intention that future iterations of the design could reduce the device size to recover efficiency once other parts of the design are tested and proven. Input and output matching networks were designed using S-parameter simulation and the nonlinear model biased at the appropriate operating point. Shunt inductance components were integrated into both matching networks to allow for drain and gate bias to be added to the circuit. Simulation of the first (input) stage with ideal elements yielded 11.1 dB of gain and an output power (P1dB) of +22 dBm. Once again tuning of the circuit was deferred until Triquint modeled elements replaced ideal elements in order to reduce the number of tuning iterations.

Since the output of the first (input) stage as well as the input of the second (output) stage were both matched to 50  $\Omega$ , the two stages could be cascaded with no changes to the matching networks. Initial simulation of the complete cascaded circuit with ideal elements yielded gain of 21.5 dB at center band (5250 MHz) and output power (P1dB) of +26.1 dBm. Wide band simulation from 0.5 to 10.5 GHz verified stability remained unconditional for the new cascaded circuit.

With a complete cascaded circuit designed and simulated with ideal elements, the next step in the design was to verify physical layout within the package constraints was achievable. Triquint modeled inductors, capacitors, and resistors were generated in the layout mode along with the two GFET transistors and ground vias. Individual L and C Triquint components were sized based on comparison simulations with ideal elements as a starting point. Working without interconnecting traces the components were arranged to form an "paper doll" layout that approximated desired final layout. This activity confirmed that physical layout within package restrictions would be possible. Subsequent steps added transmission line interconnects and refined component placement trying to minimize the overall footprint while not violating design rules or placing components in such proximity as to create potential for undesired interactions. From this physical layout ADS generated a schematic for simulation. Going from layout to schematic presented some minor but relatively surmountable problems. Such an approach worked for this circuit but would not be advisable for more complicated circuit designs.

An initial simulation of the new cascaded circuit with Triquint modeled elements and interconnects revealed a noticeable reduction in gain and a larger than expected rise in the stability factor  $\mu$ . Leaving the initial separate matching networks intact allowed for easy independent simulation of the first and second stages. After confirming high stability factors for each stage, the input stability resistance and capacitance values were adjusted to recover gain while still maintaining unconditional stability from 0.5 to 10.5 GHz. Further simulations adjusted matching network component values to optimize gain, output power, ripple, and VSWR performance. With acceptable performance, the bias networks were added and the final circuit was re-simulated to verify no bias circuit induced interactions.

At this point in the design the Class F matching network was attempted. The approach undertaken would create a short condition for the 2<sup>nd</sup> harmonic and an open condition for the third harmonic at the circuit output by the addition of a shunt L-C circuit. This would create the desired waveform shape of achieving maximum voltage and current swing while transitioning through a lower powered bias point (high voltage matched with low current, high current matched with low voltage). Initial simulations used ideal elements and yielded improved output power (P1dB) and efficiency (PAE) performance by 2-3 dB and 7-8% respectively. Unfortunately, attempts to realize the circuit with Triquint modeled elements failed since the required inductance at the 3<sup>rd</sup> harmonic (15.75 GHz) to generate the open condition appeared as capacitance due to self resonance of the spiral inductors. The only element architecture found to come close to the desired inductance (approximately 17 nH) at the required frequency was a spiral inductor of 1.25 or fewer turns that would encircle most if not all of the chip. Any simulations with Triquint modeled elements

continuously generated noticeably worse gain and efficiency at which time the Class F goal was abandoned. More on this issue is discussed in the conclusions section of this paper.

## Modeled Performance

A summary of cascaded circuit performance including Triquint modeled elements and all interconnects is listed in Table 2. The performance data listed was generated using DC, S-Parameter, and Single Tone Harmonic Balance simulations using Agilent ADS software. Design requirements are also listed in the table and compliance with each requirement is indicated.

**Table 2 -- Performance Summary and Compliance Matrix**

Parameter	Design Requirement/ Goal	Simulated Performance (including Triquint elements and interconnects)	Performance Compliance
Operating Frequency Range	5150 to 5350 MHz	5150 to 5350 MHz	Compliant
Bandwidth	> 200 MHz	> 200 MHz	Compliant
Gain	> 12 dB (15 dB Goal)	21.5 dB at 5250 MHz center frequency	Compliant
Gain Ripple over Frequency	$\pm 0.5$ dB	$\pm 0.25$ dB	Compliant
Output Power (P1dB)	> +24 dBm	+25 dBm	Compliant
Efficiency (Power Added Efficiency)	> 20% @ P1dB (25% Goal)	19.6%	Not-Compliant*
Input and Output VSWR	< 1.5:1	1.4:1 (Input) 1.5:1 (Output)	Compliant
Supply Voltage	+7 V and -5 V	+7 V and -5 V	Compliant
Size	60 x 60 mil ANACHIP	60 x 60 mil	Compliant
Mode of Operation	Class F	Class A	Non-Compliant*

\* **Non-Compliance for Efficiency and Mode of Operation** - Class F Operation was not achievable due to component restrictions at high frequencies (for reasons previously discussed in Introduction section of this paper). The mode of operation is the primary reason for efficiency non-compliance. A secondary reason for low efficiency is the over-sizing of transistors for the initial iteration of the design to ensure high output power performance.

Complete plots of simulation results are included on the following pages. Listed results include:

**Figure 1 -- Simulation Results – Circuit With Ideal Elements (page 5)**

- Power Added Efficiency
- Gain
- Dynamic Load Line
- Stability
- Input and Output Impedance (VSWR and Return Loss)
- Gain Compression

**Figure 2 -- Narrowband Simulation Results - Triquint Elements and Interconnects (page 6)**

- Gain
- Stability
- Gain Compression
- Input and Output Impedance (VSWR and Return Loss)
- Dynamic Load Line
- Power Added Efficiency

**Figure 3 -- Wideband Simulation Results - Triquint Elements With Interconnects (page 7)**

- Gain

- Stability
- Input and Output Impedance (VSWR and Return Loss)

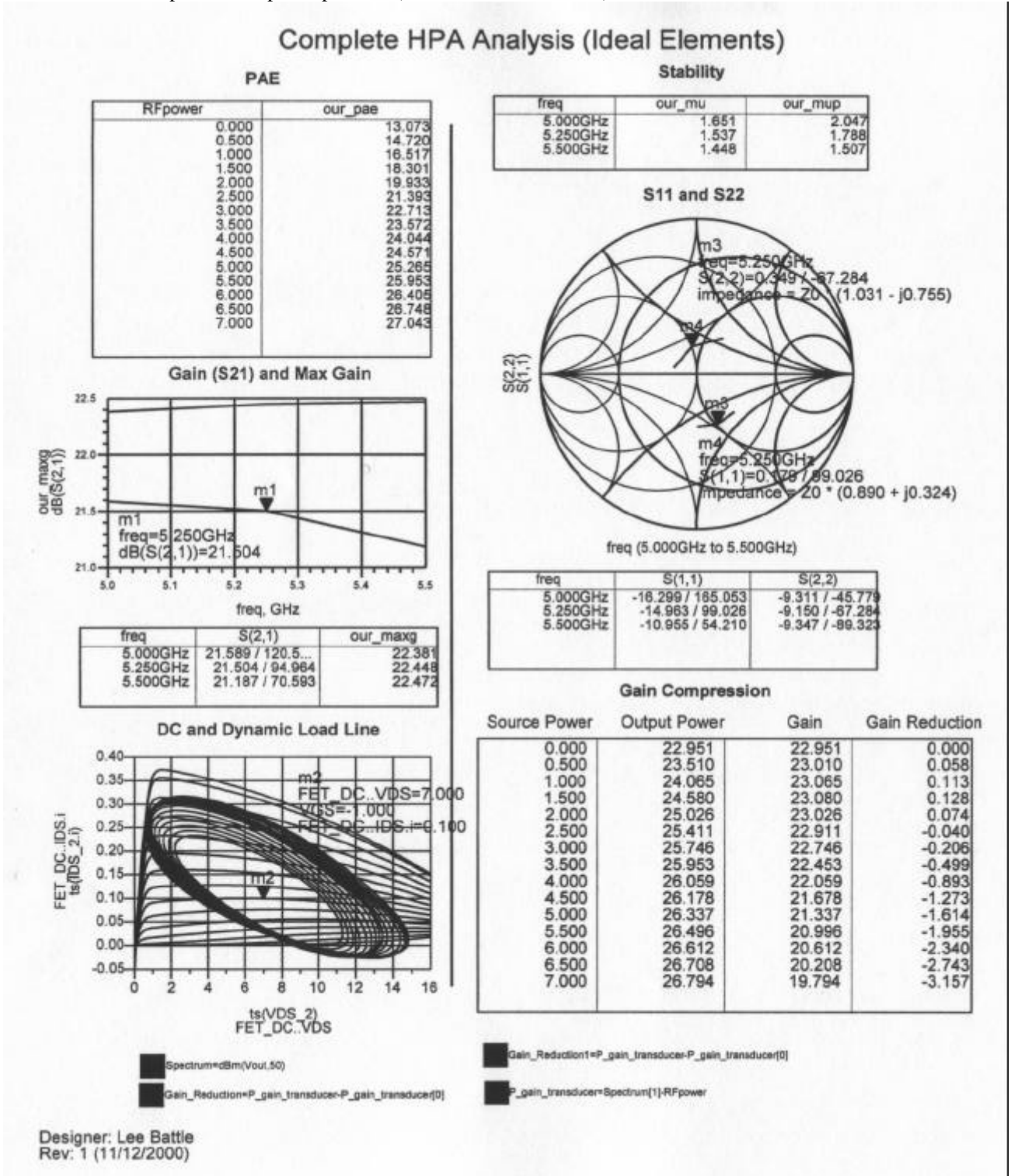
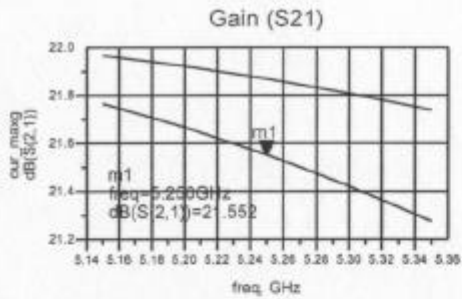


Figure 1 -- Simulation Results – Circuit With Ideal Elements

Complete HPA - Narrowband Analysis  
(Triquint Elements and Interconnects)



freq	S(2,1)	our_maxg
5.150GHz	21.766 / 67.497	21.967
5.200GHz	21.668 / 61.345	21.922
5.250GHz	21.552 / 55.369	21.869
5.300GHz	21.421 / 49.567	21.808
5.350GHz	21.277 / 43.941	21.739

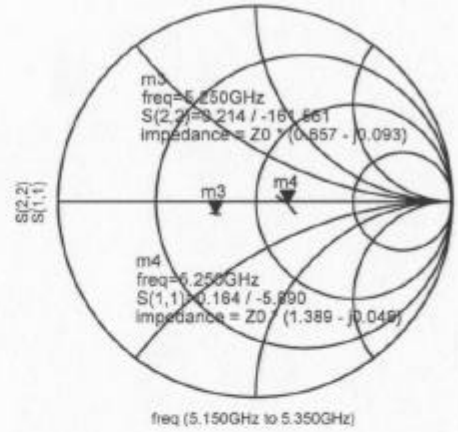
Stability

freq	our_mu	our_mup
5.150GHz	2.960	3.835
5.200GHz	2.639	3.447
5.250GHz	2.725	3.126
5.300GHz	2.621	2.870
5.350GHz	2.528	2.667

Output Power Compression (P1dB)

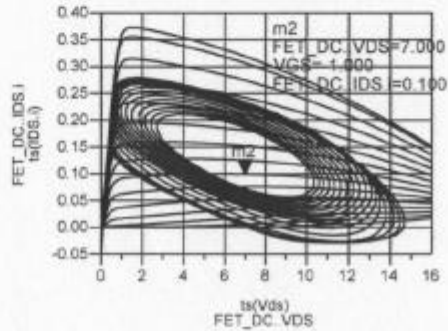
Source Power	Output Power	Gain	Gain Reduction
-3.000	19.752	22.752	0.000
-2.500	20.292	22.792	0.040
-2.000	20.836	22.836	0.084
-1.500	21.379	22.879	0.127
-1.000	21.918	22.918	0.166
-0.500	22.441	22.941	0.189
0.000	22.934	22.934	0.162
0.500	23.384	22.884	0.132
1.000	23.797	22.797	0.045
1.500	24.175	22.675	-0.078
2.000	24.489	22.489	-0.263
2.500	24.738	22.238	-0.515
3.000	24.984	21.984	-0.768
3.500	25.242	21.742	-1.011
4.000	25.379	21.379	-1.373
4.500	25.434	20.934	-1.818
5.000	25.476	20.476	-2.277

Input and Output Match - Return Loss



freq	S(1,1)	S(2,2)
5.15GHz	-19.45 / 14.51	-14.56 / -1.58E2
5.20GHz	-17.35 / 2.68	-13.95 / -1.60E2
5.25GHz	-15.69 / -5.89	-13.39 / -1.62E2
5.30GHz	-14.37 / -12.88	-12.88 / -1.63E2
5.35GHz	-13.29 / -18.39	-12.43 / -1.65E2

Dynamic Load Line Output Stage



Efficiency

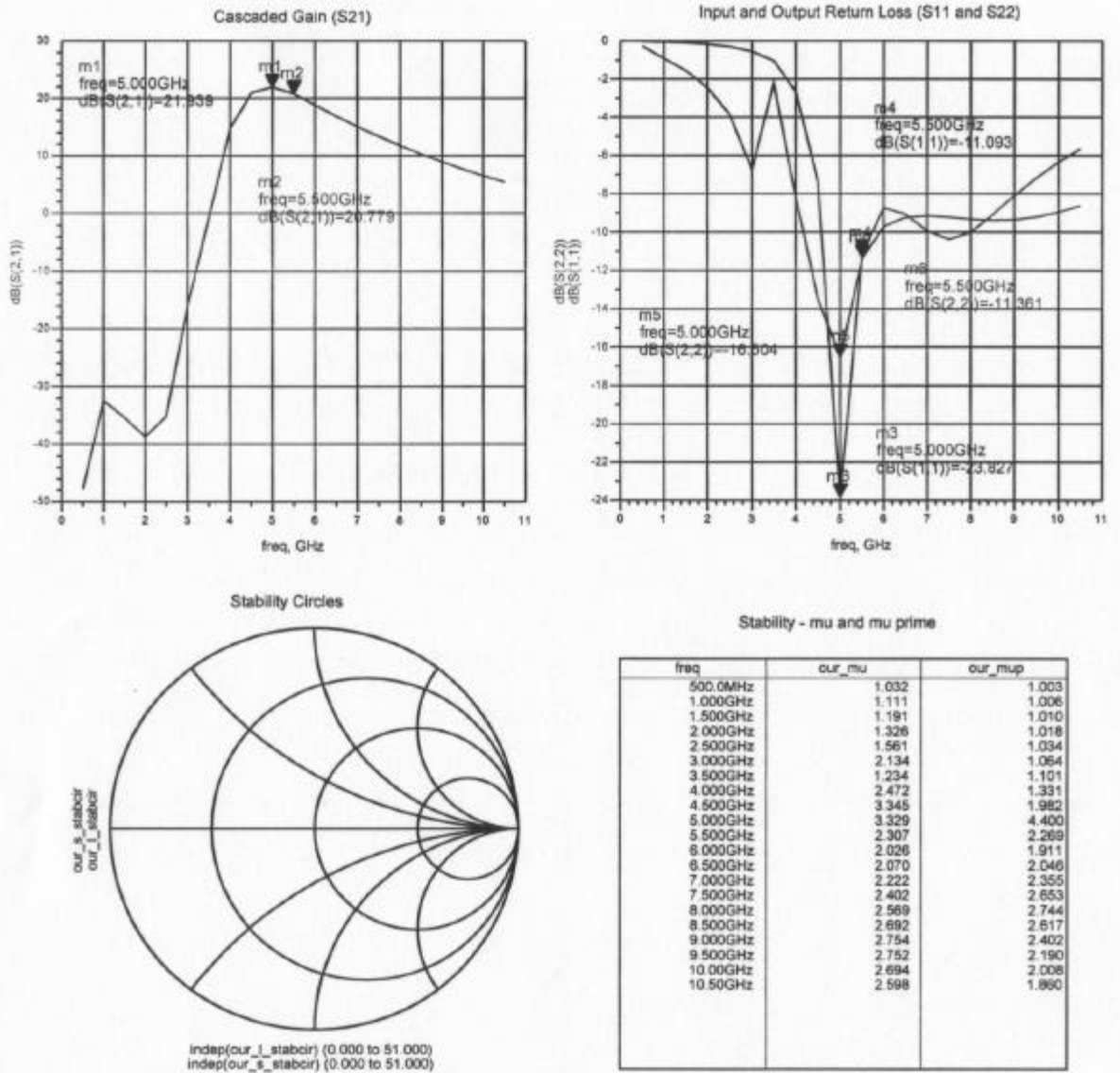
RFpower	our_pae
-3.000	5.740
-2.500	6.484
-2.000	7.325
-1.500	8.273
-1.000	9.328
-0.500	10.477
0.000	11.685
0.500	12.914
1.000	14.158
1.500	15.412
2.000	16.653
2.500	17.981
3.000	19.575
3.500	21.200
4.000	22.127
4.500	22.615
5.000	22.985

Spectrum#dBm(Vout,50) Gain\_Reduction#P\_gain\_transducer-P\_gain\_transducer Gain\_Reduction#P\_gain\_transducer-P\_gain\_transducer P\_gain\_transducer=Spectrum(1)-RFpower

Designer: Lee Battle Filename: Final Narrow 12/4/2000

Figure 2 -- Narrowband Simulation Results - Triquint Elements and Interconnects

Complete HPA - Wideband Analysis  
(Triquint Elements and Interconnects)



Designer: Lee Battle    Filename: Final Wide    12/4/2000

Figure 3 -- Wideband Simulation Results - Triquint Elements With Interconnects

## **Schematics and Layout Diagrams**

Schematics and a layout diagrams for the complete circuit are included on the following pages. Diagrams and details for each are as follows:

**Figure 4 -- Simple Schematic (no interconnects) (page 9)**

This schematic includes all circuit elements using Triquint equivalent models. Microstrip interconnects have been omitted to simplify schematic viewing. The schematic illustrates the RF signal input at the left and RF signal output at the right. Circuit bias is provided using a common +7 V drain bias connection and individual gate bias connections. Connections are provided for fixed value gate bias ( $V_{gs}$ ) using resistor divider networks and a fixed -5 V DC supply or a direct connection can be used to provide variable gate bias ( $V_{gs}$ ) using an adjustable DC supply.

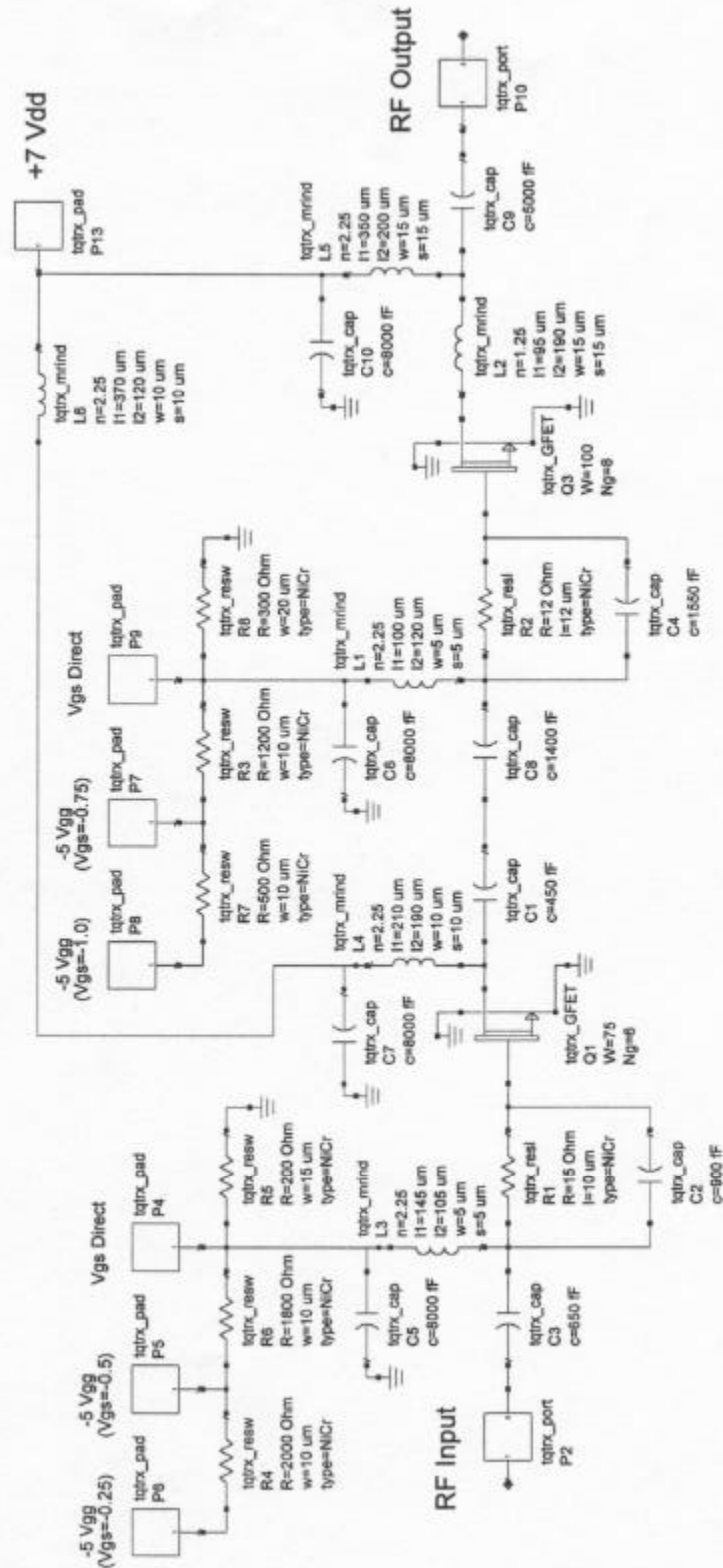
**Figure 5 -- DC Schematic (no interconnects and inductors) (page 10)**

This schematic illustrates a DC equivalent of the circuit including bias supply voltages and replacing inductors with equivalent DC shorts. Node voltages and currents are indicated from ADS simulation. Actual gate and drain voltage and drain-source currents have been highlighted (Note that an error exists in second stage gate bias schematic labels - connection port for  $V_{gs}=-1.0$  actually provides -0.75 and alternate bias port for  $V_{gs}=-0.75$  actually provides -1.0 - the labeling is correct in actual layout).

**Figure 6 -- Final Layout (page 11)**

This figure illustrates the final layout of the complete two-stage HPA. All connection ports are labeled appropriately.

Complete HPA - Simple Schematic  
No Interconnects Included



Designer: Lee Battle Filename: Tri\_Cascade\_Simple 12/3/2000

Figure 4 -- Simple Schematic (no interconnects)

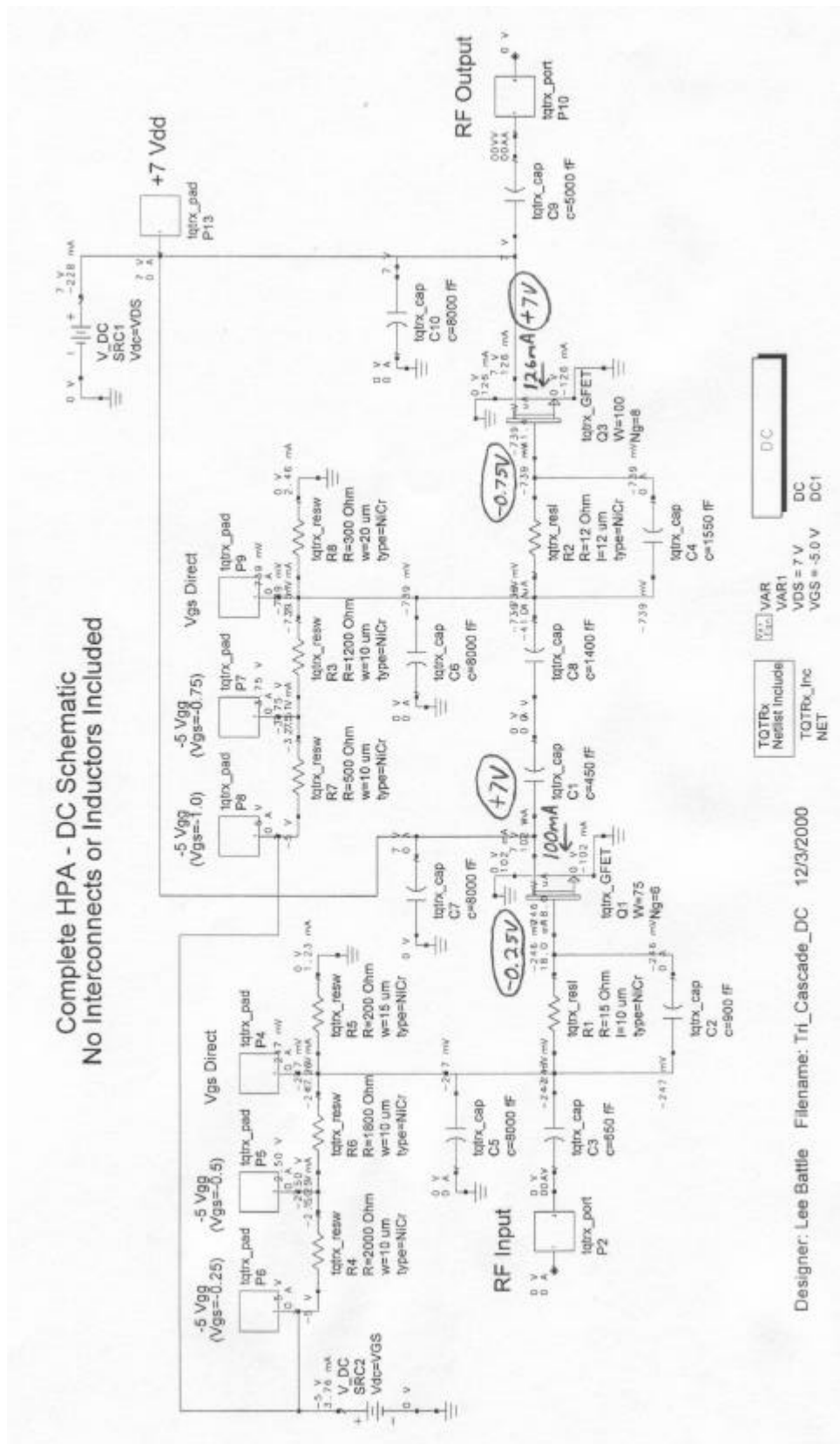


Figure 5 -- DC Schematic (no interconnects and inductors)



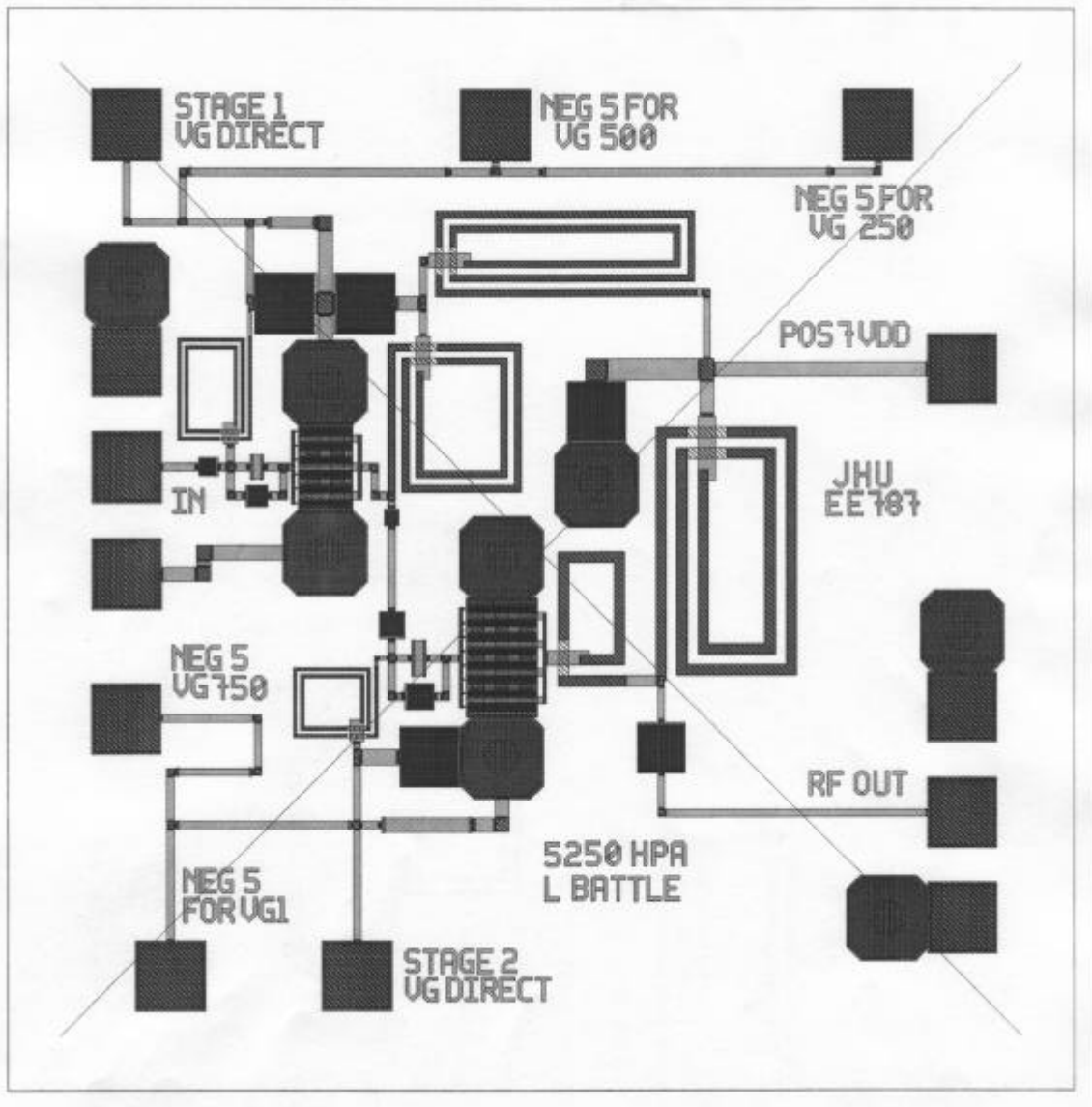


Figure 6 -- Final Layout

## Test Plan

This section outlines the test plan for test of measurement of actual circuit after fabrication.

### Equipment required

- Wafer probe station to provide connection capability to circuit under test
- Network analyzer with appropriate cables and calibration standards
- DC power supply for applying circuit bias
- DC voltage and current measurement equipment

### **Visual Inspection Testing**

**Purpose:** To identify any visually obvious errors or defects prior to applying power to circuit and attempting performance measurements.

**Setup:** Requires inspection of circuit under test using wafer probe station.

- Procedure:**
1. Install the circuit under test into the wafer probe station (if not already installed)
  2. Visually inspect the circuit and compare to paper plot of layout generated during design phase. Verify proper circuit is to be tested and no obvious errors or defects exist (inverted circuit elements, missing elements, fabrication defects).

### **DC Testing**

**Purpose:** To verify proper DC operation including verification of bias voltage and currents

**Setup:** Requires connection to circuit under test using wafer probe station, application of appropriate DC voltages with power supplies, and DC voltmeter/ammeter probe.

- Procedure:**
1. Install the circuit under test into the wafer probe station (if not already installed)
  2. Apply +7V DC to +7 Vdd connection port on circuit. Apply -5V DC to first stage -5 Vgg ( $V_{gs}=-0.25$ ) connection port. Apply -5V DC to second stage Vgs Direct connection port (this will set second stage to pinch-off)
  3. Measure and record +7 Vdd current consumption and compare with expected (100 mA). Measure and record actual first stage Vgs voltage and compare with expected (-0.25 V)
  4. Repeat procedure placing first stage into pinch-off and applying -5V to appropriate connection ports (for  $V_{gs}=-0.75$  V). Measure and record actual current and voltage and compare with expected values.
  5. Apply -5 V to appropriate bias connections for both first and second stage for normal operation. Measure and record actual total current consumption and compare with expected value.

### **Swept Frequency Testing**

**Purpose:** To measure small signal circuit performance using a single tone, swept frequency input signal at a fixed power level.

**Setup:** Requires connection to circuit under test using wafer probe station, application of appropriate DC voltages with power supplies, and input signal injection and output signal measurement using a network analyzer.

- Procedure:**
1. Install the circuit under test into the wafer probe station (if not already installed). Apply appropriate DC bias to circuit.
  2. Setup and calibrate network analyzer for a narrow band frequency sweep from 5.0 to 5.5 GHz with a signal power level of approximately 0 dBm and connect analyzer to appropriate amplifier signal ports.
  3. Measure and record S-parameter performance and compare to expected values. Repeat measurements for different bias conditions if desired.
  4. Setup and calibrate network analyzer for a wide band frequency sweep from 0.5 to 10.5 GHz (or as restricted by test equipment) with a signal power level of approximately 0 dBm.
  5. Measure and record S-parameter performance and compare to expected values. Repeat measurements for different bias conditions if desired.

### **Swept Power Testing**

**Purpose:** To measure circuit performance using a single tone, swept power input signal at a fixed frequency.

**Setup:** Requires connection to circuit under test using wafer probe station, application of appropriate DC voltages with power supplies, and input signal injection and output signal measurement using a network analyzer.

**Procedure:**

1. Install the circuit under test into the wafer probe station (if not already installed). Apply appropriate DC bias to circuit.
2. Setup and calibrate network analyzer for a power sweep from -3.0 dBm to +4.0 dBm frequency of 5.25 GHz and connect analyzer to appropriate amplifier signal ports.
3. Measure and record gain compression performance and compare to expected values. Repeat measurements for different bias conditions if desired. Measurements can also be made over other swept power ranges if desired.

### **Conclusions and Recommendations**

Dependant upon results from actual circuit measurement, a second iteration of the design could improve a few areas. One area for possible improvement would be reevaluating the size of the particular transistors used. If actual measured data indicates margin in output power capability, the devices could be resized and/or bias changed to reduce the DC power consumption and improve efficiency. Also, matching networks could be tuned based on measured data to improve input/output match and an inter-stage matching network could be developed to possibly eliminate some components and reduce overall circuit footprint. A new attempt could be made at achieving Class F operation by trying one of three approaches. The first approach would be to develop a different circuit topology that does not require such a large value of inductance at the 2<sup>nd</sup> and 3<sup>rd</sup> harmonic frequencies. A second approach would be to consider use of an off chip inductor. This would help achieve the desired inductance value but possibly introduces some new problems related to packaging and proximity of matching network to transistor output. A third approach would be to consider Class F matching network requirements simultaneously with impedance and power capability when sizing the FET device. This may yield better results since the value of inductance needed for the matching network is proportional to the modeled  $R_{ds}$  and  $C_{ds}$  transistor values.

The design effort was considered successful since the majority of the design goals were achieved within the given time period. Goals not achieved include Class F operation and power added efficiency due mostly to difficulties realizing the desired circuit topology using the modeled elements. Aside from those requirements, all other design goals were achieved in some instances with respectable margin. The most difficult challenge to overcome during the design process was related to learning HP ADS software and gaining access to design equipment (computer lab). Quite a few years have passed since this designer has used this particular simulation package not to mention the various changes and updates that have occurred during that time. Accessing the simulation software and workstation while maintaining normal working hours at my job was difficult. This problem was somewhat alleviated when weekend hours became available.

C BAND MMIC UP/DOWN  
CONVERTER FINAL REPORT

by

Ray Gabany

Johns Hopkins University

Fall 2000

Johns Hopkins University

Abstract

C BAND MMIC UP/DOWN  
CONVERTER FINAL REPORT

by Ray Gabany

Course Instructors: Craig Moore and John Penn  
Department of Electrical Engineering

The need for Monolithic Microwave Integrated Circuit (MMIC) mixers that can operate as both up and down converters for a HIPERLAN 5.2 chip set is the driving force behind this work. This paper introduces a novel approach to the design and development of a MMIC C band up/down converter that fits on a 60 x 60 mil chip. The goals are to convert a 350 MHz IF up to 5150 to 5350 MHz RF with an LO of 4800 to 5000 MHz. The mixer must also be able to mix the RF frequencies down to an IF frequency of 350 MHz. Bias supply to the diodes are used for starved LO operation while a lumped element hybrid is used for supplying signals to the mixing diodes.

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## ACKNOWLEDGMENTS

The author wishes to thank Craig Moore and John Penn of Johns Hopkins University/Applied Physics Labs for their tutelage and instruction of a MMIC design course, which made the design of this MMIC possible. The author also wishes to thank Gary Wray and Agilent for the use of the Advanced Design System (ADS) software, which was used to design this MMIC. Finally, the author wishes to thank TriQuint Semiconductor for the device models and the fabrication of the MMIC so that the device could be tested and the measurements compared to the simulated data.



## GLOSSARY

**DFET.** TriQuint Semiconductor D-Type Field Effect Transistor

**IF.** Intermediate Frequency

**LO.** Local Oscillator

**MMIC.** Monolithic Microwave Integrated Circuit

**MIM.** Metal Insulated Metal

**MLIN.** Microstrip Line

**MTEE.** Microstrip Tee Interconnection

**NiCr.** Nickel Chromium

**RF.** Radio Frequency

## *Chapter 1*

### INTRODUCTION

This chapter introduces a description of the circuit as well as the design philosophy used to select the circuit topology and the trade-offs associated with this selection.

#### Circuit Description

The circuit topology selected is a 180-degree hybrid rat race mixer, with shunt FET diodes. The mixer is comprised of a lumped element 180-degree hybrid and 100 $\mu$ m DFETs with the drain and source tied together to form a schottky diode.

The local oscillator (LO) is applied to the shunt DFET diodes through a 180-degree lumped element hybrid where the LO signal is injected into the hybrid port and splits the LO into a 180-degree phase difference between the two shunt DFET diodes. RF and IF ports share the same port of the lumped element hybrid. The signals for the RF and IF are separated by using a simple inductor-capacitor high pass filter structure for the RF port and the IF port uses a low pass filter structure.

Bias is easily supplied to the DFETs through a bias line since the DFET diodes are in a shunt configuration. The bias voltage is divided with a pair of NiCr resistors in a voltage divider configuration in order to ease the power supply requirements when fine-tuning to lower voltages.

## Design Philosophy

The design philosophy was driven by several factors. The first is the available choices of mixer circuits could be used in order to perform both up conversion and down conversion. This leads to selection of the popular double balanced mixers or the rat race mixer since 90-degree hybrid mixers can only mix up or down based on the orientation of the diodes.

The second criterion was which of the remaining choices would satisfy the other requirements. Since the double balanced mixer would require two more diodes than the 180-degree hybrid mixer, the LO requirements would be greater as well as the bias supply requirements. The double balanced mixer would also require baluns that would exceed the size specification of a 60 x 60 mil ANACHIP.

Therefore, the proper selection was that of a 180-degree lumped element hybrid rat race mixer. The classic approach is to tie the other side of the diodes together to form the IF port of the mixer. This however would make the routing more difficult since the diodes would be at opposite corners of the hybrid. To tie them together would require routing under or over the RF port of the mixer on the MMIC.

Therefore, a novel approach was taken were the DFET diodes would be used in a shunt configuration. This placed the IF port at the same port as the RF where by the phase and power between the diodes would be 0-degrees and evenly split.

## Trade-Offs

The trade-offs of this approach are several. First the impedance matching of the DFET diodes at their bias condition greatly affects the VSWR of the 180-degree hybrid. Varying the bias of the DFET diodes moves the VSWR of the LO, RF, and IF match around. Baluns used in a double balanced configuration would

have better VSWR as opposed to a singly balanced 180-degree mixer whose VSWR is dependent on the diode match.

Second the port-to-port isolation is also dependent on the filters as opposed to that of a doubly balanced mixer. The LO to RF isolation however is equal to that of the hybrid isolation as evident in the compliance matrix. Since size was an important specification, the double balanced mixer was too large.

The shunt diode mixer on the other hand had several good trade-offs opposed to the classic hybrid mixer approach. The first is that the IF filter would have been necessary in the classic approach as well so no extra space was required. The shunt diode approach also provided a means of placing the DFET diodes at the corners of the hybrid without routing over or under the RF port. And finally, the injection of the bias for the starved LO was easy to achieve using shunt DFET diodes.

Since the conversion loss was greater than the specification, better matching for the DFET diode impedances over a larger range of bias conditions may be necessary to improve performance.

## Chapter 2

### MODELED PERFORMANCE

This chapter begins with the specification compliance matrix and then looks at plots of the simulated performance. The plots for the final layout version of the chip are illustrated.

#### Specification Compliance Matrix

The following table is the specification compliance matrix. All of the specifications were met except for the conversion loss, which was about 1 dB higher. Several of the goals were also reached in the design of this MMIC mixer.

Table 1. Compliance Matrix

Description	Specification	Design Goal	Simulated
Frequency	RF = 5150 to 5350 MHz	RF = 5150 to 5350 MHz	RF = 5150 to 5350 MHz
	LO = 4800 to 5000 MHz	LO = 4800 to 5000 MHz	LO = 4800 to 5000 MHz
	IF = 350 MHz	IF = 350 MHz	IF = 350 MHz
Isolation (LO/RF)	10 dB min.	16 dB	16 dB typical

Conversion Loss	10 dB max.	7 dB	11 dB typical
LO Power	+10 dB max.	+7 dB	+10 dB
VSWR, 50 Ohm	2.5:1 max.	1.5:1	1.6:1 RF 1.5:1 LO 2.3:1 IF
Supply Voltage	0 to +5 V	0 to +5 V	+2.8 V typical
Size	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP

### Predicted Performance

This section begins with Figure 1, which shows the final layout simulated performance of the 180-degree hybrid. The port labeled S11 is the LO port, port S33 is the RF port, and ports 2 and 4 are the DFET diodes. The phase difference between the DFETs is about 180 degrees from the LO port. The power division between the RF/LO ports and the DFET diodes is around 3 dB.

The Hybrid layout uses the TriQuint elements such as spiral inductors, MIM capacitors, MLIN, and MTEE interconnections.

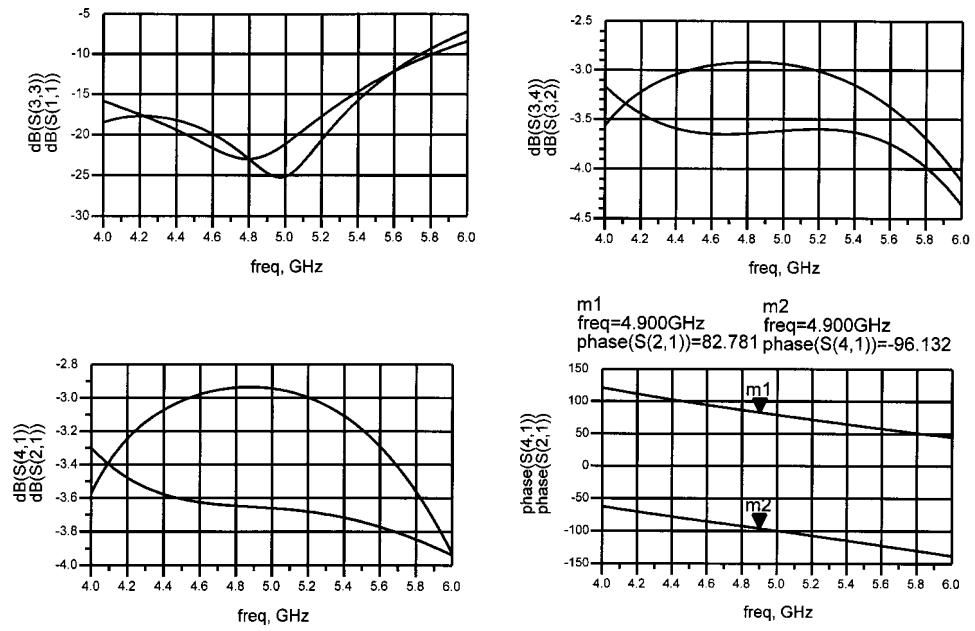


Figure 1. Final Hybrid

Figure 2 shows the simulated plots of the RF and IF filters used to separate the RF and IF signals that share the same port of the mixer.

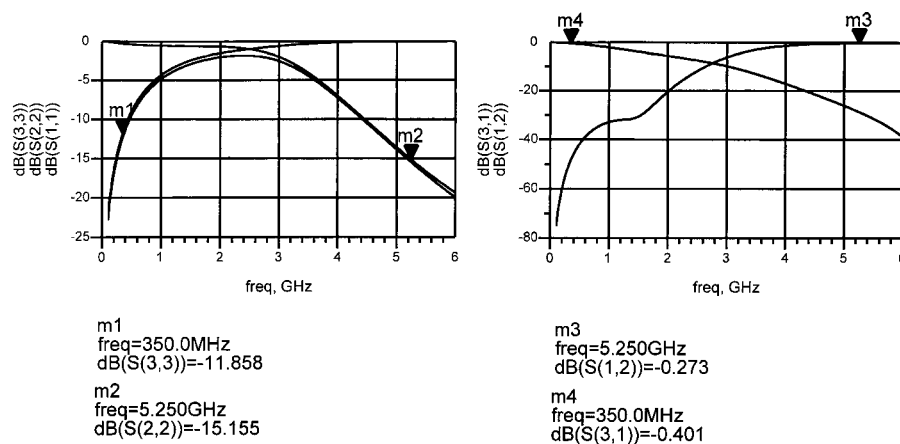


Figure 2. RF/IF Filters

Figure 3 shows the match and hence the compliance with the VSWR specification for the final layout of the mixer. This plot was obtained by setting the DC bias at around 0.7 V drops across the DFET diodes.

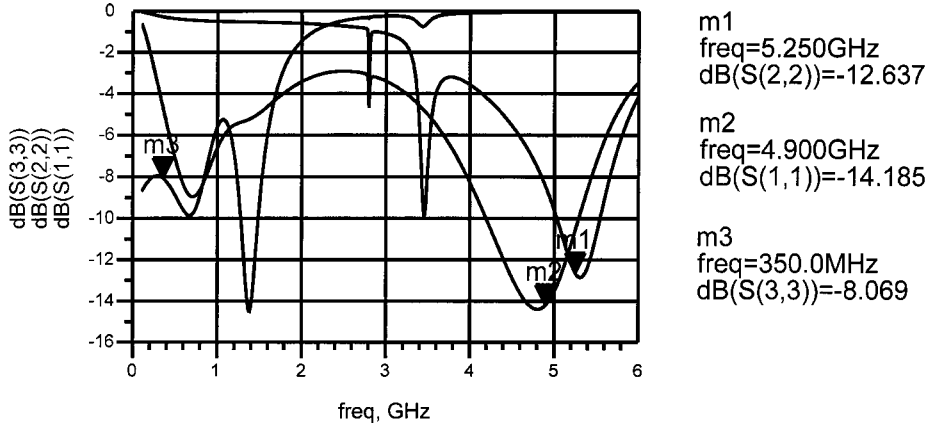


Figure 3. Mixer Match

Figure 4 shows a close up of the mixer matches at the RF, LO, and IF ports. The match is broad enough that slight variations in processing should still maintain the desired match at the ports.

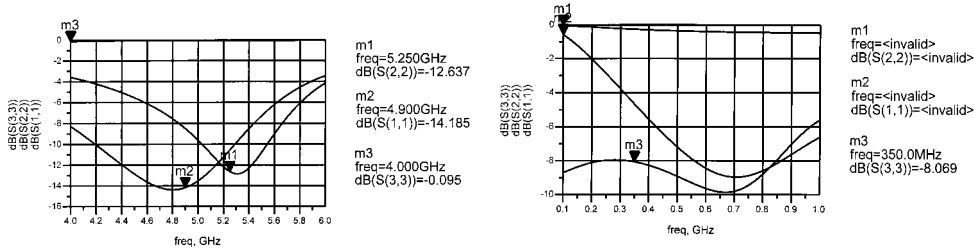


Figure 4. Port Matches

Figures 5, 6, and 7 show the mixer conversion loss and frequency spectrum for the low band, mid band, and high band response of the mixer as a down



converter. This was simulated using an LO power of +10 dBm and an RF input power of -20 dBm.

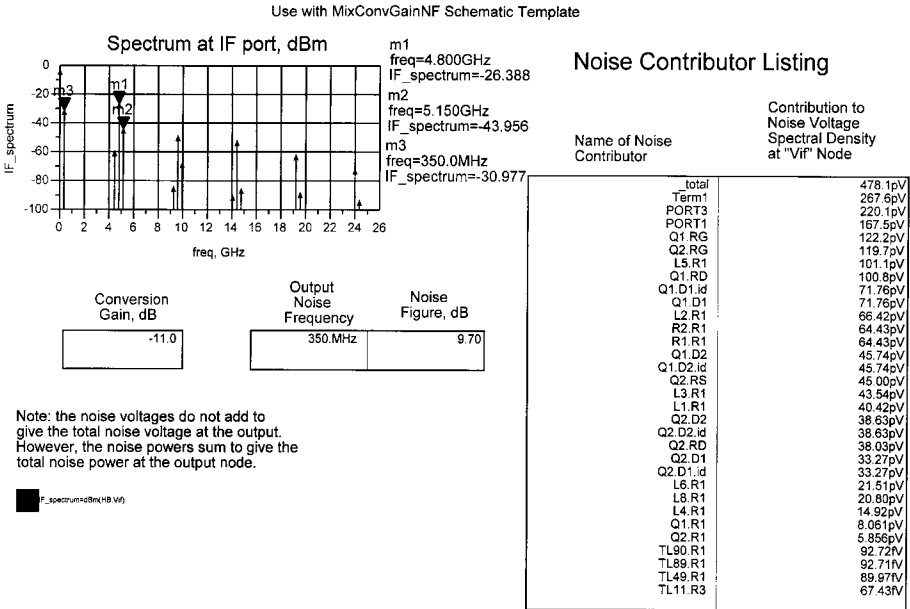
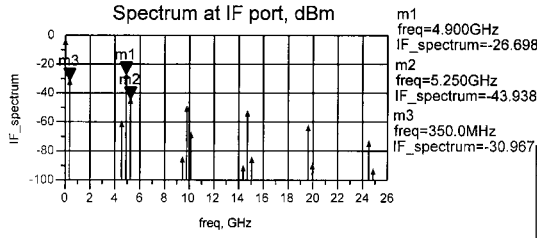


Figure 5. Down Converter (Low Band)

Use with MixConvGainNF Schematic Template



Conversion Gain, dB	Output Noise Frequency	Noise Figure, dB
-11.0	350.MHz	9.64

Note: the noise voltages do not add to give the total noise voltage at the output. However, the noise powers sum to give the total noise power at the output node.

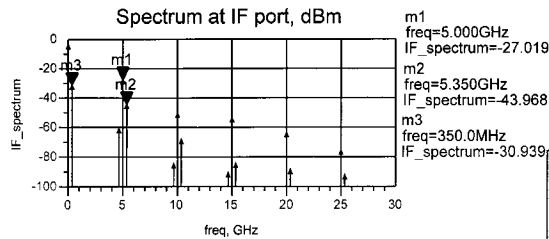
$F_{\text{spectrum}}(\text{dB}) = (\text{dB V})$

### Noise Contributor Listing

Name of Noise Contributor	Contribution to Noise Voltage Spectral Density at "Vif" Node
_total	476.9pV
_Term1	267.2pV
PORT3	221.2pV
PORT1	169.2pV
Q1.RG	120.6pV
Q2.RG	118.8pV
L5.R1	100.7pV
Q1.RD	99.46pV
Q1.D1.id	71.62pV
Q1.D1	71.62pV
L2.R1	66.86pV
R2.R1	63.50pV
R1.R1	63.50pV
Q1.D2	45.87pV
Q1.D2.id	45.87pV
Q2.RS	43.79pV
L3.R1	43.53pV
L1.R1	40.78pV
Q2.D2	37.33pV
Q2.D2.id	37.33pV
Q2.RD	37.24pV
Q2.D1	32.50pV
Q2.D1.id	32.50pV
L6.R1	21.19pV
L8.R1	20.80pV
L4.R1	13.72pV
Q1.R1	8.131pV
Q2.R1	5.251pV
TL90.R1	92.97fV
TL89.R1	92.95fV
TL49.R1	89.62fV
TL11.R3	67.65fV

Figure 6. Down Converter (Mid Band)

Use with MixConvGainNF Schematic Template



Conversion Gain, dB	Output Noise Frequency	Noise Figure, dB
-10.9	350.MHz	9.61

Note: the noise voltages do not add to give the total noise voltage at the output. However, the noise powers sum to give the total noise power at the output node.

$F_{\text{spectrum}}(\text{dB}) = (\text{dB V})$

### Noise Contributor Listing

Name of Noise Contributor	Contribution to Noise Voltage Spectral Density at "Vif" Node
_total	475.6pV
_Term1	268.9pV
PORT3	222.5pV
PORT1	170.5pV
Q1.RG	119.0pV
Q2.RG	113.9pV
L5.R1	100.3pV
Q1.RD	98.11pV
Q1.D1.id	71.85pV
Q1.D1	71.85pV
L2.R1	67.21pV
R2.R1	62.58pV
R1.R1	62.57pV
Q1.D2	46.30pV
Q1.D2.d	46.30pV
L3.R1	43.50pV
Q2.RS	42.61pV
L1.R1	41.22pV
Q2.RD	36.45pV
Q2.D2.d	34.70pV
Q2.D2	34.70pV
Q2.D1.d	30.63pV
Q2.D1	30.63pV
L6.R1	20.87pV
L8.R1	20.36pV
L4.R1	12.81pV
Q1.R1	8.540pV
Q2.R1	6.007pV
TL90.R1	93.25fV
TL89.R1	93.23fV
TL49.R1	89.28fV
TL11.R3	67.81fV

Figure 7. Down Converter (High Band)

Figures 8, 9, and 10 show the mixer conversion loss and frequency spectrum for the low band, mid band, and high band response of the mixer as an up converter. This was simulated using an LO power of +10 dBm and an IF input power of -20 dBm.

It can also be seen from these plots that since the LO power is +10 dBm and the LO leaking out of the RF port is typically -6 dBm, the LO to RF isolation is calculated to be 16 dB which is one of the goals of this design.

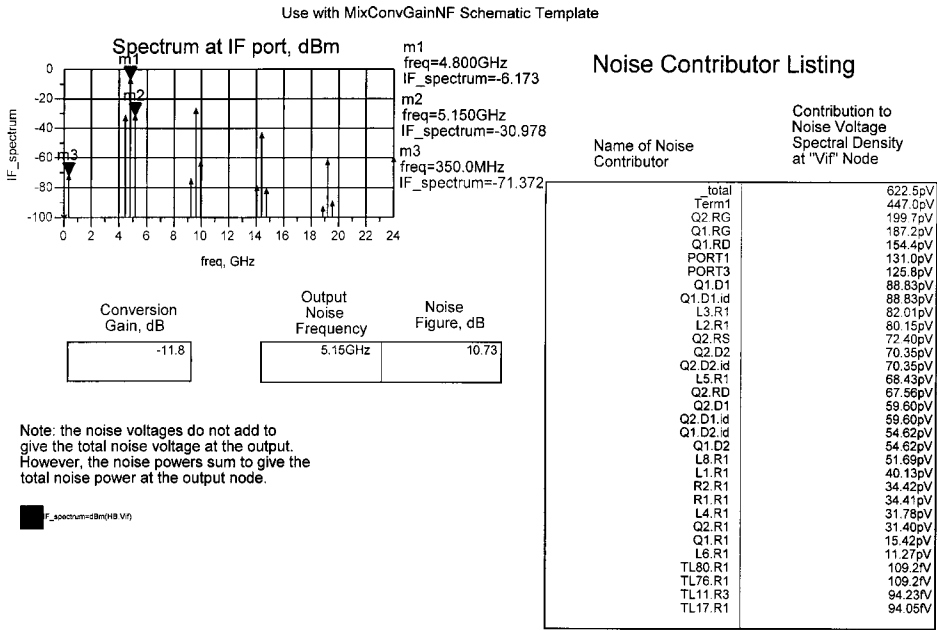


Figure 8. Up Converter (Low Band)

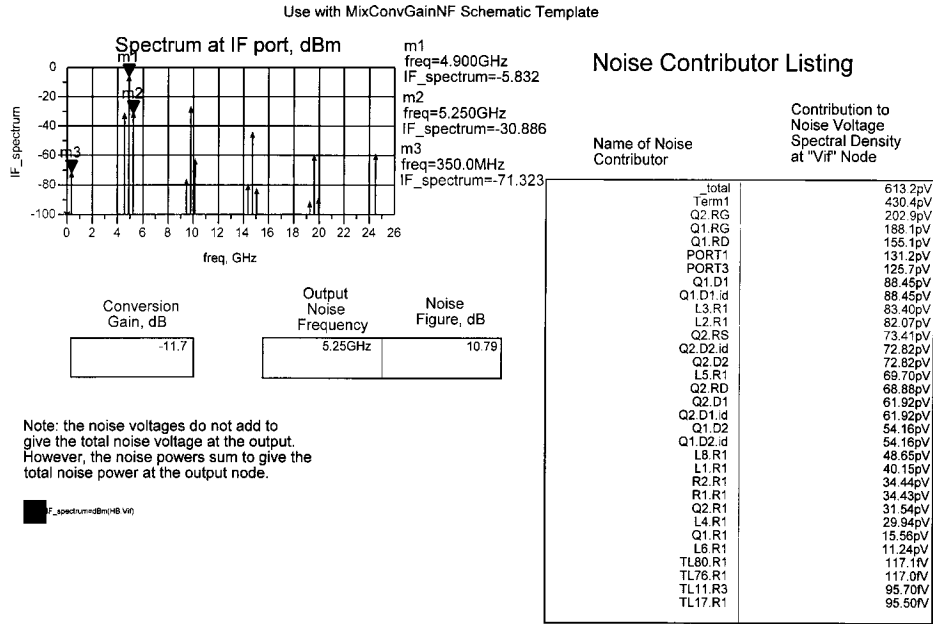


Figure 9. Up Converter (Mid Band)

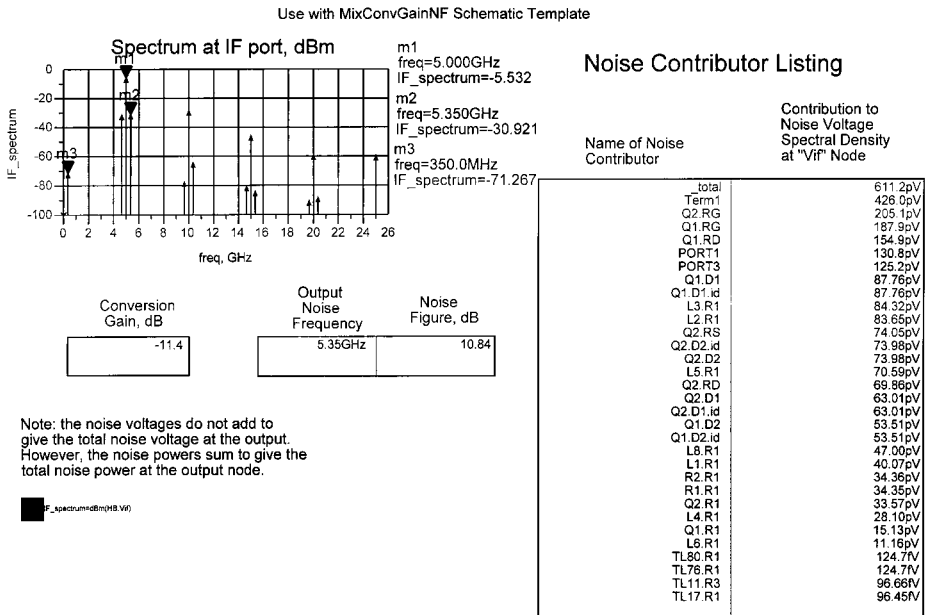


Figure 10. Up Converter (High Band)

Figure 11 shows the final layout of the C Band Up/Down Converter MMIC mixer.

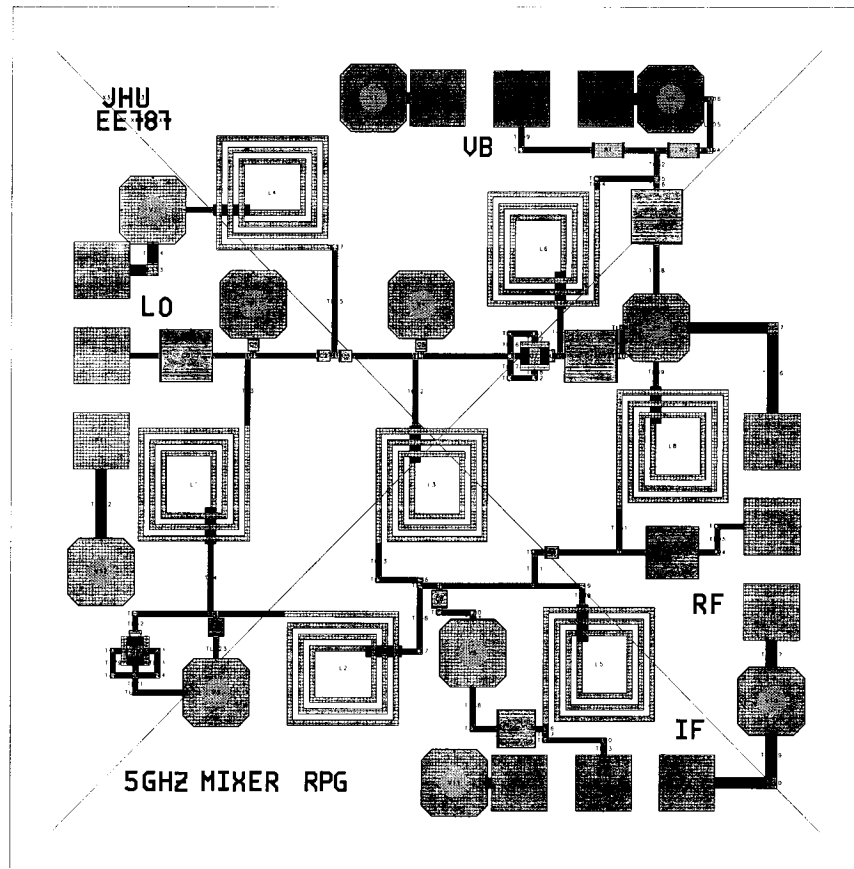


Figure 11. Final MMIC Mixer Layout

## Chapter 3

### SCHEMATIC DIAGRAM

The following Figure 12 is the simplified schematic for the C band up/down converter mixer.

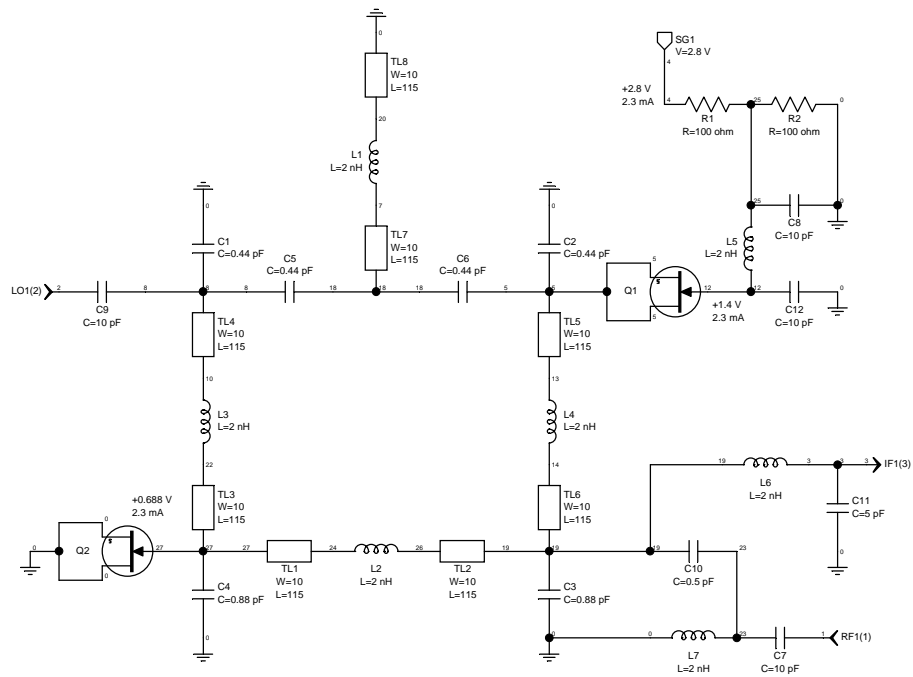


Figure 12. Simplified Mixer Schematic

The only other addition to this circuit necessary to make the mixer complete is the requirement of an external blocking capacitor for the IF port since there was no room on the MMIC to insert one.

## *Chapter 4*

### DC ANALYSIS

The schematic of Figure 12 in Chapter 3 shows the DC bias voltages and currents. The external biases for all the simulations were set to +2.8 V and a current of 2.3 mA. This gave a +0.7 V drop across the DFET diodes to turn them on and allow for operation of a starved LO.

The resistive divider allows for fine-tuning of the voltage drops across the DFET diodes without making difficult adjustments to the power supplies during test.

## Chapter 5

### TEST PLAN

The following test plan is offered to assist in the taking of the measurements of the mixer for comparison with the simulated results. Figure 13 shows the test equipment requirements and MMIC Mixer connections for measuring down and up conversion. The solid lines are for down conversion measurements and the dashed lines are for up conversion measurements.

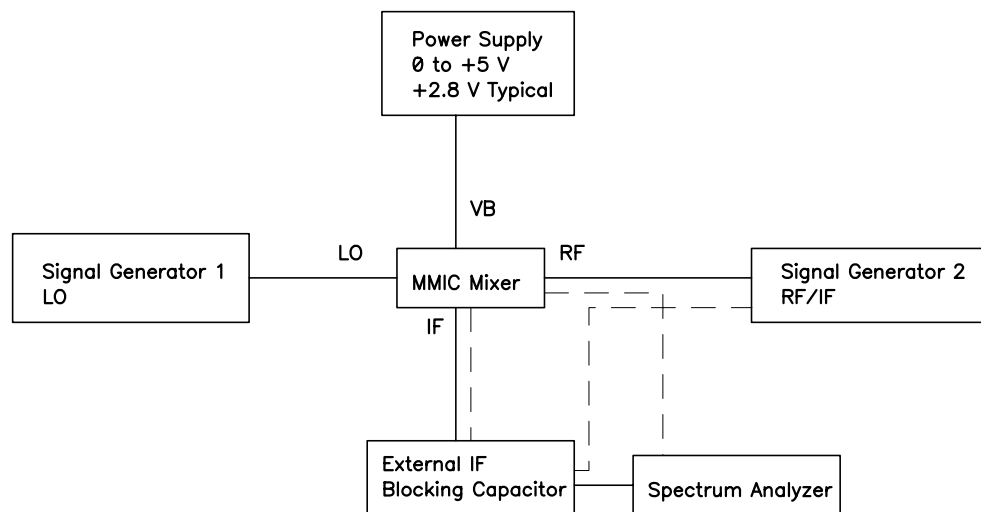


Figure 13. Test Setup

The signal generator for the LO should be set to +10 dBm and the other signal generator for the RF/IF should be set to a power level of -20 dBm. This will provide for measurements that are comparable to the simulated results. These results would be displayed on the spectrum analyzer in the form of a frequency spectrum similar to Figures 5 through 10.



For VSWR measurements a directional coupler should be placed at the LO, RF, and IF ports so that reflected power can be measured on a power meter and used to calculate the VSWR of each port. An alternative method would be if the Wiltron or some other vector network analyzer can accommodate mixer measurements, then the VSWR of each port could be swept over frequency rather than measuring the reflected power at specific frequencies.

## *Chapter 6*

### CONCLUSIONS AND RECOMMENDATIONS

A novel approach to a MMIC C band up/down converter was presented with simulated performance of a final layout version. The simulated results show that a shunt DFET diode mixer could be designed using a 180-degree lumped element hybrid with good results. This allowed for easier layout on a 60 x 60 mil ANACHIP and for bias supply injection.

The specifications were met with some of the goals achieved except for the conversion loss. Better matching of the DFET diodes could be achieved over a broader range if more room was available. This would provide better VSWR over a broader frequency range and would be less susceptible to process variations. Although the conversion loss was higher than desired, the conversion loss was very flat across the RF and LO frequencies.

Finally, sharper filters for the RF and IF ports could be used by adding more sections if more room was available. This would provide better RF to IF isolation which is dependent on the filters. Also an on-chip blocking capacitor for the IF port would be desired if more room on the chip could be achieved.

## REFERENCES

Maas, Stephen A., *Microwave Mixers, Second Edition*. Artech House, Inc., 1993.

Pozar, D. *Microwave Engineering Second Edition*. John Wiley & Sons, 1998.

Moore, Craig and Penn, John. *Class Handouts*. JHU/APL. 2000.



## **1.0 ABSTRACT**

Frequency doublers are the most common application of frequency multipliers due to their high efficiency, circuit simplicity, and minimum generation of unwanted harmonics. The MMIC circuit presented in this paper was designed to double the input frequency band tuned at 2.4GHz – 2.5GHz to 4.8GHz-5.0GHz with isolation for the fundamental and third harmonic  $> 16\text{dB}$ . This frequency doubler will be included in the LO chain of a simplex transceiver for the C-Band Hyperlan wireless local area network (WLAN) system.

## **2.0 INTRODUCTION**

### 2.1 Circuit Description:

This MMIC circuit consists of a frequency generator (X2), band reject filters at the fundamental and the third harmonic frequency and a bandpass filter. The nonlinear component used to generate an output signal rich in harmonics is the Triquint 300um GFET device. There is a stabilizing resistor at the input. A double supply scheme was employed to provide the proper bias to the device.

### 2.2 Design Philosophy:

The initial phase in the multiplier design is determining the feasibility of the desired performance from the specifications given. In order to do this, it was necessary to check the characteristics required from the active and passive elements that would be used to achieve the specified performance. Knowing that the multiplier design is a function of the active device's nonlinear characteristics, it is important to choose the right device based on the frequency of operation, level of input drive, bias conditions and terminations at the fundamental frequency, and its ability to generate harmonics. For this design, the 300um

GFET device was chosen and biased to operate close to pinchoff where  $V_{DS} = 5V$  and  $V_{GS} = -1.85V$ . The bias was chosen in pinchoff because in the vicinity of pinchoff a half-wave rectified sinusoidal current is generated that is rich in even harmonics. Next, it was important to design optimum input and output matching networks such that the input network is matched to the fundamental and the output network is matched to the second harmonic. The input matching network employ simple series L and shunt C topology and the output matching networks employ a simple series L topology. However, since microwave transistors are active devices with intrinsic feedback, it was necessary to check the stability of the device over a wide frequency range (.5GHz – 8GHz). After checking the stability of the device, there was noticed that within the low frequency range the device was unstable. A shunt-stabilizing resistor was incorporated at the input to increase the device's stability performance over a wide range of frequencies. The gate bias was applied to the stabilizing resistor with another simple LC network that contained a 10pF capacitor and 6pH inductor. An output filter section was needed to reject the fundamental and third harmonics. Two bandreject resonator sections were designed on the output to prevent low frequencies and frequencies higher than  $2f_0$  from being amplified by the device. The band reject resonator for  $f_0$  along with a resistor divider was used to supply the appropriate bias to the drain. Finally, a bandpass filter incorporating one resonator was added in cascade with the bandstop filter in order to achieve the desired output response.

### 2.3 Tradeoffs:

There are several tradeoffs to the particular design chosen. By fine tuning the input and output circuits to achieve maximum input VSWR at the fundamental and maximum output VSWR at the second harmonic frequency, this approach results in a narrow-band multiplier, exhibiting less than 10% fractional bandwidth. Due to the size constraints, no output amplifier design was employed to boost the output power at the second harmonic. This in turn resulted in low conversion gain of

-6dB. The biasing conditions were not optimum for this type of design. Operating closer to pinchoff would introduce stronger effects of the harmonics at the output. Due to the limitations of the nonlinear model, the operating point had to be slightly above pinchoff in order to achieve consistent results.

The bandpass resonator at the output increased the bandwidth of the design, however, it wasn't symmetric about the operating frequency band. Employing an output amplifier would cause the design to be more centered about the operating frequency and possibly eliminating the need for a bandpass filter. Utilizing a single supply topology would allow for an output amplifier, however, due to conversion problems with the simulator, a double supply topology was utilized instead.

### 3.0 MODELED PERFORMANCE

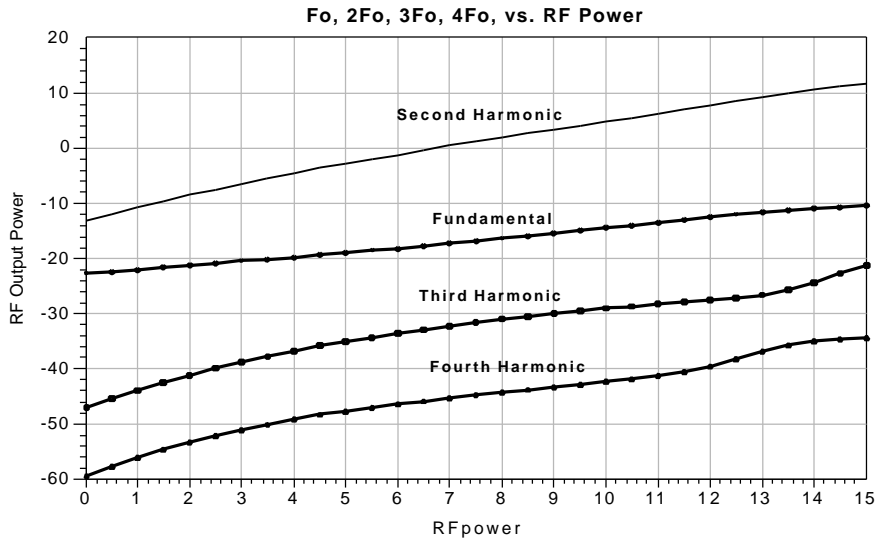
The following table gives information concerning the original specifications and the modeled results.

	Original Spec	Result Before Layout	Result After Layout
<b>Frequency</b>	Output= 4.8GHz-5.0GHz Input = 2.4GHz-2.5GHz	input= 2.4GHz-2.8GHz output= 3.5GHz-5GHz	input= 2.4GHz-2.8GHz output= 3.5GHz-5GHz
<b>Conversion Loss</b>	3dB,max; 0dBgoal	-6dB	-6dB
<b>Input Power</b>	+ 10dBm	+ 10dBm	+ 10dBm
<b>Isolation</b>	fo= 16dB,min: 25dB, goal 3fo= 20dB,min: 30dB, goal	fo= -19dB, 3fo= -33dB	fo= -19dB, 3fo= -33dB
<b>VSWR, 50</b>	2.5:1,max.; 1.5:1, goal	1.3:1,out.; 1.0:1, in	1.1:1,out.; 1.1:1, in
<b>Supply Voltage</b>	+ 5V, -5V; + 5, only	+ 6.5V, -1.85V	+ 6.5V, -1.85V
<b>Size</b>	60 X 60 mil	60 X 60 mil	60 X 60 mil

Table 3.1 Original Specifications vs. Modeled Performance

Conversion loss could have been attainable with an additional output amplifier, however, due to size limitations, this was not a viable option. The operating frequency band is sensitive to the output filter with a maximum input

match at 2.5GHz and maximum output match at 4.9GHz. The output filter added 2dB of loss to performance.



The following plots illustrate the simulated performance after layout.

Figure3.1 Output power of first 4 harmonics.

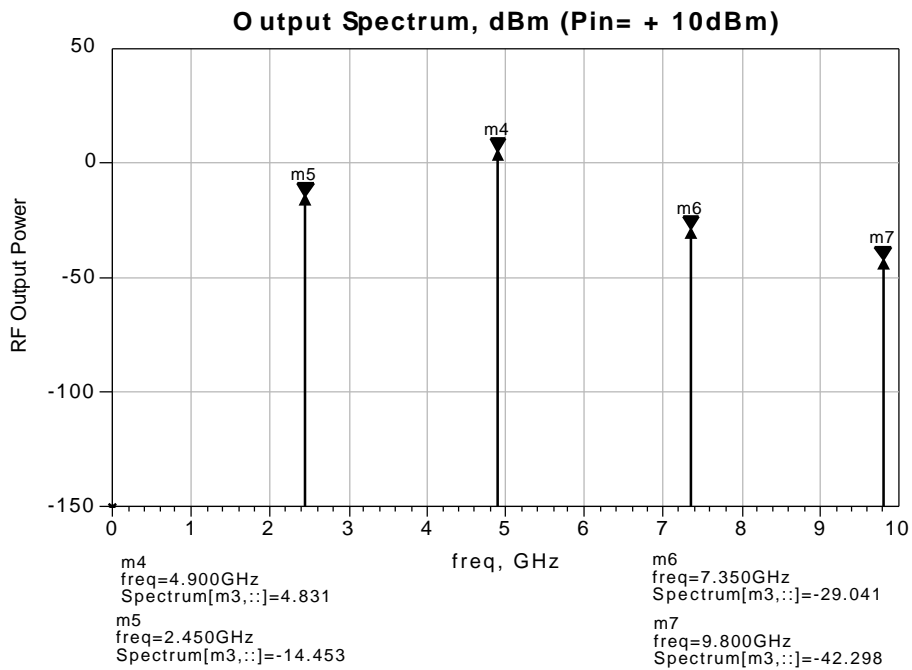
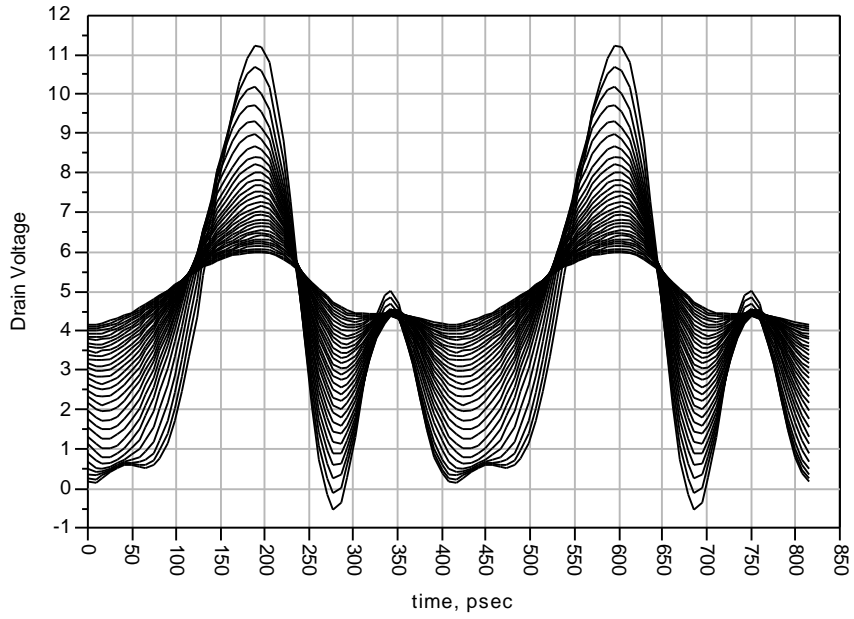




Figure3.2 Output power spectrum of first 4 harmonics

Figure3.3 Output Voltage Waveform (for  $0\text{dBm} > P_{in} > +15\text{dBm}$ )  
**O**utput Voltage **W**aveform



**O**utput **C**urrent **W**aveform

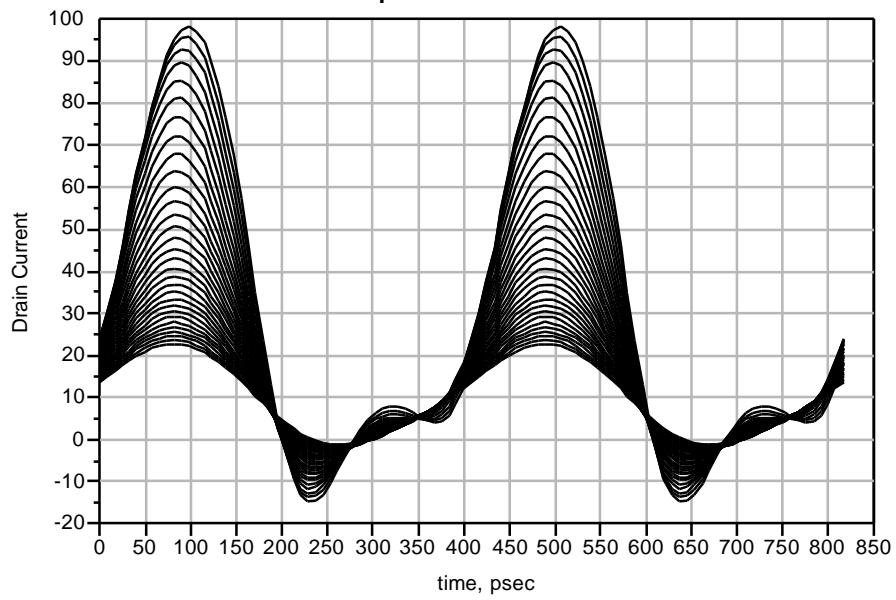


Figure3.4 Output Current Waveform (for 0dBm>Pin> +15dBm)

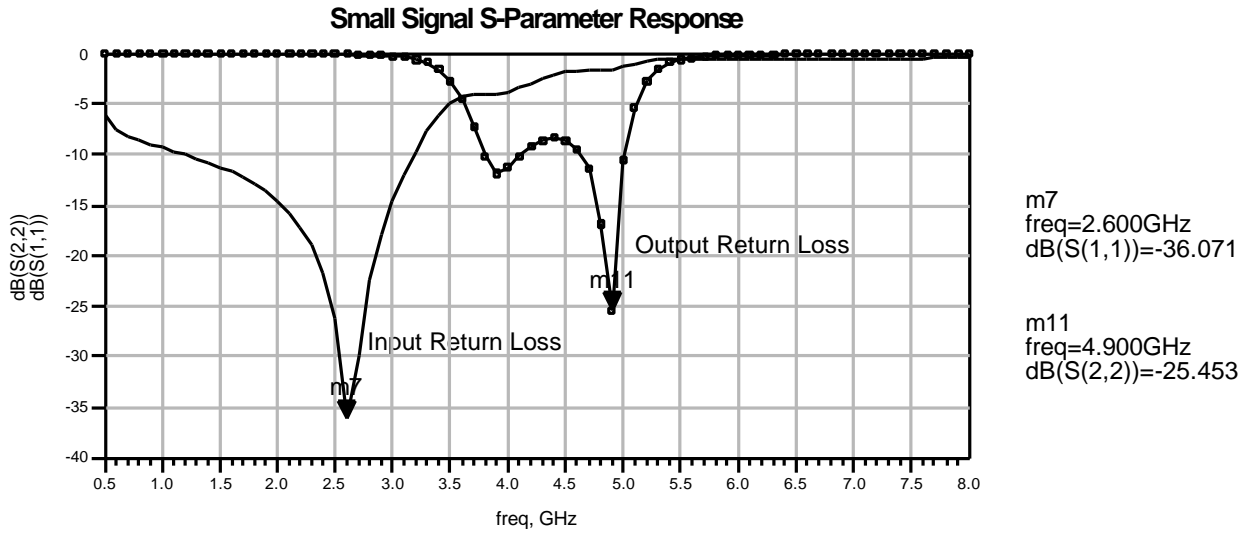
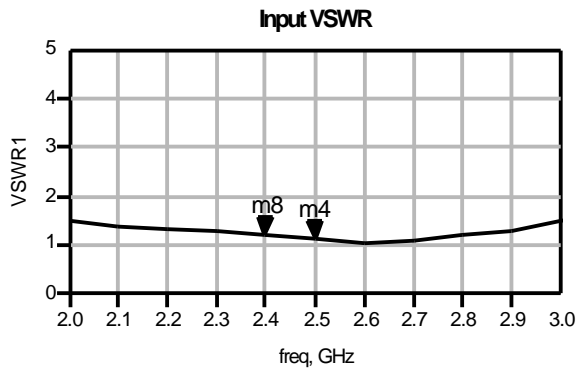
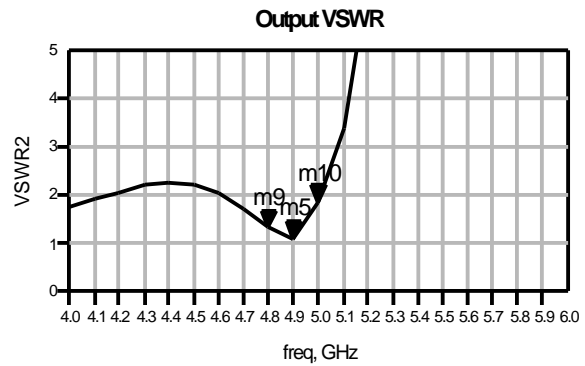


Figure3.5 Input and Output Match Results

Figure3.6 Input and Output VSWR Results



m8	m4
freq=2.400GHz	freq=2.500GHz
VSWR1=1.178	VSWR1=1.104



m9	m5	m10
freq=4.800GHz	freq=4.900GHz	freq=5.000GHz
VSWR2=1.337	VSWR2=1.113	VSWR2=1.841

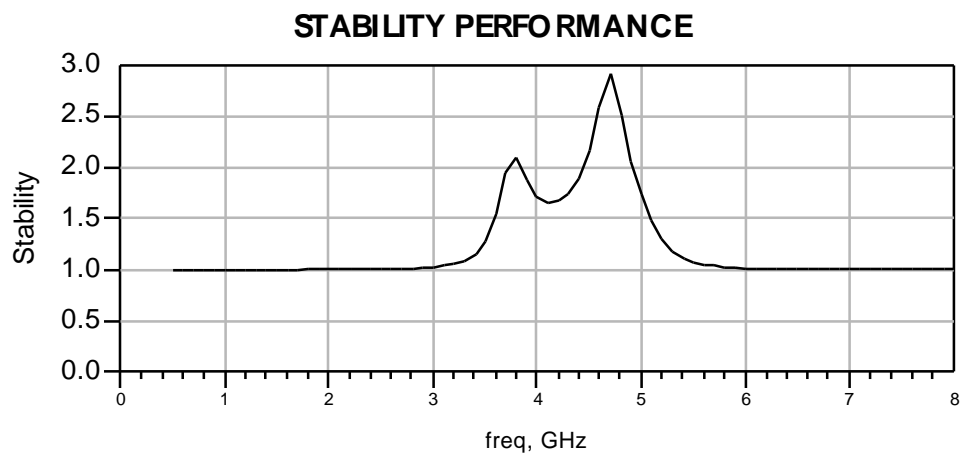


Figure3.7 Stability Performance over extended frequency band.

## 4.0 SCHEMATIC DIAGRAM

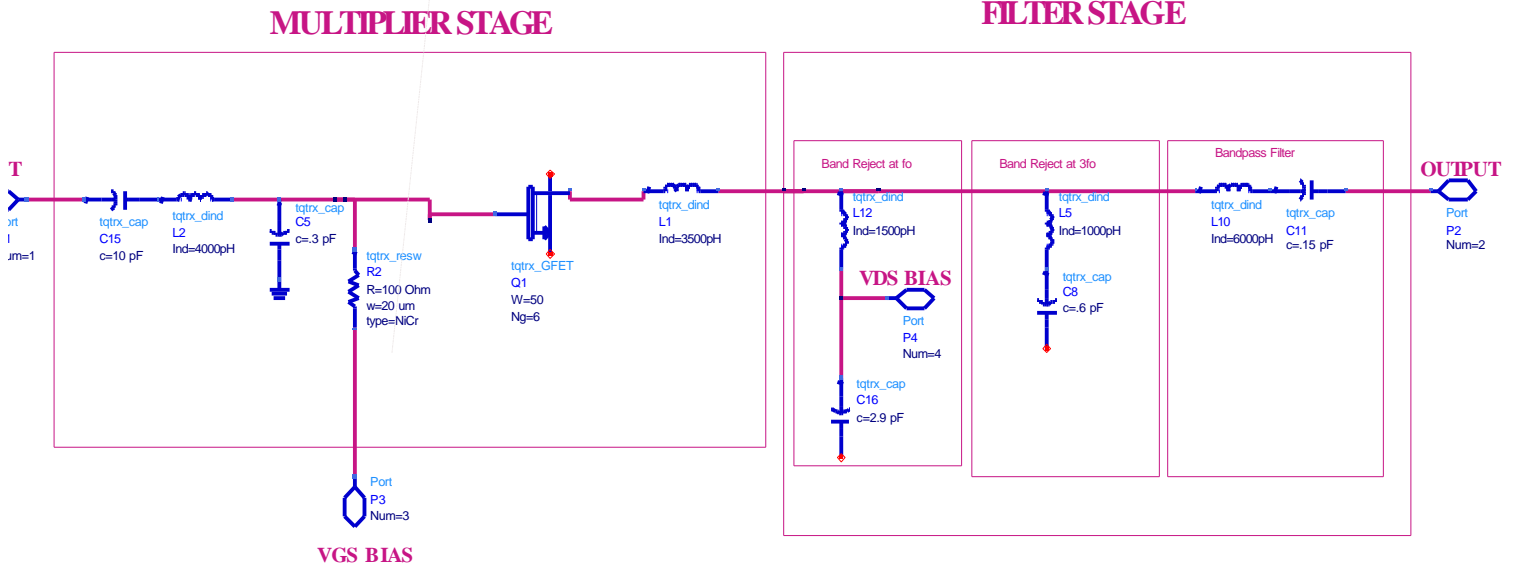


Figure4.1 Simplified Schematic Diagram

## 5.0 DC ANALYSIS

(See Appendix A for simplified DC Schematic)

The +6.5V source applied to the drain measures 22mA of current dc and 8.5mA of ac current and the -1.85V source applied to the gate measures 10uA of current. There is an expected current swing of up to approximately 65mA and a voltage swing of up to 8V with supplied input power of +10dBm. The MIM capacitor breakdown voltage is around 10V and the maximum current carrying capacity for the spiral inductors is 180mA. In addition the NiCr resistors utilized in the resistor divider are 105um in width and are more than capable of handling the current capacity specified at 1mA/um. The interconnections between Metal1 and Metal 2 combined are able to handle 27mA/um of current. The DC lines are 10um.

## 6.0 TEST PLAN

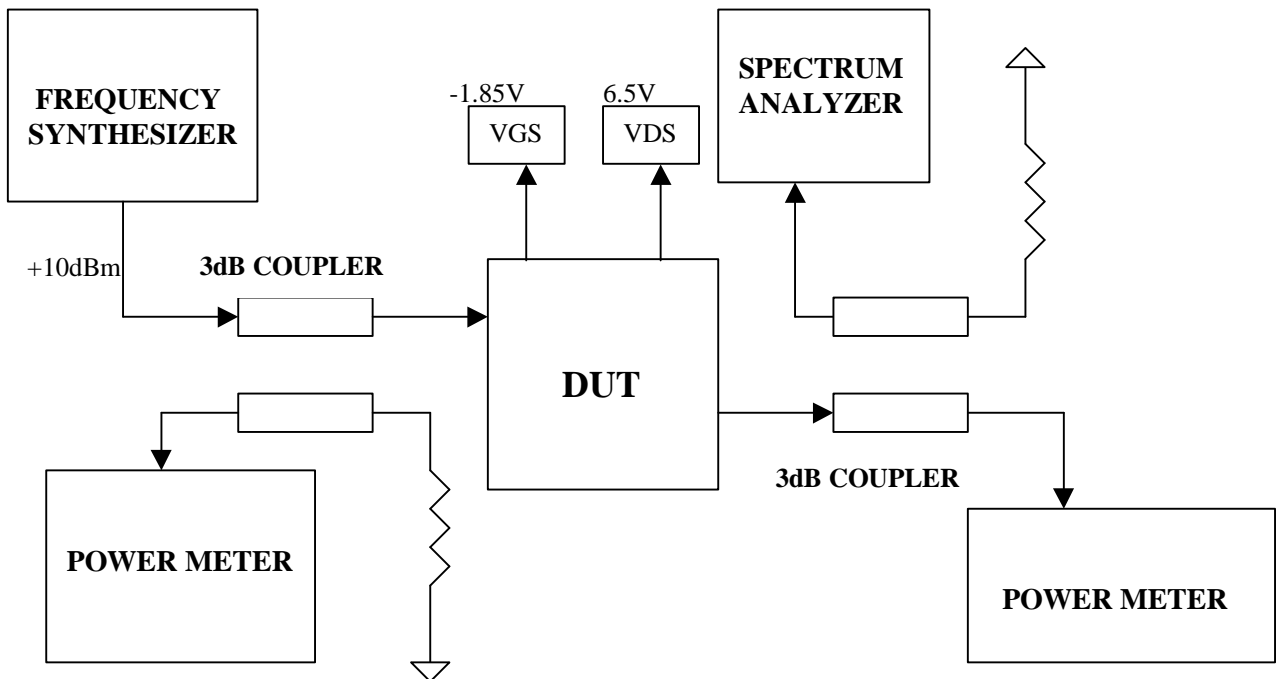


Figure6.1 Abbreviated harmonic test plan.

The above figure illustrates an abbreviated test plan that can measure the harmonic performance of the multiplier circuit. To test the small signal performance of the circuit design a network analyzer can be replaced at the input and output ports of the multiplier.

## **7.0 CONCLUSIONS AND RECOMMENDATIONS**

In conclusion, this multiplier design is very sensitive to the output filter section. Any slight variance in the capacitance within  $\pm 0.01\text{pF}$  the response of the filter is greatly affected. In a second pass design, a better filter section would need to be implemented to decrease sensitivities and losses added to the circuit. In addition, a self-bias scheme could be employed in order to increase available space on chip. In turn, the available space would allow for an output amplifier that would boost the conversion gain at the second harmonic at the required RF input drive.

## APPENDIX A

## APPENDIX B

Multiplier X2 Layout



## REFERENCES

Camargo, E., *Design of FET Frequency Multipliers and Harmonic Oscillators*, Boston, MA: Artech House, 1998.

Maas, S., *Nonlinear Microwave Circuits*, Norwood, MA: Artech House, 1988.

MILLIMETER-WAVE DRIVER  
AMPLIFIER: A MMIC APPROACH

by

Joe Giacinto

A Design Project submitted in fulfillment  
of the requirements for

EE 801

JOHNS HOPKINS UNIVERSITY

May 7, 2000

JOHNS HOPKINS UNIVERSITY

Abstract

MILLIMETER-WAVE DRIVER  
AMPLIFIER: A MMIC APPROACH

by Joe Giacinto

Professor:

John Penn  
Applied Physics Laboratory

To fulfill the objectives of EE801, “Independent Study: Topics in Electrical Engineering”, a design project consisting of a MMIC millimeter-wave amplifier was selected. At the onset of this investigation, a broadband device with useable gain, noise figure and output power across 20-40 GHz was desired. Such a device would find extensive applications in the emerging LMDS (Local-Multipoint-Distribution Service) market as a driver amplifier in portions of the microwave spectrum recently made available by the FCC. Also, such a device would find use in tactical systems such as airborne radars, spacecraft communications/surveillance payloads or electronic counter-measures, where size is at a premium.

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## ACKNOWLEDGMENTS

The author wishes to thank his EE787, EE788 classmates for providing valuable criticism and comments. He also wishes to thank Agilent Technologies (formerly HP) for providing access to the Series IV design software at the Kossiakoff Center. Triquint Semiconductor is to be commended for continued support of student projects.

## *Introduction*

### **Circuit Description**

Amplifiers find applications in most any type of microwave receiving or transmitting system. The process of signal amplification is basic to the task of signal detection or transmission. With the recent availability of millimeter-wave spectrum, commercial providers of broad-band services are in need of low-cost, highly integrated devices for use in next generation cellular products and information appliances. At the present time, there is dearth of broad-band gain blocks covering the 20-40 GHz band. Moreover, much of the presently available devices are large, discrete-based designs rather than smaller MMICs. As fabrication techniques have matured, the possibility of millimeter-wave MMIC amplifiers has become feasible. For this design, P-HEMT devices realized in Gallium Arsenide are utilized as the gain elements. P-HEMT devices, by the nature of their pseudomorphic junctions, tend to operate at very high frequencies and exhibit exceptionally low noise figure.

A balanced amplifier architecture was used for this design. Early in the investigation, it was found that a single FET amplifier would not exhibit much useable gain over an octave band, much less a sub-octave. The balanced configuration permits the use of more than one device and provides for some phase cancellation of device mis-match. However, these come at the price of higher loss at the front end, compromising noise figure. Lange couplers are used as the combining elements, as they can be reasonably realized in monolithic form at 30 GHz. The balanced amplifier consists of two stages, each using 8x50 um P-HEMTS power-combined, for a total of four transistors. A linear model fit to swept data was provided by the device manufacturer. A proprietary non-linear Materka model based on extracted device parameters was also provided to

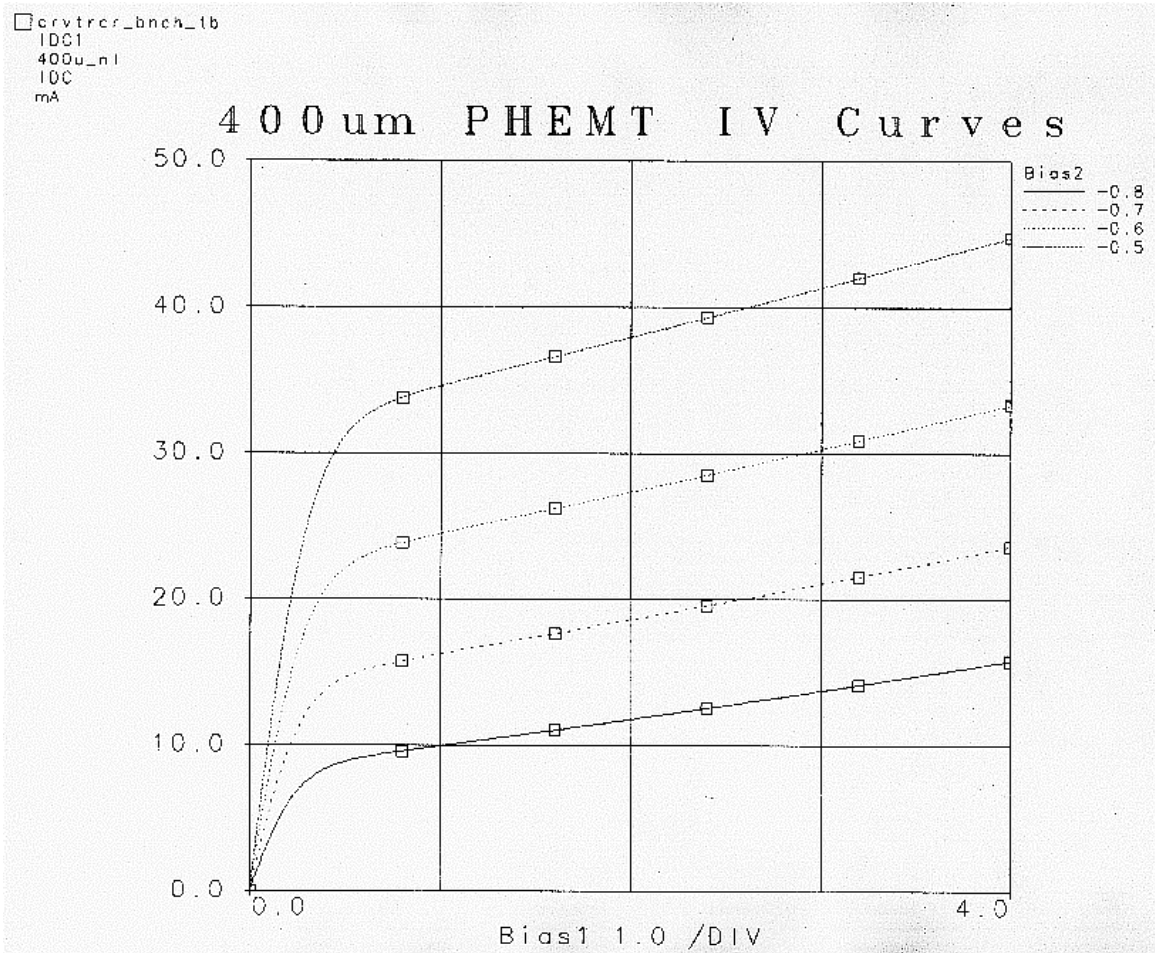
generate IV curves, output power, third and second order intercept and power-added efficiency simulations. Each device is biased identically, though provision is made in the design to independently adjust the biases during laboratory tests. The drain bias lines of each device also serve as part of the output matching network. The output match consists of a high-impedance open stub and a low impedance series-connected transmission line. The input matching network consists of shunt capacitor and low-impedance transmission line. Gate bias-tees are realized as conventional quarter-wave structures with large bypass capacitors. At these high frequencies, distributed matching techniques do not consume as much circuit real estate, moreover, the utility of purely lumped element matching techniques becomes minimal beyond 20 GHz.

### **Design Philosophy**

At the onset, several possible device architectures were explored. A feedback amplifier and a two-stage design were analyzed. The feedback design exhibited minimal gain and poor noise figure. Also, it was not readily apparent how to realize the series inductor-capacitor-resistor (at these frequencies) required to couple signal energy from output to input. This approach was quickly abandoned for the simpler two-stage design. Unfortunately, this design was unable to achieve broad-band performance. Both designs were made to be unconditionally stable from 1 GHz to beyond 40 GHz using a parallel resistor-capacitor combination at the device input. MU and K parameters were both simulated. A low value shunt capacitor at the transistor gate was found to make the input matching network design far more tractable and aided in stability. Both designs made use of “noise circle” and “gain circle” design techniques. The input matching networks were designed to present the transistor gates with the optimum reflection coefficient for low-noise operation. Due to the stability of the devices, a simple conjugate match was used as the basis of the output matching network design.

Of the two designs, the two-stage design yielded the most promise. In order to broad-band the gain, a “high-low” design approach was pursued. Noise circles and conjugate matching techniques tend to work well over narrow-bandwidths. At bandwidths approaching an octave, variation in the input and output impedance of most solid-state devices makes this design methodology more difficult to apply. However, the use of two stages permits some flexibility. The “high-low” approach involved designing and tuning the first stage at a low frequency (the low end of the band), using the familiar noise circle/conjugate matching techniques. The same procedure is applied to the second stage, only for the higher end of the band. Both stages are then cascaded, yielding a double-tuned response. However, both devices are matched well to  $50 \Omega$  over only a subset of the desired band. The trick is to have the second stage response to complement the first stage response to provide gain equalization. Inter-stage Matching networks are then tuned to “de-Q” the double-tuned response and achieve gain flatness across the band. One of the target goals for this design was a noise figure 3 dB or less, with a linear gain greater than 10 dB. Also, a saturated output power of approximately 15-20 dBm was desired. These initial specifications provided the basis for bias point selection. Data provided by the manufacturer and simulation of designs based on slightly different bias points quickly narrowed down the possibilities. In order to best meet the aforementioned specifications, a gate bias of  $-0.6 \text{ V}$  with the drain at  $3 \text{ V}$  was selected. Measured data from the manufacturer indicated this would yield a drain current of  $\sim 20 \text{ mA}$ , which was low enough to keep the noise figure from growing too large, yet high enough to anticipate a reasonable amount of output power. Noise figure is a strong function of device bias. High levels of current are indicative of many charge carriers. The more carriers, the larger the noise process and subsequent increase in device noise figure. Simulations carried out with the provided Materka models yielded a slightly higher current than the manufacturer’s data indicated. The models were initially for a  $600 \mu\text{m}$  device, however the area



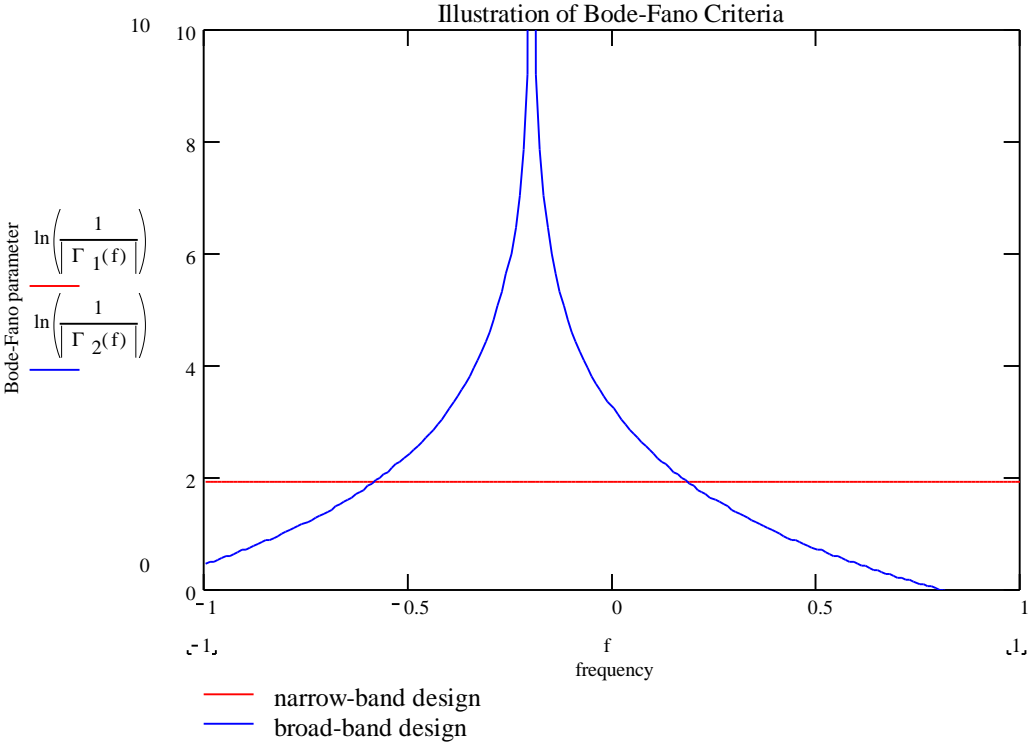


parameter was scaled to represent a 400um transistor. The final design will have provision for independent bias adjustments, so this discrepancy can be addressed during device measurement and test.

**Trade-Offs**

Early in the design, compromises had to be made. It became apparent that achieving a full octave bandwidth (20-40 GHz) was going to be very difficult with the chosen two-stage design. Another architecture, such as a distributed amplifier may have been explored to achieve the desired full octave performance, but distributed amplifier designs tend to have other undesirable characteristics such as low gain and high noise figure. Judicious tuning and adjustment of inter-stage matching networks ultimately yielded a design exhibiting 13 dB gain ( $\pm 1$  dB) from

25 to 33 GHz. The 3 dB bandwidth of the device extends from 24 to 34 GHz. Noise figure is less than 4 dB across this band. In effect, noise figure and gain were traded-off for improved broad-band performance. The well known Bode-Fano criteria supports this observation, whereas there is a limit to the extent at which a matching network can be improved. In essence, a nearly “perfect” match can be obtained at a single frequency, however, examination of the Bode-Fano parameter shows that this may not be the most efficient way of achieving a broad-band match. By trading off reflection coefficient magnitude over bandwidth, a better match may be achieved over a broader band, yet it will be less than the “nearly” perfect match over a narrow-band. The areas bounded by the two integrals are equal, yet in the case of the broad-band amplifier, the input reflection coefficient is higher.



Another target goal for the design was creating a device which would fit in a 60x100mil chip area. As the design progressed, the two-stage design morphed into a balanced configuration using two Lange couplers. Each “stage” then became the double-tuned, “high-low”, two-stage design. A six-section Lange gave better broad-band performance, yet introduced excessive insertion loss which compromised noise figure. In the end, a four-section Lange coupler centered at 30 GHz yielded satisfactory performance. The progression to a balanced design quickly consumed the available real estate. Instead of two 400um devices, the design now had four, with four biasing networks instead of two. However, since the performance of the amplifier dramatically improved, it was agreed to allow the design to grow. In its final rendition, the design will most likely be fabricated on a 120x150mil size chip.

*Modeled Performance*

**Specifications**

The following target specifications were used in design of the MMIC amplifier. Simulated performance numbers are also listed.

<b><u>MMIC AMPLIFIER SPECIFICATION MATRIX</u></b>		
Frequency: 20-40 GHz		
Desired Size: 60x60 mil		
<u>PARAMETER</u>	<u>TARGET GOAL</u>	<u>POST-LAYOUT SIMULATION</u>
GAIN	15 dB (10 dB min)	*24-34 GHz 3 dB BW  11 dB at band edges  14 dB at 30 GHz
NOISE FIGURE	2 dB (3 dB max)	*24-34 GHz  4 dB
RETURN LOSS (INPUT/OUTPUT)	15 dB (10 dB min)	*25-36 GHz  >10 dB
SATURATED OUTPUT POWER	20 dBm (15 dBm min)	*24-34 GHz  20 dBm

Additional parameters not specified, but also simulated, are included for reference.

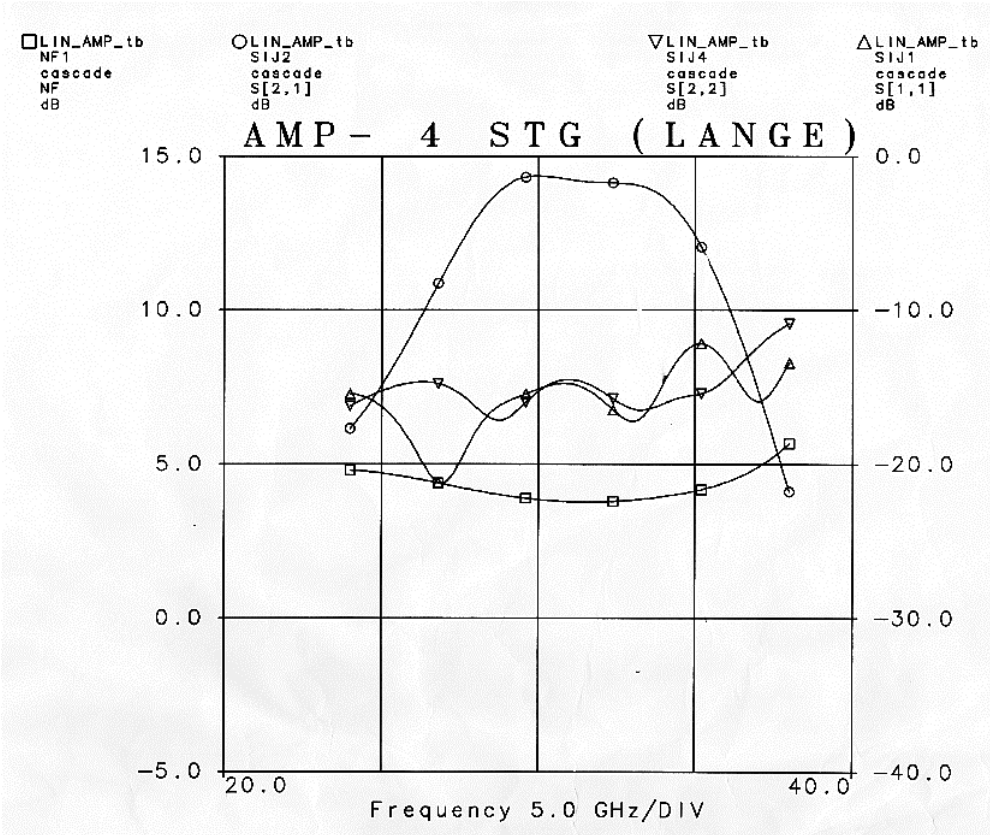
<b><u>ADDITIONAL SIMULATED PARAMETERS</u></b>	
<u>PARAMETER</u>	<u>POST-LAYOUT SIMULATION</u>
Third-Order Intercept Point	
Second-Order Intercept Point	
Power-Added Efficiency	18.6%

**Predicted Performance**

As has been already stated, several different implementations were explored. Each approach had its merits, yet an optimal solution to all initial specifications proved difficult. A balanced amplifier design proved to yield the best performance compromise. Linear S-parameter simulations were conducted using a linear model fit to measured device data. Harmonic balance non-linear simulations using a scaled version of the 600um Materka model were also performed.

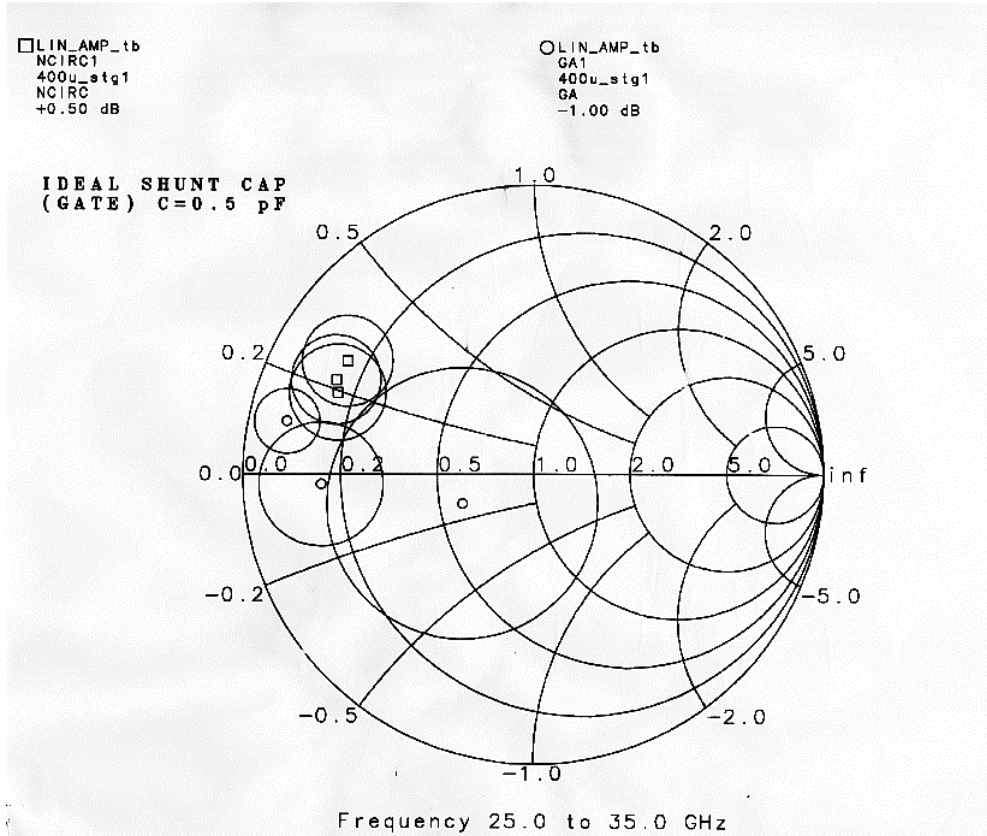
Prior to layout, the design was optimized using ideal elements. Performance of this virtual “proto-type” was satisfactory. In particular, the bandwidth was narrower than the design goal and the noise figure was slightly higher. Return loss was within specification. At these frequencies of operation, there is some uncertainty as to the accuracy of the Series IV models for transmission lines and interconnects between components. Parasitics have a much more pronounced effect on circuit performance as frequency increases. In particular, a low-value

shunt capacitor was used at the transistor gate to move the noise-match points closer to the real axis. Doing this allowed a  $50\ \Omega$  match to be obtained by simply using a length of low-impedance transmission line. This suggestion was provided by Craig Moore to John Penn. However, there was concern that the low value capacitance would be shifted in value due to the metal interconnects introducing

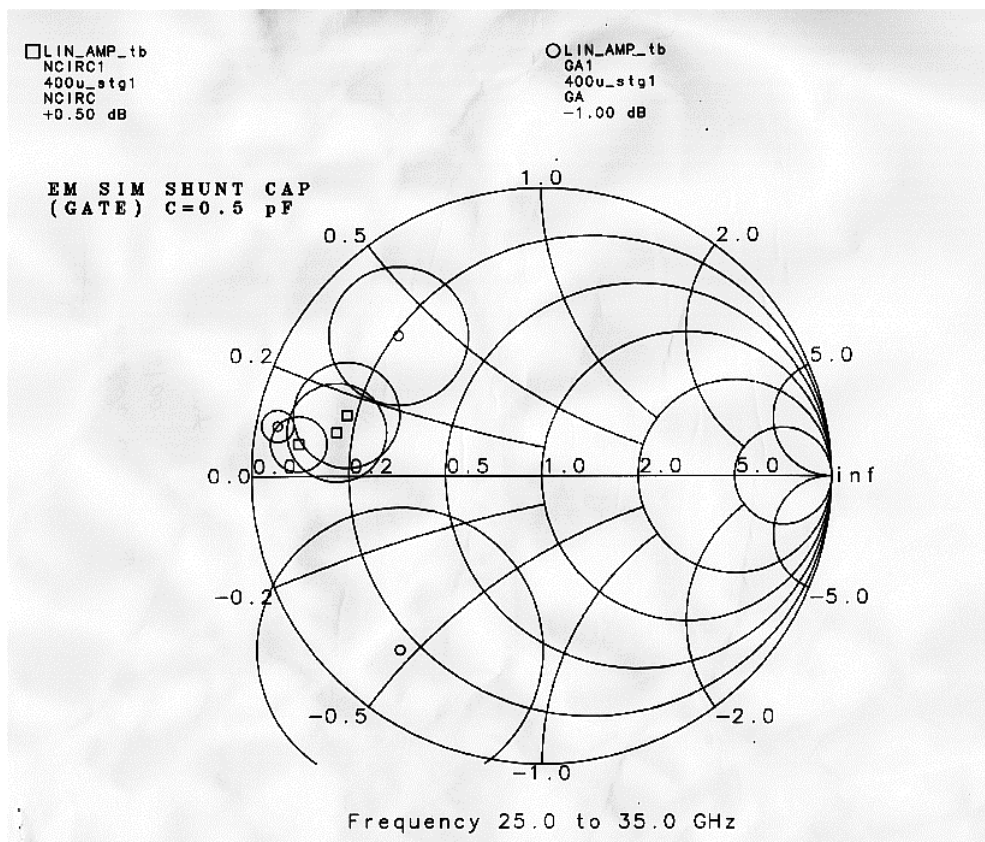


additional reactances at these high frequencies.

In order to perform a sanity check on the simulations, John Penn provided S-parameter data of a physics-based full-electromagnetic simulation of the planar capacitor structure, for 0.33 and 0.5 pF capacitors. The ideal capacitors were removed from the simulation with the two-port data from the EM simulation as substitute. The ideal simulation predicted a shunt capacitance of 0.5 pF.

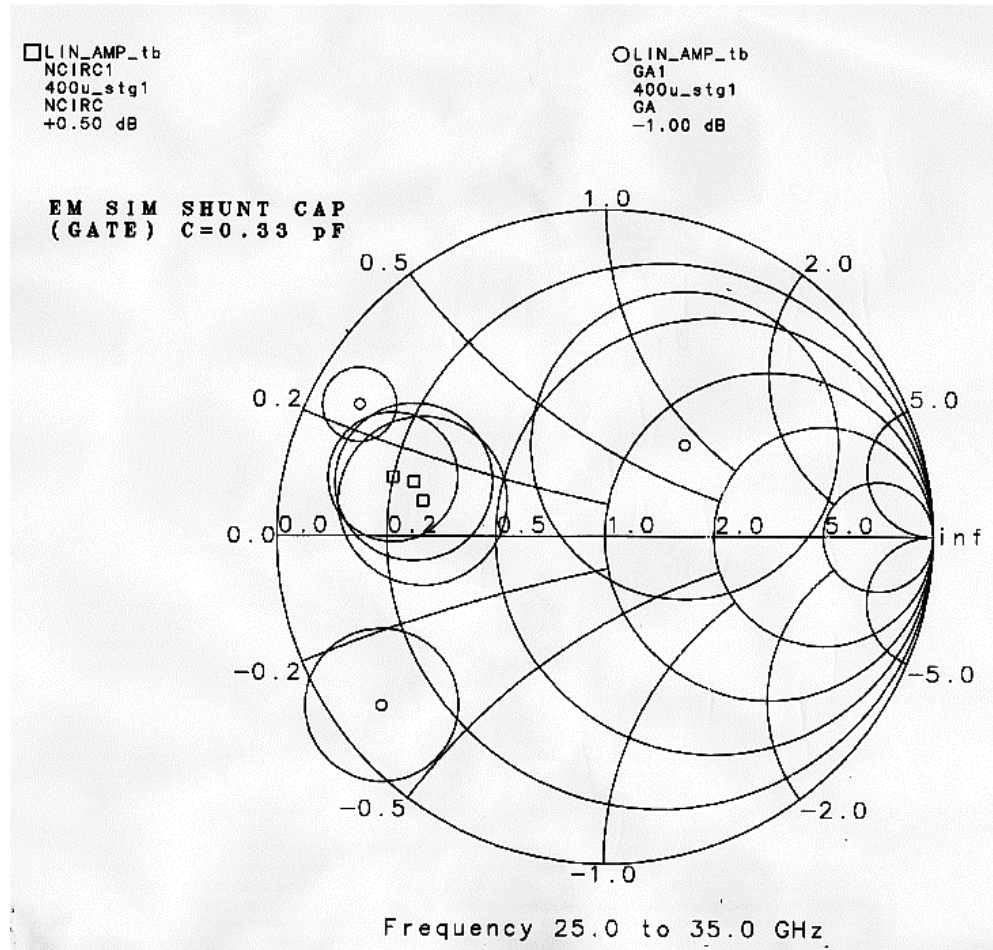


The simulation using the EM-physics based data is markedly different from the ideal circuit simulation. It appears that the 0.5 pF capacitor is a bit too high in value. The primary impact on the amplifier performance was the introduction of a severe low-pass response which down-shifted the high-end frequency response by roughly 5 GHz. Another simulation using a 0.33-pF capacitor (EM data) shows better agreement



The 0.33-pF capacitor was ultimately used in the design. Provisions were made in the capacitor implementation to allow for a modest level of tuning. A “tuneable” capacitor using conductive epoxy to adjust capacitor cells was envisioned.

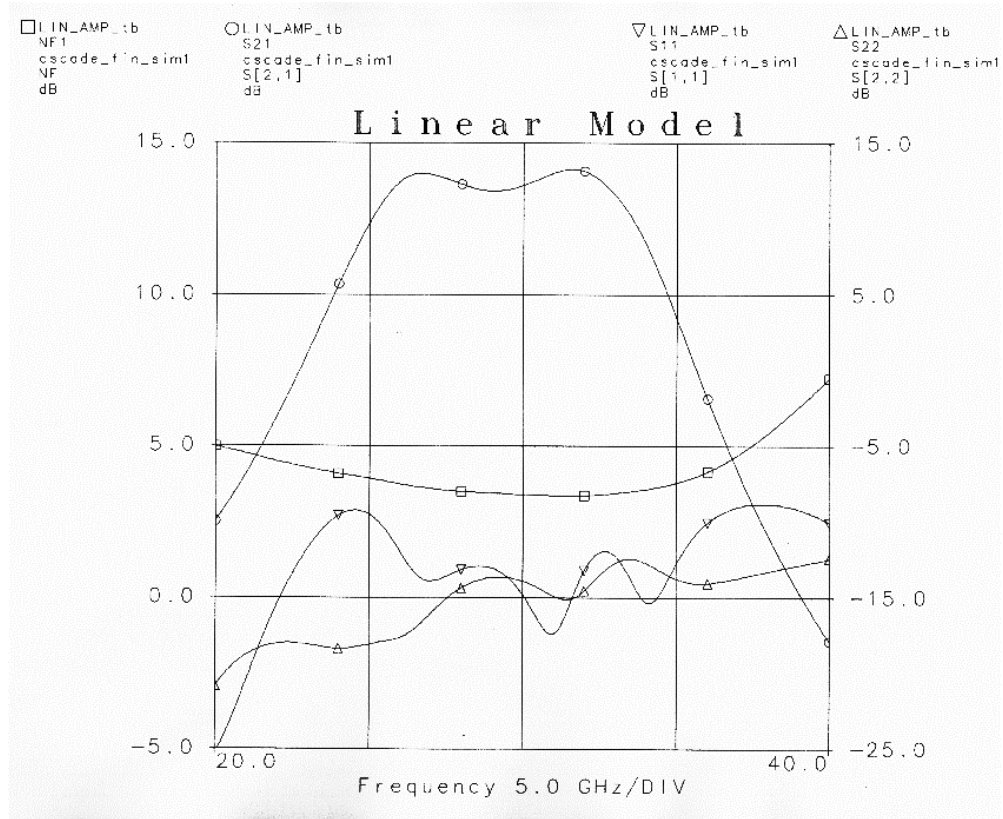




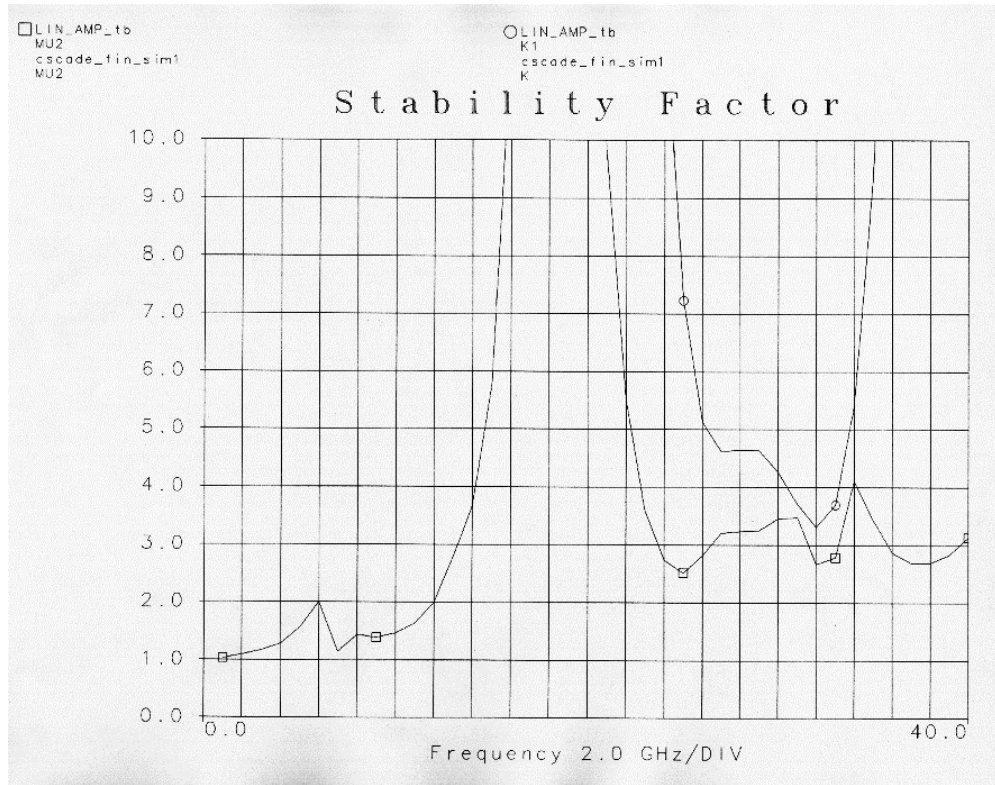
This will allow some amount of post-production tuning, should there be any shift in the actual capacitance.

With the input capacitor issue resolved, the design tasks focused on the tuning of inter-stage matching networks to recover bandwidth. Gain was simulated using the linear model and the non-linear Materka model under small-signal conditions. The first iteration of the balanced amplifier utilized a drain biasing network separate from the output matching network. An attempt was made to combine the drain bias and output matching network to save chip real estate. The final revision of the design utilized the drain bias lines to provide the shunt inductor

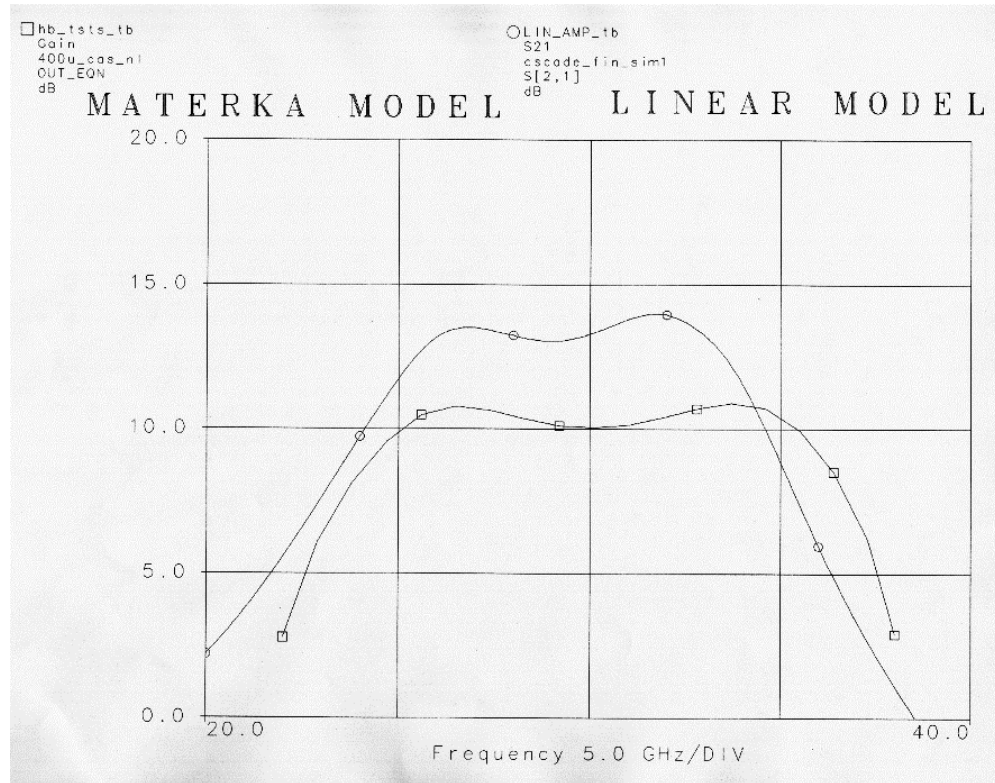
required in the output matching network. Only minor tuning was required to recover the device performance.



Gain and noise figure are both close to the original design specifications, though there is little margin.

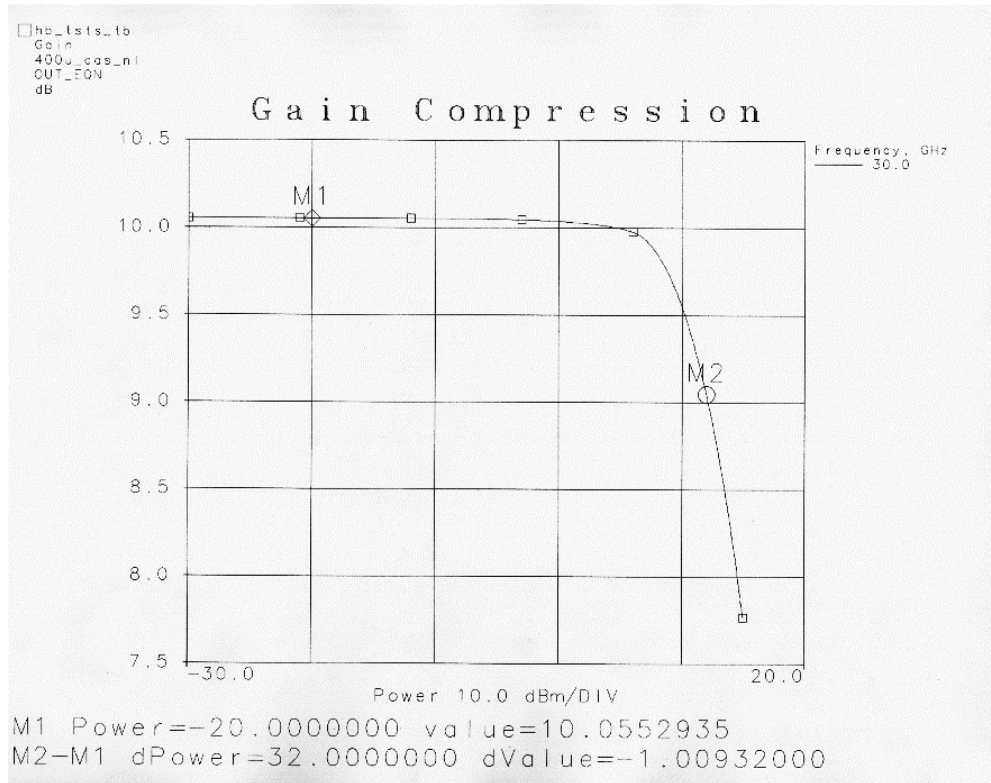


Stability was also checked for each stage and the completed amplifier. The design is unconditionally stable from 1-40 GHz.

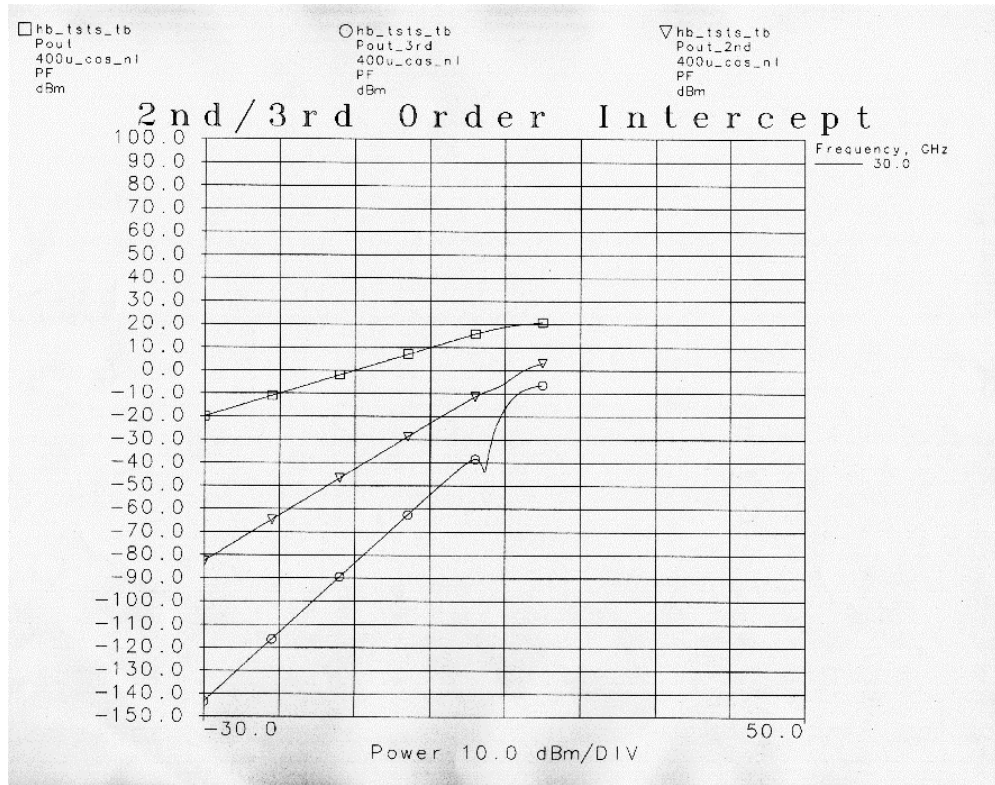


A “manual” equation for gain was written in the Series IV harmonic-balance test bench to simulate small-signal gain using the Materka model. Input power was set to  $-20$  dBm to ensure small signal conditions. The basic form of the gain response agree between the two simulations, however the Materka model predicts 3-4 dB less gain.

One-dB compression point was also simulated using the non-linear model and harmonic balance test bench. The one-dB compression point is  $+12$  dBm, with 9 dB of gain, for an output power of  $+21$  dBm at 1 dB gain compression. These numbers exceed the original specifications.



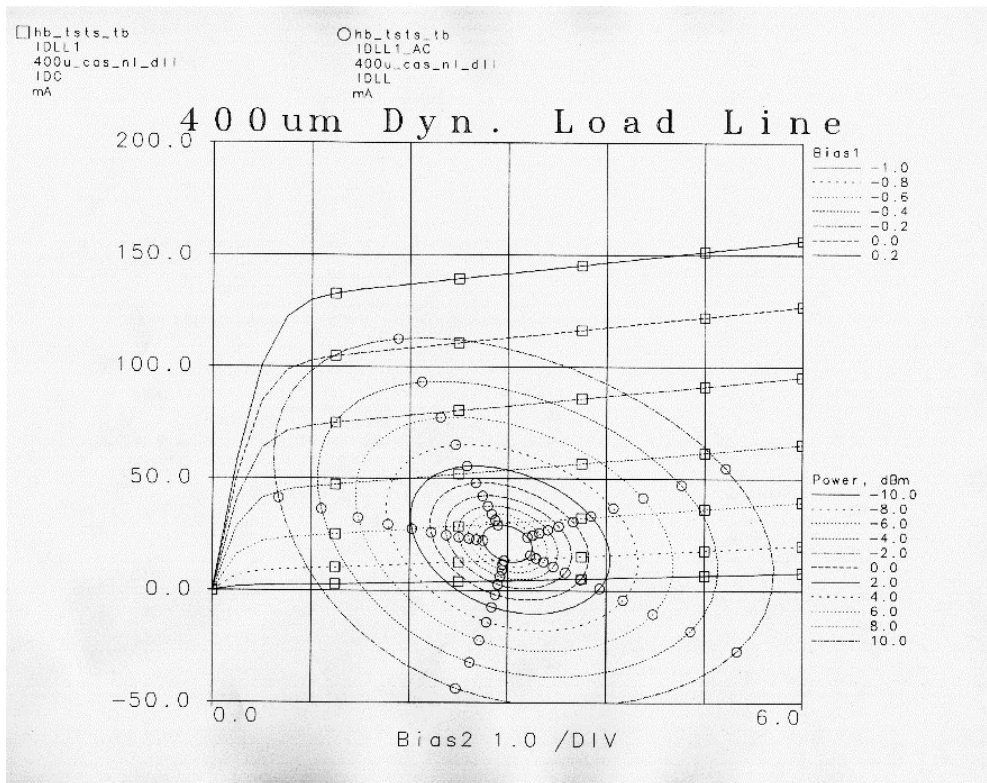
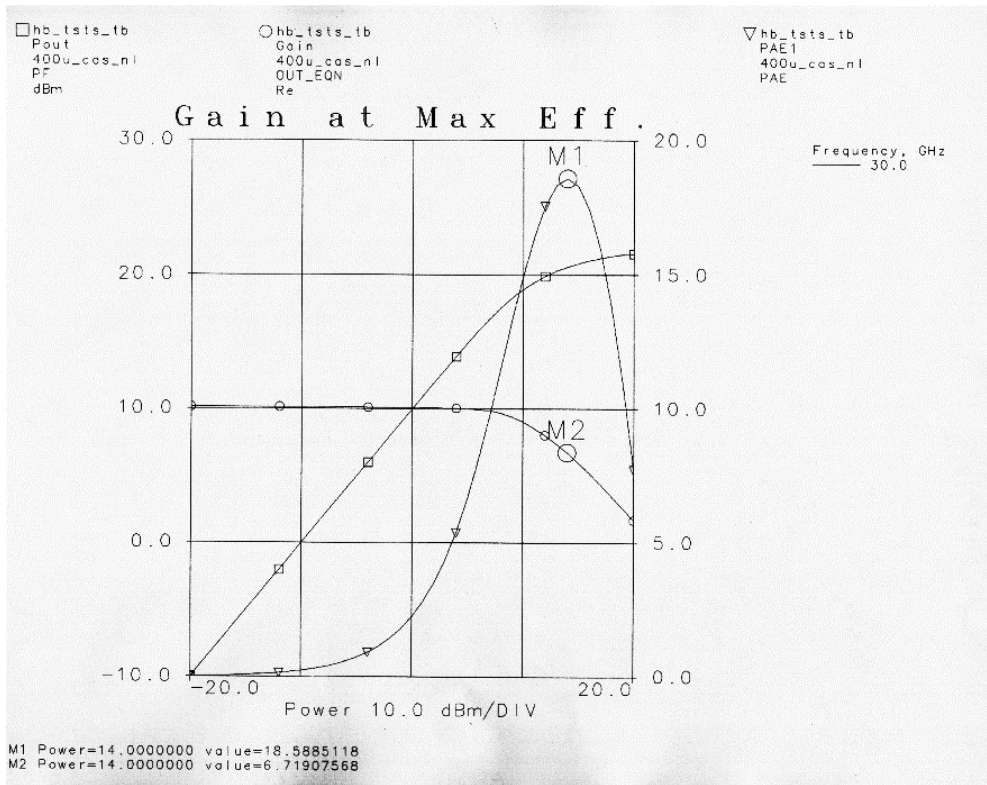
Additional parameters were also simulated to fully characterize the amplifier. Plots are included of: 1. 2<sup>nd</sup>/3<sup>rd</sup> order gain slopes (to calculate 2<sup>nd</sup> and third order intercept points), 2. PAE (power-added efficiency, and 3. Dynamic Drain Current Load Line (single transistor, part of output stage).



Extrapolation of the third and second order slopes yield a second order output intercept point of + dBm and a third order output intercept point of + dBm, respectively.

### Probed Response

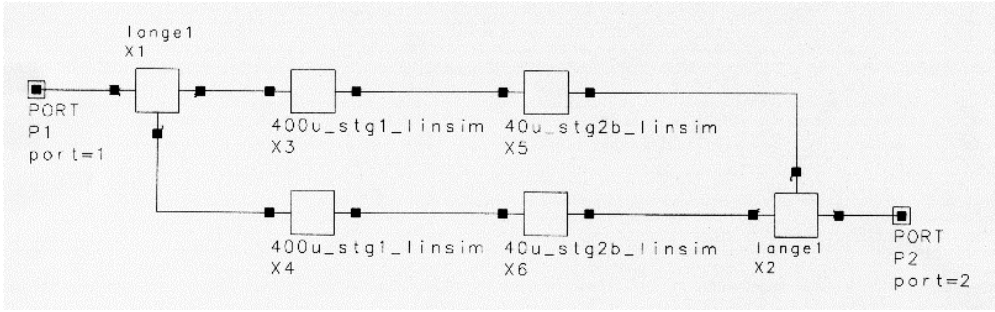
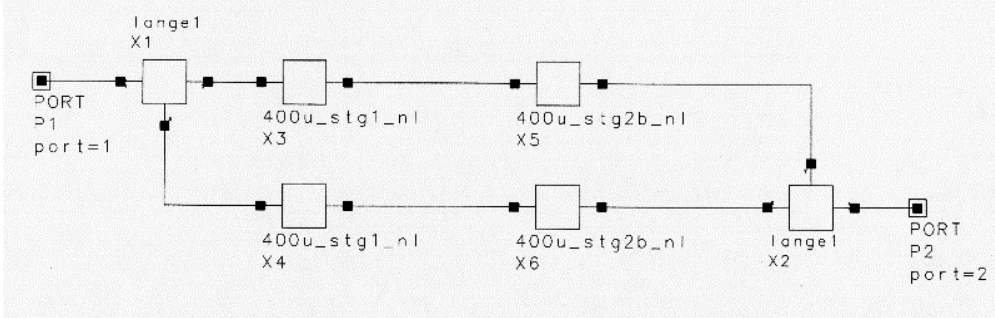
TO BE ADDED AFTER CHIPS ARE MEASURED IN WINTER OF 2001.







**Final Electrical Schematic**



\*Schematics for each individual sub-circuit are attached separately for brevity

**DC Schematic**

## DC Analysis

### Component Current Stress

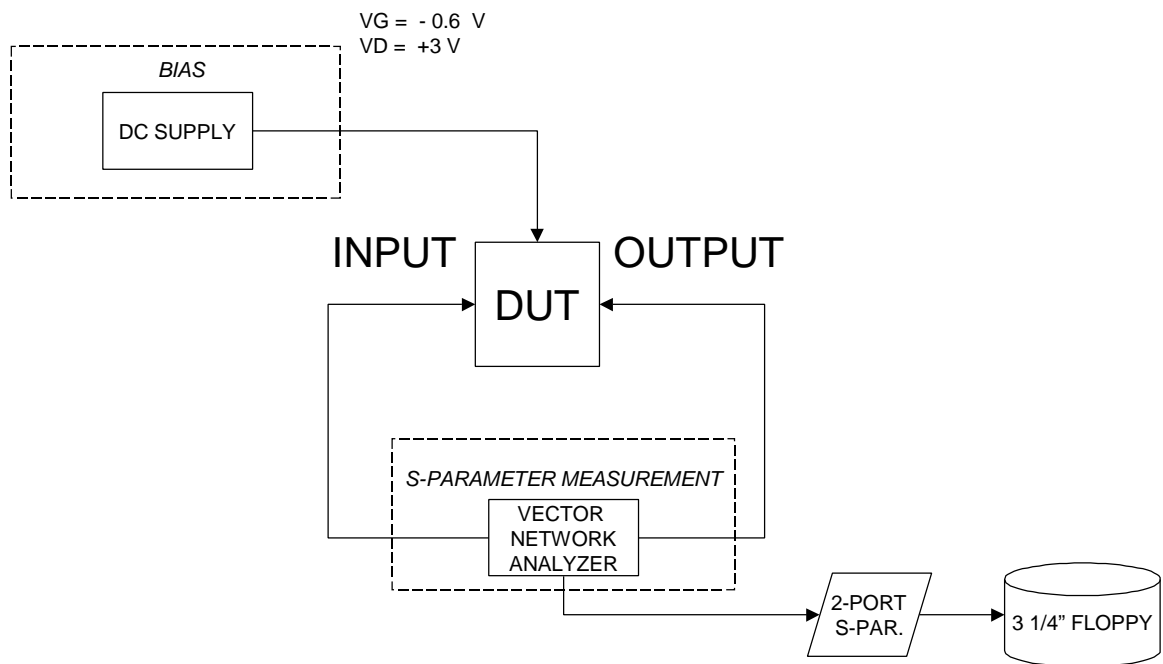
One of the chief causes of device failure in MMICs is mis-applied DC bias, or incorrectly designed bias networks.. Oversight in the design of the bias network can lead to currents that may exceed the handling capability of metal interconnect traces or the rating of bias resistors. Thin, purposefully inductive bias lines may not be able to carry the required DC current. Currents in specific bias branches, trace width, and device technology where analyzed to determine if any bias currents exceeded the ratings of the MMIC structure.

<b><u>DC BIAS CHECK</u></b>			
<b>BIAS POINT</b>	<b>CURRENT/ VOLTAGE</b>	<b>MINIMUM LINE WIDTH</b>	<b>RESISTOR SIZE/TYPE</b>
GATE –INPUT & OUTPUT STAGES	minimal current/ -0.6 V	10 $\mu\text{m}$	N/A
DRAIN – INPUT & OUTPUT STAGES	20 mA/ 3V	25 $\mu\text{m}$	N/A

10  $\mu\text{m}$  wide line (interconnect) can handle up to 180 mA. Currents are well within the capabilities of chosen device technology.

**Equipment Diagram**

**TEST SETUP - S-PARAMETER MEASUREMENT**

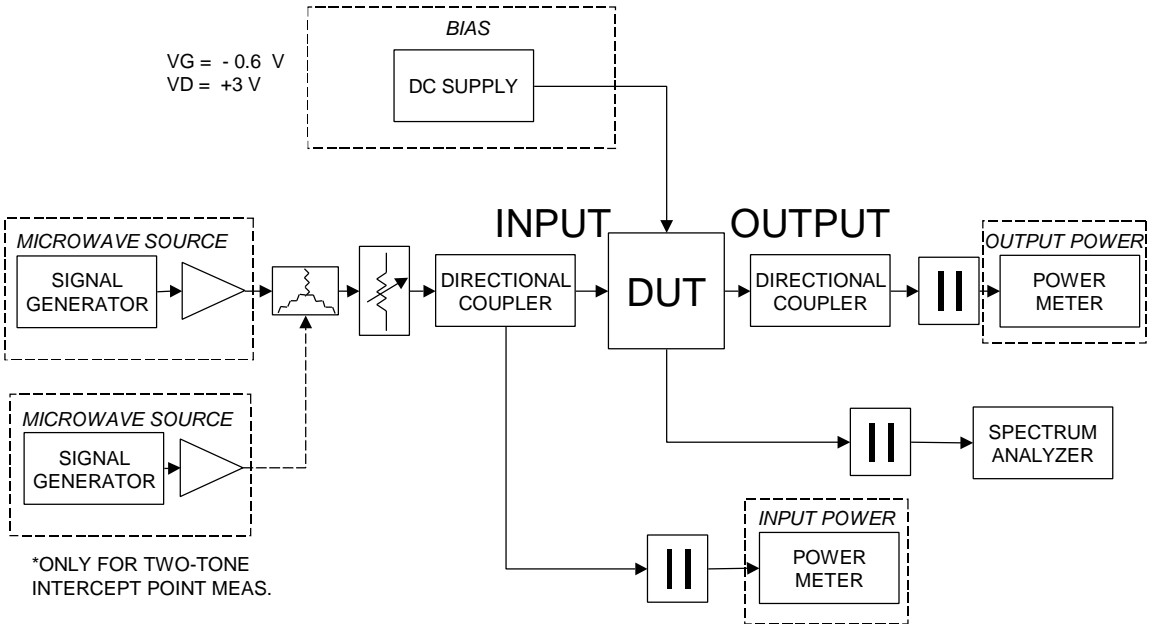


This test set will be used to obtain two-port S-parameter data for the amplifier. The data will be written to a floppy in a magnitude/phase format. Hard copy plots can be immediately generated in log-magnitude format; to get immediate results for gain, in/output return loss and isolation, however, the S-parameters on disk will allow computation of other parameters, such as stability. Since the amplifier operates roughly from 25 to 35 GHz, appropriate low-loss coaxial cables should be used for all RF interconnects. All connector interfaces should be cleaned with alcohol or another suitable solvent to remove any fine particles

that would corrupt the measured response. At these high frequencies, such special care is mandatory. Prior to making measurements, All instruments must be calibrated and cable losses accounted for.

In order to measure device output power (under large signal conditions) and third order intercept point, a different test set is required (shown below). The same general precautions should be followed when assembling and calibrating the equipment.

**TEST SETUP - LG. SIG. OUPUT POWER  
INTERCEPT POINTS**



**REQUIRED TEST EQUIPMENT**

**\*ALL MICROWAVE INSTRUMENTS MUST PROVIDE 20-40 GHz COVERAGE**

<b>INSTRUMENT/DEVICE</b>	<b>QUANTITY</b>
Quad-output DC Lab supply	1
Microwave Signal Generator	2
Power Amplifier (+20 dBm Pout)	1
Microwave Spectrum Analyzer	1
Adequate supply of low-loss coaxial test cable and connectors	N/A
Wafer probe station, microwave probes, needle probes for biasing	1 station
Microwave Power Meter	2
Directional Bridge	1
Directional Coupler	2
Microwave Step Attenuator	1
Microwave Vector Analyzer or Eqv.	1

### **Biasing Procedure**

1. Connect all test equipment per the attached test setup diagram.
2. Mount the mixer MMIC in the probe station test fixture
3. Set power supply to  $-0.6$  V, and  $+3$  V. Set the current limit to 150 mA.
4. Using needle probes, apply  $-0.6$  V GATE voltage FIRST, then apply 3 V DRAIN bias.

### **S-Parameter Measurement Procedure**

1. Set the network analyzer to provide  $-20$  dBm output power; this will ensure the amplifier is operating under small signal conditions.
2. Calibrate the network analyzer for a full two-port measurement. Set the start frequency to 20GHz, the stop frequency to 40 GHz and number of sweep point to 801. Connect device as shown in first test diagram, note current draw on power supply.
3. Generate hardcopy plots of all four S-parameters using a "log-magnitude" format. Save softcopies of the S-parameters to disk using a complex "magnitude-angle" format.

### **Output Power Measurement Procedure**

1. Do NOT hook up RF power to the DUT yet! Set the microwave source to provide a single tone at 30 GHz. The output power of the source/amplifier combination should be about  $+20$  dBm.
2. Using the step attenuator and noting the coupling ration of the directional coupler, measure 0 dBm at the output of the step attenuator.

3. Connect the DUT input as shown in the diagram. Note the output spectrum and power level. Step the input power in one dB steps using the step attenuator, up to +15 dBm input power (measured in the input coupler). Note the output power and point where signal gain decreases by one dB (one dB compression point). Note current draw on power supply.

### **Two-Tone Third-Order Intercept Point**

1. Connect all test equipment as shown in the second test diagram. Using the step attenuator and power meter, ensure the RF power does not exceed –20 dBm. Set microwave source #1 to 30.1 GHz. Set microwave source #2 to 29.9 GHz.
2. Note the noise figure and third-order intercept points of the spectrum analyzer. It may be necessary to use a buffer amplifier or adjust the spectrum analyzer resolution bandwidth. The spectrum analyzer should have an intercept point at least 20 dB higher than the DUT so that accurate measurements can be made.
3. Set the spectrum analyzer to a center frequency of 30 GHz. Two tones should be visible, plus the third-order product side-bands: (2 X input tone #1)-(tone #2) and (2 X input tone #2)-(tone #1). Set the bandwidth to 500 MHz.
4. Step the input power in 1dB steps until the side-bands are 5-10 dB above the noise floor of the spectrum analyzer. Generate a hardcopy plot that shows all four tones. If possible, use markers to note the delta from the main tones to the third-order side-bands.
5. Use the following formula to compute the third-order intercept point:

$$IP3 = \text{input signal level} + (\Delta \text{difference between desired and side-band})/2$$

<b><u>MMIC AMPLIFIER COMPLIANCE TEST MATRIX</u></b>	
<b>PARAMETER</b>	<b>TEST</b>
2-Port S-Parameters	X
1 dB Compression Point/Saturated Output Power	X
Input Two-Tone third order intercept point	X



## *C o n c l u s i o n s*

### **Findings**

A millimeter-wave, monolithic, balanced amplifier has been designed and simulated. At millimeter-wave frequencies, different techniques are used in the design of monolithic microwave components. Physics-based EM simulations of circuit structures (in particular, shunt-connected capacitors) proved to be an important tool in performing investigative predictions of the device performance. For example, the EM simulations have shown circuit parasitics to be a limiting factor in component sizing. As a result of these analyses, provisions will be made in the final design to “tune” critical capacitor values. Since the amplifier design was at such a high frequency, distributed techniques were used throughout the design. This differed from my previous experience designing MMICs at lower frequencies, where lumped techniques are solely used due the size limitations at lower microwave frequencies. Linear and non-linear methods were employed to simulate device performance. Amplifier-specific parameters that were simulated included small signal gain, return loss, large signal gain, saturated output power, noise figure, stability, power-added efficiency and second/third order intercept points. Experience was gained designing MMICs using a pHEMT process. It is hoped the experience gained will benefit other students hoping to use the pHEMT proces in future courses..

Early in the design, a feedback and simple two-stage design were explored. Unfortunately, both designs failed in satisfactorily meeting the original device specifications. Late in the design process, a balanced configuration was pursued. This design came closest in meeting the original specifications. Biasing of the amplifier was kept very simple, with gate and drain bias being applied directly. Techniques such as self biasing were not pursued, as experience with the pHEMT process was limited. Direct biasing of the gates and drains will allow

more flexibility during device test. Overall, this has proven to be a very interesting project. New design techniques for use in designing millimeter-wave monolithic microwave components were used. I gained very valuable experience and insights into the challenges of designing monolithic components at millimeter-wave frequencies.

### **Recommendations**

In future iterations of this design, it would prove interesting to expend more effort in completely EM simulating the entire circuit structure. For this design, due to limited time, only critical components of the amplifier were EM simulated. Each key sub-circuit could be simulated using a physics-based EM simulator, such as SONNET, Agilent Technology's MOMENTUM, or HFSS. Unfortunately, these simulations can take excessive amounts of time and require fast workstations. The disparities between the ideal circuit models and the EM simulations at millimeter-wave frequencies should tend to drive designers to use more EM simulations as they pursue designs at higher frequencies.

Another area that demands some attention is the phenomena of "odd-mode" circuit oscillations. As was learned in EE788, K and MU factor analysis that is based on linear device parameters ( $Z$  or  $S$ -parameters) fails to reveal this condition. It is most often a problem in design using two or more active devices in a combiner arrangement (such as this balanced amplifier). Direct computation of the circuit eigenvalues as mentioned in Freitag's 1992 MTT conference paper is possible, however, a simpler approach using time-domain simulation has been put forward by Dale Dawson (EE788 class notes). Unfortunately, a transient simulator was not available at the time of this project to pursue this further.

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