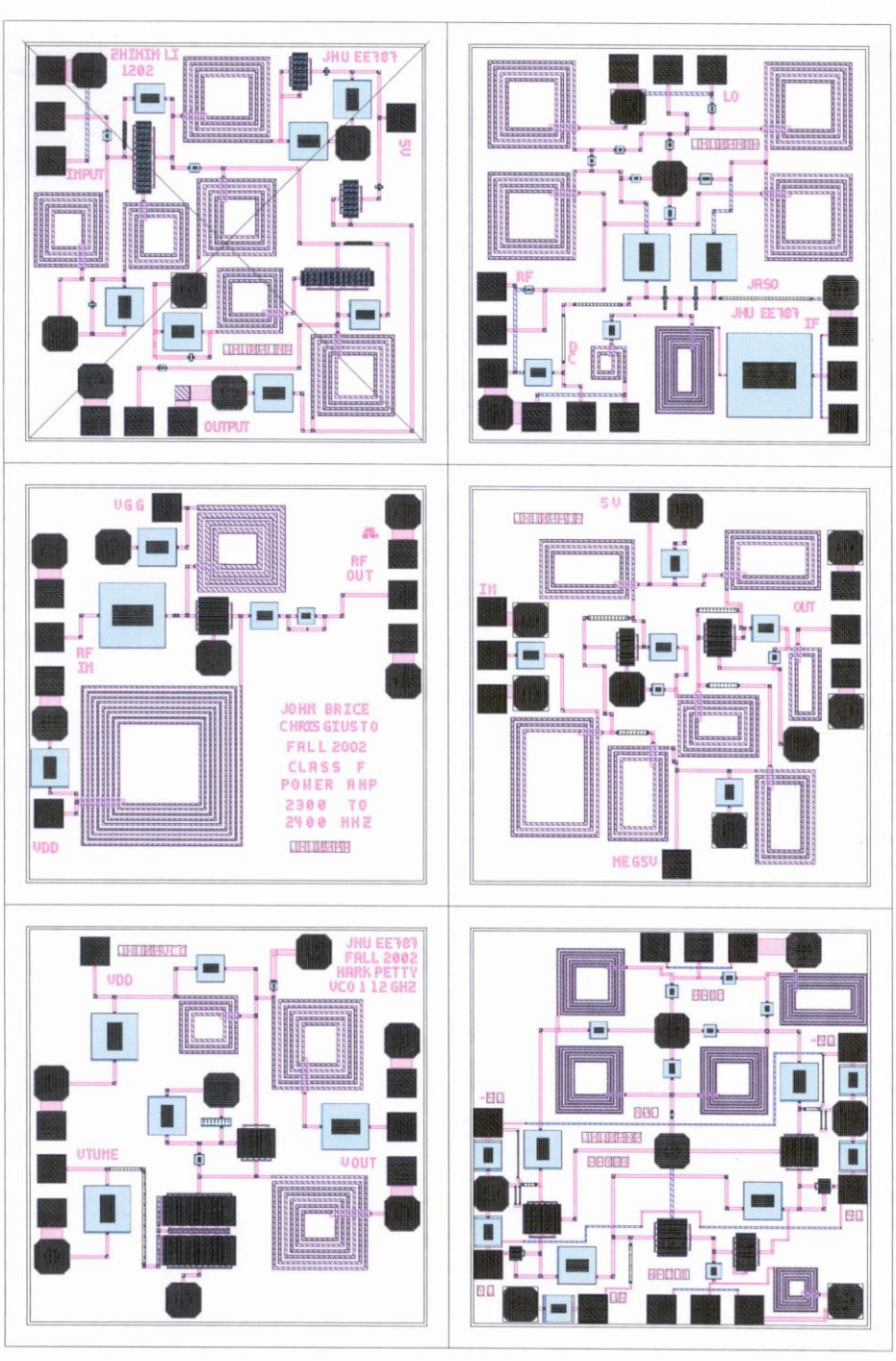
Fall 2002 JHU EE787 MMIC Design Student Project Results
Supported by TriQuint and Agilent Eesof
Professors Craig Moore and John Penn

Low Noise Amplifier—Li Zhimin
Mixer---Jeff Jaso
Medium Power Amplifier—John Brice & Chris Giusto
Post Amplifier—Kerron Duncan & Walter Tates
Frequency Doubler—Ming-Zhi Lai
Voltage Controlled Oscillator—Mark Petty



S-BAND LOW NOISE AMPLIFIER (LNA)

FINAL PROJECT REPORT

December 9, 2002

Zhimin Li

Microwave Monolithic Integrate Circuit (MMIC) Design Course
525.787
Fall 2002
John Hopkins University

TABLE OF CONTENTS

1.0 Summary

A Low Noise Amplifier (LNA) operation at S-Band (2.3GHz to 2.5GHz) has been design as part of a project for the MMIC course at the John Hopkins University. The project is a duplex transceiver employing a receive array for the S-Band wireless communications service(WCS) and industrial, scientific, and medical (ISM) frequencies. The LNA is one of the nine unique designs. Each design is contained on a 60 mil square ANACHIP die using the TriQuint TQTRX design process, with vias, 4 mil (100 um) thick wafer and TOM3 FET model in ADS. Agilent Advanced Design Systems (ADS 2002) is used for the design software. The predicted LNA design achieved all design goals including gain greater than 15 dB, noise figure less than 3 dB (1.12dB MAX), input IP3 great than +5dBm (+7dBm), and input/output VSWR 1.5:1. The LNA will be fabricated by TriQuint and tested with in year 2003.

2.0 Introduction

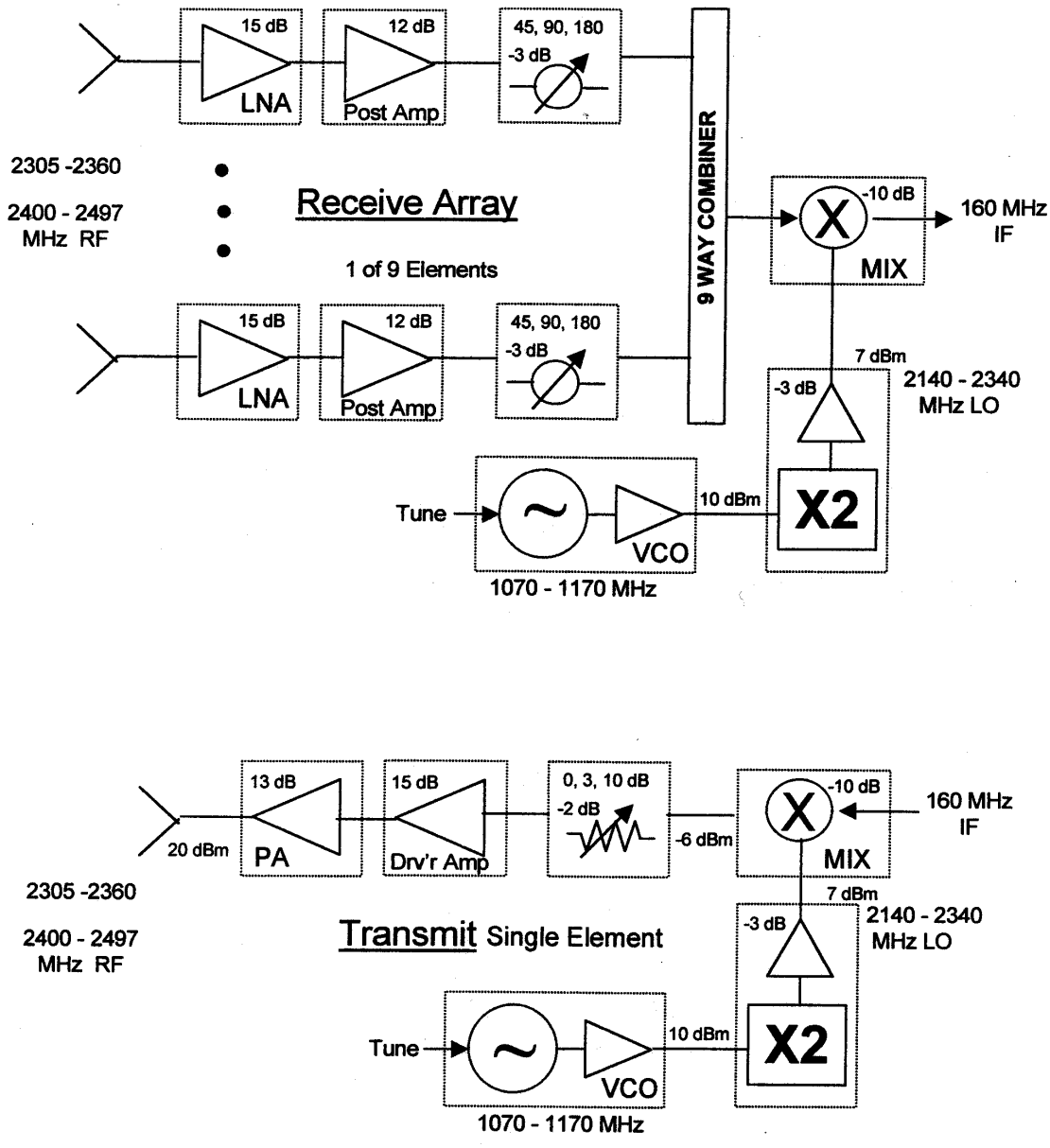
A Low Noise Amplifier (LNA) operation at S-Band (2.3GHz to 2.5GHz) has been design as part of a project for the MMIC course at the John Hopkins University. The project is a duplex transceiver employing a receive array for the S-Band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies. The LNA is one of the nine unique designs. Each design is contained on a 60 mil square ANACHIP die using the TriQuint TQTRX design process, with via, 4 mil (100 um) thick wafer and TOM3 FET model in ADS. Figure 1 is a chip set diagram for the 2305 – 2360 MHz WCS and 2400 – 2497 ISM Bands.

2.1 Circuit Description

The LNA circuit design was a cascaded two-stage amplifier. 600um DFET (12 fingers X 50um) is used for both stages. In order to achieve a single +5Volt power supply, self-biasing was used for both stages. A series inductor at each source of DFET was used for stabilization. High pass matching networks for input/output ports and inter-stage matching were used for reducing the number of entire chip elements. An active load (300um DFET) for each stage amplifier, which generated 20mA constant bias current, was used for saving chip area. A feedback RC circuit for each stage was added to achieve the better performance of gain, gain ripple and stabilization.

2.2 Design Philosophy

Based on its low noise figure and gain characteristics, we choose TriQuint DFET for the LNA design. According to the S-Parameter information of 300um DFET (standard S-parameter file at bias condition Ids=10mA, Vds=2V), two 300um DFETs paralleled together must be used for each stage because of LNA gain and IIP3 issues. From DC curve of 300um DFET, one can see that if Vgs=0V, IDSS=20mA@ Vds=2.5V. See figure 2. 300um DFET active load can be used base on the 300um DFET DC curve for



Chip Set for the 2305 - 2360 MHz WCS and
2400 - 2497 MHz ISM Bands

Figure 1: Chip set for the 2305 – 2360 MHz WCS and 2400 – 2497 MHz ISM Bands

each stage DC bias. The bias point we chosen for each stage of 600um DFET is same, listed as following Table 1:

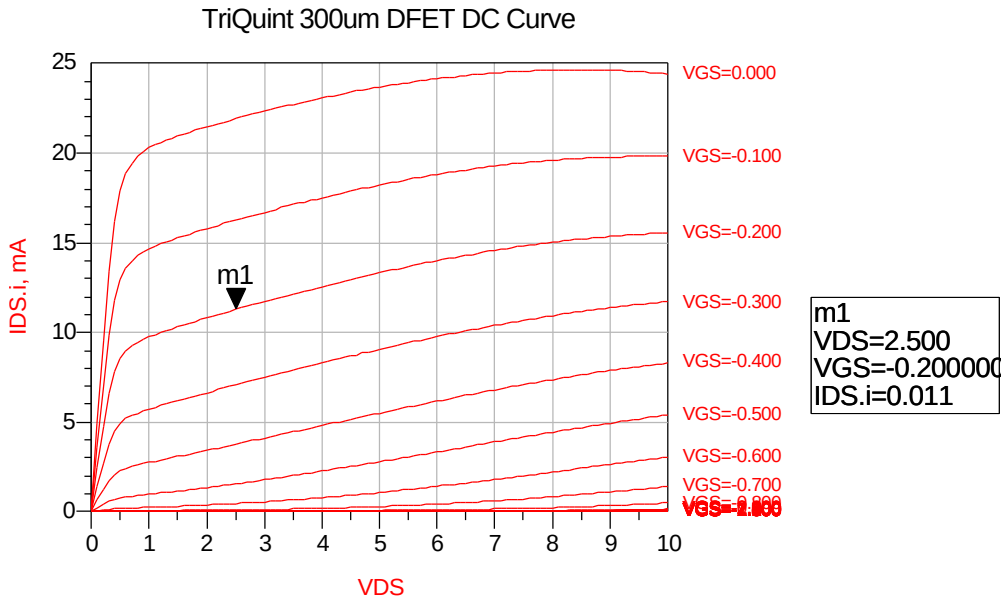


Figure 2: 300um DFET DC Curve

First stage	Second stage
Vds=2.5V	Vds=2.5V
Vgs=-0.17V	Vgs=-0.17V
Ids=20mA	Ids=20mA

Table 1: 600um DFET DC bias point

The design process was focused on achieving a stable design, the goals of high gain, low noise figure, high input IP3, lower gain ripple and good input/output port matching across a desired frequency band (2.3GHz to 2.4GHz). First, we need add an inductor to the source pin of DFET to stabilize it. The value, which we found is 2500 pH. Figure 3 shows the input and output stability circles at frequency 2.4GHz in Smith chart. Table 2 shows the stable factor K and Δ over the frequency range from 500MHz to 5GHz. K>1 and Δ>0, that means the transistor is unconditional stable.

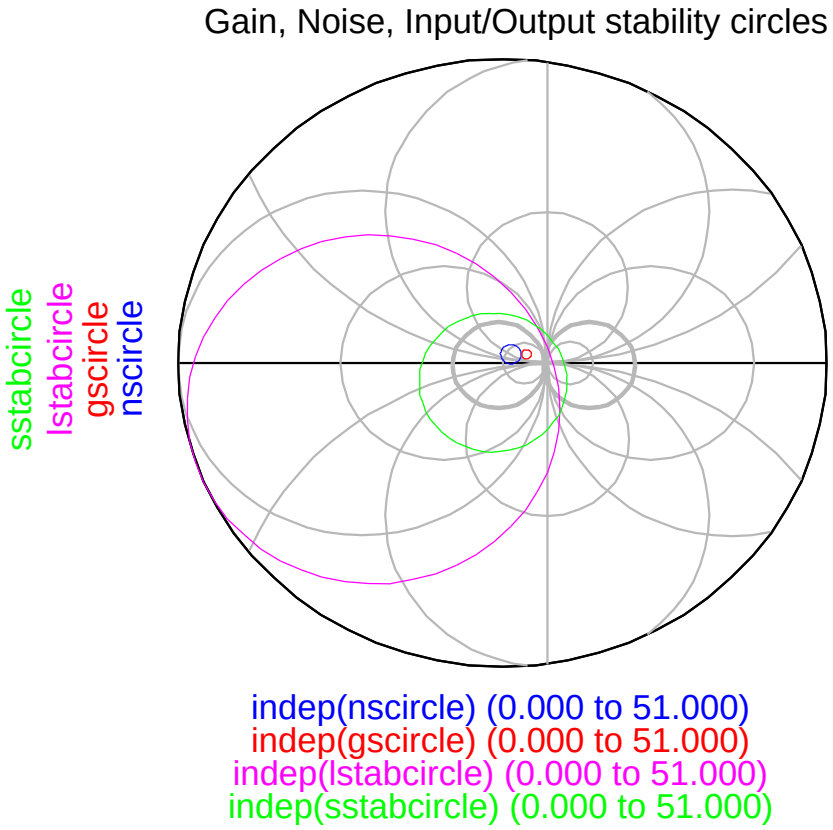


Figure 3: Input and Output stability circles with Gain and Noise Circles

freq	k	Δ
500.0MHz	1.113	1.018
1.000GHz	1.086	0.651
1.500GHz	1.071	0.463
2.000GHz	1.058	0.363
2.500GHz	1.045	0.297
3.000GHz	1.032	0.246
3.500GHz	1.020	0.200
4.000GHz	1.010	0.155

Table 2: Stable factor K and Delta

Second, in order to achieve as greater gain and lower noise figure as possible, a Gs gain circle and noise circle were drawn on one smith chart. See figure 4. An intersection point between Gs gain circle and noise circle is Γs. Γs = 2.1+j1.15. After Γs was found, an input matching network was calculated using high pass network. The reason using high pass network is to have few chip elements, so that chip area can be saved. The shunt inductor can be used as a part of matching network as well as self-bias inductor.

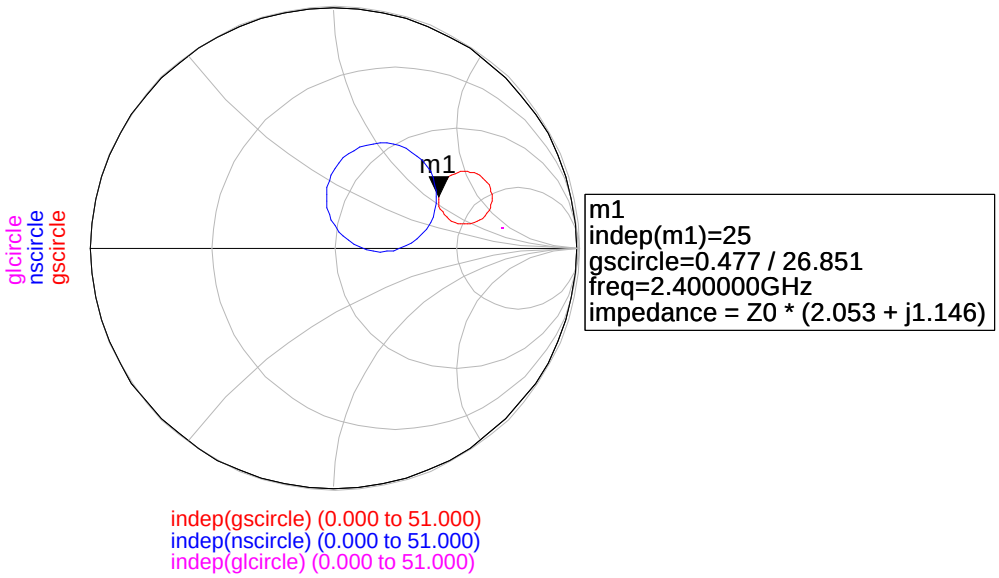


Figure 4: Gs gain circle and noise circle at f=2.4 GHz

Third, after input matching network was calculated, output matching network need to be calculated as well. In order to provide maximum power transfer to the load, ΓL should equal to S22 conjugate. We found out S22 then the output matching network was calculated. Therefore single stage Low Noise amplifier was designed using 300um DFET S-parameter file. Because we only have 300um DFET S-parameter file, to get 600um DFET, two 300um DFET S-Parameter file need to be paralleled.

Now two single 600um DFET low noise amplifiers cascaded together to become one Low Noise Amplifier. The real TriQuint elements that would be required for the layout of final design replaced the ideal elements of the initial LNA design. We call this new one is a simplified schematic since there are no bends, tees MLINs which the final layout need them to finish the chip layout.

Do S-Parameter simulation of the simplified low noise amplifier, the simulation result (such as Gain, noise figure, VSWR and DC bias points) will be shown later at Section 3.2 Predicted Performance. This is the linear simulation using S-Parameter file. We need do a linear simulation with non-linear DFET model and harmonic balance non-linear simulation with non-linear DFET model for the non-linear performances of LNA such as P1dB and input IP3. Simply, replaced S-Parameter file by the non-linear model of 600um

DFET. Do simulation, the result will be shown later at Section 3.2 Predicted Performance.
Regarding layout, the layout process involves interconnection appropriate bends, tees, and MLINs to the optimized LNA design with TriQuint elements. General design guidelines include: keeping the separation as much more as possible between components, sharing vias as many as possible, making sure that a maximum allowable current through a resistor is 1 mA per 1um resistor's width. After finishing the layout, we need re-simulate the layout schematic (simplified amplifier plus bends, tees and MLINs) , if the simulation result is too much off that of the simplified amplifier schematic, we need re-tune the layout elements until the two simulation results are close enough.

2.3 Trade-offs

The major trade-off for designing low noise amplifier is the gain and the noise figure. It is not possible to get maximum gain and minimum noise figure at same time. Therefore, we need trade off the gain and noise figure to get more gain and less noise figure.

3.0 Modeled Performance

3.1 Specification Compliance Matrix

Table 2 shows the design specifications and the predicted performance for this LNA.

Table 3: Design Spec and Predicted Performance

Characteristic	Spec Goal	Simplified Schematic LNA performance	Final LNA predicted Performance
Frequency	2300 to 2500 MHz	2300 to 2500 MHz	2300 to 2500 MHz
Band width	> 200 MHz	> 200 MHz	> 200 MHz
Gain	> 15 dB	15.5 @ 2.4 GHz	16.5 @ 2.4 GHz
Gain ripple	±0.5 dB max	< ±0.5 dB	< ±0.5 dB
Noise figure	< 3 dB	1.2 dB	1.2 dB
Input IP3	>+5 dBm	+7 dBm	+7 dBm
VSWR, 50 Ohm	<1.5:1 input & output	1.4:1 max	1.6:1 max
Power supply voltage	+5 Volts only	+5 Volts only	+5 Volts only
Chip size	60 x 60 mil ANACHIP		60 x 60 mil ANACHIP

3.2 Predicted Performance

The following simulation results show the performances of this low noise amplifier.

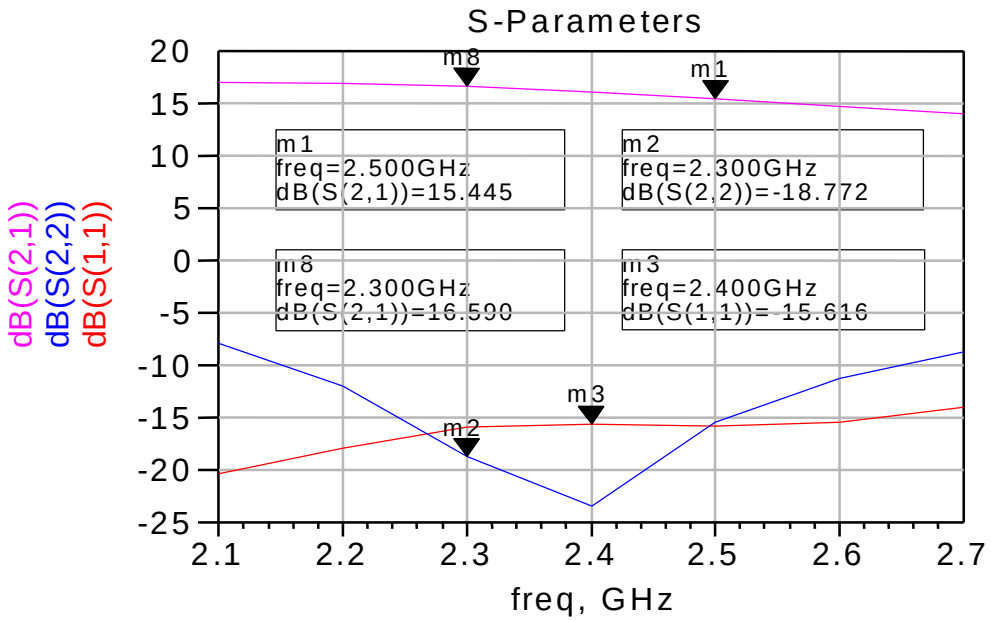


Figure 5: S-Parameter performances of simplified schematic LNA (linear simulation using 300um DFET S-Parameter file)

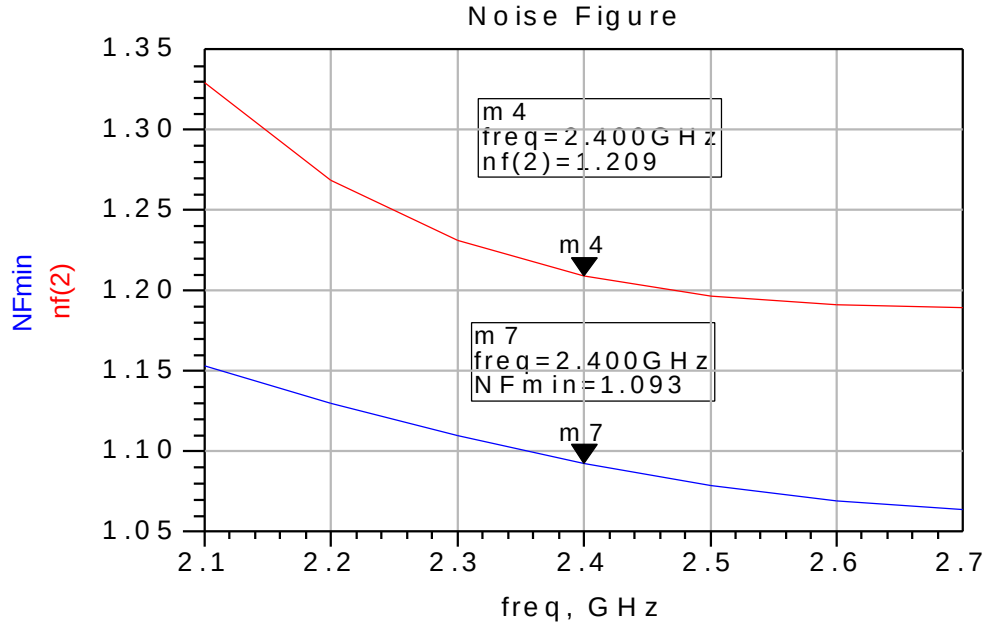


Figure 6: Noise figure performance of simplified schematic LNA (linear simulation using 300um DFET S-Parameter file)

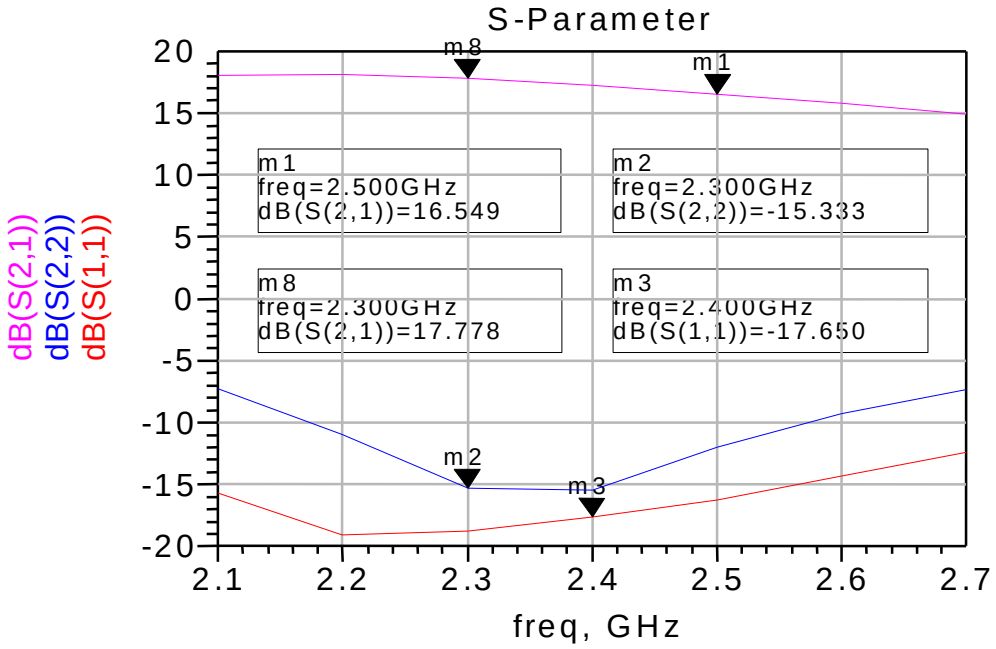


Figure 7: S-Parameter performances of simplified schematic LNA (linear simulation using 600um DFET non-linear TOM3 model)

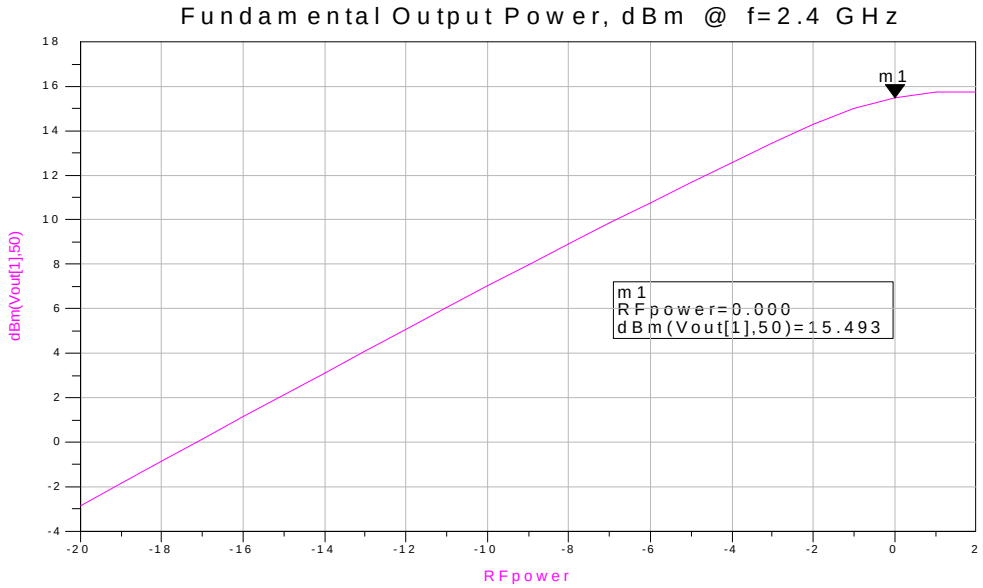


Figure 8: P1dB performance of simplified schematic LNA (harmonic balance simulation using 600um DFET non-linear TOM3 model)

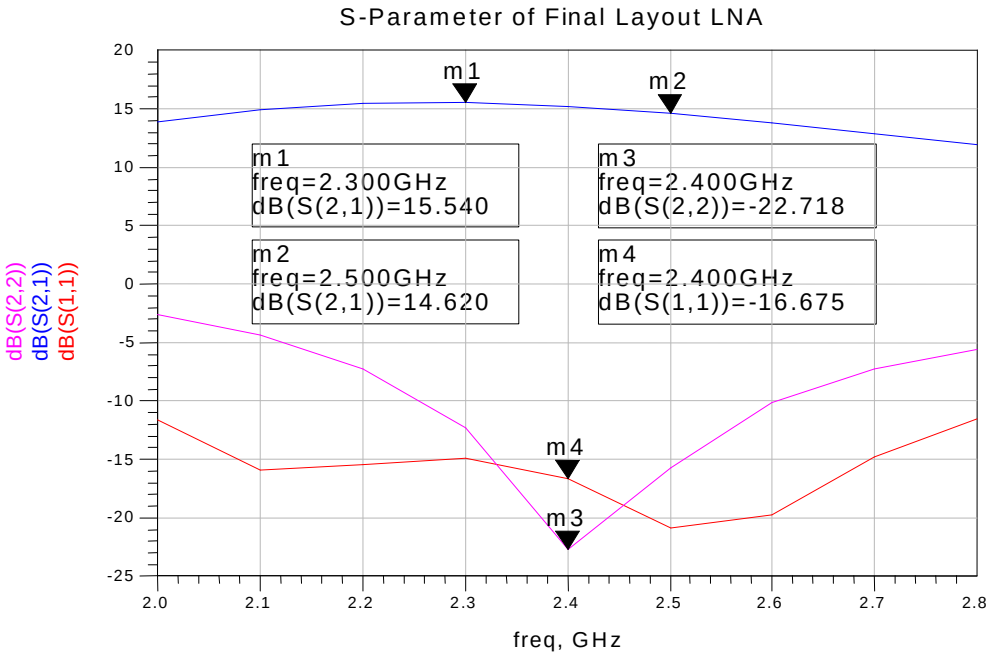


Figure 9: S-Parameter performances of final layout schematic LNA (linear simulation using 300um DFET S-Parameter file)

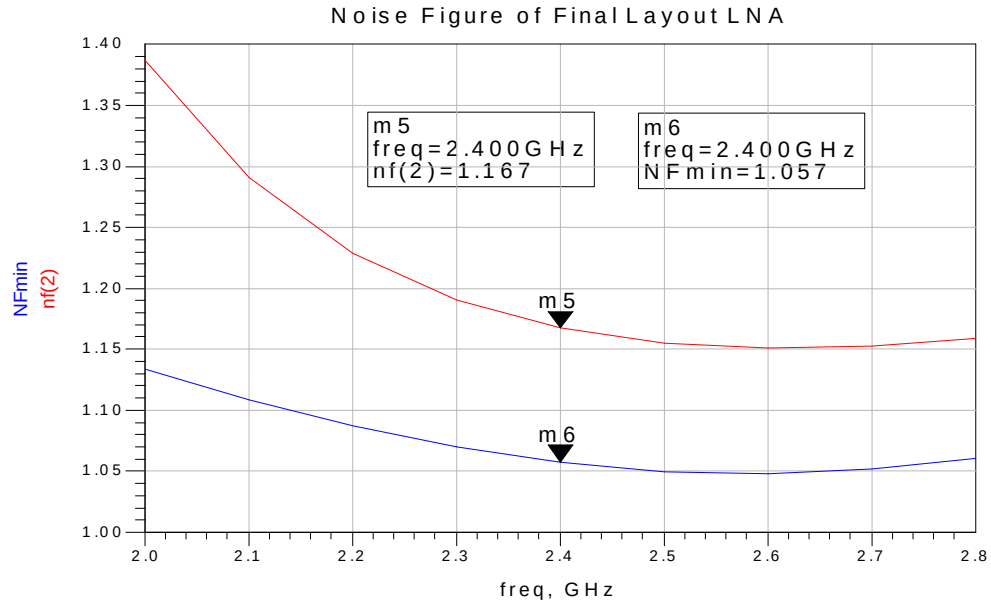


Figure 10: Noise figure performance of final layout schematic LNA (linear simulation using 300um DFET S-Parameter file)

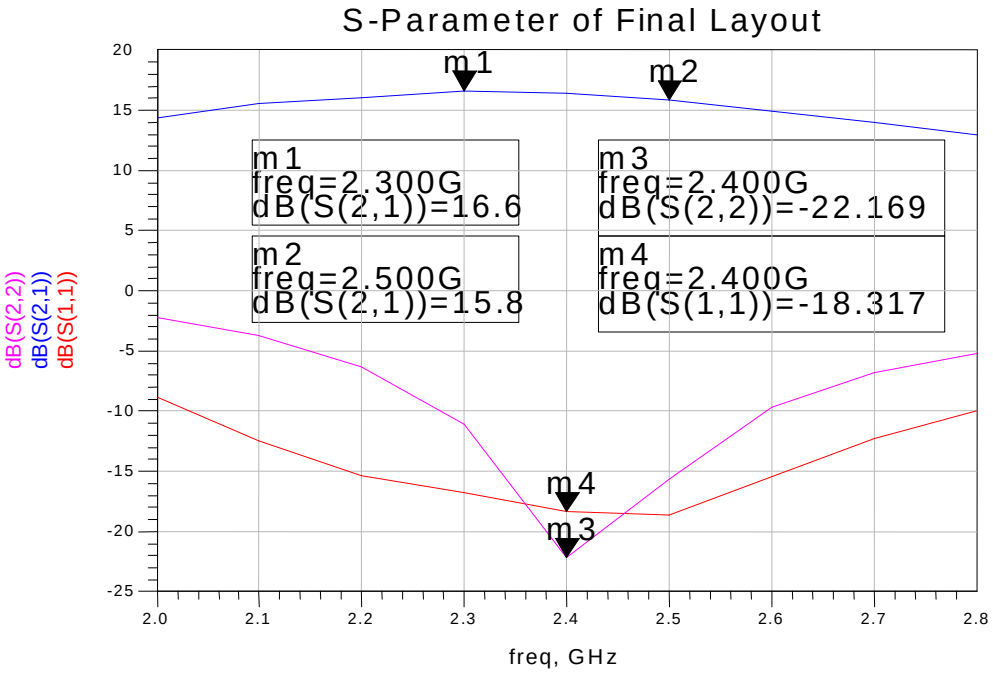


Figure 11: S-Parameter performances of final layout schematic LNA (linear simulation using 600um DFET non-linear TOM3 model)

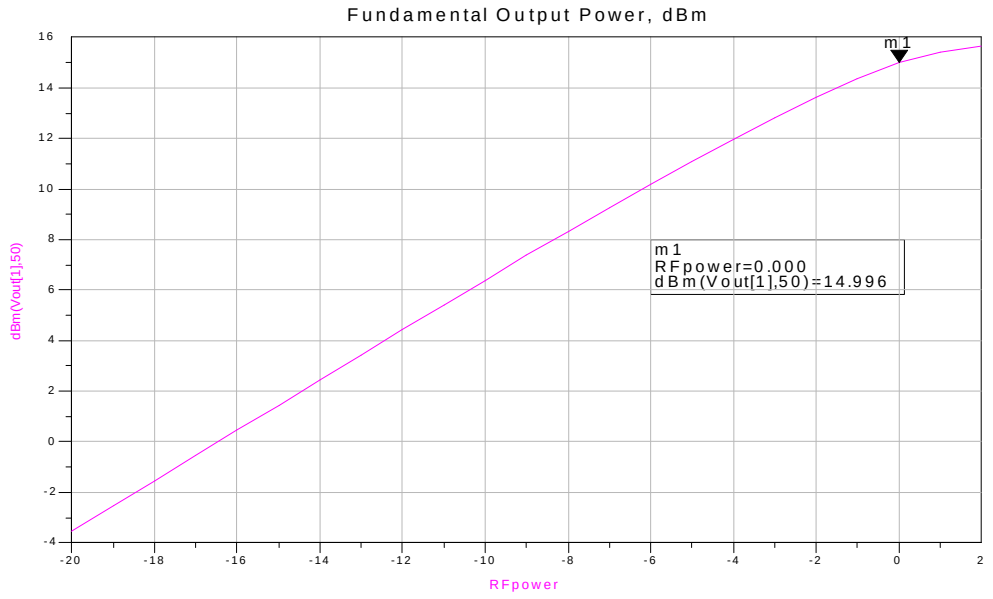


Figure 12: P1dB performance of final layout schematic LNA (harmonic balance simulation using 600um DFET non-linear TOM3 model)

4.0 Schematic diagrams and Layout

The following schematics are including in this report.

Figure 14: LNA simplified Schematic with S-Parameter file
Figure 15: LNA final layout schematic with DFET non-linear model
Figure 16: LNA final layout in ANACHIP

5.0 DC Analysis

Table 4 shows the DC bias simulation results for both stages DFET of LNA.

First stage DFET	Second stage DFET
Vds=2.38 V Vgs=-0.17 V Ids=21.7 mA	Vds=2.38 V Vge=-0.17 V Ids=21.7 mA

Table 4: DC bias simulation results for both stages DFET of LNA

Figure 13 shows DC bias simulation results on simplified LNA schematic using 'Annotate DC simulation' function

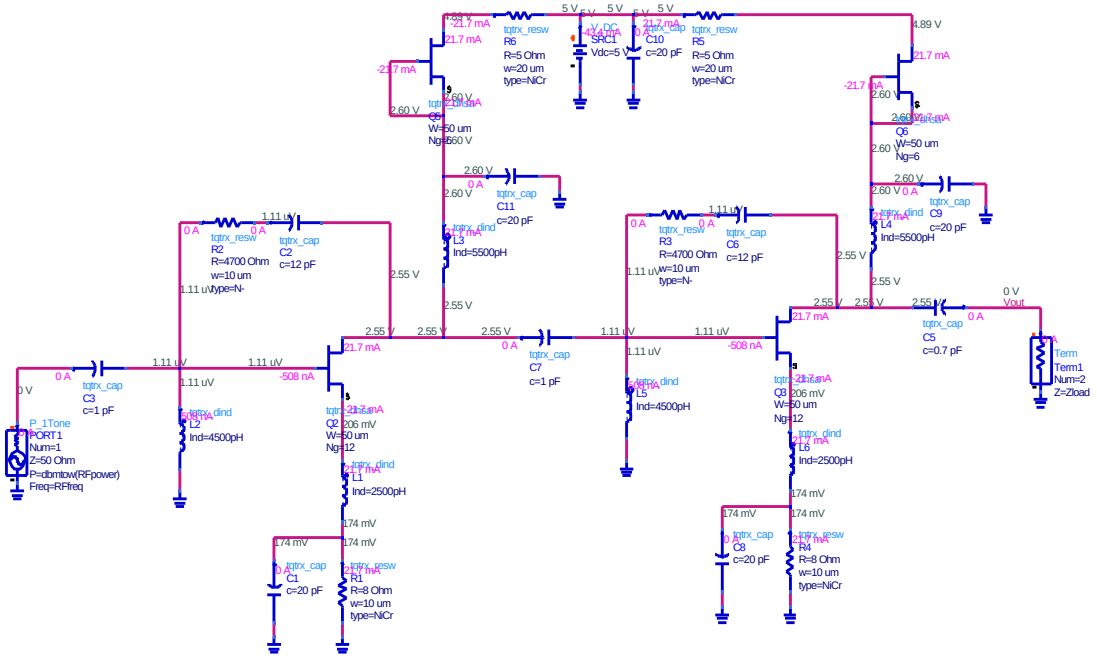


Figure 13: DC bias simulation results on simplified LNA schematic using 'Annotate DC simulation' function

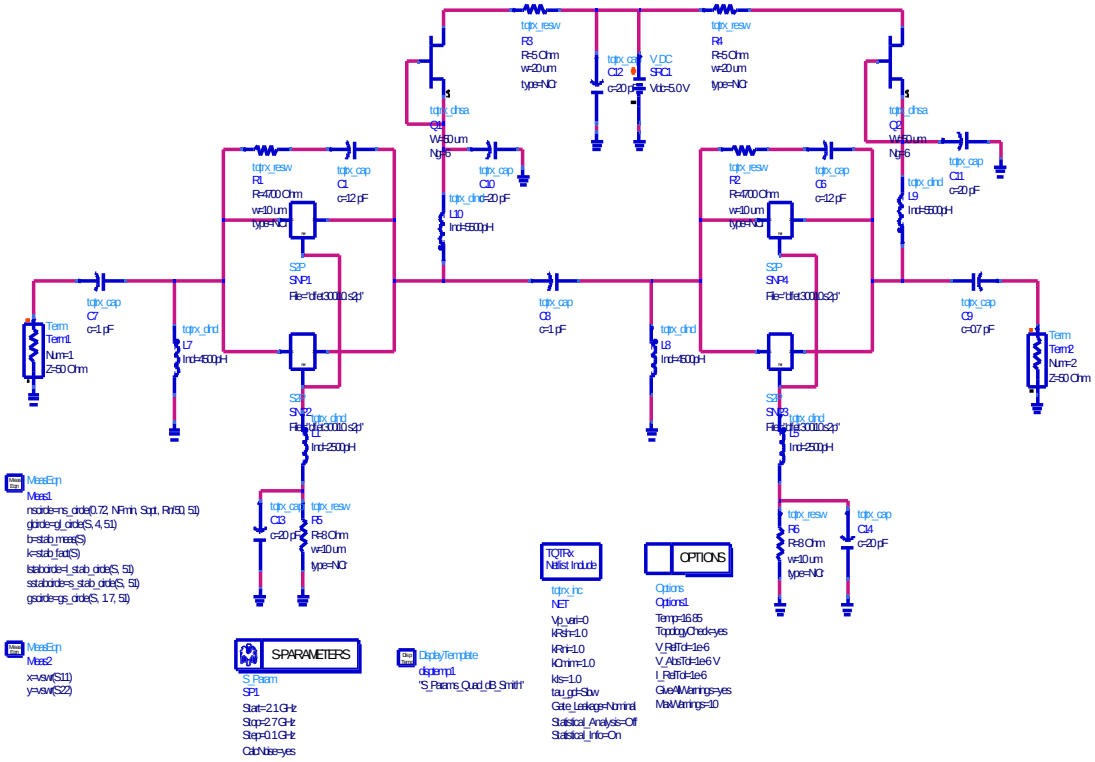


Figure 14: LNA simplified Schematic with S-Parameter file

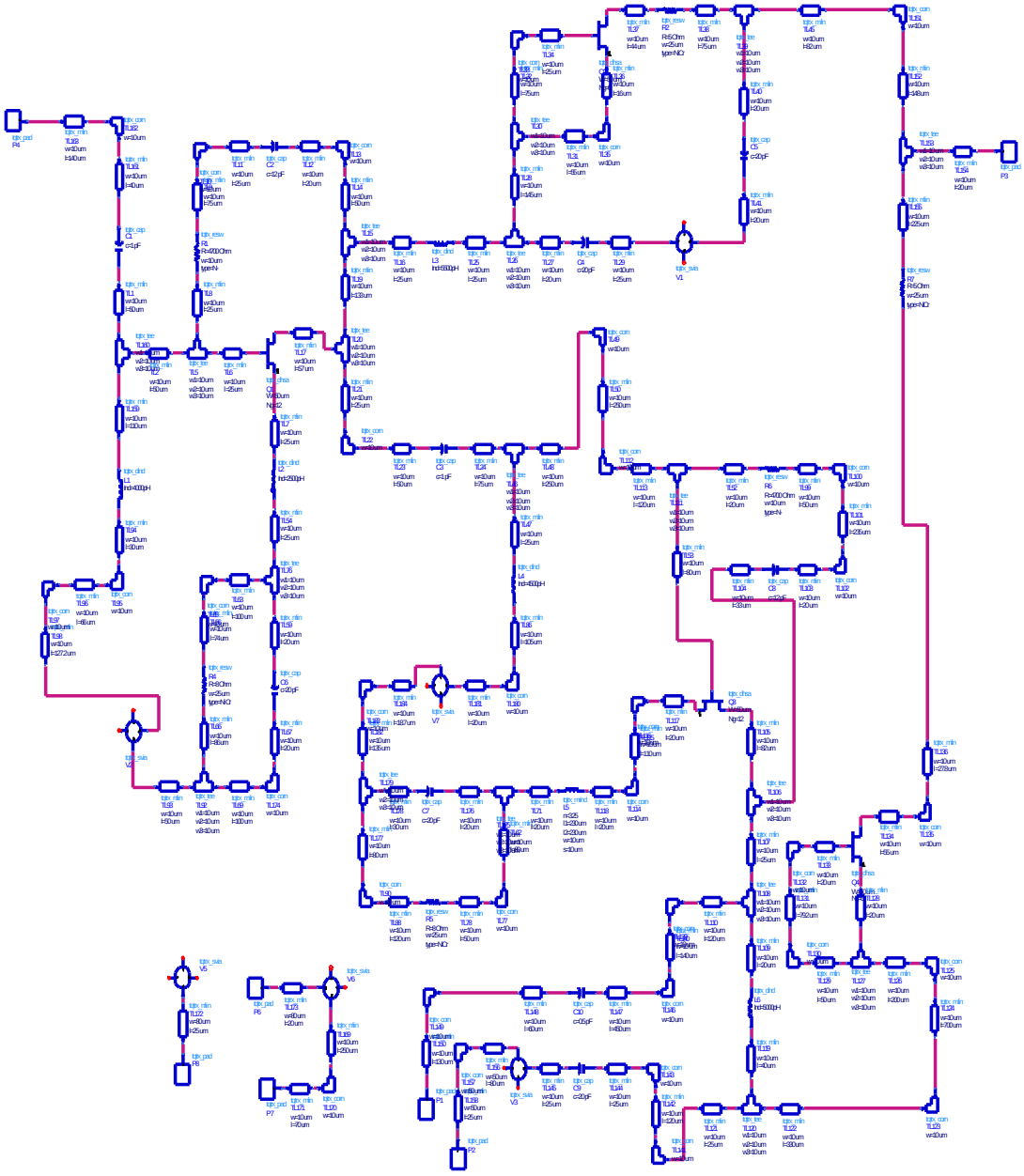


Figure 15: LNA final layout schematic with DFET non-linear model

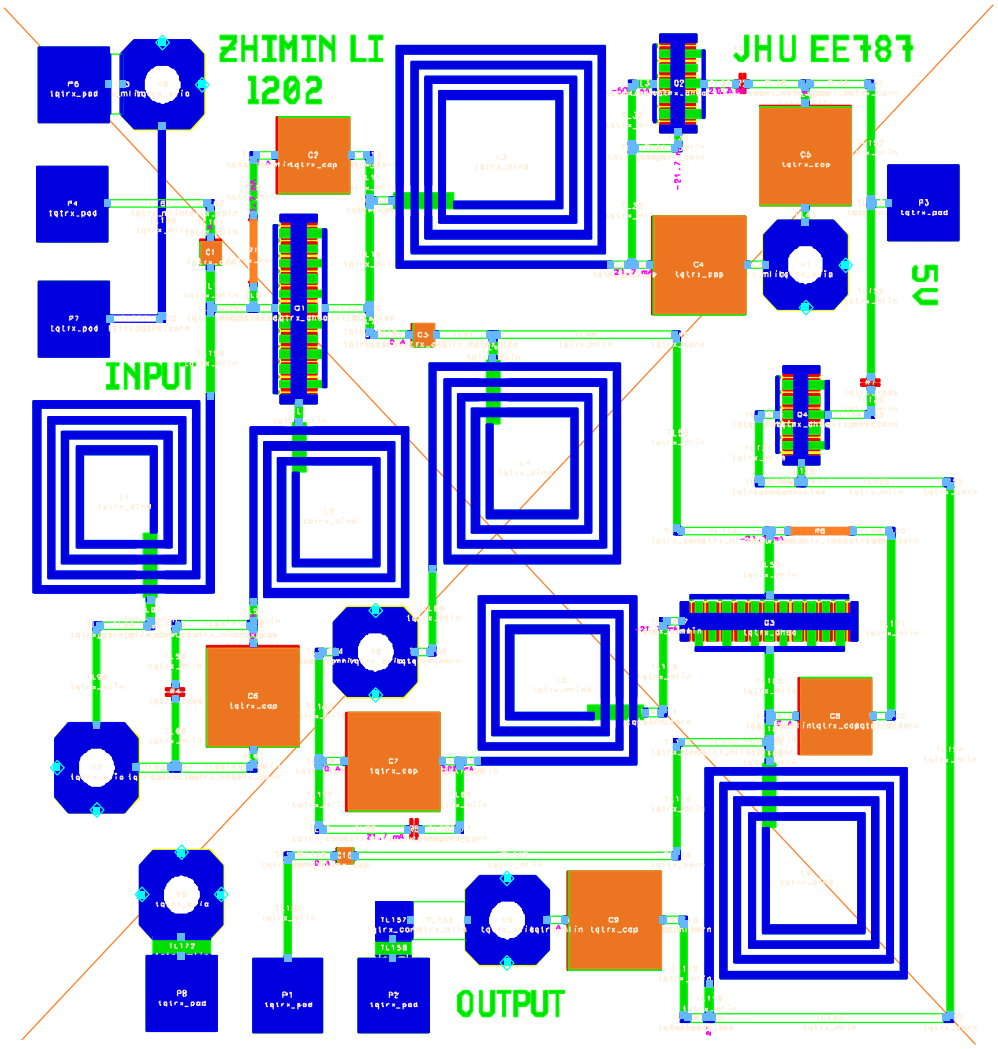


Figure 16: LNA final layout in ANACHIP

6.0 Test Plan

6.1 Test Equipment

The following test equipments or equivalent are necessary to measure the LNA performance:

- Agilent 8510 Network Analyzer
- Agilent xxxx Noise figure meter
- 5 V DC Power Supply
- Synthesized Signal generators to 26 GHz
- Power combiner
- Spectrum analyzer to 18 GHz
- Cascade Model 43 wafer probe station with up to 4 RF probes & 4 DC needle probes

6.2 Turn On Procedure

Extreme caution should be taken when turning on the +5 Volt DC power supply. Make sure the Ground wire is firmly connected on ground PAD before the +5 Volt DC power supply is connected. The required DC voltage and DC current are listed as following:

- The required voltage for the LNA is +5 V DC
- The DC current is around 42 mA

6.3 S-Parameter Measurement

- Calibrate the network analyzer from 2 to 2.8 GHz
- Position the bias probe on the 5V pad
- Position the input probes on the “INPUT” pads
- Position the output probes on the “OUTPUT” pads
- Make S11, S21, S12, S22 measurements, plot the data and store all data on disk

6.4 Noise figure Measurement

- Calibrate the noise figure meter
- Position the bias probe on the 5V pad
- Position the input probes on the “INPUT” pads
- Position the output probes on the “OUTPUT” pads
- Make noise figure measurements and record the data

6.5 Input IP3 testing

- Set f1=2.4 GHz, f2=2.45 GHz

- Set each tone power level of output port of power combiner to –10 dBm
- Use the spectrum analyzer to measure the delta of power lever between fundamental frequency and third order frequency
- The input IP3 should equal to $-10+\Delta/2$ dBm

7.0 Conclusion and Recommendations

The LNA design and layout were very successful. It met all the goals. The gain is great than 15 dB over the desired frequency, noise figure is less than 1.3dB much less the spec of 3 dB, and input IP3 is great than +5 dBm. The layout of LNA is so nice and well organized. There is no recommendation.

8.0 Project file

The project file has been submitted on 3.5 inch HD diskette

9.0 GDSII (CALMA) Layout file

The GDSII layout file has been submitted to instructors

The Design of an S-band Single Balanced Mixer for Starved Diode Operation

Jeffrey Jaso

Johns Hopkins University EE525.787

December 9, 2002

1. Abstract

This paper presents the design strategy, simulation results, and final layout of a MMIC S-band single balanced mixer optimized for starved diode operation. The design fits on a 60 mils square die and is to be fabricated using the Triquint Semiconductor TRx process for GaAs. Agilent's Advanced Design System (ADS) in conjunction with Triquint's proprietary library was the software tool used for simulation and layout.

The RF band of the mixer is 2300-2500MHz; the LO band is 2140-2340MHz; and the IF center frequency is 160MHz. The mixer can be used for both upconversion and downconversion. With a 5V DC bias applied to the diodes and with a 0dBm LO power level, the mixer achieved the following performance:

- Conversion Loss < 10dB
- LO VSWR <= 1.6 : 1
- RF VSWR <=2.2 : 1
- IF VSWR < 2.1 : 1
- LO/RF Isolation > 27dB
- IF/RF Isolation > 19dB
- LO/IF Isolation > 39dB

All prescribed minimum performance specifications were met, and many of the design goals were also achieved.

2. Introduction

In selecting the mixer topology the first decision was between double balanced and single balanced approaches. The former affords excellent isolation and good VSWR over a wide bandwidth, but at the expense of greater conversion loss, higher LO drive level, and a more complicated layout due to the ring diode structure. Furthermore, the ring diode structure complicates DC biasing of the diodes.

A single balanced mixer, on the other hand, provides moderate isolation, good VSWR over a narrow bandwidth, and low conversion loss—all in a simple structure that lends itself well to DC biasing.

Given the emphasis on conversion loss and starved diode operation in this design, coupled with moderate VSWR and isolation requirements, a single balanced approach was the more judicious choice. A single balanced mixer is typically implemented in one of two ways: with a 90^0 or 180^0 hybrid (see Figures 1 and 2)[1]. While the conversion loss of the two varieties are similar, the LO/RF isolation of the 180^0 hybrid is determined mainly by the inherent isolation of the coupler, but the VSWR of the LO and RF ports is mainly set by the VSWR looking into the diode circuitry. The LO/RF isolation of a mixer using a quadrature hybrid, however, is mainly a function of the return loss of the coupler, while the VSWR is dictated by the quality of the terminations at the RF/LO frequencies. An important limitation of the 90^0 hybrid approach is that it cannot function simultaneously as an upconverter and downconverter. Since this dual capability was an important goal of this design, the 180^0 hybrid approach was favored. The inductors provide a DC path to ground as well as an IF return, while the capacitor provides an RF path to ground to allow the diodes to be pumped. To supply DC bias current, the inductors in the actual design are replaced with resistors.

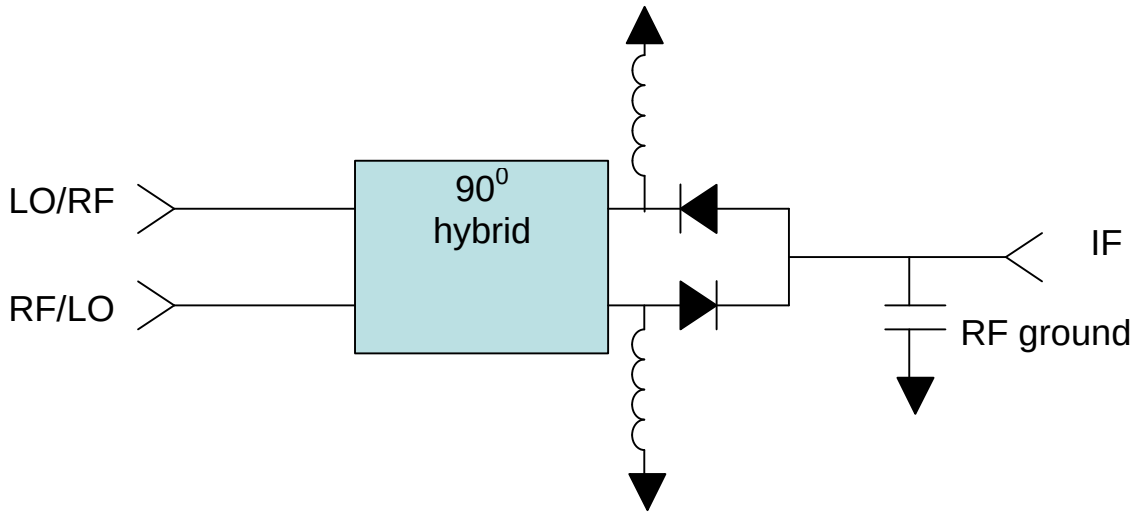


Figure 1: Single Balanced Mixer Using 90^0 Hybrid

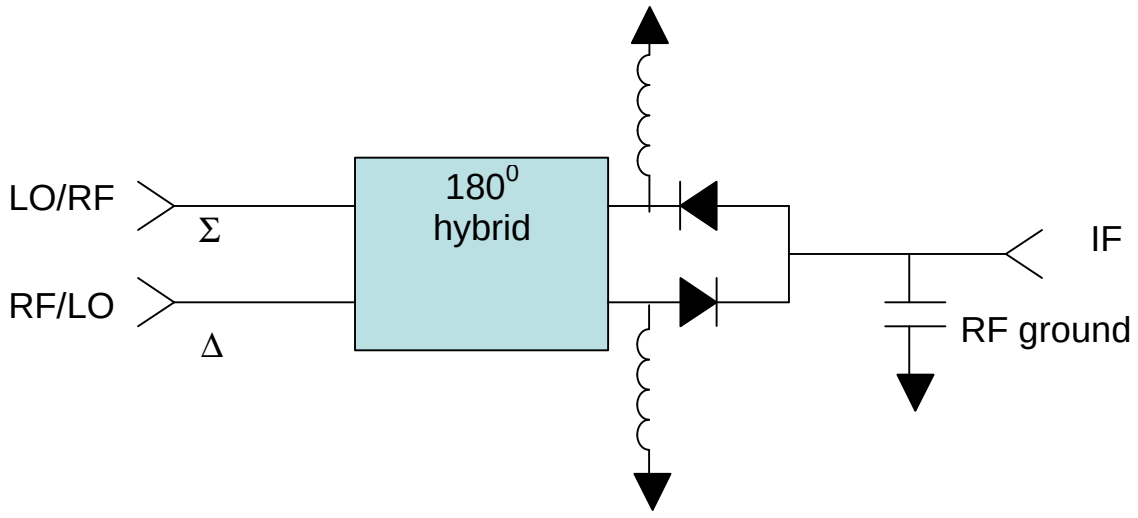


Figure 2: Single Balanced Mixer Using 180^0 Hybrid

3. Specifications and Modeled Performance

Table 1 contains the combined specifications for the S-band downconverter and upconverter alongside the modeled performance of the circuit extracted from the final layout. All specifications were met in addition to several of the design goals. The boldfaced results indicate that the design goals were achieved. Figures 3-8 display simulation data for upconversion and downconversion operation at the center frequency and the band edges. Table 1 includes worst-case results.

	Specs	**Goal**	**Modeled Results**
RF Frequency (MHz)	2300 - 2500	N/A	2300 - 2500
LO Frequency (MHz)	2140 - 2340	N/A	2140 - 2340
IF Frequency (MHz)	160	N/A	160
Isolation: LO/RF port (dB)	> 10	>=7	**27**
Isolation: IF/RF (dB)	N/A	N/A	**19**
Isolation: LO/IF (dB)	N/A	N/A	**39**
Conversion Loss (dB)	<= 10	<=7	10
LO power (dBm)	<= 7	0	**0**
VSWR (50 W): LO	<=2.5:1	<=1.5:1	1.6: 1
VSWR (50 W): RF	<=2.5:1	<=1.5:1	2.2: 1
VSWR (50 W): IF	<=2.5:1	<=1.5:1	2.1: 1
DC Bias Voltage (V)	0 -5	N/A	**5**
Die Size (mil x mil)	60 x 60	60 x 60	**60 x 60**

Table 1: Specifications and Modeled Results

4. Schematic, Design Notes, and Layout

Figure 9 depicts a stripped down version of the final design without transmission line elements. A lumped element realization of a ratrace hybrid designed at the center frequency of the combined RF-LO band (2140 – 2500MHz) performs the function of the balun, with the LO and RF attached to one pair of mutually isolated ports and the two diodes connected to the other pair.[2] The 10dB return loss bandwidth of the hybrid is roughly equivalent to the LO/RF band of the mixer. A pair of 30pF DC blocking capacitors (C26 and C27) and one 100pF capacitor allows DC current to flow through the diodes. The current through the diodes is set by the sum of two 1500Ω resistors and the composite DC resistance of the diodes. The optimum DC voltage is 5V. The diodes are overlap diodes rather than FETs with drain and source terminals shorted. A diode width of 80μm resulted in the optimal combination of RF/LO and IF VSWR as well as conversion loss.

Two 0.75pF capacitors to ground (C33 and C35) act as simple matching stubs to improve the VSWR at the LO and RF ports. The IF matching network consists of a single series 14nH inductor (L15). In fact, the optimal value would be close to 50nH, but the size of such a component would be prohibitively large. A 500pH inductor (L14) resonates with the bypass capacitor (C29) to provide an RF ground but also to present a high impedance at IF. A 100pF DC blocking capacitor (C30) is placed at the IF port. As large as this value is for a MMIC design, it still represents a compromise since it still appears as a significant impedance at IF. In keeping with the objective of requiring no off-chip components for this design, the largest DC blocking capacitor that could fit was selected.

To measure the large signal VSWR at each mixer port, dual directional couplers were placed at each port. Γ was found by calculating the ratio of incident to reflected voltage at the coupled ports of the couplers, and VSWR in turn was determined by the relation:

$$VSWR = (|\Gamma| + 1)/(|\Gamma| - 1)$$

The final layout submitted for fabrication appears in Figure 10. Each of the four ports is labeled appropriately. Each signal port is flanked on both sides by ground pads to accommodate test probes. The ratrace coupler occupies the upper half of the chip, with the bottom right consisting of the IF matching network and DC block. Care was taken to keep as much space between inductors as possible to minimize mutual coupling.

5. DC Analysis

Figure 11 presents a simplified DC schematic with DC annotations at each node. It is apparent that the DC bias is isolated from the ratrace coupler by the blocking capacitors. With the voltage supply set to 5V, the current flowing through the 80μm diodes is 1.29mA, safely below the maximum 10mA rating of the two 10μm bias resistors. This implies a DC diode resistance of roughly 440Ω. This indicates that the diodes are not fully turned on.

6. Test Plan

Figures 12-13 show the test setup for the mixer for upconverter and downconverter operation, respectively. Note that a spectrum analyzer and dual directional coupler need not be present at each port simultaneously. However, whenever a directional coupler is present at a port, each coupled port must be terminated in 50Ω.

For upconverter operation, the test plan is as follows:

1. Calibrate: determine insertion loss of directional coupler(s) and cables.
2. Set LO signal generator to midband frequency (2240MHz) and power level such that 0dBm is present at the LO port.
3. Set IF signal generator to 160MHz and power level such that –10dBm is present at the IF port.
4. Measure LO+IF, IF, and LO at RF port with spectrum analyzer. Add cable and coupler losses to calculate conversion loss, LO/RF isolation, IF/RF isolation. Vary bias voltage to obtain optimal values.
5. Calculate VSWR at LO and IF ports: Measure incident and reflected power at respective coupler ports; convert to voltage; and compute gamma and VSWR.
6. Repeat steps 2-5 at lowest LO frequency 2140MHz.
7. Repeat steps 2-5 at highest LO frequency 2340MHz.

(Optional) For downconverter operation, the test plan is as follows:

8. Set LO signal generator to midband frequency (2240MHz) and power level such that 0dBm is present at the LO port.
9. Set RF signal generator to 2400MHz and power level such that –10dBm is present at the RF port.
10. Measure IF, LO, and RF at IF port with spectrum analyzer. Add cable and coupler losses to calculate conversion loss, LO/IF isolation, IF/RF isolation. Vary bias voltage to obtain optimal values.
11. Calculate VSWR at LO and RF ports: Measure incident and reflected power at respective coupler ports; convert to voltage; and compute gamma and VSWR.
12. Repeat steps 2-5 at lowest LO (2140MHz) and RF 2300MHz frequencies.
13. Repeat steps 2-5 at highest LO (2340MHz) and RF 2500MHz frequencies.

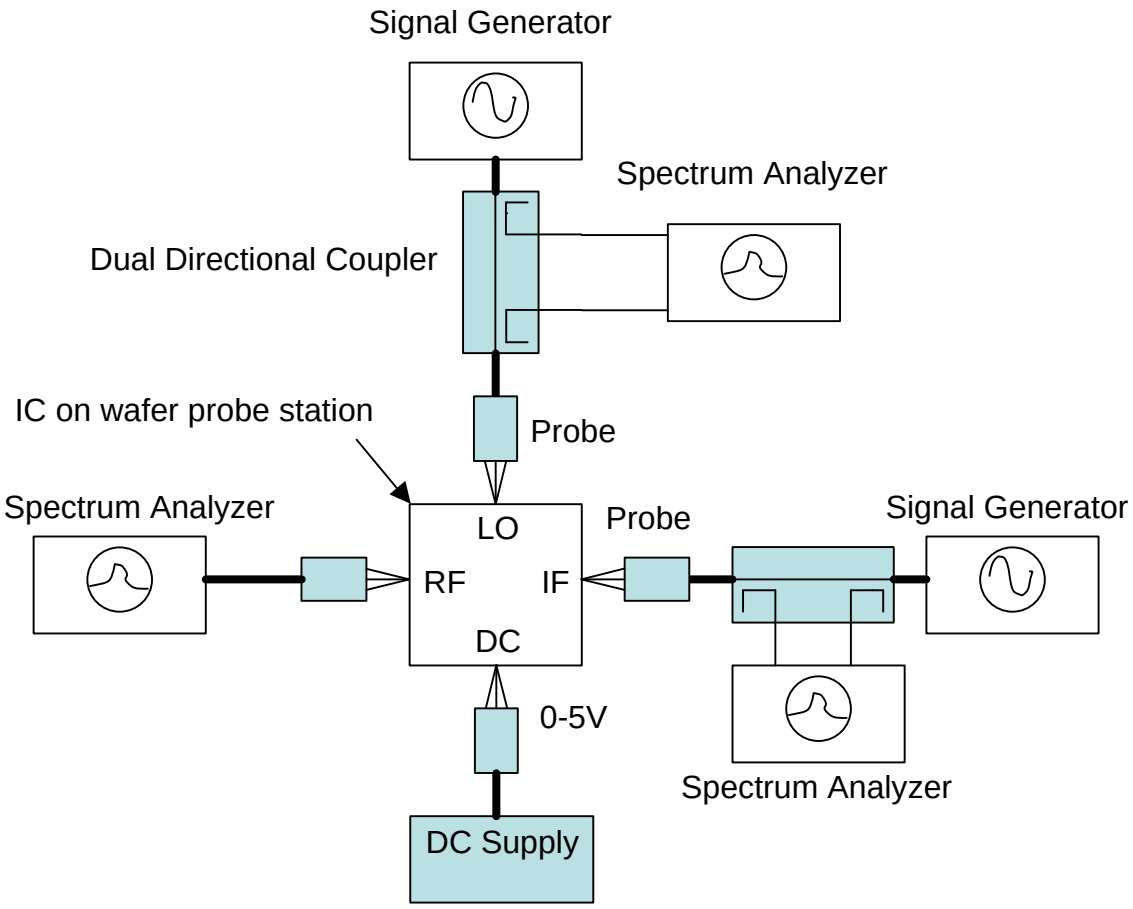


Figure 13: Test Setup for Upconverter Operation

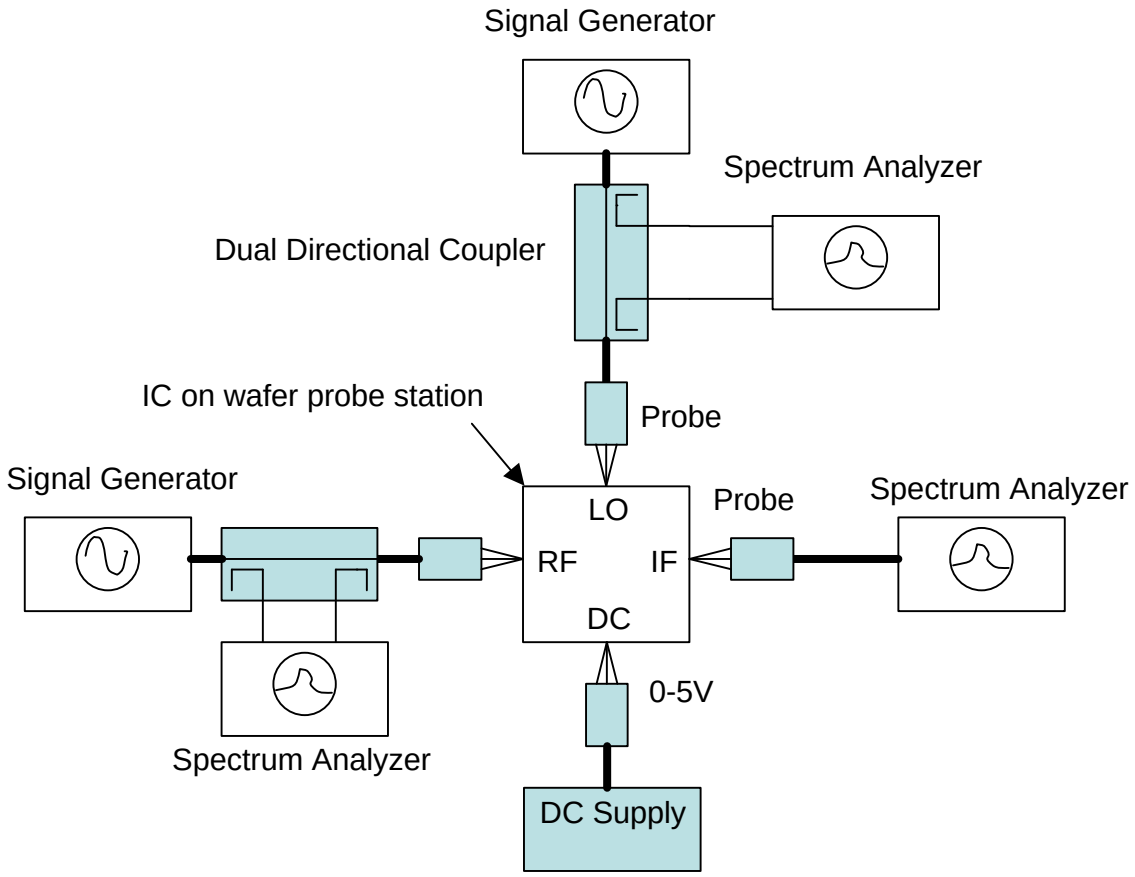


Figure 14: Test Setup for Downconverter Operation

Conclusions and Recommendations

Even though the MMIC was designed to operate without any necessary external components, the user should take the following precaution. A DC bias at the RF or LO port will not affect the performance of the mixer; however, the RF and LO ports are effectively shorted together at DC. Therefore, a DC blocking capacitor should be used if the user's LO and/or RF circuitry would present a DC bias to either port.

If desired, the IF VSWR can be reduced to below 1.5: 1 with the addition of a 43nH inductor in series with the IF port. The conversion loss will also drop by 0.2dB. Any value up to 43nH will improve the VSWR.

In the design of the mixer, prior to incorporating the DC bias a conversion loss less than 7dB was easy to achieve with an LO level of 7dBm. However, the conversion loss specification with DC bias and an LO level of 0dBm was met with little margin to spare. The DC analysis revealed that the diodes are not fully turned on with a 1.29mA bias. However, increasing the current by reducing the value of DC bias resistors lowers the impedance at the diode ports and results in greater conversion loss. This effect can be compensated by the insertion of series RF chokes, IC real estate permitting. A second attempt at this design should investigate this approach, making sure to maintain a symmetrical design to preserve a balanced circuit to ensure high isolation. In other words, the resistance and inductance in the bias path should be divided equally on either side of the diodes, as with the current design.

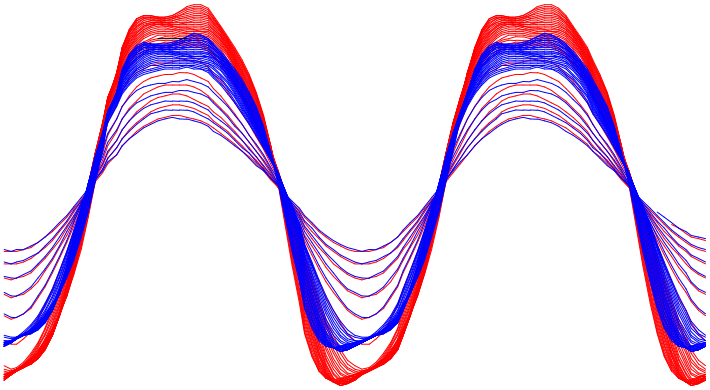
Finally, a layout oversight resulted in the omission of a 0.75pF tuning capacitor at the RF port. The inclusion of this capacitor lowers the RF VSWR to below 1.6: 1 and reduces the conversion loss by 0.5dB.

7. Bibliography

1. Vendelin et al, *Microwave Circuit Design: Using Linear and Nonlinear Techniques*, John Wiley & Sons, New York, 1990, pp. 536-552.

2. Stephen A. Maas, *Nonlinear Microwave Circuits*, IEEE Press, New York, 1997, p. 273.

S Band Class F Power Amplifier



John Brice
&
Christopher Giusto

Johns Hopkins University
MMIC Design
525.787
Fall 2002

S Band Class F Power Amplifier

Abstract

A MMIC design for an S-Band Class F Power Amplifier has been realized. This design calls for an efficient amplifier with a bandwidth of greater than 200 MHz with a small signal gain of a minimum of 13 dB and a target of 15dB. The design called for a gain ripple of ± 0.5 dB. The output needed should be greater then 20 dBm @ 1 dB compression point. Addition specifications called for a voltage standing wave ratio 1.5 to 1, an efficiency of greater then 20% at the 1 dB compression point. The design had to be fitted on a 60 x 60 mil chip using TriQuint components.

S Band Class F Power Amplifier

Introduction

Circuit Description:

The circuit was realized first with ideal lumped elements and then with TriQuint components and finally with microstrip line connections. The circuit in figure 6 shows the input match, output match, a harmonic trap, bias circuits, DC feeds, and RF short. The input match was realized with C13 and L1. R1 is a stabilizing resistor used for stability. L1 also is used as a RF block for the gate supply. L4 is the drain RF block. C6 and C7 are capacitor used to short any RF signal which reach the supply. C11 and L16 are used to trap the harmonics. C15 is used to match the load and Block any DC voltage from reaching the load.

Design philosophy:

A 600 um TriQuint GFET was chosen with 6 fingers. This is based on which model gives the closest results to actual performance of the transistors. The GFET model was shown in class to give very good result with the gate bias considered. These transistors were also good power handling transistors.

The bias was chosen to about 25 % of Idss. The voltage was chosen based on limitation of the supply. This gave the bias shown in figure 10. The output was matched using the cripps method in order to maximum power across a 50 ohm load. This value was chosen to be ~10 pF. This value later changed due to tuning. The input match was then chosen to give the best match for the transistors and the output power match. This was realized with a ~59 pF cap and a 3.7 nH inductor (L1). L1 was also used as an RF block for the gate supply. Looking at initial results the design was not stable and the R1 resistor needed to be added in order to stabilize the design. This lowered the gain but also stopped to design from oscillating. In order for the design to provide high efficiency, the drain voltage should look like a square wave and the drain current should look like a triangle. The parallel circuit of C11 and L10 were determined in order to trap or block all harmonics except the fundamental. Two additional components were also used in order to short the second harmonic but it was later removed because the values, which were calculated, were unrealizable. He design suffered efficiency loss and let a small portion of the 2^{nd} harmonic to reach the load. The drain voltage waveforms are shown in figure 12. While the current looks similar to a triangle the voltage looks similar to a square. The waveforms could have been improved but that would require handling higher order harmonics. The design was started from the beginning using TriQuint capacitors and resistors. This was done because the TriQuint resistors and mim capacitor give very good performance agreement with ideal elements except for added

resistance. It was determined that using TriQuint components would help stabilize the design with the added resistance associated with each component as well as give good results. The inductors were chosen after the design was completed. The inductors had to be model in order to give the same performance as the ideal results. This is shown in figure 11. The tuning of the harmonic circuits was done in a similar manor. By tuning the harmonic circuits for VSWR and small signal gain the output waveforms were slightly distorted. This is probably due to the inductances changing from ideal to real and being slightly out of tune with each other. The distortions are shown in figure 12. But upon further examination at marker 22, it is showing that the distortion starts at an RF input power of 11 dBm's which is around the same point the design reaches the 1 dB compression point.

Trade-offs:

The trade-off for this design was directly associated with which design specifications were the most important. Initially, meeting the 25% was a goal, which could be reached. Efficiencies as high as ~70% were traded off in order to meet small signal gain. Also in order to stable the design the gain suffered. The VSWR was not met and could not be met and meet the other specifications. Also the efficiency suffered because the higher order harmonics were not addressed. This is because additional components would have made the design too large to fit on the 60 x 60 chip requirement. Also additional components would have brought the small signal gain down further. Another keynote is shown in figure 13 that shows that the 2^{nd} harmonic is actually coming through. This is due to the elimination of the last harmonic circuit.

Modeled Performance

The following compliance matrix shows the specifications given and our results before and after layout.

	Specification	Pre – Layout	Post - Layout
Transistor class	Class F	Yes	Yes
Frequency	2300 to 2500 MHz	Yes	Yes
Gain	13 dB	12.205 dB	12.297 dB
Gain Ripple	+/- 0.5 dB	0.052 dB	0.031 dB
Power out, @ 1dB	20 dBm	23.78 dBm	23.82 dBm
Efficiency	20%, 25% goal	37.175%	37.551%
VSWR	<1.5:1	>1.5:1	>1.5:1
Supply Voltage	+7, -5 Volta	Yes	Yes
Size	ANACHIP	Yes	Yes

From the previous matrix you can see that we are meeting the specification for everything except VSWR and Small signal gain. Our VSWR did not meet the spec however the amplifier is not oscillating. We needed to sacrifice VSWR in order to maintain the more important efficiency and power (figure 1, 3). We just missed the gain spec of 13 dB at 12.2 pre - layout and 12.3 post - layout. We were able to maintain an extremely small gain ripple (figure 1, 3). Our efficiency and power level exceeded our goal by over 10% (figure 2,4).

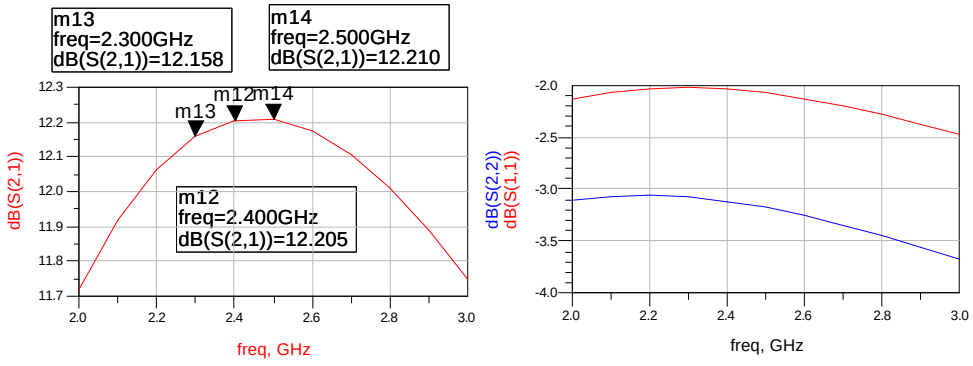


Figure 1
Pre - layout, small-signal responses. Gain, VSWR.

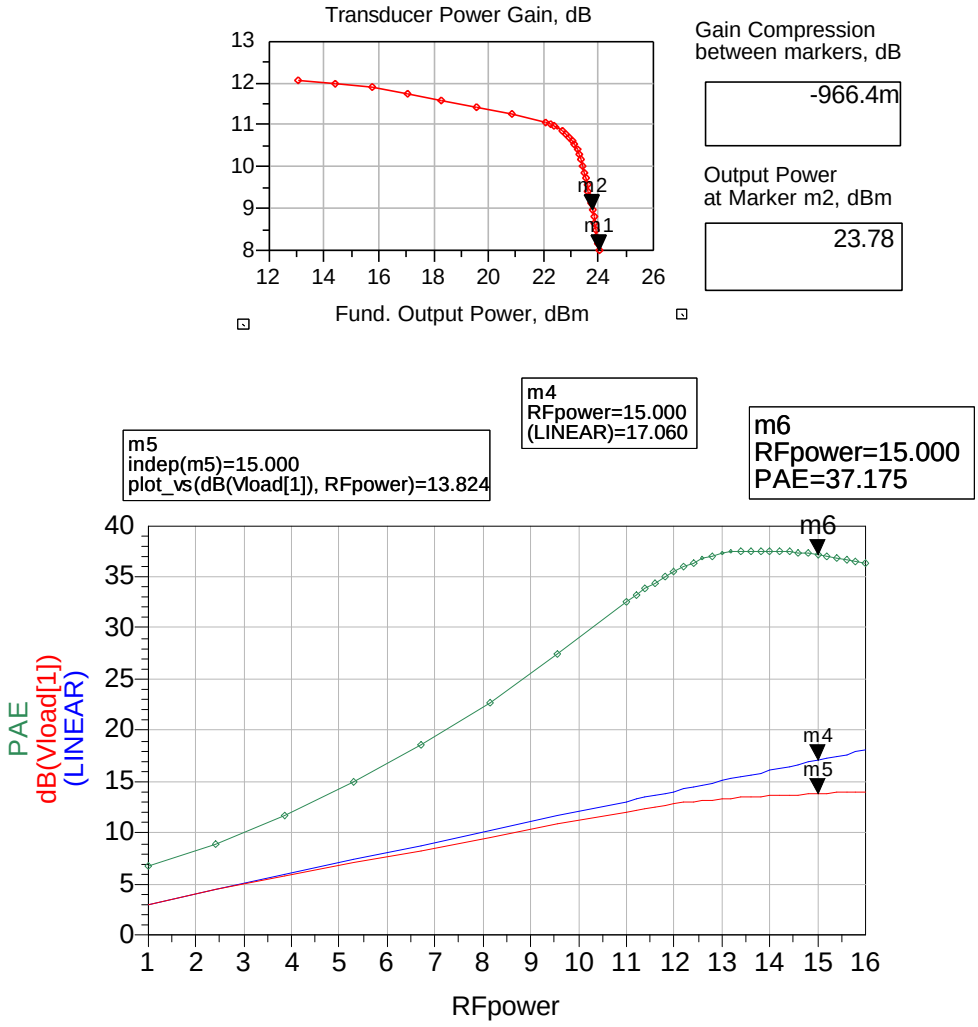


Figure 2
Pre – Layout large – signal responses. Power Added Efficiency, Output power at 1 dB compression point.

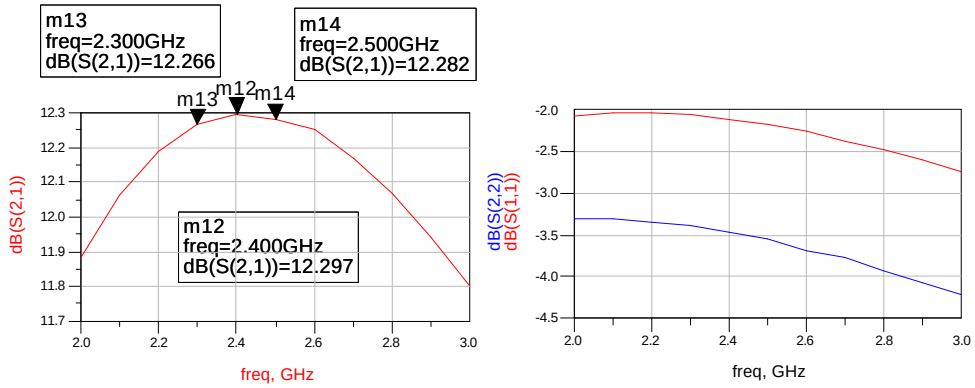


Figure 3
Post – Layout Small signal responses

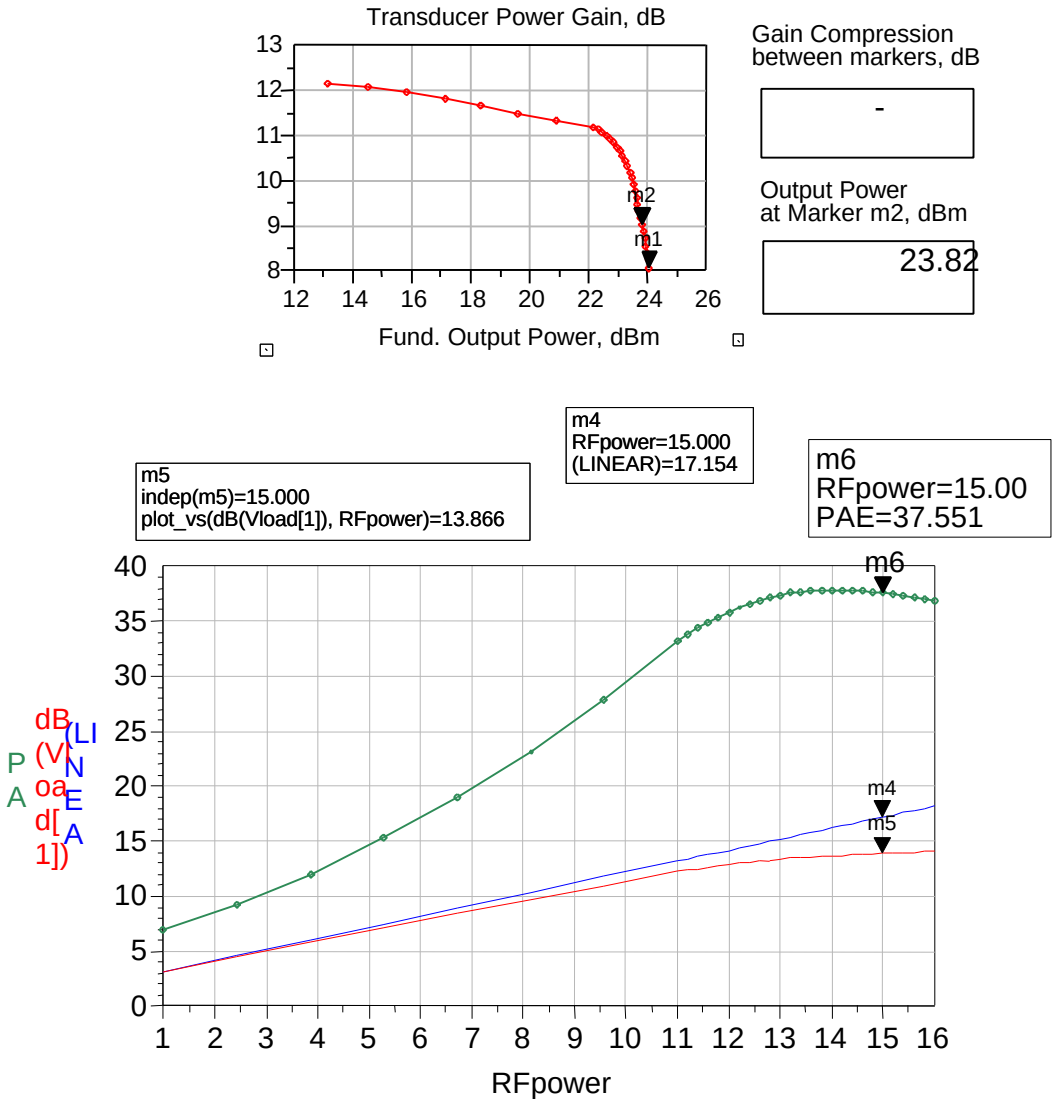


Figure 4
Post – Layout large Signal Reponses

Schematic Diagrams and Layout

Simplified Schematic (pre-layout)

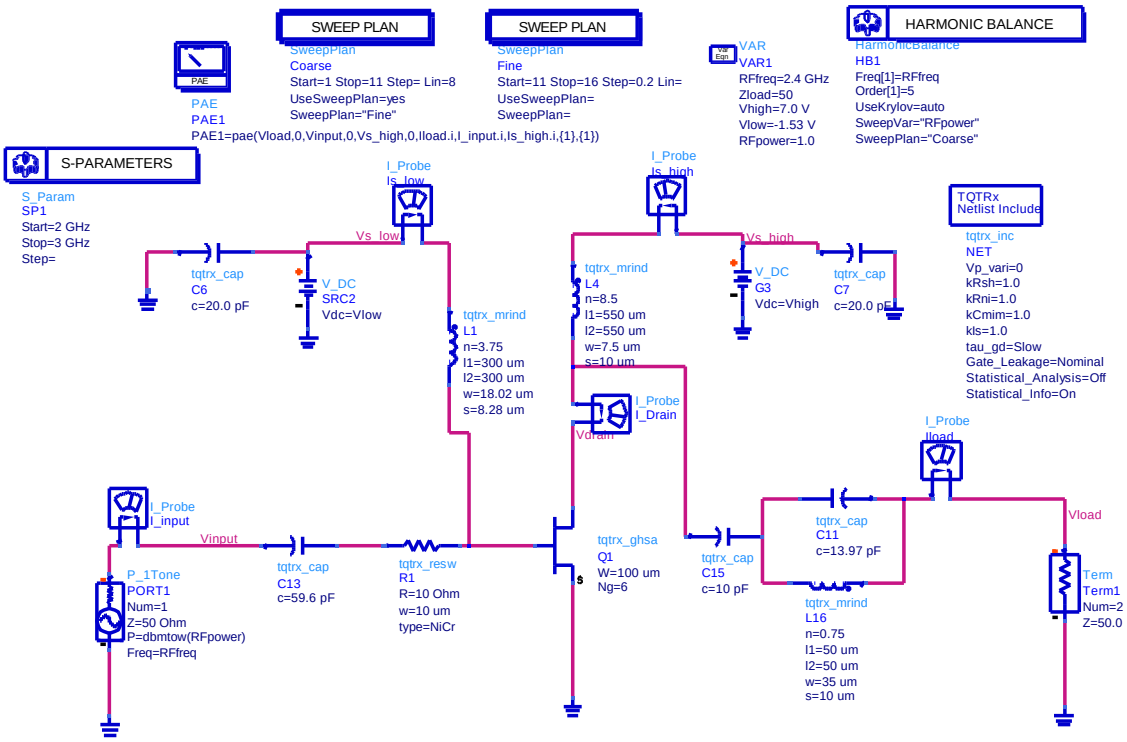


Figure 6
Schematic (post-layout)

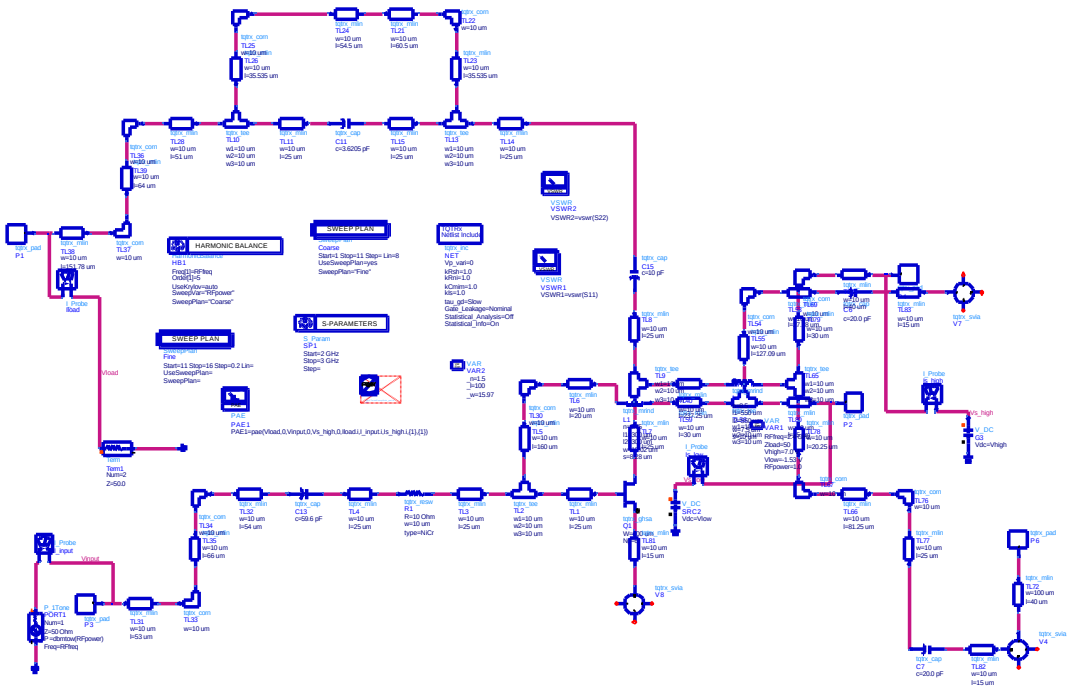


Figure 7

Final Layout

For this layout we tried to keep things simple and use as little space as possible.

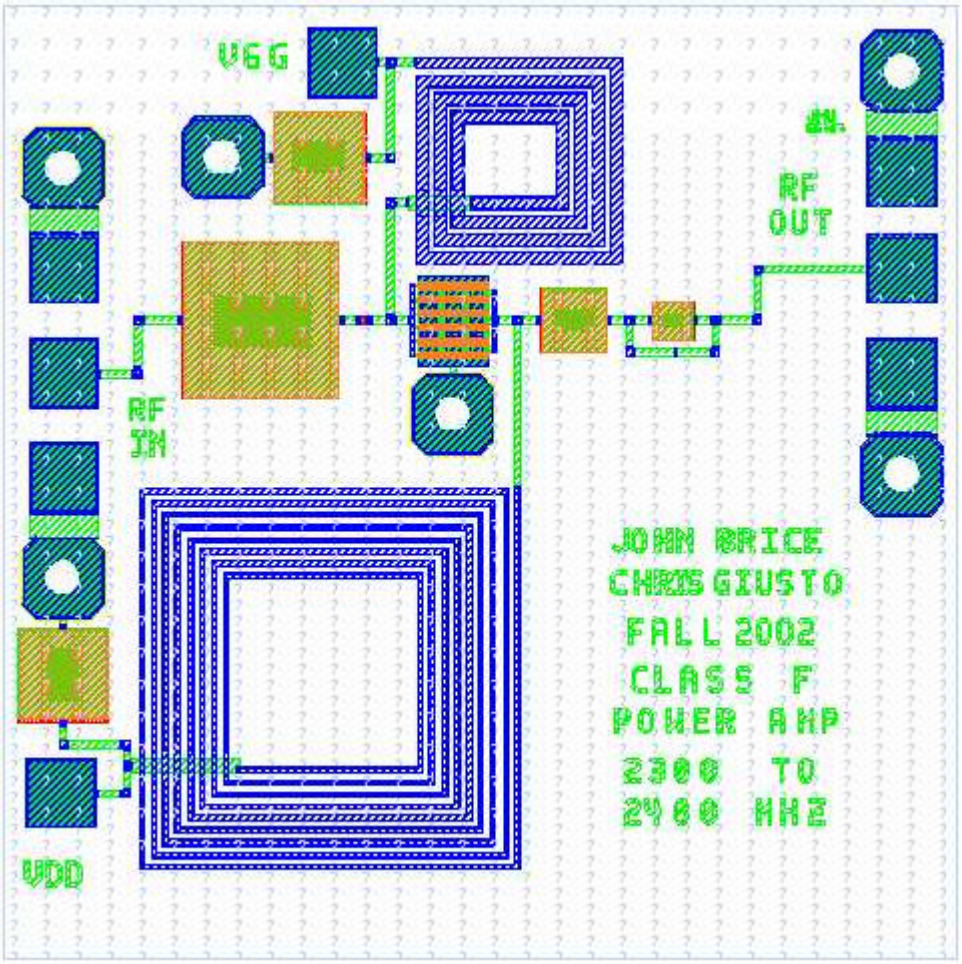


Figure 8

DC Analysis

The following shows DC schematic (simplified) with bias check.

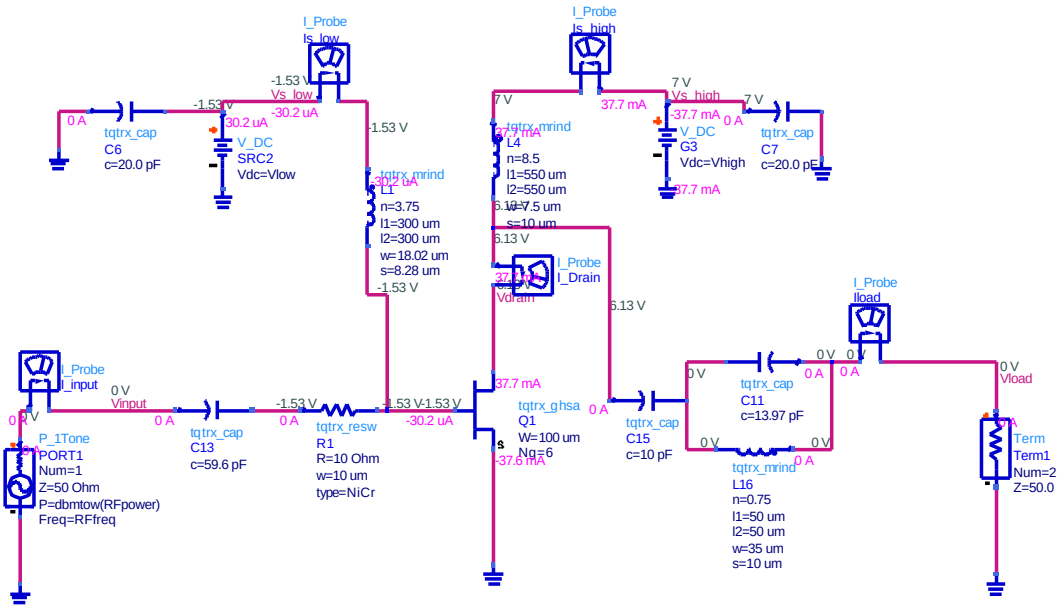


Figure 9

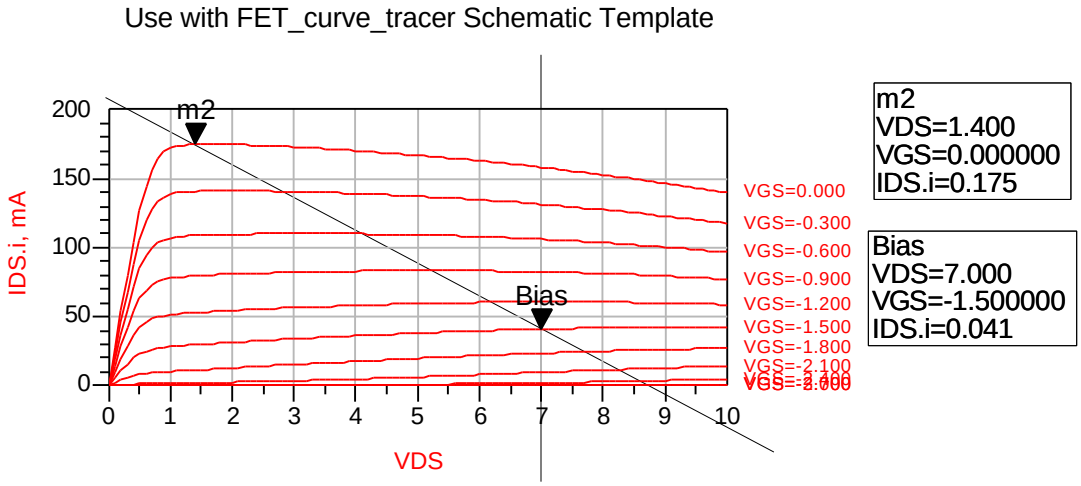


Figure 10

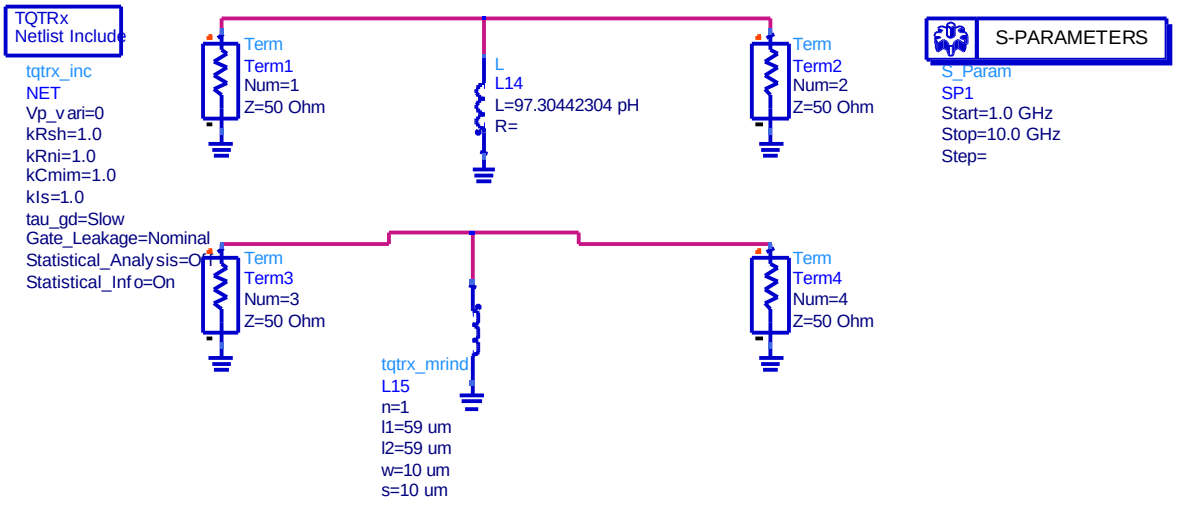


Figure 11

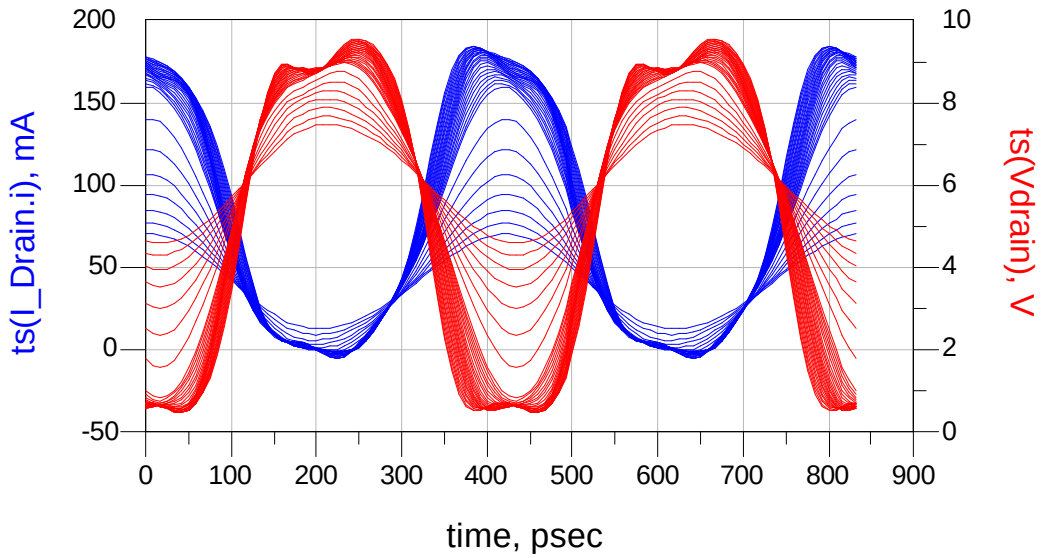


Figure 12

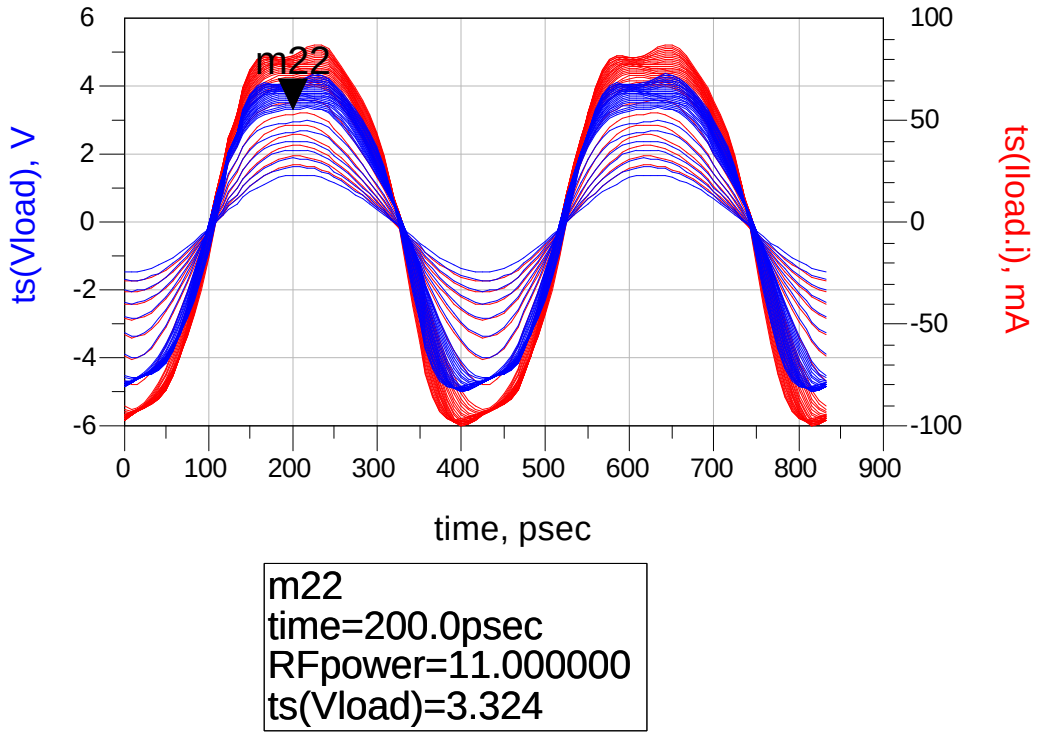


Figure 12 Output Waveforms

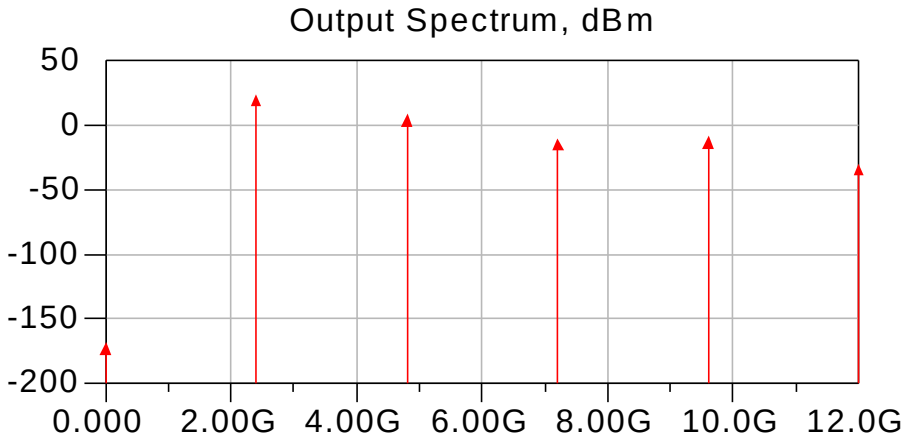


Figure 13 Output Spectrum

Test Plan

Use Cascade probe station to connect the probes to the RF in and RF out ground signal ground pads. Connect the 7 and –5 volt supplies to the VGG and VDD pads respectfully.

Use the VNA 8510 to measure all small signal data. Use a spectrum analyzer along with any needed power meters to measure the large signal aspects.

Conclusion

A class f power amplifier has been realized. Due to the chip size and trade offs all of the required specifications were not met. All of the specifications were met but those, which were not met, came reasonable close. The design was simulated, laid out and analyzed. The design does demonstrate classical class F characteristics and exceed our expectation for this project. This project allowed us to grow as RF MMIC designers.

References

Steven C. Cripps,"**RF Power Amplifiers for Wireless Communications**," Artech House, 1999, chapters 3, 5, 8.

Fredrick H. Raab, "**Maximum Efficiency and Output of Class-F Power Amplifiers**," IEEE transactions, Vol 49, NO.6, JUNE 2001, pp 1162-1166.

A.N. Rudiakova and V.G. Krizhanovski, "**Driving Waveforms For Class-F Power Amplifiers**,"IEEE MTT-S Digest, 2000, pp 473-476.

Moore, Craig and Penn, John. *Class Handouts.* JHU/APL. 2002.

MMIC Design Project
S Band Post Amplifier

By: Kerron Duncan and Walter T. Tates

Due Date: 12/09/02

EE525.787

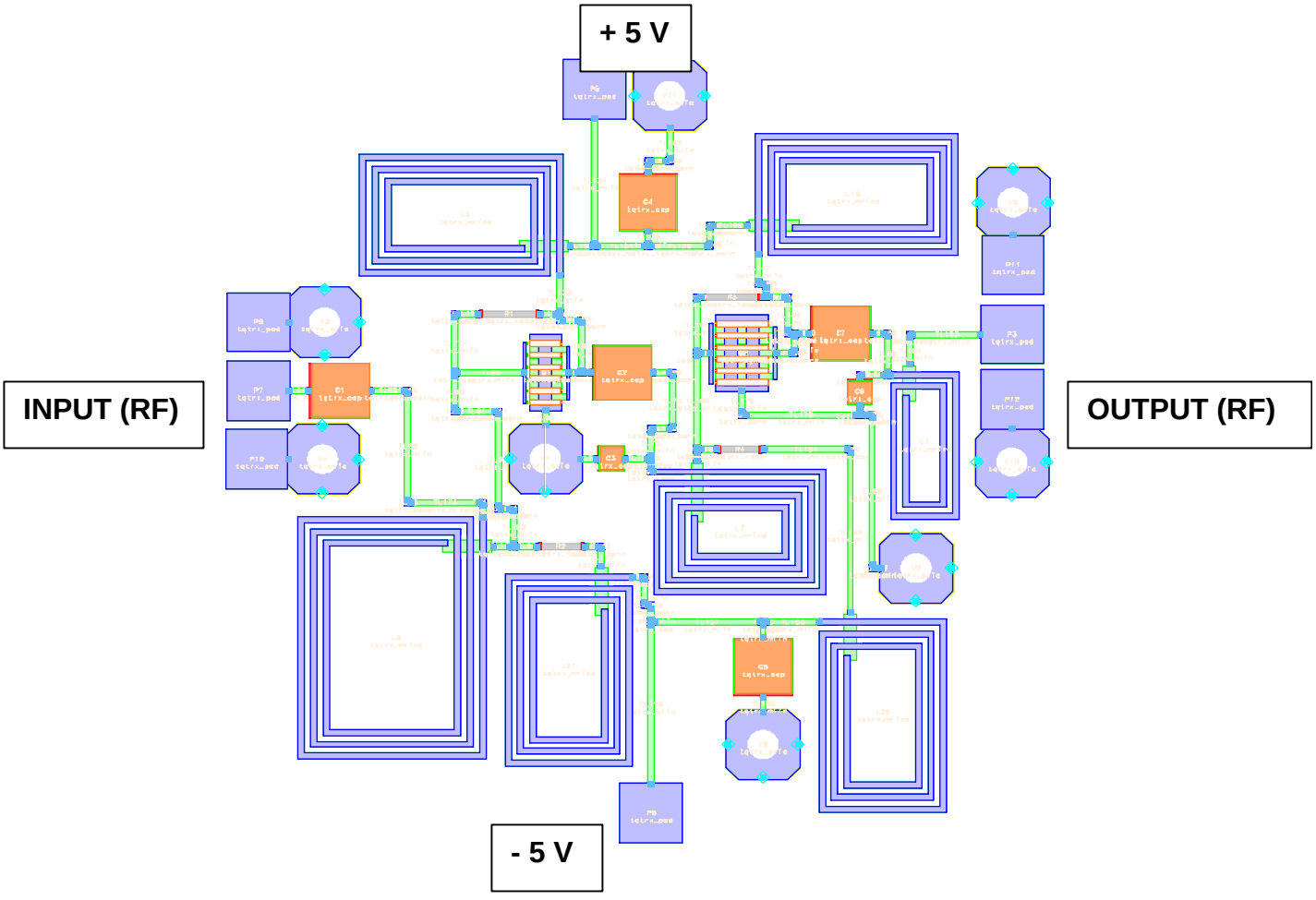
Table of Contents

Abstract

This report documents the design of a post amplifier for primary use at 2.4GHz and using the Triquint TRx process. The design was produced as part of the MMIC Design Course taught at Johns Hopkins University during the Fall 2002 semester.

The post amplifier was designed for use in an S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies.

The design software used to design the post amplifier was Agilent's Advanced Design System 2002C (ADS). The elements used were custom model elements based on Triquint process. The design was laid out on a 60 x 60 mil Anachip.



Introduction

Circuit Description
The circuit topology selected for the design was a cascaded two-stage amplifier layout, which requires two power supplies (of opposite polarity). The matching networks were designed using lumped element topology.

Design Philosophy
The design specifications of the post amplifier called for an emphasis to be placed on gain and IP3. In the early stages of this design, a series of ideal case design using both the GFET and DFET transistor models sized at 300 and 500 um. It was determined that the 500 um GFET was the optimal choice device for this sort of application. Due to the gain requirement of 12 dB or more, we decided to use 300 um for the first stage and a 500 um for the second stage.

The first step in designing the post amplifier was to determine where the device should be biased. This stage was made fairly simple by utilizing ADS's Amplifier=> DC and Bias Point Simulations => and FET IV Curves template. For maximum gain, we already had in mind that we wanted to bias the device at IDSS 1/2. By correctly using the template, we determined that we wanted to bias the first stage at:

Ids = Idss/2 = 83mA/2 = 41.5mA @ 5 V = Vds, 900 mV = Vgs
And the second stage at:
Ids = Idss/2 = 138mA/2 = 69mA @ 5 V = Vds, 900 mV = Vgs

The next step in the design was to determine the input and output matching circuitry for the first and second stages separately. With the Cripps method in mind, this was process was accomplished through the use of ADS's Amplifier=>S-parameter Simulations=> S-parameters, noise figure...etc template. Ideal elements were used for the first iteration of designs for each stage.

Upon completing the matching networks for each stage, both stages were optimized for optimal gain, output power, and return loss. The results were analyzed using both linear and nonlinear simulated data. The two separate stages were than combined and the overall performance of the amplifier is optimized. After satisfactory performance is obtained using the ideal elements in the combined two-stage design, the ideal elements are replaced by Triquint elements. Special attention was given to the Triquint inductors as have been shown to be lossier than ideal inductors.

The final stage of the design process was to shift the design from schematic in layout. The circuit was tweaked and placed element by element into the given 60 x 60 mil anachip frame. Microstrip lines, tees, and vias were substituted for there ideal counterparts.

Trade-offs

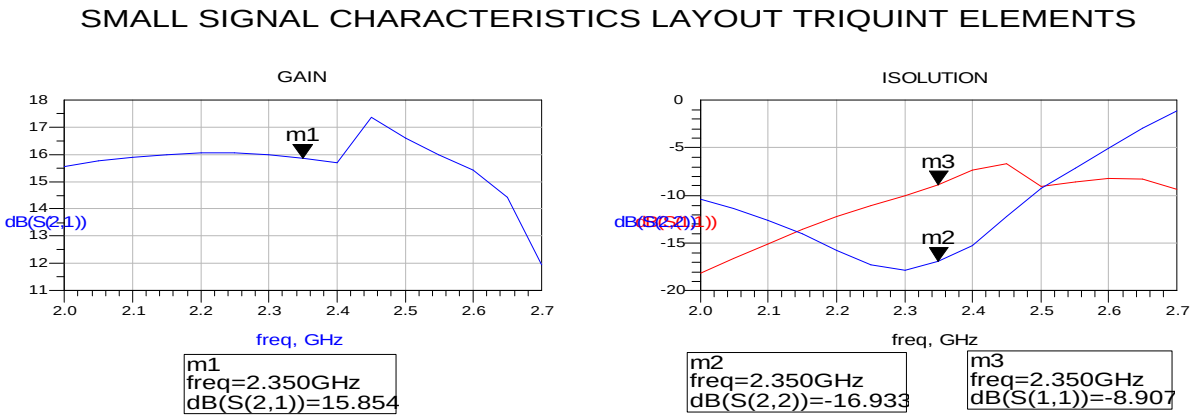
Two trade-offs considered in the design stemmed from the fact that the design was implemented using a dual-supply bias network. One trade-off considered in the design was that the correct sequencing of turning on/off power supplies was critical to avoid device burnout. Another trade-ff encountered in the design was that of space, since by utilizing two power supplies, we also had to add extra bias inductors.

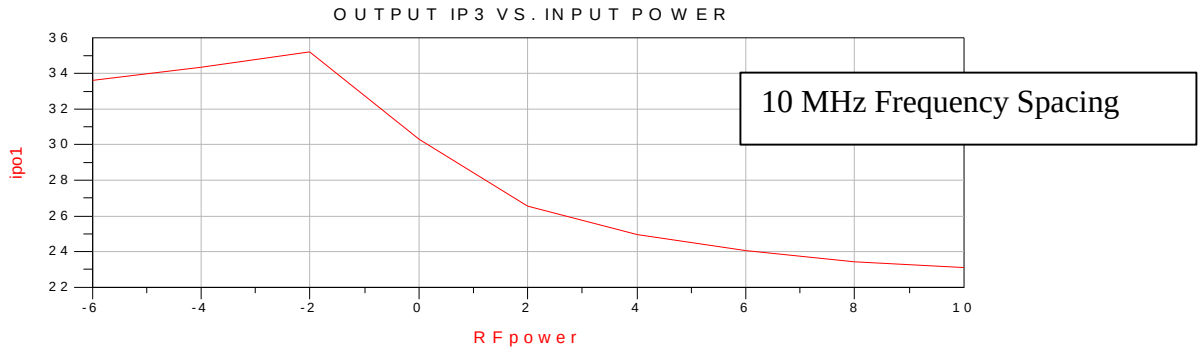
Modeled Performance

Specification Compliance Matrix

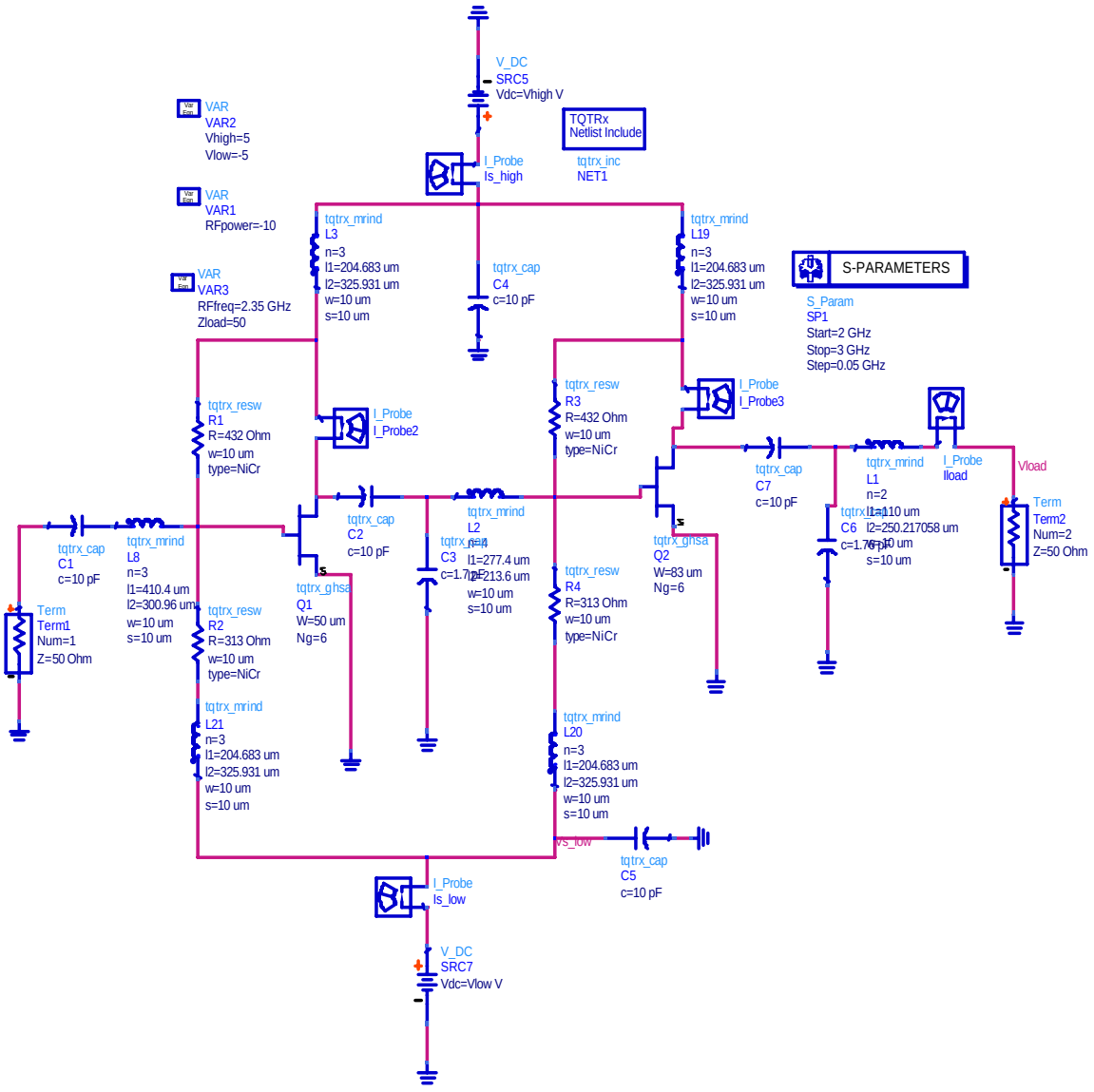
	Specification Goal	Triquint Elements Pre Layout	Final Layout Schematic
Frequency	2300 to 2500 MHz	2300 to 2500 MHz	2300 to 2500 MHz
Bandwidth	>200 MHz	> 700 MHz	> 700 MHz
Gain	>12 dB 15dB, Goal	> 15dB	> 15dB
Output IP3	> +20 dBm	> +22 dBm	> +22 dBm
VSWR, 50 Ohm	<1.5:1 input & output	1.51:input 1.8:1 output	2.1:1:input 1.3:1 output
Supply Voltage	+/- 5 Volts; +5 Volts Goal	+/- 5 Volts	+/- 5 Volts

Predicted Performance

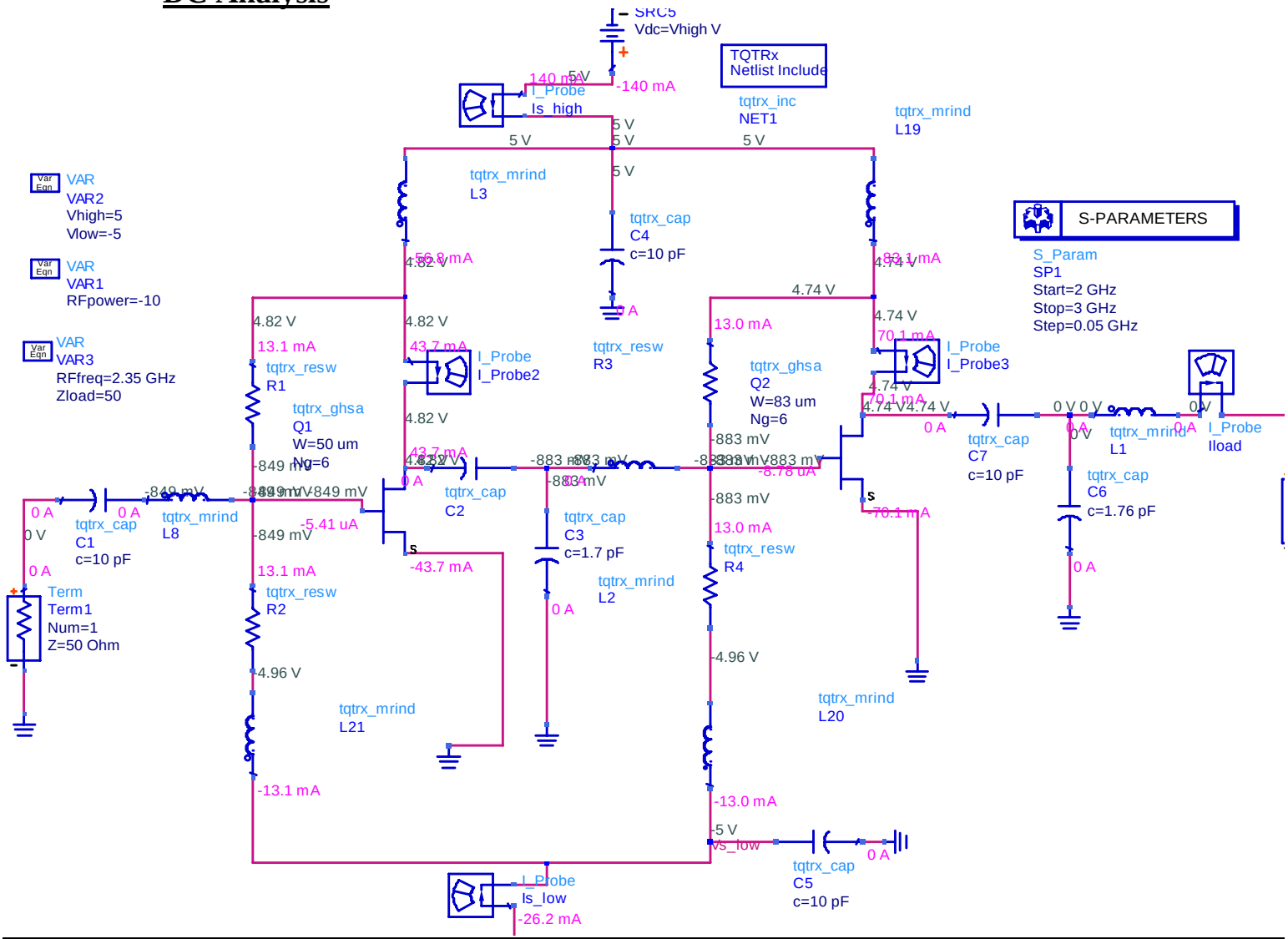




Schematic Diagrams



DC Analysis


SRC5
Vdc=Vhigh V
TQTRx
Netlist Include
tqtrx_inc
NET1
tqtrx_mrind
L19
I_Probe
Is_high
140 mA
-140 mA
5 V
tqtrx_mrind
L3
tqtrx_cap
C4
c=10 pF
VAR
VAR2
Vhigh=5
Vlow=-5
VAR
VAR1
RFpower=-10
VAR
VAR3
RFfreq=2.35 GHz
Zload=50
S-PARAMETERS
S_Param
SP1
Start=2 GHz
Stop=3 GHz
Step=0.05 GHz
4.82 V
56.8 mA
13.1 mA
tqtrx_resw
R1
tqtrx_ghsa
Q1
W=50 um
Ng=6
I_Probe
I_Probe2
43.7 mA
tqtrx_resw
R3
tqtrx_ghsa
Q2
W=83 um
Ng=6
13.0 mA
4.74 V
83.1 mA
70.1 mA
I_Probe
I_Probe3
tqtrx_cap
C7
c=10 pF
tqtrx_mrind
L1
I_Probe
Iload
tqtrx_cap
C6
c=1.76 pF
-849 mV
-883 mV
-5.41 uA
-8.78 uA
-43.7 mA
-70.1 mA
tqtrx_cap
C2
tqtrx_cap
C3
c=1.7 pF
tqtrx_mrind
L2
tqtrx_resw
R4
-4.96 V
tqtrx_cap
C1
c=10 pF
tqtrx_mrind
L8
Term
Term1
Num=1
Z=50 Ohm
tqtrx_mrind
L21
tqtrx_mrind
L20
-13.1 mA
-13.0 mA
-5 V
Vs_low
tqtrx_cap
C5
c=10 pF
I_Probe
Is_low
-26.2 mA

Test Plan

The following items and test procedures are recommended to test the S-band post amplifier

Linear Parameters

Equipment: Vector network analyzer (Agilent 8510)
Probe Station
Bias Supplies

Procedure:

- Calibrate the network analyzer from 0.45 to 10 GHz
- Place the bias probe on the pad of the chip labeled “5V” and “NEG5V”.
- Place probe tips on the designated pads. The input port is labeled “IN” and the output port is labeled “OUT”.
- Turn on the two power supplies.
- Record data.

Power measurements

Equipment: Signal Generator
Spectrum Analyzer

Procedure:

- Connect the signal generator probe to the input pad of the amplifier chip, which is the port marked “IN”.
- Connect the spectrum analyzer probe to the output pad of the amplifier chip which is the port marked “OUT”.
- Place the bias probe on the pad of the chip labeled “5V” and “NEG5V”.
- Power supplies.
- For Pin vs. Pout set the generator to the frequency of interest and sweep the power up to, but not exceeding, 10 dBm.
- Record measurements from spectrum analyzer after each interval.

Conclusion & Recommendations

In conclusion, we noted that we could have optimized one stage for VSWR and weighted this goal a little more than the others possibly. However, it would have involved a trade-off in gain (or noise figure). Finally, a more thorough Monte Carlo analysis could have been done in order to make the design more robust and less dependent on device variation.

WCS Band Frequency Doubler Design

Using Triquint TQTRx Process

by

Ming-Zhi Lai

December 2002

JOHNS HOPKINS UNIVERSITY
EE525.787 MMIC Design
Instructors:
C. Moore, J. Penn

Abstract

WCS BAND FREQUENCY
DOUBLER DESIGN

by Ming-Zhi Lai

A balanced frequency doubler MMIC design is presented in this report. Given the performance requirements, the doubler was designed utilizing Agilent's Advanced Design System (ADS) package bundled with Triquint TQTRx design kit, and was laid out on a 60 x 60 mil Anachip. Along with other designs for the MMIC design class, the frequency doubler will be part of a chip set for use in the WCS band transceiver application.

TABLE OF CONTENTS

1 INTRODUCTION

1.1 Circuit Description

The designed frequency doubler will work at the LO port in the applications operating under Wireless Communication Service (WCS) band, which is from 2305 to 2360 MHz. The doubler's input frequency ranges from 1070 to 1170 MHz, and output from 2140 to 2340 MHz.

The schematic consists of three parts, which are the 180-degree hybrid, the multipliers, and the output stage amplifier. The 180-degree hybrid provides two output signals, with 180-degree phase difference to each other, feeding to the frequency multipliers.

The multiplier is a GFET biased at the point close to the pinch-off region of the FET DC IV curve. Operating at this bias point can generate strong second harmonic frequency output, and yet keep the higher order frequencies low in magnitude.

Due to the balanced configuration of design, combine the multiplier outputs from both branches will ideally eliminate all the odd-order harmonic frequencies. The second harmonic frequency, along with other weak higher-even-order components, will be boosted to the desired output power level by the last stage amplifier.

1.2 Design Philosophy

1.2.1 180 Degree Hybrid

In the beginning phase of the project, there are several approaches to design the frequency doubler. One of them is to drive the multiplier hard to generate harmonic components and the filter out unwanted frequencies. The balanced configuration was adopted because it has the advantage of the simplicity of the

circuitry, since the filter stage design could be bypassed. Due to the size limitation of the anachip and the low operating frequency, the width and line spacing of the spiral inductors in the hybrid has decreased half to 5 um to minimize the size and save the chip space. This results in more resistance in the Triquint inductors, and creates more attenuation of the signal. More amplification at the output stage is therefore required to compensate the loss here.

1.2.2 Class AB Amplifier (Multiplier)

The 600 um (100X6) GFET was chosen for use in the multiplier because of its power handling capability and ability to generate stronger second harmonic frequency. The GFET is biased at Vgs=-2V and Ids=10mA, which is very close to the pinch-off region. A 200 ohm shunt resister at the input side is introduced to provide a connection point for the bias voltage, Vgs.

1.2.3 Output Stage Amplifier

The output stage utilizing another 600 um (100X6) GFET, no input matching network since this transistor already has –10 dBm S11 without any matching circuitry, which is already sufficient for our application. Output matching network has been designed to have better output VSWR, since the output power, by specification requirement, is not high (0 dBm), and with the VSWR optimized OMN, this amplifier has a very high power compression point already..

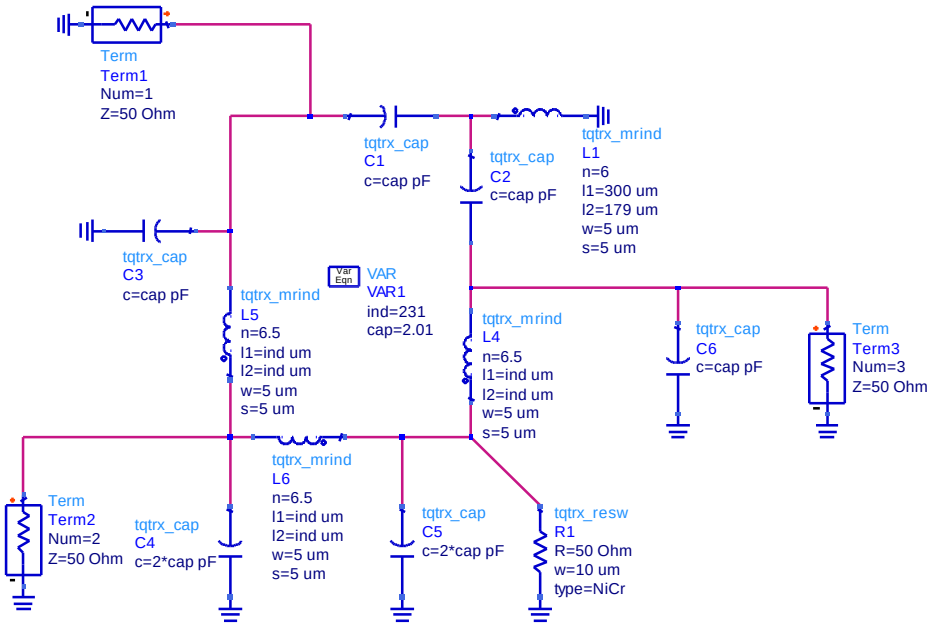
1.3 Trade-Offs

The first trade-off I have encountered in the project is the size of the hybrid and the loss. Due to the relatively low frequency, the size of the hybrid would be very remarkably large. With limited space in Anachip, I have to compromise the loss with the space. In this design project, the loss is two more dB, which can be easily compensate by either the class AB amplifier or the output stage amplifier.

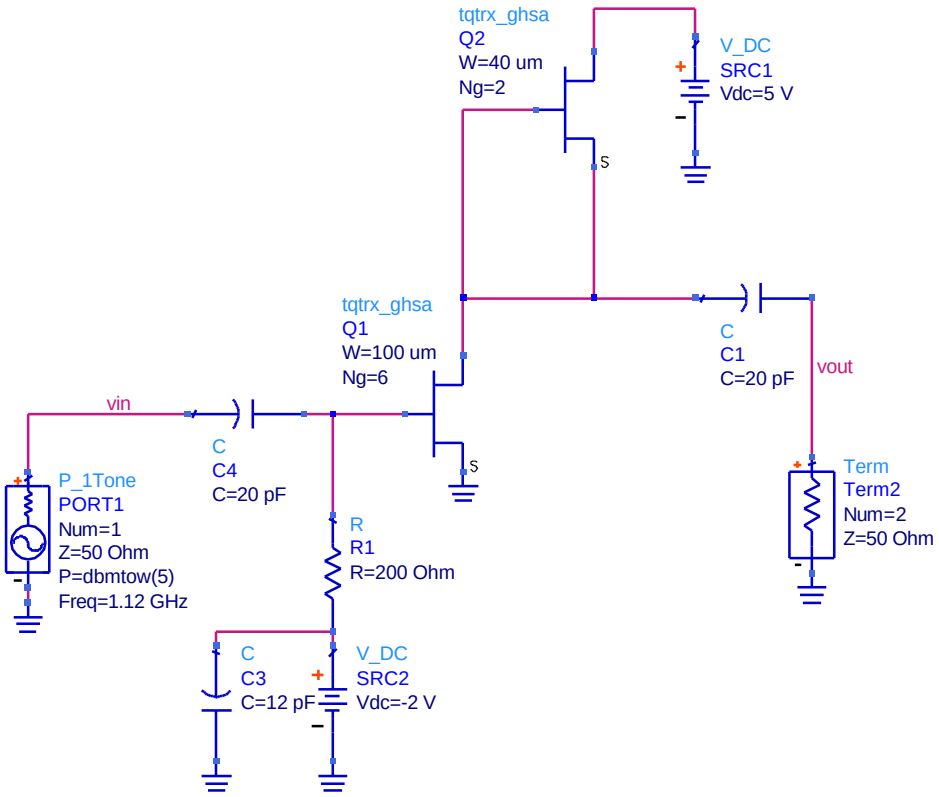
Second would be the trade-off between the power gain and the current. Worries about the loss in the hybrid make me try to achieve higher power gain at both the class AB amplifier and the output stage amplifier by using larger GFET (600 um). This became to be very rewarded in return, with +10 dBm input, this frequency doubler could achieve +17 dBm output, which is way over the requirement and failed the specifications. At the same time, the current in the design became very large, such as in the output stage amplifier, and bias current Ids=110 mA.. As the result, I should compromise with the gain performance, since the overall requirement is not hard to achieve.

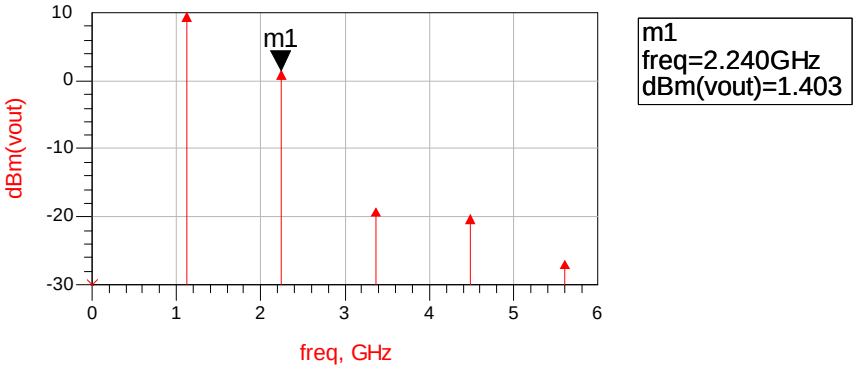
2 SCHEMATIC DIAGRAMS

2.1.1 180 Degree Hybrid Schematic



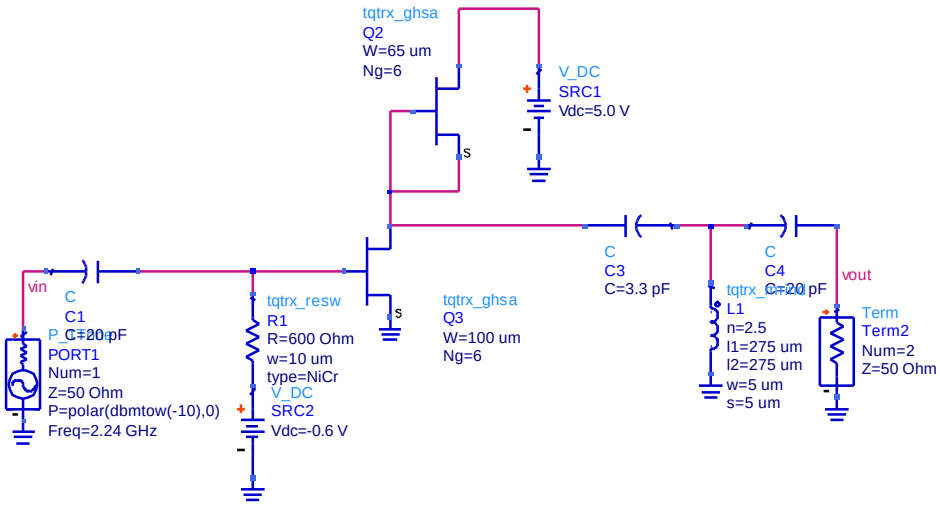
2.1.2 Class AB Amplifier Schematic





the class AB shows very good second order harmonic frequency output, at the same time, the higher order harmonics still have at least 30 dBc compression compare to the fundamental frequency.

2.1.3 Output Stage Amplifier Schematic



the 600 um (100 x 6) GFET with the active 390 um (65 x 6) GFET load, which providing 109 mA Ids to have the output stage working as a linear class A amplifier. Note that there is a stabilized 600 ohm shunt resister on the input side, and the OMN here is not to optimize output power performance, but just to achieve better output VSWR.

3 MODELED PERFORMANCE

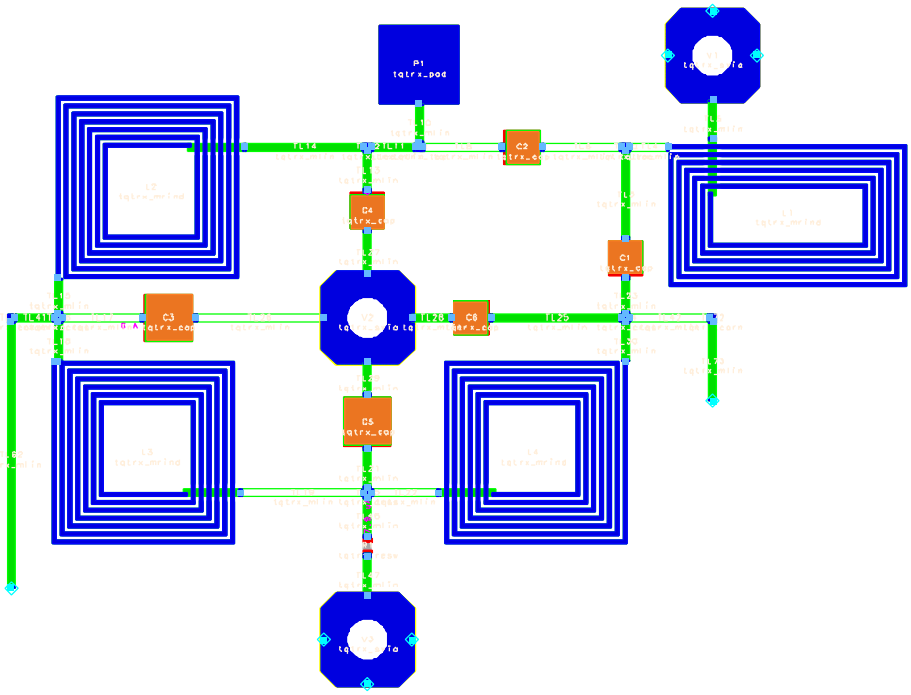
3.1 Specification Compliance Matrix

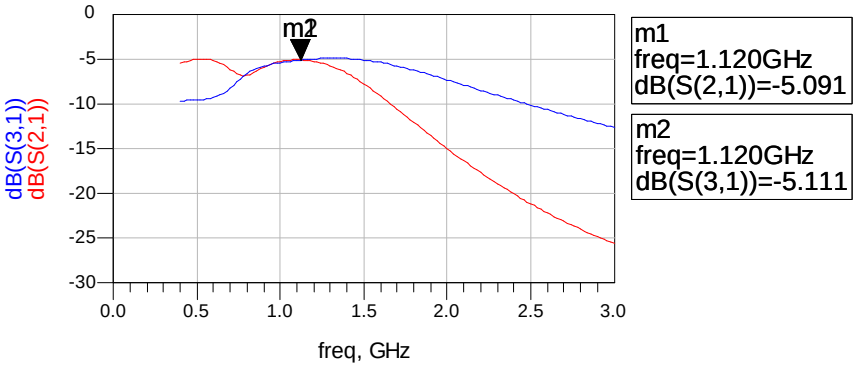
The compliance matrix summarizes all the design parameters and requirements of the frequency doubler.

	Specification	Simulation Result
Input Frequency	1070 – 1170 MHz	
Output Frequency	2140 – 2340 MHz	
Conversion Loss	3 dB max., 0 dB goal	
Input Power	+10 dBm	
Spurious – Fundamental	16 dBc min., 25 dBc goal	
Spurious – Third	20 dBc min., 30 dBc goal	
VSWR (50Ω)	2.5:1 max., 1.5:1 goal	
Supply Voltage	± 5 Volts, goal: +5 V only	
Size	60 x 60 mil Anachip	

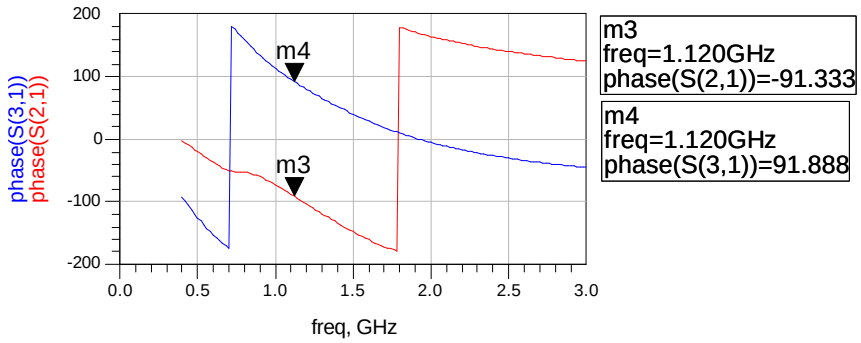
3.2 Predicted Performance

3.2.1 180 Degree Hybrid Performance

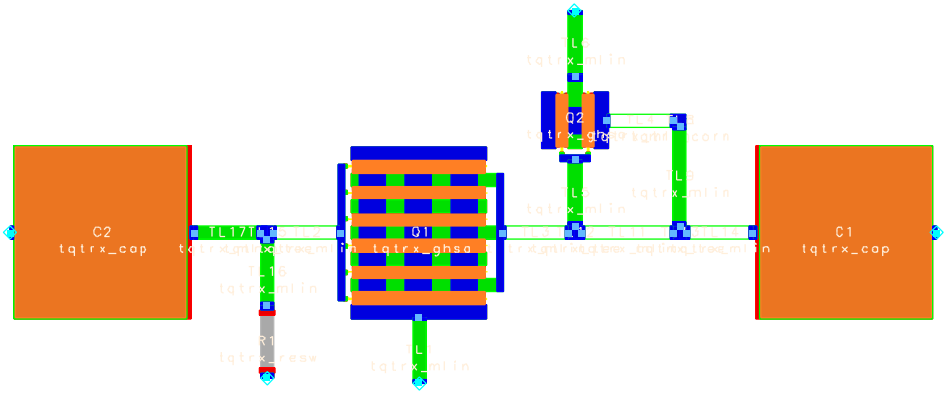


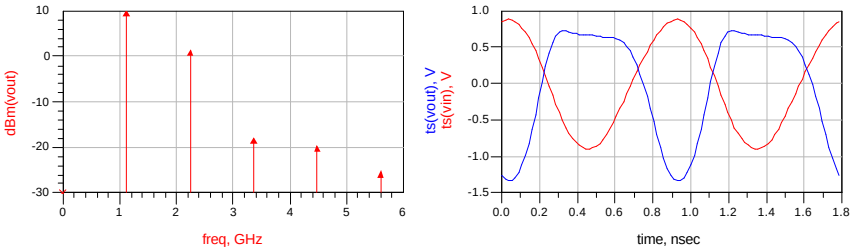


using the smaller width and line spacing inductors turns out to have more resistance and therefore, the output of the hybrid becomes more lossy. The phase difference is also off by 2 degree.

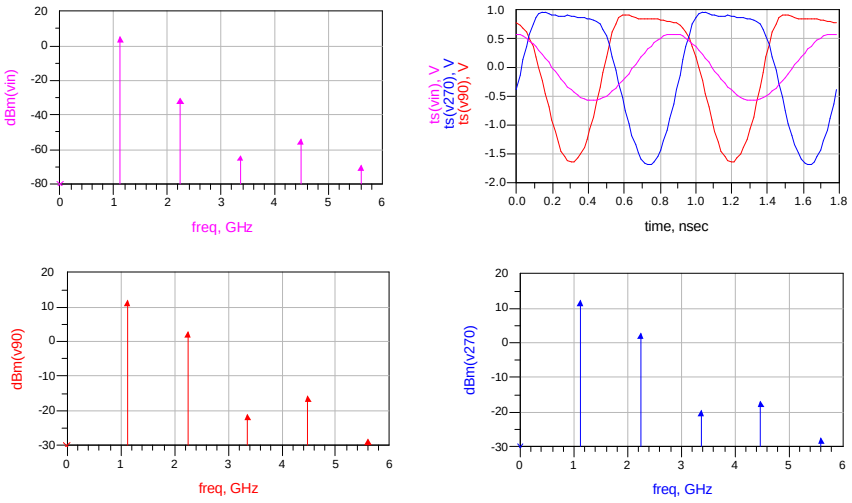


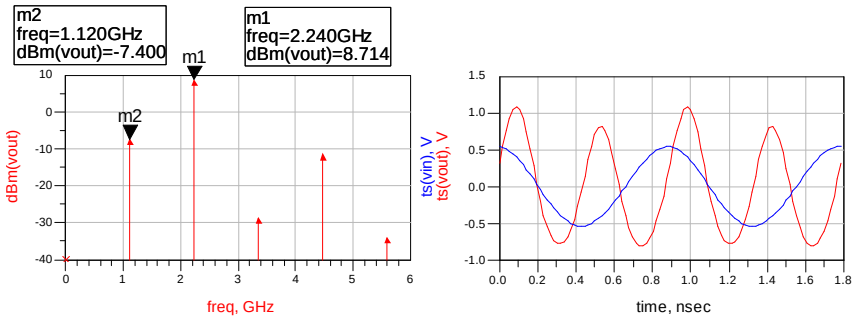
3.2.2 Class AB Amplifier Performance





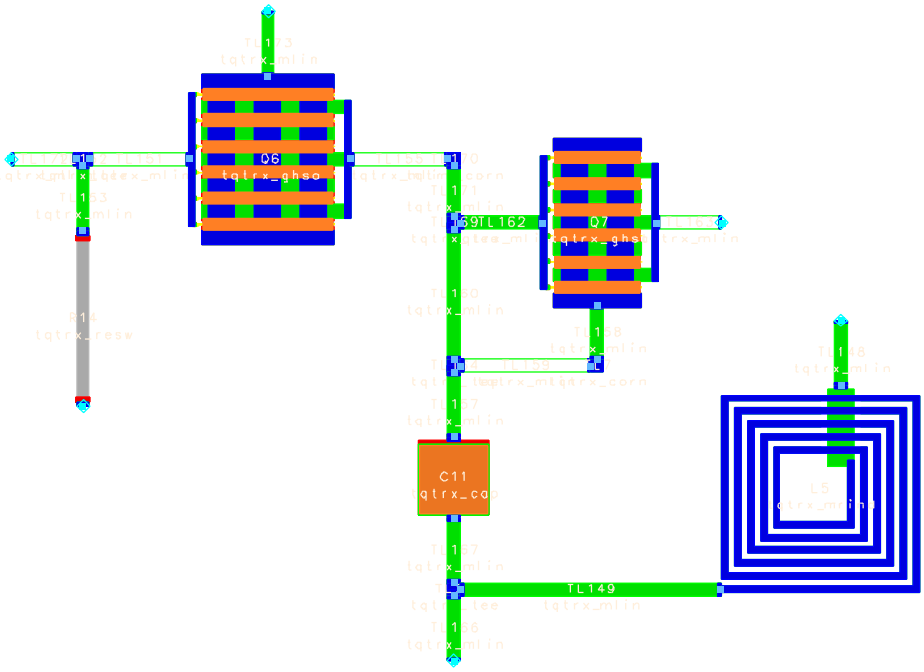
Connect the 180 degree hybrid and the two class AB amplifiers: v90 and v270 are the outputs from two branches.

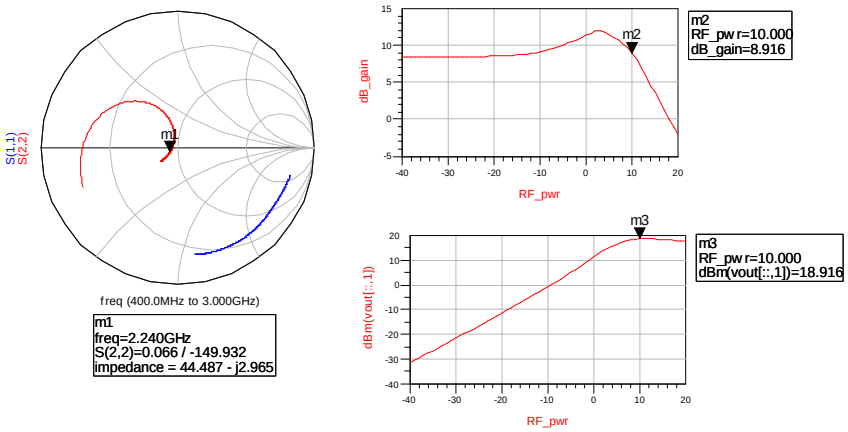




Combine the outputs of the two class AB amplifiers, all odd-ordered harmonics should be canceled, however, in out design and simulation, due to the slight mismatch of the two outcomes, there will be some considerable amount of the fundamental frequency that will feed into the output stage amplifier.

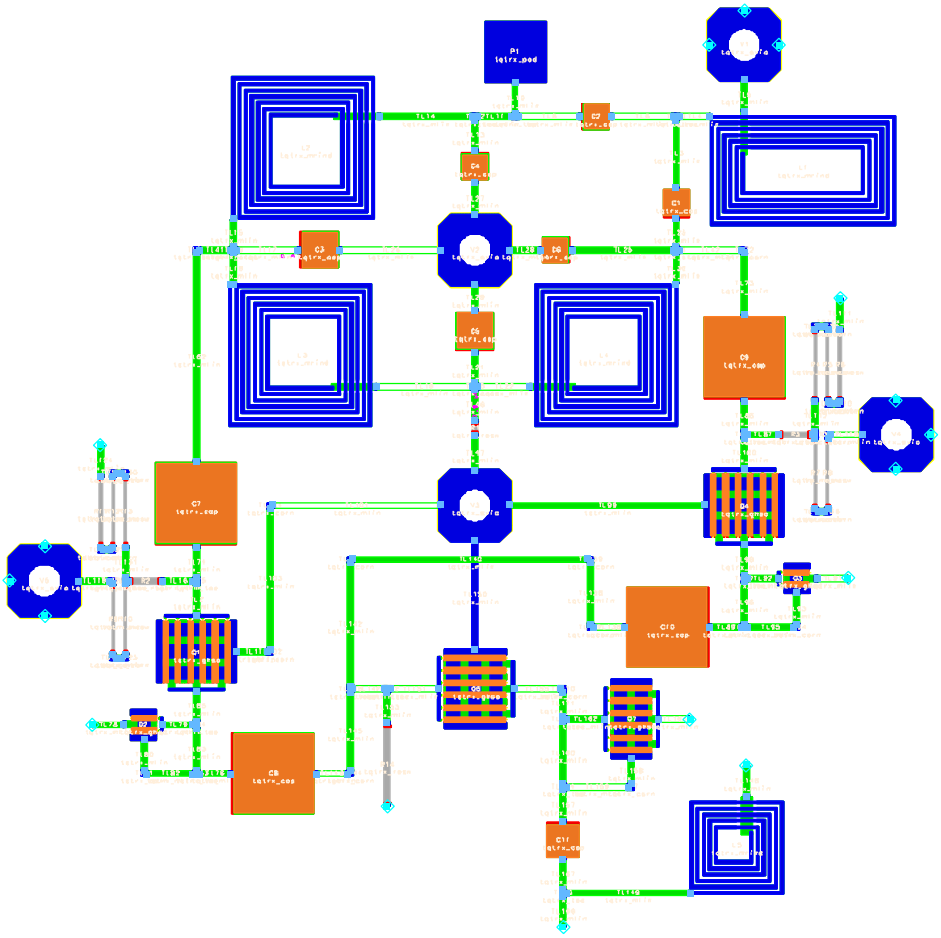
3.2.3 Output Stage Amplifier Performance

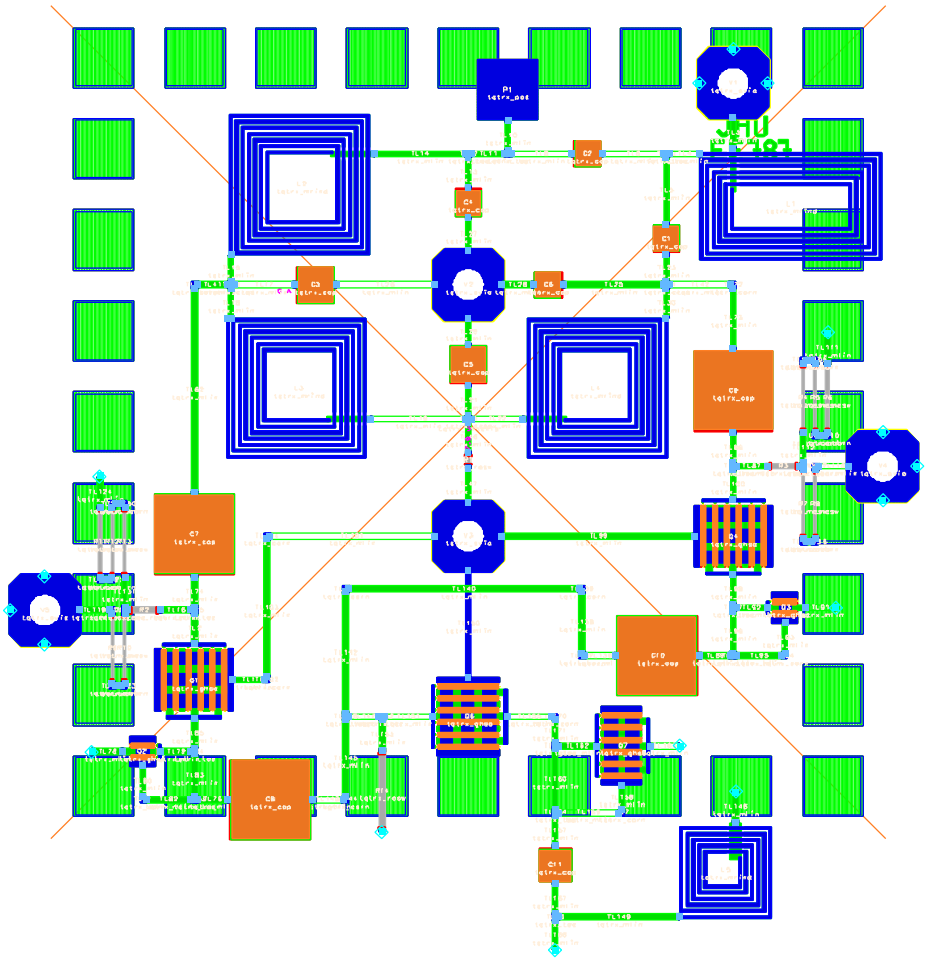


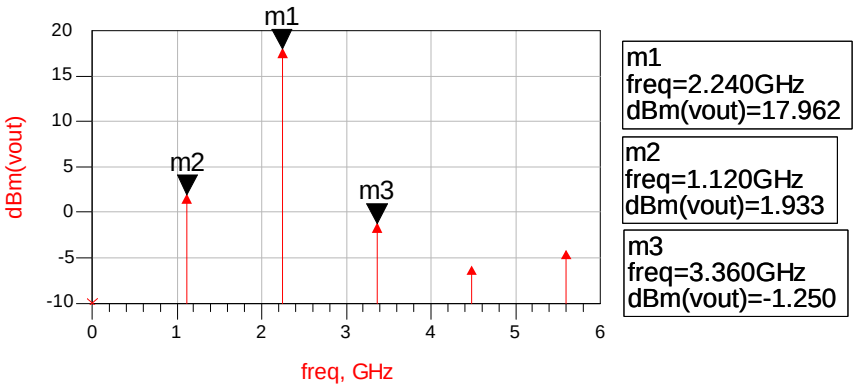


the output stage has very good output VSWR and the input P1dB is at 10 dBm, and can handle the power up to 18.9 dBm.

3.2.4 The Frequency Doubler

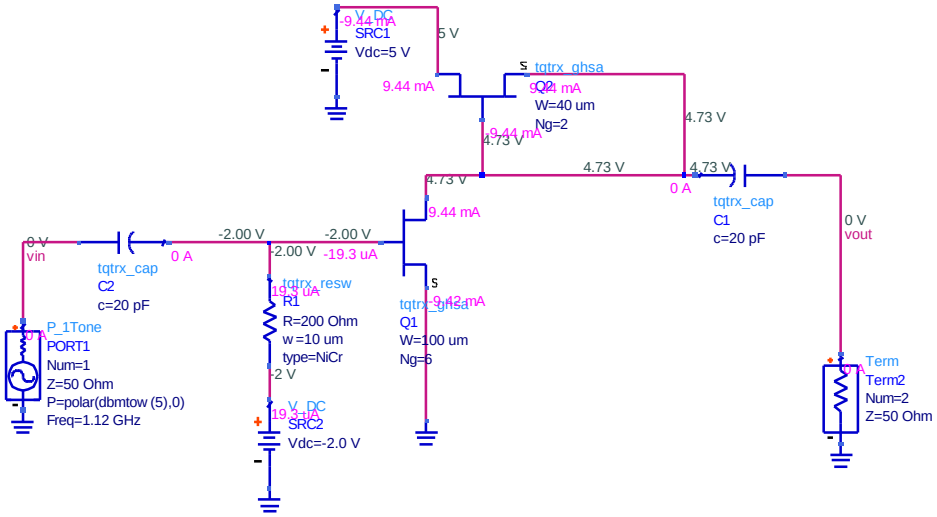





m1
m2
m3
20
15
10
5
0
-5
-10
dBm(vout)
0
1
2
3
4
5
6
freq, GHz
m1
freq=2.240GHz
dBm(vout)=17.962
m2
freq=1.120GHz
dBm(vout)=1.933
m3
freq=3.360GHz
dBm(vout)=-1.250

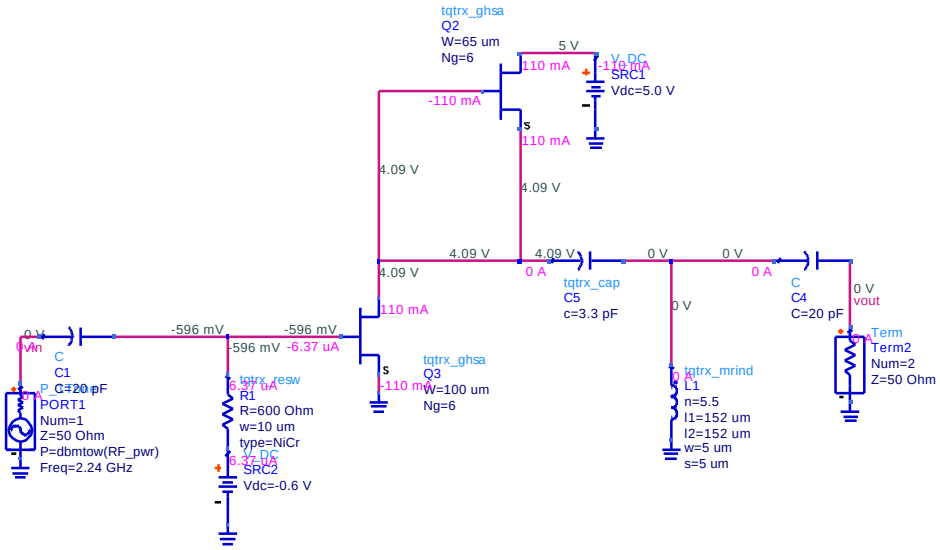
4 DC ANALYSIS

4.1 Class AB Amplifier



the 600 um GFET is biased under Ids=9.44 mA, Vgs=-2V

4.2 Output Stage Amplifier



the 600 um GFET is biased at Ids=110 mA, and Vgs=-0.6 V.

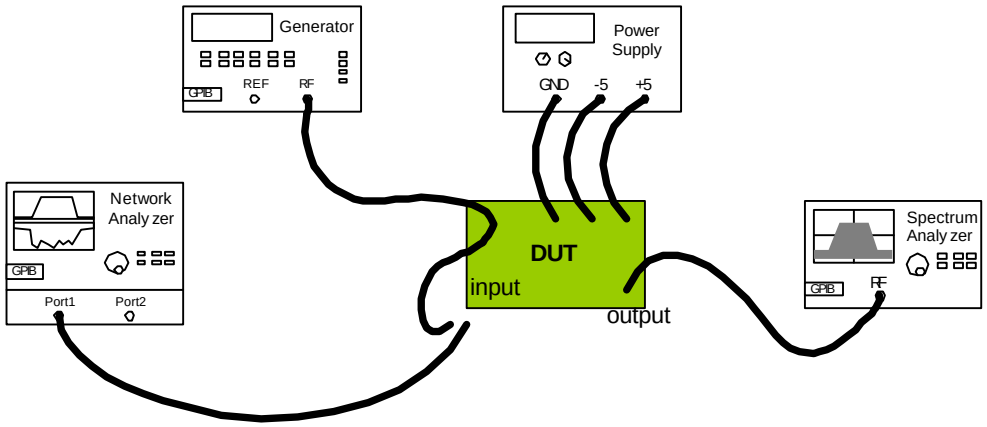
5 TEST PLAN

This section of report outlines the test plan and setup configuration to evaluate the fabricated chipset.

5.1 Test Equipment

Test Equipment	
Wafer probe station	1
RF signal generator	1
Spectrum analyzer	1
Network Analyzer	1
DC power supply	1
Digital multi meter	1

5.2 Test Setup



5.3 Test Procedures

1. Mount the DUT chip on the probe station, apply DC voltage (± 5V).

2. Input +10 dBm signal, frequency 1070 MHz, 1120 MHz, and 1170 MHz (B, M, T), measure the output power with spectrum analyzer, read and record the values at 2140 MHz, 2240 MHz, and 2340 MHz, respectively.

3. Input +10 dBm signal, frequency 1120 MHz, measure the output power with spectrum analyzer, read and record the values at 1120 MHz, 2240 MHz, and 3360 MHz, respectively.

4. Using network analyzer, measure the input VSWR/ input return loss.

5. Refer to section 3.1 for test specifications.

6 CONCLUSION AND RECOMMENDATION

The choice of using the balanced design with 180 degree hybrid turned out to simplified the circuitry a lot. However, the hybrid itself would take as much as space as the filter stage would take.

More improvement could be done easily done, due to time constraint, I could only work on the design after the submit ion of the report:

1. I've over estimated the effect of the lossy hybrid. The class AB amplifier and the output stage could be redesigned, to reduce the operation current and at the same time, meet the gain requirement.

2. The DC bias circuitry could be redesigned and achieve the goal of using only one DC supply.

3. The input VSWR could be tuned to have better performance.

4. The spurious performance can be optimized by tuning the two output branches of our design.

Course No	Course Name			Page
525.787.91	Monolithic Microwave Integrated Circuit Design			1(23)
Prepared By	*Email*	*Phone*	*ID*	*Date*
Mark F. Petty	mark.petty@erols.com	410-647-6793		12/08/02
Instructors	*Email*	*Phone*	*T.A*	*Final Project*
Craig Moore	craig.moore@jhuapl.edu	443-778-5920	Nathan Richardson	1.12 GHz
John Penn	john.penn@jhuapl.edu	443-778-6814	n8lrich@apl.jhu.edu	VCO

An Initial Swing at Controlled Instability

An
L - Band VCO

Center Frequency = 1120 MHz
Bandwidth = 100 MHz

A Student Project Designed By
Mark F. Petty

For
The Johns Hopkins University – Applied Physics Laboratory
Class # 525.787 - Monolithic Microwave Integrated Circuit Design

Instructors:
Craig Moore
John Penn

Fall 2002

Prepared By	Email	Phone	ID	Date
Mark F. Petty	mark.petty@erols.com	410-647-6793		12/08/02
Instructors	*Email*	*Phone*	*T.A*	*Final Project*
Craig Moore	craig.moore@jhuapl.edu	443-778-5920	Nathan Richardson	1.12 GHz
John Penn	john.penn@jhuapl.edu	443-778-6814	n8lrich@apl.jhu.edu	VCO

ABSTRACT:

This paper describes an L-Band voltage controlled oscillator, VCO, designed for a student's semester final project for the Johns Hopkins University, Monolithic Microwave Integrated Circuit, MMIC, class # 525.787. This VCO is one of several student designs used to form a "Wireless Communications Service", WCS, system or an "Industrial, Scientific and Medical", ISM, system. The computer aided design, CAD, tools used for this project include Agilent's Advanced Design System, ADS, version 1.5, and MathWork's Student Edition of Matlab release 12. The VCO's target of fabrication is TriQuint Semiconductor's Texas 0.6 μm Gallium Arsenide fab. TriQuint provided the device library used to describe the circuit elements within the VCO. The VCO requirements include: a center frequency of 1170 MHz; a tuning range of +/- 50 MHz; minimum output power of +10dBm, desired output power of +13dBm; supply voltage of +/- 5 volts, desired supply voltage of + 5 volts only; frequency tuning voltage of 0 – 5 volts; output impedance of 50 ohms, nominal; sized to fit on the 60 x 60 mil TriQuint ANACHIP.

INTRODUCTION:

Sustained oscillation results from, in short, an unstable amplifier. Since the amplifier circuit is a basic building block of electrical circuitry, much work has been performed to predict and prevent the instability of amplifiers. Pozar [1] discusses the derivation of stability circles for the input and output ports of networks, and the "K and Δ" stability parameters. The S-Parameter derived K and Δ stability parameters are further messaged into centers and radii for source and load stability circles, which are then plotted on Smith Charts. Edwards [2] developed the μ, and μ', stability parameters which allowed for the direct comparison of the stability in designs. Figure 1 illustrates the common problem of amplifier design, the last piece of the design, the output matching network, OMN, yields a reflection coefficient in the unstable region.

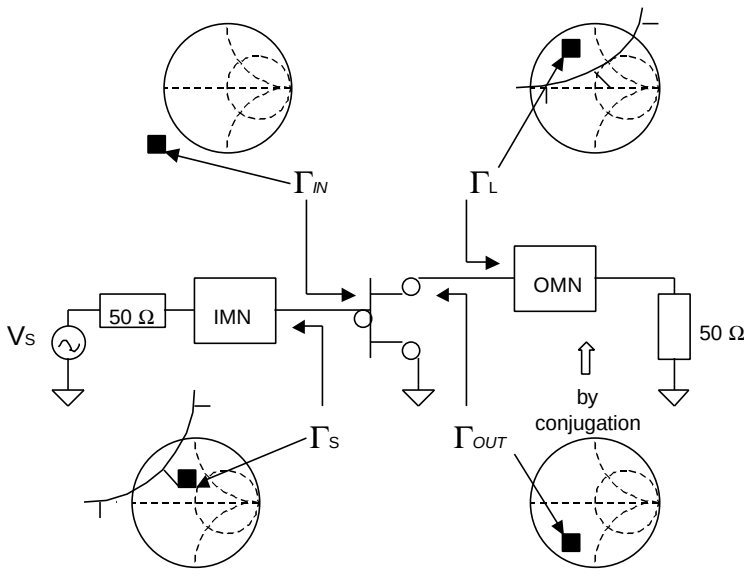


Figure 1. Illustration of the stability problem in designing an amplifier. Tick marks designate stableside of stability circles. Redrawn from Edwards [3].

So, to design an oscillator, simply design an amplifier with an input and/or output reflection coefficient in their corresponding unstable region. Unfortunately it is not that easy. Remember, the above example was designed from the start to yield a stable amplifier, and it resulted in a possible oscillator. Yet, that is still the core of oscillator design methodology, find an unstable amplifier and don't stabilize it with input and output matching networks.

At the core of an oscillator there is an amplifier, and at the core of an amplifier there is an active device. The TriQuint Texas GaAs fabrication process yields three versions of MESFETs, to choose as the active device. A GFET was chosen because the negative gate to source voltage, V_{GS}, allows for easily biasing the transistor with a single power source. The GFET was sized at 600 μm wide to ensure that enough current flow was available to meet the power output spec. A common source amplifier design was chosen for its straightforward simplicity.

A MESFET with one terminal grounded reduces to a two-port device. The frequency response of a two-port device, or network is described by its two-port S-Parameters. Two port S-Parameters are readily available from the device manufacturer for many packaged parts or quickly computed by the ADS software for transistors designed as part of a MMIC chip. Multiple S-Parameter described devices, or networks, can be connected and the combined S-Parameters calculated to accurately describe the frequency response of the resultant network. The resultant network for this VCO consists of a resonance generator, and two-port amplifier, and a load, as shown in figure 2.

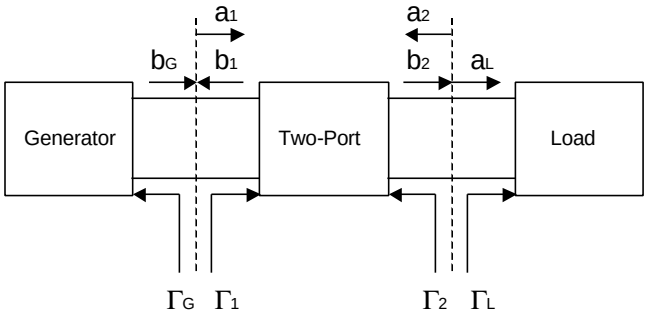


Figure 2. Loaded two-port network connect to generator.

The S-Parameter conditions needed for oscillations are, $k<1, \Gamma_G \cdot S'_{11}=1, \Gamma_L \cdot S'_{22}=1$, Vendelin [4]. Where $k=\dfrac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2\cdot|S_{12}\cdot S_{21}|}, \Delta=S_{11}\cdot S_{22}-S_{12}\cdot S_{21}$. And $\Gamma_1=S'_{11}=\dfrac{b_1}{a_1}$.

There are two solutions where the product of two variables equals one. A – Both variables equal one. B – Each variable is the multiplicative inverse of the other. Which means one of these two reflection coefficients, Γ_G or Γ_1 is greater than one. A reflection coefficient greater than one results from an input impedance with negative resistance. The generator for the VCO contains only passive components, which yield a $\Gamma_G < 1$. Therefore, $\Gamma_1 > 1$ or, the input impedance of the two-port amplifier must contain a negative resistance. To begin the design of an oscillator, first meet the condition of negative impedance for the two-port amplifier. Next, design a resonance circuit with an output reflection equal to the input reflection of the two-port amplifier. Third, design an output-matching network to maximize power transfer to the load.

Inside the two-port amplifier box resides a common-source connected mesfet amplifier. DC power is applied through a parallel L-C resonator to the mesfet's drain. The resonant frequency of the L-C tank equals the target frequency of the VCO, 1.12 GHz. The TriQuint GaAs process yields devices with good inherent stability. So, add a 10 Ω source resistor to aide in the design of an unstable amp. The shunt source capacitor increases the negative resistance of the circuit, while also increasing the effective capacitance looking into the gate of the transistor, Rhea [5]. The source resistor value also sets the DC operating condition V_{GS} = -0.6 V, since the gate is grounded. The circuit contains approximately 60 mAmps of current flow through the device.

A parallel L-C resonance tank serves as the oscillation signal generator. The shunt inductor of the parallel resonator doubles as the DC bias ground for the mesfet's gate. The resonator's variable capacitance is constructed with two 100 x 12 µm drain to source shorted mesfet varactors. The tuning voltage connects to the circuit at the drain-source common node between the two mesfets. The gate of one mesfet is grounded and the second gate connects to the inductor and amplifier. The tuning voltage biases both varactor mesfets because both gates are DC connected to ground, one gate is directly grounded and the second gate is grounded through the inductor. As figure 3 shows, include the emitter, feedback, and amplifier input capacitances and the amplifier input inductance to accurately calculate the resonant frequency, f_0. Assumed varactor capacitance of 0.55 pF at bias voltage, V_b = 0 V, 0.4 pF at V_b = 1 V, and 0.3 pF at V_b = 2 V. Varactor characterization performed on 300 µm GFET, Penn [6], scale accordingly.

$$f_0 = 1/\left(2p\sqrt{LC}\right) \quad f_0 = 1/\left(2p\sqrt{9\times10^{-9}\cdot 2.51\times10^{-12}}\right) = 1.059\times10^{9}\,Hz$$

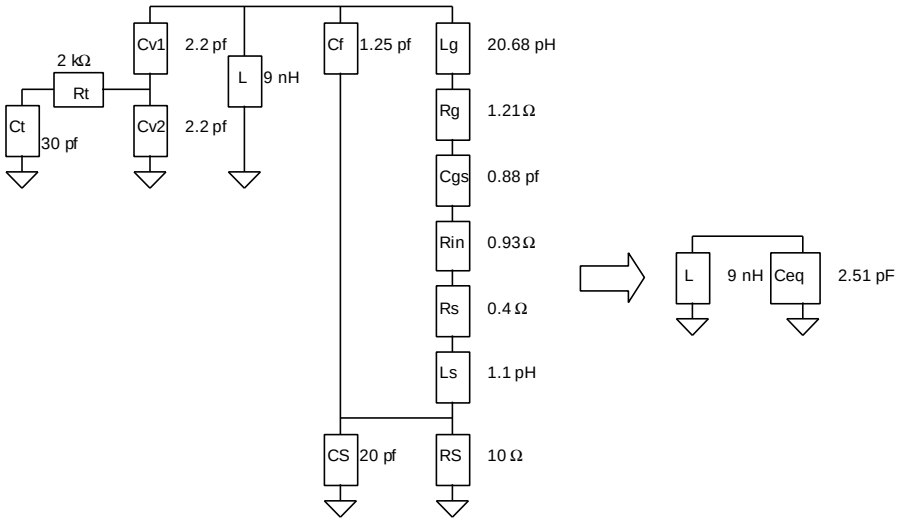


Figure 3. TriQuint linear GaAs MESFET model incorporated into the L-C resonance calculation.

Design the output-matching network with S_{11} equal, or as close as possible, to the conjugate of S22 of the two-port amplifier, for maximum power transfer to the load. Some matching sacrifice may need to be made here due to the practicality of device sizes.

MODELED PERFORMANCE:

Specifications Compliance Matrix for L-Band Voltage Controlled Oscillator

	Specification	Pre-Layout	Post-Layout	Fabbed IC
Frequency Range	1070 to 1170 MHz	1056 to 1171 MHz	1012 to 1056 MHz	
Output Power	> +10 dBm > +13 dBm goal	~ +19 dBm	~ +19 dBm	
Control Voltage	0 to 5 Volts	0 to 2 Volts	0 to 0.5 Volts	
Supply Voltage	± 5 Volts + 5 Volts only goal	Single +5 Volt Supply	Single +5 Volt Supply	
Output Impedance	50 Ω, nominal	50 Ω, nominal	50 Ω, nominal	
Size	60x60 mil ANACHIP	Fits	Fits	

Design performance is questionable. Although the pre-layout design meets specs and the goals, the post-layout design fails to meet the specs. The predicted frequency shifts down, out of the specified range. And, the application of tuning voltage greater than approximately 0.5 volts causes the oscillator to fail.

SCHEMATIC DIAGRAMS:

List of the appended schematics and simulations:

Biased MESFET Schematic
Resonant Tank Input Matching Network Schematic
Input Matching Network's S22 overlaid in the Biased MESFET Source Stability Circles
Output Matching Network Schematic
Output Matching Network's S11 conjugate match with the S22 of the Biased MESFET
Biased MESFET Instability Simulations
IMN and Biased MESFET Schematic
IMN and Biased MESFET Start-Up Transient Simulation
IMN, Biased MESFET, & OMN Schematic
IMN, Biased MESFET, & OMN Start-Up Transient Simulation
IMN, Biased MESFET, & OMN Harmonic Balance Pre-Layout Schematic
IMN, Biased MESFET, & OMN Harmonic Balance Pre-Layout Simulation
IMN, Biased MESFET, & OMN Harmonic Balance Post-Layout Schematic
IMN, Biased MESFET, & OMN Harmonic Balance Post-Layout Simulation
VCO Layout within 60x60 mil ANACHIP
Simplified DC Schematic Annotated with DC Bias Values

DC Analysis:

DC analysis shows that the source resistor is too thin to carry the ~ 60 mAmps of current. The 10-Ω NiCr resistor needs a width greater than 60 mm. New layout required prior to fabrication.

TEST PLAN:

Apply tuning voltage, to "VTUNE" labeled pad on IC, equal to zero volt first, to discharge the varactor connected mesfets. Next connect the +5 volt supply to "VDD" labeled pad. Connect spectrum analyzer to pad labeled "VOUT". Compare DC current to predicted current value from the DC analysis above. Compare oscillator output frequency and power with values predicted by Harmonic Balance simulations above.

CONCLUSION & RECOMMENDATIONS:

With its undersized source resistor this design should NOT be fabricated. If everything else simulated properly after layout it still would not hurt to clean up the layout a little more. The ground-signal-ground probe pads for the VTUNE input are unnecessary because VTUNE is a DC bias voltage. The VDD input trace has an unneeded section between the bend and the input cap. And the ground connection under the varactor mesfet should also be straight.

Countless hours were spent trying to understand and bring together the methodologies of several authors' texts, more than those referenced. The confusion acquired by reading several texts simultaneously, then achieving ADS simulation results in disagreement with that author's predictions can be summarized by the following passage.

> "Although the negative resistance analysis characterizes the conditions leading to oscillation and predicts the oscillation frequency accurately, the author's experience is that relating the results of the analysis to the noise performance of the oscillator is unreliable. This is a controversial position to take because of the existence of a paper by K. Kurokawa which contains a rigorous analysis of the noise performance of the negative resistance oscillator…" Rhea [7]

Even "experts" still disagree about microwave design.

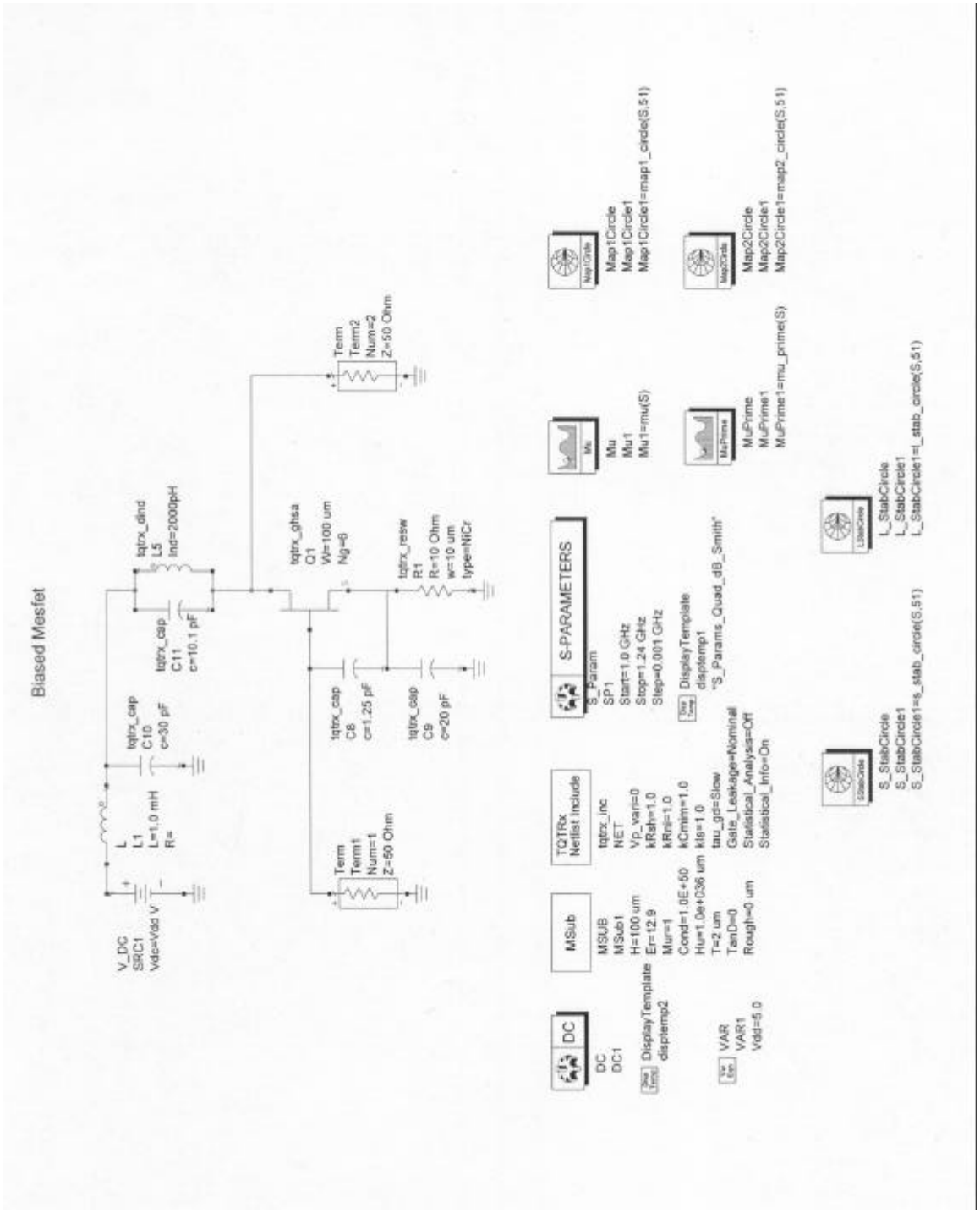
My goal was to complete a design on a topic that was not discussed in class for the specific reason of testing myself. Unfortunately, I fell short of that goal. Too much time was lost with a too complicated initial design. Because it simulated successfully sometimes while I attempted to dial in the frequency I ignored the overall fragility of the design. I still don't understand what broke the design when it was transferred from circuit without interconnects to one with interconnects. What parasitic components crippled my design? I hope that the Dorsey Center will be available between semesters so I may have the opportunity to build a better oscillator.

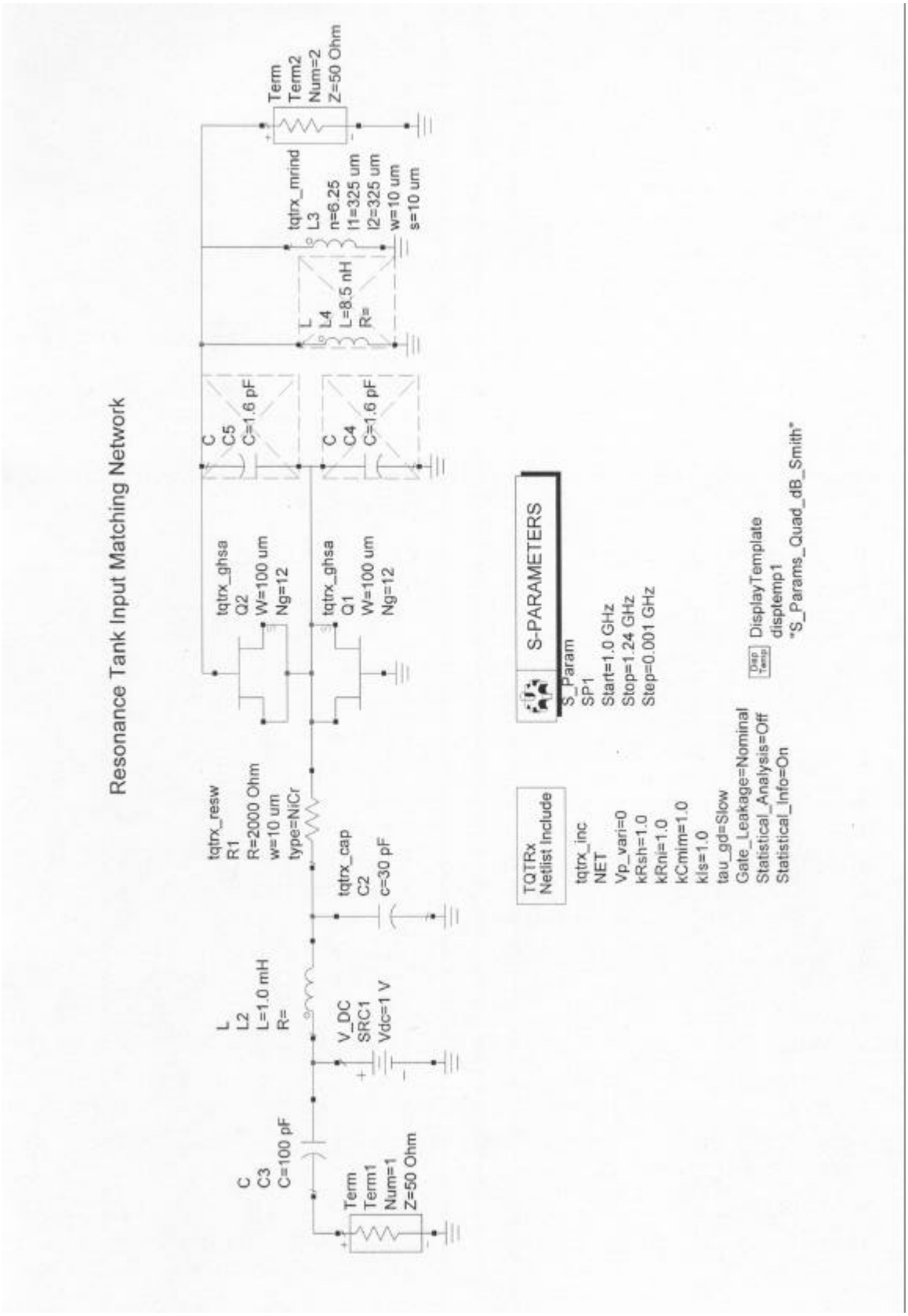
ACKNOWLEDGEMENTS:

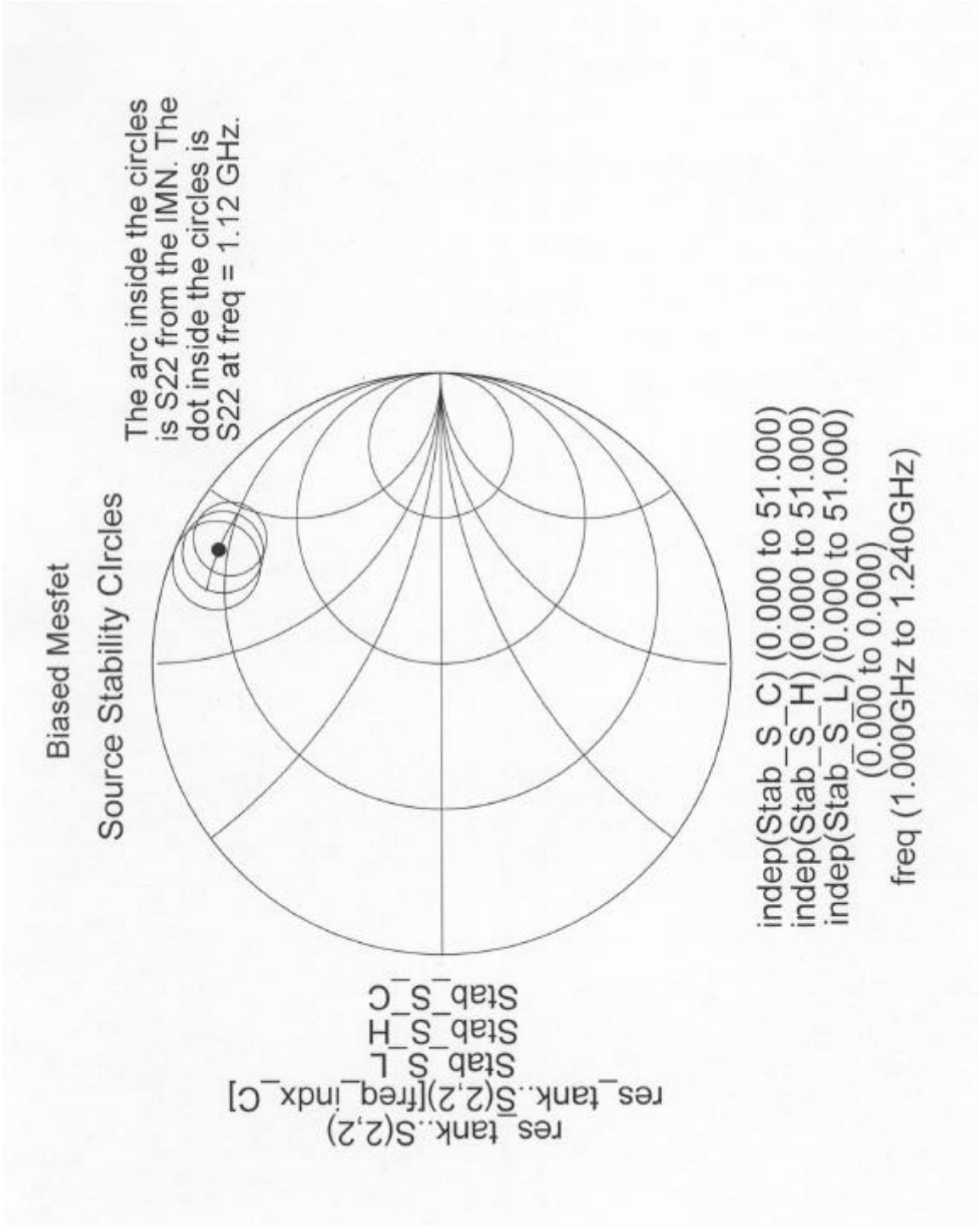
With corporations demanding experience workers at all levels, and that new hires be productive immediately upon starting employment. Realistic design oriented courses offered at colleges and universities are the only manner for someone to change their technical career track. It is with sincere gratitude that I thank all those involved in making the Monolithic Microwave Integrated Circuit design course at Johns Hopkins University a reality. My thanks go to instructors Craig Moore and John Penn. To the Agilent Corporation for providing the ADS simulation software. To TriQuint Semiconductor Corporation for providing the GaAs process library and agreeing the fabrication student designs. And to Gray Wray for supporting the ADS tool for a bunch of whining students.

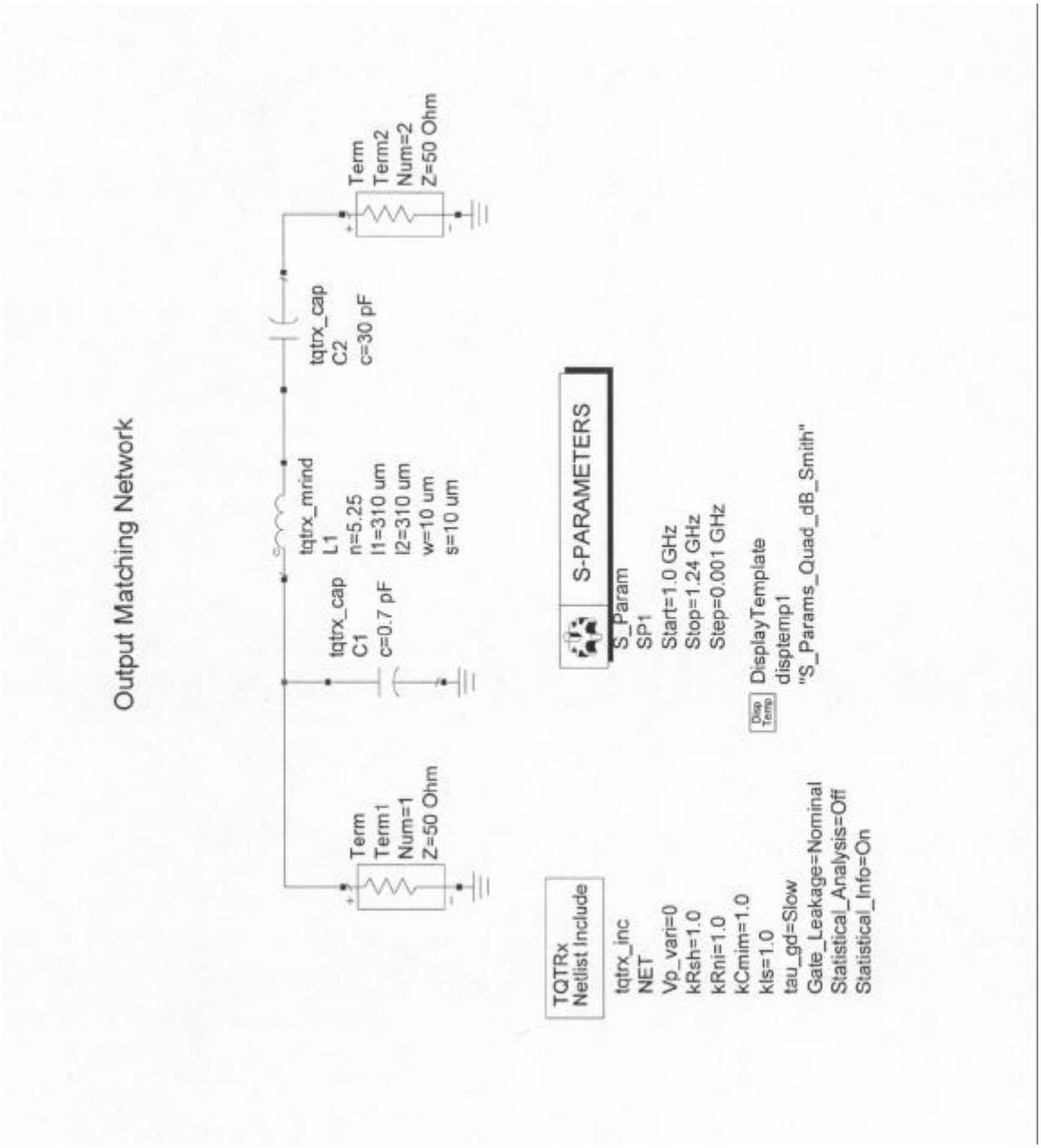
REFERENCES:

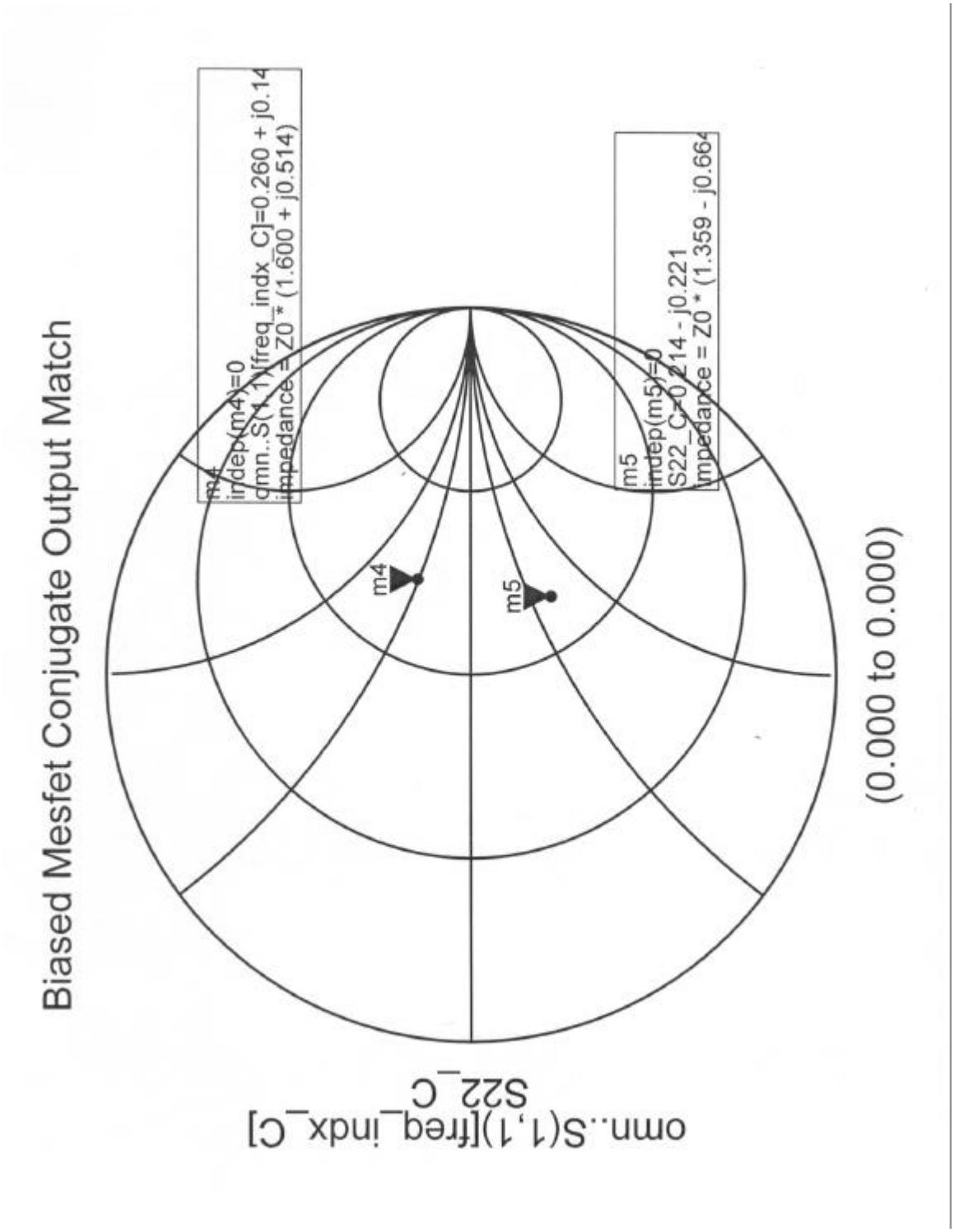
1. D. M. Pozar, *Microwave Engineering*, New York, NY: John Wiley & Sons, 1998, pp. 612-616.
2. M. L. Edwards and J. H. Sinsky, "A new criterion for linear 2-port stability using a single geometrically derived parameter," *IEEE Trans. Microwave Theory Tech.*, vol. 40, no. 12, pp. 2303-2311, Dec. 1992.
3. M. L. Edwards, S. Cheng, and J. H. Sinsky, "A Deterministic Approach for Designing Conditionally Stable Amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 7, pp. 1567-1575, July 1995.
4. G. D. Vendelin, *Design of Amplifiers and Oscillators by the S-Parameter Method*, New York, NY: John Wiley & Sons, 1982, pp. 132.
5. R. W. Rhea, *Oscillator Design and Computer Simulation*, Atlanta, GA, Noble, 1990, pp. 67.
6. J. Penn and C. Moore, "Notes for Lecture #4, TriQuint Process Active MMIC Circuit Elements," Johns Hopkins University course 525.787.91, pp. 70, Fall 2002.
7. R. W. Rhea, *Oscillator Design and Computer Simulation*, Atlanta, GA, Noble, 1990, pp. 66.

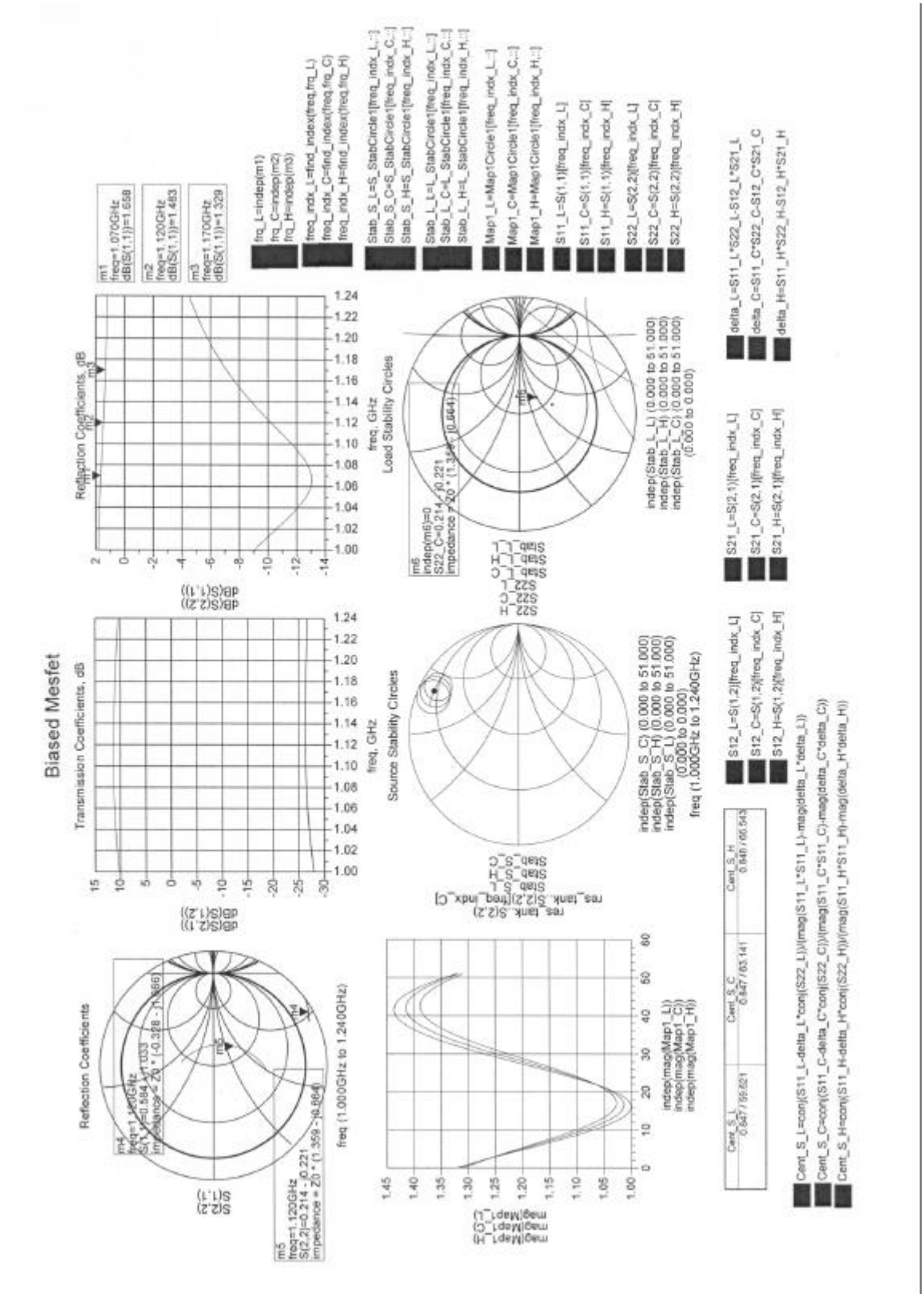

Biased Mesfet
V_DC
SRC1
Vdc=Vdd V
L
L1
L=1.0 mH
R=
tqtrx_cap
C10
c=30 pF
tqtrx_dind
L5
ind=2000pH
tqtrx_cap
C11
c=10.1 pF
tqtrx_ghsa
Q1
W=100 um
Ng=6
tqtrx_resw
R1
R=10 Ohm
w=10 um
type=NiCr
tqtrx_cap
C8
c=1.25 pF
tqtrx_cap
C9
c=20 pF
Term
Term1
Num=1
Z=50 Ohm
Term
Term2
Num=2
Z=50 Ohm
DC
DC
DC1
MSub
MSUB
MSub1
H=100 um
Er=12.9
Mur=1
Cond=1.0E+50
Hu=1.0e+036 um
T=2 um
TanD=0
Rough=0 um
TQTRx
Netlist Include
tqtrx_inc
NET
Vp_var=0
kRsh=1.0
kRni=1.0
kCmim=1.0
kis=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
S-PARAMETERS
S_Param
SP1
Start=1.0 GHz
Stop=1.24 GHz
Step=0.001 GHz
DisplayTemplate
displtemp1
"S_Params_Quad_dB_Smith"
Mu
Mu1
Mu1=mu(S)
MuPrime
MuPrime1
MuPrime1=mu_prime(S)
Map1Circle
Map1Circle1
Map1Circle1=map1_circle(S,51)
Map2Circle
Map2Circle1
Map2Circle1=map2_circle(S,51)
L_StabCircle
L_StabCircle1
L_StabCircle1=l_stab_circle(S,51)
S_StabCircle
S_StabCircle1
S_StabCircle1=s_stab_circle(S,51)
DisplayTemplate
displtemp2
VAR
VAR1
Vdd=5.0

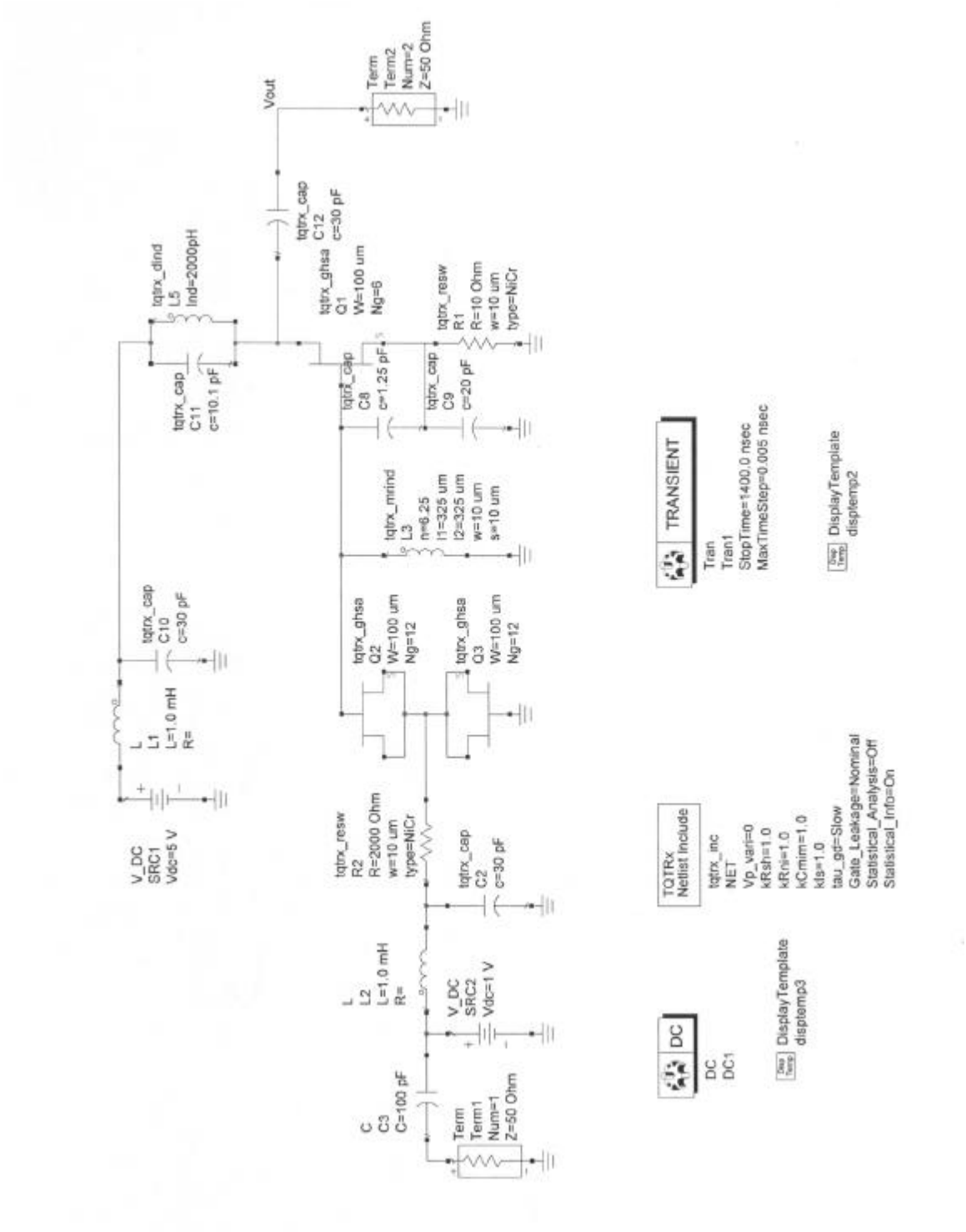

Resonance Tank Input Matching Network
Term
Term2
Num=2
Z=50 Ohm
tqtrx_mrind
L3
n=6.25
l1=325 um
l2=325 um
w=10 um
s=10 um
L
L4
L=8.5 nH
R=
C
C5
C=1.6 pF
C
C4
C=1.6 pF
tqtrx_ghsa
Q2
W=100 um
Ng=12
tqtrx_ghsa
Q1
W=100 um
Ng=12
tqtrx_resw
R1
R=2000 Ohm
w=10 um
type=NiCr
tqtrx_cap
C2
c=30 pF
L
L2
L=1.0 mH
R=
V_DC
SRC1
Vdc=1 V
C
C3
C=100 pF
Term
Term1
Num=1
Z=50 Ohm
S-PARAMETERS
S_Param
SP1
Start=1.0 GHz
Stop=1.24 GHz
Step=0.001 GHz
TQTRx
Netlist Include
tqtrx_inc
NET
Vp_vari=0
kRsh=1.0
kRni=1.0
kCmim=1.0
kls=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
DisplayTemplate
disptemp1
"S_Params_Quad_dB_Smith"

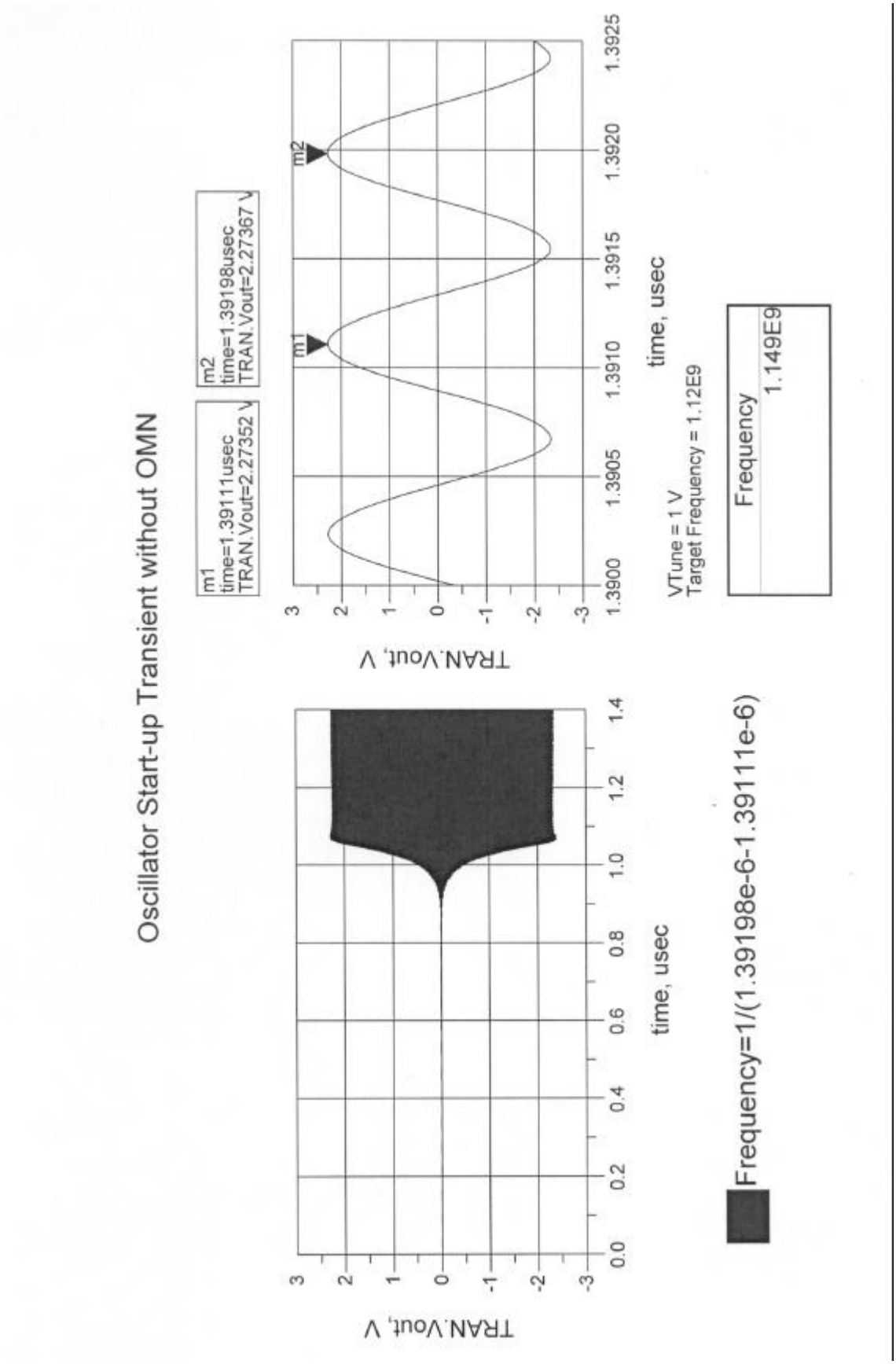

Biased Mesfet
Source Stability CIrcles
The arc inside the circles is S22 from the IMN. The dot inside the circles is S22 at freq = 1.12 GHz.
indep(Stab_S_C) (0.000 to 51.000)
indep(Stab_S_H) (0.000 to 51.000)
indep(Stab_S_L) (0.000 to 51.000)
(0.000 to 0.000)
freq (1.000GHz to 1.240GHz)
res_tank..S(2,2)
res_tank..S(2,2)[freq_indx_C]
Stab_S_L
Stab_S_H
Stab_S_C

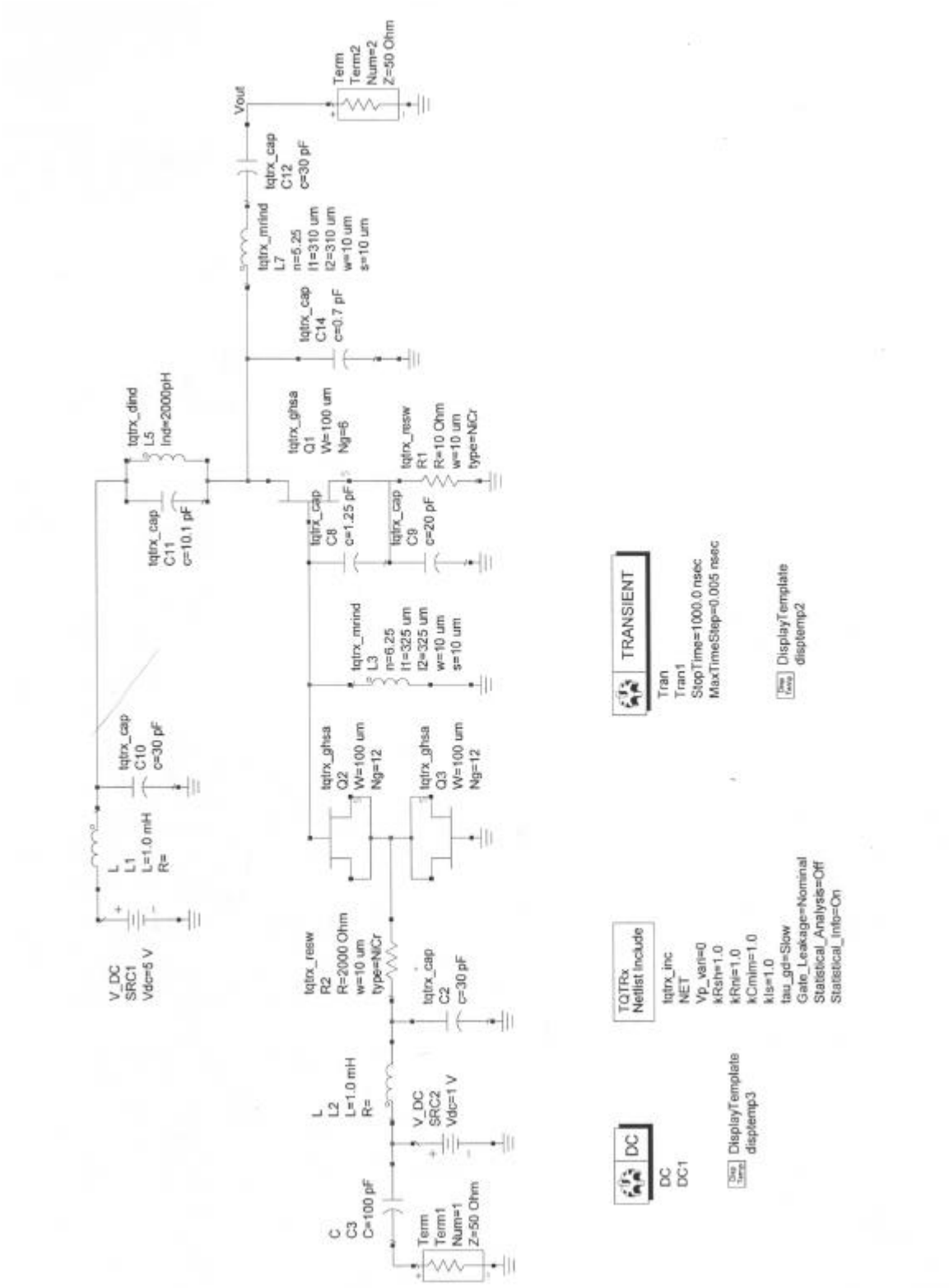

Output Matching Network
Term
Term2
Num=2
Z=50 Ohm
tqtrx_cap
C2
c=30 pF
tqtrx_mrind
L1
n=5.25
l1=310 um
l2=310 um
w=10 um
s=10 um
tqtrx_cap
C1
c=0.7 pF
Term
Term1
Num=1
Z=50 Ohm
S-PARAMETERS
S_Param
SP1
Start=1.0 GHz
Stop=1.24 GHz
Step=0.001 GHz
DisplayTemplate
disptemp1
"S_Params_Quad_dB_Smith"
TQTRx
Netlist Include
tqtrx_inc
NET
Vp_vari=0
kRsh=1.0
kRni=1.0
kCmim=1.0
kls=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On

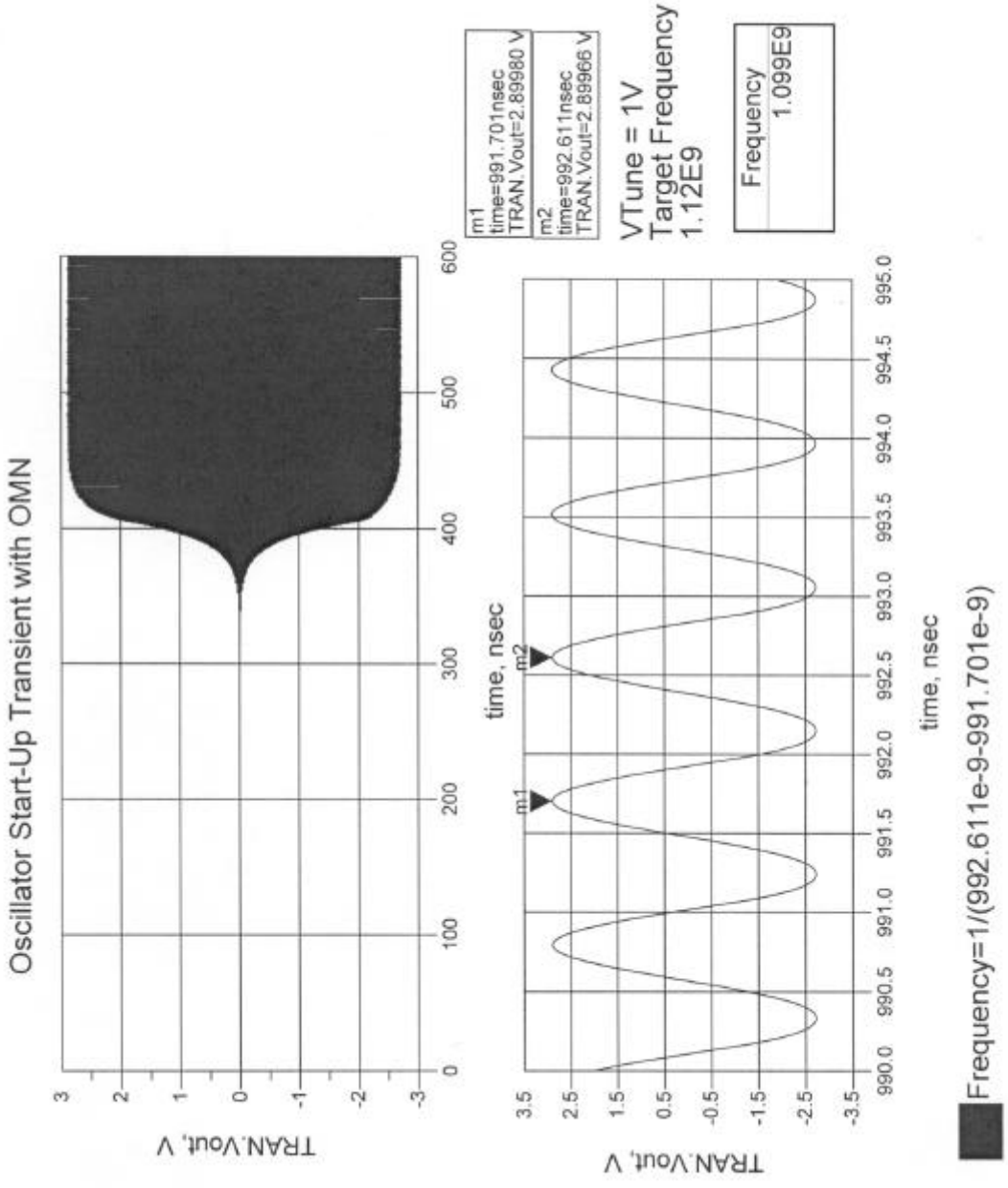

Biased Mesfet Conjugate Output Match
(0.000 to 0.000)
omn..S(1,1)[freq_indx_C]
S22_C
m4
indep(m4)=0
omn..S(1,1)[freq_indx_C]=0.260 + j0.14
impedance = Z0 * (1.600 + j0.514)
m5
indep(m5)=0
S22_C=0.214 - j0.221
impedance = Z0 * (1.359 - j0.664
m4
m5

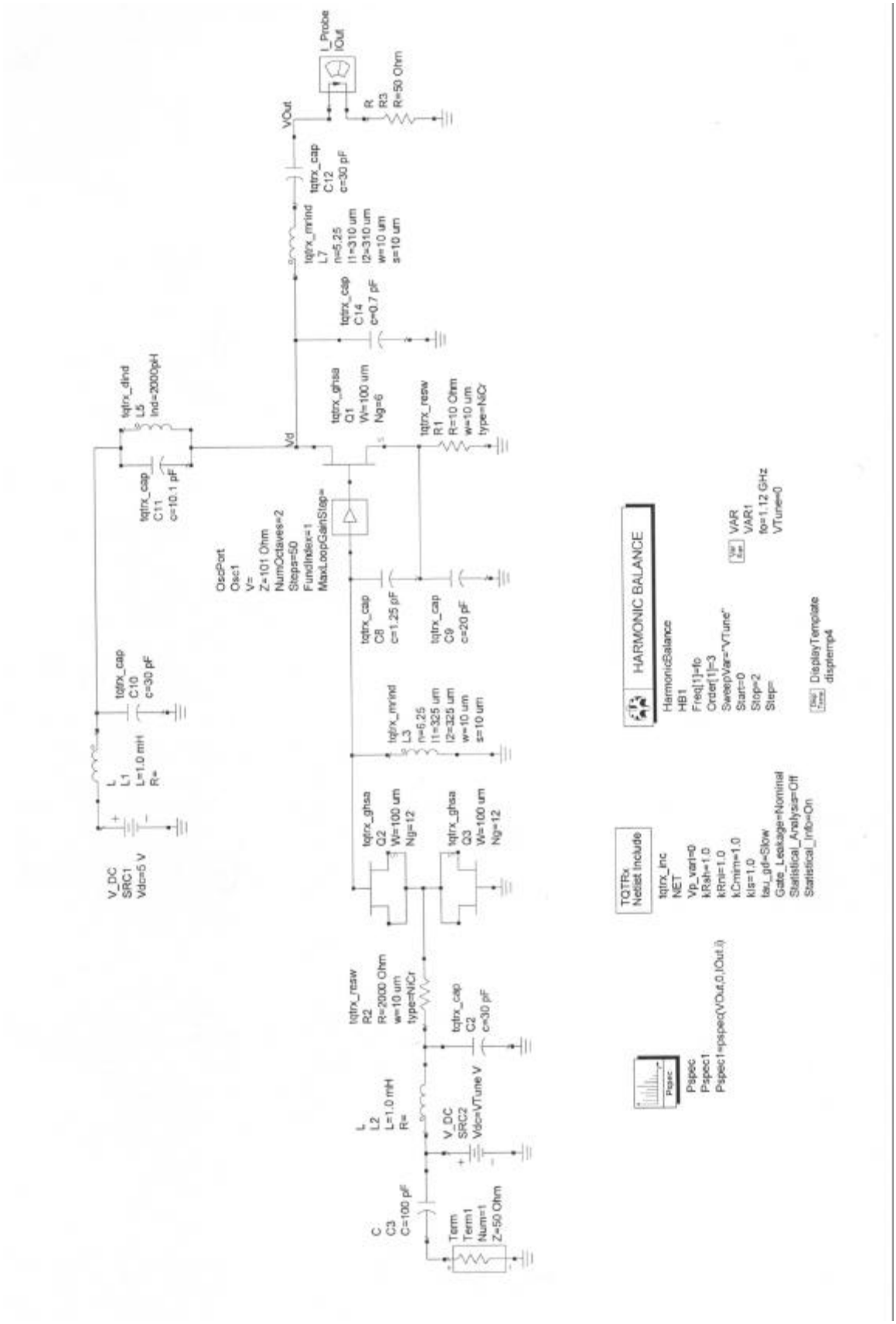

Biased Mesfet
Transmission Coefficients, dB
Reflection Coefficients, dB
Load Stability Circles
Source Stability Circles
Reflection Coefficients
freq, GHz
freq (1.000GHz to 1.240GHz)

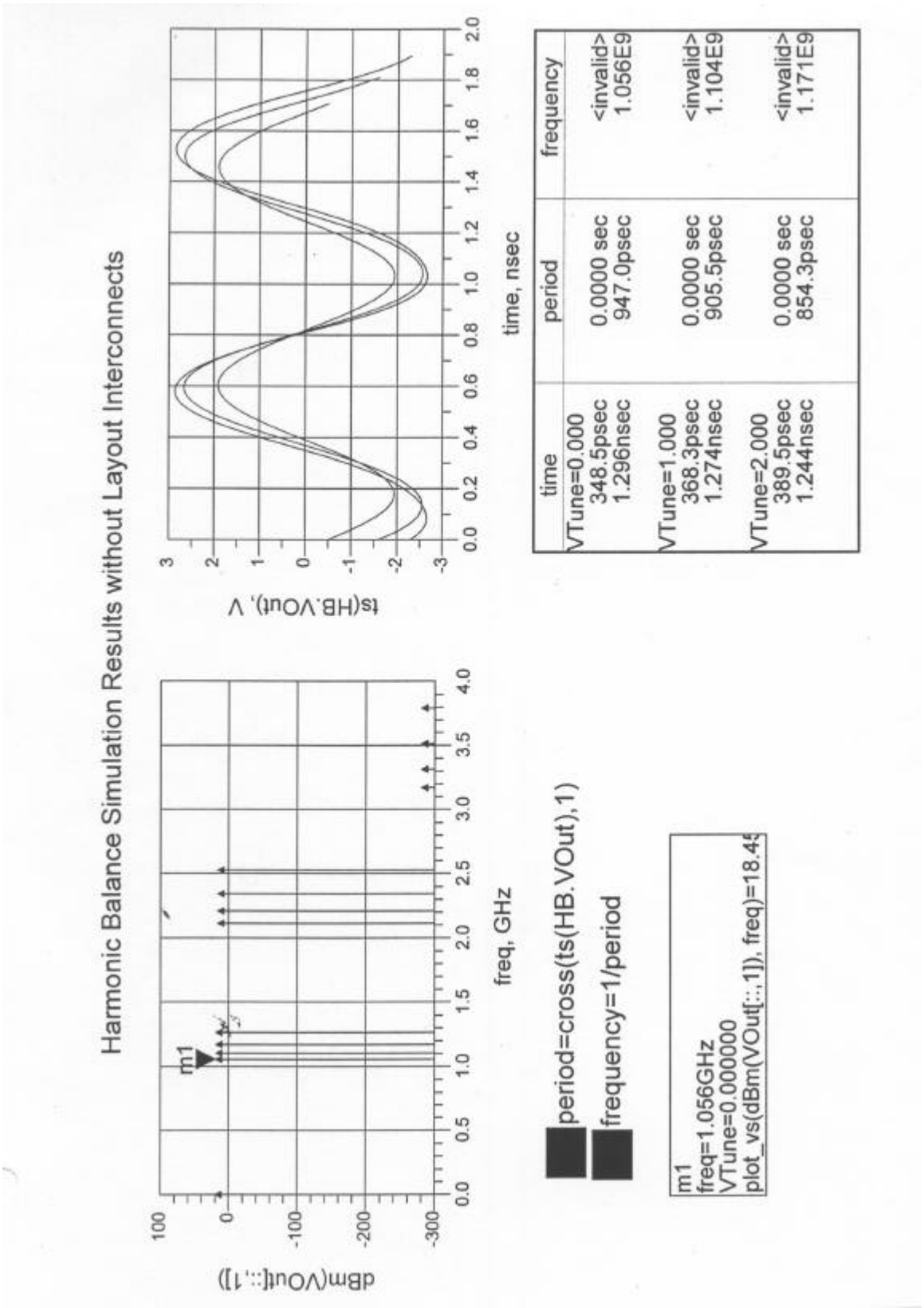

Vout
Term
Term2
Num=2
Z=50 Ohm
tqtrx_cap
C12
c=30 pF
tqtrx_ghsa
Q1
W=100 um
Ng=6
tqtrx_dind
L5
Ind=2000pH
tqtrx_resw
R1
R=10 Ohm
w=10 um
type=NiCr
tqtrx_cap
C11
c=10.1 pF
tqtrx_cap
C8
c=1.25 pF
tqtrx_cap
C9
c=20 pF
tqtrx_mrind
L3
n=6.25
l1=325 um
l2=325 um
w=10 um
s=10 um
tqtrx_cap
C10
c=30 pF
L
L1
L=1.0 mH
R=
tqtrx_ghsa
Q2
W=100 um
Ng=12
tqtrx_ghsa
Q3
W=100 um
Ng=12
V_DC
SRC1
Vdc=5 V
tqtrx_resw
R2
R=2000 Ohm
w=10 um
type=NiCr
tqtrx_cap
C2
c=30 pF
L
L2
L=1.0 mH
R=
V_DC
SRC2
Vdc=1 V
C
C3
C=100 pF
Term
Term1
Num=1
Z=50 Ohm
TRANSIENT
Tran
Tran1
StopTime=1400.0 nsec
MaxTimeStep=0.005 nsec
DisplayTemplate
disptemp2
TQTRX
Netlist include
tqtrx_inc
NET
Vp_var=0
kRsh=1.0
kRni=1.0
kCmim=1.0
kls=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
DC
DC
DC1
DisplayTemplate
disptemp3

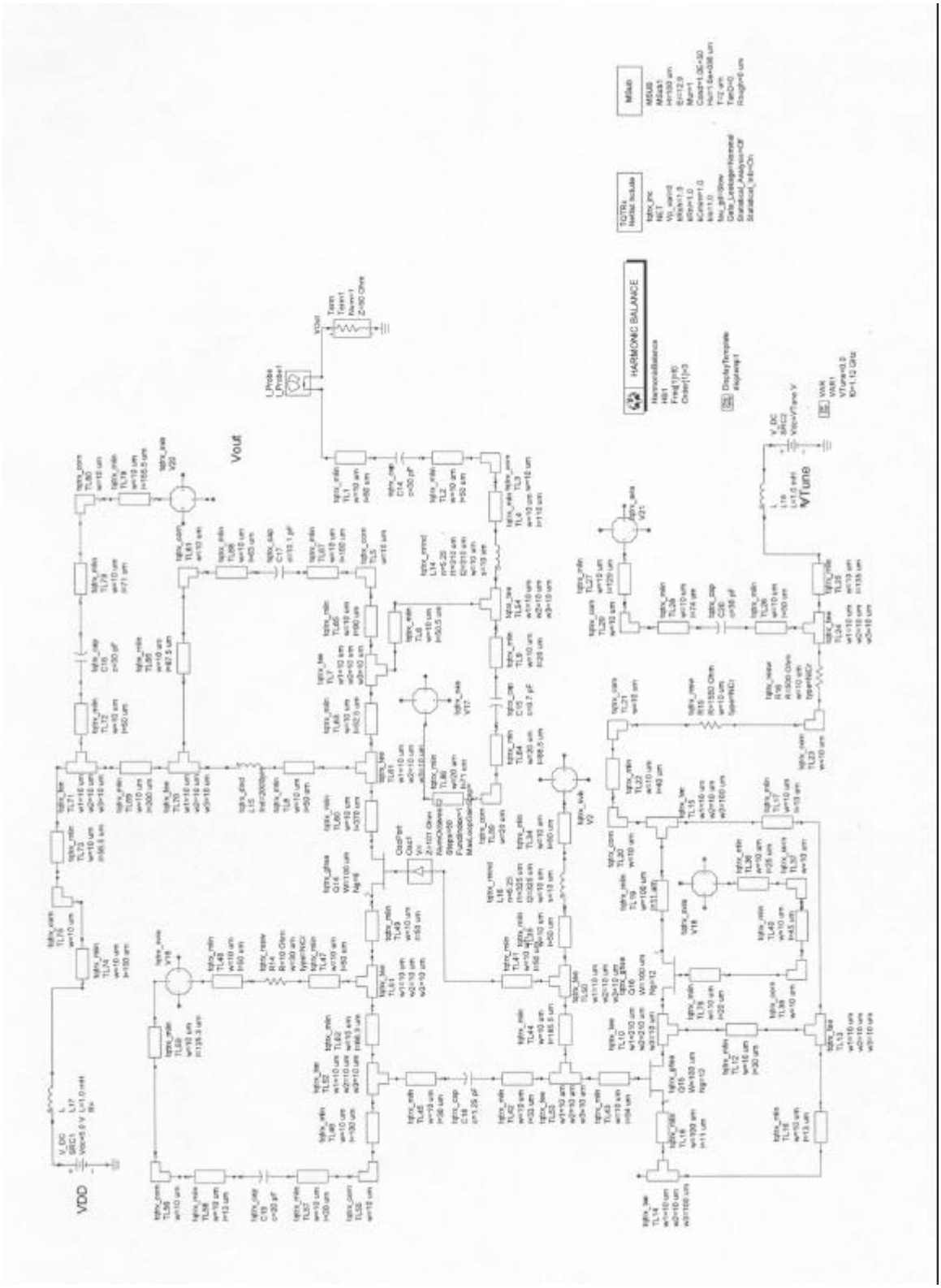

Oscillator Start-up Transient without OMN
m1
time=1.39111usec
TRAN.Vout=2.27352 V
m2
time=1.39198usec
TRAN.Vout=2.27367 V
TRAN.Vout, V
time, usec
VTune = 1 V
Target Frequency = 1.12E9
Frequency
1.149E9
Frequency=1/(1.39198e-6-1.39111e-6)

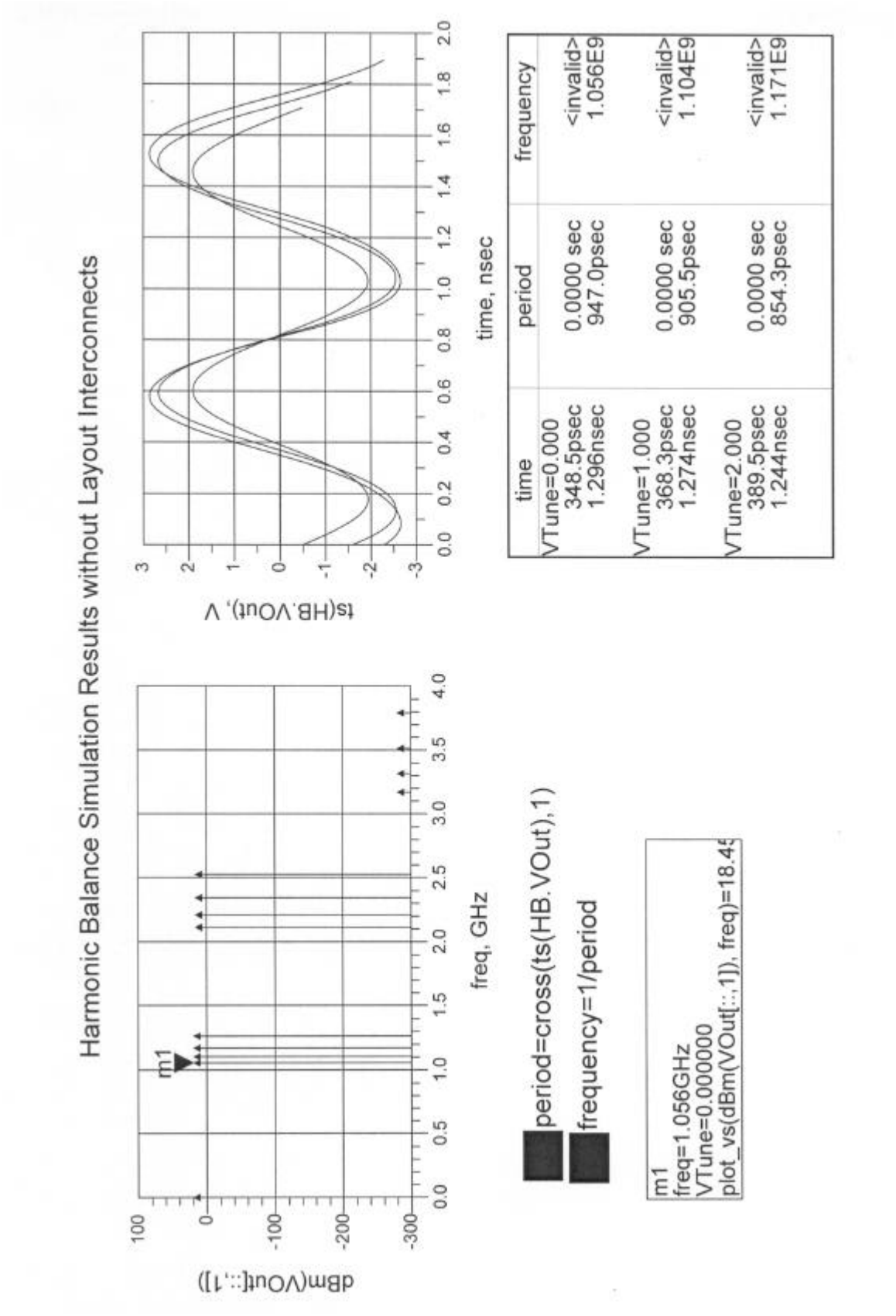

Term
Term2
Num=2
Z=50 Ohm
Vout
tqtrx_cap
C12
c=30 pF
tqtrx_mrind
L7
n=5.25
l1=310 um
l2=310 um
w=10 um
s=10 um
tqtrx_cap
C14
c=0.7 pF
tqtrx_dind
L5
Ind=2000pH
tqtrx_ghsa
Q1
W=100 um
Ng=6
tqtrx_resw
R1
R=10 Ohm
w=10 um
type=NiCr
tqtrx_cap
C11
c=10.1 pF
tqtrx_cap
C8
c=1.25 pF
tqtrx_cap
C9
c=20 pF
tqtrx_mrind
L3
n=6.25
l1=325 um
l2=325 um
w=10 um
s=10 um
tqtrx_cap
C10
c=30 pF
tqtrx_ghsa
Q2
W=100 um
Ng=12
tqtrx_ghsa
Q3
W=100 um
Ng=12
L
L1
L=1.0 mH
R=
V_DC
SRC1
Vdc=5 V
tqtrx_resw
R2
R=2000 Ohm
w=10 um
type=NiCr
tqtrx_cap
C2
c=30 pF
L
L2
L=1.0 mH
R=
V_DC
SRC2
Vdc=1 V
C
C3
C=100 pF
Term
Term1
Num=1
Z=50 Ohm
TRANSIENT
Tran
Tran1
StopTime=1000.0 nsec
MaxTimeStep=0.005 nsec
DisplayTemplate
disptemp2
TQTRx
Netlist Include
tqtrx_inc
NET
Vp_vari=0
kRsh=1.0
kRni=1.0
kCmim=1.0
kls=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
DC
DC
DC1
DisplayTemplate
disptemp3

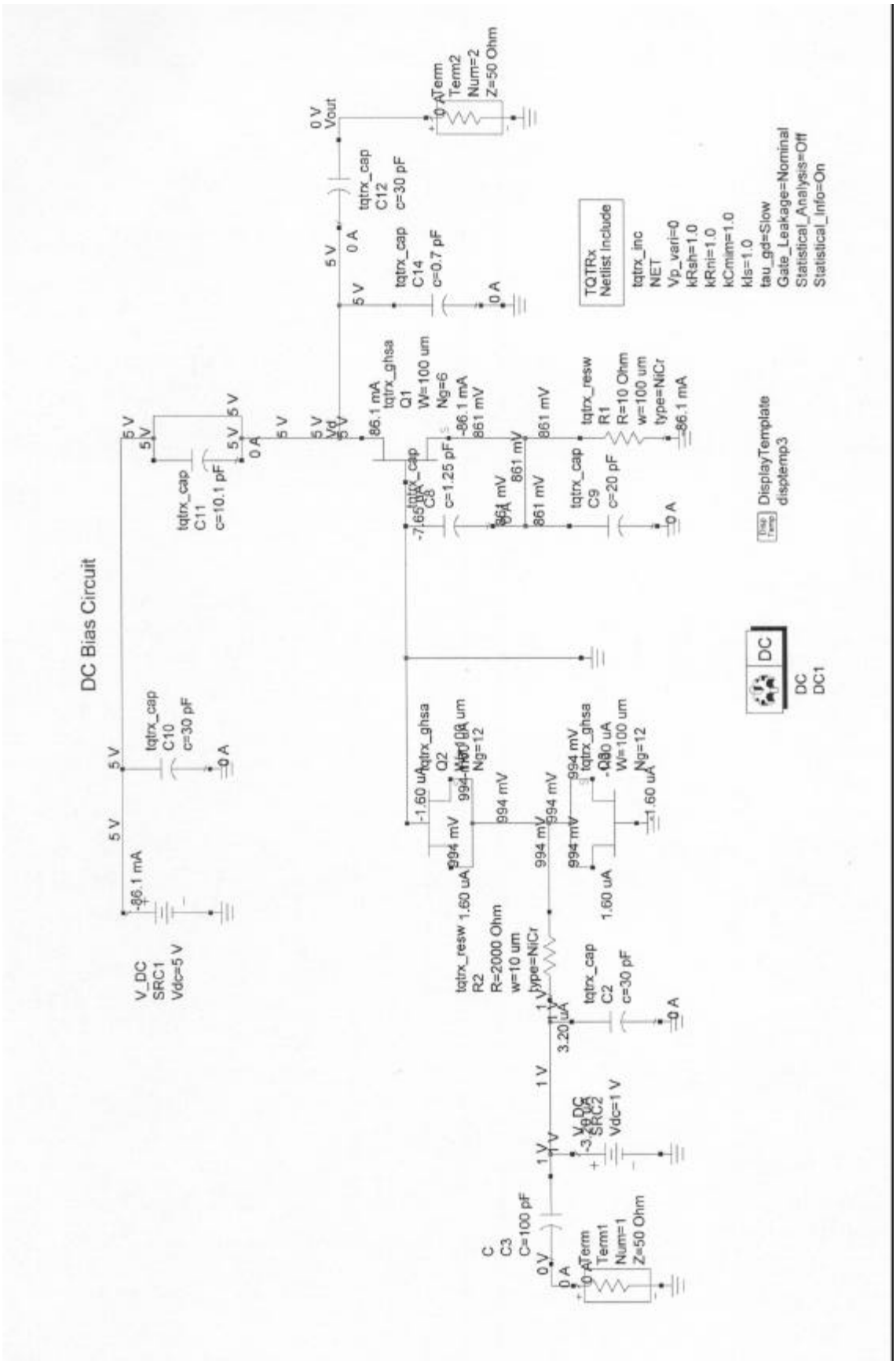

Oscillator Start-Up Transient with OMN
TRAN.Vout, V
time, nsec
m1
time=991.701nsec
TRAN.Vout=2.89980 V
m2
time=992.611nsec
TRAN.Vout=2.89966 V
VTune = 1V
Target Frequency
1.12E9
Frequency
1.099E9
Frequency=1/(992.611e-9-991.701e-9)

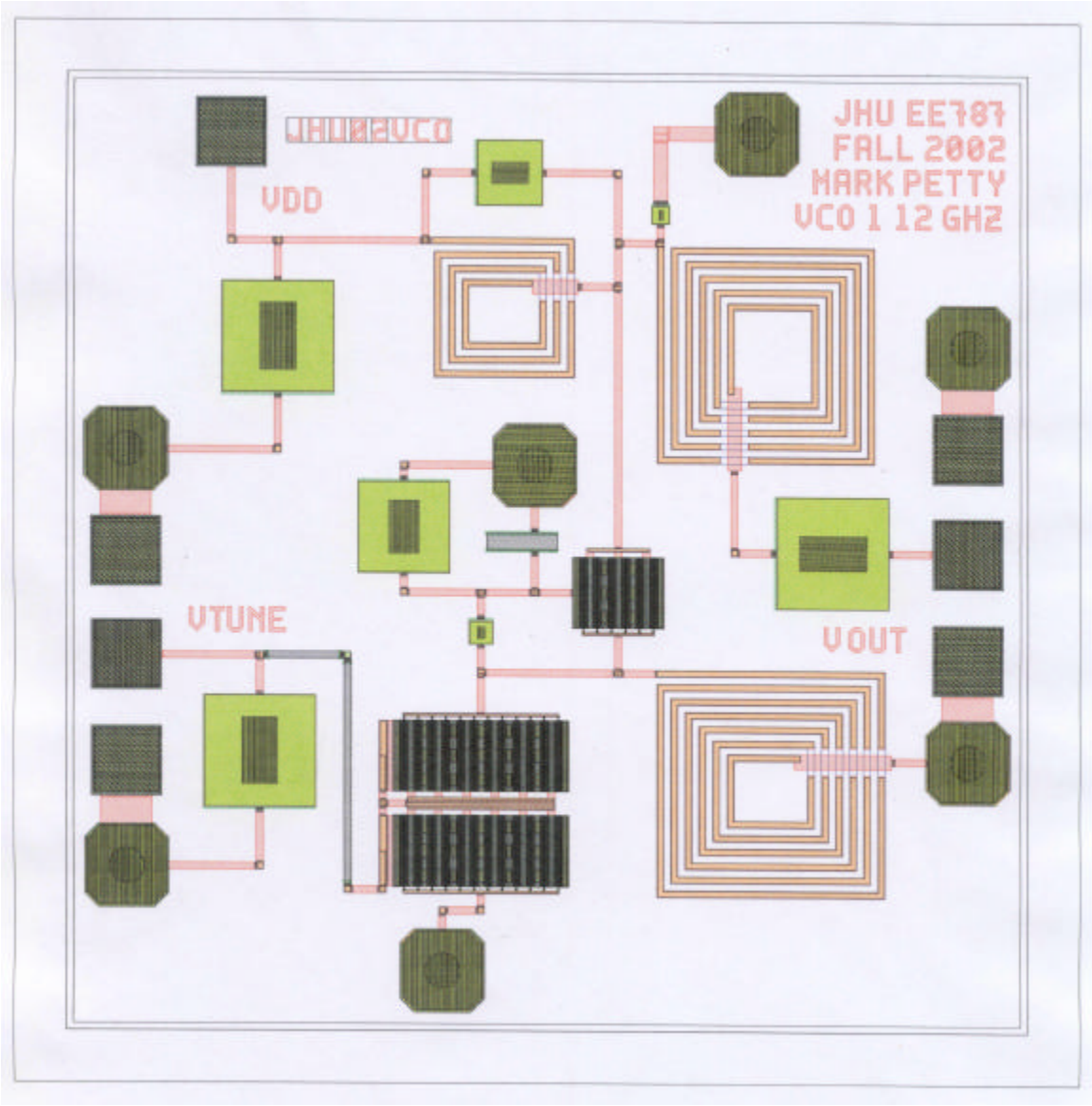

I_Probe IOut
VOut
R R3 R=50 Ohm
tqtrx_cap C12 c=30 pF
tqtrx_mrind L7 n=5.25 l1=310 um l2=310 um w=10 um s=10 um
tqtrx_cap C14 c=0.7 pF
tqtrx_dind L5 Ind=2000pH
tqtrx_ghsa Q1 W=100 um Ng=6
tqtrx_resw R1 R=10 Ohm w=10 um type=NiCr
Vd
tqtrx_cap C11 c=10.1 pF
OscPort Osc1 V= Z=101 Ohm NumOctaves=2 Steps=50 FundIndex=1 MaxLoopGainStep=
tqtrx_cap C8 c=1.25 pF
tqtrx_cap C9 c=20 pF
tqtrx_cap C10 c=30 pF
tqtrx_mrind L3 n=6.25 l1=325 um l2=325 um w=10 um s=10 um
L L1 L=1.0 mH R=
V_DC SRC1 Vdc=5 V
tqtrx_ghsa Q2 W=100 um Ng=12
tqtrx_ghsa Q3 W=100 um Ng=12
tqtrx_resw R2 R=2000 Ohm w=10 um type=NiCr
tqtrx_cap C2 c=30 pF
L L2 L=1.0 mH R=
V_DC SRC2 Vdc=VTune V
C C3 C=100 pF
Term Term1 Num=1 Z=50 Ohm
HARMONIC BALANCE
HarmonicBalance HB1 Freq[1]=fo Order[1]=3 SweepVar="VTune" Start=0 Stop=2 Step=
VAR VAR1 fo=1.12 GHz VTune=0
DisplayTemplate disptemp4
TQTRx Netlist Include
tqtrx_inc NET Vp_var=0 kRsh=1.0 kRnp=1.0 kCmim=1.0 kls=1.0 tau_gd=Slow Gate_Leakage=Nominal Statistical_Analysis=Off Statistical_Info=On
Psparc Psparc1 Psparc1=psparc(VOut,0,IOut,0)


Harmonic Balance Simulation Results without Layout Interconnects
ts(HB.VOut), V
time, nsec
time
period
frequency
VTune=0.000
348.5psec
0.0000 sec
<invalid>
1.296nsec
947.0psec
1.056E9
VTune=1.000
368.3psec
0.0000 sec
<invalid>
1.274nsec
905.5psec
1.104E9
VTune=2.000
389.5psec
0.0000 sec
<invalid>
1.244nsec
854.3psec
1.171E9
dBm(VOut[::,1])
freq, GHz
m1
period=cross(ts(HB.VOut),1)
frequency=1/period
m1
freq=1.056GHz
VTune=0.000000
plot_vs(dBm(VOut[::,1]), freq)=18.45


HARMONIC BALANCE
Vout
VTune
VDD


Harmonic Balance Simulation Results without Layout Interconnects
ts(HB.VOut), V
time, nsec
time
period
frequency
VTune=0.000
348.5psec
0.0000 sec
<invalid>
1.296nsec
947.0psec
1.056E9
VTune=1.000
368.3psec
0.0000 sec
<invalid>
1.274nsec
905.5psec
1.104E9
VTune=2.000
389.5psec
0.0000 sec
<invalid>
1.244nsec
854.3psec
1.171E9
dBm(VOut[::,1])
m1
freq, GHz
period=cross(ts(HB.VOut),1)
frequency=1/period
m1
freq=1.056GHz
VTune=0.000000
plot_vs(dBm(VOut[::,1]), freq)=18.45


DC Bias Circuit
V_DC
SRC1
Vdc=5 V
tqtrx_cap
C10
c=30 pF
tqtrx_cap
C11
c=10.1 pF
tqtrx_cap
C12
c=30 pF
tqtrx_cap
C14
c=0.7 pF
tqtrx_ghsa
Q1
W=100 um
Ng=6
tqtrx_cap
C8
c=1.25 pF
tqtrx_cap
C9
c=20 pF
tqtrx_resw
R1
R=10 Ohm
w=100 um
type=NiCr
tqtrx_ghsa
Q2
W=100 um
Ng=12
tqtrx_ghsa
Q3
W=100 um
Ng=12
tqtrx_resw
R2
R=2000 Ohm
w=10 um
type=NiCr
tqtrx_cap
C2
c=30 pF
V_DC
SRC2
Vdc=1 V
C
C3
C=100 pF
TQTRx
Netlist Include
tqtrx_inc
NET
Vp_vari=0
kRsh=1.0
kRni=1.0
kCmim=1.0
kIs=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
DisplayTemplate
disptemp3
DC
DC1
Term
Term2
Num=2
Z=50 Ohm
Term
Term1
Num=1
Z=50 Ohm


JHU02VCO
VDD
JHU EE787
FALL 2002
MARK PETTY
VCO 1 12 GHZ
VTUNE
VOUT