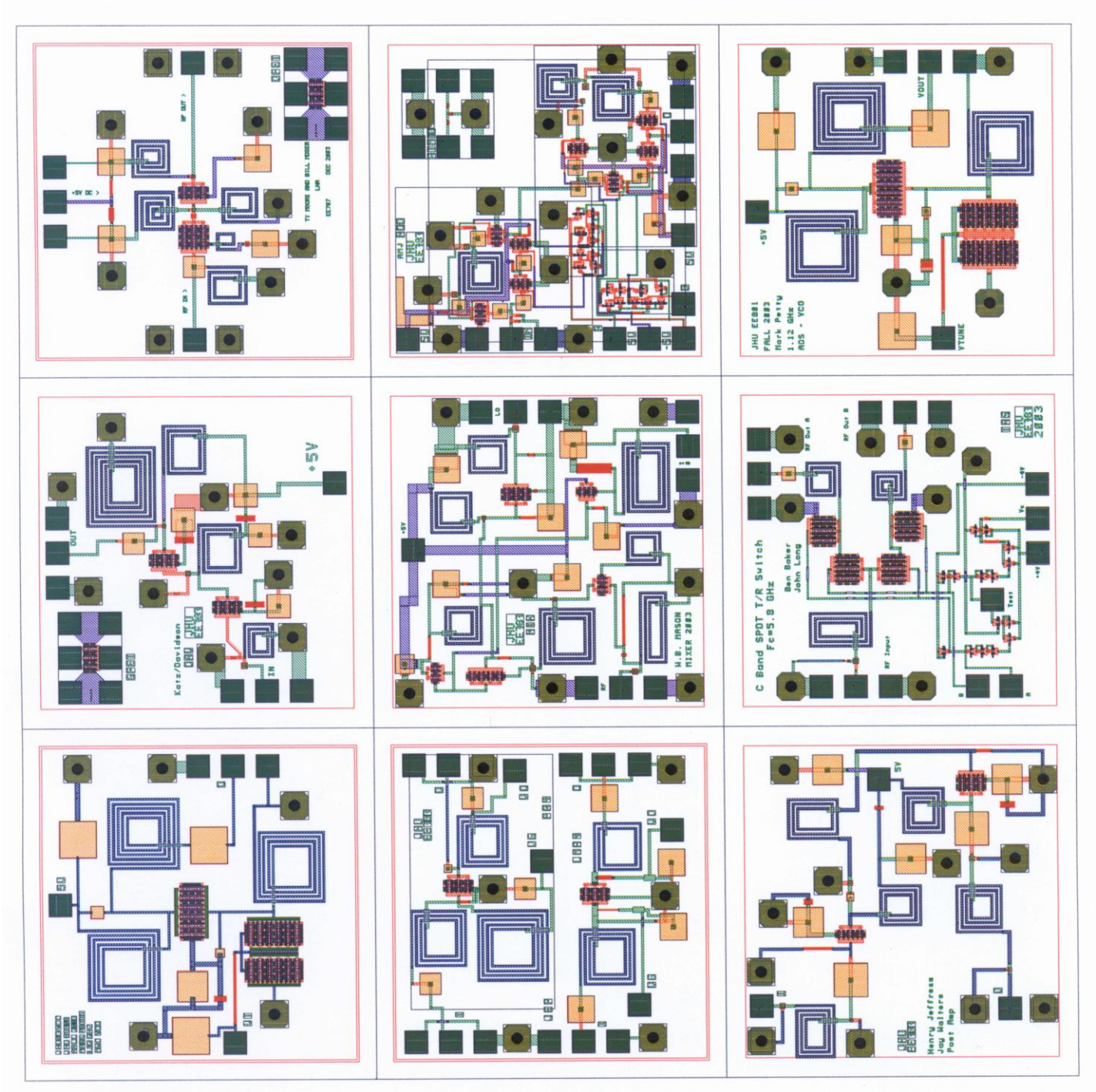
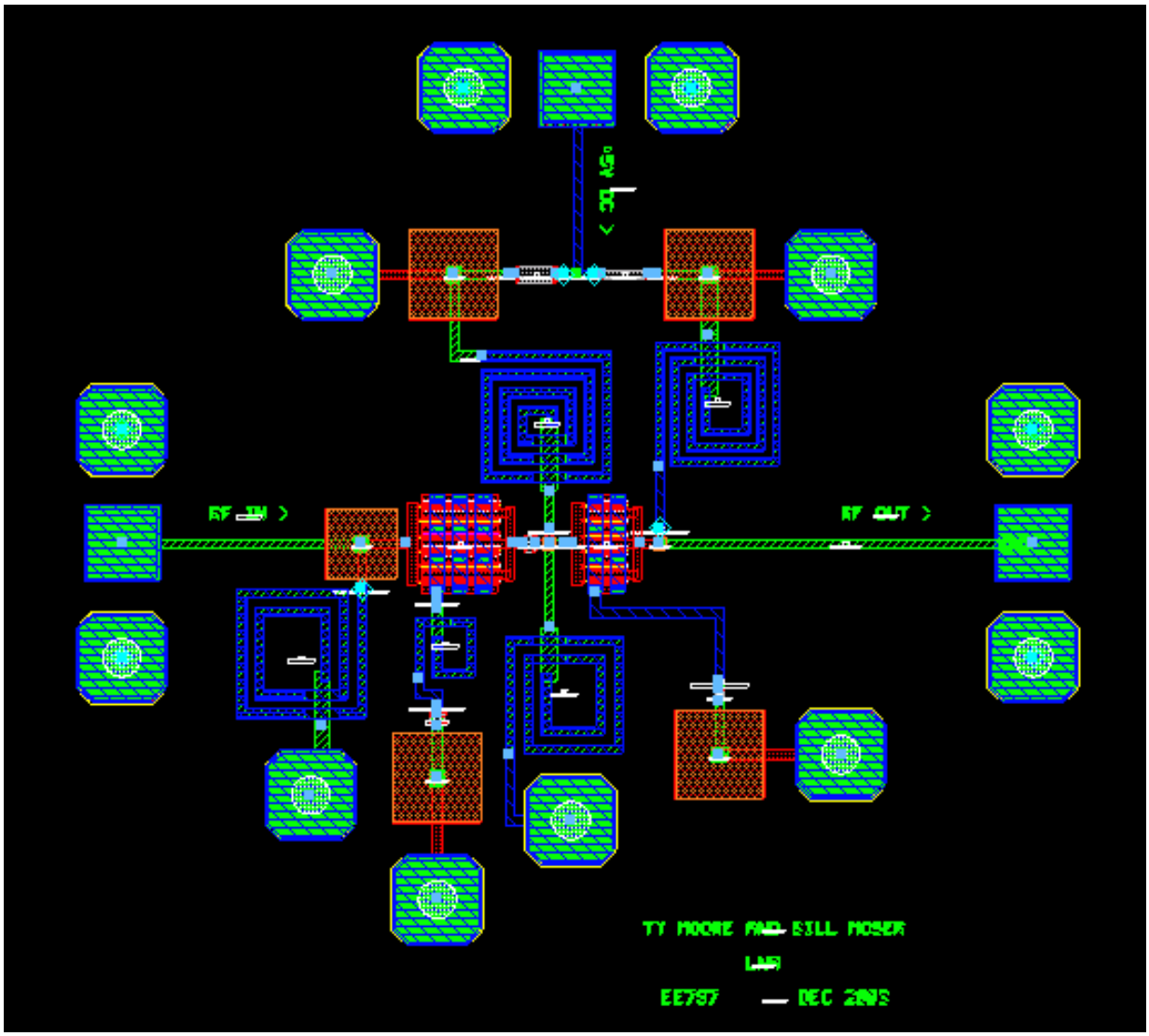
Fall 2003 JHU EE787 MMIC Design Student Project Results
Supported by TriQuint and Agilent Eesof
Professors Craig Moore and John Penn

Low Noise Amplifier—Ty Moore & Bill Moser
Mixer---Brad Mason
Post Amplifier—Henry Jeffress & Jay Walters
Driver Amplifier—Jeff Katz & John Davidson
QPSK Modulator—Aaron Johns
TR Switch—John Long & Ben Baker
Plus Special Project EE801 VCO—Mark Petty



C-Band Low Noise Amplifier
Final Report
EE525.787
Fall 2003



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Abstract

A GaAs Monolithic Microwave Integrated Circuit (MMIC) Low Noise Amplifier (LNA), operating at C-band has been designed using Agilent Advanced Design System (ADS 2003a) with TriQuint Semiconductor linear and non-linear models. The LNA is an integral part of a Simplex Transceiver chipset being developed by Professors and Students of the Johns Hopkins University, Whiting School of Engineering MMIC Design course. This paper details the design, design philosophy, design trade-offs and simulated performance of the LNA.

Introduction

The Simplex Transceiver operates in the Industrial, Scientific, and Medical (ISM) band with an RF center frequency of 5800 MHz, a 3 dB bandwidth of 150 MHz and a transmit power of ¼ Watt. The transceiver IF is 0.5 to 20 MHz and the modulation format is QPSK. The LNA is one of nine unique designs that make up the Transceiver system. Figure 1 is a block diagram of the Transceiver system.

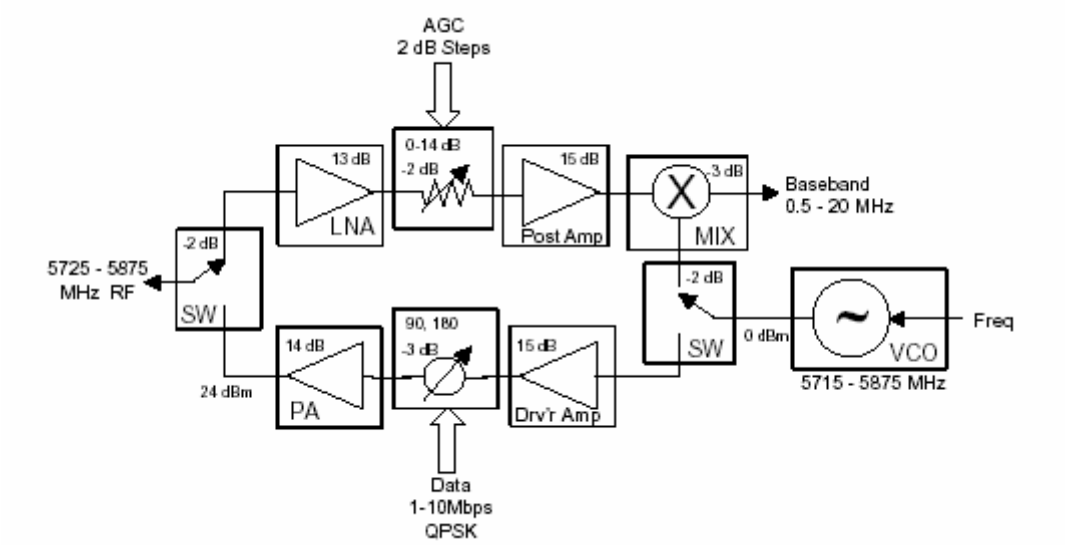

Figure 1 Simplex Transceiver Block Diagram

The RF downconverter chain noise figure is set by the noise figure of the LNA and the insertion loss of the Transmit / Receive Switch. The required LNA noise figure is 3 dB and the insertion loss of the T/R switch is 2 dB for a system noise figure of 5 dB. The required LNA gain is 13 dB, with a gain ripple of ± 0.5 dB. Input and output Voltage Standing Wave Ratio (VSWR) is specified at 1.5:1.

Circuit Description

To meet the gain specification of 13 dB a two stage design is required. The first stage is a 600 μM DJFET (6 fingers, each 100 μM wide), with Ids ≈ 15 mA. The 600 μM DJFET

was chosen to provide significant gain in the first stage while providing a reasonable noise figure. The second stage is a 300 μM DJFET (6 fingers, each 50 μM wide) with Ids ≈ 7.5 mA. A self bias configuration was chosen so that a single +5.0 Volt power supply could be used. Both FETs were biased with Vds = 2.7 V and Vgs = -0.3V. Source inductances were included on both stages for stability as well as a series stabilizing resistor on the drain of the first stage. All matching networks are included on chip.

Design Philosophy

Design of the LNA began by selecting the proper bias points for both FETs. Simulation of the FET dynamic load lines was performed using the TriQuint DJFET non-linear model. Next stability of both amplifier stages was verified as individual stages. To stabilize the first stage a source inductance of 250 pH was required along with a 20Ω series drain resistor. The second stage required a 500 pH source inductance. With the bias points and stabilizing components determined the input match of the first stage was designed for a 2.5 dB noise figure and VSWR < 1.5:1 using ideal lumped elements and the 300 μM DJFET linear S2P file. This provided a 0.5 dB noise figure margin for losses induced by the TriQuint lumped elements and microstrip traces. The 600 μM DJFET was simulated by using two 300 μM S2P files in parallel. With the input match determined the output match of the second stage was then designed to provide an output VSWR < 1.5:1. With the input and output matches determined, the interstage match was designed so that a conjugate match was presented to each amplifier. Fortunately, a simple highpass Π network provided a good match and convenient bias injection points. With the LNA now designed, stability, noise figure, gain, input and output VSWR were checked and component values adjusted as required to meet the specifications. After all specifications were met with margin the FET non-linear models were installed and the amplifier configured for self bias operation with a single power supply. Again the ideal components were adjusted so that the specifications were met with margin then replaced with TriQuint lumped elements and substrate vias. The TriQuint elements were adjusted so that the specifications were met with margin and then layout of the LNA on a 60 mil x 60 mil die (ANACHIP) began. As microstrip traces were inserted in the design the lumped elements were tuned to compensate for the degradation in performance. As the layout was performed care was taken to separate components by at least 24 μM (two trace widths) and to keep trace lengths to a minimum. Input and output pads were added to the design in a Ground – Signal – Ground orientation so that the probing station probes could be used for testing the die.

Trade-offs

Designing an LNA consists of trading gain, stability, N.F., input and output match. As the input match is altered to provide the best noise figure the gain is reduced and the input VSWR becomes larger. Stability can also be affected by the input and output match. During the design process unconditional stability over all frequencies was treated as the most important parameter. After unconditional stability was achieved the design was altered to achieve a noise figure with 0.5 dB margin. The 600 μM DJFET chosen for the first stage provided ample gain, so trading gain was not an issue. Obtaining a 1.5:1 input VSWR while maintaining a 2.5 dB noise figure was the most challenging part of the design.

Modeled Performance

Simulations of the design indicate that all specifications have been met. The following sections detail the simulation results.

Specification Compliance

Table 1 is a Specification Compliance Matrix which details the design specifications, simulated results of the simplified design, simulated results of the final design / layout and the design margin. All specifications have been met or exceeded.

Parameter	Specification	Simplified Design w/ TriQuint Components	Final Design and Layout	Margin
Operating Frequency	5725 to 5875 MHz	5725 to 5875 MHz	5725 to 5875 MHz	N/A
Bandwidth (3dB)	> 150 MHz	> 1 GHz	> 1 GHz	> 850 MHz
Gain	> 13 dB	17.6 dB	17.0 dB	4.0 dB
Gain Ripple	± 0.5 dB max	- 0.3 dB	± 0.3 dB	± 0.2 dB
Noise Figure	< 3dB	2.75 dB	1.9 dB	1.1 dB
Output IP3	> +5 dBm	+25 dBm	+24 dBm	19 dBm
Input VSWR	< 1.5:1	1.34:1	1.275:1	4 dB
Output VSWR	< 1.5:1	1.09:1	1.21:1	5.5 dB
Supply Voltage	± 5 Volts; +5 Volt, goal	+5 Volt	+5 Volt	N/A

Table 1
Specification Compliance Matrix

Predicted Performance

The LNA gain is required to be at least 13 dB with a maximum gain ripple of ± 0.5 dB and a 3 dB bandwidth of > 150 MHz. The following figures illustrate the simulated performance of the simplified design.

Figure 2 Gain - Simplified Schematic

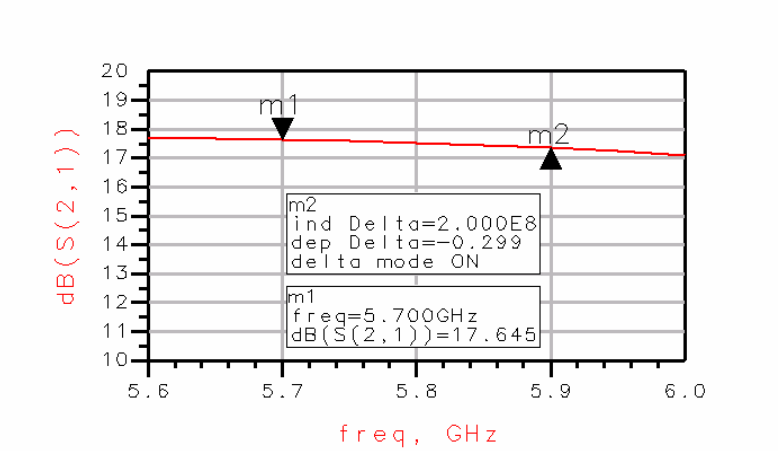

Figure 3 Gain Ripple – Simplified Schematic

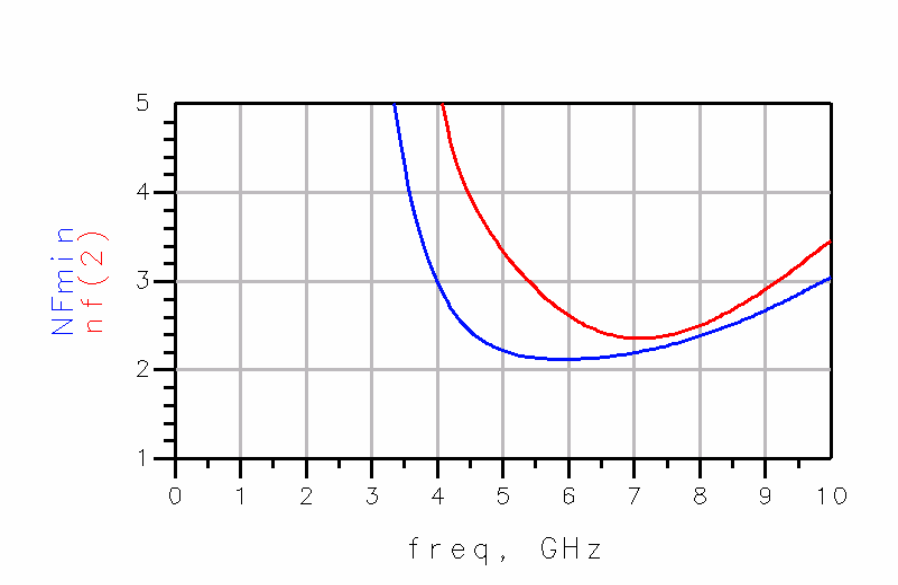

Figure 4 Noise Figure – Simplified Schematic

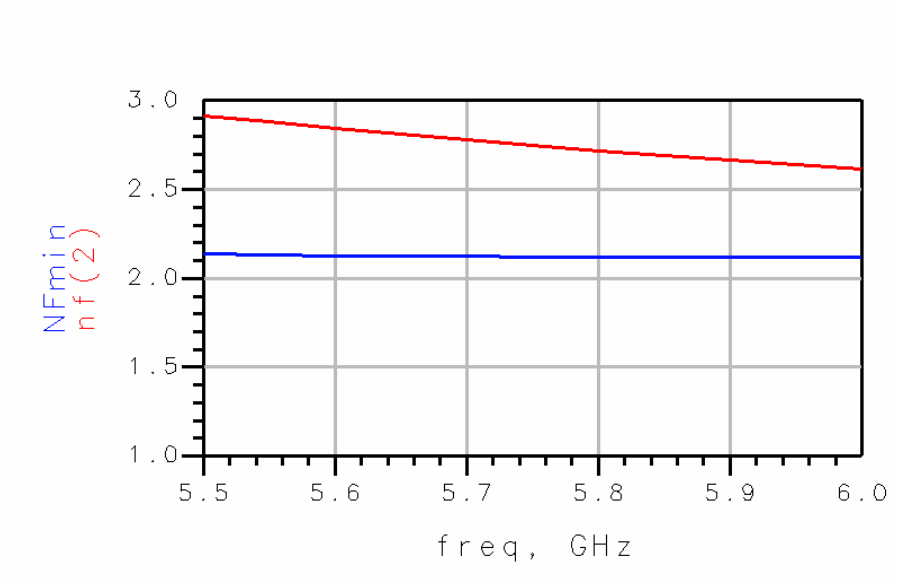

Figure 5 Noise Figure over 3 dB Bandwidth– Simplified Schematic

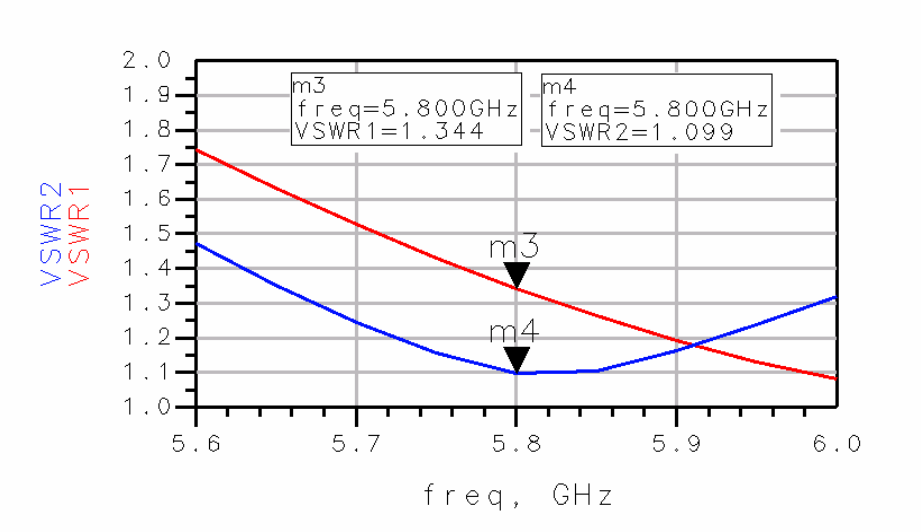

Figure 6 Input and Output VSWR – Simplified Schematic

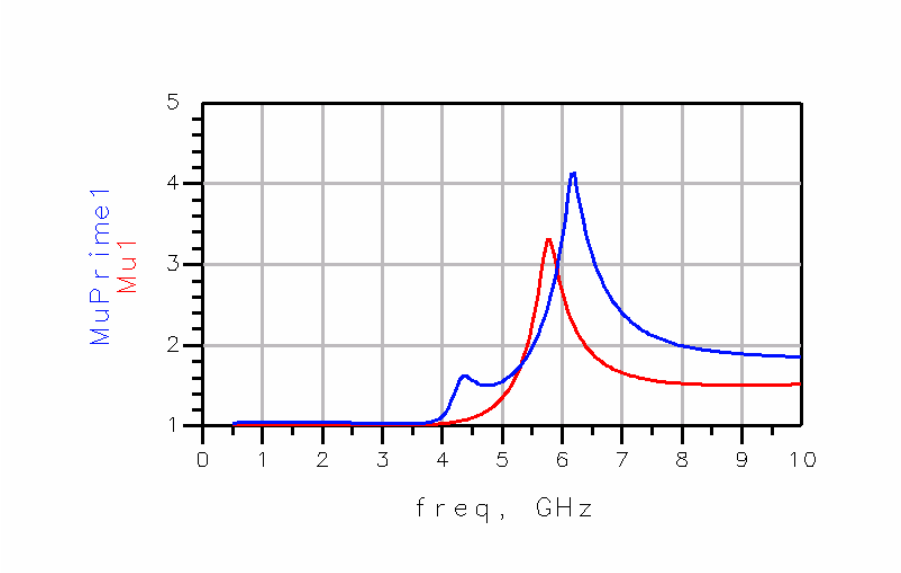

Figure 7 Stability – Simplified Schematic

The following figures illustrate the performance of the completed LNA including all microstrip connections.

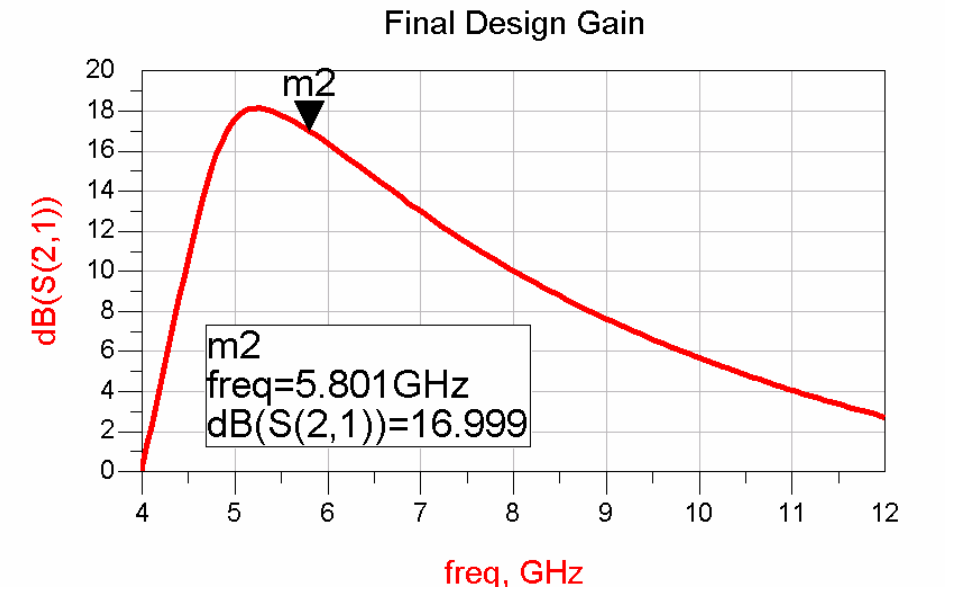

Figure 8 Gain – Complete Design

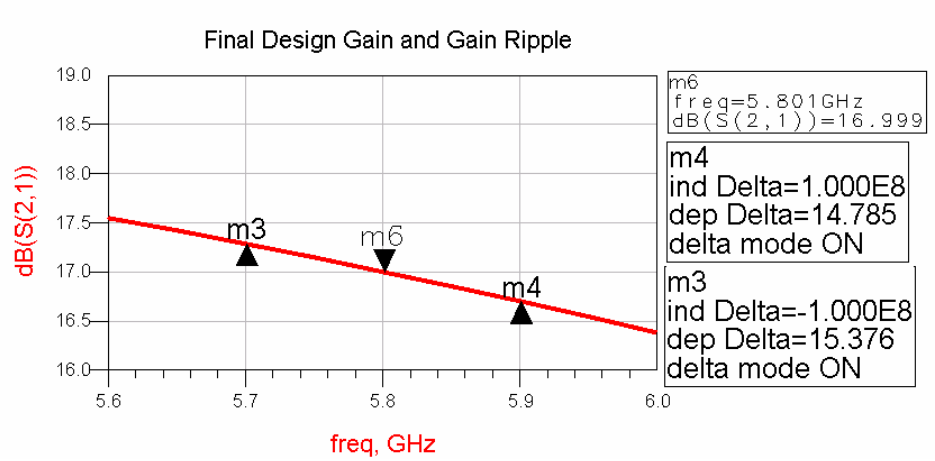

Figure 9 Gain Ripple – Complete Design

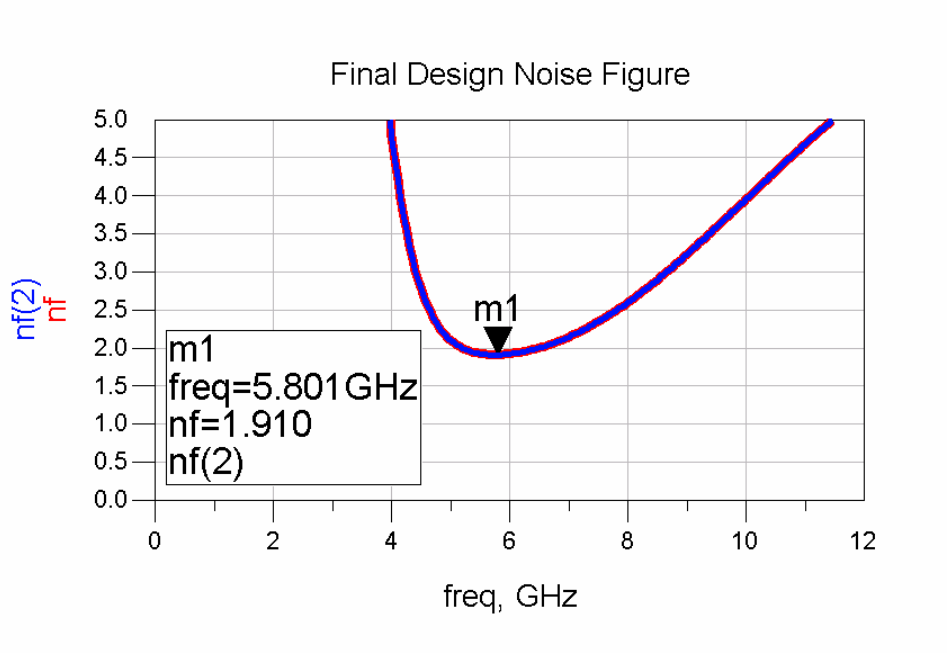

Figure 10 Noise Figure – Complete Design

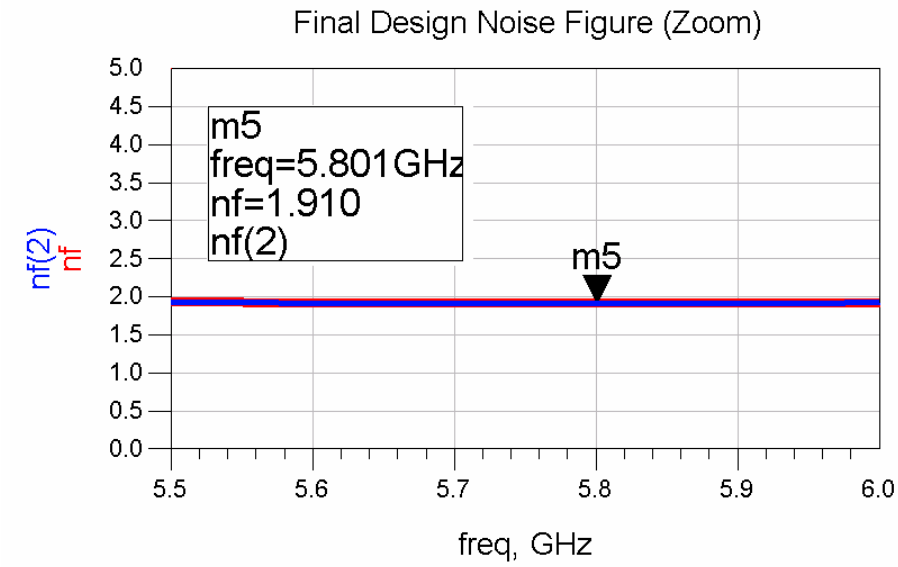

Figure 11 Noise Figure Over 3 dB Bandwidth – Complete Design

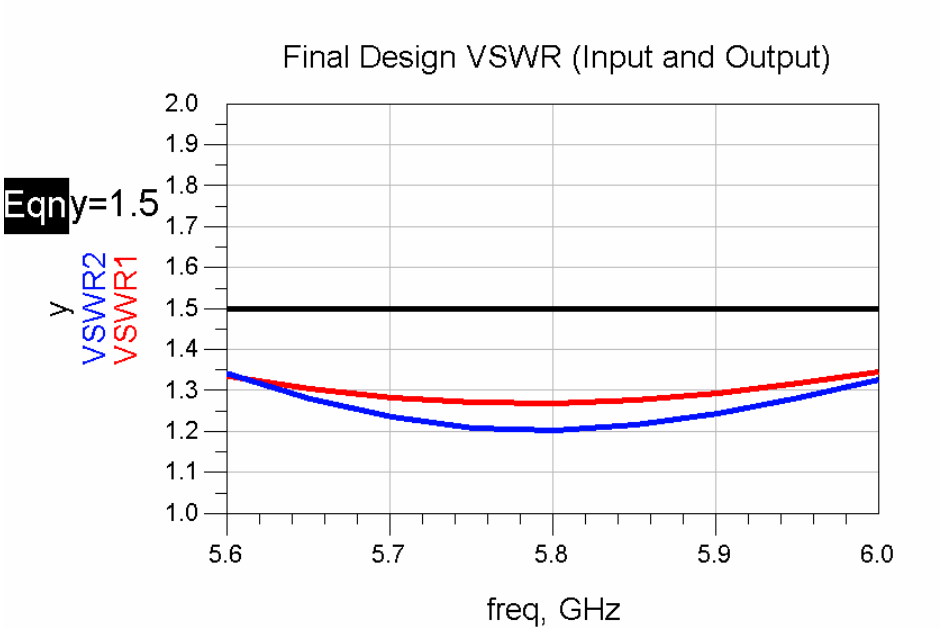

Figure 12 Input and Output VSWR– Complete Design

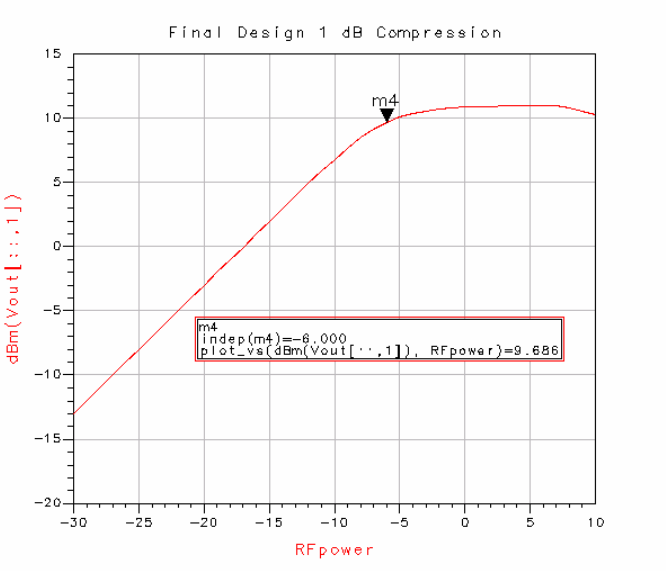

Figure 13 1 dB Compression – Complete Design

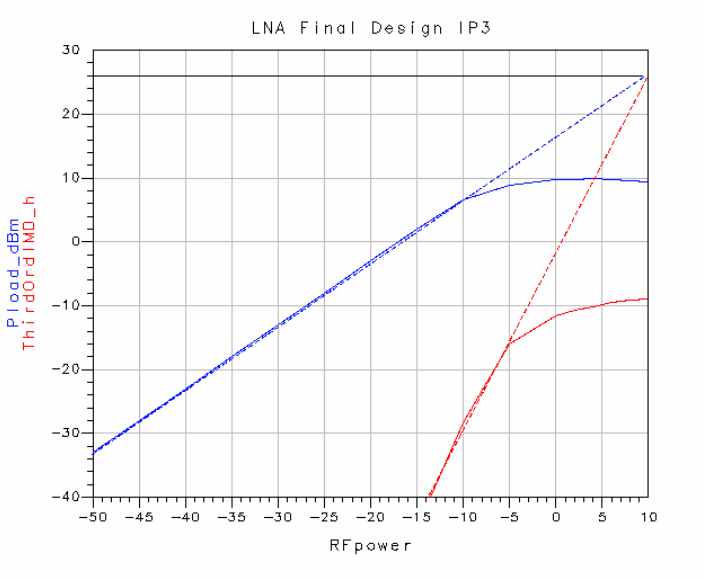

Figure 14 IP3 – Complete Design

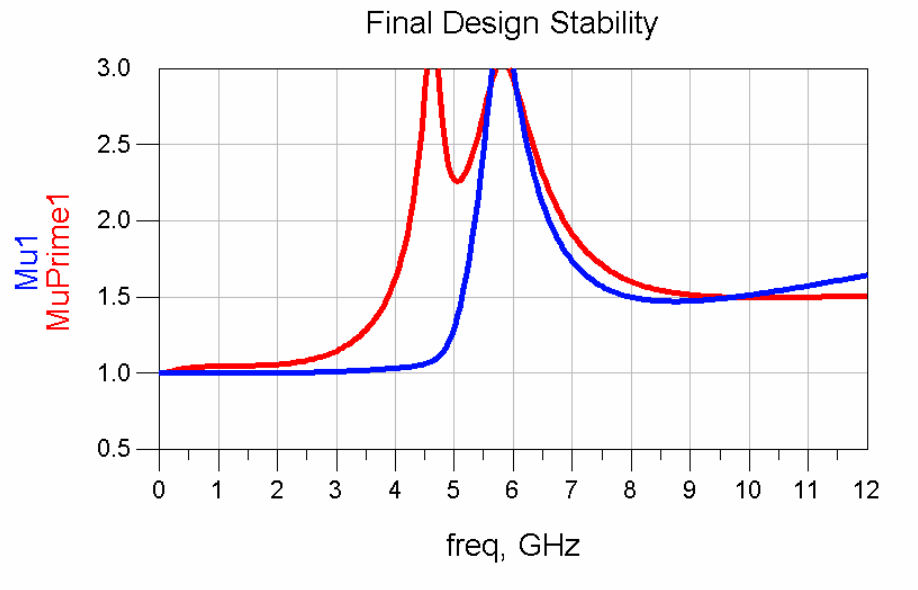

Figure 15 Stability – Complete Design

Schematic Diagrams

Simplified Schematic

Figure 16 is a schematic diagram of the design with TriQuint components, prior to layout.

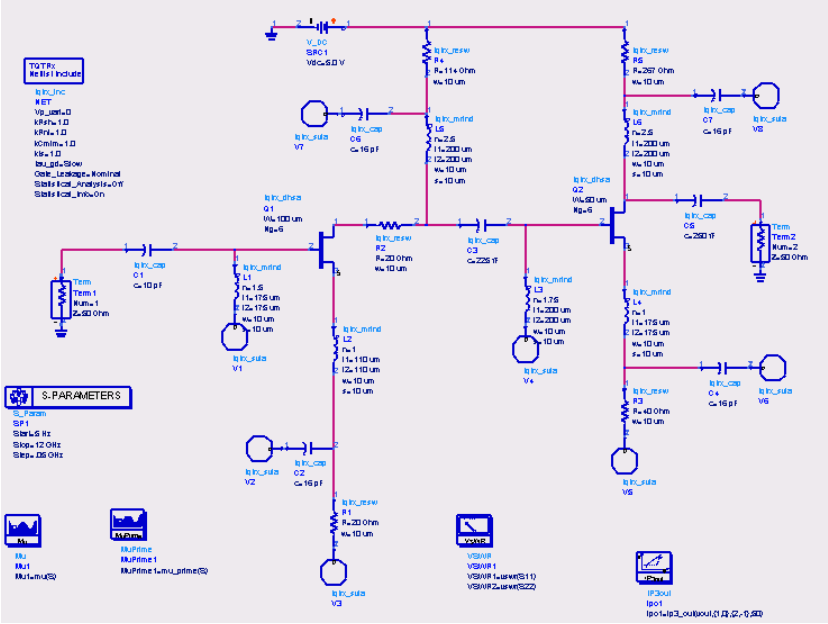

Figure 16 Simplified Design Schematic

Complete Design

Figures 17 and 18 are schematic diagrams of the final design with TriQuint components and microstrip traces. Two figures were used for clarity.

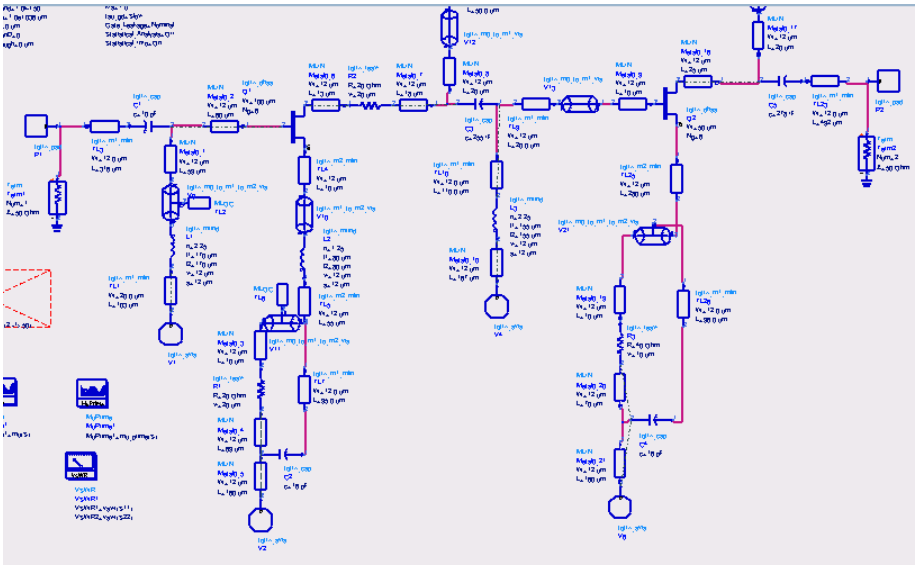

Figure 17 Final Design Schematic

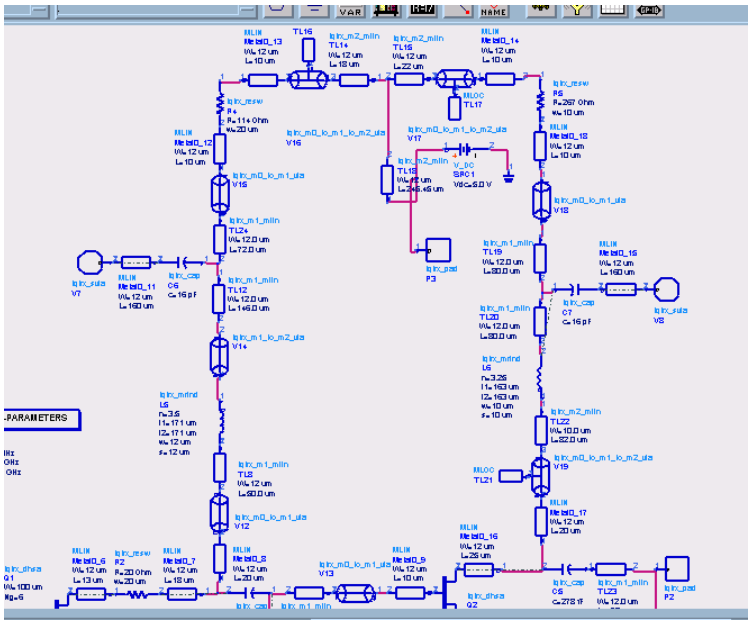

Figure 18 Final Design Schematic Continued

Final Layout

Layout of the LNA was performed with TriQuint components and microstrip traces. Interconnects were routed on Metal 1 and Metal 2 wherever possible. Those interconnects routed on Metal 0 were kept as short as possible and are 12 µM wide to provide ample current carrying capability (1.5 mA/µM = 18 mA). As microstrip traces were inserted in the design the lumped elements were tuned to compensate for the degradation in performance. This required the replacement of the second stage shunt source stabilizing inductor with a microstrip trace. As the layout was performed care was taken to separate components by at least 24 µM (two trace widths). Input and output pads were added to the design in a Ground – Signal – Ground orientation so that the probing station probes could be used for testing the die.

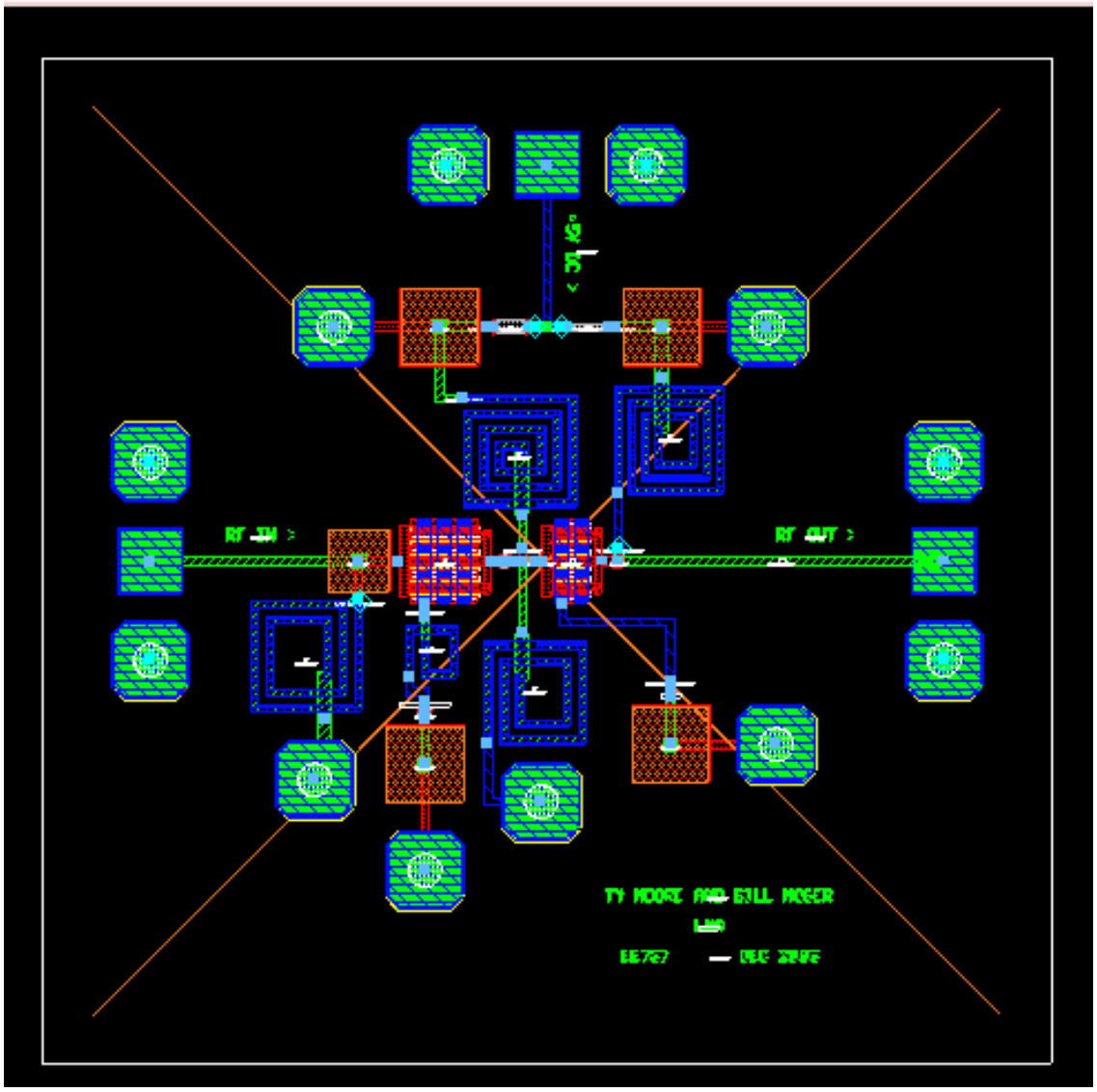

Figure 19 Final Design Layout

DC Analysis

Simplified Schematic

The input stage was designed to provide ample gain for the amplifier so that the noise figure would not be compromised by the output stage. As such, the input FET was scaled to twice the output FET (600 μM vs 300 μM) and biased so that Ids was also two times that of the output stage. Table 2 details the DC operating points of the LNA simplified design and Figure 20 is a DC annotated schematic.

Stage 1	Stage 2
Vds = 2.721 V	Vds = 2.737 V
Vgs = 0.299 V	Vgs = 0.293 V
Ids = 14.6 mA	Ids = 7.32 mA

Table 2 Simplified Schematic DC Operating Points

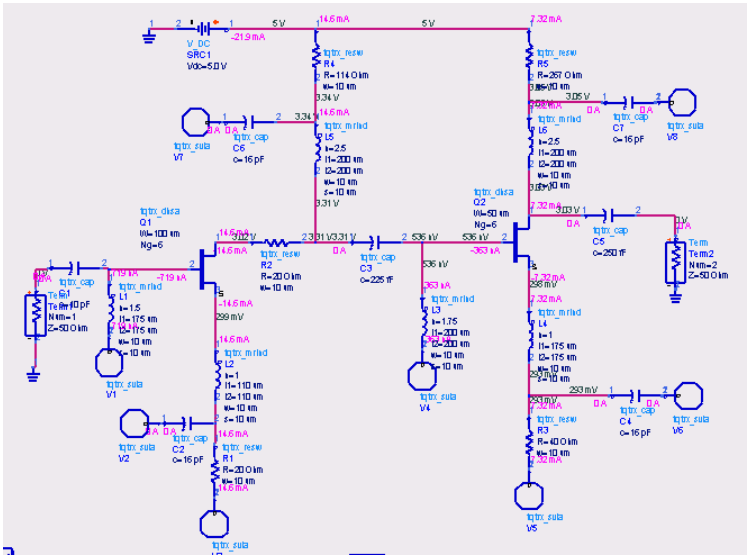

Figure 20 Simplified Design DC Operating Points

Complete Design

Table 3 details the DC operating points of the LNA complete design and Figure 21 is a DC annotated schematic.

Stage 1	Stage 2
Vds = 2.727 V	Vds = 2.714 V
Vgs = 0.293 V	Vgs = 0.296 V
Ids = 14.7 mA	Ids = 7.4 mA

Table 3 Complete Design DC Operating Points

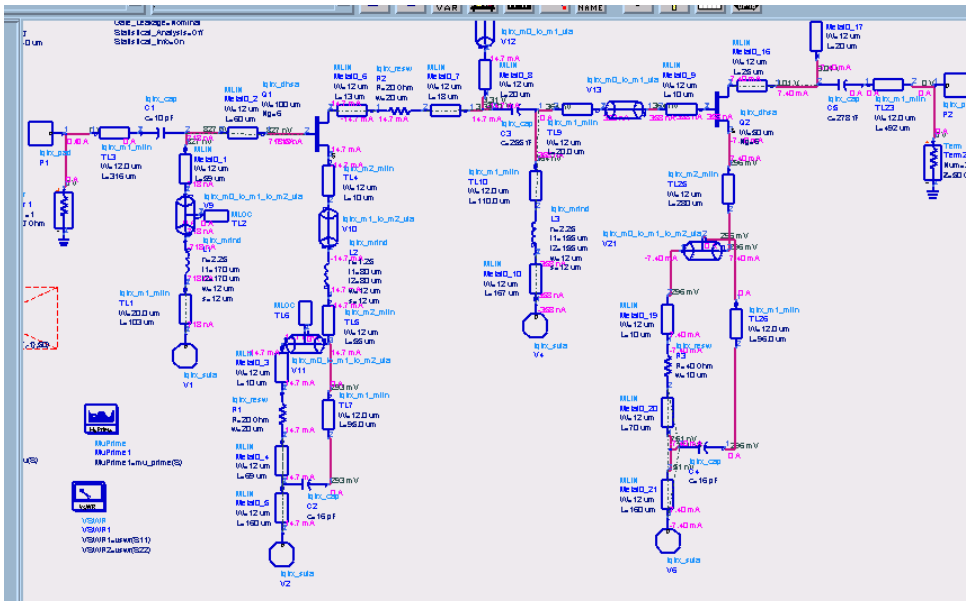

Figure 21 Final Design DC Operating Points

Component Stress

A maximum current of 15 mA is drawn by the first stage, so the resistors in this stage were sized to handle 20 mA by setting the width to 20 µM (1mA/µM). The second stage resistors carry 7.5 mA and are 10 µM wide. The overall power consumption for the die is approximately 110 mW (5 Volts @ 22 mA).

Test Plan

Verification of the LNA will require tests for noise figure, gain, VSWR (input and output), 3 dB bandwidth and power consumption. Noise figure shall be verified with a Noise Figure Meter capable of operating at 5.8 GHz while the remaining RF tests shall be performed with a Network Analyzer such as an Agilent 8510. Power consumption shall be verified by monitoring the current and voltage supplied to the die.

Test Configuration

A probing station with a Ground – Signal – Ground probe orientation is required to inject the RF signal and monitor the LNA output. An additional probe is required to provide bias to the LNA.

Turn On Procedure

Set the dc power supply for 5.0 Volts.
Set the current limit for 30 mA.
Apply power to the die.

S-Parameter Measurement

Perform a full calibration on the network analyzer from 1 to 10 GHz.

Connect the bias probe to the +5V IN pad.
Connect the input probe to the RF IN pad.
Connect the output probe to the RF OUT pad.
Perform the Turn On Procedure.
Measure S21 of the LNA and store the measurement data.
Measure S11 of the LNA and store the measurement data.
Measure S22 of the LNA and store the measurement data.
Turn off power supply.

Noise Figure Measurement

Perform a calibration on the noise figure meter at 5.8 GHz.
Connect the bias probe to the +5V IN pad.
Connect the input probe to the RF IN pad.
Connect the output probe to the RF OUT pad.
Perform the Turn On Procedure.
Measure the noise figure of the LNA and store the measurement data.
Turn off power supply.

Conclusion and Recommendations

The design of a GaAs Low Noise Amplifier operating at C-band has been completed. The LNA design meets or exceeds all design criteria in simulation and it is expected the TriQuint fabricated die shall as well. Measurements of the manufactured die will be performed, compared to the simulated results and published at a later date.

An Active Cascode Mixer With Inter-stage Matching

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Johns Hopkins Part-time Programs
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EE787 Fall 2003

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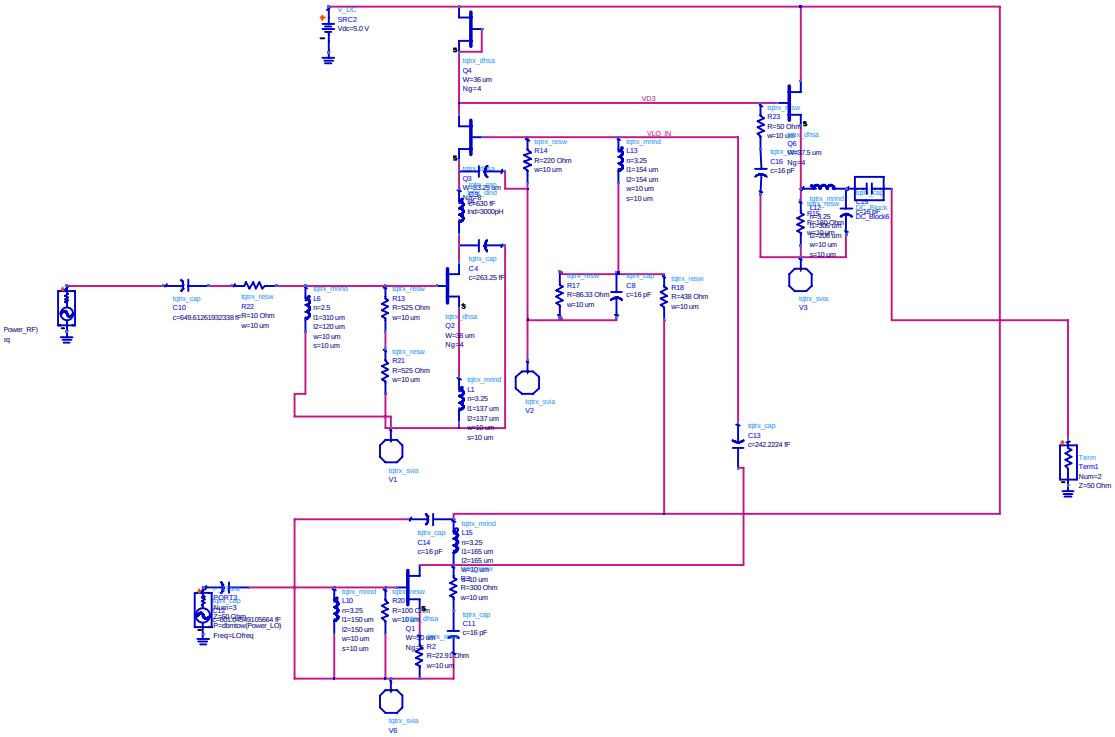
1. Abstract

The following paper presents a 5.8GHz active, down converting, mixer; producing an intermediate frequency (IF) of .5-20MHz. The circuit is a variant of the dual gate mixer. It uses two separate MESFETs and inter-stage matching to maximizing the conversion gain while maintaining the desirable isolation characteristics of the dual gate mixer. An on-chip amplifier for the local oscillator is integrated with the circuit. The entire circuit is biased using a single +5V supply, drawing approximately 250mW of DC power. The mixer and the amplifier for the local oscillator are all successfully laid out on a 60mil by 60mil chip using the Triquint TQTRX process.

RF Schematic Figure 1,



2. Circuit description

The circuit can be divided into three sections the mixer the LO amplifier and the IF buffer. The mixer can be further subdivided into the RF common source amplifier stage and the LO common drain stage. Each of these sections provides a distinct function and will be addressed separately.

The core of the design is the mixer itself. The mixer topology is based on the traditional dual gate mixer. In the dual gate mixer a FET with two gates is employed with the upper most gate being driven by the LO and the lower gate being driven by the RF. The mixing would take place as a result of the nonlinear characteristics of the IV curves of the two channels. The dual gate mixer is often modeled as a stack of two distinct FETs in a cascode arrangement. The mixer design presented here takes this model literally. Two distinct FETs are used in the cascode arrangement with inter-stage matching (See figure 1) to maximize the gain and power transfer between the LO and

the RF signals in the hopes of achieving significant conversion gains while maintaining the isolation benefit of the dual gate topology.

As in the dual gate mixer the lower FET is driven by the RF input signal. This FET looks like a common source amplifier and was designed as such (See figure 2) with the notable exception that the bias point is chosen at the edge of the saturation region to facilitate mixing when this FET is presented with the LO at the drain. In this case the matching criteria was simply to get reasonable gain. As such a simultaneous available gain match of 8 dB was the design target. (see figure 3) A source inductor and a shunt resistor at the gate, both had to be used to stabilize the amp. The input match is implemented by way of a series capacitor and a shunt inductor. This matching network provides DC blocking, and an easy access point for the DC bias to the gate at the expense of some bandwidth. Two element matches were chosen exclusively throughout the circuit due to space constraints with similar trades offs between space and bandwidth. The output matching circuit consisted of a series inductor and a shunt capacitor; which is the only feasible arrangement that will not interfere with the DC bias.

Figure 2. RF Input Schematic

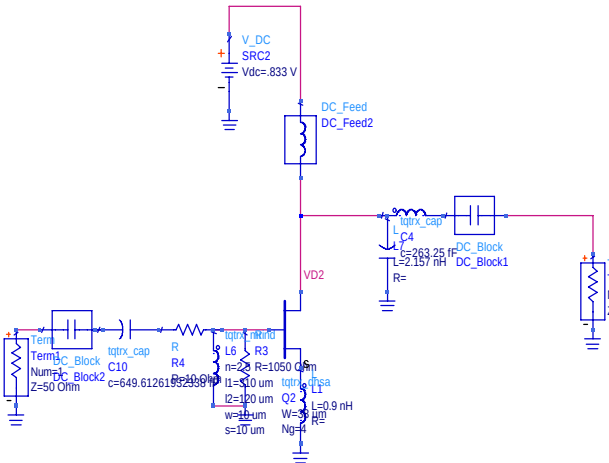
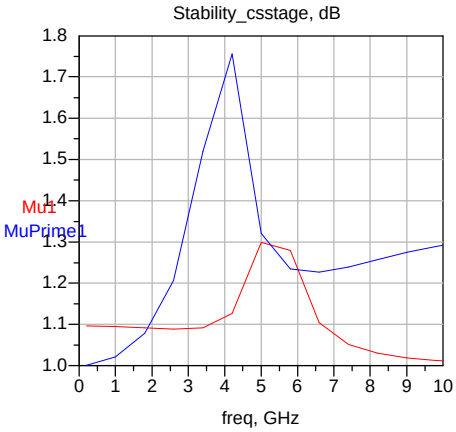
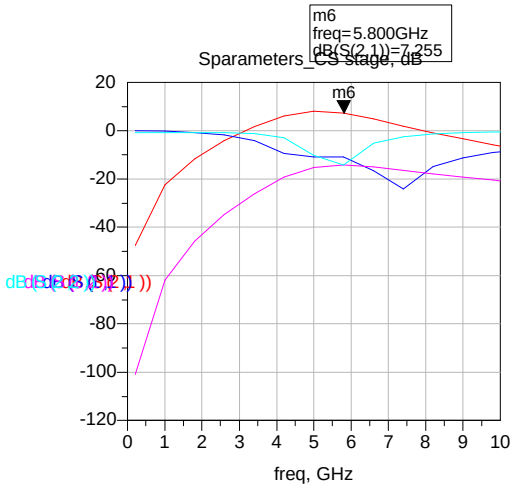


Figure 3 Sparams and stability for RF input stage





The second aspect of the mixer is the upper FET, which is driven by the amplified local oscillator (LO). The upper FET can look like any of the three basic amplifier types depending on the perspective considered. To the LO it looks like both a common drain and common source amplifier. The output of the lower FET is appears as either the output of a common drain stage or the input to a common gate stage. And to the IF port it appears as the output of either a common source or common gate amplifier. To varying degrees the upper FET acts as all

these things. The function that is most critical to our purpose is the common drain amplifier (See figure 4), because this will present the LO signal to the lower FET to facilitate mixing. Thus this matching of this circuit was designed with the idea of limiting the loss in the follower to less than 3 dB. (see figure 5) The output matching network was designed as a shunt capacitor and a series inductor as in the lower FETs output stage so as not to interfere with the DC bias of the mixer. A shunt resistor was place at the gate to aid with stability and the DC bias is provided by a resistor network that also serves to make the input to the FET appear close to 50 ohms. Upon simulating the characteristics of the input of the upper FET it was found that the input to the FET was sufficiently close to 50 ohms that an additional reactive matching network was not warranted when weighed against the space it would require.

Figure 4 Common drain LO Input.

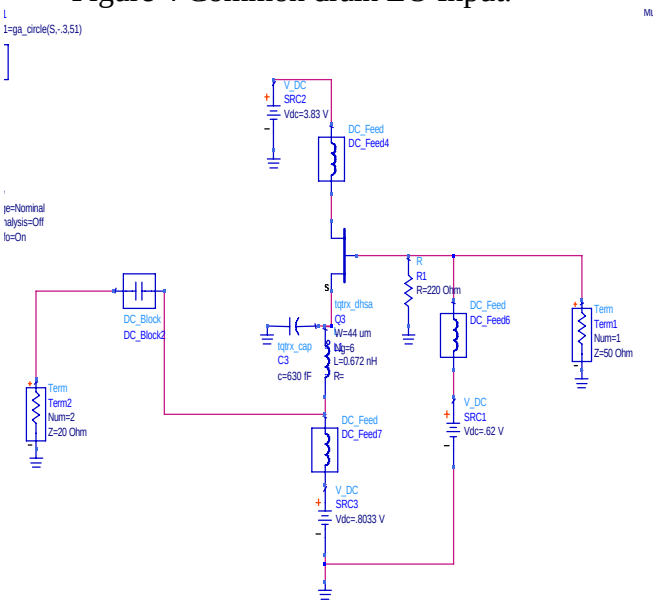
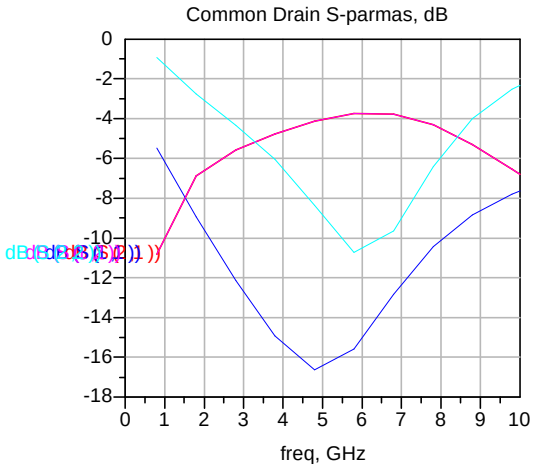
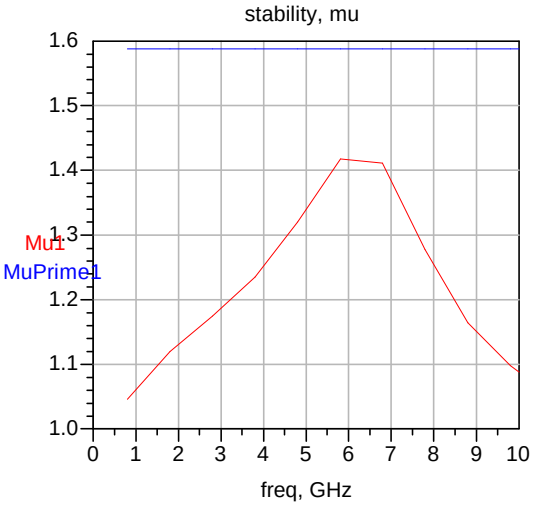


Figure 5, LO Common Drain stage Sparams and stability

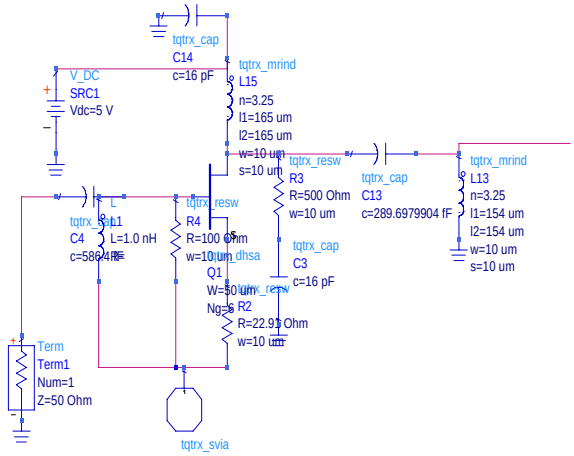




The effects of the other amplifier effects were only considered in terms of their effect on stability. The common gate stage presented to both the IF and RF signals could be beneficial in attaining conversion gain but it was not pursued in this design. The common gate and common source behaviors do present a concern for stability and as such a series resistor on the input to the lower FET and a shunt resistor on the IF port were added after the sections were combined to correct an observed stability concern.

Once the mixing takes place the IF signal, along with the RF and LO is presented at the drain of the upper FET. As the IF is .5 - 20MHz in this design Low frequency circuit concepts are easier to consider and just as applicable as RF concepts. The drain of the upper FET experiences significant loss in the IF signal when presented with a 50ohm load. The gain improves as the load resistance increases. This is a classic low frequency current drive problem and is easily addressed by adding a follower stage to the output. No input matching is needed or desired as the large, at < 20 MHz, gate impedance of the FET is the desired The final functional portion of the circuit is the LO amplifier. This is a simple common drain amplifier (see figure 6) added to gain up the LO to provide a larger LO signal to the gate of the upper FET. The only design consideration here is that the gain not be overly large, as there is a direct tradeoff between LO gain and LO to RF isolation. A gain of 7 was the design target and once again a series capacitor and shunt inductor provided the input matching to facilitate DC blocking and applying the DC bias to the gate. On the output side a shunt resistor capacitively linked to ground is added to aid stability and as always the series capacitor and shunt inductor matching network was used.

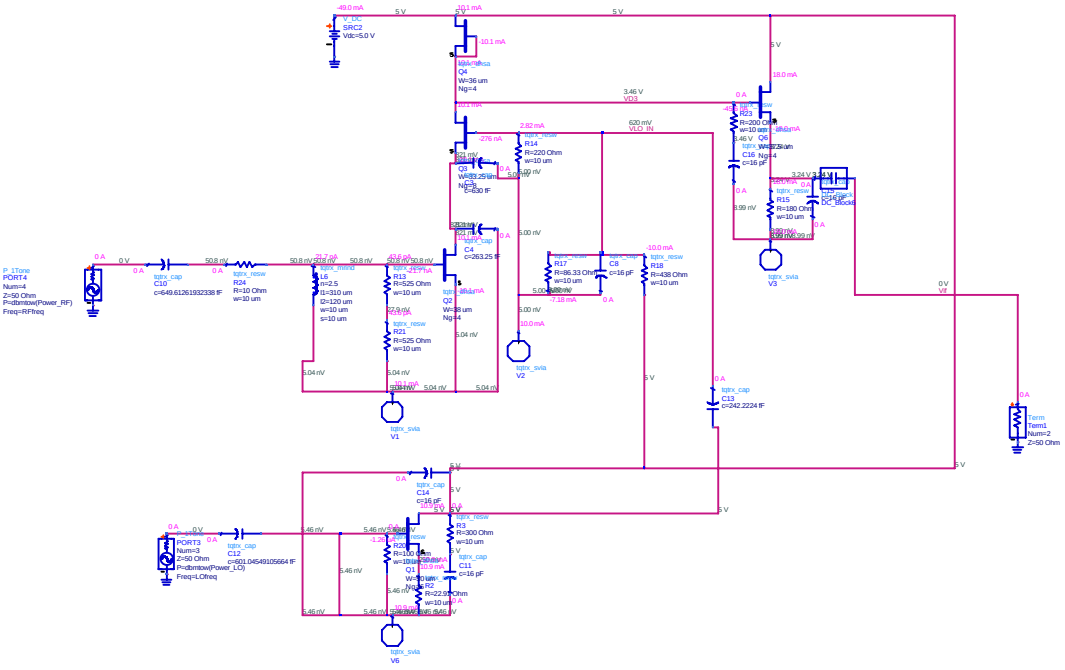
Figure 6 LO amplifier



apparent load. Passive matching on the output of the follower was not feasible due to the large physical size of components to match at < 20MHz. Filtering was opted for instead of matching as component size to effectively filter the LO and RF was much more reasonable. It is possible to match the IF by having appropriately sizes FETS in the follower stage but this was neglected due to time constraints; under the assumption that, at the IF frequency, the gains of power matching are minimal when confronted with the utility of using low frequency circuit techniques once the RF has been down converted.

Overall the various components integrated very well in simulation. The stability problem mentioned earlier was the only difficulty noted in the integration phase.

Figure 7 DC schematic.



3. DC Bias Description

The DC biasing of this circuit deserves some special attention. Care must be taken with the biasing of the cascode mixer section as one must bias a stack of FETs as opposed to a single device. The biasing is achieved by using an appropriately sized FET biased as an IDSS current source applying 10mA. (see figure 7) The controlled current is used to force the FETs to a certain VDS as opposed to the more common method of a controlled point on the IV curve and, at DC, acts like a source resistor relative to the upper FET. So, the upper FET is sized to pass slightly more current than the current source provides at a VDS small enough so as not to cutoff the current source above it (see figure 9). The gate bias generated by a resistive voltage divider but must be calculated relative to the VDS of the lower FET. It is significant to note that on must account for the stabilizing VDS forcing the FETs to a specific current. This current is fed through the upper FET and in to the lower FET that is also biased at 0Vgs and is slightly larger, so that the Vds bias will fall at the knee between the saturation and triode regions of the IV curve (see figure 8) where maximum nonlinearity occurs and the most mixing can take place. The upper FET is now biased in a modified self-bias configuration. The controlled current being forced into the lower FET pulls the VDS of the lower FET to a specific

resistor when calculating for the bias network.

Figure 8 Lower FET Bias point.

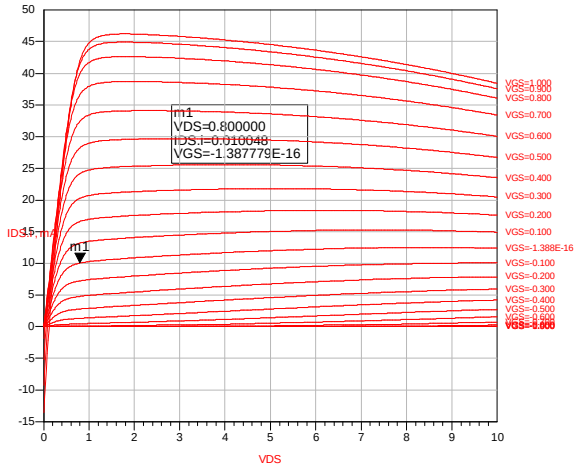
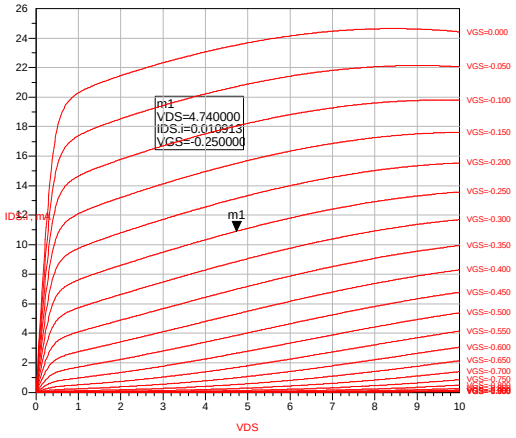


Figure 9 Upper FET bias point



The biasing of the other portions of the circuit is less involved. The follower is biased by selecting a desired current, in this case 20mA and appropriately sizing a FET for that current and providing a source resistor of a value sufficient to create the proper voltage conditions knowing that the gate voltage is the DC voltage at the drain of the upper FET of the mixer. The LO amplifier uses gate voltage of 0V and a FET appropriately sized to source 10mA configured in the classic self-bias arrangement. (see figures 6)

The Circuit Layout is shown in figure 22. Bypass caps were placed at various points on the DC 5V line and 10um lines were the standard connection between elements. The only place were current capacity was a concern was in the follower load resistor which was increased to 40um in width to accommodate the 30mA bias current for this stage. There is some concern about the use of metal one in the connection to the FETs. However, this is a part of the standard library and is beyond my control.

4. Simulation Results

The graphs below detail the relevant results. The three port S-parameters show isolation, matching and the various gains. (figure 10)
The stability plots (figures 11-13) are of questionable accuracy since I am not certain that looking at a three port network in this fashion is valid and that it completely characterizes the inter-stage stability but the unconditional stability shown in these plots does provide reassurance that some basic stability criteria are met. As an aside stability simulations were done on internal nodes using high impedance terminations. The accuracy here is also questionable but these did indicate a stability problem at an internal node and in the interest of caution this problem was corrected as noted earlier. The VSWR (figure 17) is adequate and with a little additional work it appears that reasonable bandwidth is achievable. Lastly one can see the IF spectrum that shows the mixing products and the conversion gain (figure 18). The significant gain is in keeping with the design goal of gain while maintaining isolation.

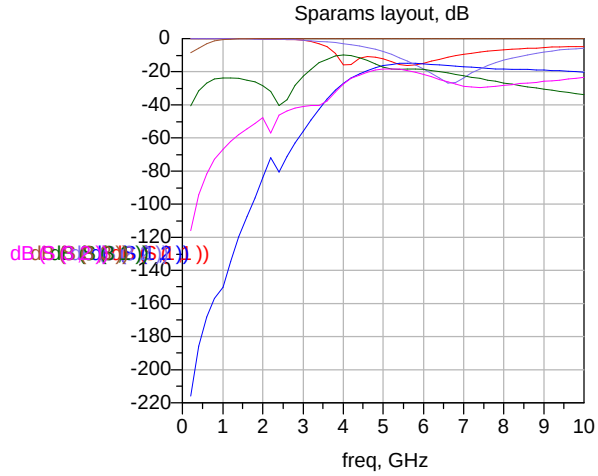
The results are shown in the following table and plots.

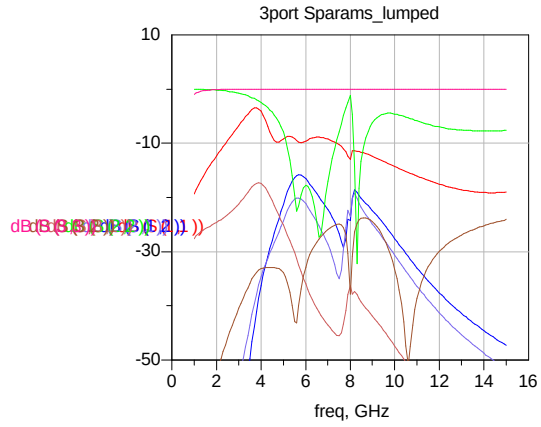
Specification Name	Conditions*	Specification requirement	Lumped Element Simulation	Layout Simulation	Measured Results
Isolation		10dBm 16 dBm goal	13dBm	14dBm	TBD
Conversion gain		-2dBm	3.99 dBm	3.55 dBm	TBD
VSWR	RF, LO, IF,	2.5 ;1.5 goal	1.3, 2.0, 300+	1.3, 2, 10	TBD
DC Icc		NA	50mA	50.9mA	TBD
Frequency range		RF 5.725-5.875 GHz LO 5.715-5865 GHz IF .5-20 MHz			TBD

***** Assume all measurements made with a –10dBm RF signal and a –2dBm local oscillator 50 ohms on all ports and a 5 volt power supply.

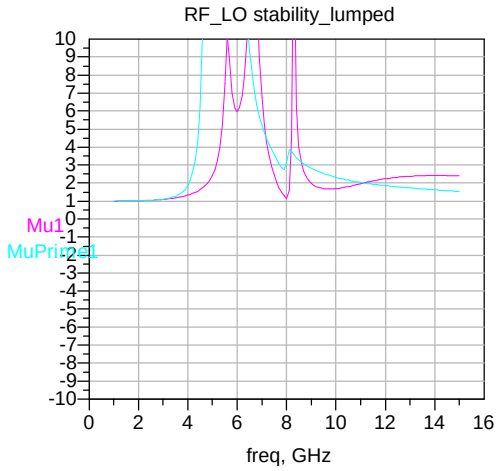
Relevant circuit characteristics.

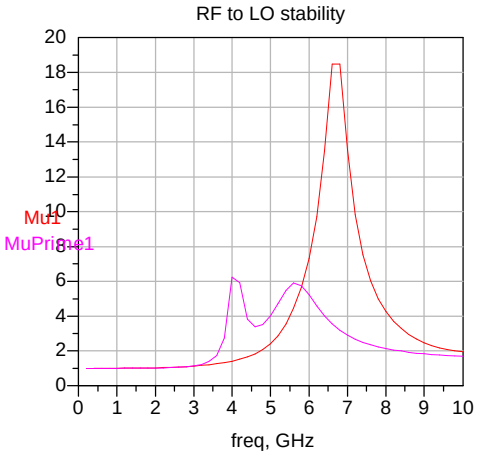
The 3 port S-parameters Lumped element and Layout Figure 13.



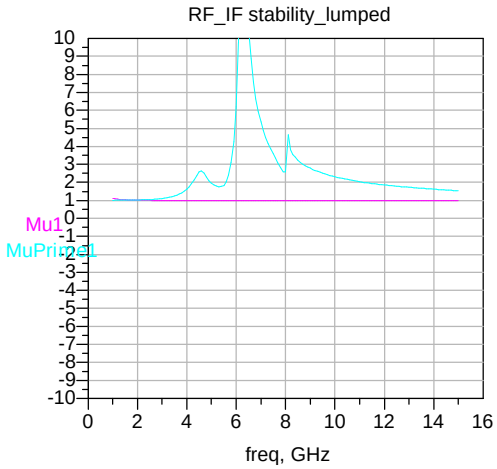


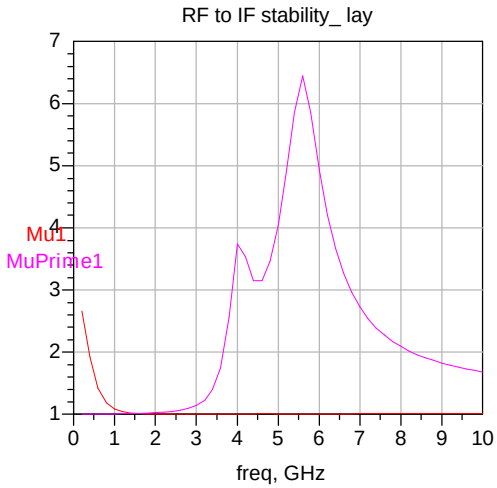
RF to LO stability Lumped element and Layout figure 11



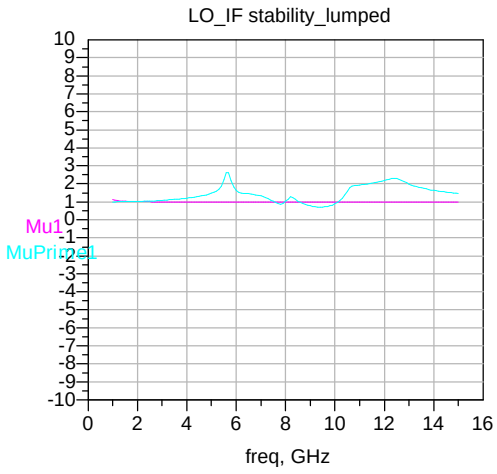


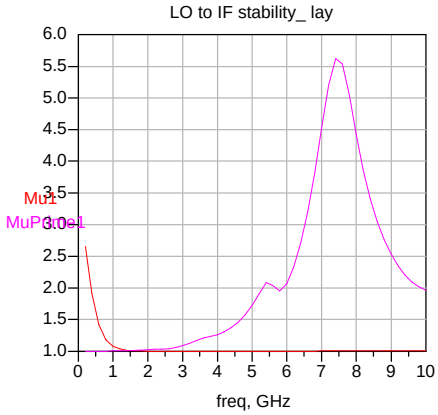
RF to IF stability Lumped element and Layout figure 12



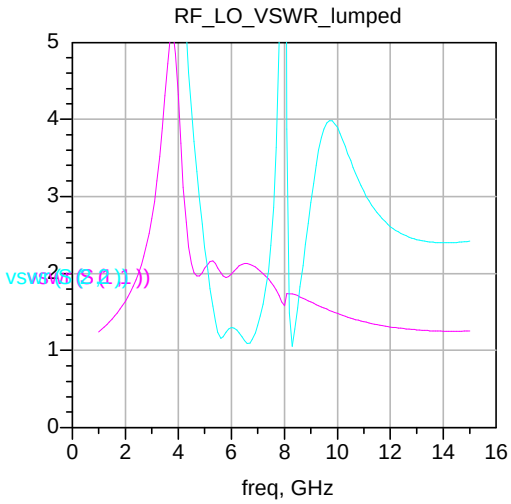


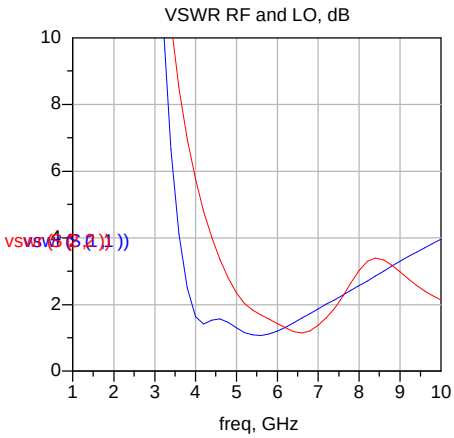
LO to IF stability Lumped element and Layout Figure 13.

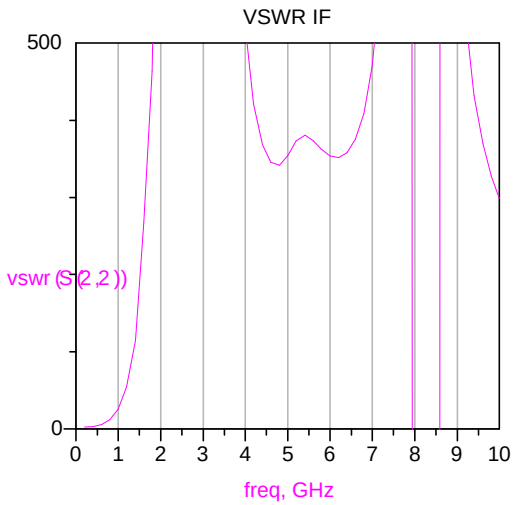




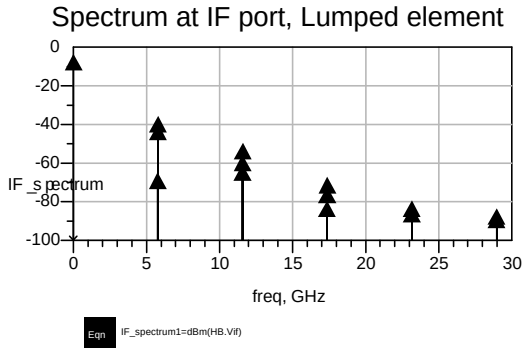
LO IF RF VSWR Lumped element and Layout figure 14.



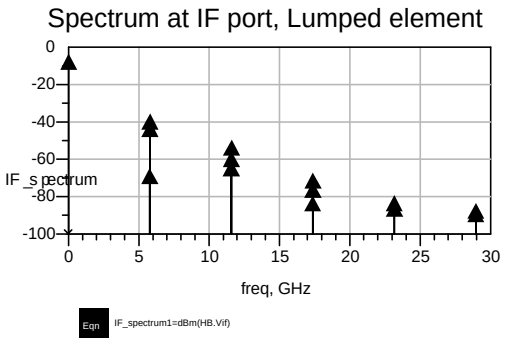




IF power spectrum Lumped element and Layout figure 15.



Output Frequency	Conversion Gain, dB
10.00MHz	5.651

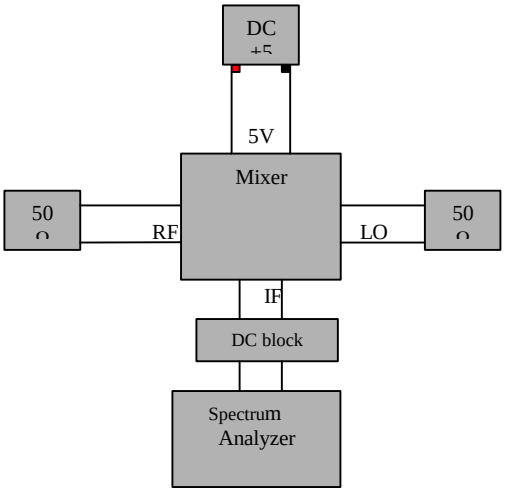


Output Frequency	Conversion Gain, dB
10.00MHz	5.651

5. Test Plan

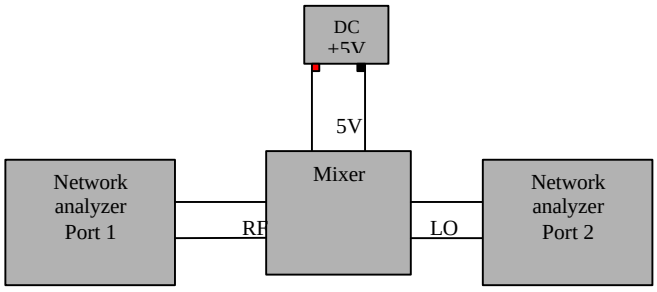
The testing of the mixer will have to be done in three stages; first a power up test, followed by a linear performance test, and concluding with a test of the actual mixing performance. When performing any tests a DC bypass cap or 100nF or more would be recommended near the probe input for additional bypass, and a DC block that will function from 500kHz to 10GHz is necessary on the IF port. The Power up test will require a DC power supply, a spectrum analyzer and two 50 ohm terminations (See figure 16)

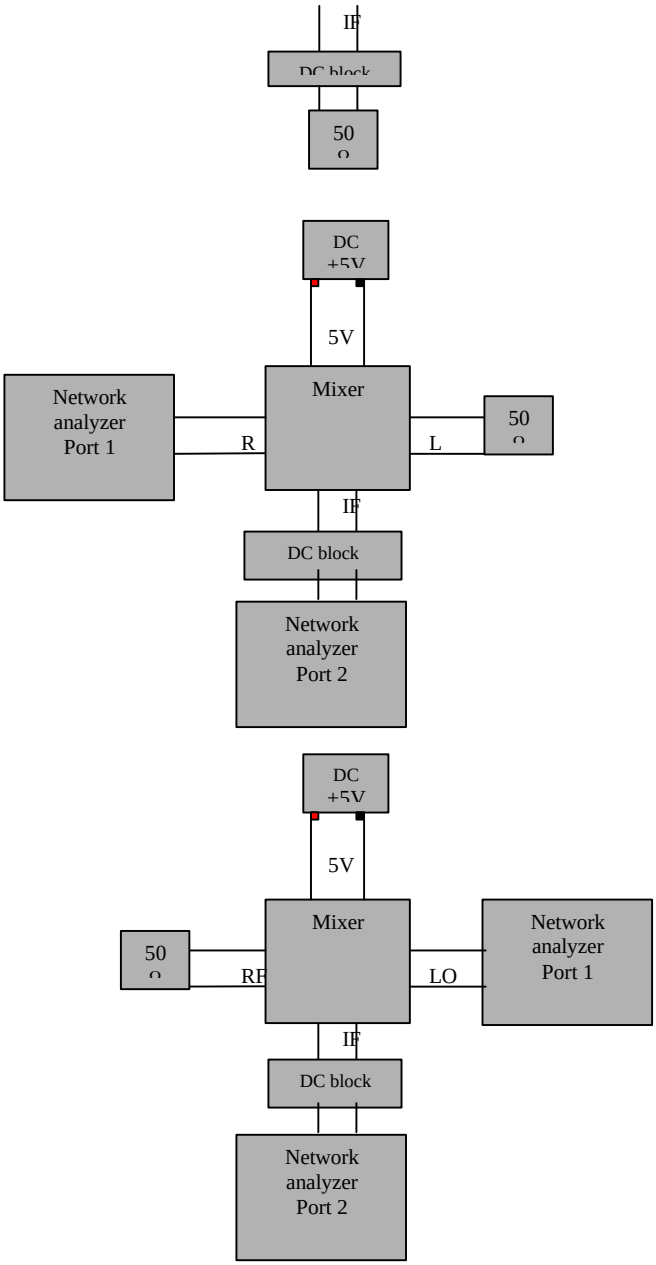
Power on test setup Figure 16.



Upon power up the supply current should be checked to see if the proper current is being drawn (50mA) the spectrum analyzer should be connected to the IF port to check for any oscillations before other tests are performed. After the power up test A liner test should be performed using a network analyzer. A series of the three Two port S-parameter will need to be taken to confirm VSWR and to make sure the frequency performance falls into the expected bands. I would measure between the LO ad RF ports first (See figure 17).

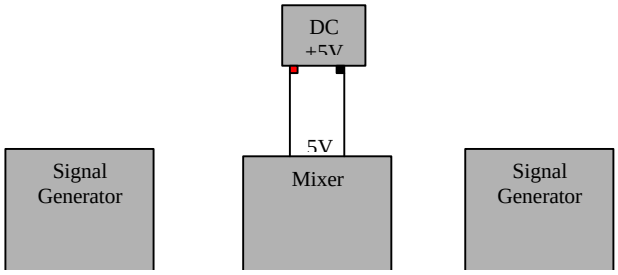
Linear Tests Figure 17.

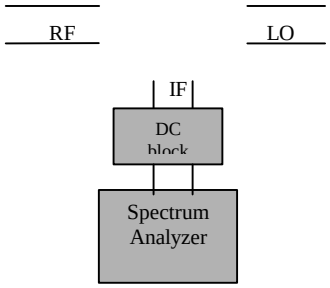




Look for bother the VSWR in the design frequency band an also observe the isolation between the two ports. Next measure the linear parameters between the RF and IF ports noting VSWR and gain/isolation at both the IF and RF frequencies. Perform the same measurements between the LO ad IF ports. Finally Using two signal sources and a spectrum analyzer measure the mixing performance (see figure 18).

Mixer test setup Figure 18.





The RF port should be driven at –10Bm and 5.7GHz and the LO port should be driven at –2dBm at 5.790 GHz. This will serve to match the measured performance. Measurements at other power levels should be made and variations in the RF an LO frequencies, with I the design range should be performed to the degree practical to confirm the performance of the circuit.

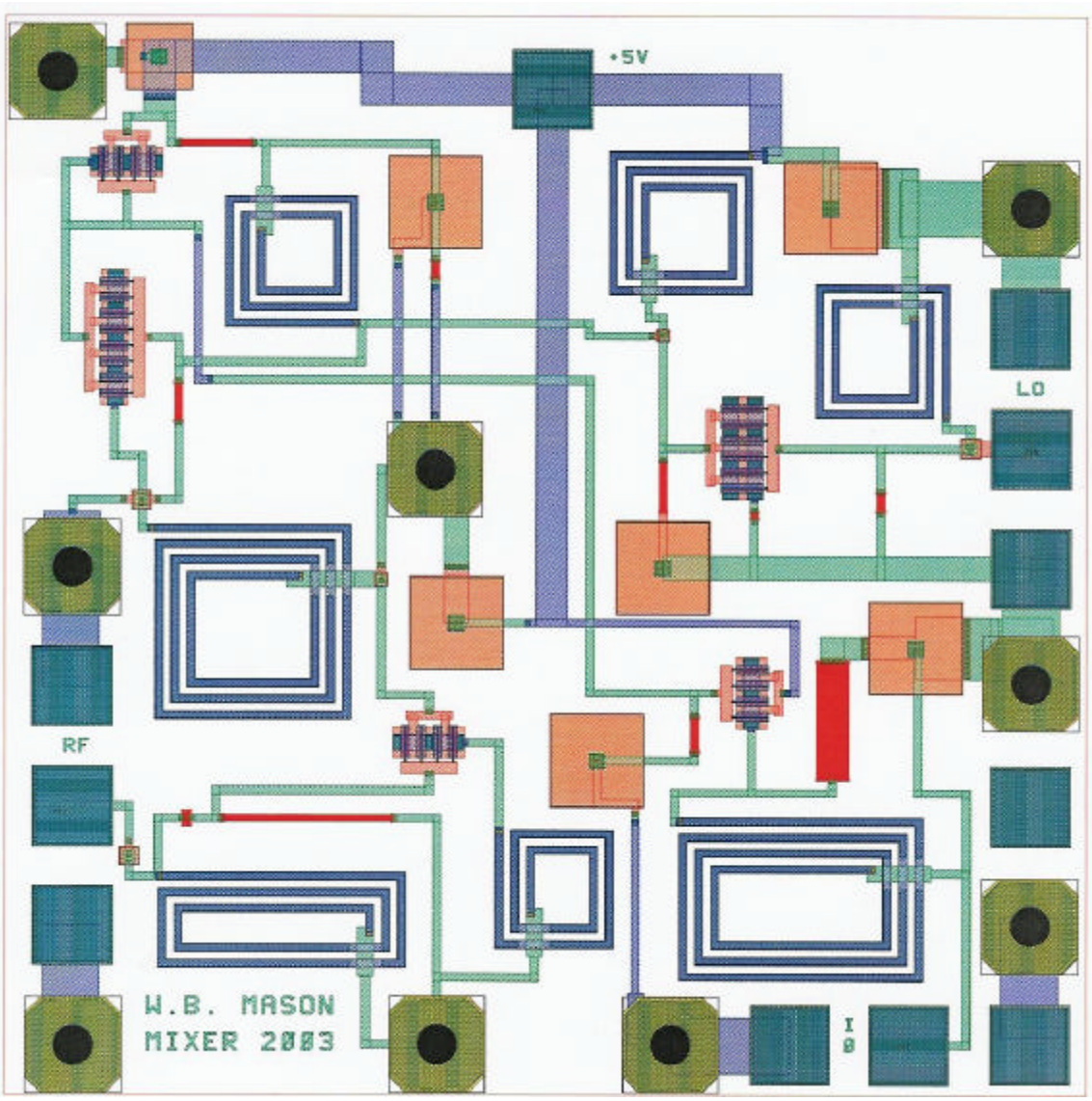
6. Conclusion and Recommendations

The simulation results seem good considering the design specifications. The VSWR and LO driver requirements and isolation all appear adequate and within spec. The fact that the mixer has significant gain is well beyond what I expected from this circuit. The major concern I am left with is stability. I was unable to design a simulation that guaranteed stability to my satisfaction thus I feel there is a potential for oscillation is some interaction between the stages that was not adequately explored. The measured results will put this issue to rest.

In terms of future work; for this design I think the difference in performance between the Layout simulation and the lumped element simulation shows a great deal of potential for optimization of the layout design. Based on my own experiments I feel there may even be more potential in the lumped element design with proper optimization. These optimizations were neglected at this time due to time constraints and the fact that the current design meets or exceeds the specifications. In addition to optimization and active matching network could be integrated into the follower stage to effect satisfactory VSWR at the IF port.

Improved filtering could be added to the IF output and the matching networks could be redesigned to optimize bandwidth. I believe that all these are possible with out increasing the size or power requirements of the chip largely through more efficient use of the layout area.

Figure 19 Chip layout



MMIC Design
EE787

Post Amplifier

Authors:
Henry Jeffress
Jay Walters

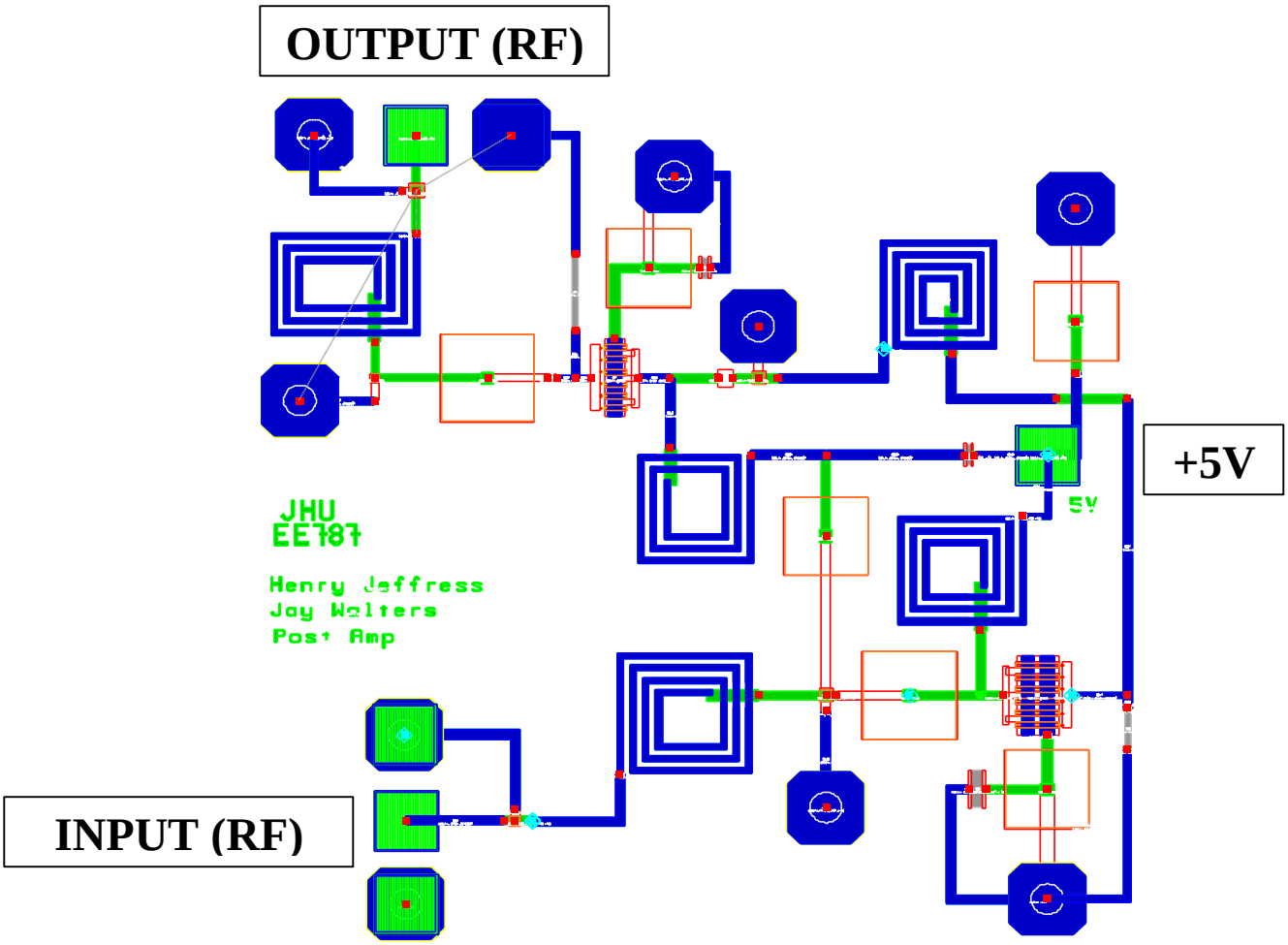
12/08/2003

Table Of Contents

ABSTRACT

This report documents the design of a post amplifier for use as part of a simplex transceiver for the C-band industrial, scientific, and medical (ISM) band. More specifically, the post amp is design to work primarily from 5.725 Ghz to 5.875 Ghz, which is a 0.15 Ghz bandwidth. For the manufacturing of our post amp we will be using a Triquint Trx process.

The Post Amp design was simulated using Agilent's Advanced Design System 2003C (ADS) software using elements based upon Triquints process. The layout was also done using ADS using a 60 x 60 mil AnaChip.



INTRODUCTION

Circuit Description

The circuit topology selected for the design was a cascaded two-stage amplifier layout requiring only one power supply. The matching networks were designed using lumped element topology.

Design Philosophy

The Post Amplifier needed to be designed with a minimal gain of 15 dB. We used this specification to first determine that we needed more than one stage. A simple analysis was run on Gfet's at different gate widths in order to determine the MaxGain of the device. This will allow the determination of the gate sizes for each stage in order to obtain the required gain. It was found that using a 200 micron GFET for the first stage and a 400 micron GFET at the second stage would give us more gain than needed which would allow room to sacrifice gain for a better match.

The first step in designing the post amplifier was to determine where the device should be biased. Determining this is simply done by using ADS's Amplifier=> DC and Bias Point Simulations => and FET IV Curves template. For maximum gain, we already had in mind that we wanted to bias the device at IDSS / 2. By correctly using the template, we determined that we wanted to bias the first stage at:
Ids = Idss/2 = .028mA = 28.0 5 V = Vds, -.88 V = Vgs
And the second stage at:
Ids = Idss/2 = .056mA = 56.0mA @ 5 V = Vds, -.88 mV = Vgs.

The next step in the design was to determine the input and output matching circuitry for the first and second stages separately. With the Cripps method in mind, this process was accomplished through the use of ADS's built in SmGamma1 and SmGamma2 functions. These functions return the simultaneous match input and output reflection coefficients. Once these were determined we used the small utility "smith.exe" to determine the matching network that would translate the match of our design to the Gamma's calculated by ADS. This produced very accurate input and output matching networks.

Upon completion of the matching networks for each stage, both stages were optimized for optimal gain, output power, and return loss. The results were analyzed using both linear and nonlinear simulated data. The two separate stages were then combined and the overall performance of the amplifier was optimized. After satisfactory performance was obtained using the ideal elements in the combined two-stage design, the ideal elements were replaced by Triquint elements. Special attention was given to the size of the Triquint elements, especially the inductors, which have been shown to be lossier than ideal inductors. The final stage of the design process was to generate a layout of the circuit that was just simulated. Considering the layout of each element during optimization was extremely helpful during the layout process. All elements were placed such that they fit withing the 60 x 60 mil Anachip and that isolation and crosstalk were

minimized. Another consideration with the layout was that of power-handling of elements and traces. Where applicable elements were enlarged and traces widened to be able to handle the current. This was only an issue in the DC Bias path. Once the layout is complete, the simulation was tweaked to add all the new element values, microstrip lines, tees, and vias and re-simulated to make sure performance was still acceptable.

Trade-offs

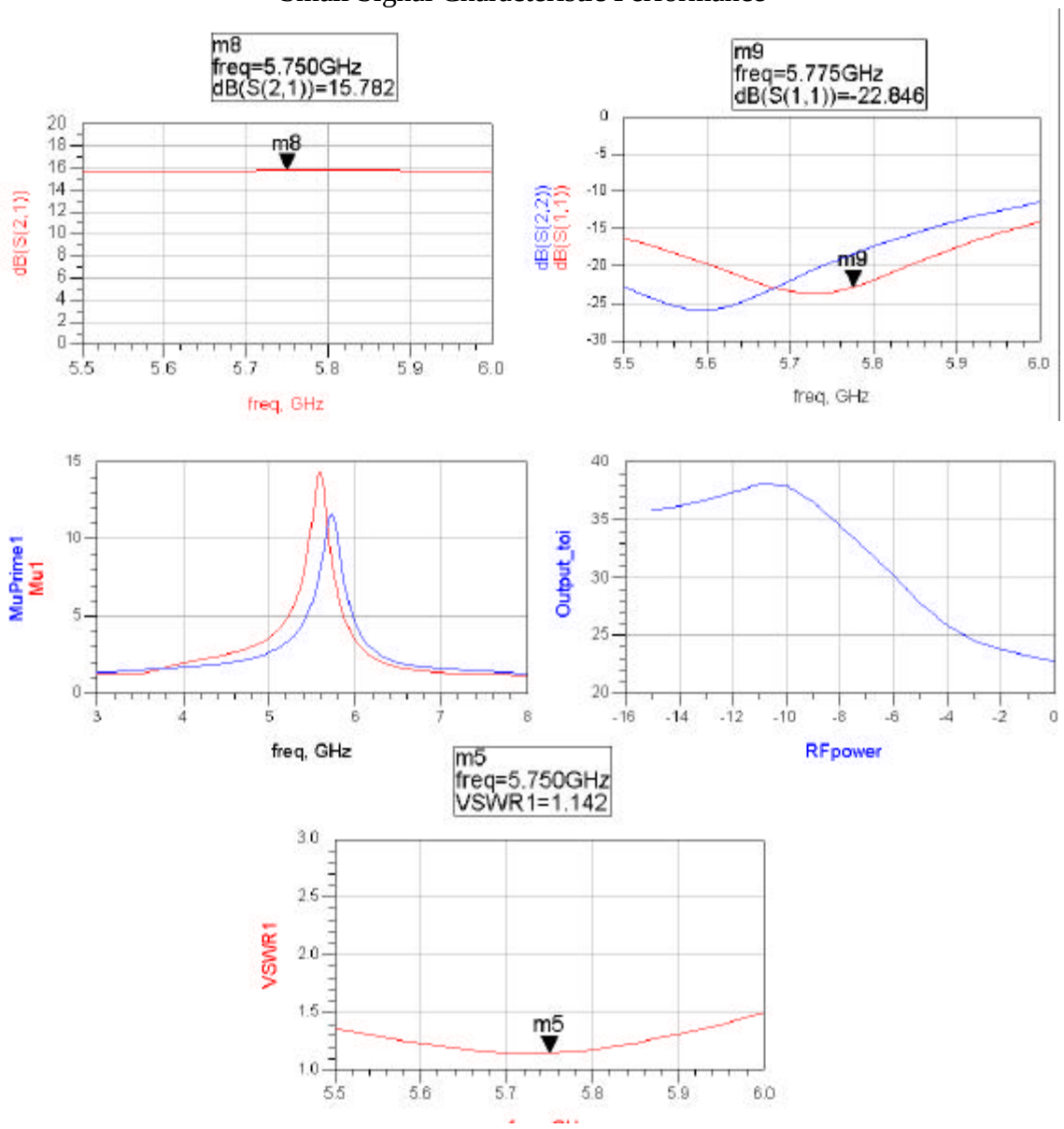
As with any design this C-Band Post Amplifier design had a couple of trade-offs. However, the ability to design the Amplifier utilizing just one power supply increased the efficiency of the design from a layout standpoint (less biasing inductors) and allowed us a great deal more versatility in the layout. Of course, nothing is perfect and sacrificing one spec. to achieve another is commonplace. The Gain, IP3, and VSWR performance were all sacrificed at some point to obtain the ideal balance between the three while still maintaining the requirements.

Modeled Performance

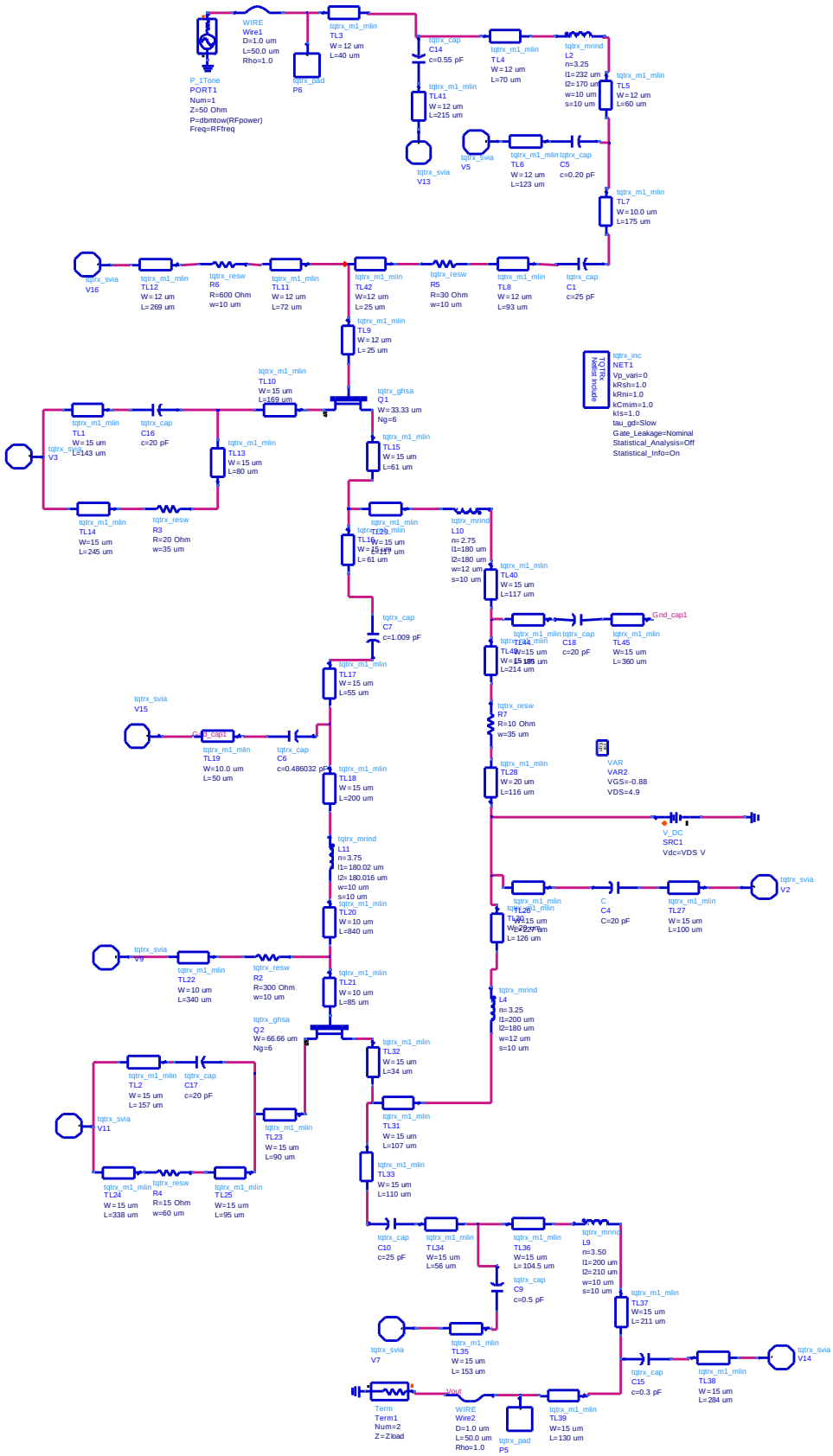
	Goal	Triquint Simulation	Final Layout Schematic
Frequency	5725 to 5875 MHz	5725 to 5875 MHz	5725 to 5875 MHz
Bandwith	> 150 MHz	> 500 MHz	> 500 MHz
Gain	> 15 dB	> 18 dB	> 15 dB
Output IP3	> + 15 dB	> +25 dB	> +22 dB
VSWR, 50 Ohms	< 1.5 : 1 input and output	1.5:1 input and output	< 1.5 :1 input and output
Gain Ripple	+/- 0.5 dB	+/- 0.25 dB	+/- 0.5 dB

Predicted Performance

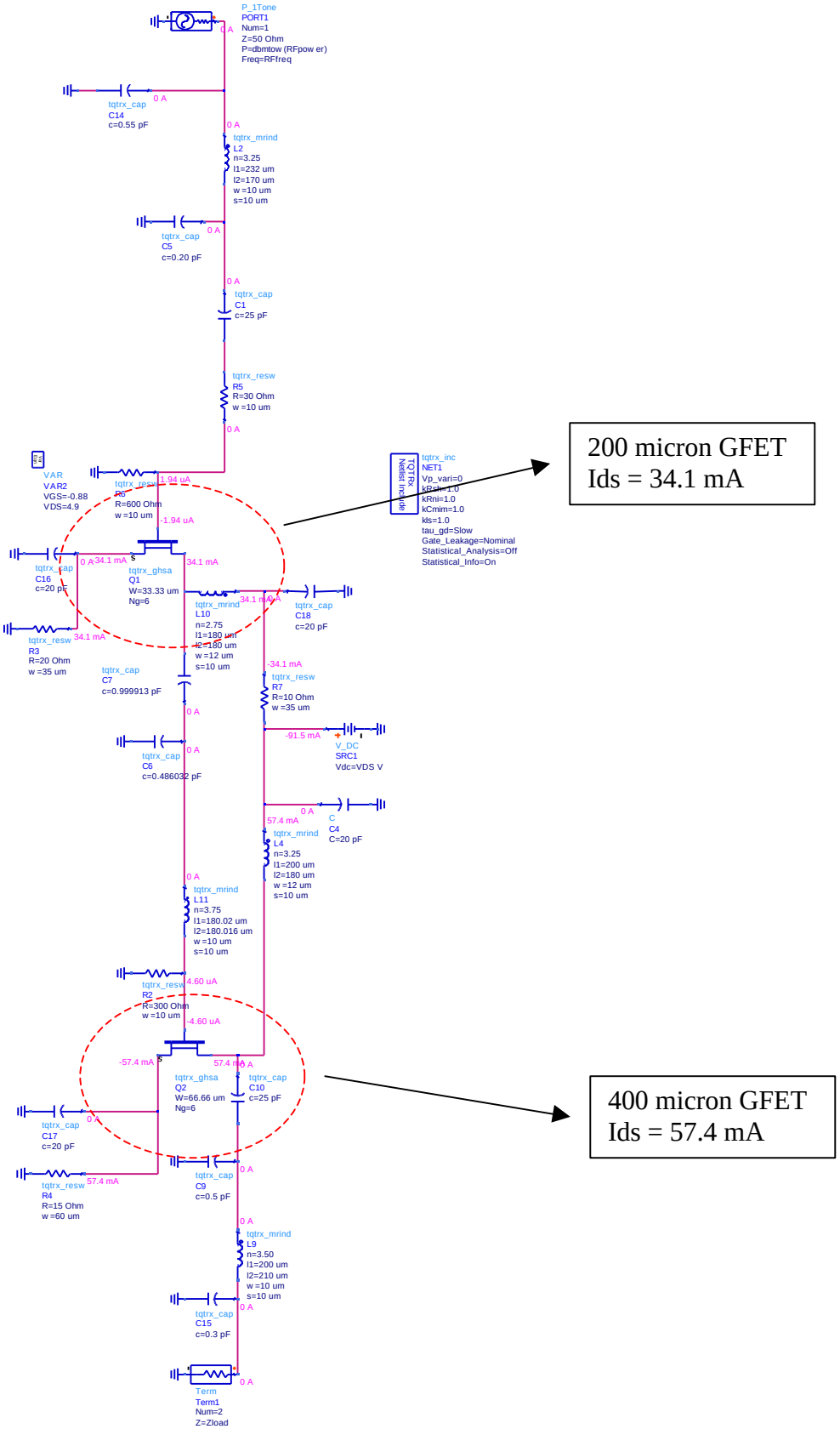
Small Signal Characteristic Performance



Schematic Diagrams



DC Analysis


P_1Tone
PORT1
Num=1
Z=50 Ohm
P=dbmtow (RFpow er)
Freq=RFfreq
tqtrx_cap
C14
c=0.55 pF
tqtrx_mrind
L2
n=3.25
l1=232 um
l2=170 um
w =10 um
s=10 um
tqtrx_cap
C5
c=0.20 pF
tqtrx_cap
C1
c=25 pF
tqtrx_resw
R5
R=30 Ohm
w =10 um
VAR
VAR2
VGS=-0.88
VDS=4.9
tqtrx_resw
R6
R=600 Ohm
w =10 um
1.94 uA
-1.94 uA
tqtrx_cap
C16
c=20 pF
tqtrx_ghsa
Q1
W=33.33 um
Ng=6
34.1 mA
tqtrx_mrind
L10
n=2.75
l1=180 um
l2=180 um
w =12 um
s=10 um
tqtrx_cap
C18
c=20 pF
tqtrx_resw
R3
R=20 Ohm
w =35 um
tqtrx_cap
C7
c=0.999913 pF
tqtrx_resw
R7
R=10 Ohm
w =35 um
-34.1 mA
-91.5 mA
V_DC
SRC1
Vdc=VDS V
tqtrx_cap
C6
c=0.486032 pF
C
C4
C=20 pF
57.4 mA
tqtrx_mrind
L4
n=3.25
l1=200 um
l2=180 um
w =12 um
s=10 um
tqtrx_mrind
L11
n=3.75
l1=180.02 um
l2=180.016 um
w =10 um
s=10 um
tqtrx_resw
R2
R=300 Ohm
w =10 um
4.60 uA
-4.60 uA
-57.4 mA
tqtrx_ghsa
Q2
W=66.66 um
Ng=6
tqtrx_cap
C10
c=25 pF
tqtrx_cap
C17
c=20 pF
tqtrx_resw
R4
R=15 Ohm
w =60 um
tqtrx_cap
C9
c=0.5 pF
tqtrx_mrind
L9
n=3.50
l1=200 um
l2=210 um
w =10 um
s=10 um
tqtrx_cap
C15
c=0.3 pF
Term
Term1
Num=2
Z=Zload
tqtrx_inc
NET1
Vp_vari=0
kRshi=1.0
kRni=1.0
kCmim=1.0
kls=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
200 micron GFET
Ids = 34.1 mA
400 micron GFET
Ids = 57.4 mA

Test Plan

The following items and test procedures are recommended to test the C-band post amplifier

Linear Parameters

Equipment: Vector network analyzer (Agilent 8510)
Probe Station
Bias Supply

Procedure:

- Calibrate the network analyzer from 0.45 to 15 GHz
- Place the bias probe on the pad of the chip labeled "+5V"
- Place probe tips on the designated pads. The input port is labeled "INPUT" and the output port is labeled "OUTPUT".
- Turn on the two power supplies.
- Record data.

Power measurements

Equipment: Signal Generator
Spectrum Analyzer

Procedure:

- Connect the signal generator probe to the input pad of the amplifier chip, which is the port marked "INPUT".
- Connect the spectrum analyzer probe to the output pad of the amplifier chip which is the port marked "OUTPUT".
- Place the bias probe on the pad of the chip labeled "+5V".
- Power supplies.
- For Pin vs. Pout set the generator to the frequency of interest and sweep the power up to, but not exceeding, 10 dBm.
- Record the measurements from spectrum analyzer after each interval.

Conclusion & Recommendations

In conclusion the C band post amplifier design was a success and met and exceeded all of the specification goals. Being able to design the post amp using just one power supply increases the complexity of the design and layout but makes the post amp more robust and easier to test and incorporate into the larger system, in this case the C-band transceiver.

EE525.787
C BAND DRIVER AMPLIFIER
MMIC DESIGN PROJECT

Jeffrey Katz
John Davidson
12/08/03

Abstract

This paper covers the design, results, and conclusions of our EE787 MMIC project. Our goal for this project was to design a C Band Driver Amplifer using a TriQuint MMIC process. This design was a part of a larger system design, which was defined in class. The system design is a C Band Simplex Transceiver at HiperLan [Wireless LAN] and ISM frequencies. Its block diagram is shown in diagram 1. From this system design our requirements were derived, which are shown in Table 1. Our GaAs substrate was defined by the MMIC process, and we were allotted a total area of 60 by 60 mil for our design. The primary tool for this project was ADS v2003a with a TriQuint library.

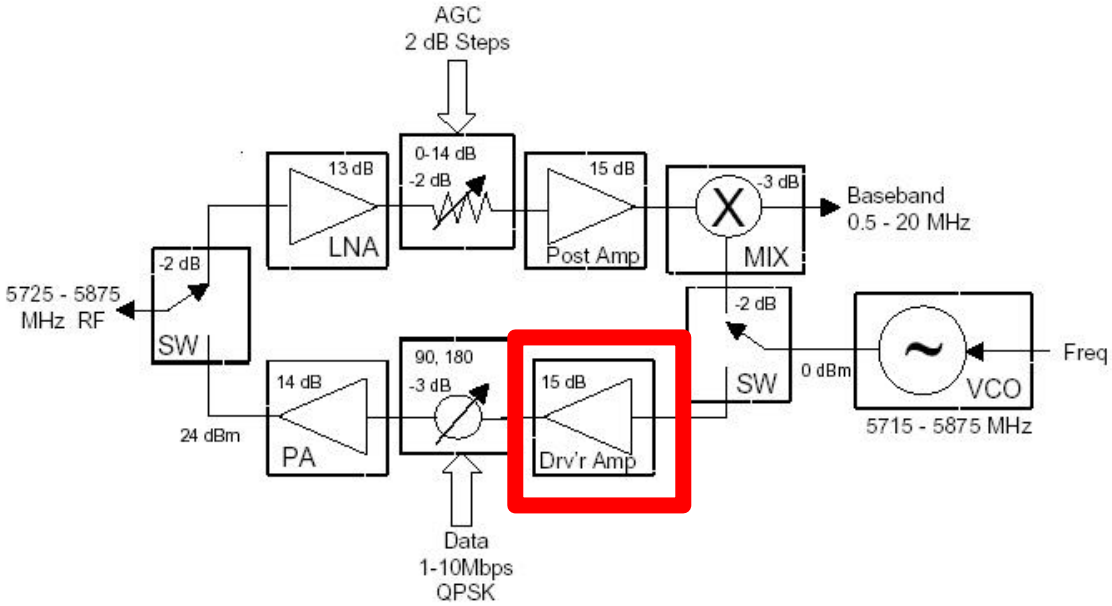


Diagram 1.

C Band Driver Amplifier Requirement

	Requirements
Frequency	5725 to 5875 MHz
Bandwidth	> 150 MHz
Gain	> 15 dB
Gain Ripple	±0.5 dB max
Output Power	> +13 dBm at 1 dB compression
VSWR	<1.5:1 input and output

Table 1.

Circuit Topology

Our circuit topology was naturally a direct result of our design requirements. Due to the amount of gain and power required and our prior knowledge of the TriQuint process and its capabilities, we knew that we would need a two stage amplifier constructed of TriQuint GFETS. We then chose the size of both FETS to be 300 micron. There were three factors in this selection: power out, the models are optimised for accuracy for the 300 micron FET, and having both stages be the same size for design simplicity. Next we chose the biasing scheme to be self biasing due to our requirement for a single supply voltage of +5 volts. Since we didn't think we'd have a problem meeting the gain, bandwidth, and power requirements we then focused on the VSWR requirements. To meet this requirement, the input and output would have to have a complex conjugate match. We chose the bias point to be roughly 60% of IDSS [The actual ended up at 67%]. Therefore after considering all of the requirements our optimal circuit topology naturally suggested itself.

FET Bias Point

Parameter	Value
Stage 1 Vgs	-0.566 V
Stage 1 Vds	3.754V
Stage 1 %IDSS	67%
Stage 1 IDS	56.6 mA
Stage 2 Vgs	-0.565 V
Stage 2 Vds	4.325V
Stage 2 %IDSS	67%
Stage 2 IDS	56.5 mA

Table 2.

Design Methodology

We began by creating a single stage, 300 micron FET with ideal matching and bias feed and blocking elements. We designed the matching elements for this single stage to be simultaneously complex conjugate matched to 50 ohms [both input and out]. Next we looked at stability. An input shunt resistor was added to make this stage more stable. We then cascaded the single stage with a second identical stage. The SMITH CHART program was used to combine the output network of the first stage with the input network of the second stage. The match between the two stages was designed to already include a DC blocking cap and a shunt inductor [that we could also use as a DC Block and a DC feed]. The input match of the first stage was also designed to naturally include a DC block. However we were not as lucky with the output match of the second stage. Next we changed the bias scheme to take advantage of our matching networks and to include the source RC network that creates the self-biasing. We chose these values based on the 67% of IDSS that we were expecting from our chosen bias point. Next we converted these ideal elements to real elements. For the large inductors we found we could get smaller layout dimensions by using MRIND's with a high number of turns. We also put a bias isolation resistor in the path to the first stages' drain. We added this resistor to prevent

feedback oscillation and stability problems. The added resistor was applied to the first stage to ensure that we didn't sap our output power in the second stage [we could afford to lower our power out in the first stage]. Next we looked at the total circuit stability and ensured our design was stable as a whole. Finally we proceeded to layout and DRC. In our DRC we found that we routed too many high current bias paths thru narrow metal zero and NiCr Resistors. We either widened these paths or changed to another metal layer. We then tuned all of our elements to ensure we met requirements.

Layout and Schematic

Please see the following schematic and layout depictions for our final circuit topology and design.

Layout

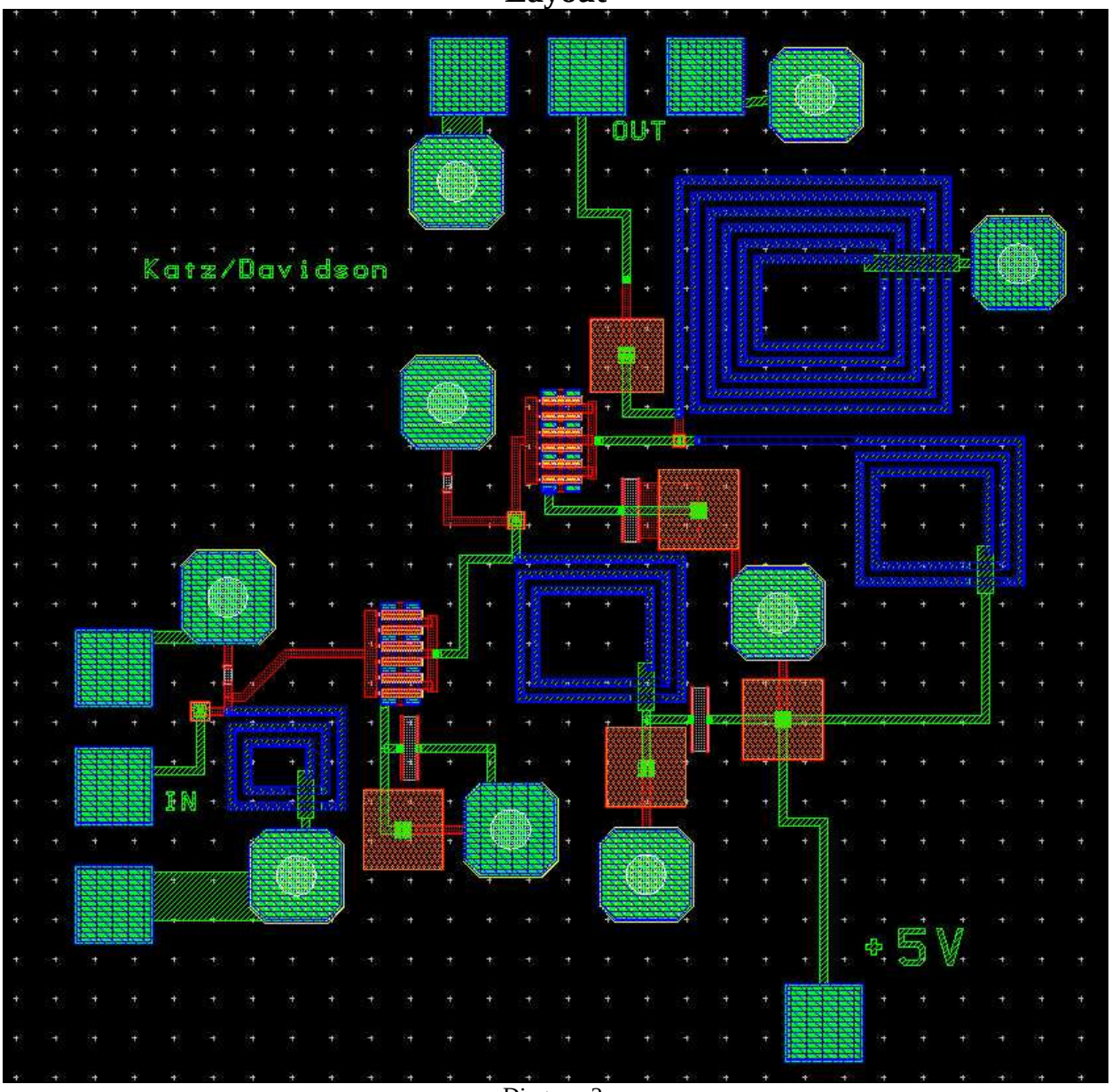


Diagram 2.

Simplified Schematic

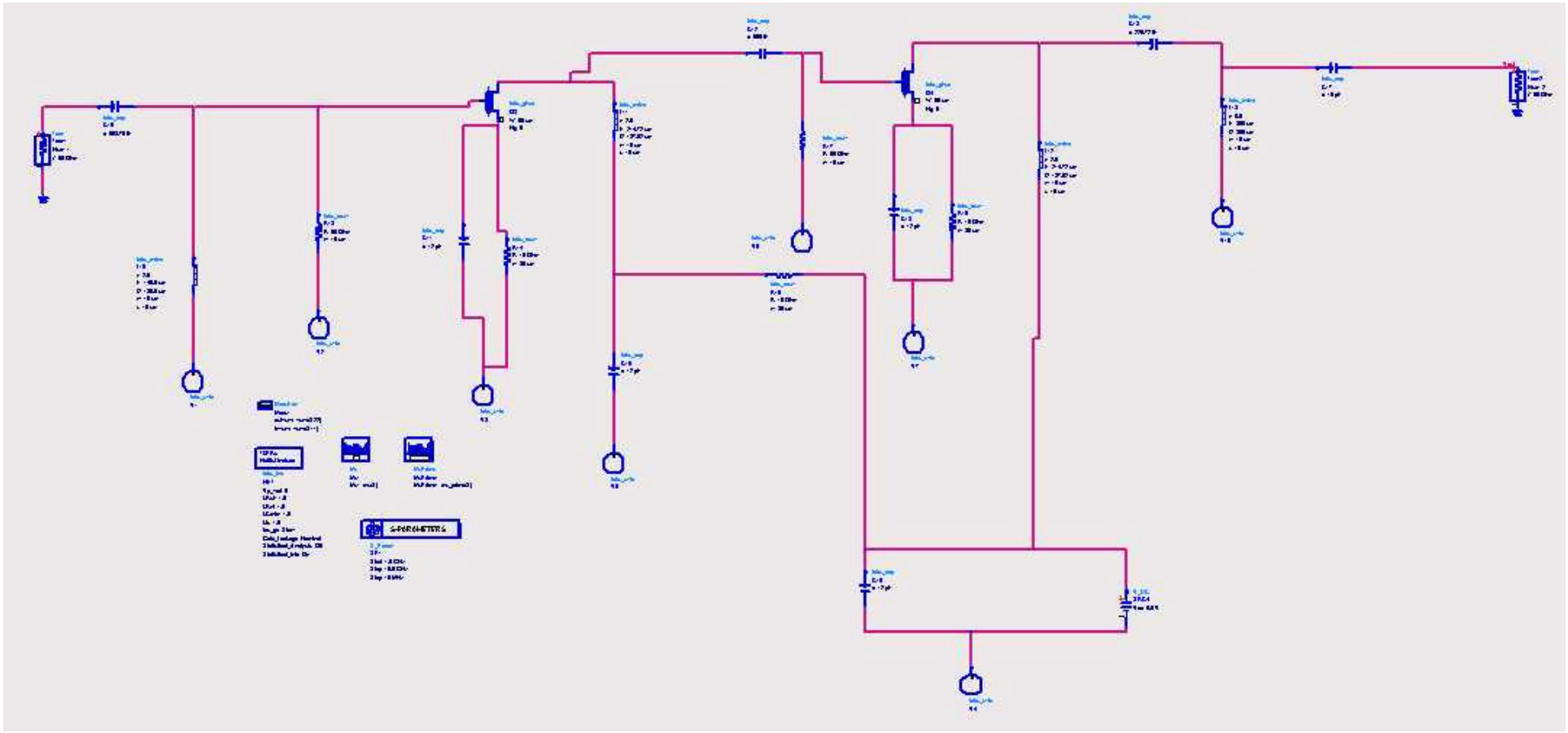


Diagram 3.

Schematic - ALL

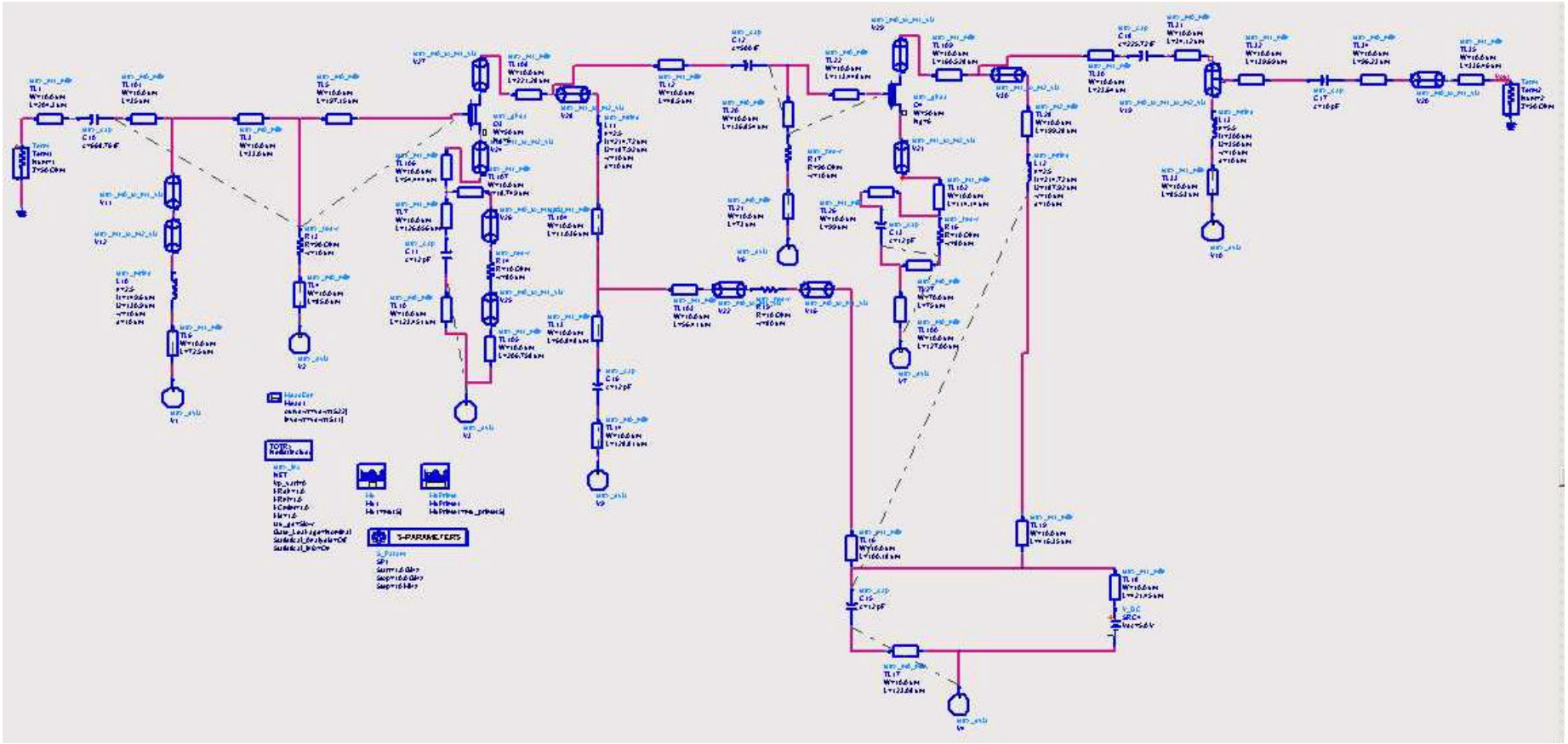


Diagram 4.

Schematic – Part 1

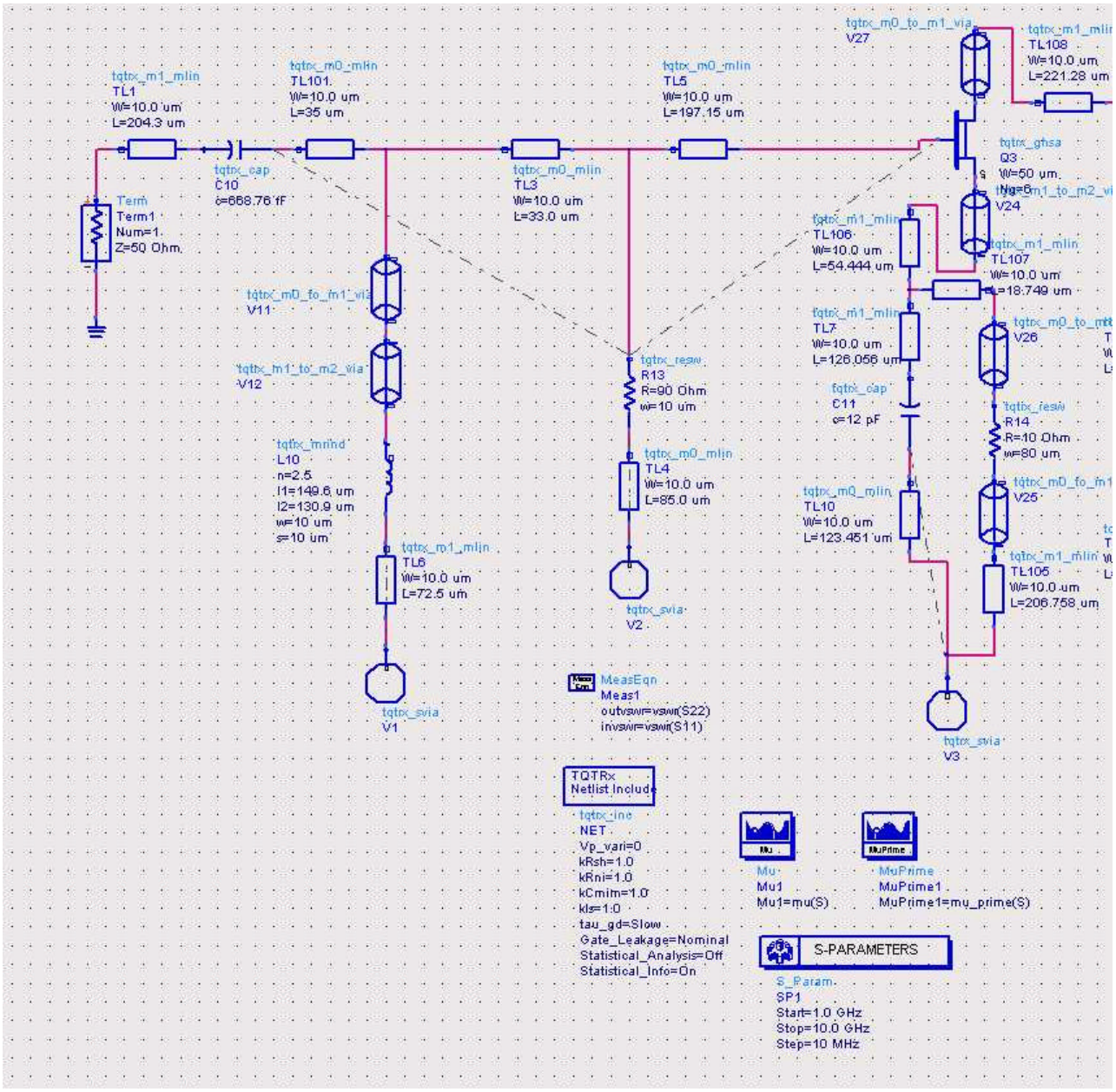


Diagram 5.

Schematic – Part 2.

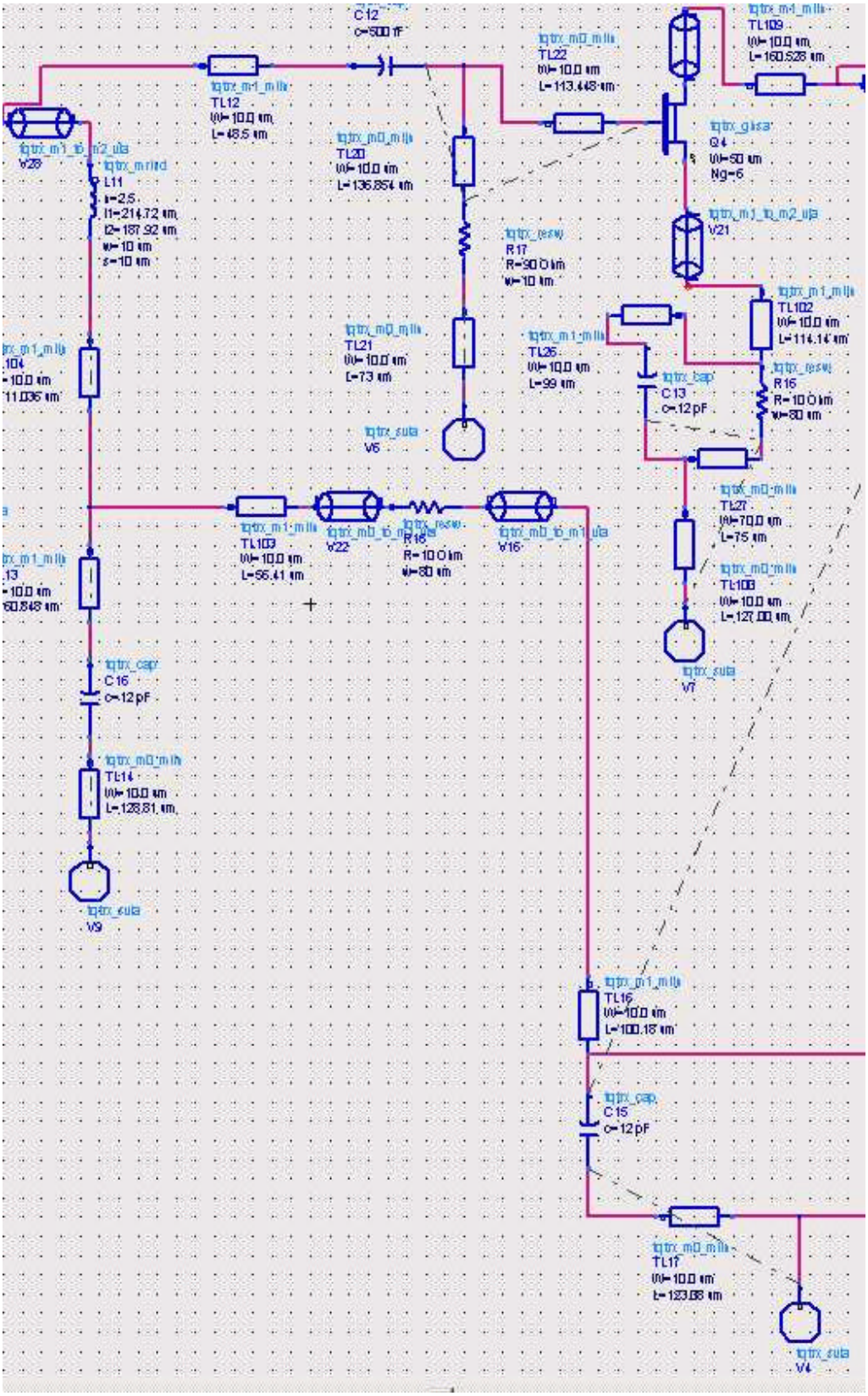


Diagram 6.

Schematic – Part 3

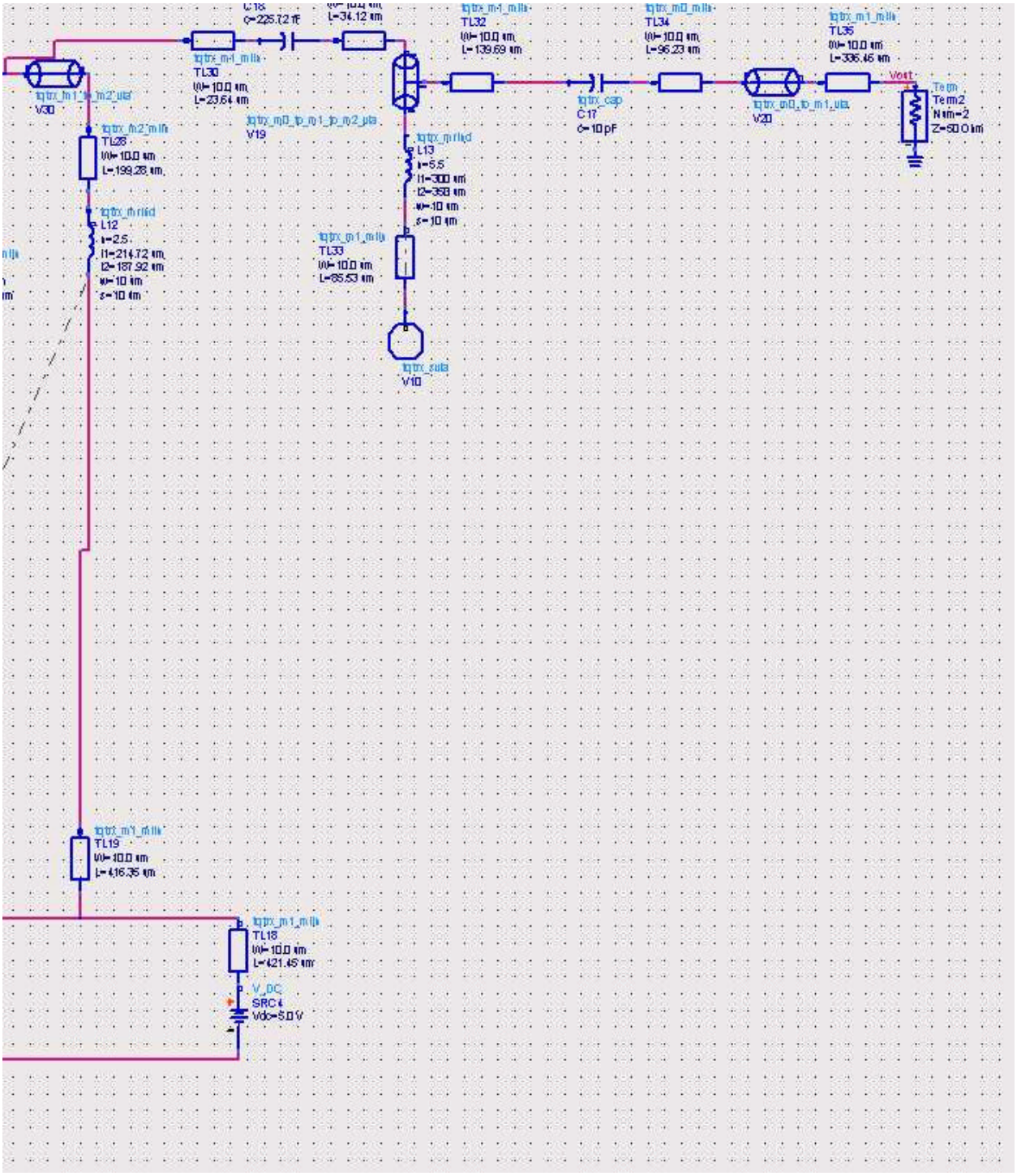


Diagram 7.

Simulated Performance

Please see the following plots and tables for our simulated performance.

C Band Driver Amplifier Performance vs. Requirements

	Requirements	Achieved
Frequency	5725 to 5875 MHz	yes
Bandwidth	> 150 MHz	yes
Gain	> 15 dB	17.35 dB
Gain Ripple	±0.5 dB max	+/- 1.75dB
Output Power	> +13 dBm at 1 dB compression	13.8 dBm
VSWR	<1.5:1 input and output	Approx. 1.5:1
Supply Voltage	+5 Volts	+5 V

Table 3.

Pout vs. Pin

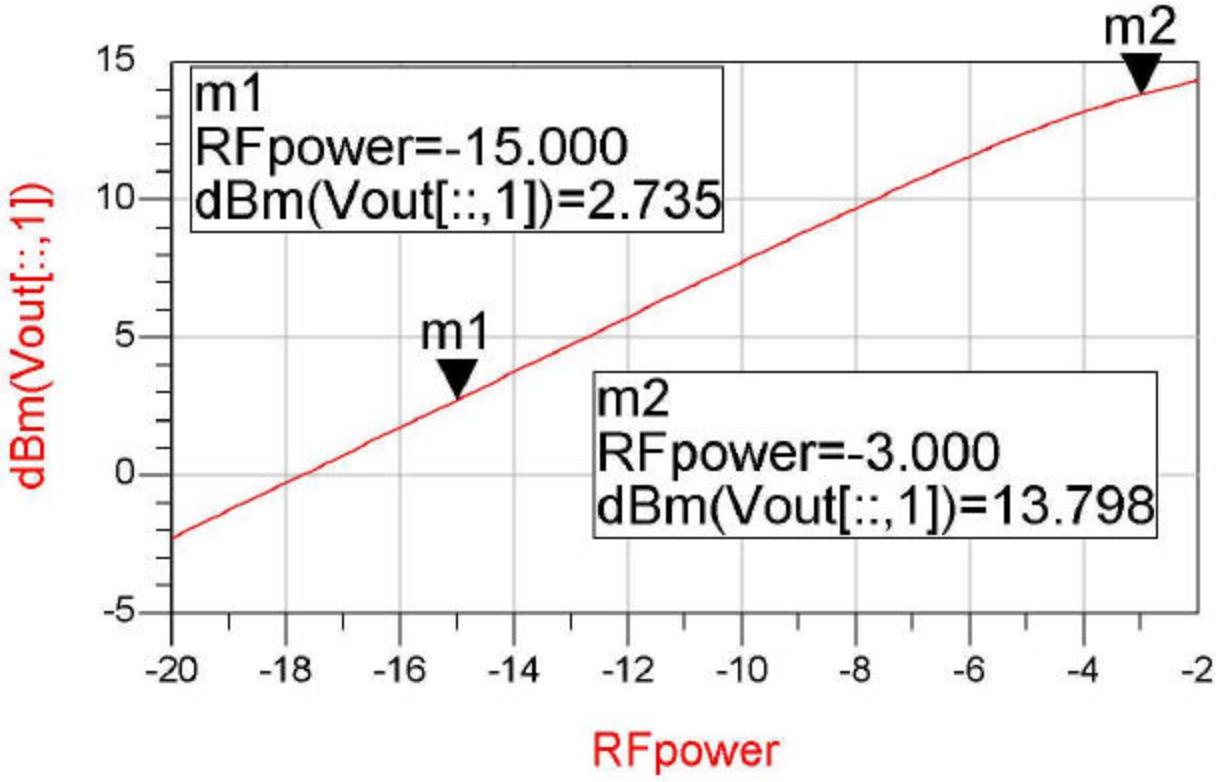


Diagram 8.

Marker m2 is P1dB. Gain is 17.735. Output power at P1dB = 13.8 dBm.

S Parameters (S21)

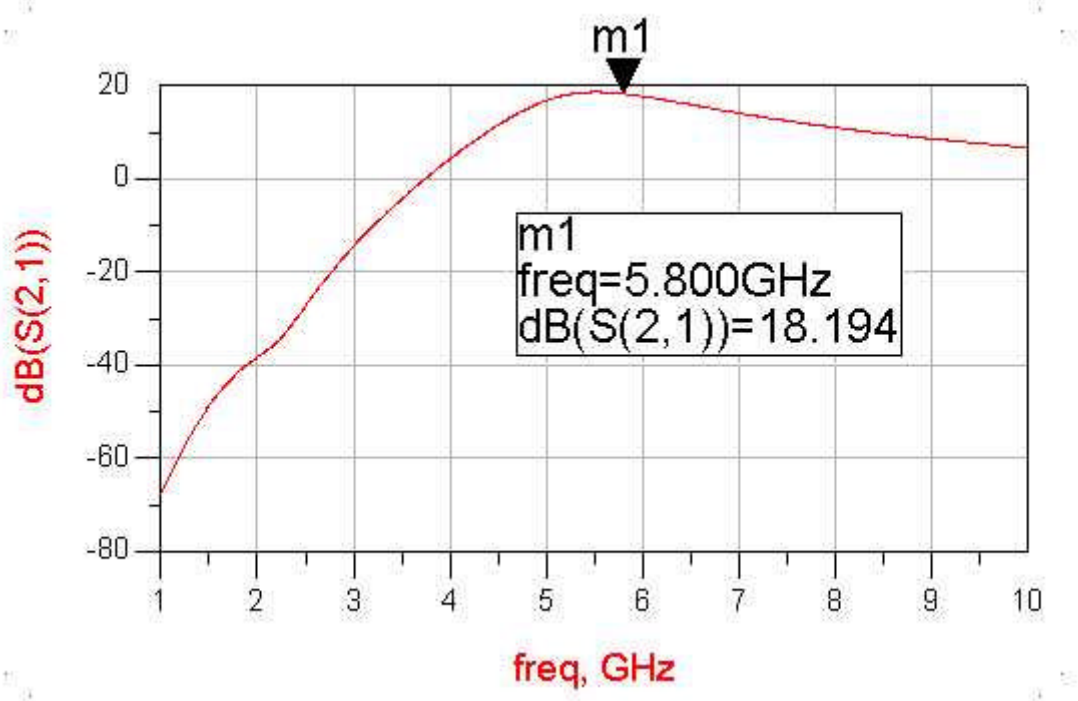


Diagram 9.

S Parameters (S21) – Gain Ripple

Diagram 10.

Stability

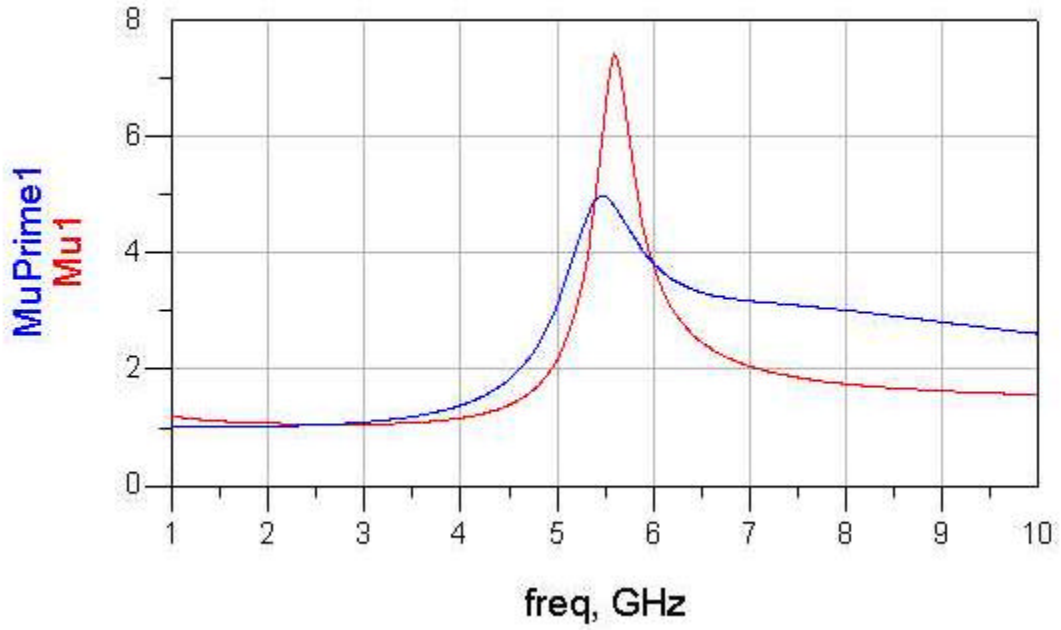


Diagram 11.

Input and Output VSWR

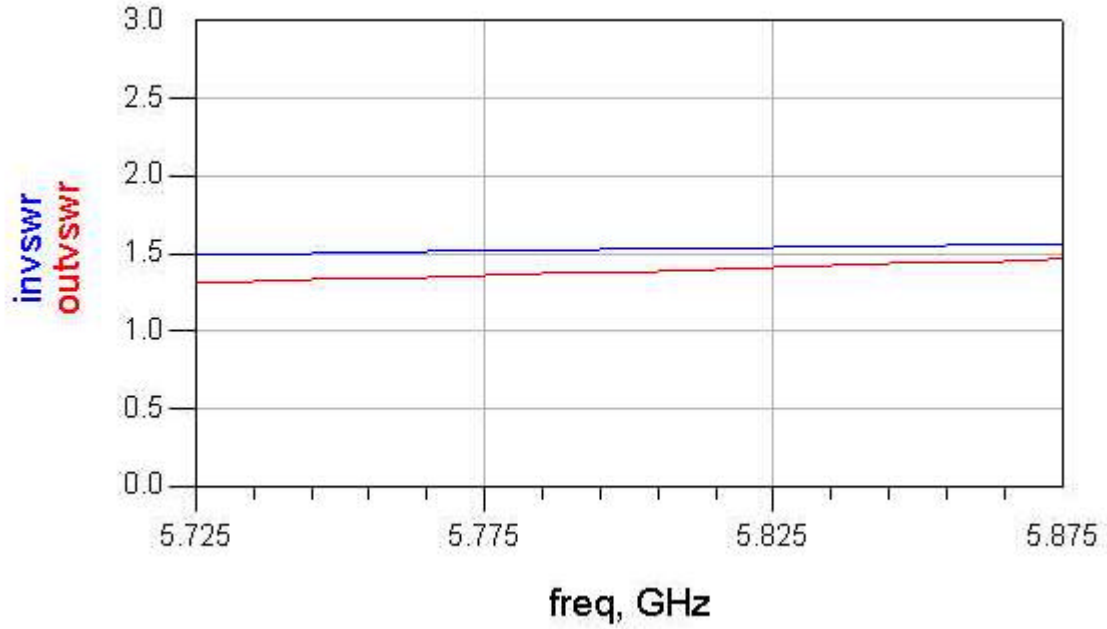


Diagram 12.

Test Procedure

Spectrum Analyser [with signal generator] :

Since this circuit is self biased there is no specific DC power up sequence. Therefore the test procedure is dramatically simpler.

1. Connect input to signal generator using special MMIC probe and workstation.
2. Connect output to Spectrum Analyser thru an attenuator.
3. Connect power supply to bias pad.
4. Bring up power supply slowly to 5V while monitoring current for possible shorts.
5. Set input signal to 5.8GHz and at an input power 10 dB below predicted P1dB point. Measure linear gain. Increase input power until P1dB is reached, measure P1dB output power.
6. Set input signal to sweep across specificed band in Table1. Capture Pout versus Frequency.

Network Analyser :

1. Connect input to network analyzer using special MMIC probe and workstation.
2. Connect output to Network Analyser thru an attenuator.
3. Apply 5V to bias pad.
4. Take data on S Parameters.

After tests have been performed compared with simulated performance.

Conclusion & Recommendations

In this design we uncovered many schematic, layout, and design requirement challenges. We believe we were able to overcome all of these challenges thru the help and support of peers and professors. All requirements were met [although input VSWR was marginal] and several design catastrophes were avoided. Several design tricks were employed to improve layout and reduce the number of components required. While connectivity in the layout tool was absurdly difficult, in the end we were able to achieve a layout and a design that we were happy with.

As far as recommended design improvements, the current design has no real ability to handle process variations. An active bias scheme could be employed to aid in that regard. Also there is likely some room to marginally improve input VSWR, however we feel the gains would not be worth the effort.

A 5.8 GHz MMIC Quadrature Modulator in GaAs

Prepared by:

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Microwave Monolithic Integrated Circuit (MMIC) Course
Johns Hopkins University
Fall 2003

Abstract

This paper documents the design of a Quadrature Modulator in the 5.8GHz Industrial-Scientific-Medical (ISM) Band, using the TriQuint TQS TRx process. The design was completed to fulfill the requirements of the Microwave Monolithic Integrated Circuit (MMIC) Course at The Johns Hopkins University. The modulator was designed using a TriQuint-provided library for Agilent's Advanced Design System (ADS), on a 60x60 mil GaAs substrate. It was designed to be used in a high data rate QPSK transmitter, when combined with other projects designed in the course.

Intro

This paper documents the design of a Quadrature Modulator in the 5.8GHz Industrial-Scientific-Medical (ISM) Band, using the TriQuint TQS TRx process. The design was completed to fulfill the requirements of the Microwave Monolithic Integrated Circuit (MMIC) Course at The Johns Hopkins University. The modulator was designed using a TriQuint-provided library for Agilent's Advanced Design System (ADS), on a 60x60 mil GaAs substrate. It was designed to be used in a high data rate QPSK transmitter, when combined with other projects designed in the course.

Circuit Description

The modulator circuit was designed as separate 90° and 180° switchable phase-shifters in series, allowing for a net switchable phase shift of 0°, 90°, 180°, or 270°. The phase-shifters were constructed with a pair of input switching FETs, a phase-delay or bypass path, and a pair of output switching FETs. The phase-shifters run on a bipolar supply of ±5Vdc. Incorporated on-chip are a pair of complementary-output TTL-to-bipolar drivers that allow control of the phase-shifters using standard TTL level logic signals; one driver is needed per phase-shifter. The drivers produce 0 and -3.5V control outputs to the phase-shifters, and operate on ±5Vdc.

Design Philosophy

The primary goal in designing the modulator is to ensure the proper phase change between the various states, 90° for QPSK. QPSK also relies on a I/Q constellation where each symbol has equal amplitude, thus amplitude matching between the 4 phase states was the secondary design goal. Other important design criteria included allowing TTL control levels, and a sufficient IP3 so as not to compress and introduce higher-order products when driven directly by a 0dBm VCO, since the transmitter system as envisioned has no output bandpass filter.

The first step was designing the two phase-shifters. The 90° shifter uses a single lumped-element $\lambda/4$ transmission line at the center frequency, while the 180° shifter uses two $\lambda/4$ lines in cascade; this approach simplified design and simulation since the two shifter were nearly identical. The 90° shifter, being the slightly less complex one, was designed first.

The switching was implemented using the FETs in a switched amplifier topology, with the input applied to the gate, and the output at the drain, using TriQuint 140μm DFETs to provide adequate IP3. This approach provides a very high impedance at the "off" FET, since R_{GS} is much greater than R_{DS} in the off state, which improves the isolation. This also provides gain, controllable by a drain bias resistor, compensating for any losses in the delay elements or the chip. Since the signal must pass through four switches, this technique was used, as a traditional drain-source switching system would be lossy itself,

and provide no means to compensate for other system losses. Switching control from the bipolar drivers was provided by a 1.5kΩ bias resistor at the gate.

The completed 90° shifter had two signal paths: FET-Line-FET, and FET-pad-FET. The line was implemented as a PI-network, with shunt capacitors at input and output, and a series inductor. The pad was used initially to provide amplitude matching between the delayed path and the non-delayed path. It was subsequently removed, and the amplitude match was accomplished by varying the drain bias resistors in both paths until there was less than 1dB of variation over the operating band.

The 180° shifter was designed from the 90° shifter by adding a second λ/4 line, and combining the common-node shunt capacitor into a single capacitor for simplicity. Drain resistances were varied to compensate for the additional loss in the longer transmission line, but otherwise the shifters are identical.

When cascaded, the two shifters provided nearly 15dB of small-signal gain, while presenting a poor input VSWR. Since this gain was not necessary according to the original design guidelines, 5dB was sacrificed as input attenuation to provide better than a 2:1 VSWR over the entire operating bandwidth. No complicated matching was necessary. Overall, the system has a nominal gain of 10dB, with an amplitude variation of ±0.5dB between phase states over the operating band.

The TTL-to-bipolar drivers were designed from a reference schematic provided by the course instructor, using 12μm and 18μm DFETs.

Trade-offs

The most significant trade-off was in using the switched-amplifier technique instead of a classic switch. While the classic switch would have consumed less current, initial simulations proved to be too lossy to meet the design requirements. It also would have relied on purely passive amplitude matching, adding to the total loss. A hybrid amplifying/passive switch approach was considered, but it eliminated the symmetry, and made the design more complicated.

Modeled Performance

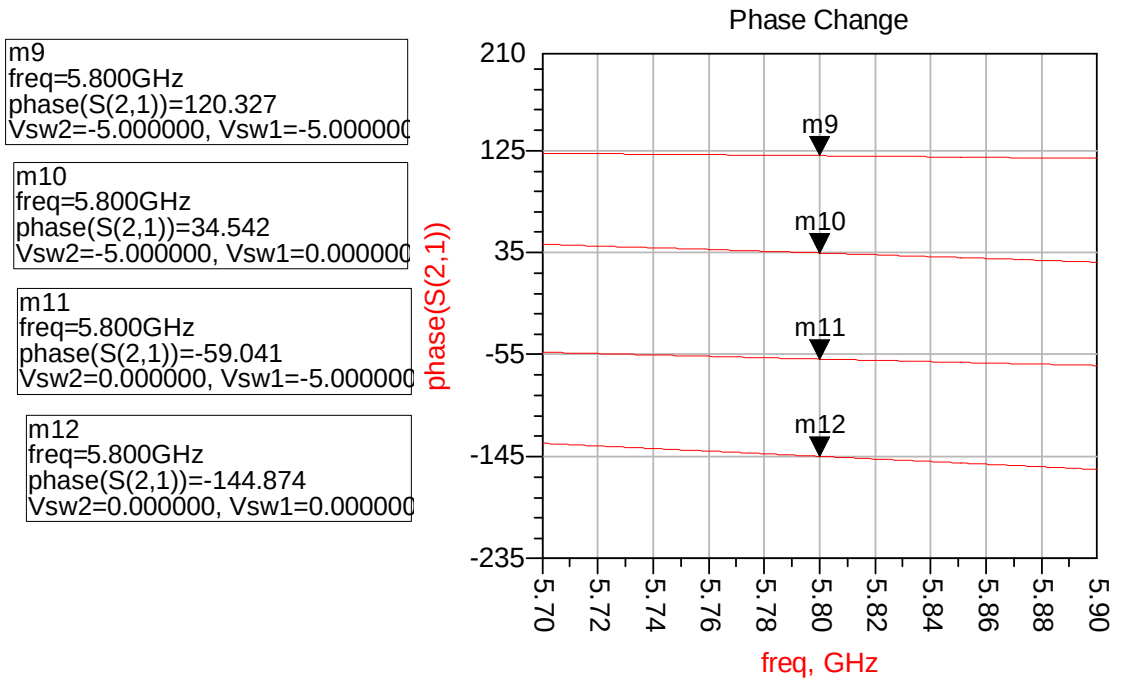
Specifications

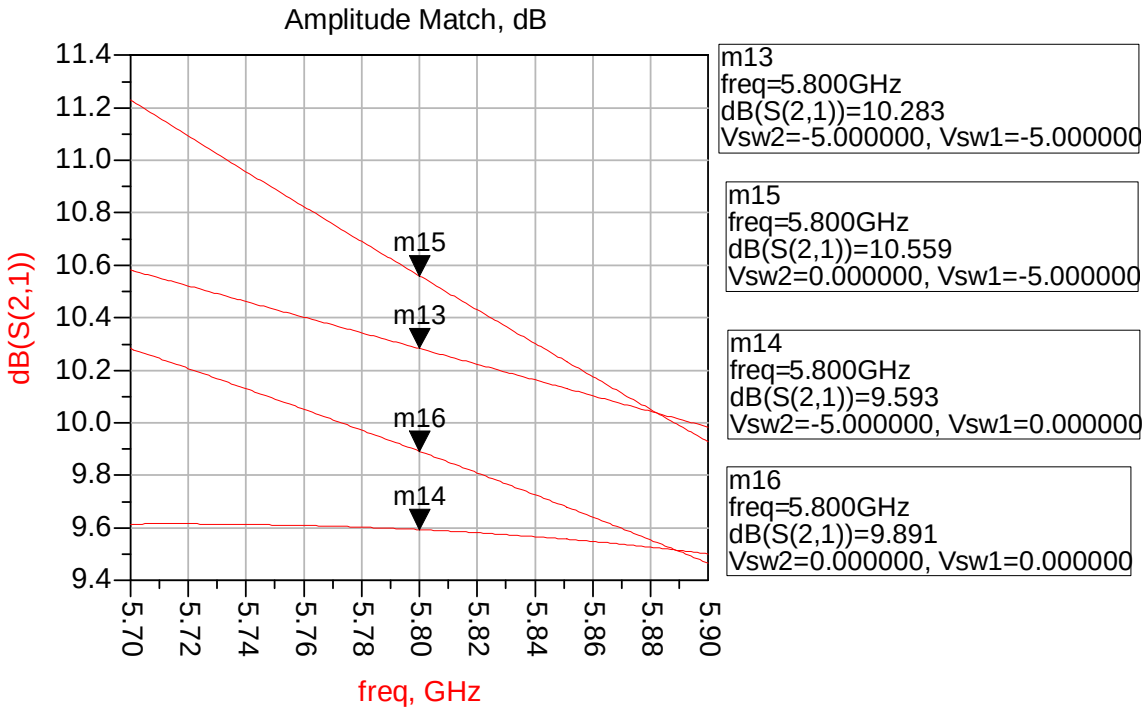
The following table contains the performance specifications for the modulator:

Frequency	5.8 GHz ± 100 MHz
Vsupply	± 5Vdc
Control	+5V TTL
Amplitude Balance	± 1dB
Phase Shift	90° ±5°
Instantaneous Bandwidth	0 to 20 MHz

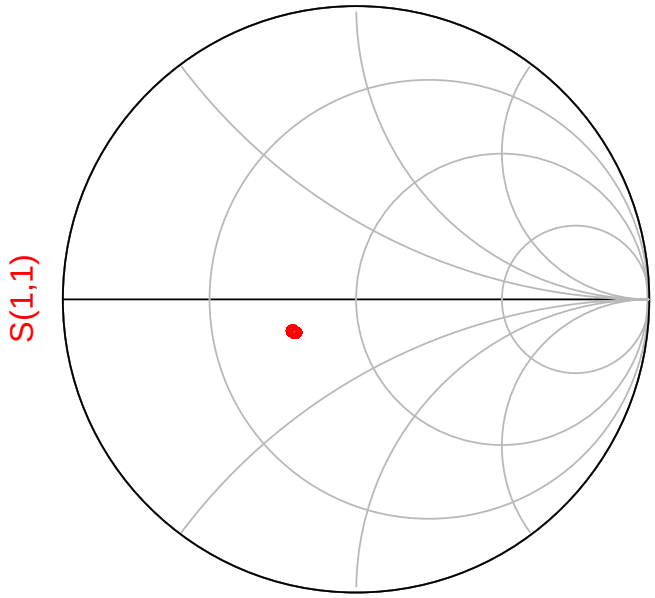
Predicted Performance

Below are plots of the simulated performance. All parameters were met.



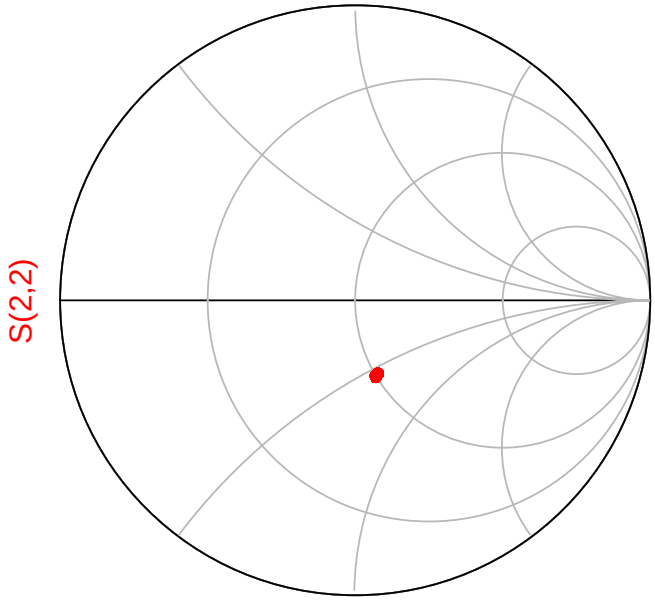


Input Reflection Coefficient



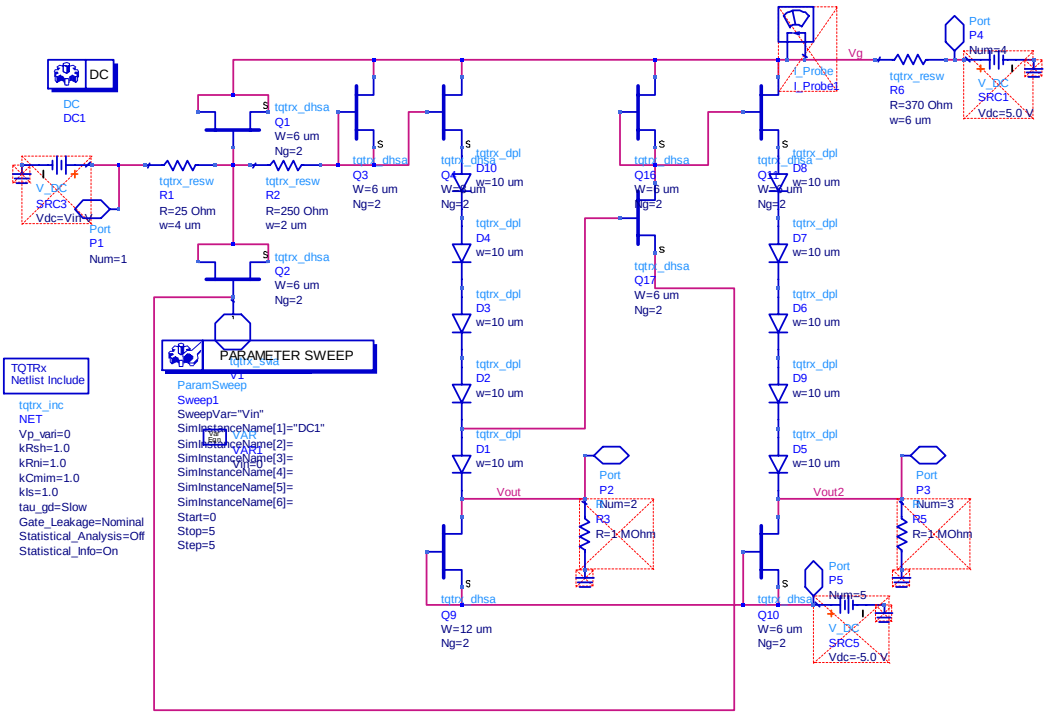
freq (5.700GHz to 5.900GHz)

Output Reflection Coefficient

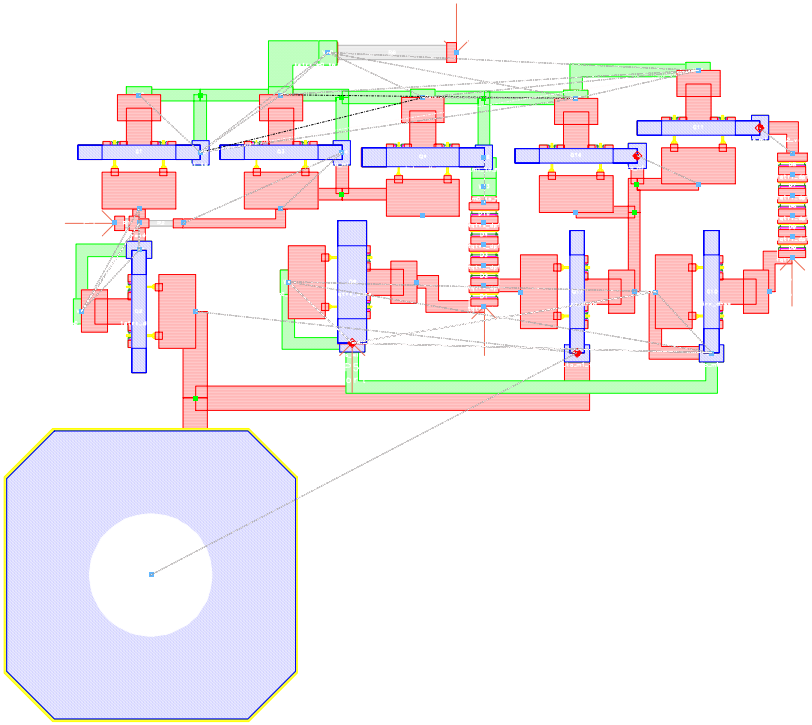


freq (5.700GHz to 5.900GHz)

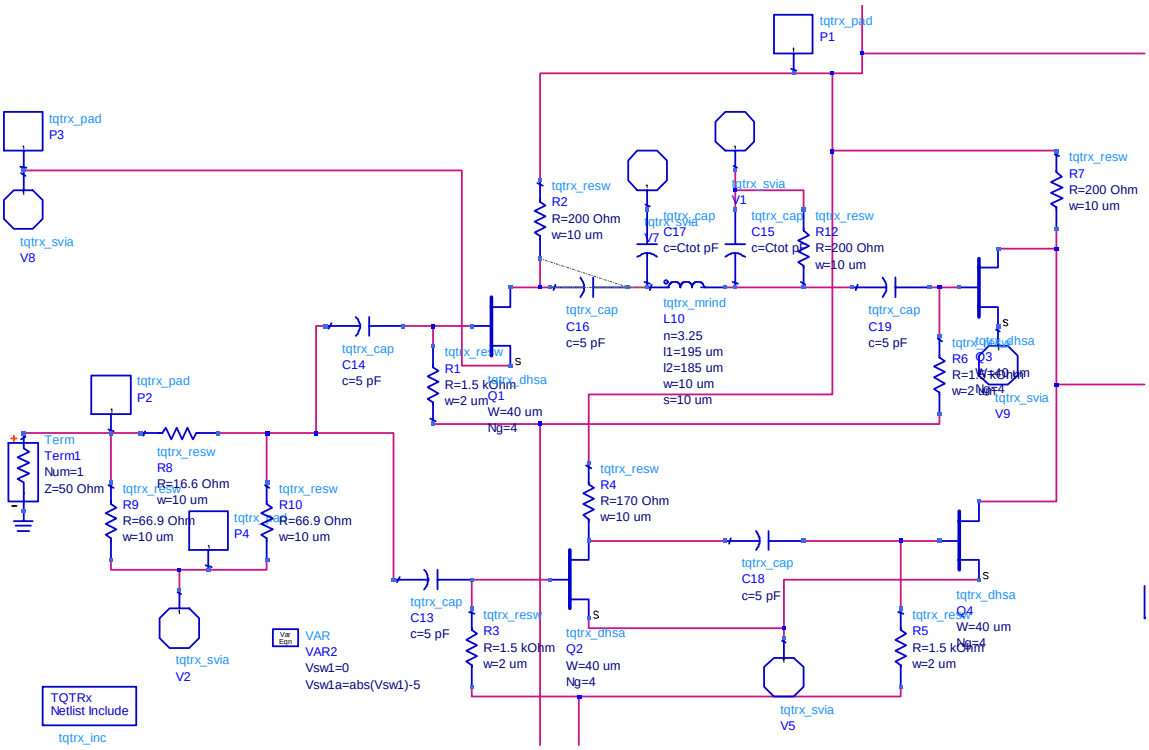
Schematics



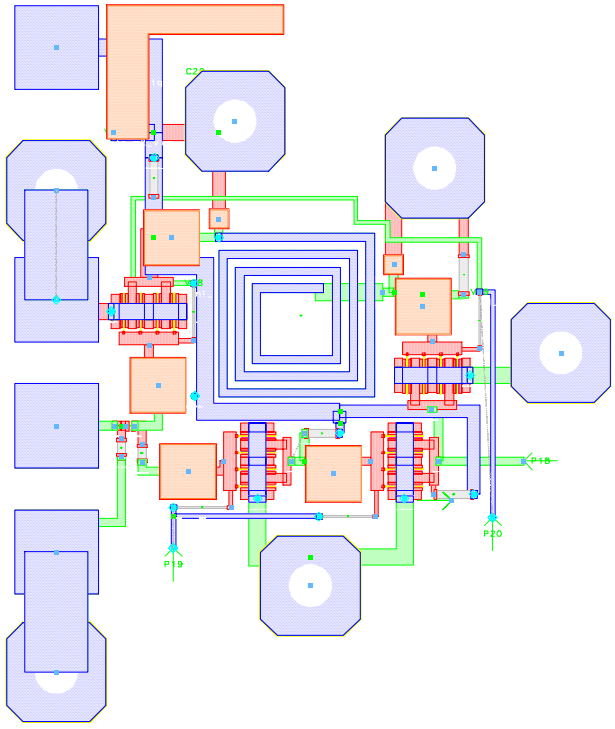
Driver Schematic



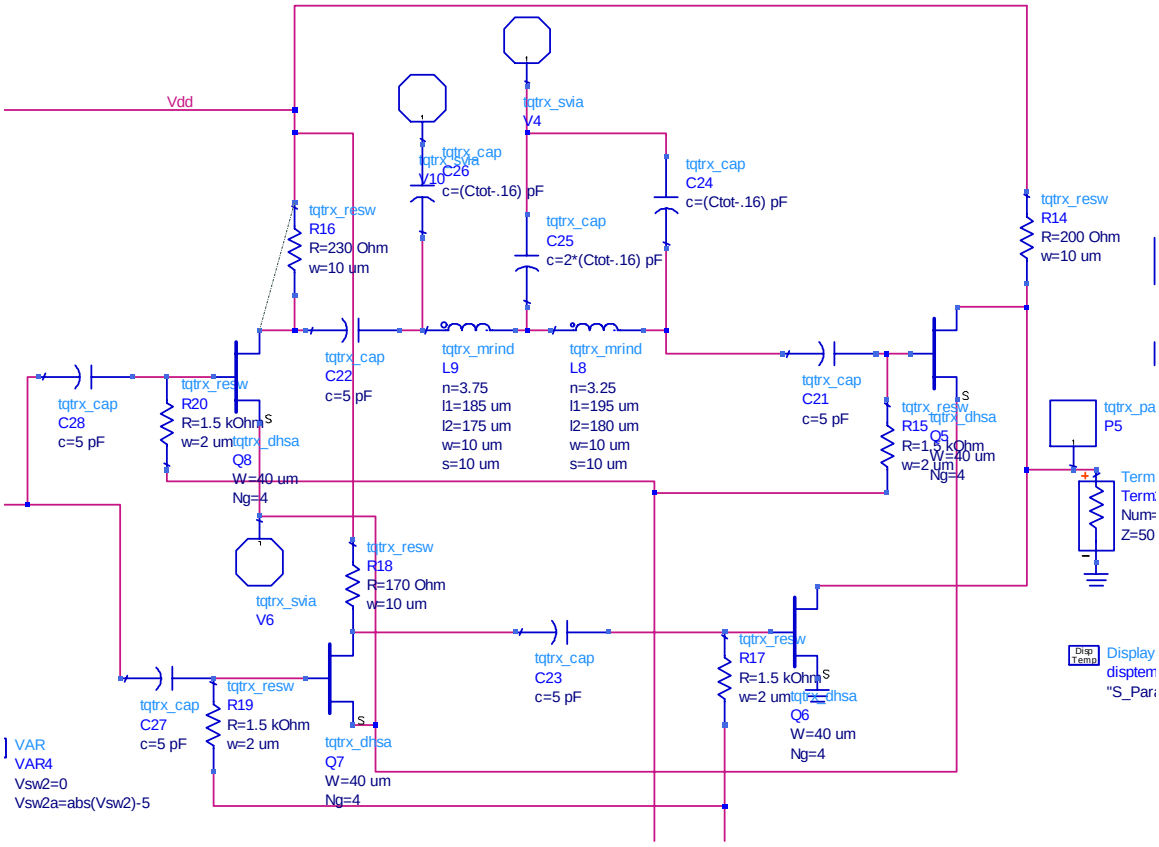
Driver Layout



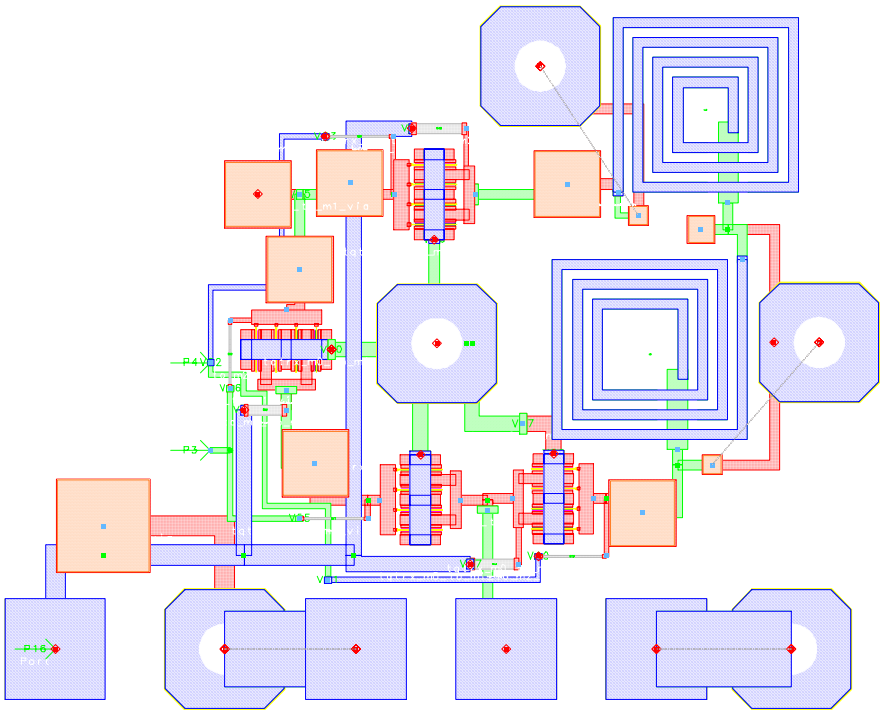
Quarter-Wave Shifter Schematic



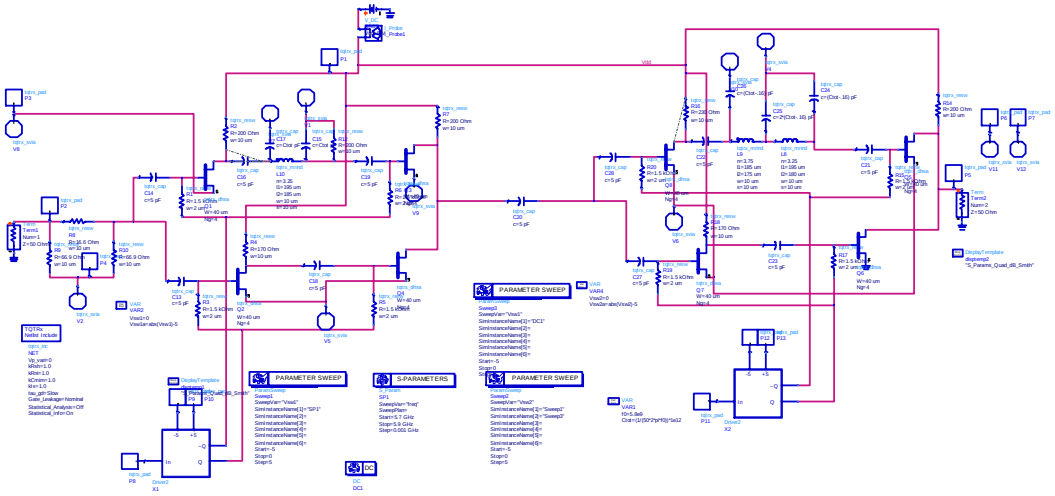
Quarter-Wave Shifter Layout



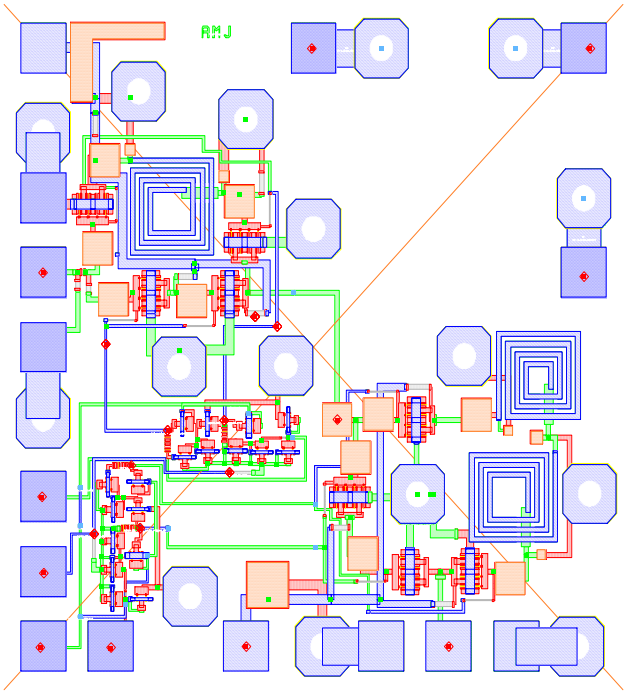
Half-Wave Shifter



Half-Wave Shifter



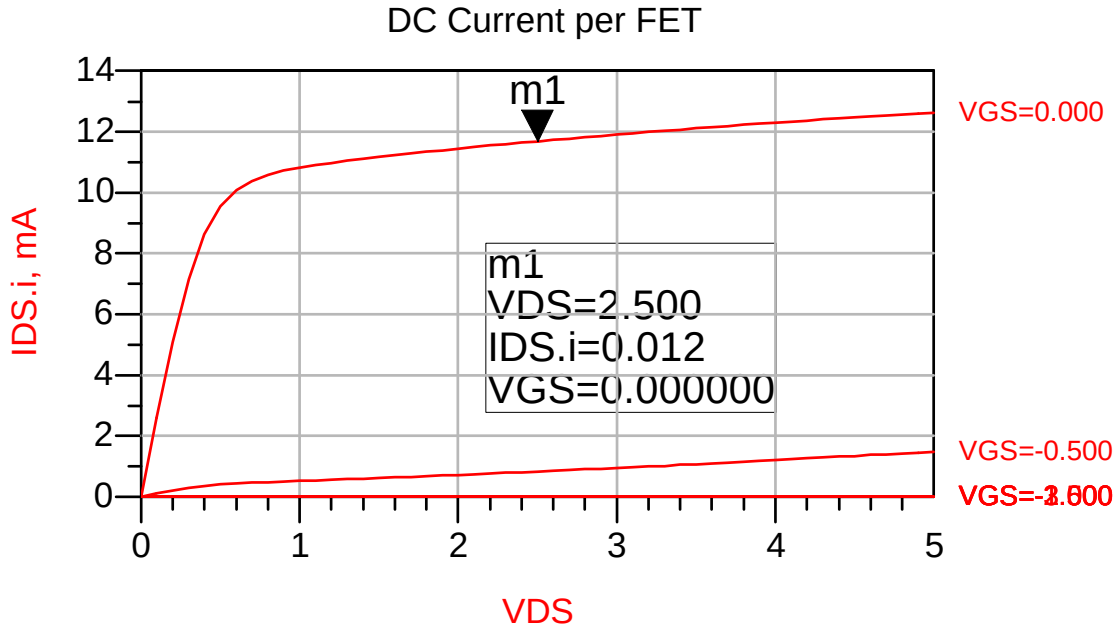
Complete Schematic



Complete MMIC

DC Analysis

Total current consumption is approximately 57mA, which is not unacceptable. While a design without gain would have had a lower current, this still meets the design goals.



Current Consumption (mA)

freq	I_Probe1.i
Vsw2=-5.000, Vsw1=-5.000 0.0000 Hz	57.61mA
Vsw2=-5.000, Vsw1=0.000 0.0000 Hz	57.46mA
Vsw2=0.000, Vsw1=-5.000 0.0000 Hz	57.31mA
Vsw2=0.000, Vsw1=0.000	

Test Plan

The following equipment is required for test:

- ±5 Vdc supply
- Spectrum Analyzer
- RF Signal Generator
- Function Generator (x2, phase locked), for control signals
- Vector Signal Analyzer **or** Quadrature Demodulator
- Oscilloscope

Proper power sequencing must always be followed; ensure grounds are connected, then connect the -5 Vdc and then +5 Vdc. Next, connect the function generators to the control inputs, with a square wave output at the modulation frequency, and levels of 0-5V. Use the oscilloscope to adjust the relative phase of the generators to approximately 90°, this will create modulation that will rotate the output constellation.

Connect the RF signal generator to the input at the desired frequency, with a power level of 0dBm. Connect the vector signal analyzer to the output, and configure it for a QPSK modulation. The constellation should now be visible. Alternatively, connect the quadrature demodulator to the output of the MMIC, and connect the I and Q signal to the oscilloscope, set in X-Y mode. After adjusting the holdoff on the trigger, the QPSK constellation should be visible.

Measure the relative phase and amplitude of the four constellation points to ensure they are within 1dB relative amplitude, and 90° phase rotation. Next, connect the spectrum analyzer to the output, and measure the output power; compute the gain. Last, open the spectrum analyzer's span to check for high-order mixing products.

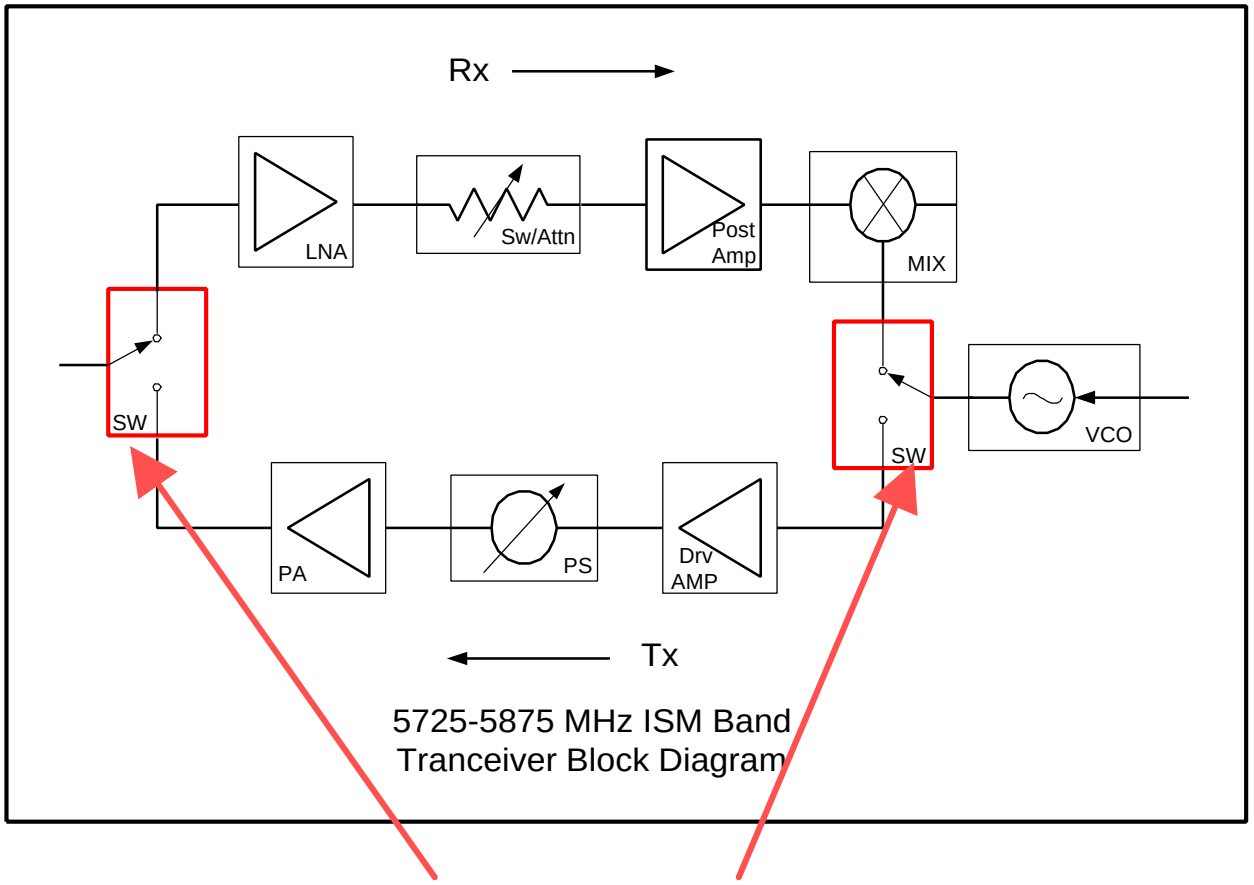
Conclusions and Recommendations

The modulator design and layout appear successful. The next step would be to create an actual I/Q mixer to allow higher-order modulations, such as 16QAM, or 8OFDM to be used.

Final Design Review
C-Band SPDT Switch
12/8/03

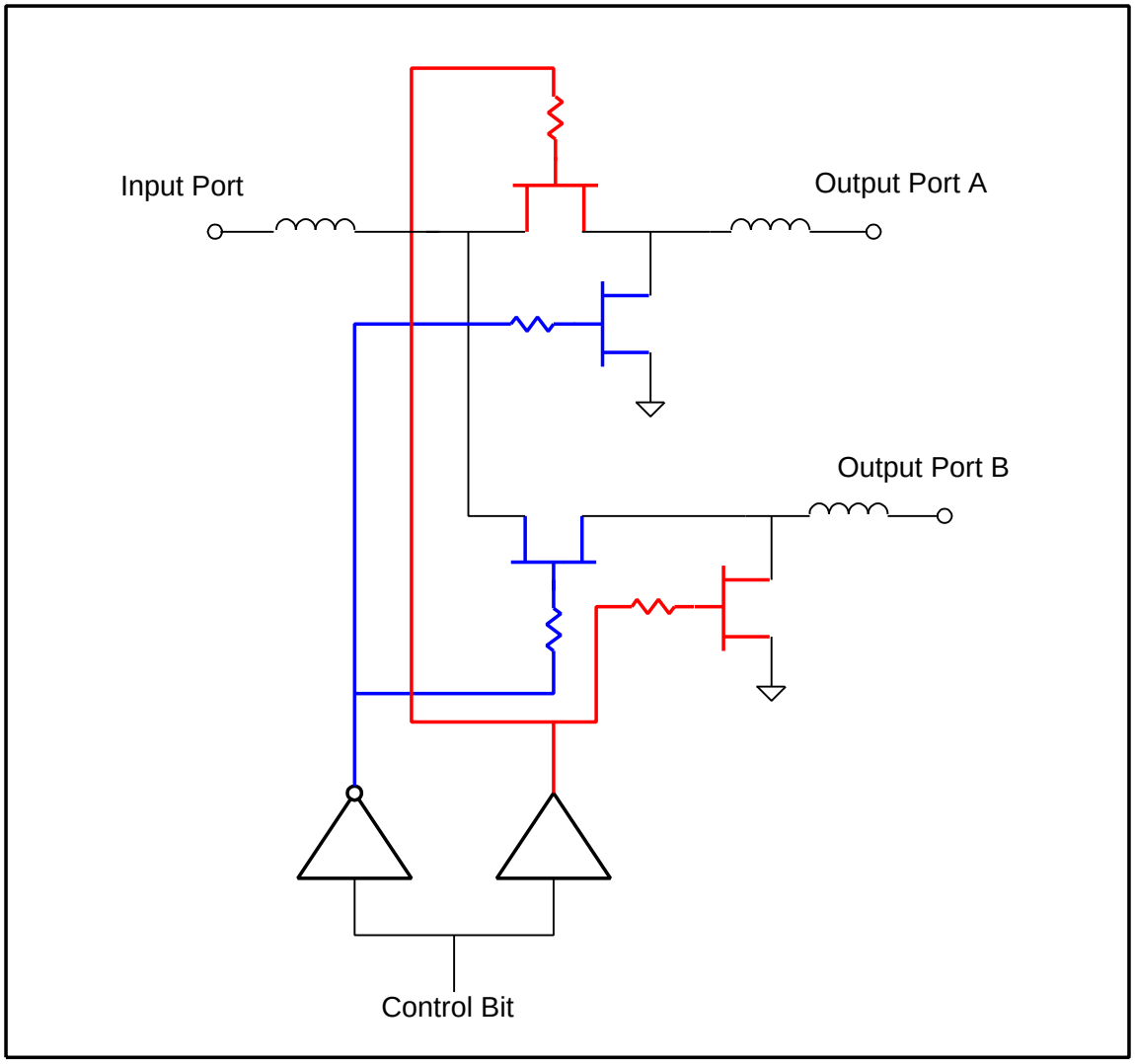
Ben Baker
John Long

System Block Diagram

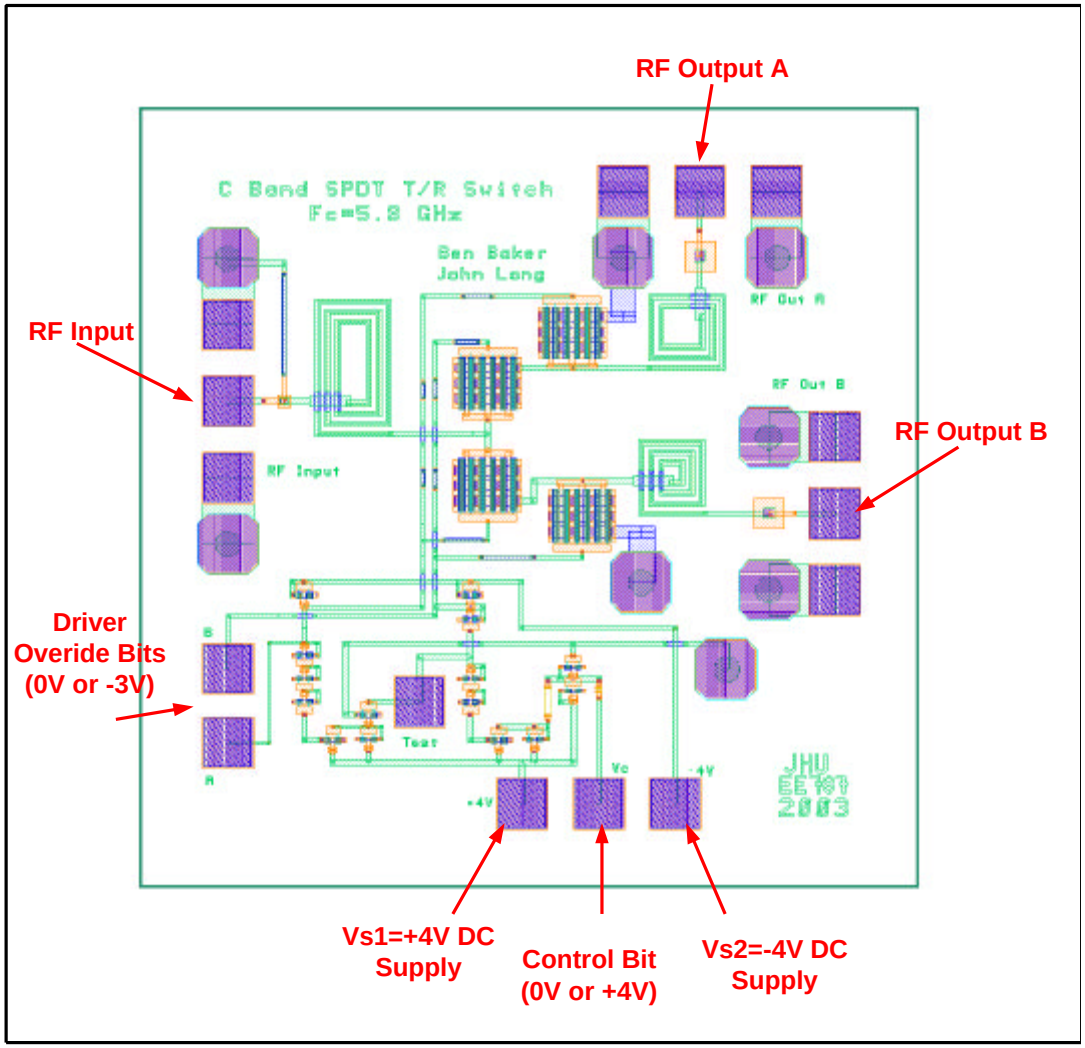


SPDT Switch

Simple Circuit Diagram

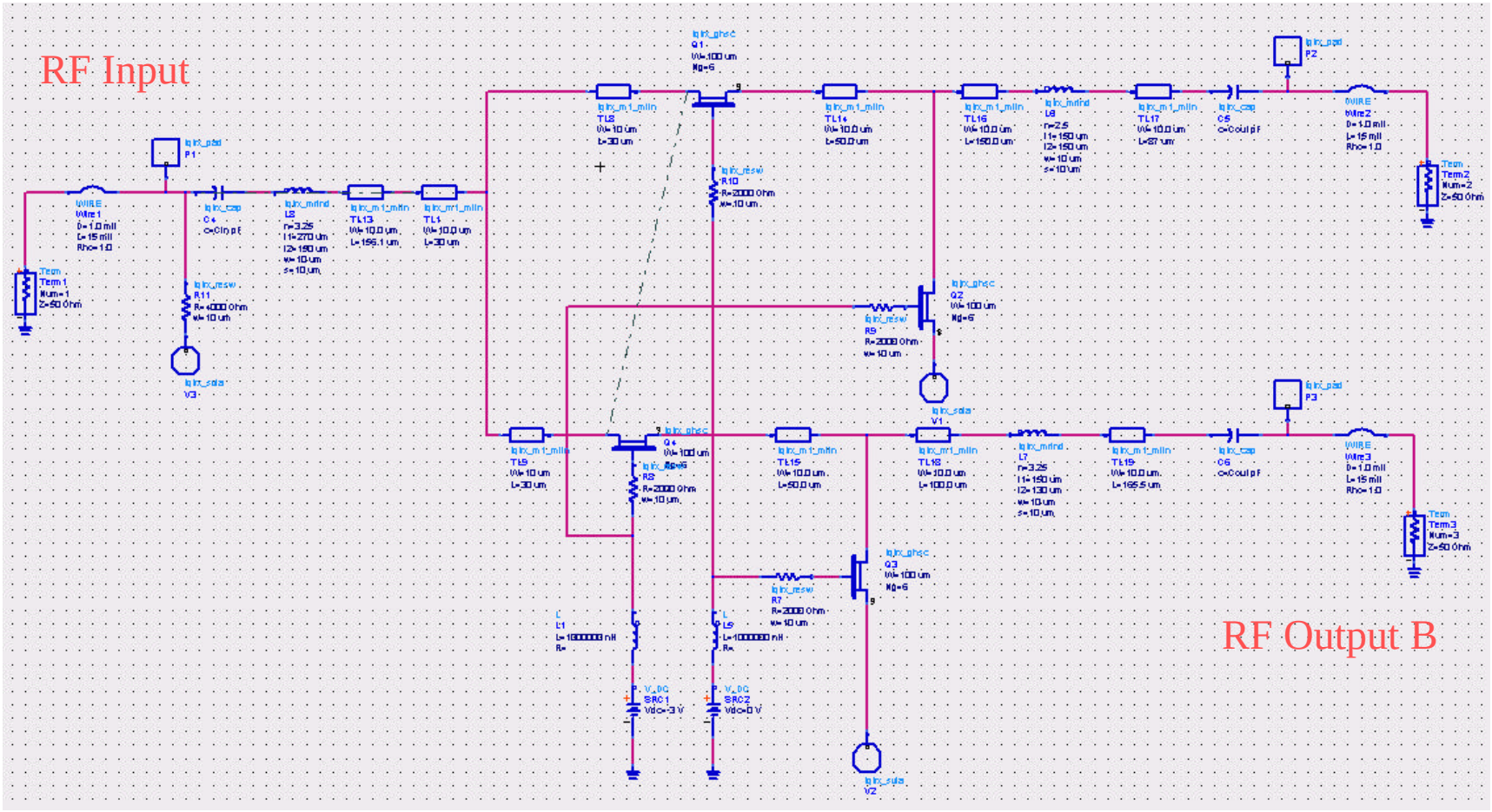


SPDT Layout & I/O

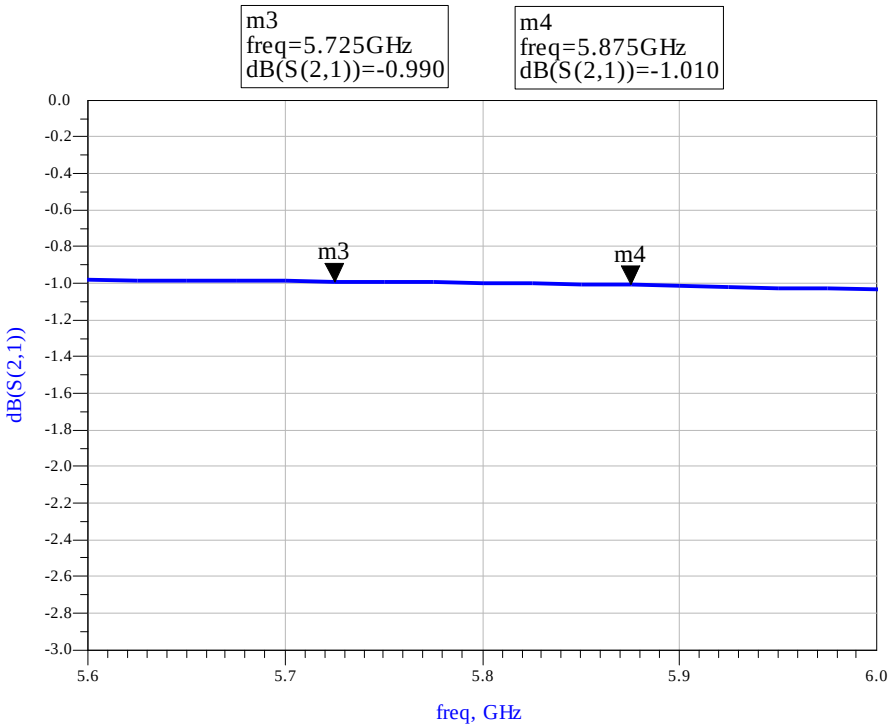


Control Bit Voltage	Vc1 [V]	Vc2 [V]	Low Loss Path
+4V	0V	-3V	S(21)
0 V	-3V	0V	S(31)

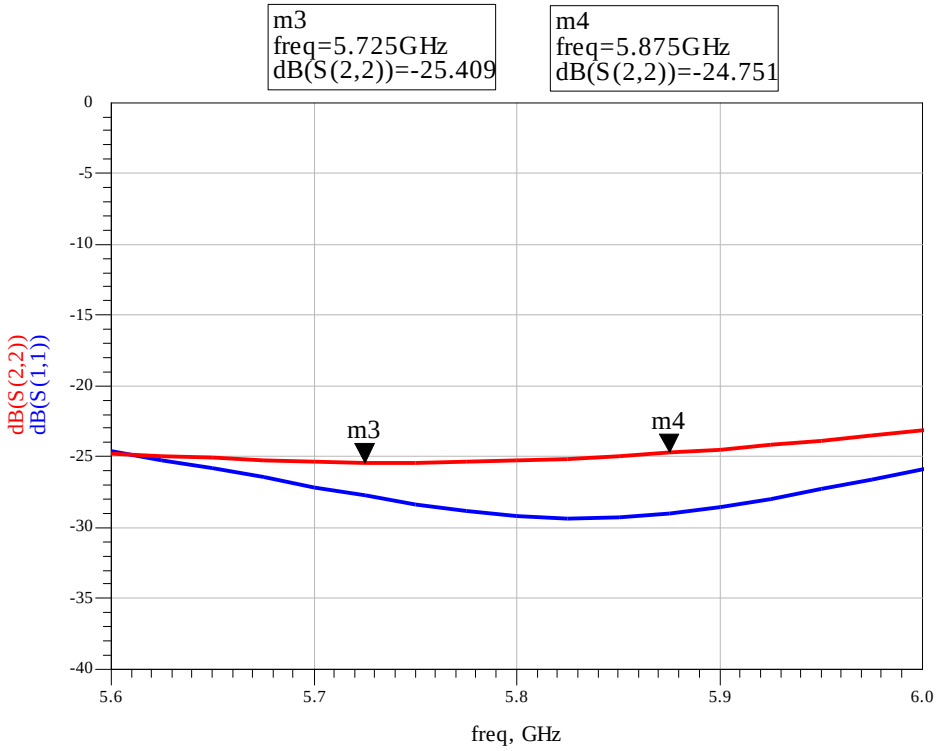
ADS SPDT Schematic



Simulated Performance

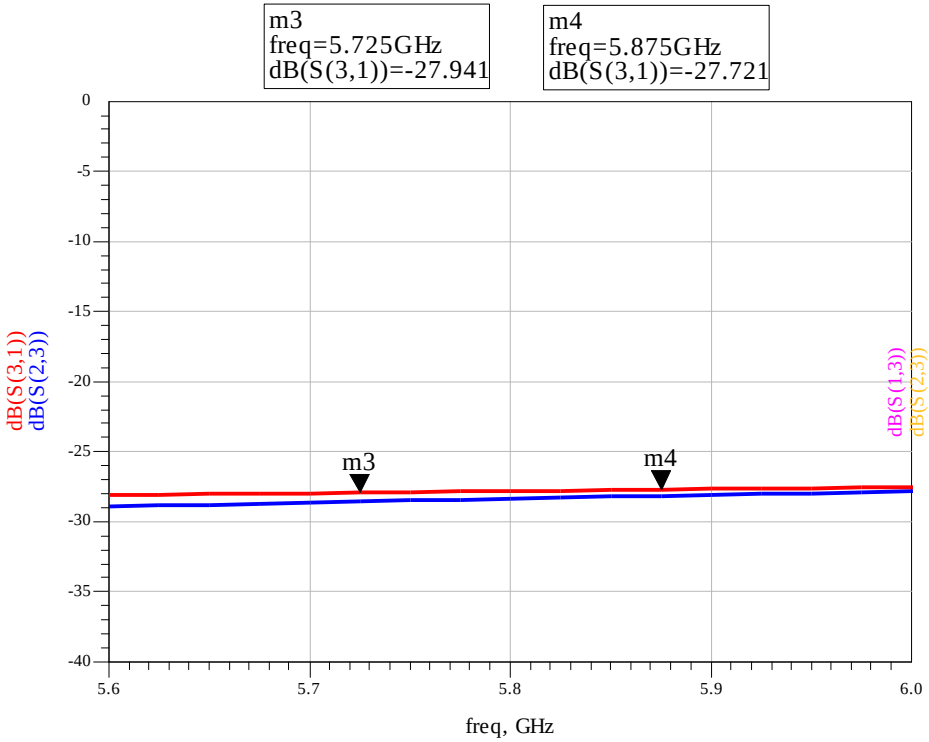


Insertion Loss

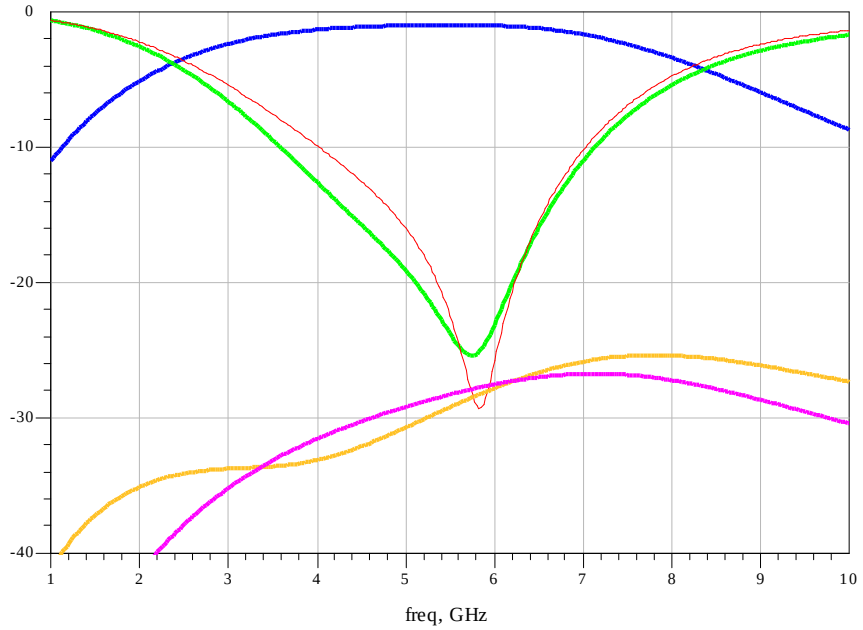


Return Loss

Simulated Performance



Isolation

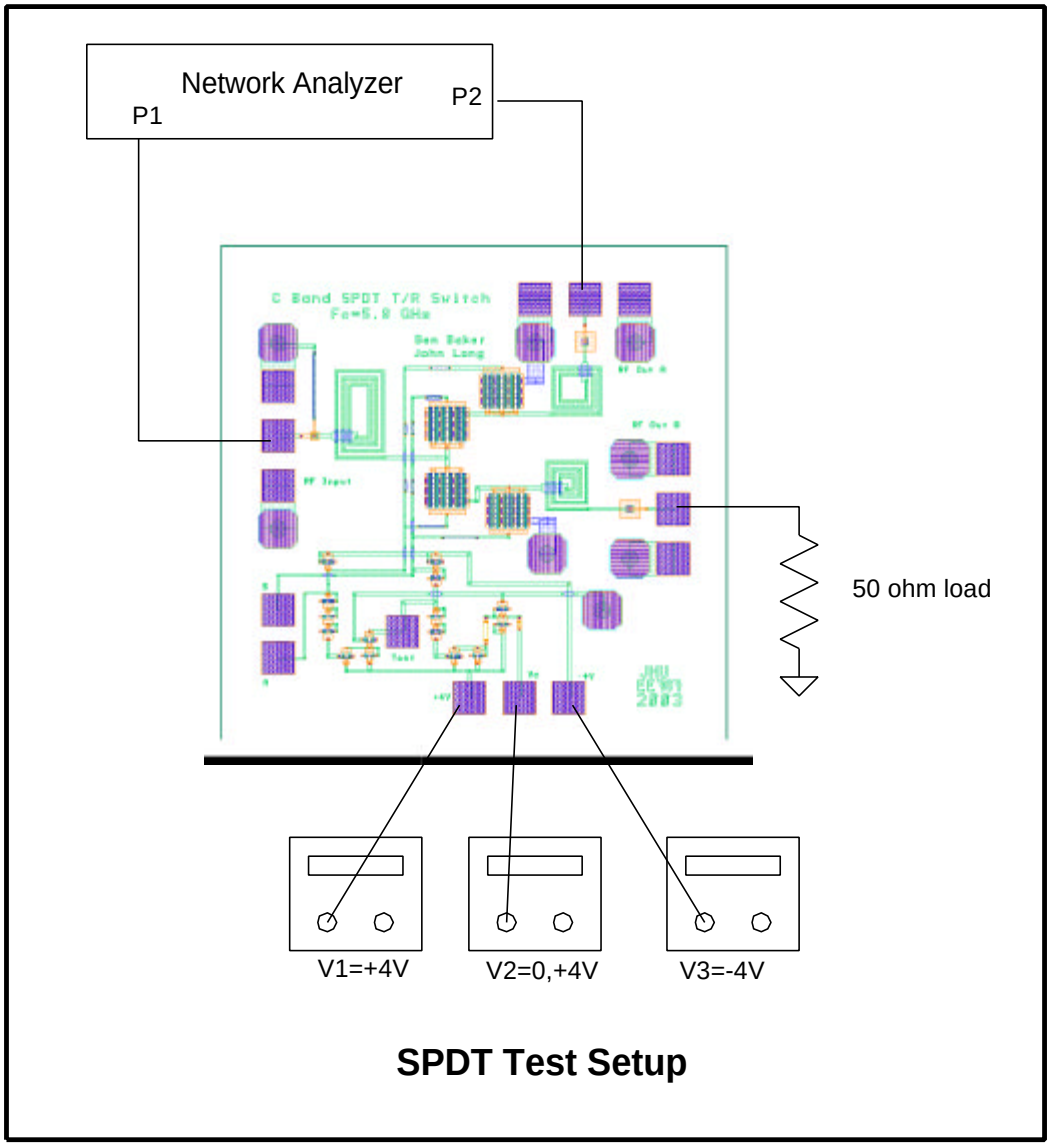


All Sparameters

Specification Compliance Matrix

	Specification	**Predicted Performance**
Frequency	5725 to 5875 MHz	4.7-6.8 GHz
Bandwidth	>150MHz	2 GHz
Insertion Loss	<2dB (1.5dB goal)	1dB
Isolation	>20dB	>25dB
Power Handling	>+24dBm @<2dB	+24dBm@ in low loss state
VSWR	<1.5:1 input and output (-14dB RL)	<-25dB
Supply Voltage	+/- 5V	0 &+4V
Control	TTL	TTL and manual control
Size	60x60 mil	60x60 mil

SPDT Test Setup



-Small Signal S-parameters
-Pin vs Pout

The Second Swing at Controlled Instability

An
L – Band VCO

Center Frequency = 1120 MHz
Bandwidth = 100 MHz

A Student Project Designed By
Mark F. Petty

For
The Johns Hopkins University – Applied Physics Laboratory
Class # 525.801 – Special Project I:
Monolithic Microwave Integrated Circuit Design

Fall 2003

ABSTRACT:

This paper describes the re-design of an L-Band voltage controlled oscillator, VCO. The original VCO design[1] was a student's final project in the Johns Hopkins University Monolithic Microwave Integrated Circuit, MMIC, class numbered 525.787. This VCO semester project will identify and correct the problems of the first design. The VCO was design with the Agilent's Advanced Design System, ADS, version 2003A. The VCO's target of fabrication is TriQuint Semiconductor's Texas 0.6 Gallium Arsenide facility. The VCO performance parameters include: center frequency of 1170 MHz; a tuning range of +/- 50 MHz; minimum output power of +10 dBm, desired output power of +13 dBm; supply voltage of +/- 5 volts, desired supply voltage of + 5 volts only, tuning voltage 0 – 5 volts; output impedance 50 ohms, nominal; and sized to fit on the 60 x 60 mil TriQuint ANACHIP.

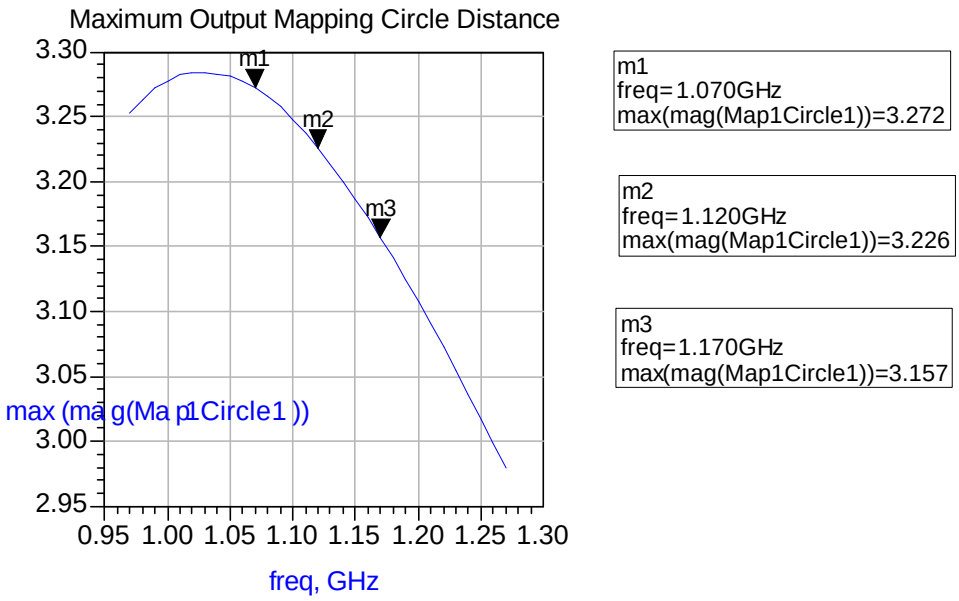
DESIGN INTRODUCTION:

The original VCO's design is a parallel resonator connected to a common source amplifier. Therefore, this re-design effort will continue to use a common source amplifier. A parallel resonator at the gate input determines the frequency of oscillation. A second parallel resonator serves as a high impedance current supply to the amplifier FET's drain. An output matching network coverts the high impedance FET output to a nominal 50 ohms. The frequency determining parallel resonator is comprised of two diode connected GFET devices as the voltage controlled variable capacitor and a MRIND inductor, a physical size defined inductor element. A single common source GFET amplifier provides the circuit's gain. The common source MESFET VCO design is uncommon. The bipolar device equivalent design, the common-emitter VCO is also uncommon. The common emitter (source) VCO has fabrication issues stemming from large capacitor and inductor values and performance issues due to the Miller effect because neither the base nor the collector is grounded, Rogers and Plett[2]. However, the design was shown functional at the MIC level, discrete devices mounted on a printed circuit board, by Edwards[3].

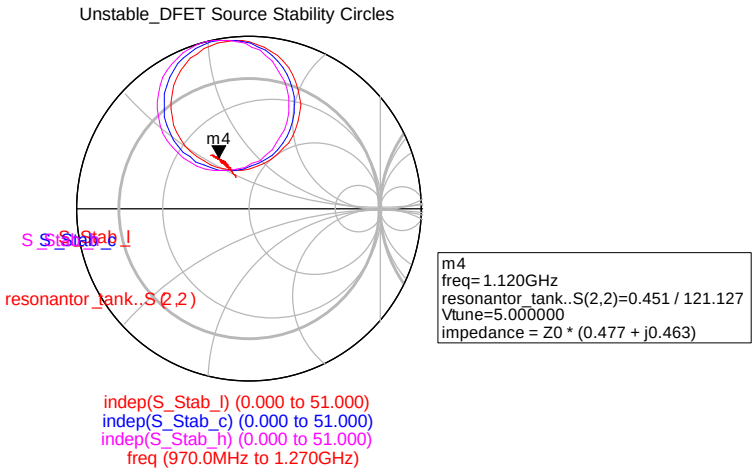
The design methodology starts by adding source resistance to an active device, in this case a MESFET, to create instability. The amount of instability is measured by the parameter maxMP2, the maximum value of the output mapping circle, Edwards[3]. Tune the source resistance until maxMP2 equals approximately 3 at the desired frequency. The parameters maxMP1 and maxMP2 equal the algebraic inverse of the corresponding μ stability parameters. The μ and μ' stability parameters are quantitative figures of merit for the stability of an amplifier, Edwards[4]. Thus, it stands to reason that their algebraic inverses maxMPx are figures of merit for the instability of an amplifier. Now connect a resonator circuit to the input of this appropriately unstable amplifier.

Determine maxMPx from simulations executed on a biased FET device. This includes the parallel resonator current supply and the external gate to source feed back capacitor, Cgs. Also, include a source resistor bypass capacitor of reasonably low impedance, from five to ten ohms.

Below is a graph of maxMP1, the maximum distance from the center of the smith chart to the edge of the output mapping circle. The markers indicate the upper, lower, and center points of the frequency range. Marker dialog boxes, right, indicate the exact value of the maxMP1 function.



Once an adequately unstable, and biased device, is configured, design the input resonator circuit for the frequency range of interest. To insure that there circuits match, plot the output reflection coefficient, S22, of the resonator circuit and the source stability circles of the unstable biased FET circuit on the same smith chart. Design the resonator such that S22 is positioned inside the source stability circles.



Next design an output matching circuit, and tweak achieve the desired frequency.

SIMULATION SUMMARY:

Specifications Compliance Matrix for Original L-Band Voltage Controlled Oscillator

	Specification	Pre-Layout	Post-Layout	Fab'ed IC
Frequency Range	1070 to 1170 MHz	1056 to 1171 MHz	1012 to 1156 MHz	1005 to 1155 MHz
Output Power	> +10 dBm > +13 dBm goal	~ +19 dBm	~ +19 dBm	~ +18.5 dBm
Control Voltage	0 to 5 Volts	0 to 2 Volts	0 to 0.5 Volts	0 to 0.5 Volts (Sometimes)
Supply Voltage	± 5 Volts. Goal - +5 Volts only.	Single +5 Volt Supply	Single +5 Volt Supply	Single +5 Volt Supply
Output Impedance	50 Ω, nominal	50 Ω, nominal	50 Ω, nominal	Untested
Size	60x60 mil ANACHIP	N/A	Fit	Fit

TEST SUMMARY:

The VCO output frequency ranged from 1.005 to 1.155 GHz, approximately 50 MHz below simulations and 70 MHz below the specified range. The output range is sufficient to cover the specified parameter, 100 MHz. The 5 volt single supply bias current measured 74 mA, 10% below simulations. The measured output power, 18.5 dBm, (include 0.5 dBm of cable loss) was 0.5 dBm less than expected. The low 2^{nd}, 3^{rd}, and 4^{th} harmonic power levels indicate a clean sinusoidal signal. The second chip's functionality repeatedly ceased when the tuning voltage exceeded 3.3 volts. This failure, collapse of the oscillator's amplitude, mirrored the intermittent simulation failures seen while tuning the final design.

TEST DATA:

Chip 1:

VTune (V)	Freq (GHz)	Power dBm	P(h2) dBm	P(h3) dBm	P(h4) dBm
0.0	1.005	17.8	-40.0	-19.3	-25.5
0.5	1.012	17.8	-42.0	-18.2	-24.5
1.0	1.036	18.0	-41.2	-17.5	-23.3
1.5	1.058	18.0	-36.8	-18.3	-22.7
2.0	1.084	17.7	-34.2	-21.2	-23.7
2.5	1.113	17.0	-32.8	-25.3	-25.7
3.0	1.133	17.0	-29.8	-26.5	-25.7
3.5	1.142	16.8	-29.0	-27.8	-25.7
4.0	1.147	16.8	-28.7	-28.3	-25.8

4.5	1.151	16.7	-28.0	-28.5	-25.5
5.0	1.155	16.7	-27.8	-28.7	-25.3

Chip 2:

VTune (V)	Freq (GHz)	Power dBm	P(h2) dBm	P(h3) dBm	P(h4) dBm
0.0	1.008	17.3			
0.5	1.014	18.0			
1.0	1.038	18.0			
1.5	1.060	18.0			
2.0	1.085	17.5			
2.5	1.114	16.5			
3.0	1.133	16.2			
3.3	1.138	15.7			

Stops Oscillating VTune > 3.3.

IDENTIFIED PROBLEMS:

Frequency range offset 50 MHz low:

1) A possible source of this offset is that some parasitic capacitances and inductances of elements in the resonant tank were not included in the respective device models, resulting in simulated frequency incorrectly high. Since, other classmate's designs agreed well with their respective simulations, incomplete parasitic modeling has low probability as the source of the error.

2) Another possibility is that the fabrication process yielded elements at the extreme or outside their tolerances. Since, other classmate's designs agreed well with their respective simulations, extreme fabrication process variance has a low probability as the source of the error.

3) Simulations indicated that small changes in either the absolute value of the Cgs or in the ratio of the Cgs to the source resistor's bypass capacitor, typically induced oscillator frequency shifts. There is a high probability that the design's need for Cgs in absolute terms led to the frequency shift.

Oscillation collapse with high Vtune:

1) The, parallel resonator, current supply for the FET amplifier is centered at an incorrect frequency, and may have insufficient bandwidth to cover the entire frequency range with a high enough impedance for the FET's output. This concept has a fair probability of contributing to the oscillator collapse due to three factors.

A. The element values of this resonant tank are C = 10.1 pF and L = 2.0 nH. Inserting the values into the resonance equation, $f_0 = 1/(2p\sqrt{LC})$, yields an ideal resonant frequency of $f_0 = 1.1198\,\text{GHz}$. The fabricated elements contain parasitics which do alter their frequency responses.

B. The unloaded Q of a parallel resonator varies with C and inversely with L, equation 6.18 Pozar[5], as shown in the following equation. $Q = w_0 \frac{2W_m}{P_{loss}} = \frac{R}{w_0 L} = w_0 RC$. Where $W_m = W_e$ at resonance. So, the low inductor value, and the high capacitor value yield a high Q resonator, which has little bandwidth. BW = 1/Q, equation 6.21 Pozar[5].

C. The oscillator's output frequency is incorrect. Therefore, the high impedance of the current supply occurs at an incorrect frequency.

2) A within allowable parameter process variation created a larger variance for Cgs than the design's small tolerance. This idea also has a fair probability of contributing to the oscillator collapse. As previously discussed, the design tolerance for Cgs is very small.

3) The amplifier needs more gain. More gain from the amplifier could conceivably overcome the other two mentioned design weaknesses.

RE-DESIGN STRATEGY:

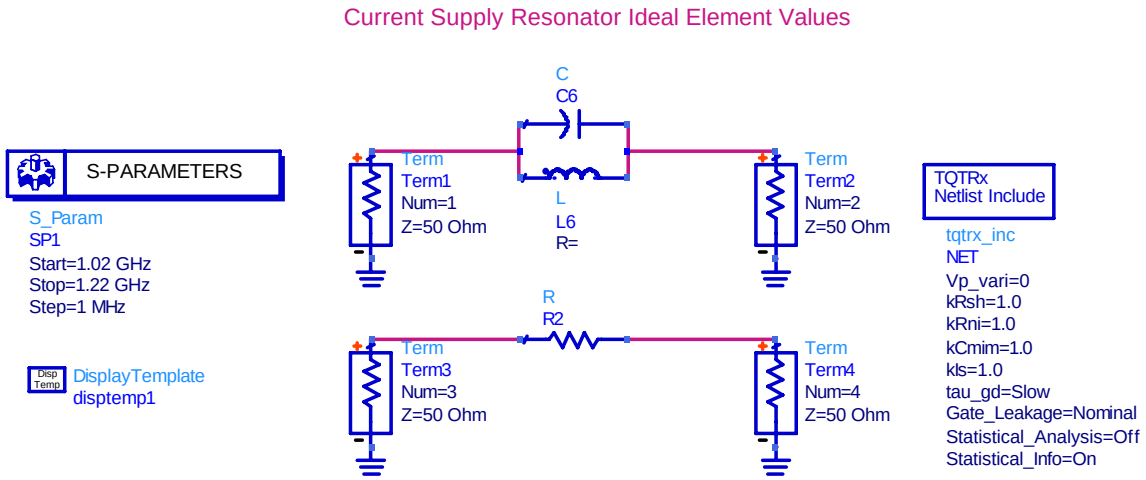
Correct the output frequency range:

The simulation results of the post-layout circuit, listed in the Specifications Compliance Matrix, align closely with the tested results. To increase the frequency range, raise the frequency of the resonance tank. Because the capacitance in the resonant tank is set primarily by the varactors, the diode connected FETs, increase the resonance tank frequency by reducing the inductor's value. As with the original design, tweak this inductor value to tune the final output frequency when the other changes are complete.

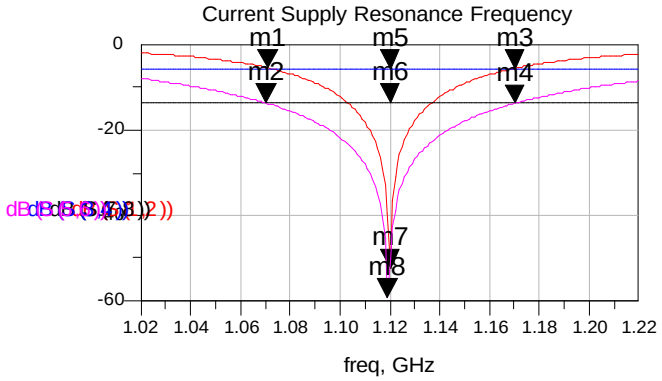
Improve the bandwidth of the current supply:

The parallel resonator current supply serves two functions. One, the inductor in the resonator has little voltage drop; parasitic resistance contributes approximately 32 mV at the 25 mA drain current of the new DFET VCO. Therefore the transistor drain is biased very near to the supply rail. Two, the parallel resonator appears to the transistor drain as a high impedance branch. So, the power of the oscillator will flow through the output port, not into the voltage supply. However, the resonator's high impedance is

frequency dependent. At the resonant frequency an ideal element circuit produces a very high impedance, yielding a transmission coefficient, S(2,1) through the resonator greater than -50 dB. However, the high impedance aspect of a parallel resonator is frequency dependant. The below circuit, setup for linear S-Parameter simulations will demonstrate how the high impedance of a parallel resonator diminished quickly as the operating frequency shifts away from the resonance frequency.



An ideal resistor is simulated simultaneously with the parallel resonator to provide an ohmic comparison to the transmission coefficient result expressed in decibels, dB. The simulations show a 5% shift away from the resonant frequency lowers the transmission coefficient from -52 to -5.5 dB. An 88 ohm series resistor produces -5.5 of attenuation, and 380 ohms produces to -13.6 dB. To produce -50 dB, R = …



Red - 1.12 GHz, Ideal Elements:
L = 2.0 nH, C = 10.1 pF

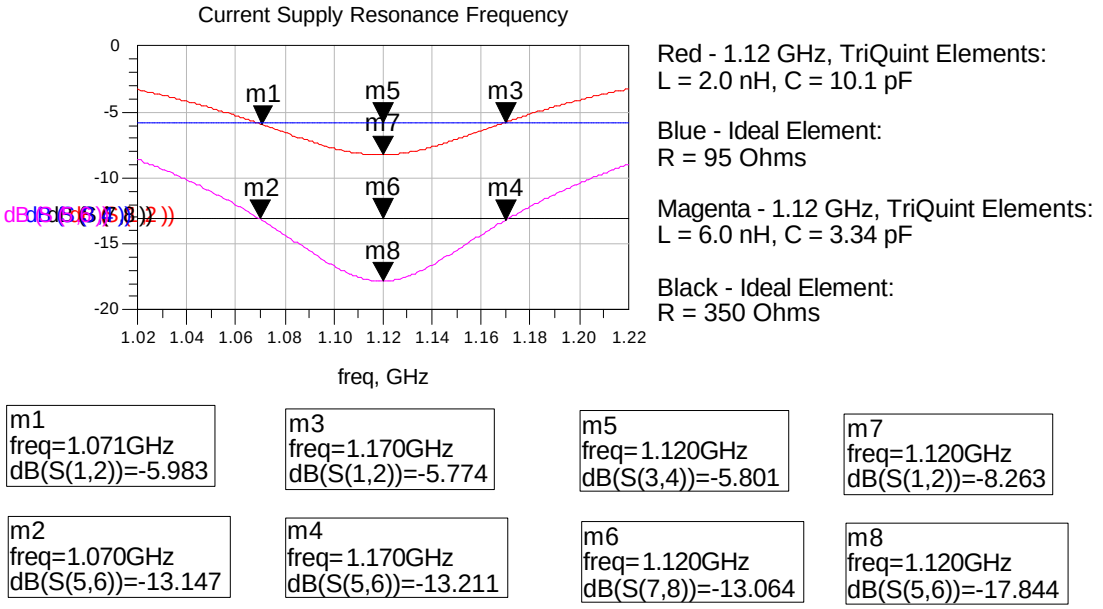
Blue - Ideal Element:
R = 88 Ohms

Magenta - 1.12 GHz, Ideal Elements:
L = 6.0 nH, C = 3.34 pF

Black - Ideal Element:
R = 380 Ohms

m1 freq=1.071GHz dB(S(1,2))=-5.429	m3 freq=1.170GHz dB(S(1,2))=-5.531	m5 freq=1.120GHz dB(S(3,4))=-5.483	m7 freq=1.120GHz dB(S(1,2))=-52.368
m2 freq=1.070GHz dB(S(5,6))=-13.610	m4 freq=1.170GHz dB(S(5,6))=-13.734	m6 freq=1.120GHz dB(S(7,8))=-13.625	m8 freq=1.119GHz dB(S(5,6))=-59.287

As shown in the previous graph, changing the resonator element values from L = 2.0 nH and C = 10.1 pF to L = 6.0 nH and C = 3.37 pF increase the impedance from approximately 88 to 380 ohms, for ideal elements. What kind of changes occurs with real elements? The largest discrete inductor in the ADS TriQuint palette is 6 nH. Rewriting the resonance equation in terms of C yields. $C = \frac{1}{(2pf)^2 L}$. Solving for C yields. C = 3.37 pF. Substituting TriQuint elements into the resonator circuit, yields the below graph.



Although the very high impedance at the resonant frequency is lost, due to parasitic losses included in the TriQuint models, the bandwidth of the resonator's impedance improves from -5.8 dB to -13.2 dB, with the larger inductor.

Provide more circuit gain:

The gain in this oscillator circuit is the gain of the MESFET common source amplifier. The unilateral transducer power gain, GTU, is the most useful definition of gain for an amplifier because it takes into consideration the source and load mismatches[6].

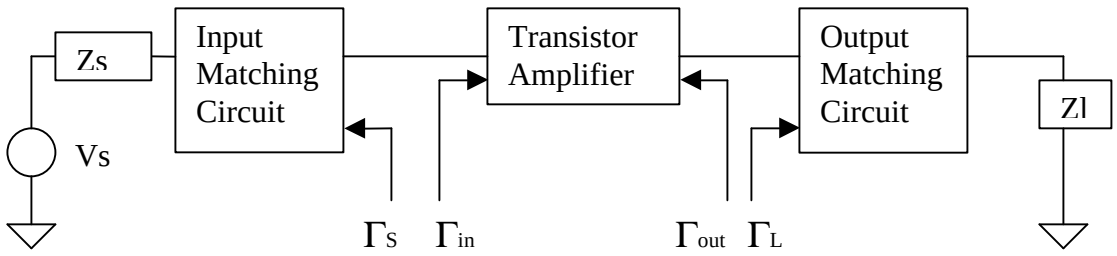
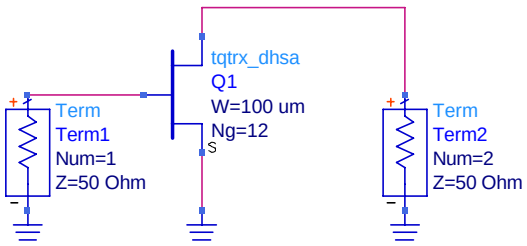


Figure 11.8, redrawn from Pozar, p.610.

As illustrated above, GTU is comprised of three components; the input matching circuit, G_S, the transistor, G_O, and the output matching circuit, G_L. Where: $G_S = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}$, $G_O = |S_{21}|^2$, and $G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}$. However, as its name implies, these simplified GTU formulae are valid only if the transistor is a unilateral device, $S_{12} = 0$, or very small. To confirm that S_{12} is very small, examine the S parameter file of the device in question or simulate or test the device. $|S_{12}|$ = 0.050, at 1.17 GHz, in the below S parameter simulation circuit. The GFET device value is 0.022; both values are close enough to zero to satisfy the simplification requirement, that the device is unilateral.



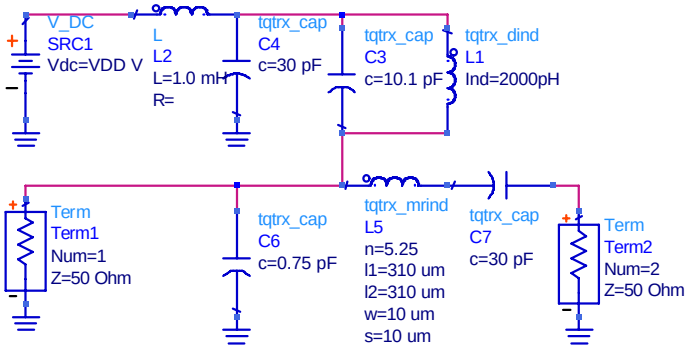
S parameter simulations of bare transistors yielded the following results.

Bare FETs

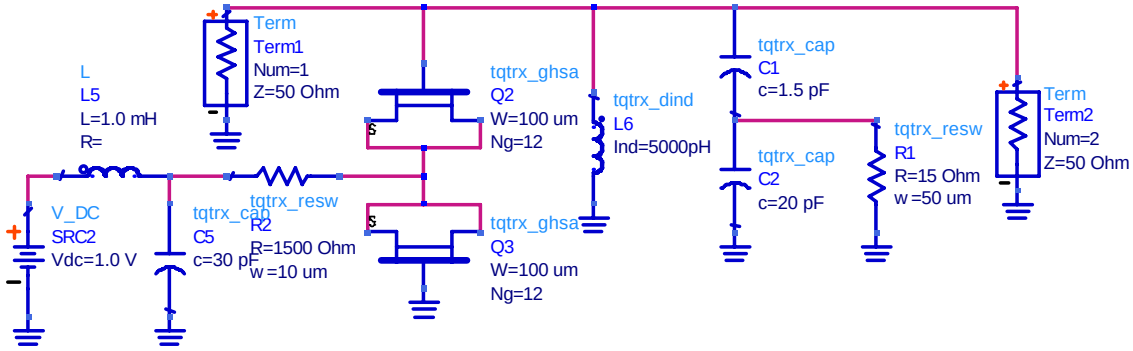
DFET	S11	S21	S22	ΓL	ΓS	Gs	Go	Gl	GTU
f_L	0.968	0.047	0.818	0.327	0.335	1.944327	0.002209	1.664386	0.007149
f_C	0.965	0.048	0.818	0.302	0.296	1.787901	0.002304	1.602943	0.006603
f_H	0.963	0.05	0.818	0.285	0.258	1.652622	0.0025	1.562304	0.006455

GFET	S11	S21	S22	ΓL	ΓS	Gs	Go	Gl	GTU
f_L	0.983	0.021	0.863	0.209	0.122	1.271888	0.000441	1.423521	0.000798
f_C	0.981	0.022	0.863	0.074	0.093	1.20039	0.000484	1.134842	0.000659
f_H	0.98	0.022	0.863	0.15	0.068	1.142586	0.000484	1.289821	0.000713

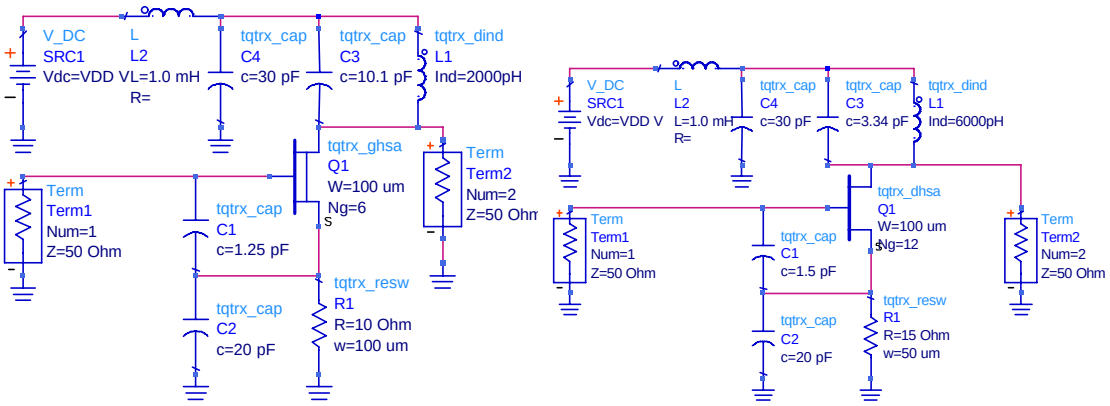
The above table calculates the GTU at the low, center and high frequency points in the specified range of operation. The OMN for bare device gain calculations is all the components forming a path to ground from the transistor gate, as shown below for the GFET device.



The IMN is similarly all the components on the input side, connected to the transistor gate, as shown below for the DFET device calculations.



The results table indicates the DFET amplifier has 10X the gain of the GFET amplifier. However, device manufactures provide S parameter data for devices under various biasing conditions. Therefore, perform the gain calculation for the devices under their respective biasing conditions. The two biased FET devices in their respective circuits are shown below.



Gain calculations on bias FETs yield less disparity, yet the DFET circuit still has approximately three times the gain of the GFET circuit. And, better matching of the output could improve further the DFET advantage.

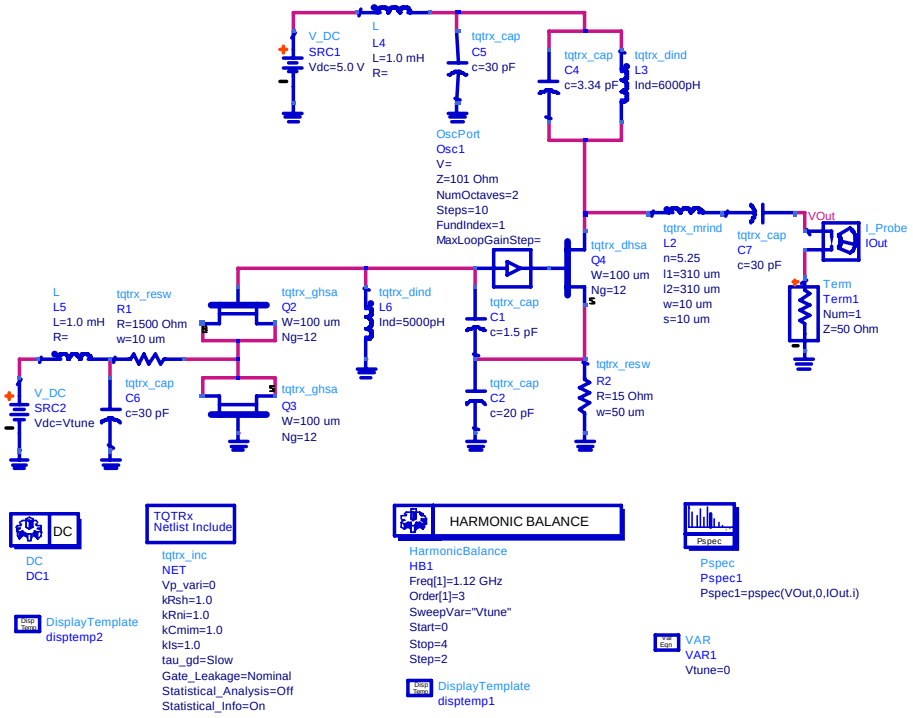
Biased FETs

DFET	S11	S21	S22	ΓL	ΓS	Gs	Go	Gl	GTU
f_L	1.391	5.524	0.583	0.339	0.292	2.594027	30.51458	1.374802	108.8233
f_C	1.34	5.316	0.611	0.356	0.271	2.284468	28.25986	1.426247	92.07669
f_H	1.297	5.092	0.633	0.373	0.252	2.066686	25.92846	1.475283	79.05449

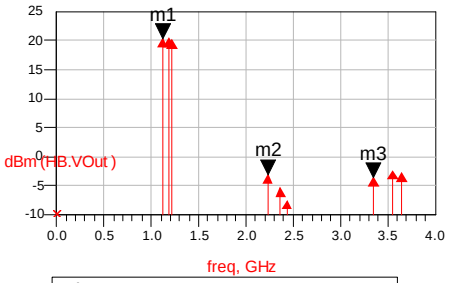
GFET	S11	S21	S22	ΓL	ΓS	Gs	Go	Gl	GTU
f_L	1.208	3.531	0.179	0.262	0.292	2.183398	12.46796	1.025267	27.91035
f_C	1.185	3.725	0.318	0.278	0.271	2.01051	13.87563	1.110359	30.97576
f_H	1.164	3.678	0.453	0.295	0.252	1.875297	13.52768	1.216346	30.85679

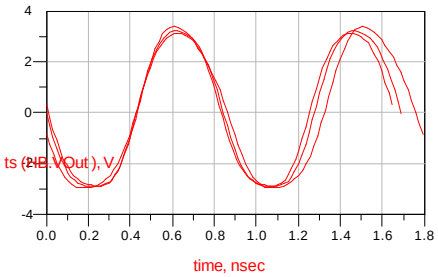
NEW 1.12 GHz VCO:

The redesigned 1.12 GHz VCO setup for a harmonic balance simulation.



Below are results from harmonic balance simulation on a circuit with no interconnects.





m1
freq= 1.115GHz
plot_vs(dBm(HB.VOut), freq)=20.360
Vtune=0.000000

m2
freq= 2.230GHz
plot_vs(dBm(HB.VOut), freq)=-3.082
Vtune=0.000000

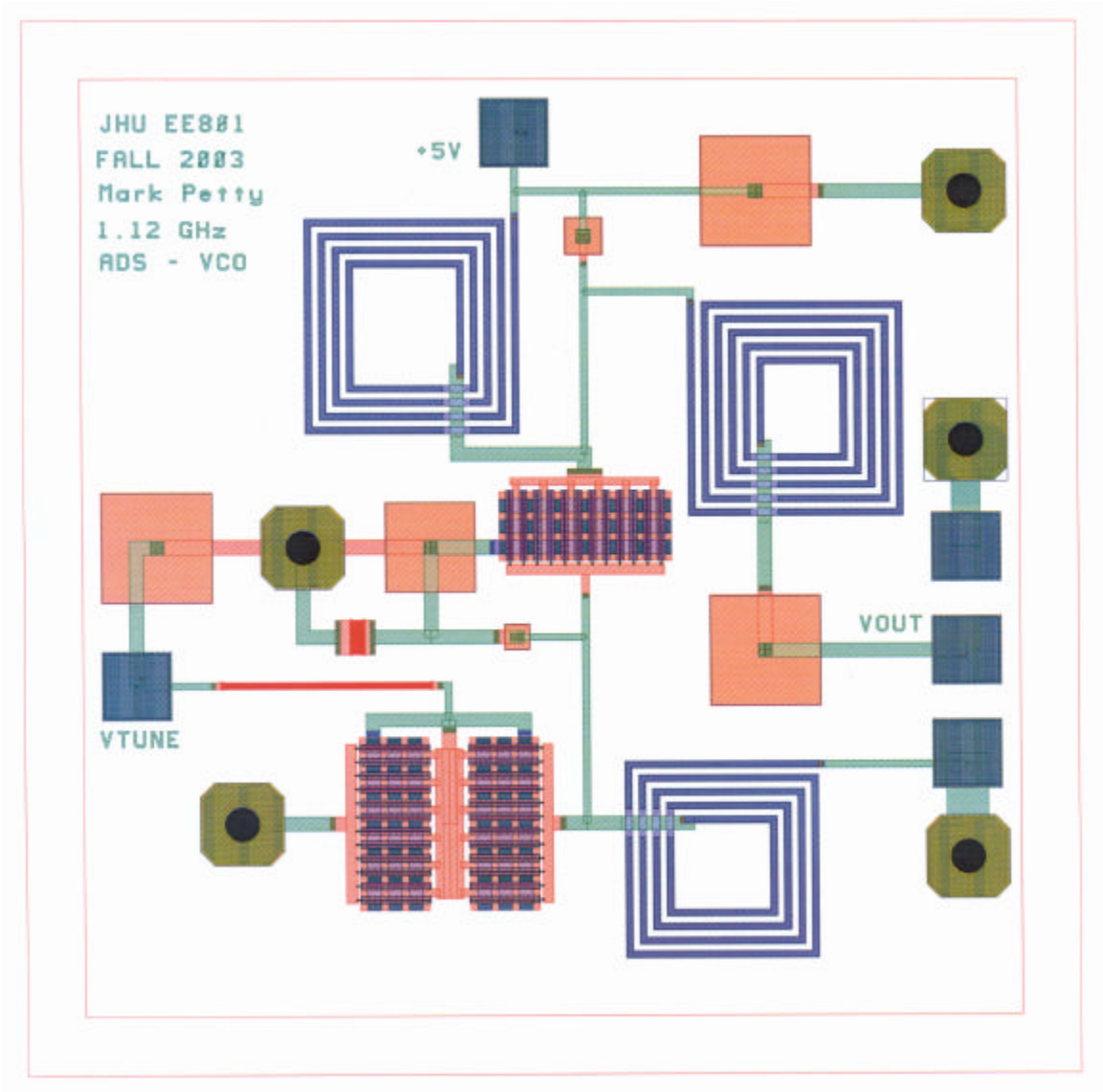
m3
freq= 3.345GHz
plot_vs(dBm(HB.VOut), freq)=-3.594
Vtune=0.000000

Eqn period = cross(ts(HB.VOut),1)
Eqn frequency = 1/period

time	period	frequency
Vtune=0.000		
426.8psec	0.0000 sec	<invalid>
1.324nsec	896.9psec	1.115E9
Vtune=2.000		
431.3psec	0.0000 sec	<invalid>
1.277nsec	845.6psec	1.183E9
Vtune=4.000		
429.8psec	0.0000 sec	<invalid>
1.253nsec	823.0psec	1.215E9

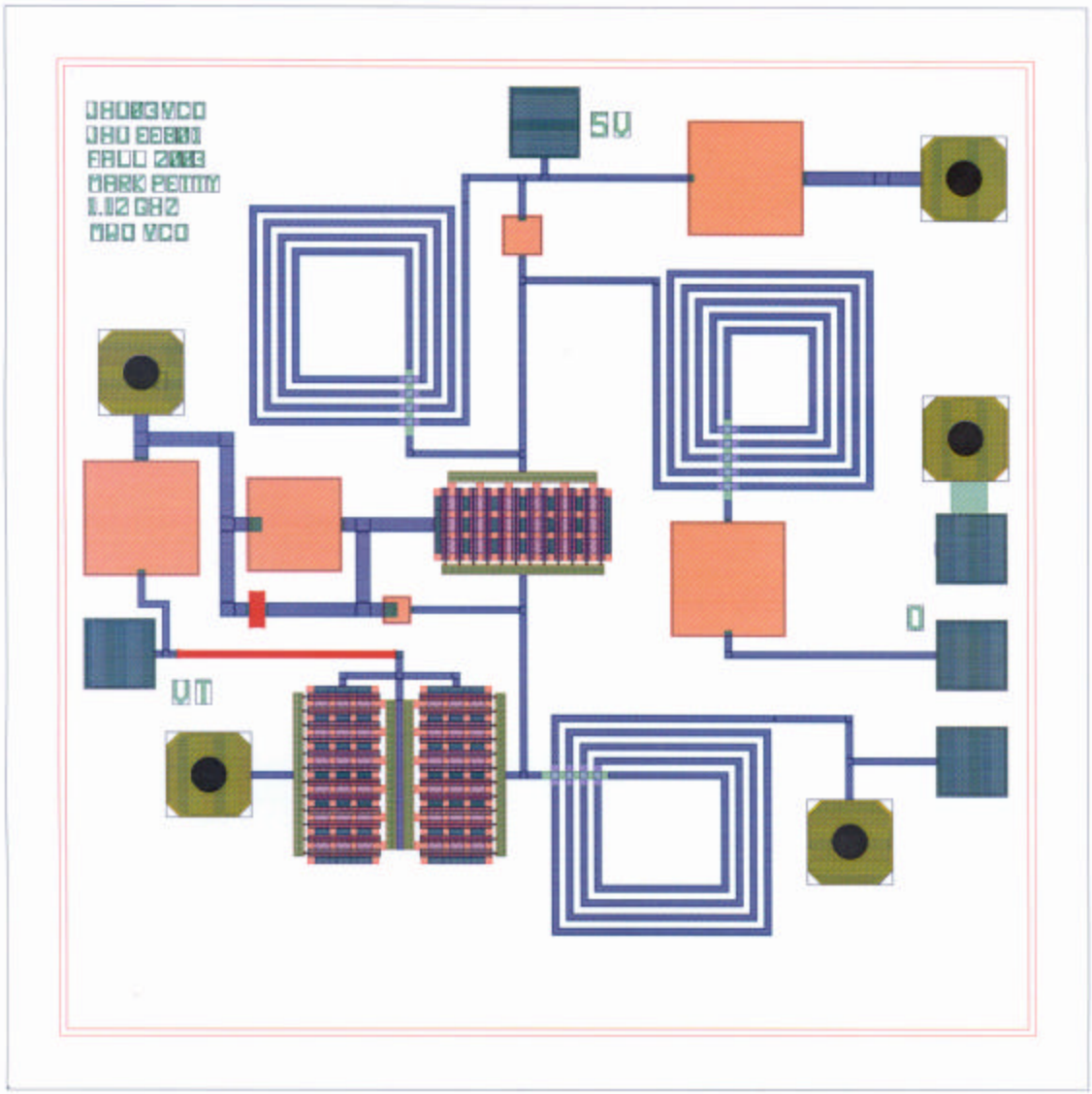
The previous device, when fabricated, had an output frequency approximately 50 MHz below the design simulations. Therefore, the output frequency of this circuit was purposefully designed approximately 50 MHz high.

The VCO design fits easily onto the ANACHIP frame, as shown below.



Microwave Office Comparison:

One of the original intents of this project was to compare simulation results from both Applied Wave Research's Microwave Office, MWO, and Agilent's ADS tool to measured data from a fabricated chip. However, later than expected delivery of the software and problems executing the TriQuint process library file limited the MWO aspect of this report to the layout of a nearly identical 1.12 GHz VCO, with the idea that simulations on the design would be completed later.



Conclusions:

The common source configuration for MMIC VCO design is problematic. The output frequency is unpredictable without EDA tools. The output frequency is affected by not only the input resonator tank, but both the external gate to source capacitance and the output matching network. Following the design methodology in the gEE-CAD tutorial, the resultant circuit had a gate transmission line of ~2700 μm and a drain transmission line length of ~7000 μm. And then both the harmonic balance and transient simulations failed to oscillate. Although this circuit configuration can yield a clean sinusoidal output, a repeatable design methodology that could predict the output frequency without excessive tweaking of element values was not found. Therefore, the author does not recommend using a common source configured VCOs.

The author would like to thank the Agilent Technologies, for the license to use their ADS software at home, and Gary Wray, their technical consultant whom jovially guides the class through many fits and starts during the semester. Thanks also to John Penn and Craig Moore, for their guidance and understanding through this troubling semester.

To Mr. Moore and Mr. Penn, this design may be over, but the project continues...

REFERENCES:

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