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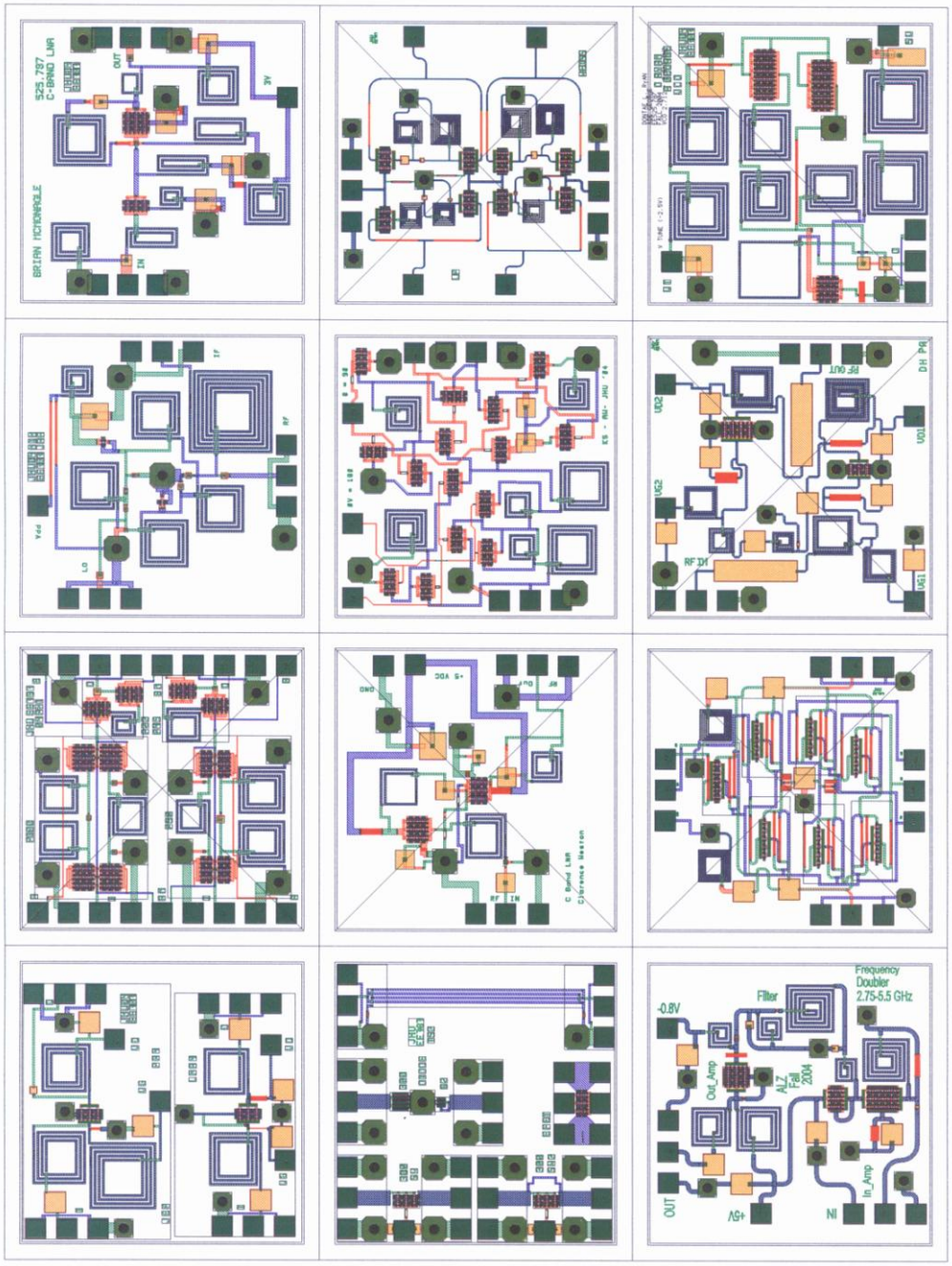

C-Band Stepped Attenuator MMIC

By:

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Microwave Monolithic Integrated Circuit (MMIC) Course
Johns Hopkins University
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Abstract

This paper documents the design and analysis of a stepped attenuator in the 5.8GHz Industrial Scientific-Medical (ISM) band, utilizing TriQuint TQS TRx process. The design was completed to fulfill the final requirements of the Microwave Monolithic Integrated Circuit (MMIC) course at the Johns Hopkins University. The design was completed utilizing Microwave Office in conjunction with the TriQuint add-on library.

Introduction

This paper is organized with a general statement of project goals, a brief outline of the project history and finally the design simulation and layout of the final circuit. Generally, stepped attenuators provide a controlled mechanism for dissipating signal power. The goal for this project was attenuation range of 0 to 9 dB in 3 dB steps operating in the 5.8GHz ISM band. The design was performed utilizing Microwave Office with the TriQuint TQS TRx add-on library and the finished design is to be fabricated by TriQuint Oregon on a 60mil x 60mil GaAs substrate. The specifications for the stepped attenuator are listed in table 1.0.

Frequency	5.15 GHz – 5.875 GHz
Insertion Loss (dB)	< 3dB with steps of 3dB
VSWR	< 1.5:1
Supply Voltage	+/- 5 volts
Control	TTL control signals

Table 1.0 – Stepped Attenuator MMIC circuit design specifications

The primary function of the circuit is specified in table 1.0 as the insertion loss. The insertion loss is the same as the attenuation but the specifications are not as stringent, basically allowing for an additional 3dB of loss. This additional loss can be thought of as an offset so, instead of 0dB attenuation 3dB, while maintaining the 3 steps of 3dB to a maximum insertion loss of 12dB.

Design Approach

The initial design approach was to switch pi or tee fixed attenuator networks in series. Each of the networks would be fixed attenuators with 3dB of attenuation, thus providing the necessary steps. The values for the networks were obtained using the design equations provide by [1] and it was decided that Tee networks would be more easily realizable. This decision came about due to the resistance values required for the two network topologies. As an added benefit the tee networks would occupy less area due to need for only one substrate via for ground. Next switches were designed using a GFET MESFET transistor. Initially a quick schematic consisting of a single FET and DC blocking caps was generated and simulated using Microwave Office. This was done to get a rough ideal of the number of gate fingers and the appropriate size. Next, a circuit schematic for an attenuator with two steps was generated and simulated. From these simulations it was determined that the insertion loss for the 0dB case exceeded the specification when additional sections were added. As a result of the initial simulations alternate configurations were investigated. One configuration was a PI topology where the shunt resistors were switch to ground and the series resistor was switched between multiple values. This topology initially proved promising with the exception of the 0dB attenuation case. Another switch was place in parallel with the network to provide a lower insertion loss path by shorting out the attenuator network. This design was later abandoned due to problems in the tightly coupled design that arose during tuning with non-ideal elements. The circuit did not provide any great advantage in complexity compared with multiple switched parallel tee or pi networks and was not developed further. The final design decided upon was parallel-switched paths of attenuators. The

circuit consists of two single pole triple throw switches connected to 0, 3 and 6 dB attenuators. Each switch has in insertion loss of about 1.5dB so the switched network is then placed in parallel with a low insertion loss switched path to provide the 0dB case. This configuration provides approximately 3,6,9 and 12 dB of insertion loss.

The switches can be simply modeled as a large resistance in parallel with a capacitor when off and a small resistance in parallel with a capacitor when on. The capacitance degrades performance of the circuit by increasing the mismatch. This problem was countered by placing shunt inductors on the input and output. These shunt inductors completed the high pass transmission line equivalent circuit and provided a good match for both the input and the output. The schematic of the circuit is shown in figure 2.0

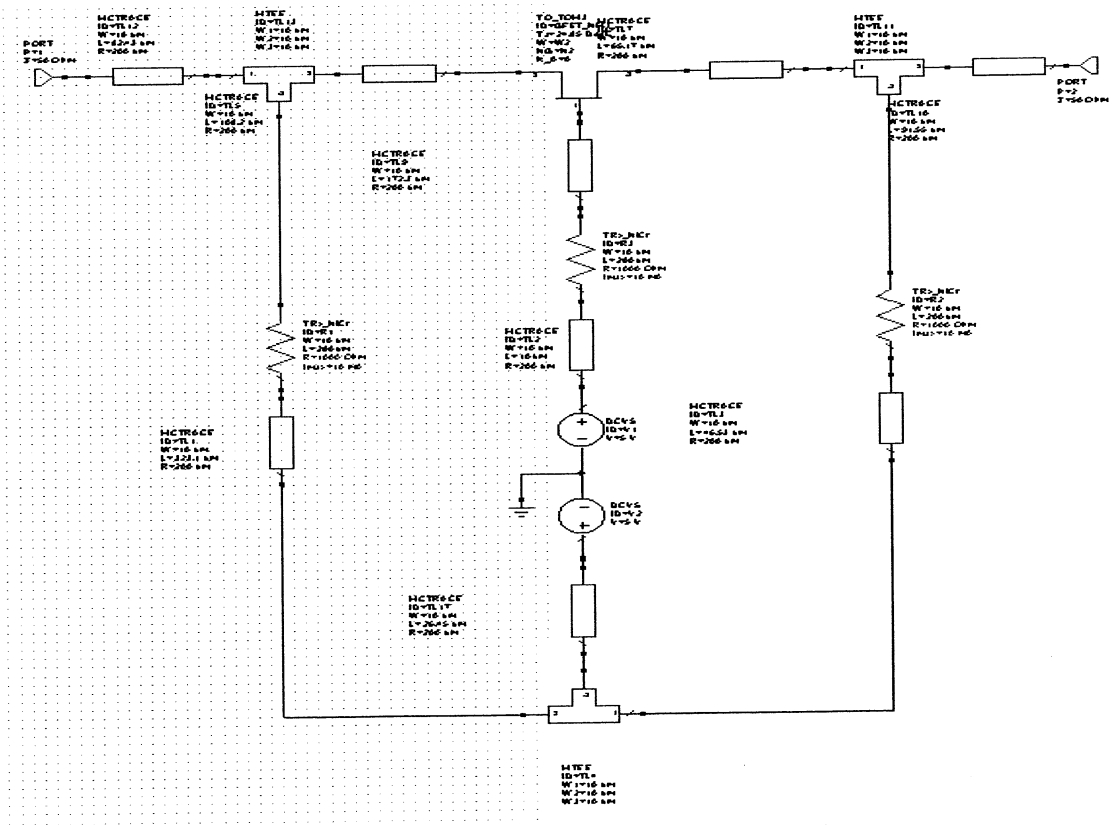

Figure 1.0 – TTL controlled FET switch schematic

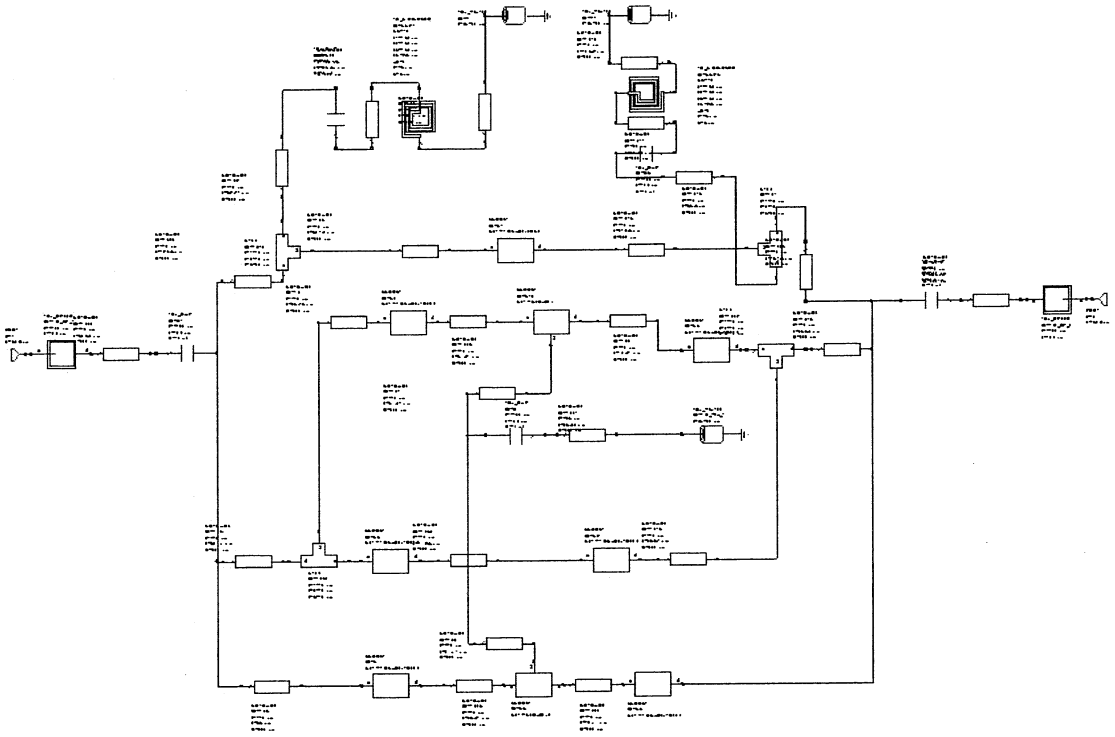

Figure 2.0 – Stepped attenuator schematic

In figure 2.0 the circuit consists of, from top down, the shunt inductors used for match improvement with DC blocks. Next, the low insertion loss path, a single switch. The next horizontal path is the 6dB insertion loss path, consisting of two switches and a 3dB fixed attenuator. Directly below that is the 3dB path, consisting of two switches and then finally, the 9dB path, which consists of two switches and a 6dB, fixed attenuator. The circuit is operated by applying 5V to gates of the switches that make any one and only one path through the circuit. Although, the circuit will not suffer and ill effects by turning on multiple parallel paths though the circuit it was not intended to be operated in this fashion and simulations of these alternate states were not performed. The following figures 3.0 thru 3.3 depict the simulation results of the circuit.

Simulations

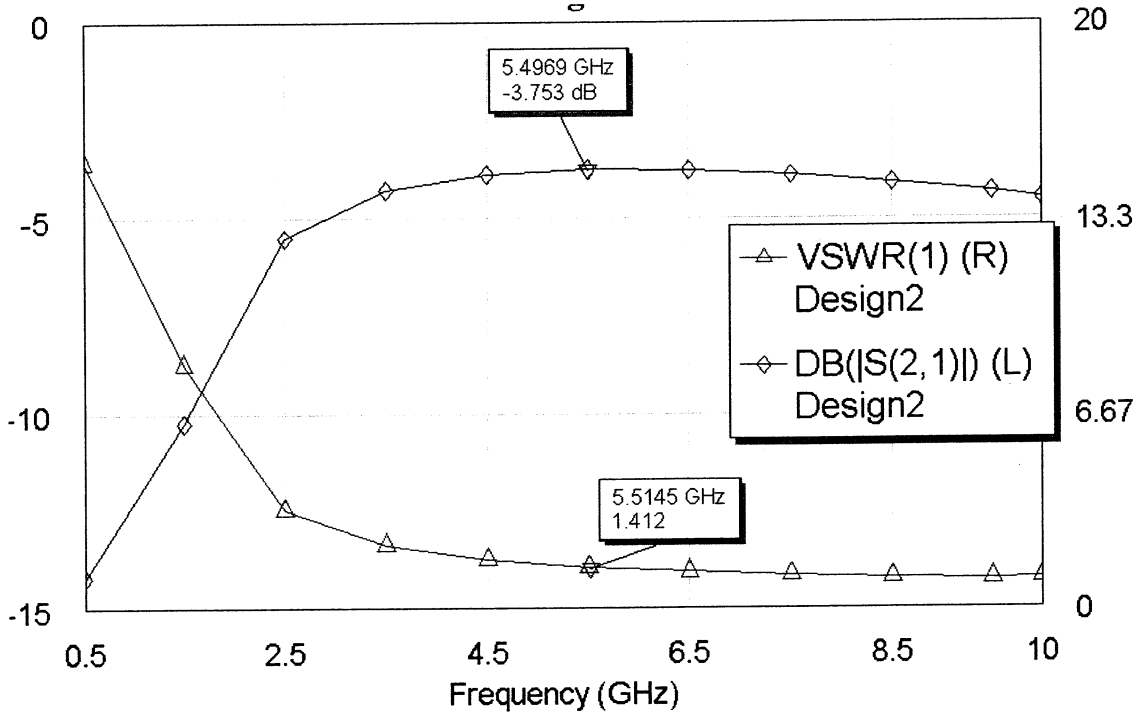

Figure 3.0 – Stepped attenuator simulation 0dB configuration.

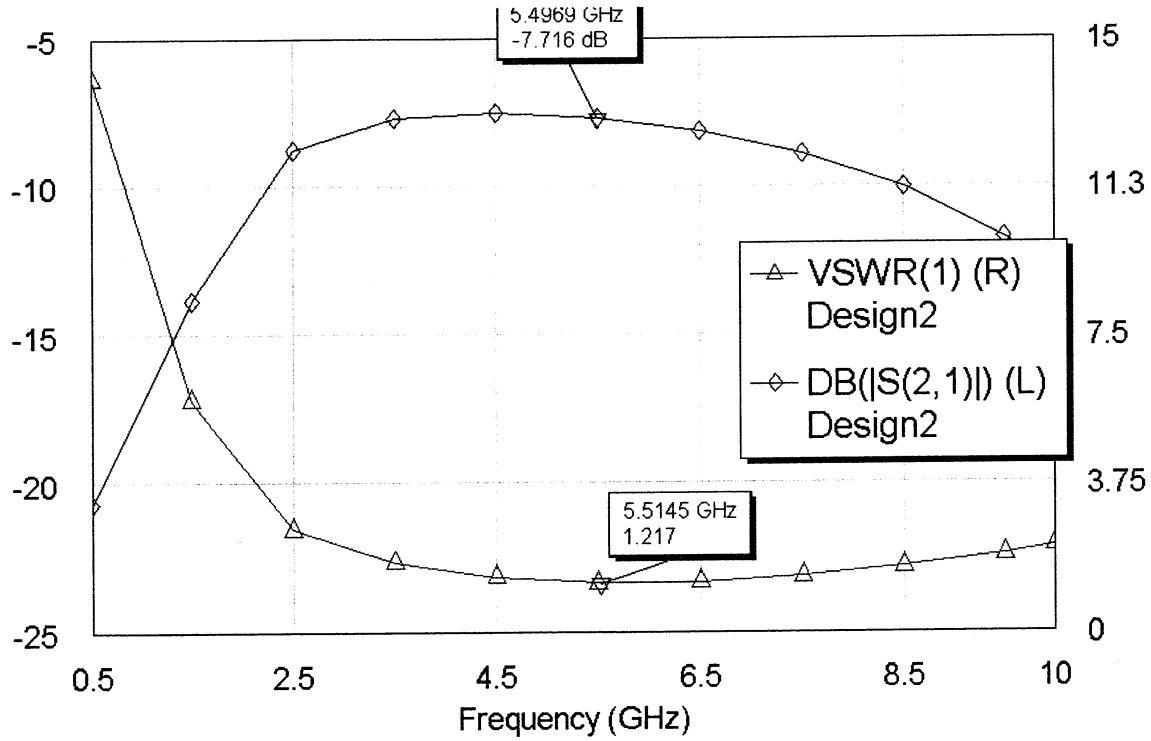

Figure 3.1 – Stepped attenuator simulation 3dB configuration.

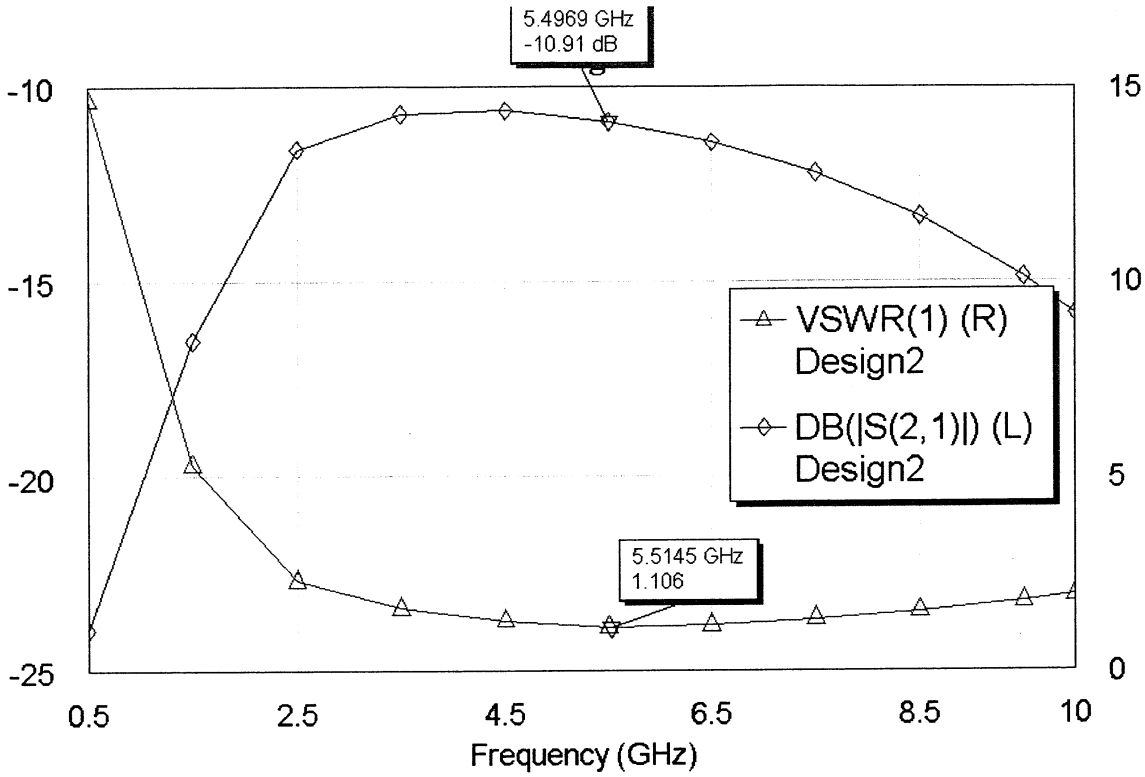

Figure 3.2 – Stepped attenuator 6dB configuration.

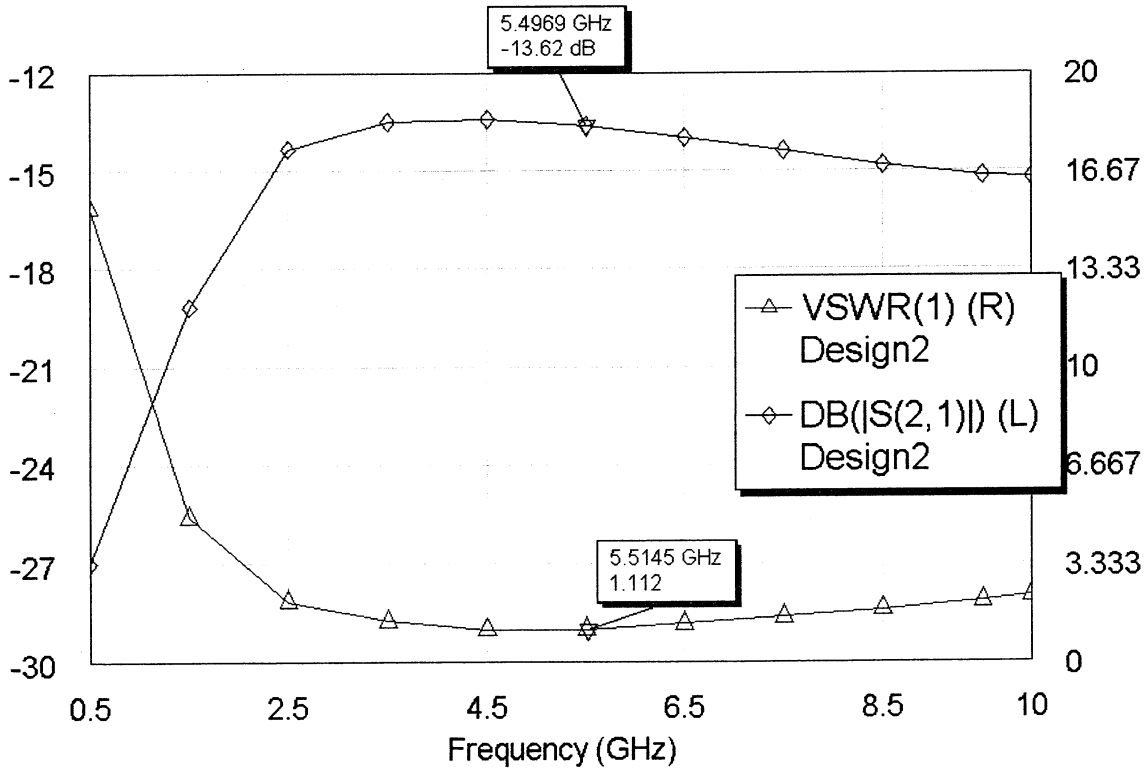

Figure 3.3 – Stepped attenuator 9dB configuration.

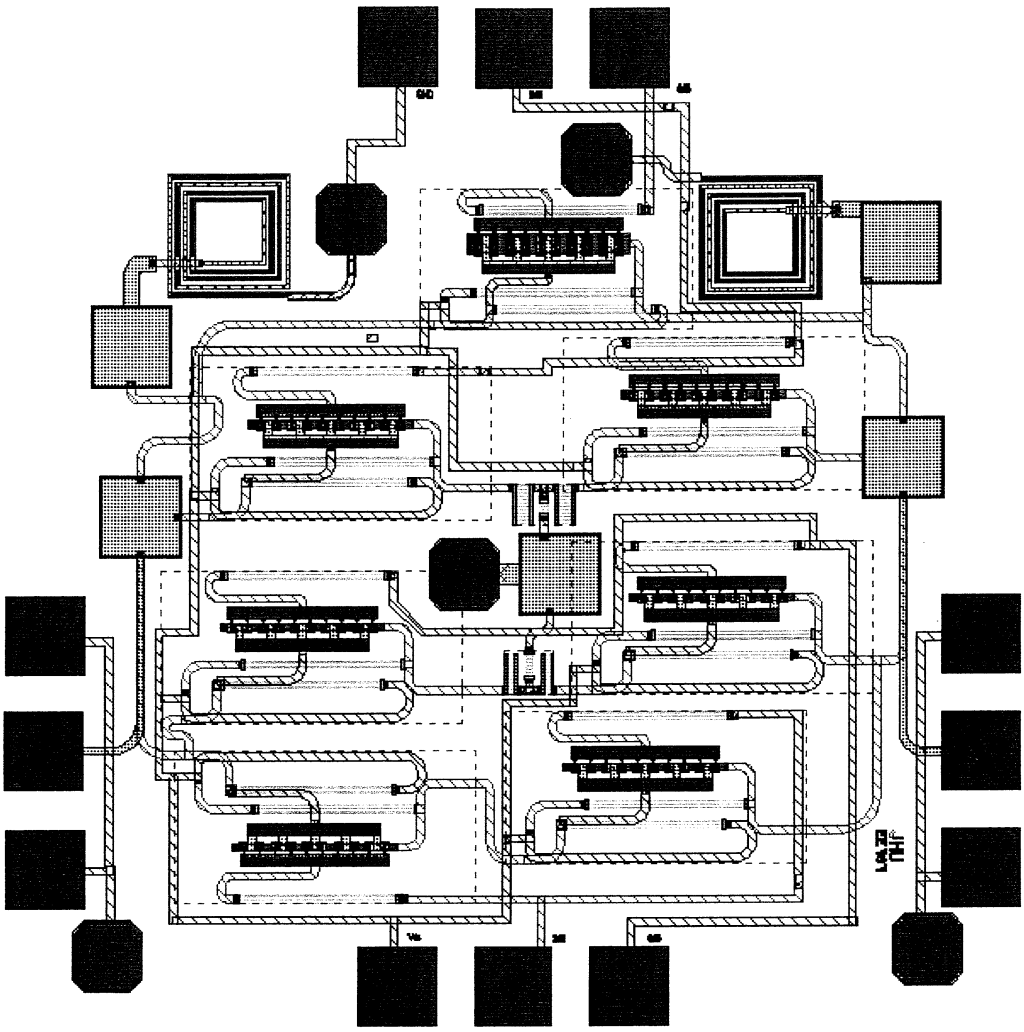

Figure 4.0 – Stepped attenuator layout schematic.

Test Plan

The equipment needed to test the circuit is listed in table 2.0 below. The procedure to test the circuit is fairly, straight forward. In figure 4.0, the circuit layout, the set of bond pads on the left and right hand side are the ground-signal-ground (GSG) connections for the RF input and output. There is no preference as to which side is the input or the output since the switches work in either direction. The sets of pads along the top and bottom are labeled and are for the DC supply voltage and TTL control signals. It should be noted that if alternate control signals are desired, say CMOS 3.3V, these can easily be accommodated by altering the DC bias of the drain and source to 3.3V in this example. The DC bias pad is labeled Vdc and is the left most bond pad located in the bottom set of three bond pads of figure 4.0. To test this circuit a network analyzer should have a full 2-port calibration performed over the frequency range. The DC bias should be applied to the circuit and all the TTL control bond pads tied to ground. The GSG probes should be connected to the network analyzer to take initial measurements and to check for any faults. In this state, off, the insertion loss should be high a low insertion loss may indicate a sever problem. If no errors are detected then the 0dB bond pad should be disconnected from ground and the control voltage applied. This measurement should be recorded and then control voltage removed, dropping the pad voltage back to ground. This method should be repeated for the 3, 6, and 9 dB pads recording the resulting data at each stage of testing.

Network Analyzer operating in C-Band	DC supply operating at 5V for TTL and Biasing
Probing Station to connect to MMIC die	

Table 2.0 – Required testing equipment.

Summary & Conclusions

This paper outlined the design process and included tradeoffs that were considered during the design. The major problem in the design was to provide low insertion loss while maintaining the desired match. The design is not optimal and is evident from the above simulation plots. This is mainly a result due to time constraints of the project. The method and general topology are useful solutions and could possibly be altered to provide better operating performance. In order to improve the operation of the 0dB configuration the layout could be changed so that the single switch providing the low insertion loss is placed closer to the GSG pads at the lower half of the circuit. This would decrease the insertion loss, as much as a dB or more, due to the reduced interconnect lengths. The current layout, as mentioned previously, is top down 0, 6, 9 and 3 dB paths. The alternate, and believed improved solution would be to layout the circuit as 9,6,3,0 or 9,6,0,3 so that the paths of lower insertion loss would have shorter interconnects. The additional losses in the longer interconnect paths could then be absorbed by lowering the attenuation of the fixed tee networks.

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[2] Russell A. Gaspari and Harold H. Yee, "Microwave GaAs FET Switching", IEEE, 1978

[3] G. J. Gardiner, "Design Techniques for GaAs MESFET Switches", IEEE MTT-S Digest, vol. L-17 pp. 405-408, 1989

[4] Ronald J. Gutmann and Nitin Jain, "Comments on GaAs MESFET Baseband-to-Microwave Passive Switches", IEEE Trans. MTT vol. 37 no 7 pp. 1154-1155, July 1989.

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UNIVERSITY
Engineering Programs for Professionals

EE525.787 – Microwave Monolithic Integrated Circuit (MMIC)
Engineering and Applied Science Programs for Professionals

Professors: John Penn & Sheng Cheng

C-Band MESFET Low Noise Amplifier

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Abstract – This paper details a C-Band, *0.6mm* MESFET low noise amplifier MMIC, designed for use in a duplex transceiver employing a HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. The LNA design was simulated using Agilent's Advanced Design Systems (ADS 2003C). TriQuint Semiconductor, Oregon, provided small-signal and large-signal FET models resulting in the LNA having more than 17dB of gain, with a NF of less than 1.6dB, and an ITOI of +7dBm. Finally, the C-Band LNA was realized in a 60x60 mil ANACHIP footprint.

FIGURE 1: STAGE 1 – 300UM DFET (6 FINGERS X 50UM WIDE 5
FIGURE 2: STAGE 2 – 600UM DFET (6 FINGERS X 100UM WIDE 5
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1. Introduction

1.1 Circuit Description

The LNA design utilizes a two-stage cascaded topology operating at C-Band frequencies (5150MHz – 5875MHz). The first stage of the LNA is a noise matched 300um DFET feeding a 600um DFET. The second stage is conjugate matched to provide the 17dB of gain and nominal 1.5dB NF across the 0.8GHz operating bandwidth. The LNA employs a self-biased configuration on both stages to eliminated needless gate bias complexity while allowing the MMIC to operate using a single +3V power supply. Stability for the LNA is addressed using source feedback on the first stage and gate-to-drain feedback on the larger second stage. Similarly, a small resistance is added in the drain bias path on the first stage to further increase stability at low frequencies. Finally, this C-Band LNA is designed with to fit into a 60x60 mil ANACHIP layout.

1.2. Design Philosophy

The LNA design was realized using large signal MESFET models from TriQuint Semiconductor, Oregon. The basic low noise amplifier design consisted of noise matching the 300μm input stage and conjugately matching the following 600μm stage. Once a noise match was determined for the 1st stage, and a basic gain match satisfied for the 2nd stage, the LNA was then optimized to meet the design requirements and compact the layout.

1.2.1. Transistor selection

The bias configuration for the two stages of the LNA was set to approximately 50% Idss for both stages. The 300μm DFET produced a reasonable noise match when biased at ~2V Vds with 11mA of drain current. The 600μm second stage was bias at ~3V Vds and 22mA of drain current. The second stage bias was selected in part to help improve the LNA's linearity, as it drew more drain current.

1.2.2. Transistor Stability

Both stages of the LNA employed stability enhancing techniques. Source feedback was implemented on the 300μm DFET to lower gain and increase its stability. Similarly, drain-to-gate feedback was designed on the 600μm DFET to help flatten the overall gain of the LNA adding to the stability margin of the MMIC. Finally, by using a self-biasing configuration for both stages, the instabilities associated with off chip gate biasing was eliminated, further increasing stability.

1.2.3. First stage input matching network

The design of the input-matching network (IMN) was determined solely by noise matching the 300μm DFET with its added source inductance. The simple three-element matching network allowed for a reasonable input match while limiting the amount of loss presented to the 1st stage DFET.

1.2.4. Interstage matching network

Once the IMN was determined, the interstage network was chosen to provide the bandwidth for the LNA. Increasing the series capacitance on the gate of the 2nd stage extended the low-end frequency response. The drain-to-gate feedback on the 2nd stage was incorporated into the design of the interstage. This feedback allowed the gain of 600μm DFET to be reduced and flattened.

1.2.5. Second stage output matching network

As with the interstage, the design of the output matching network (OMN) also involved tweaking the feedback around the 2nd stage DFET. As with the IMN, a similar three-element network was chosen providing a excellent output match while reducing the size of the layout.

1.2.6. Design optimization

Once the basic design topology was determined, the simplified LNA model was then optimized. It is important to selecting appropriate ranges for the design elements during the optimization process so that the simulator does not blindly optimize. This process quickly yielded a LNA model that satisfied the majority of the design requirements.

1.2.7. Design layout

After the LNA was initially tuned to meet the design requirements, it was then brought into layout and tweaked to fit into the 60x60 mil ANANCHIP footprint. This iterative process finally yielded the layout shown in Figure 12.

1.3. Trade-offs

Many trade-offs are implemented in designing low noise amplifiers, including trades on gain, stability, noise figure, match, and IP3. While all of these parameters are important to successful circuit design, this C-Band LNA had only one major trade-off, NF vs. input VSWR.

As with most LNA designs, input match is often traded to improve noise figure. While the spec for this C-Band LNA required a noise figure of 4dB, the design was optimized to minimize noise figure. In the effort to reduce the NF to ~1.6dB, the input VSWR specification was relaxed from 1.5:1 to a 2.1:1 ratio, resulting in a -9dB input match. Giving up 5dB of input match for a 2.4dB improvement in NF seemed to be a reasonable trade.

2. Modeled Performance

2.1. Specification Compliance Matrix

Table 1: Specification Compliance Matrix

Parameter		Units	Requirement	Design	Compliance	Comments
Size		mils	60 x 60	60 x 60	Yes	
Rx	Frequency	GHz	5.15-5.875	5.15-5.875	Yes	
	Bandwidth	GHz	0.8	0.8	Yes	
	Receive Gain	dB	>15	>17	Yes	
	Gain Ripple	dB	±0.5	0.1	Yes	
	Noise Figure	dB	4	<1.6	Yes	2.4dB improvement
	TOI	dBm	>5	7.2	Yes	
	Input VSWR		1.5:1	2.1:1	No	Traded VSWR Spec for improve noise figure
	Output VSWR		1.5:1	<1.2:1	Yes	
	Rx Current	mA		27	Yes	
	Rx Voltage	V	5	3	No	Need to add a TAN resistor to layout, w=30um, l=38um
	Stability		unconditional	unconditional	Yes	

2.2. Predicted Performance

2.2.1. Large Signal DFET DC Simulations

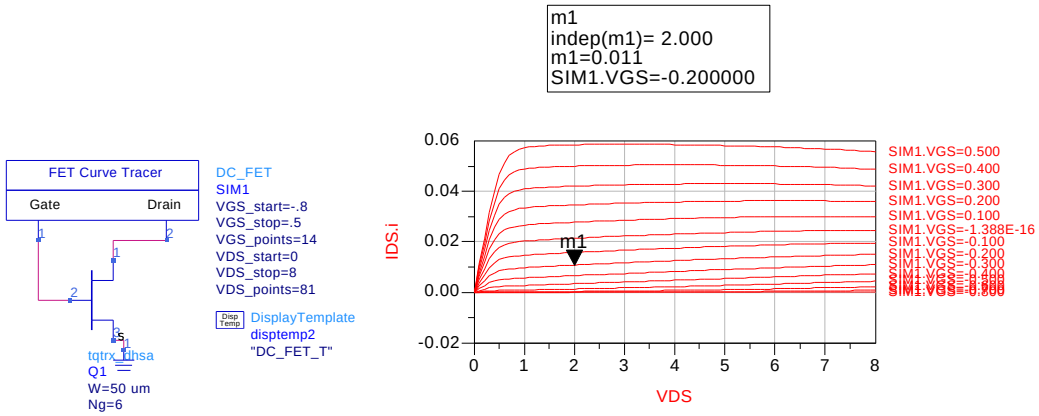


Figure 1. Stage 1 – 300um DFET (6 fingers x 50um wide)

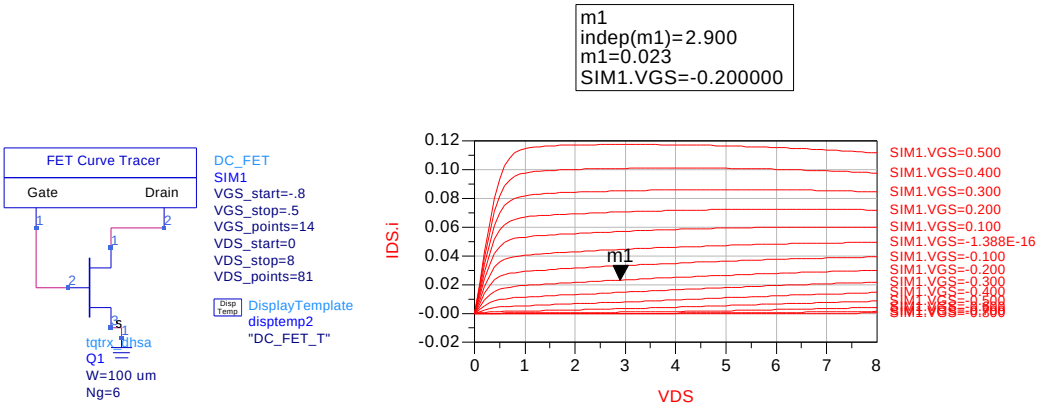


Figure 2. Stage 2 – 600um DFET (6 fingers x 100um wide)

2.2.2. Large Signal DFET RF Simulations

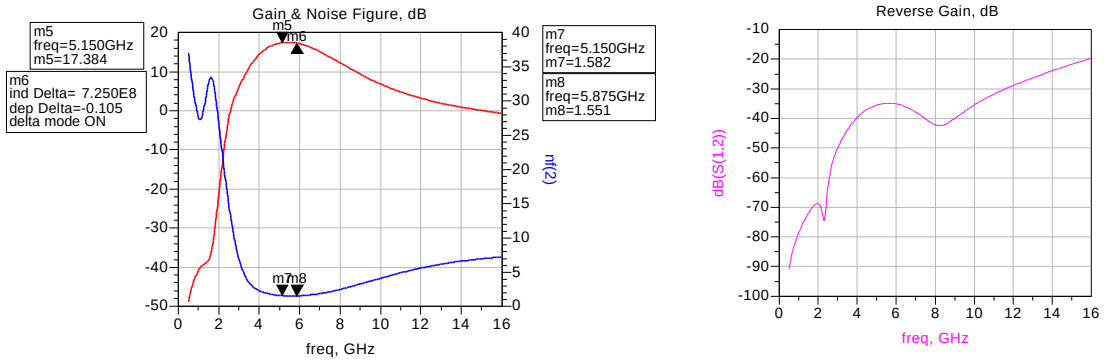


Figure 3. Complete Design – Wideband Gain, NF, and Reverse Gain Response

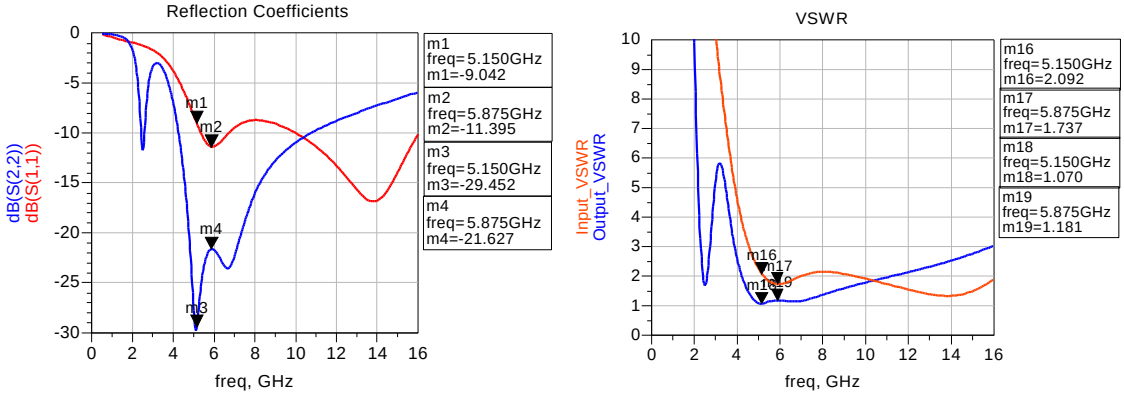


Figure 4. Complete Design – Wideband Match & VSWR Response

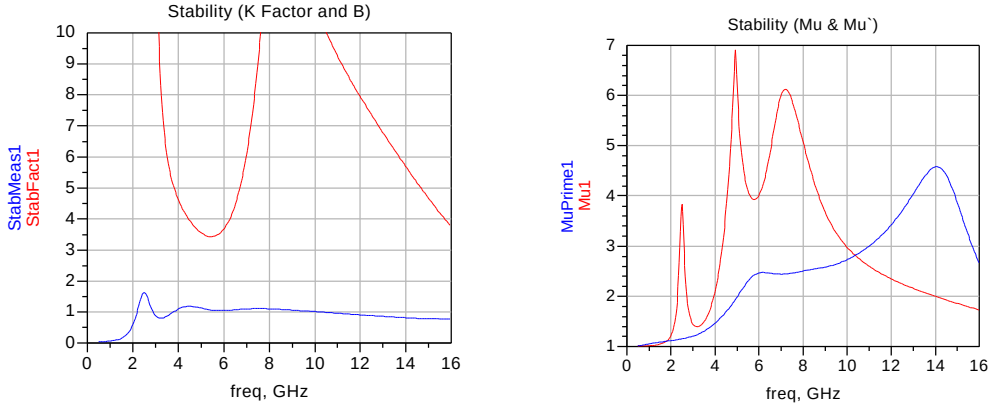


Figure 5. Complete Design – Wideband Stability Response

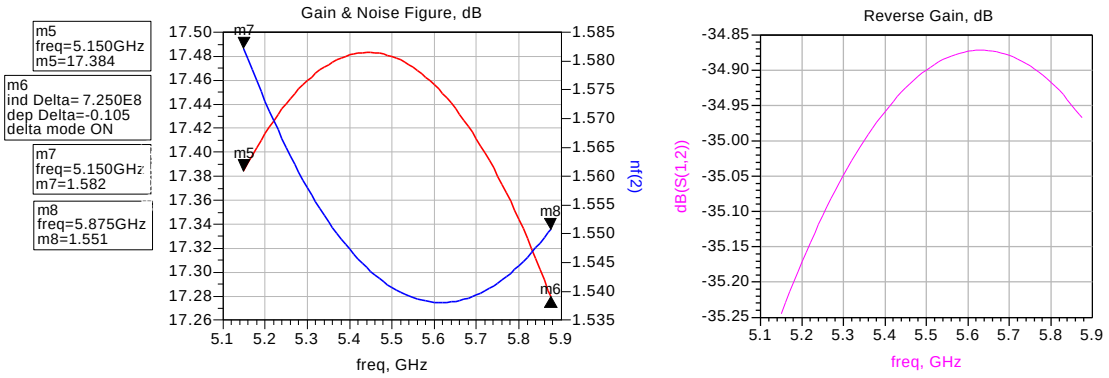


Figure 6. Complete Design – Narrow Band Gain, NF, and Reverse Gain Response

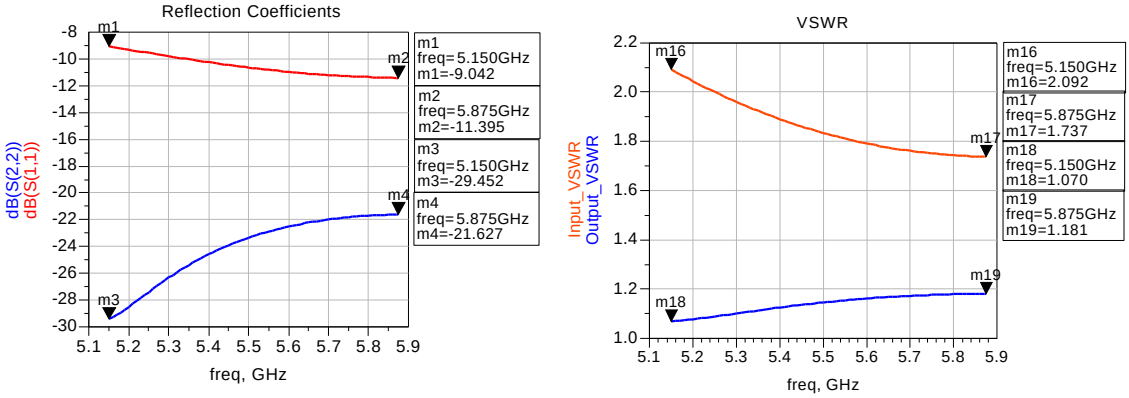


Figure 7. Complete Design – Narrow Band Match & VSWR Response

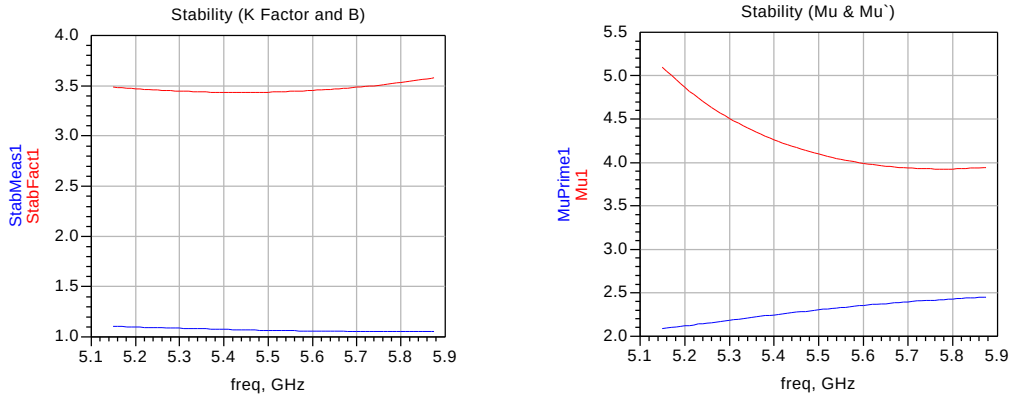


Figure 8. Complete Design – Narrow Band Stability Response

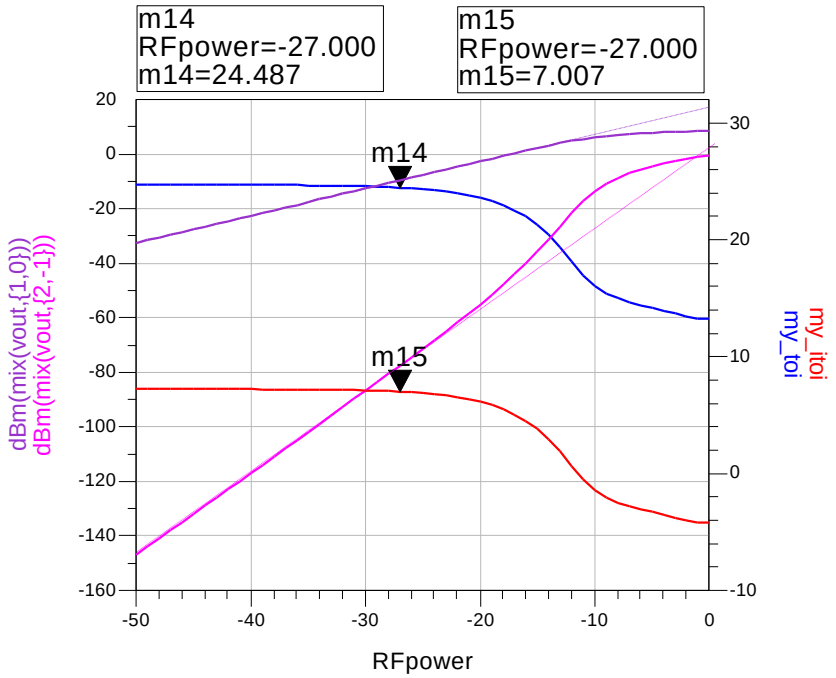


Figure 9. Complete Design – ITOI Response

RFpower	my_toi	my_itoi
-50.000	24.702	7.222
-49.000	24.702	7.222
-48.000	24.702	7.222
-47.000	24.701	7.221
-46.000	24.701	7.221
-45.000	24.700	7.220
-44.000	24.699	7.219
-43.000	24.698	7.218
-42.000	24.696	7.217
-41.000	24.695	7.215
-40.000	24.692	7.213
-39.000	24.690	7.210
-38.000	24.686	7.206
-37.000	24.682	7.202
-36.000	24.676	7.196
-35.000	24.669	7.189
-34.000	24.660	7.180
-33.000	24.649	7.169
-32.000	24.635	7.155
-31.000	24.617	7.137
-30.000	24.595	7.115
-29.000	24.567	7.087
-28.000	24.531	7.052
-27.000	24.487	7.007
-26.000	24.431	6.951
-25.000	24.361	6.881
-24.000	24.272	6.792
-23.000	24.161	6.681
-22.000	24.021	6.541
-21.000	23.845	6.365
-20.000	23.624	6.144
-19.000	23.346	5.866
-18.000	22.996	5.516
-17.000	22.556	5.076
-16.000	22.002	4.523
-15.000	21.305	3.826
-14.000	20.431	2.951
-13.000	19.357	1.877
-12.000	18.130	0.650
-11.000	16.950	-0.529
-10.000	16.050	-1.430

Figure 10. Complete Design – Tabulated ITOI Response, +7dBm @ -27dBm input Power

3. Schematic

3.1. RF Schematic

3.2. Simplified DC Schematic

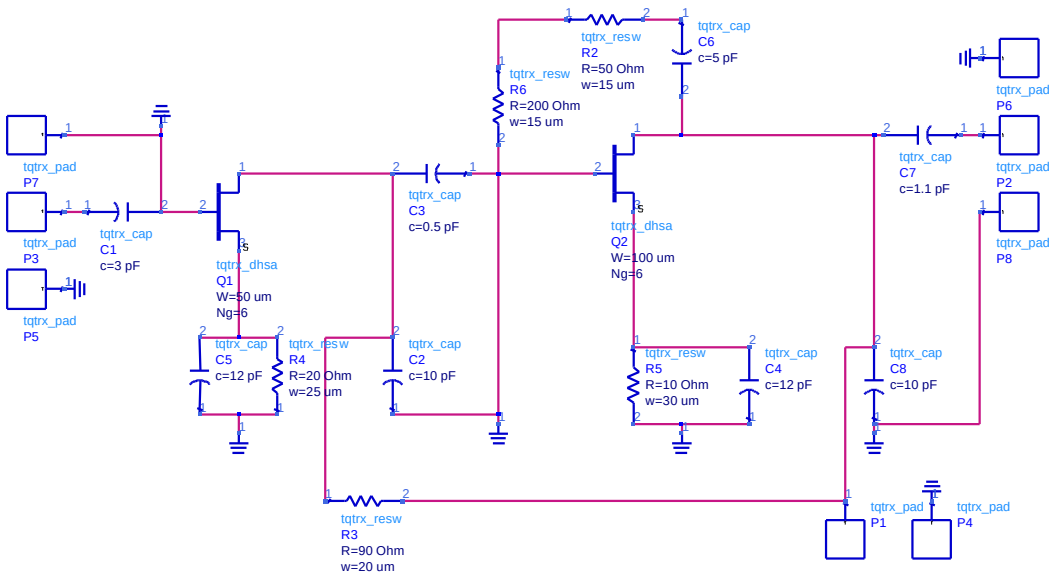


Figure 11. Simplified DC schematic of C-Band LNA

3.3. Bias Check

This C-Band LNA uses a single drain bias to supply voltage to both DFET stages. Table 2 summarizes the biasing scheme for each stage. Figures 1 & 2 show the DC test bench for each DFET stage. The first stage was chosen to operate around 2Vds, however, after implementing the self-bias network, it reduced to 1.85V. Similarly, after the self bias network was added to the second stage, Vds reduced to 2.73.

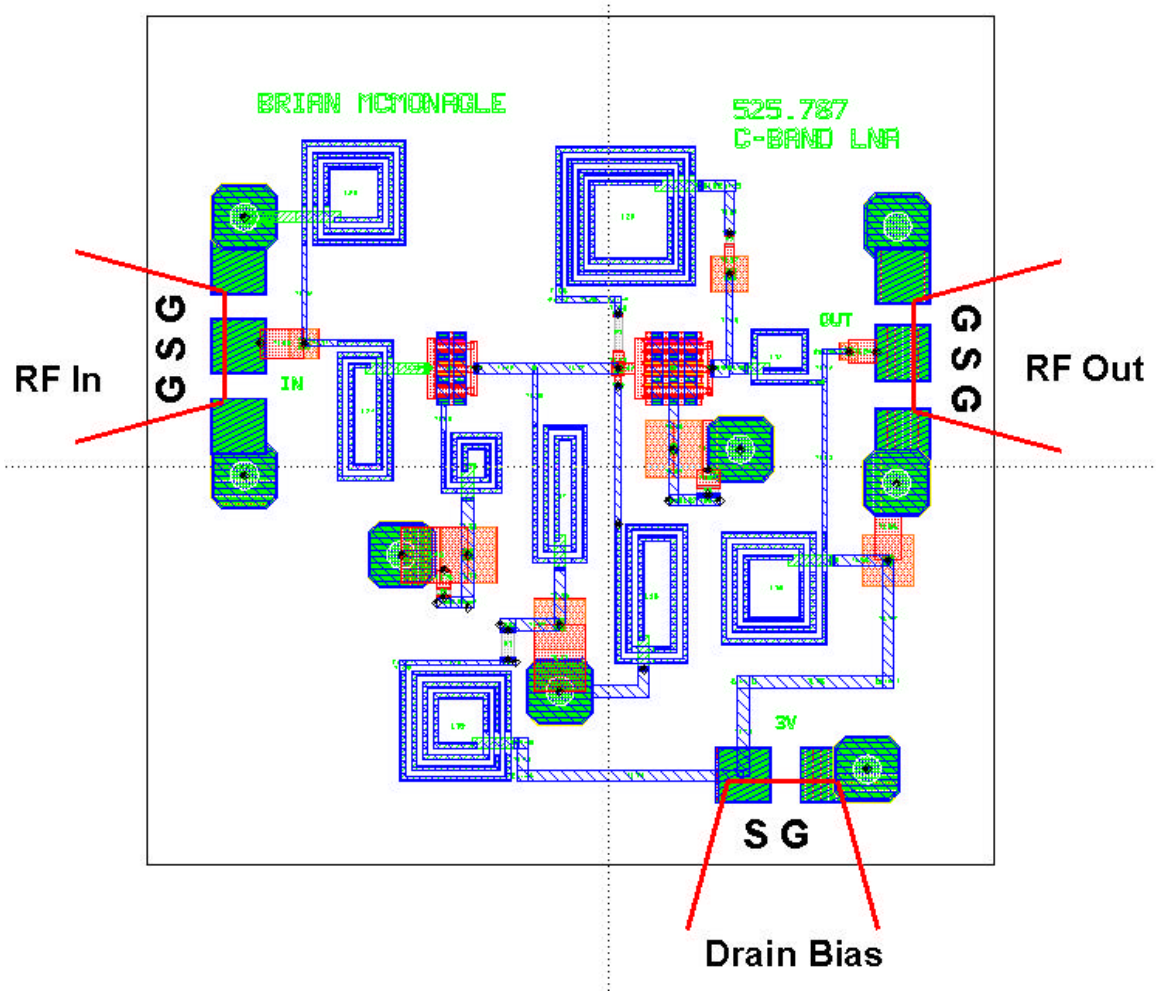
Table 2: Modeled DFET DC Parameters

Stage	Size	Vgs	Vds	Ids
1	300µm	-0.211V	1.85V	10.1mA
2	600µm	-0.215V	2.73V	21.5mA

4. Layout

4.1. Final C-Band LNA Layout

Figure 12. C-Band LNA layout showing bond pad configuration



5. Test Plans

Design verification for the C-Band LNA will involve measuring small signal s-parameters, noise figure, IP3, and DC parameters. The LNA design uses two 125µm pitch GSG probes for both of its RF contacts (East and West sides of the MMIC). The DC supply will make contact from the south side of the MMIC using a common 125µm SG probe.

5.1. Test Equipment

The following test equipment will be needed to fully characterize the LNA design.

- Agilent 8510 Network Analyzer (or comparable 2-port VNA)
- Agilent C-Band Noise Figure Meter with C-Band Noise Diode
- Simple DC Power Supply
- Spectrum Analyzer
- Two (2) Signal Generators
- Agilent Power Meter

5.2. Turn On Procedure

When testing the LNA, care should be taken that the LNA does not get over stressed with drain voltage. Also, to help protect the design from excessive current draw due to possible layout errors or defects, set the current limit of the supply to twice the nominal current pull. Since this LNA is designed to operate at 32mA, the current limit on the DC supply to approximately 65mA. With the LNA correctly probed, as shown in Figure 12, ramp the drain voltage of the DC supply slowly up to the required +3V operating voltage.

5.3. RF Measurements

Calibration needs to perform on all test equipment prior to test. Since the LNA will be probed, the VNA should be calibrated from 1–10GHz, 201 points, using a SOLT calibration standard. The noise figure test set and IP3 test set should also be calibrated. When calibrating the noise figure meter, reducing the amount of connector loss in the system this will increase the accuracy of the noise figure measurement.

5.3.1. S-Parameter Measurements

After calibrating the VNA, connect the RF and DC probes up to the LNA as shown in Figure 12. Following the "*Turn On Procedure*" for the MMIC, record the current draw off the power supply and make S11, S21, S12, and S22 measurements.

5.3.1. Noise Figure Measurements

After calibrating the noise figure test set such that the amount of calibrated loss is minimized, record the NF from 1–10GHz. Make note of the current and gain while recording the data.

5.3.1. IP3 Measurements

After calibrating the IP3 test bench, set the tone frequency separation to 10MHz, i.e. f_1=5.5GHZ, f_2=5.51GHz. This will ensure that the gain at each tone frequency will be exactly equal. Next, set the power levels of the two tones equal to one another. Start with the power levels set to a low level, i.e. –15dBm. Using a spectrum analyzer, increase the power levels of the two tones and look for the third order products to be at least 5 to 10dB above the noise floor. Record the delta between the third order products and the fundament tones – these are the third order intercept (TOI) values. To get the input TOI (ITOI) values subtract off the gain at the fundamental tone frequency. Record these ITOI values at various in-band frequencies.

6. Summary & Conclusion

The design of a C-Band, *0.6mm* MESFET low noise amplifier MMIC was described. The LNA design was simulated using ADS with TriQuint Semiconductor's large signal DFET models. These models produced an LNA with simulated gain greater than 17dB, noise figure less than 1.6dB, and an ITOI of +7dBm. Optimizing and compacting the various matching networks realized the C-Band LNA into a 60x60 mil ANACHIP footprint.

C Band MMIC LNA (Low Noise Amplifier)

Designer: Clarence Weston

Project prepared for Microwave Monolithic Integrated Circuit

(MMIC) Design

Fall 2004 Class

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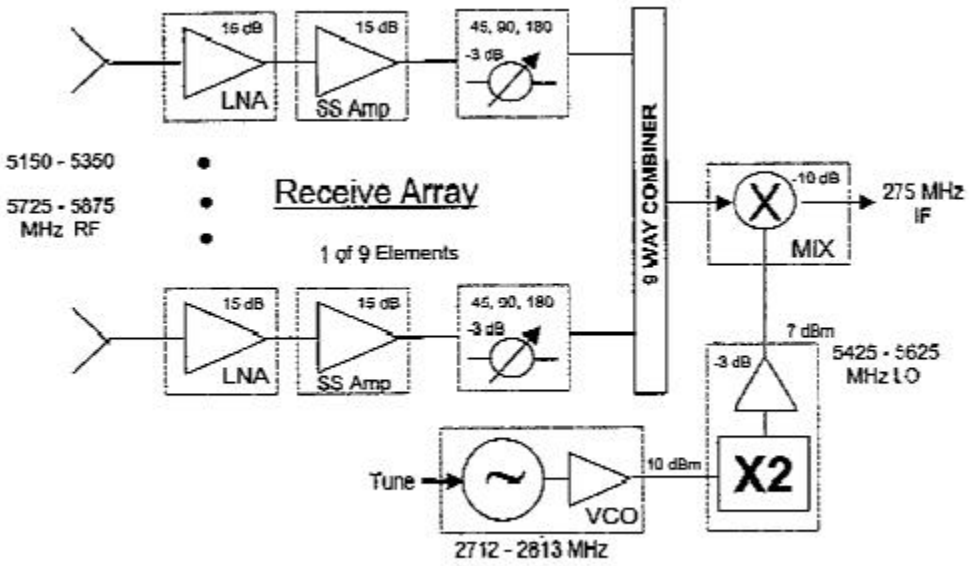
Introduction

Low Noise Amplifiers (LNAs) are very important part of the receive chain in a microwave system. It is essential that a signal be amplified early in the receive chain while adding as little noise as possible because any noise injected by these components in a system is amplified by later stages along with the desired signal.

For this application, the C-Band Low Noise Amplifier will be the first device in the receive chain for the 2004 MMIC class design at The Johns Hopkins University. The project is a duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial scientific, and medical (ISM) frequencies. This LNA will be one of nine MMIC designs that make up the S Band Transceiver.

System Block Diagram: *Figure 1.1*



LNA Design Specifications

Frequency:	5150 to 5875
Bandwidth:	>800 MHz
Gain:	>15 dB
Gain Ripple:	± 0.5 dB goal
Noise Figure:	<4dB; 3dB goal
VSWR, 50 ohm:	<1.5:1
INPUT IP3:	>+5 dBm
Supply Voltage	±5 Volts; 5 Volts only, goal
Size:	60 x 60 ANACHIP

Methodology of LNA Design:

Upon beginning this design, the gain and noise figure specifications were sought after first and then compromises were made to adjust the design accordingly to meet the other design specs. This LNA was designed to be a two-stage amplifier. Although it is possible to get substantial gain out of one stage of amplification, a one stage FET amplifier would probably have stability problems and be very hard to meet the VSWR spec because of the attenuation required to match the input and output. After being able to achieve the lowest noise figure attainable with considerable RF gain, another stage of amplification was added and tradeoffs were made to match the input and output of the circuit with the assumption that changes to S22 will not significantly affect S11.

Design tradeoffs:

Since there is always an emphasis on noise figure (NF) in a LNA design, it was preferred not to use any resistors in the first matching network of the design. Practical design techniques also make it less desirable to use large noisy inductors at the front end of an LNA, and therefore only one series inductor and a shunt capacitor were used to match the input of the FET. The result of that was a respectably low noise figure but a narrow bandwidth match at the input.

Another tradeoff with the LNA design was the gain roll off point vs. the VSWR of the design. It is very possible to have the gain roll off for the LNA to happen further away from the desired operating frequency of the design, however in doing that, the narrow band input match of the circuit moves in the opposite direction. Unfortunately the input matching network forms a low pass filter at the input of the circuit and the performance at the output directly correspond to the IMN.

Circuit Performance:

Gain

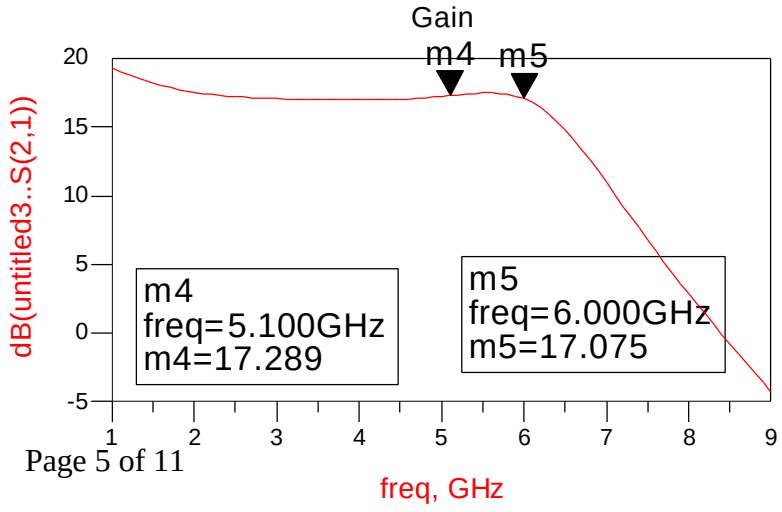


Figure 5.1

Noise Figure:

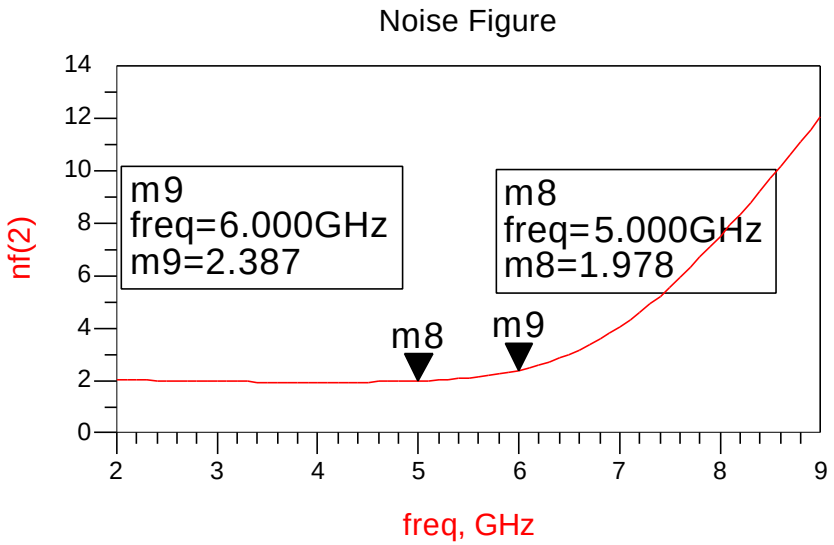


Figure 5.2

Input/Output Match

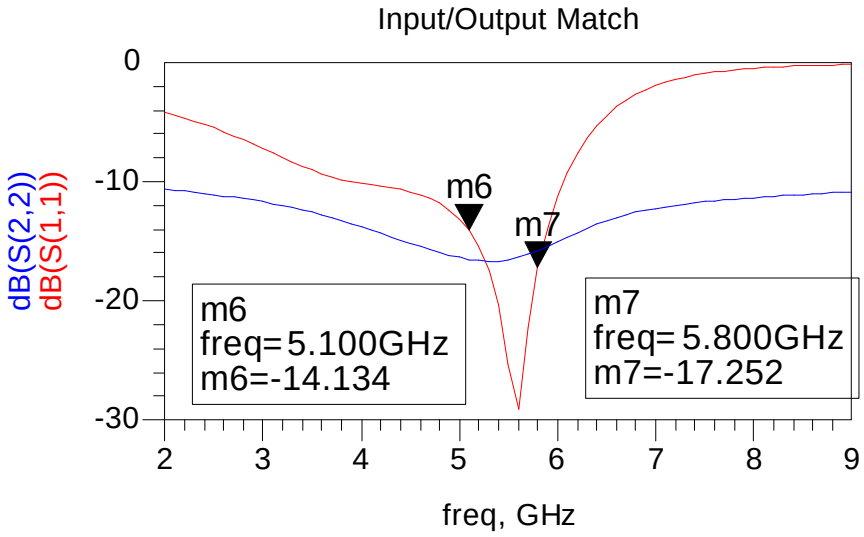


Figure 5.3

IP3

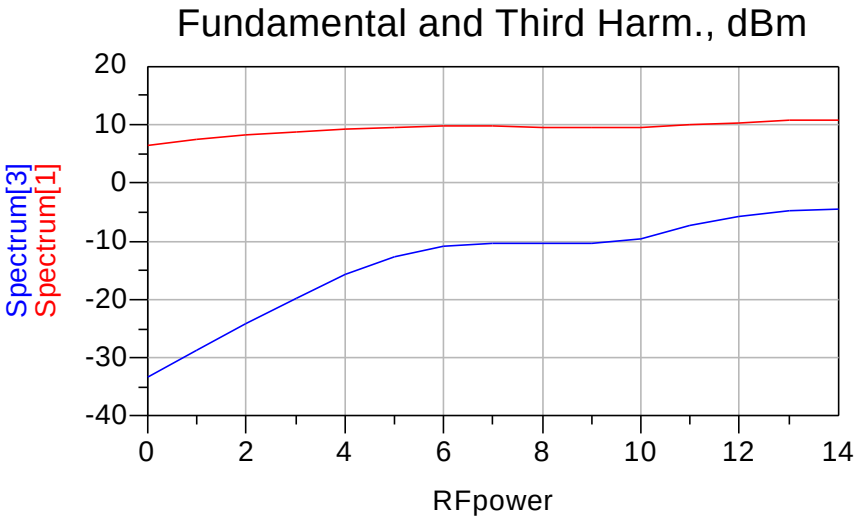


Figure 5.4

Design Specifications Vs Circuit Performance

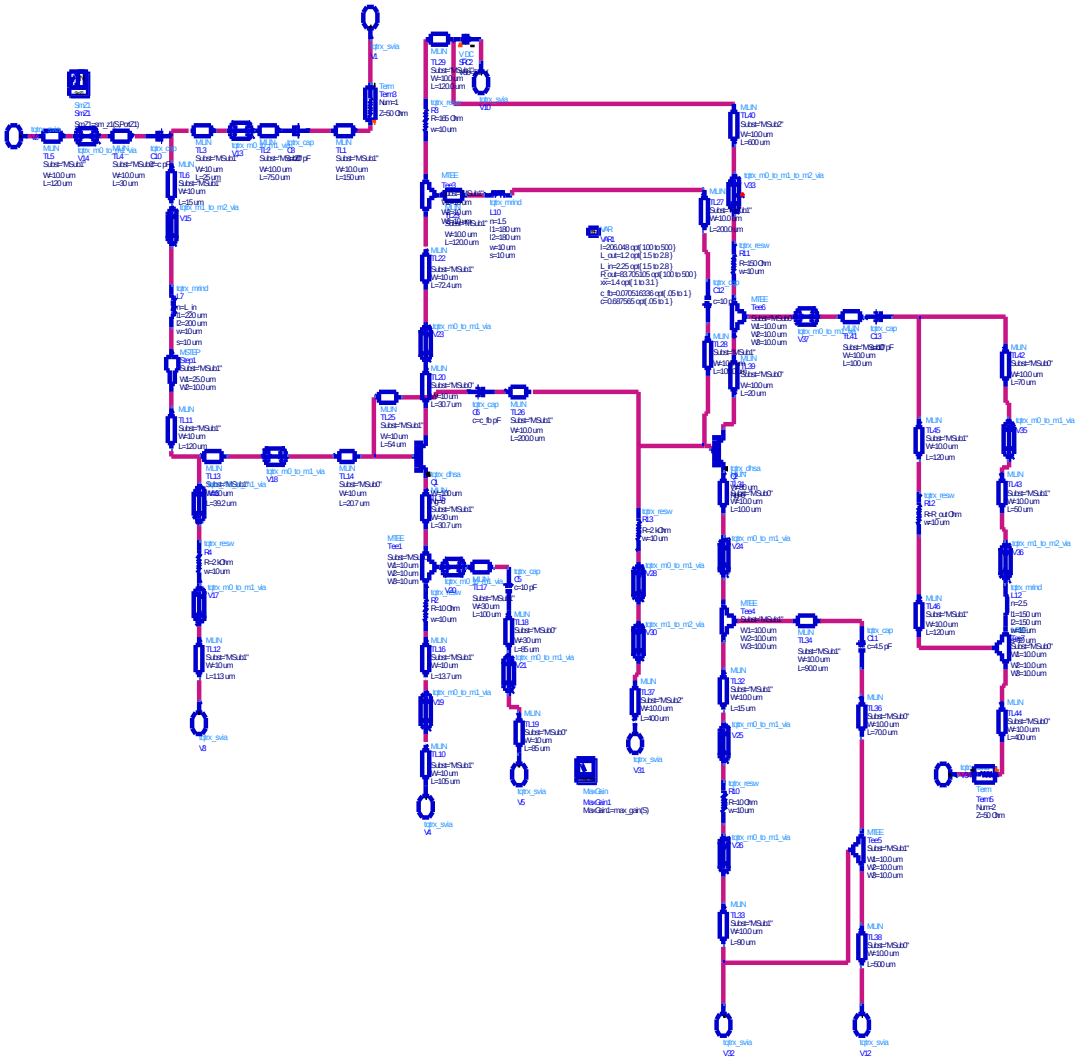
	Design Specifications	Simulated Performance
Frequency:	5150 to 5875	5150 to 5875
Bandwidth:	>800 MHz	>800 MHz
Gain:	>15 dB	>17 dB
Gain Ripple:	+-0.5 dB	>0.5 dB
Noise Figure:	<4dB; 3dB goal	<2.3dB
VSWR, 50 ohm:	<1.5:1	<1.5:1
INPUT IP3:	>+5 dBm	>+15 dBm
Supply Voltage	+-5 Volts; +5V Goal	+5
Size:	60 x 60 ANACHIP	60 x 60 ANACHIP

Drawbacks of LNA Design:

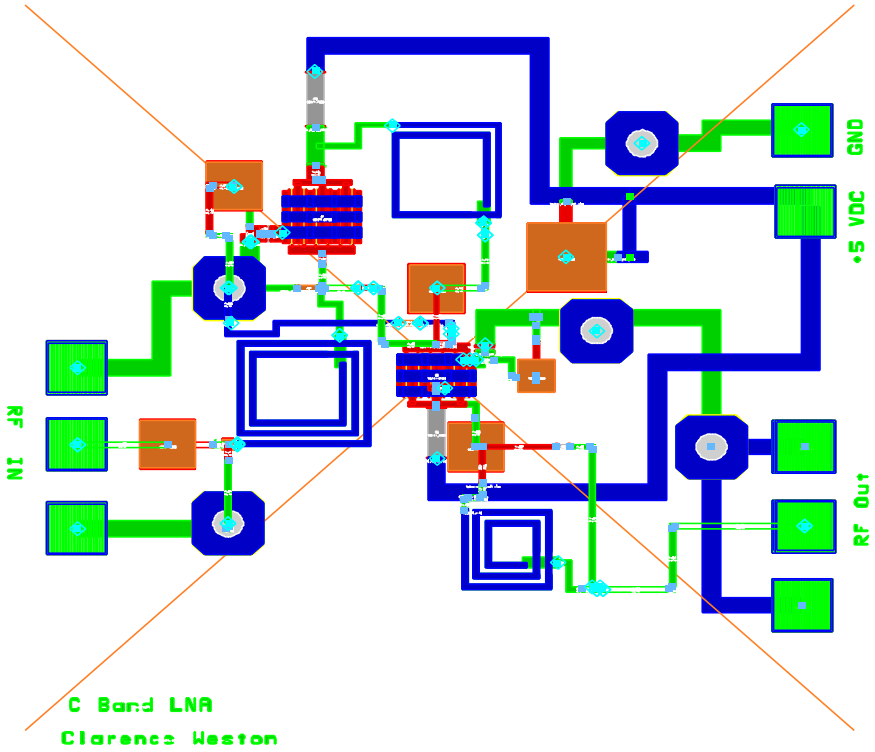
This Low Noise Amplifier (LNA) design shows a low tolerance for component variations especially at the input side of the amplifier. The lowpass type input matching network yields a practically flat gain response form 2 to 6 GHz, however the gain rolloff is very steep thereafter. The noise figure data also follows that trend, worsening continually shortly after the design frequency.

The flat gain response is helped to be achieved through the use of a small feedback capacitor from the input of the first FET to the input of the second stage. This capacitor helps with stability issues, tunes the high frequency rolloff point but unfortunately is also very sensitive go value tolerances. Also, because only two components were used to match the input side of the LNA, the IMN is very narrow band, that just covers the design bandwidth and without precise fabrication, it is very possible to miss the design frequency and end up with a relatively large mismatch at the front end.

Schematic:



LNA Layout:



Design Summary/Conclusion:

The specifications for this LNA design were challenging but achievable. There were many tradeoffs in the consideration for this design. Two of the more desirable features of this LNA is the flat gain response and broad band output match form 2 to 6GHz makes this design a very portable one in the since that an off chip tunable inductance at the input can have this amplifier operate over and 1GHz band of that 4GHz bandwidth.

Test Equipment

- 5 Volt DC Power supply
- Noise Figure Meter
- Agilent 8510 Vector Network Analyzer

Test Procedure

Turn On Procedure:

Connect the DC power supply to the DC pads on the MMIC. Slowly increase the voltage from 0 to 5 volts. (The amplifier should be drawing about 45mA.)

S-Parameter Measurement:

Calibrate the Network Analyzer from 1 to 10 GHz.

Position the input probes on the ‘RF IN’ GSG pad on the chip.

Position the output probes on the ‘RF OUT’ GSG pads on the chip.

Make all S-Data measurements and save them to a disk.

Noise Figure Measurements:

Calibrate the noise figure meter from 1 to 10 GHz.

Position the input probes on the ‘RF IN’ GSG pad on the chip.

Position the output probes on the ‘RF OUT’ GSG pads on the chip.

Make all S-Data measurements and save them to a disk.

C-Band Up/Down Converter Design Report
EE 787: MMIC Design

Jason Abrahamson

Abstract

This design report presents a C-Band up/down-converter implemented in monolithic microwave integrated circuit (MMIC) technology for a TriQuint fabrication process. The converter is based on a 180° hybrid scheme, which allows for both up and down conversion, utilizing diode-connected transistors for frequency mixing. The mixer was designed for RF frequencies of 5150-5875MHz, LO frequencies of 5425-5625MHz and an IF of 275MHz. Design simulations demonstrated LO/RF isolation >30dB, conversion loss <10dB and VSWR <2.5:1. A MMIC layout of the final design was performed within the 60x60mil ANACHIP die for a system supply voltage of 5V.

1. Introduction

An up/down converter for operation in C-band was designed using lumped elements in MMIC technology. A single mixer built on a 180° hybrid and diode-connected DFET transistors was implemented since it permits both up and down conversion in one circuit. The circuit function is to convert RF signal at 5150-5875MHz to an IF of 275MHz and vice versa. A local oscillator (LO) between 5425-5625MHz driven at 3dBm is used to achieve mixing. Conversion loss ranges from 8.6dB to 9.5dB. VSWR across the band varied from 1.3 to 2.2. The circuit was designed to be integrated into a transceiver system and thus is biased via the common supply voltage, 5V. An external blocking capacitor, 1uF typical, is required at the IF port.

1.2 Design Philosophy

The design approach was dictated by the circuit performance specifications, which in this case call for a general purpose mixer that performs both up and down conversion. Thus in selecting an architecture to implement the up/down converter, priority was given to schemes which provided greater general mixing functionality, with a footprint that could be sized to a 60x60mil die, rather than tightly focused optimization of specific signal characteristics. All circuit components were implemented by lumped elements.

1.2.1 Circuit Description

The balanced 180° hybrid mixer architecture was selected based on the following generalized properties: 1) small footprint attributed to up/down conversion ability in a single circuit, 2) excellent LO/RF isolation, 3) fair RF VSWR, and 4) good conversion loss. The 4-port architecture is concise in nature, with two mixing diodes occupying symmetrically opposite ports, a single port dedicated to both RF and IF signals, and the remaining port supplying the LO drive signal. Figure 1 is an illustrative outline of a balanced mixer architecture.

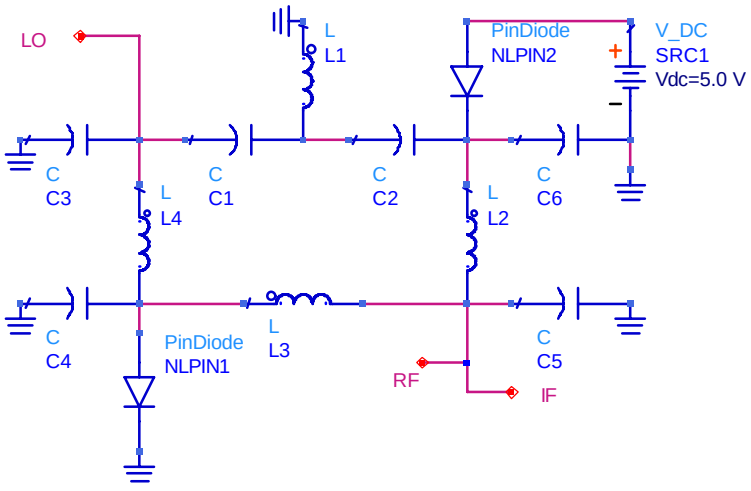


Figure 1. Illustration of a balanced 180° hybrid architecture.

1.3 Design Procedure

1.3.1 180° Hybrid Design

The principle and performance determining circuit component of the architecture is the 180° hybrid. This was designed first and optimized for equal power split and proper phase for both the LO and RF ports. Optimal power split and proper phase ensured high LO/RF isolation, minimized losses and reduced port mismatch. The hybrid consists of four 0.4pF capacitors, two 0.8pF capacitors, and four 2nH inductors.

1.3.2 Mixing Diode Design

TriQuint DFET transistors were connected in a diode configuration to provide the mixing action of the up/down converter. The transistors were then sized to match 50O at bias conditions, approximately 1.3V and 700uA, as practicality allowed. Matching the transistors to 50O minimized the circuit mismatch and consequently the VSWR. The final transistor dimensions were W=20um, N=2.

1.3.3 Bias Network Design

A common transceiver system supply voltage of 5V is expected, thus a biasing network was design to deliver the 1.3V needed to bias the mixing diodes. A simple resistive voltage divider provided the proper bias. A shunt power supply stabilizing capacitor was added that also acted as an RF short. A series spiral inductor provided RF isolation for the power supply. DC blocking capacitors of 1pF were added on the RF and LO ports. The blocking capacitor for the IF line must be very large to minimize signal attenuation and therefore is not practical for layout within the constraints of the ANACHIP die size. This must be added off chip on the IF output for proper biasing. The simulated off chip blocking capacitance was 1uF. Final estimated DC power consumption was 3.5mW.

1.3.4 RF/IF Isolation Network Design

The IF and RF input/output signals are connected to the 180° hybrid at the same port, thus in order to prevent the RF or IF signals from being shunted out each others' ports, isolation components were necessary. The IF port required the addition of a large inductor acting as an RF choke. The DC blocking capacitors on the RF and LO ports were sufficiently small to provide isolation from the IF signal.

1.3.5 Substrate and Packaging Considerations

Non-ideal circuit connections to ground and signal were simulated by adding components to act as bond pads, bond wires and vias. On chip ground connections were implemented with TriQuint substrate vias. Triquint bond pads were placed to simulate die connection and packaging parasitics such as bond wires were implemented as 300pH inductors. Although the circuit will be tested on a probe station, simulation as a packaged circuit was considered more insightful towards final product development.

1.3.6 Mixer optimization

Tuning consisted mostly of optimizing the DC blocking capacitors and RF isolation components to minimize signal loss and maximize RF/LO and RF/IF isolation.

1.3.7 Trade Offs

The major tradeoff in designing the up/down converter was performance over functionality. Obtaining low conversion loss or possibly conversion gain may have been possible if the converter had been implemented as either an up-converter or down-converter with mixing FETs. However, the ability to mix both up and down in frequency was prioritized since the specification called only for a maximum conversion loss. Additionally, given the die size constraints, more extravagant designs that provided either better match or conversion loss than the balanced 180° hybrid were not possibilities. Overall the choice of architecture was a good compromise as all design specifications were achieved.

2.0 Performance Simulations

2.1 Summary of Simulation Results

Table 1. Summary of specifications, design goals and simulation results.

Requirement	Specification	Goal	Simulation*
RF Frequency	5150-5875 MHz	5150-5875 MHz	5150-5875 MHz
LO Frequency	5425-5625 MHz	5425-5625 MHz	5425-5625 MHz
IF Frequency	275 MHz	275 MHz	275 MHz
Isolation	> 10 dB	16 dB	> 30 dB
Conversion Loss	<10 dB	7 dB	< 9.6 dB
LO Power	< 7 dBm	0 dBm	3 dBm
VSWR	< 2.5:1	1.5:1	< 2.2:1
Supply Voltage	0-5V	5V	5V
Size	60milx60mil	60milx60mil	60milx60mil

*All values indicate worse simulated result over range of operation.

2.2 Hybrid RF/LO Power Division

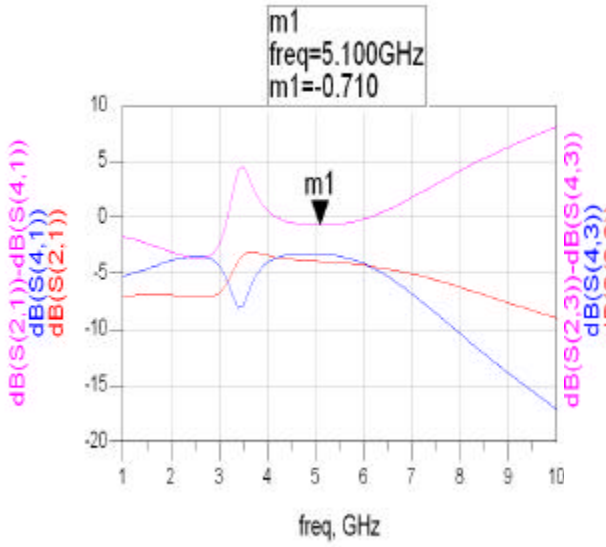


Figure 2. LO power split at mixing ports.

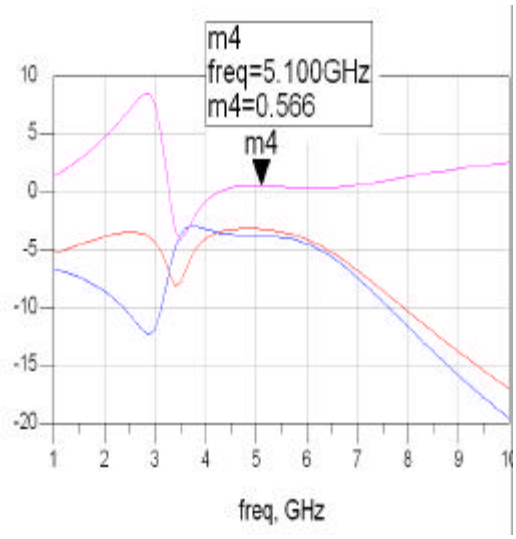


Figure 3. RF power split at mixing ports.

2.3 Mixer RF/LO Isolation and VSWR

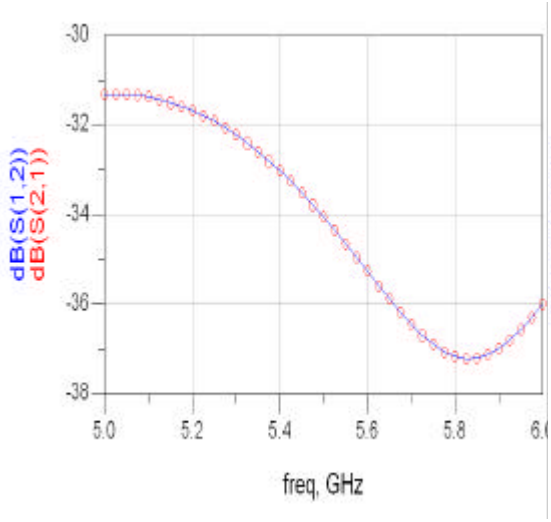


Figure 4. LO/RF isolation.

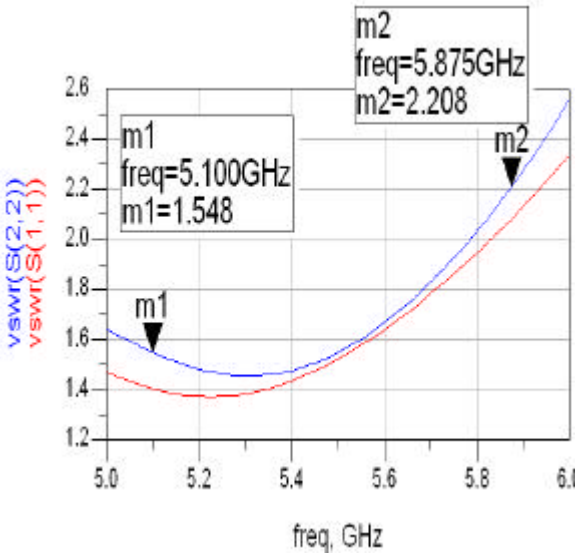
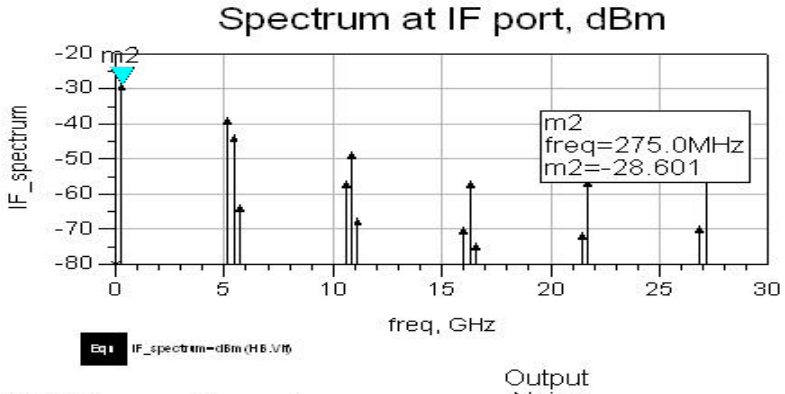


Figure 5. VSWR at LO/RF ports.

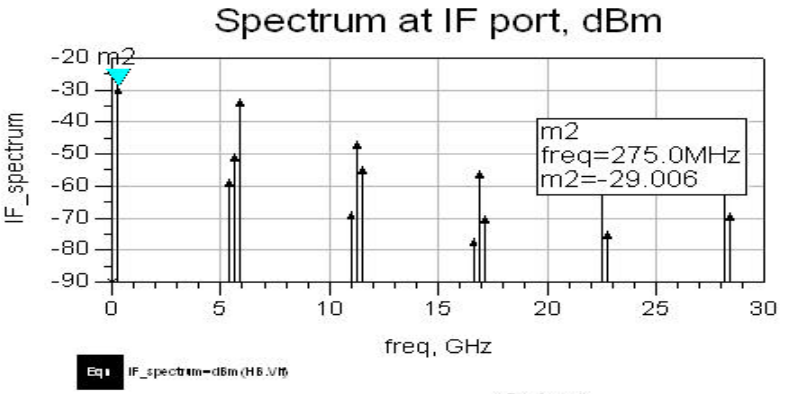
2.4 Mixer Conversion Gain



Output Frequency	Conversion Gain, dB
275.0MHz	-8.601

Output Noise Frequency	Noise Figures, dB	
noisefreq	NFdsb	NFssb
5.150E15...	107.372	107.372

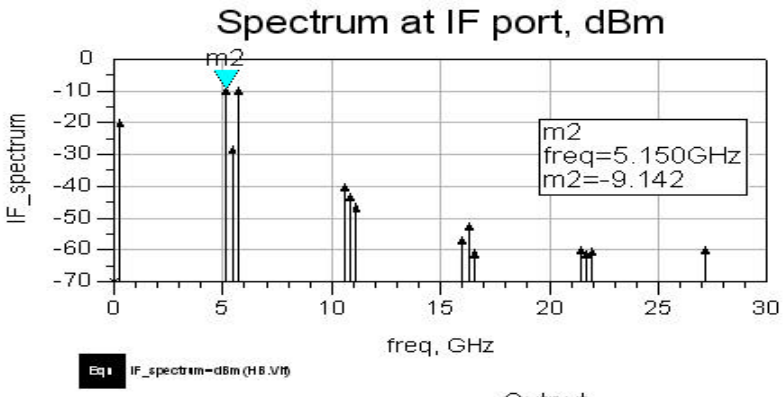
Figure 6. Conversion gain for low band down converter operation, RF=5150MHz, LO=5425MHz.



Output Frequency	Conversion Gain, dB
275.0MHz	-9.006

Output Noise Frequency	Noise Figures, dB	
noisefreq	NFdsb	NFssb
5.625E15...	108.138	108.138

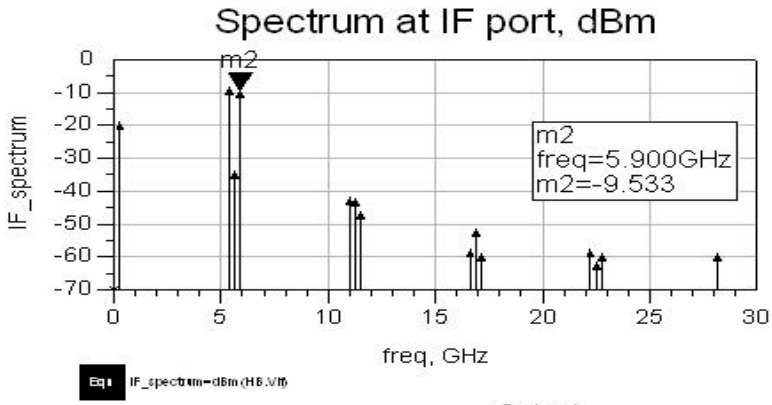
Figure 7. Conversion gain for high band down converter operation, RF=5875MHz, LO=5600MHz.



Output Frequency	Conversion Gain, dB
5.150GHz	-9.142

Output Noise Frequency	Noise Figures, dB	
noisefreq	NFdsb	NFssb
5.150GHz	8.137	8.816

Figure 8. Conversion gain for low band up converter operation, RF=5150MHz, LO=5425MHz, IF=275MHz.



Output Frequency	Conversion Gain, dB
5.900GHz	-9.533

Output Noise Frequency	Noise Figures, dB	
noisefreq	NFdsb	NFssb
5.900GHz	7.192	9.078

Figure 9. Conversion gain for low band up converter operation, RF=5900MHz, LO=5625MHz, IF=275MHz.

3.0 Schematics

3.1 RF Circuit Schematic

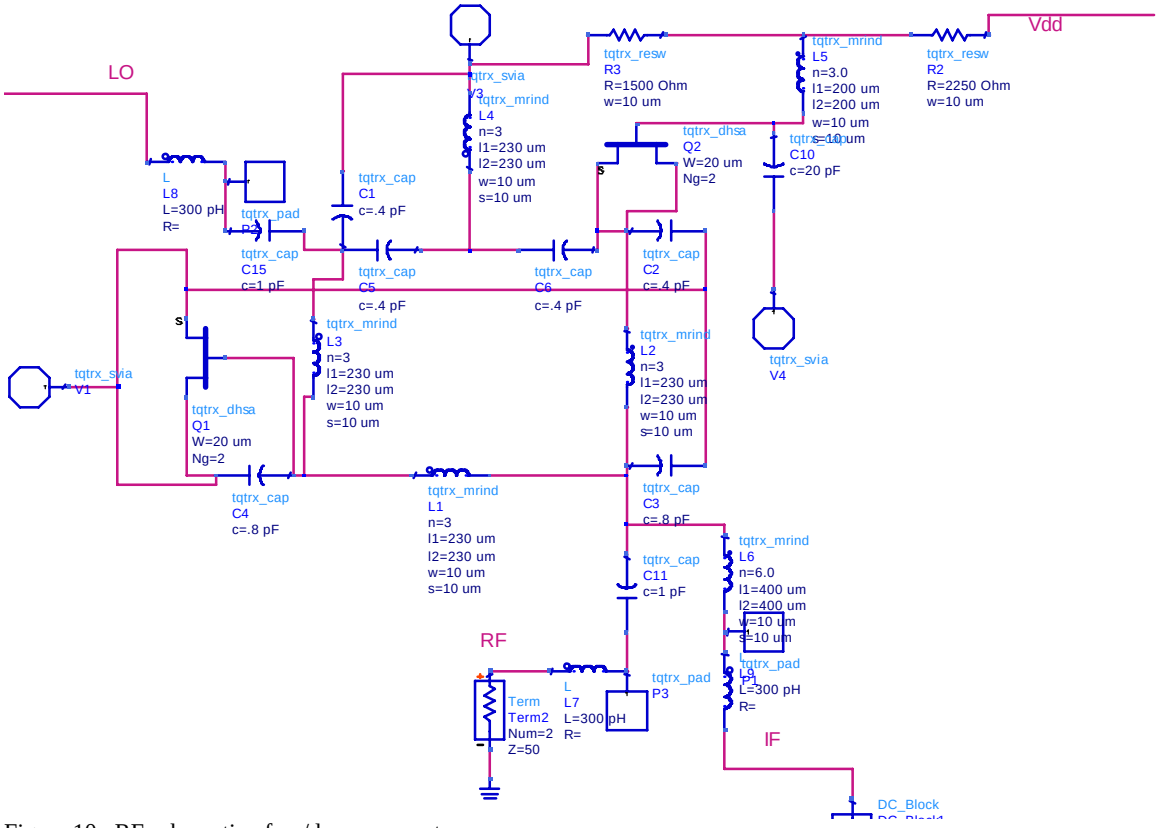


Figure 10. RF schematic of up/down converter.

3.2 DC Equivalent Schematic

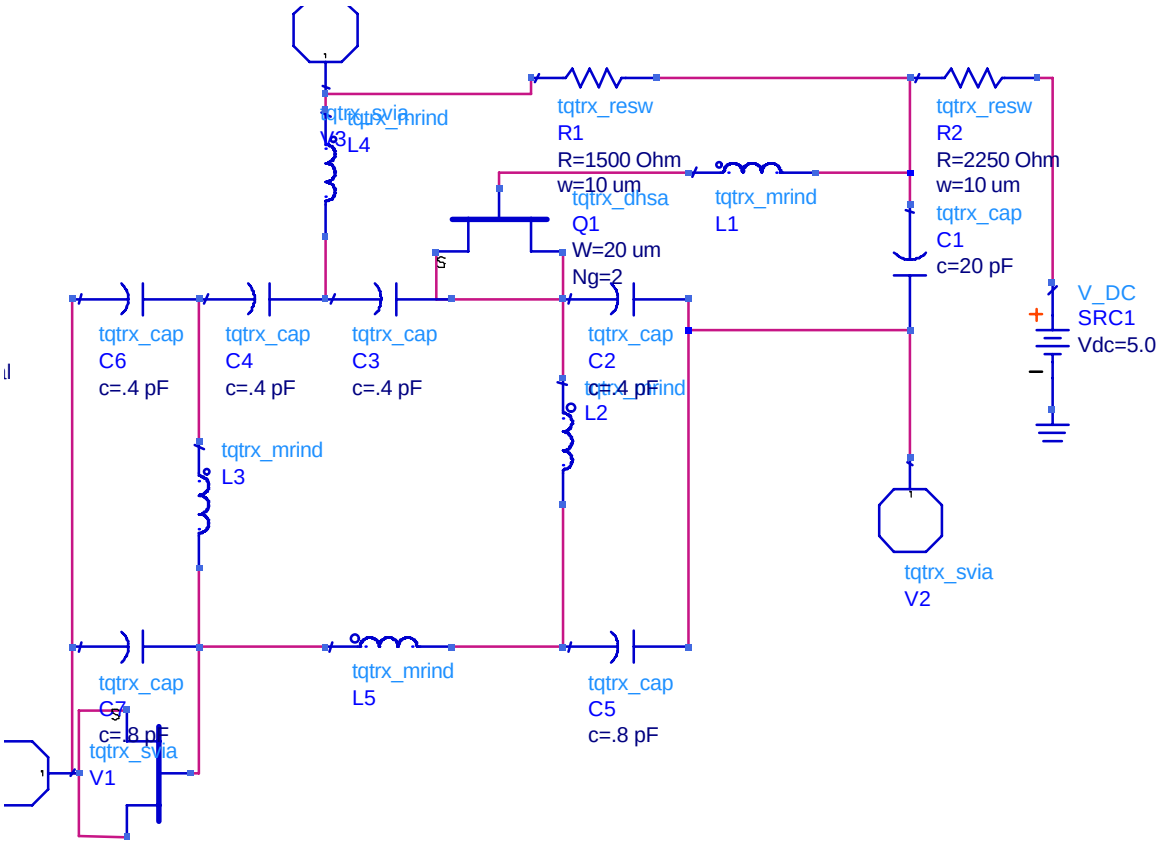


Figure 11. DC equivalent circuit for the converter.

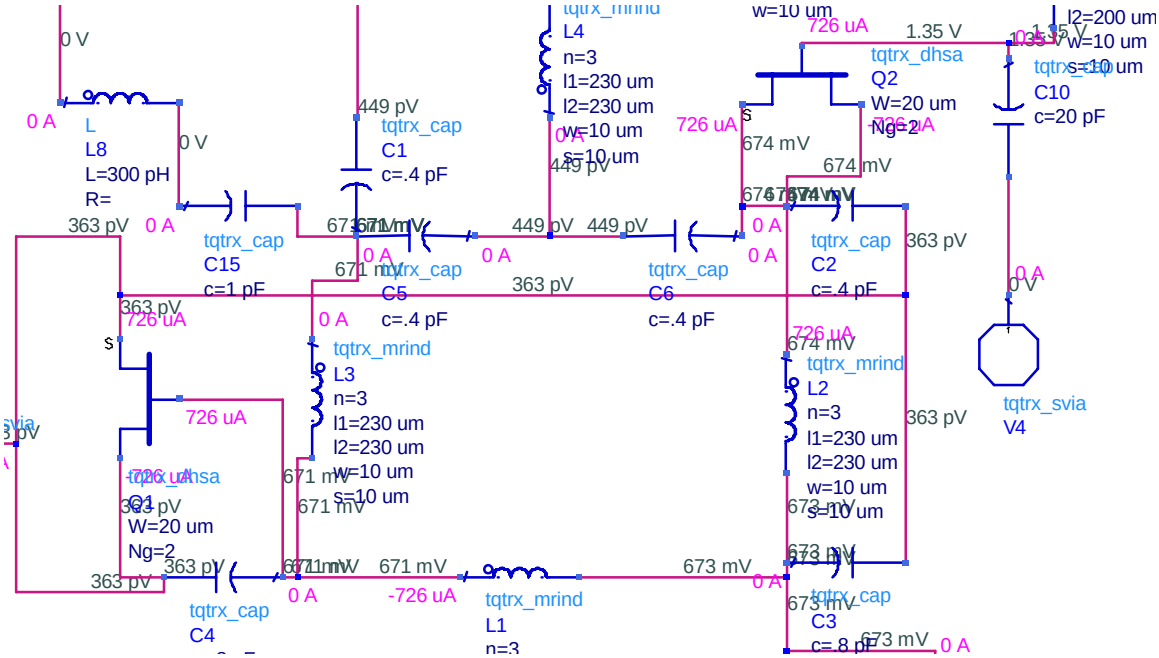


Figure 12. DC bias solution for the converter.

4.0 Circuit Layout

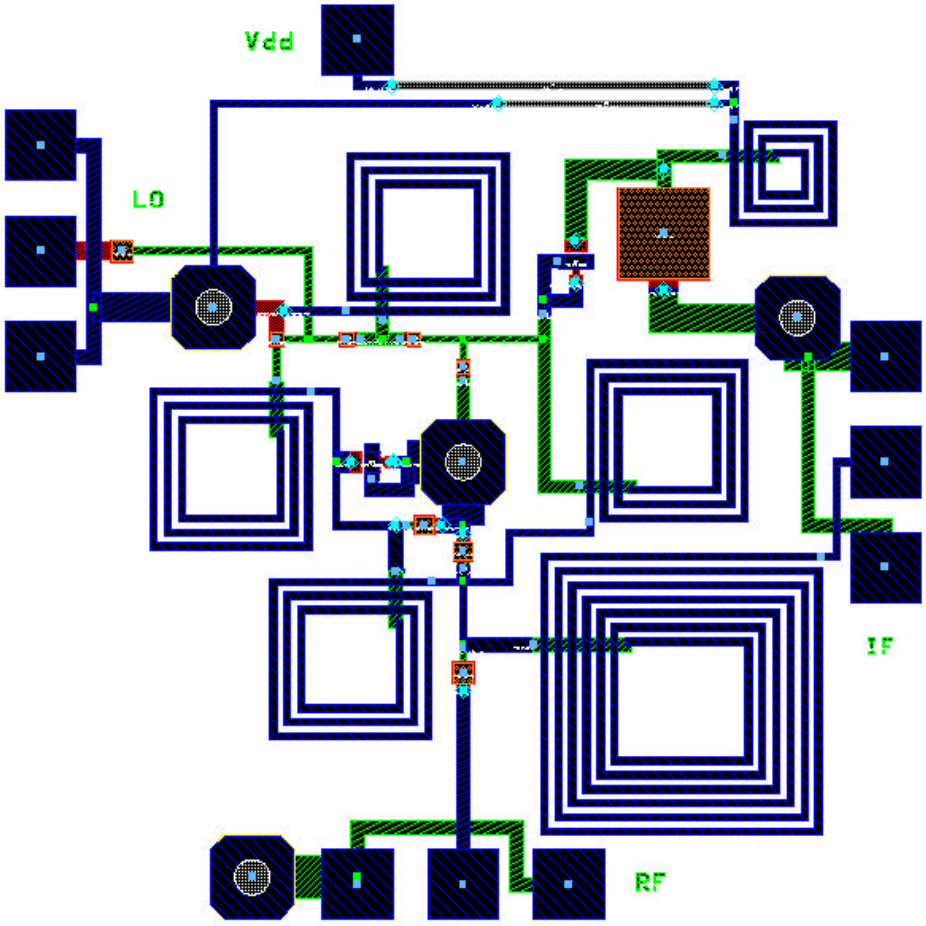


Figure 13. C-Band Up/Down converter layout.

5.0 Test Plan

For all test setups a blocking capacitor is required at the IF input to properly bias the circuit. Typical value >1uF.

5.1 Down Converter Configuration

- Set up according to Figure 14.
- Sweep LO frequency 5425-5625MHz
- Sweep RF frequency 5150-5878MHz
- Measure 275MHz IF power at spectrum analyzer.

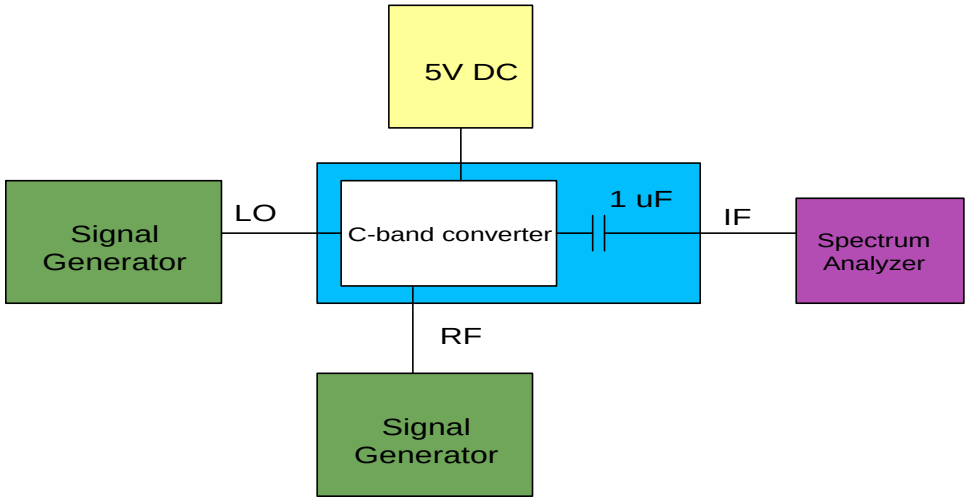


Figure 14. Test configuration for down converter conversion loss.

5.2 Up converter configuration

- Set up according to Figure 15.
- Sweep LO frequency 5425-5625MHz, maintain 275MHz IF
- Measure RF power at spectrum analyzer.

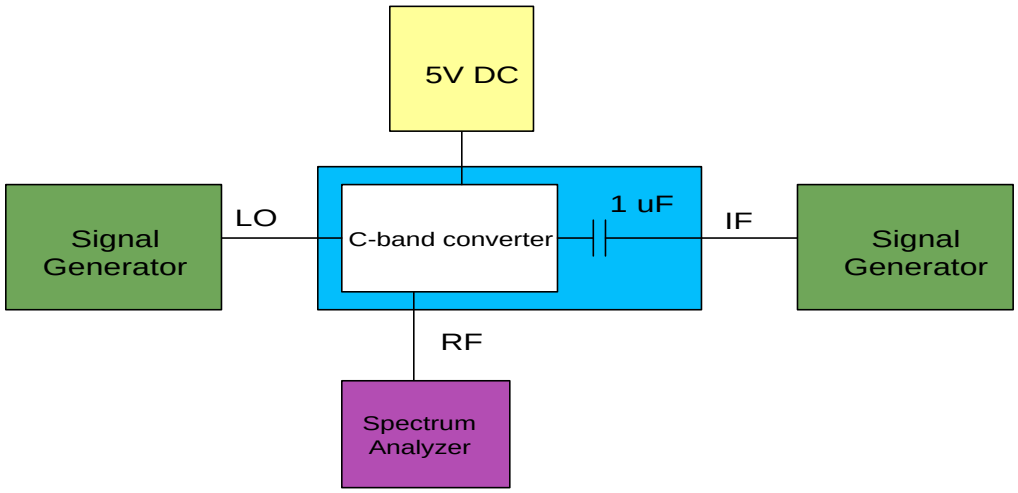


Figure 15. Test configuration for up converter conversion loss.

5.3 S-Parameter Measurement Setup

- Setup according to Figure 16.
- Sweep network analyzer over 5150-5875MHz
- Measure isolation and match at LO, RF ports.

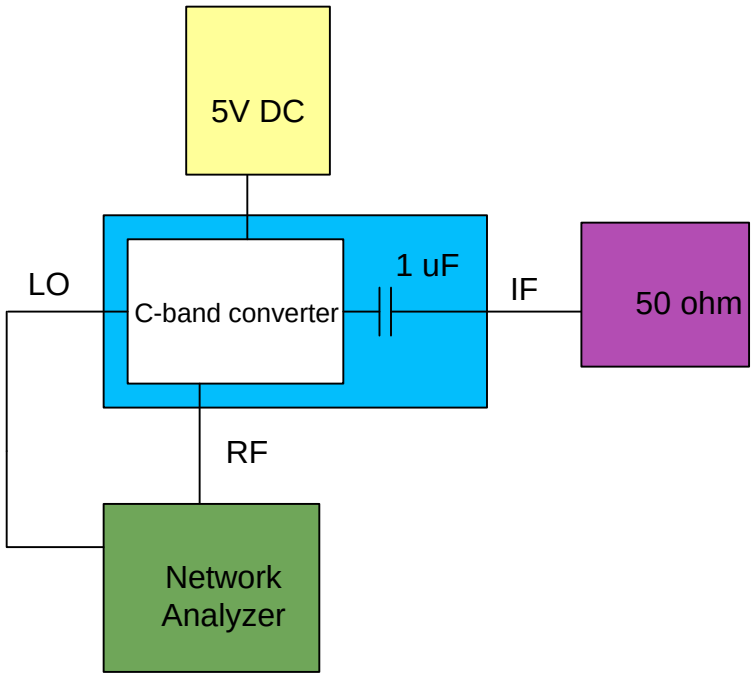


Figure 17. Measurement setup for LO/RF isolation and match.

6.0 Summary & Conclusions

A C-Band up/down converter for operation between 5150-5875MHz was designed and met all specifications. The balanced 180° hybrid architecture provided a good compromise between performance and functionality, providing excellent RF/LO isolation, fair VSWR, and good conversion loss for reasonably low LO drive. Additional filtering at all signal inputs/outputs could be added to reduce IF/RF feed-through as RF/IF signal level difference was in some cases as little as 3dB.

2 Bit Phase Shifter

Henry Weiss
EE787
Johns Hopkins University

December 13, 2004

Abstract

This report describes the design and simulated performance of a 2-Bit Phase Shifter which will be fabricated as a GaAs Monolithic Microwave Integrated Circuit (MMIC). This 2-Bit Phase Shifter is part of larger class project to implement a duplex transceiver for C-band HiperLAN wireless local area network for the industrial scientific and medical (ISM) frequencies. The design process was conducted with Microwave Office version 6.03 from Applied Wave Research using TriQuint semiconductor elements to fabricate capacitors, inductors, resistor, and FETs on a GaAs substrate.

Introduction - Phase Shifter

The 2-bit phase shifter is constructed as a two stage series phase shifter. The first stage switches between +45 and –45 degrees. The second stage switches between +90 and –90 degrees. There is a total swing of phase between –135 and +135 degrees in 4 steps of 45 degrees.

Each stage is controlled by a single control voltage or "bit" which applies complementary voltages to two pair of FET gates. When one voltage is "on" or 0 volts and the other is "off" or –5 volts. This process routes the RF signal through either a phase lead or phase lag network in each stage.

The design met the following specifications for 2 bits with control voltage of 0 /-5 volts. The return loss (S11) was less than –10dB.

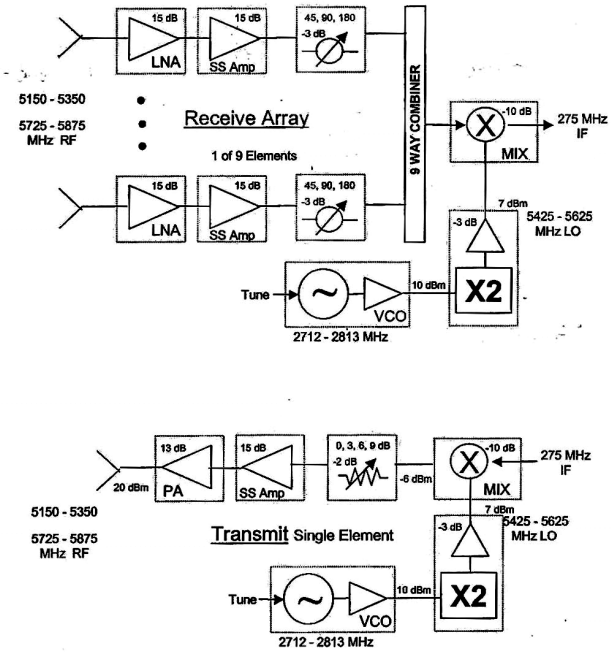
SPECIFICATIONS FOR 3 BIT PHASE SHIFTER

Goal: *FET switches with on chip TTL driver*

FREQUENCY:	5150 to 5875 MHz
BANDWIDTH:	> 800 MHz
INSERTION LOSS:	< 4 dB min IL (3 dB goal);
INSERTION BALANCE:	+/- 1dB min IL;
PHASE SHIFT:	steps 45 (goal), 90 and 180 degrees
VSWR, 50 Ohm:	< 1.5:1 input & output
SUPPLY VOLTAGE :	+ 5 Volts
CONTROL:	TTL (goal); or 0, -5V switch inputs
SIZE:	60 x 60 mil ANACHIP

The phase shifter is part of a duplex transceiver for C-band HiperLAN wireless local area network (WLAN) for the industrial scientific, and medical (ISM) frequencies.

The following is a block diagram of the class project:



Chip Set for the 5150 - 5350 MHz WLAN and
5725 - 5875 MHz ISM Bands

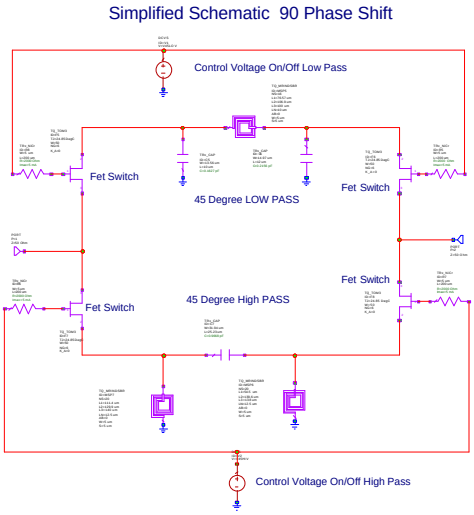
Design Approach

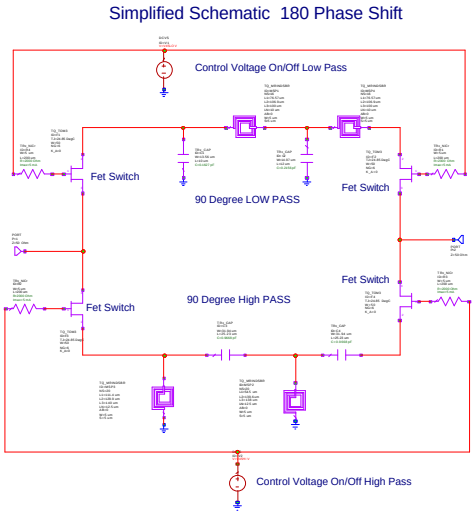
Before discussing the design approach, the following is a simplified schematic and a brief circuit description.

Each individual stage consists of 4 FET switches and two filters. The 2 top and 2 bottom pair of switches are toggled together. By applying complementary voltages of 0V and –5V to the top and bottom control voltages, respectively selects the top filter. Conversely applying –5V and 0V to the top and bottom controls, respectively will select the bottom filter.

The top filters of each stage are low pass filters and the bottom filters are high pass filters. The corner frequency of the low pass filters are set at approximately 1 GHz above the design frequency range (5.15GHz to 5.875GHz). The high pass filters corner frequency is set at approximately 1 GHz below the design frequency range. The high pass filters provide phase lead and the low pass filters provide phase lag.

The following is a simplified block diagram of each stage:

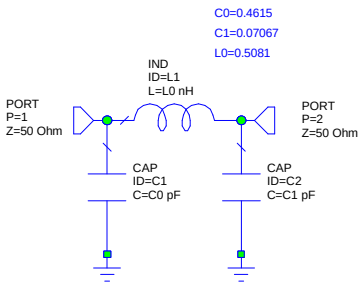


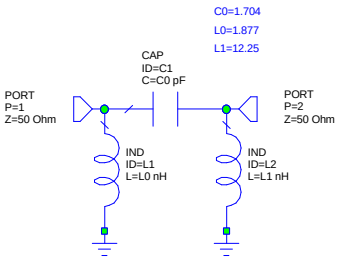


Selection of Topology

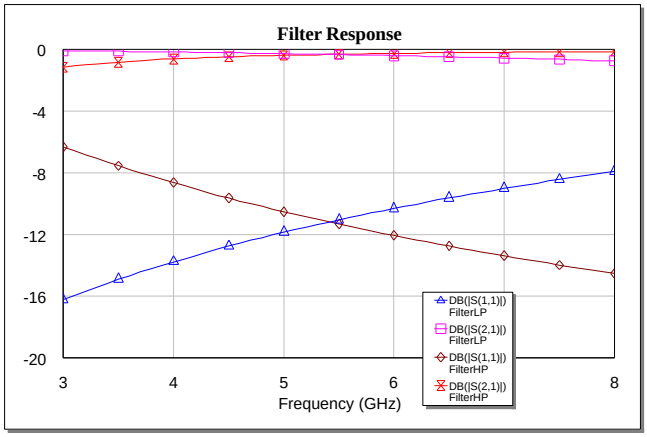
The first step is to settle on a topology for the low and high pass filters. A 3 pole filter using capacitors and inductors was selected for the 1st stage. A 4 pole filter topology was selected for the 2nd stage because of the need for greater phase shift. The critical concept here is that as more poles are added to each low pass filter or pole-zero pairs for high pass filter results in more phase shift. Balancing this requirement is the need to minimize insertion loss. Therefore as the corner frequencies are move closer and farther from the design band, the phase shift and insertion loss can be adjusted. The closer the corner frequency is to the design band, there is more phase shift and more insertion loss.

Using the filter wizard of MWO, the following initial component values of the low and high pass filters were selected.

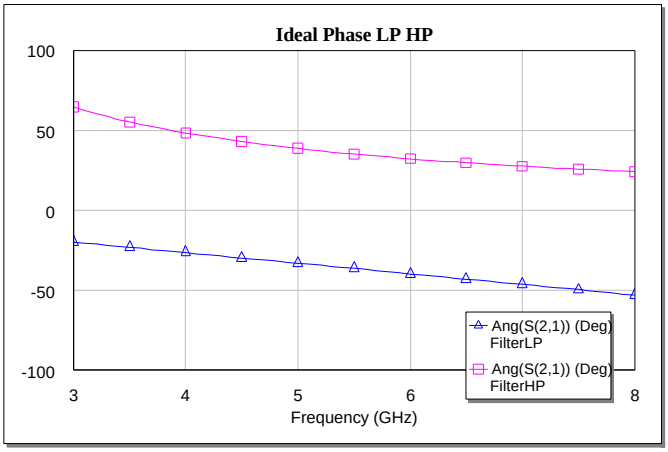




The next graph shows the initial phase shift, insertion loss (S21) and return loss (S11) of the ideal low and high pass networks:



This is the first pass as the phase lead and phase lag of the 3 pole networks:



Trade Offs

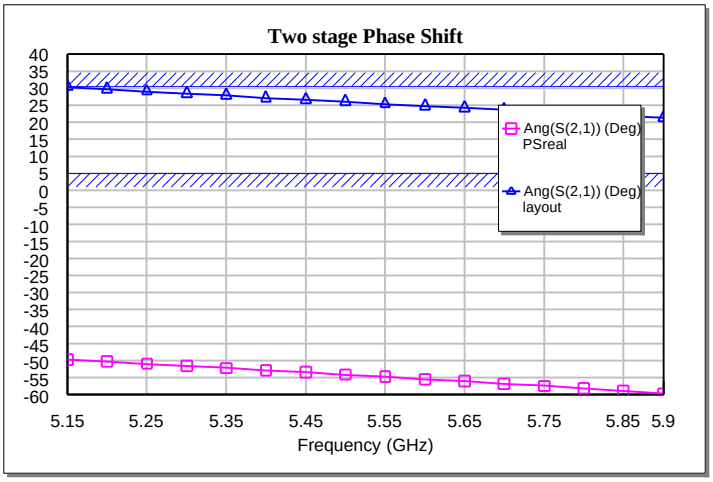
The next critical design decision is that 3 elements (and more) seems to work better because of the ability of compensating for the FET switches on either side of the filter. The FET switches can be modeled when they are “on” as a small series resistor and some small stray capacitance. The off FET switches can be modeled as a larger shunt capacitance. These capacitances can easily be compensated by the multi-stage filter. Also, the insertion loss is minimized when the filter looks like pi sections tuned to 50 ohms characteristic impedance. Another the way of visualizing this process is working with a Smith chart. The smaller capacitors and inductors are

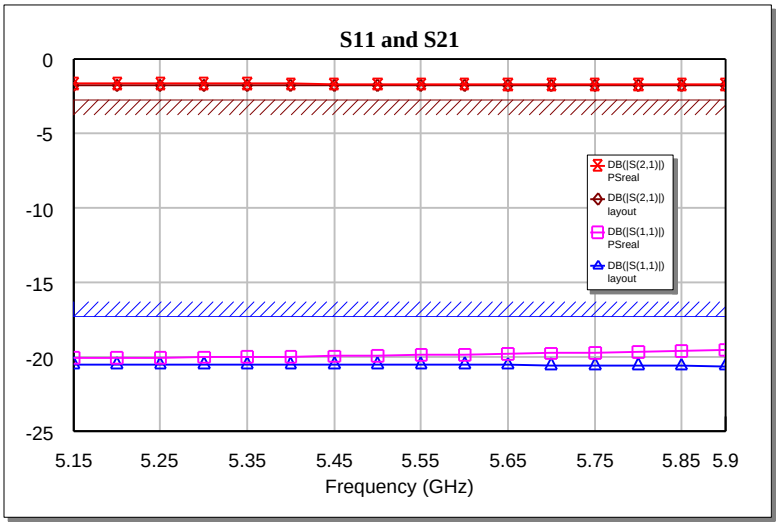
keeping the characteristic impedance closer to the origin (50 ohms) as opposed to a single large capacitor or inductor which moves the impedance farther away from the origin.

The obvious trade-off made during the design phase was to stick with just two bits. An attempt was made to use a one or two element phase shifter for +22.5 and –22.5 degrees. This would have been the third-bit or third stage of the phase shifter. There were design difficulties as discussed above using less than 3 elements. Also, at the time of the design phase it was unclear that a third stage would fit in the Anachip form factor. Also, a third stage would run very close to exceeding the 4dB insertion loss.

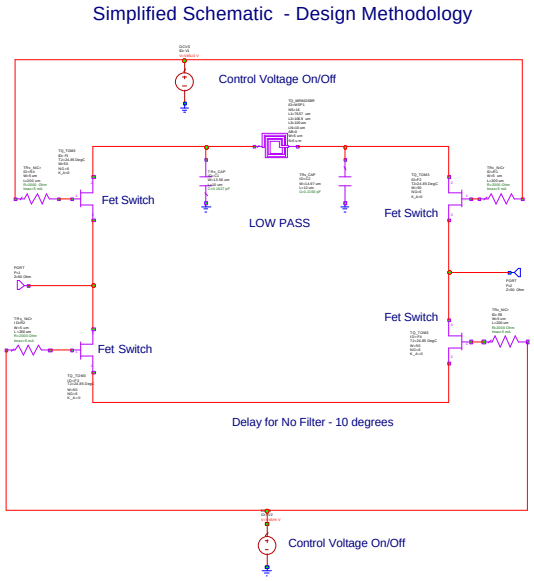
Optimization with MWO

The following graphs show the design process after the initial selection of capacitors and inductors were made. The filters were inserted in the switching matrix and then the following constraints were imposed on the optimization wizard of MWO. The inductor and capicator values were tightly constrained so they didn't drift too far. The insertion loss (S21) was constrained to be better than –3dB and the match (S11) was constrained to be less than –10dB. Then a second plot of phase was also constrained so the phase of the circuit could be adjusted up or down as needed. This process seemed to work quite well as long as the steps were small. Once the phase was adjusted to the correct value, then the S11 and S21 constraints could be more tightly adjusted to optimize the circuit further. The optimization process only took a minute for each adjustment. If the process took more than a minute then the process was stopped and the constraints loosened and optimization restarted.





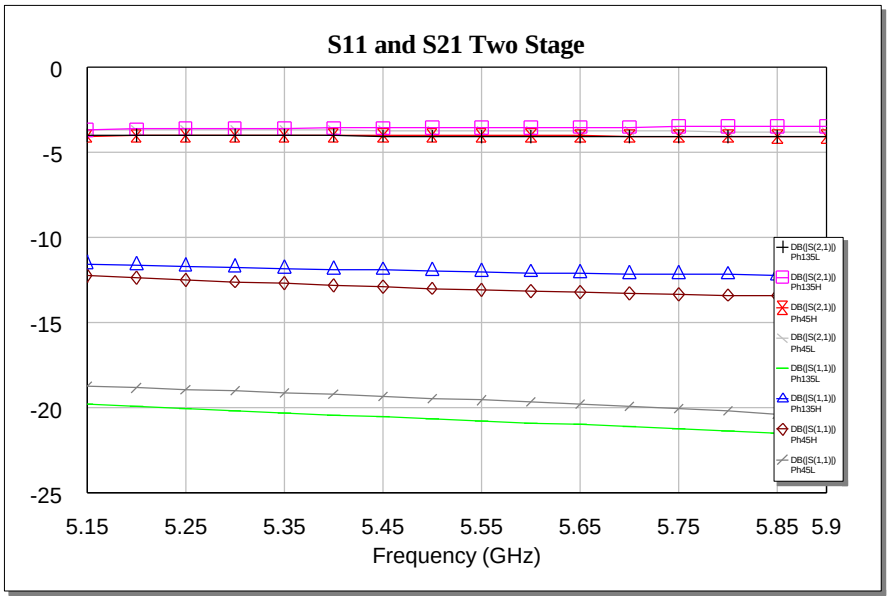
Then was one additional design process. After some initial adjustment, the phase lead circuit component values were larger than the phase lag. The harder work of the high pass circuit translated into not only larger component values but more insertion loss and less match. This also means the knee of the filter is moving closer to the design frequency. The following circuit was simulated to get an idea the 'natural" phase lag of the circuit without any filter.

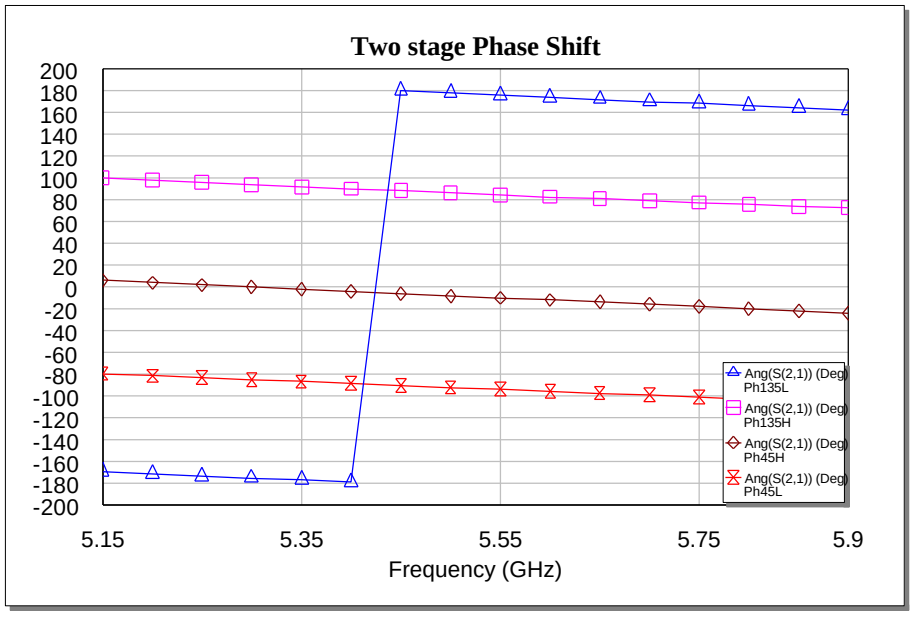


The lower path without any filtering had about 10 degrees phase shift. This offset put back into the optimization process so that the 45 degree phase lead circuit only needed to provide 35 degrees phase lead and the phase lag circuit needed to provide 55 degree phase lag. This balanced the circuits better in terms of sharing the insertion loss and match effects.

Simulations

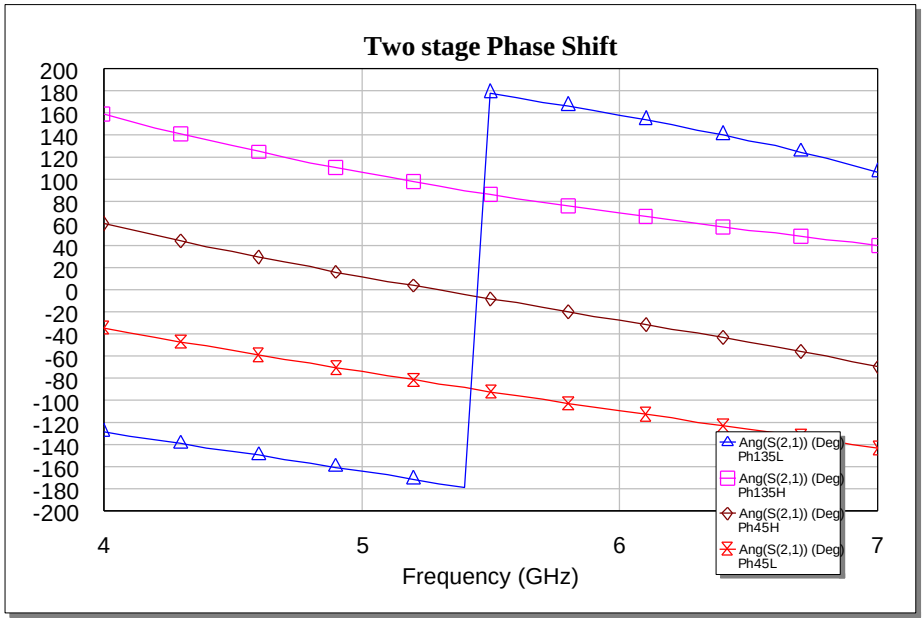
The following is the circuit performance of the phase shifter showing the phase shift, insertion loss, and match over the design frequency:



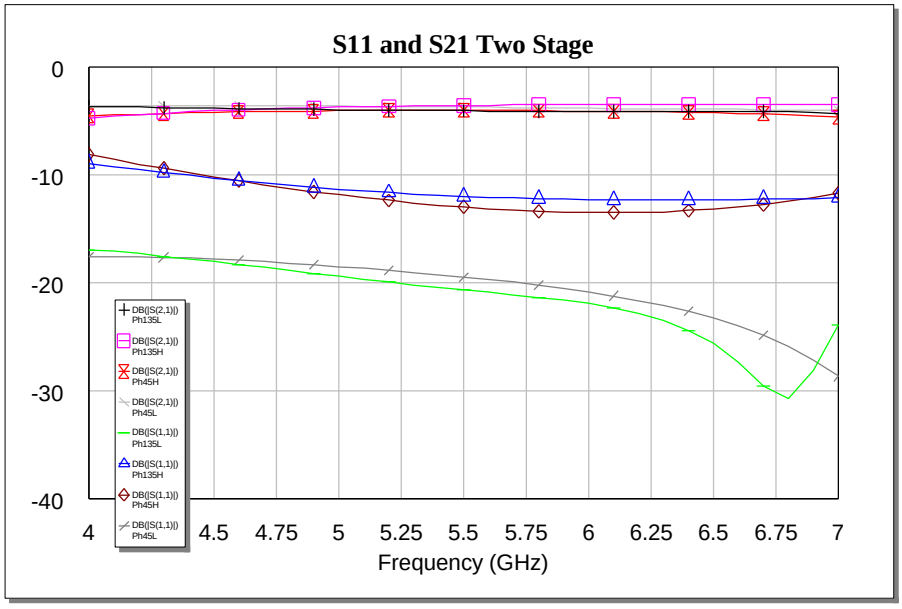


Note that the bottom blue line is the maximum phase lag, and that it folds back around after reaching –180 degrees.

These are the same plots but over a wider frequency range above and below the design frequency.

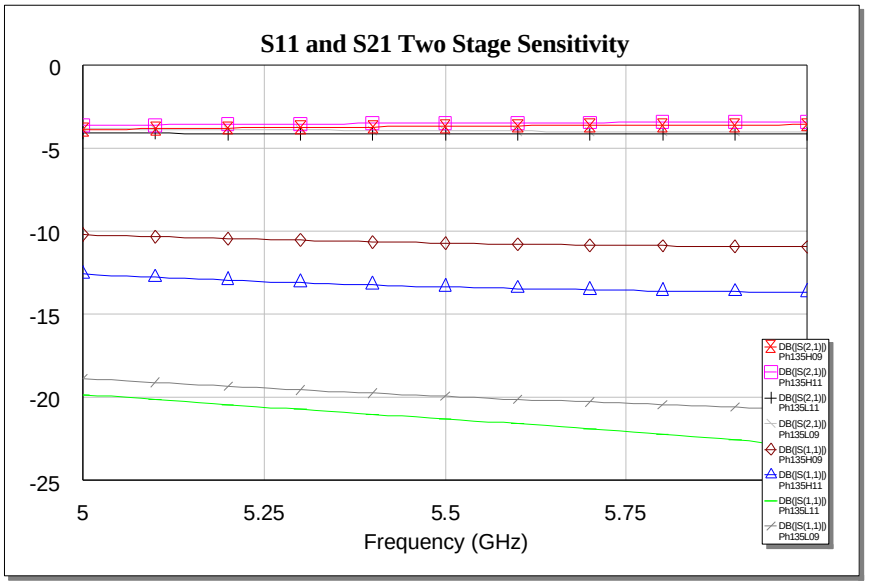


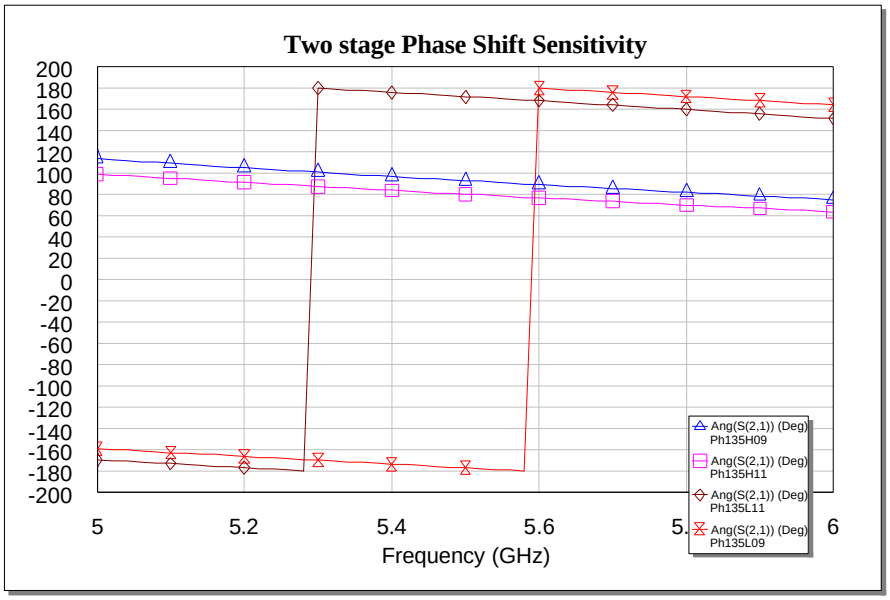
The insertion loss and match look reasonable outside the design frequency per the simulation.



Sensitivity

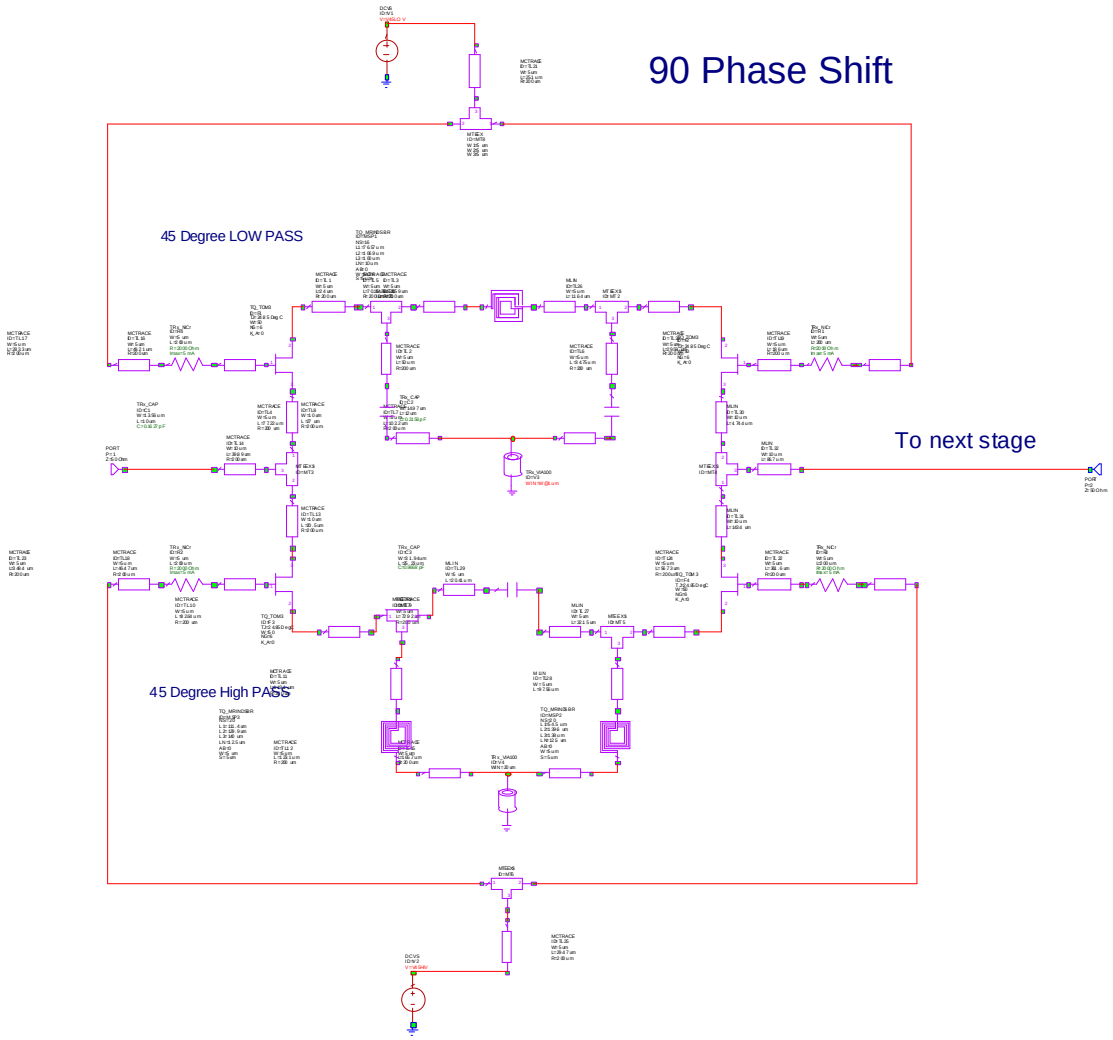
The following plots attempt to characterize the sensitivity of the circuit to process variations. The inductor values should remain fairly constant but the capacitors will vary due to process variations with the thickness of the dielectric. Each plot below is for four schematics, two set at –135 degree phase shift and two at +135 degree phase shift. The capacitance of all the capacitors are varied +/- 5% around the nominal value for a total of 10% variation. From the phase graph, the sensitivity appears to be bounded at 2 degrees per 1% variation (i.e. less than 20 degrees for 10% variation). The insertion loss is less than 1 dB variation however the return loss (S11) varies by as much as 3 dB.



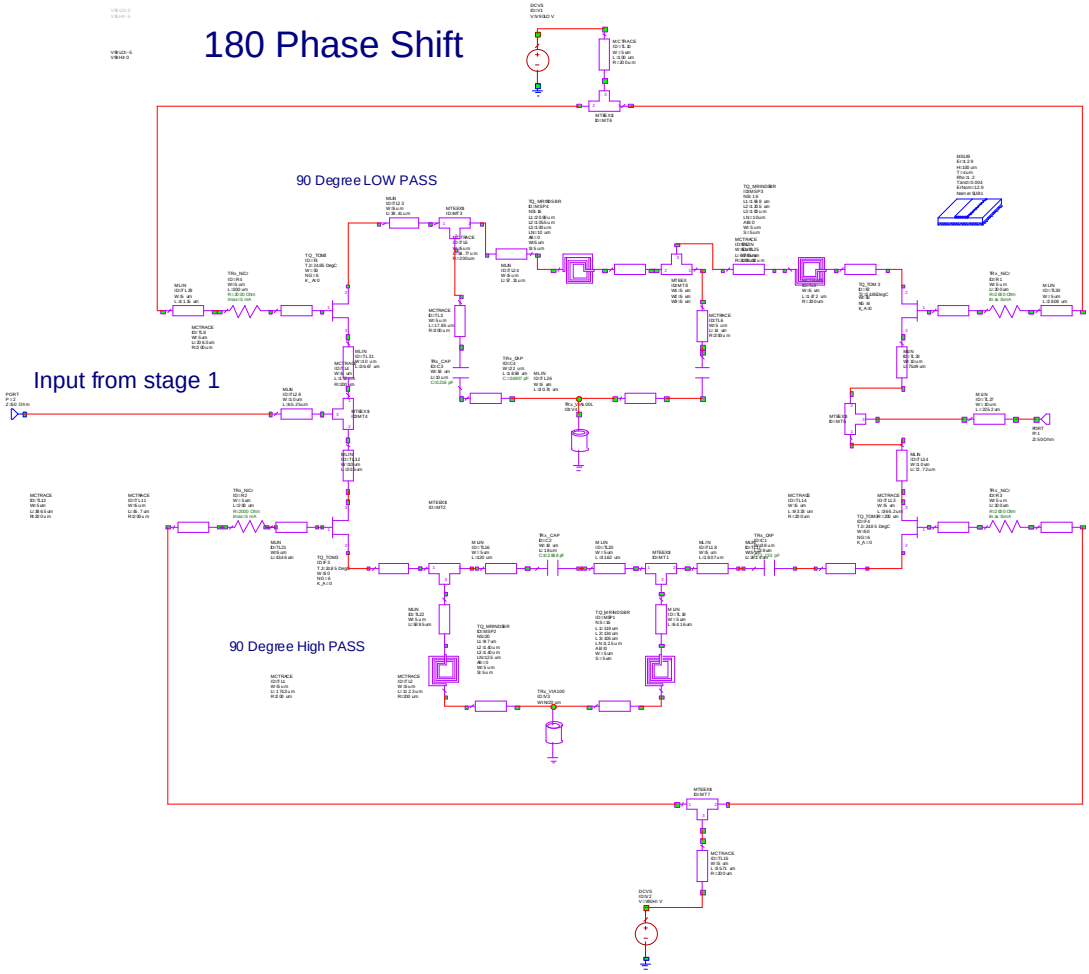


Schematic

The following is the completed circuit schematic including microstrip lines and TriQuint components for FETs, capacitors, inductors, resistors and ground vias. The Anachip pads for port connections and the additional ground pads and some ground vias are not shown in this schematic which are added to the layout. Also there are additional 2k resistors and ground pads attached to the sources of the switching FETs to provide a DC reference ground.



This is stage two with a 90 degree phase lead and a 90 phase lag network selected with the dual pair of FET switches.



Layout Plot

The input port is located at the bottom of the chip, the output port is at the top middle pad. There are ground-signal-ground pad configurations at each of these ports to facilitate probing. The lower left side control voltage pad controls the low pass network for the 45 degree phase lag circuit. The lower right control pad controls the 45degree phase lead circuit. Similarly the top left and top right control pads are for the 90 degree phase lag and lead circuits respectively.
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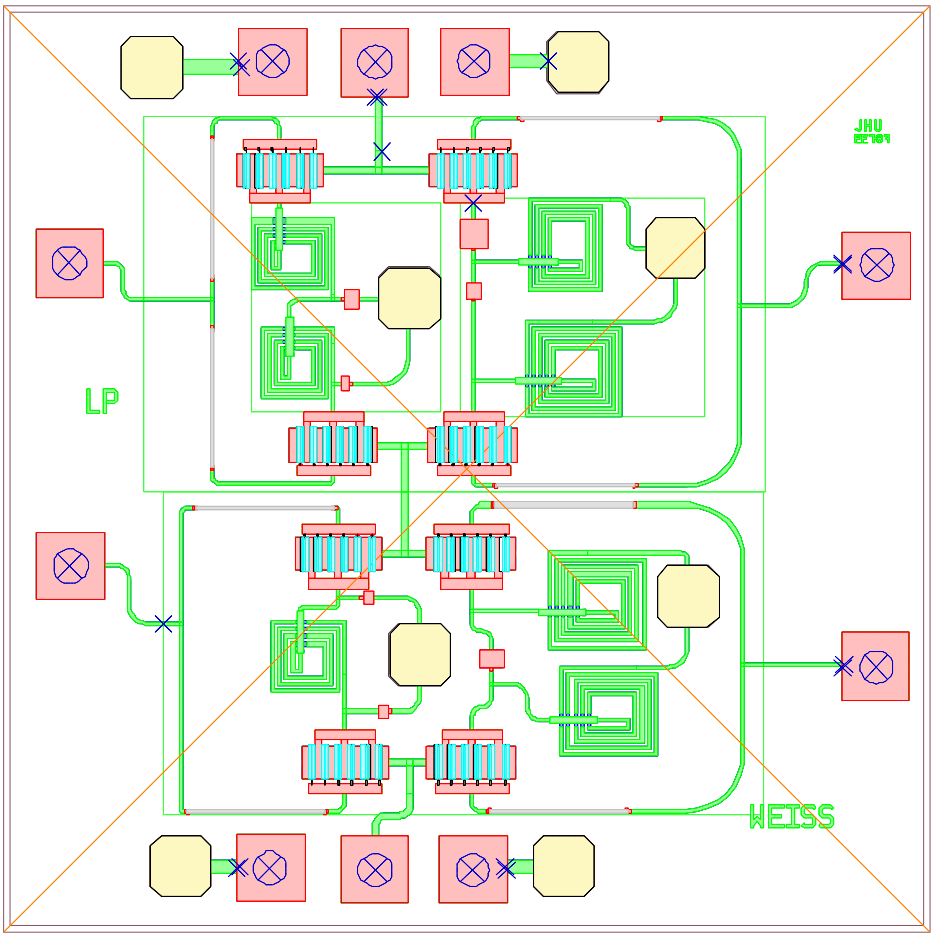
Gnd – RF Output - Gnd

DC-3



DC-4

DC-1

DC-2

Gnd – RF Input -Gnd

DC-1 and DC-2 are complementary control voltage ports for stage 1. DC-3 and DC-4 are complementary control voltage ports for stage2.

Test Plan

Verification of the phase shifter will be with a network analyzer to measure the phase shift for each of the four states of phase shift: -135, -45, +45, +135.

Equipment:

Network Analyzer 8510
Probing Station
Power supply to provide 0V and –5V control voltages

Procedure:

1) Connect port1 of the Network Analyzer via the probing station to the input port with a ground-signal-ground configuration.
2) Connect port2 of the Network Analyzer via the probing station to the output port with a ground-signal-ground configuration.
3) Connect –5V via the probing station to: DC-1 and DC-3 control voltage ports
4) Connect 0V via the probing station to: DC-2 and DC-4 control voltage ports.
5) Perform a sweep from 3 GHz to 7GHz on the Network Analyzer . Save the results of the s2p file to disk. The sweep will have magnitude and phase information of all the S parameters: s11 ,s12, s21,s2.
6) Connect –5V via the probing station to: DC-1 and DC-4 control voltage ports
7) Connect 0V via the probing station to: DC-2 and DC-3 control voltage ports.
8) Perform a sweep from 3 GHz to 7GHz on the Network Analyzer . Save the results of the s2p file to disk.
9) Connect –5V via the probing station to: DC-2 and DC-4 control voltage ports
10) Connect 0V via the probing station to: DC-1 and DC-3 control voltage ports.
11) Perform a sweep from 3 GHz to 7GHz on the Network Analyzer . Save the results of the s2p file to disk.
12) Connect –5V via the probing station to: DC-2 and DC-3 control voltage ports
13) Connect 0V via the probing station to: DC-1 and DC-4 control voltage ports.
14) Perform a sweep from 3 GHz to 7GHz on the Network Analyzer . Save the results of the s2p file to disk.
15) Compare actual results with simulation results for magnitude of S11, S21, S22 and phase of S21.

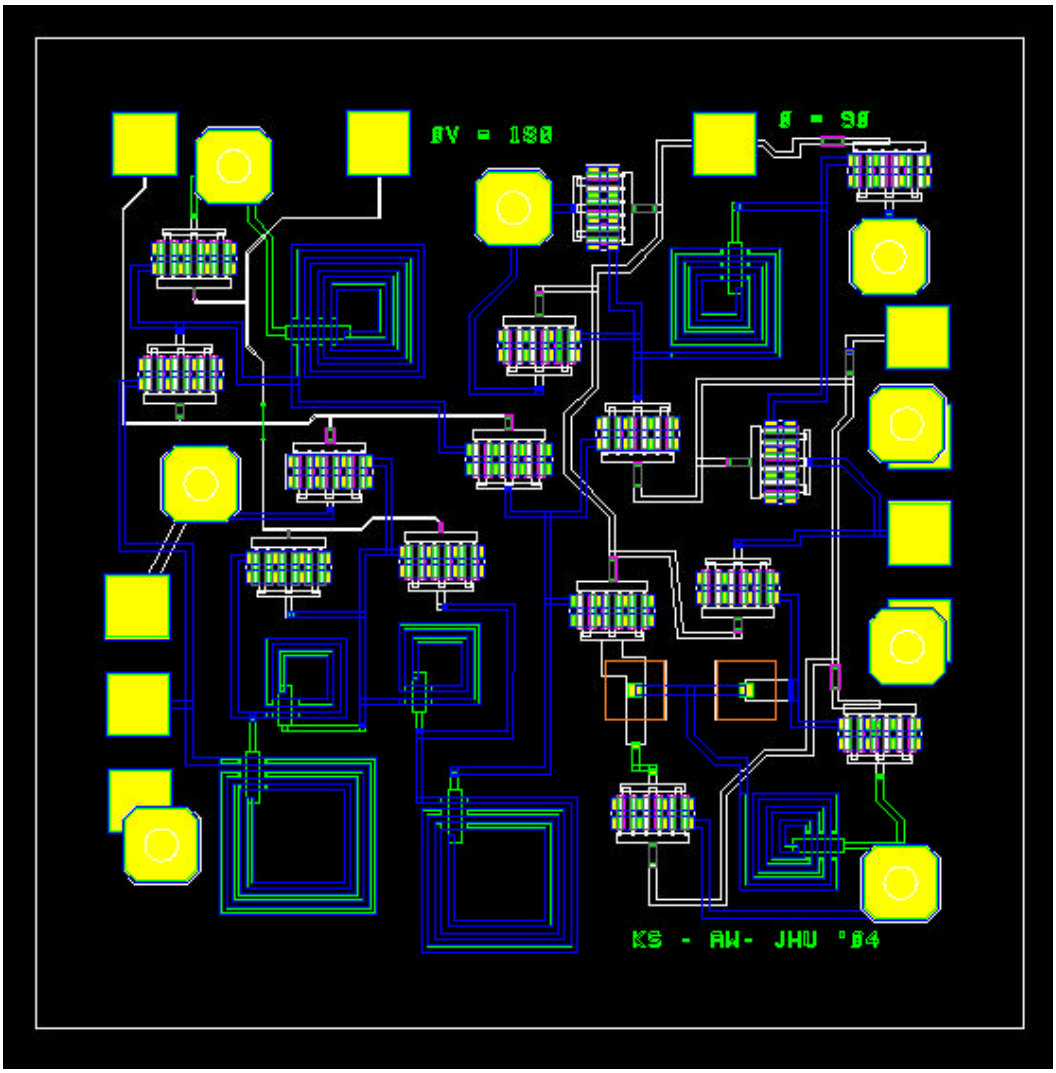
Summary & Conclusions

Most of the design criteria were met for the 2-bit phase shifter. The insertion loss was better than the 4dB specified and the VSWR goal of 1.5:1 (S11<-14dB) was approached with S11 better than -11dB (VSWR 1.8:1).The insertion balance was within the 1 dB specified across the frequency band. With the experience of this design, it might be possible to fit the third bit phase shifter which would shift between –22.5 and 22.5 degrees.

Although not the first time that MWO was used as a Cad tool, it performed reasonably well. The simulations were completed with reasonable ease. However with the layout tool, there were some connection problems that produced a warning message even though the connections were made. The newer version of software 6.5 fixes this problem with more robust connection surfaces using a “variable” setting on the faces. If a component is slightly off-grid the 6.03 software registered an error when two connection faces were “connected”.

The more significant issue is the fabrication and verification of the design using MWO. A successful track record has been established with another CAD tool and so it remains an issue to see how well the designs with MWO prove out under scrutiny of a probing station applied to the MMIC die.

C-BAND 2-Bit Phase Shifter
JHU EE787
Fall 2004



Kevin Shaffer
Andrew Walters

ABSTRACT

This report documents the design of a phase shifter for use as part of a C-band transceiver. The phase shifter is designed to work over the 5.2 to 5.9 GHz frequency band.

The phase shifter was designed using Agilent's Advanced design System (ADS) using the Triquint provided library. The layout was completed on a 60 x 60 mil AnaChip using ADS. The chip will be manufactured using the Triquint Trx process.

INTRODUCTION

Circuit Description

The circuit topology selected for the design was two high pass / low pass switched networks in series to create phase shifts of 90 and 180 degrees. The circuit was designed to use control voltages of 0 V and -5 V. Each bit requires two complimentary voltages to switch between the reference and phase shifted states.

Design Philosophy

The phase shifter design was required to have two phase bits of 90 and 180 degrees, with a loss of less than 8 dB. We chose topology from a documented switched phase Ku design. This design uses the internal characteristics of switched fets, resistive in the on state and capacitive in the off state, to create the high pass / low pass networks. The architecture has only one fet in the through path of the phase bit and should reduce the loss over a design with a switch before and after the high pass and low pass networks.

We began the design with the Ku band basic architecture and then scaled the RF components to C band. This provided a design that was close to desired. The ADS optimizer was then used to tweak the values to provide optimal results.

The next step was to add Triquint elements for simulation and layout. The ideal inductors and capacitors were replaced with Triquint MRIND and MIM capacitors and re-simulated. The result was then tweaked for performance using the Triquint elements. Layout was then completed using ADS and Triquint provided library elements.

Tradeoffs

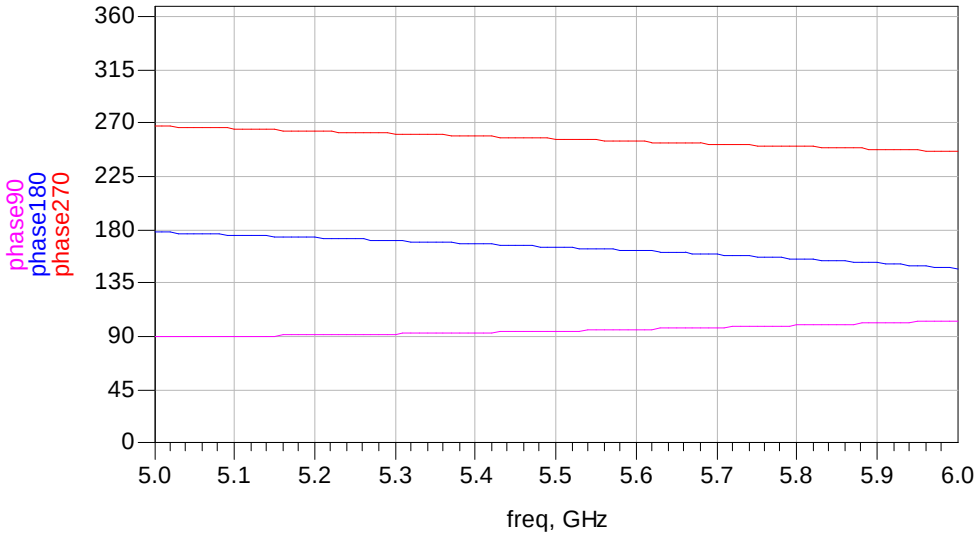
As in any design we had to make performance tradeoffs. We had to make a decision between phase error and loss. By allowing our phase to deviate from its ideal value we were able to achieve a better match over all states and less overall insertion loss.

Specifications and Compliance

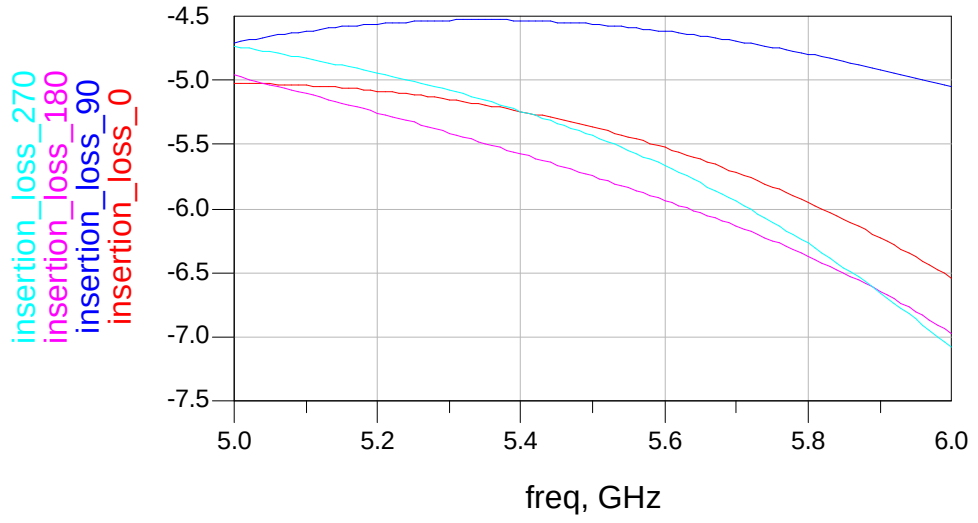
	Specification	**Compliance**
Frequency	5150 – 5875 MHz	Yes
Bandwidth	> 800MHz	Yes
Insertion Loss	< 4dB (3dB goal)	No
Insertion Balance	+/- 1dB min IL	No
Phase Shift	Steps: 45,90,180	Yes
VSWR, 50 ohms	< 1.5:1 input & output	No
Supply Voltage	+/- 5V	Yes
Control	TTL(goal); or 0,-5V switch inputs	Yes
Size	60 x 60 mil ANACHIP	Yes

Simulated Results

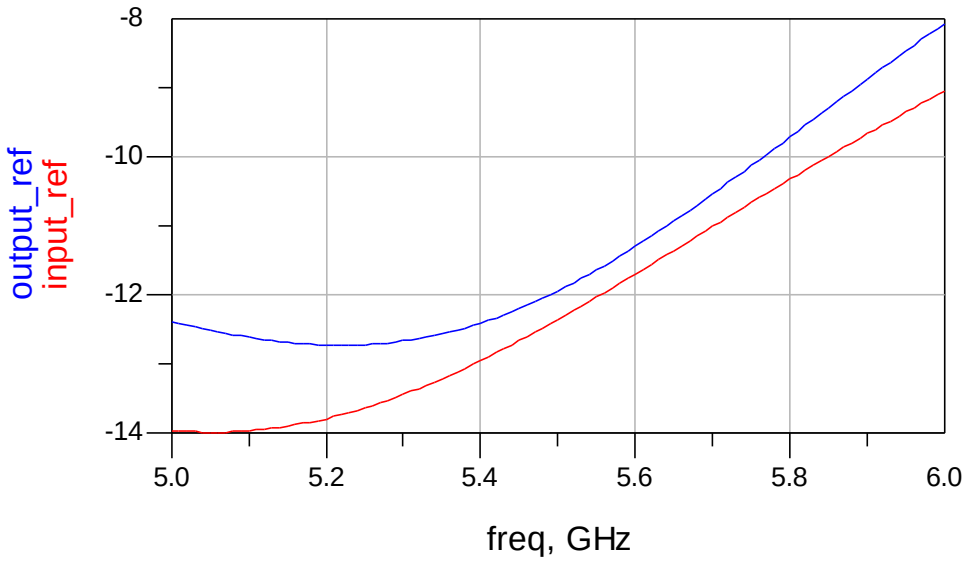
Phase of the different states references to the reference (zero phase shift) state



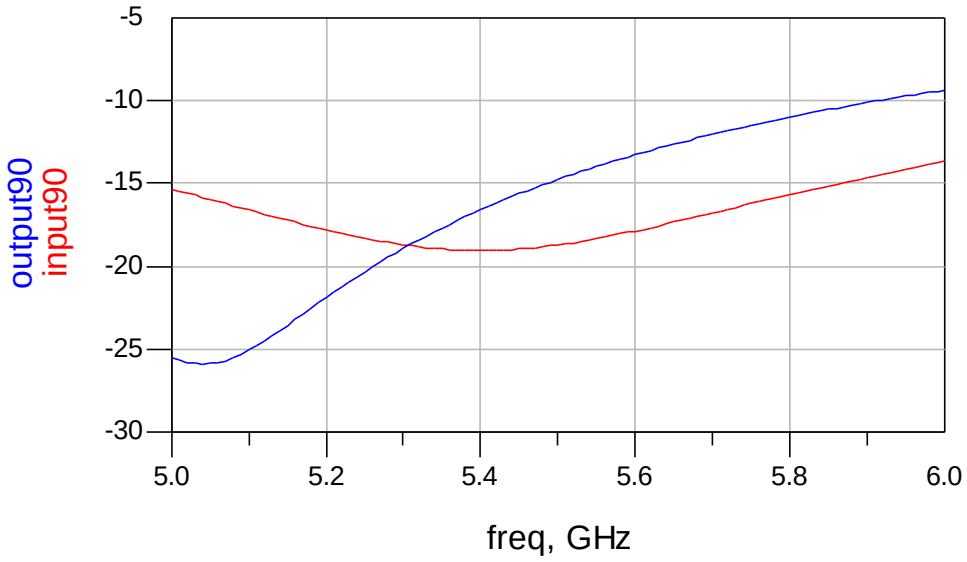
Insertion loss of the four phase states



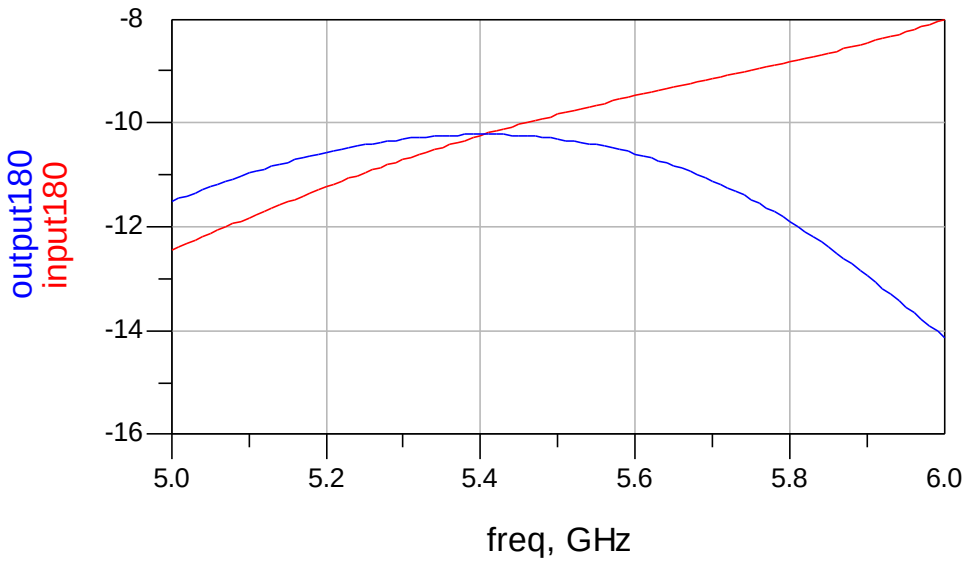
Return Loss for the zero phase state



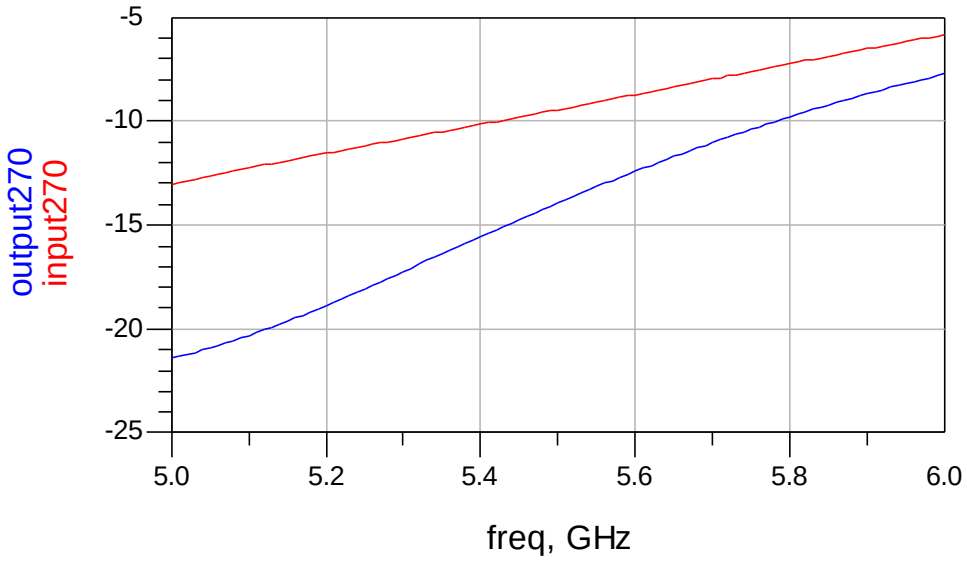
Return Loss of the 90° state



Return Loss of the 180° state

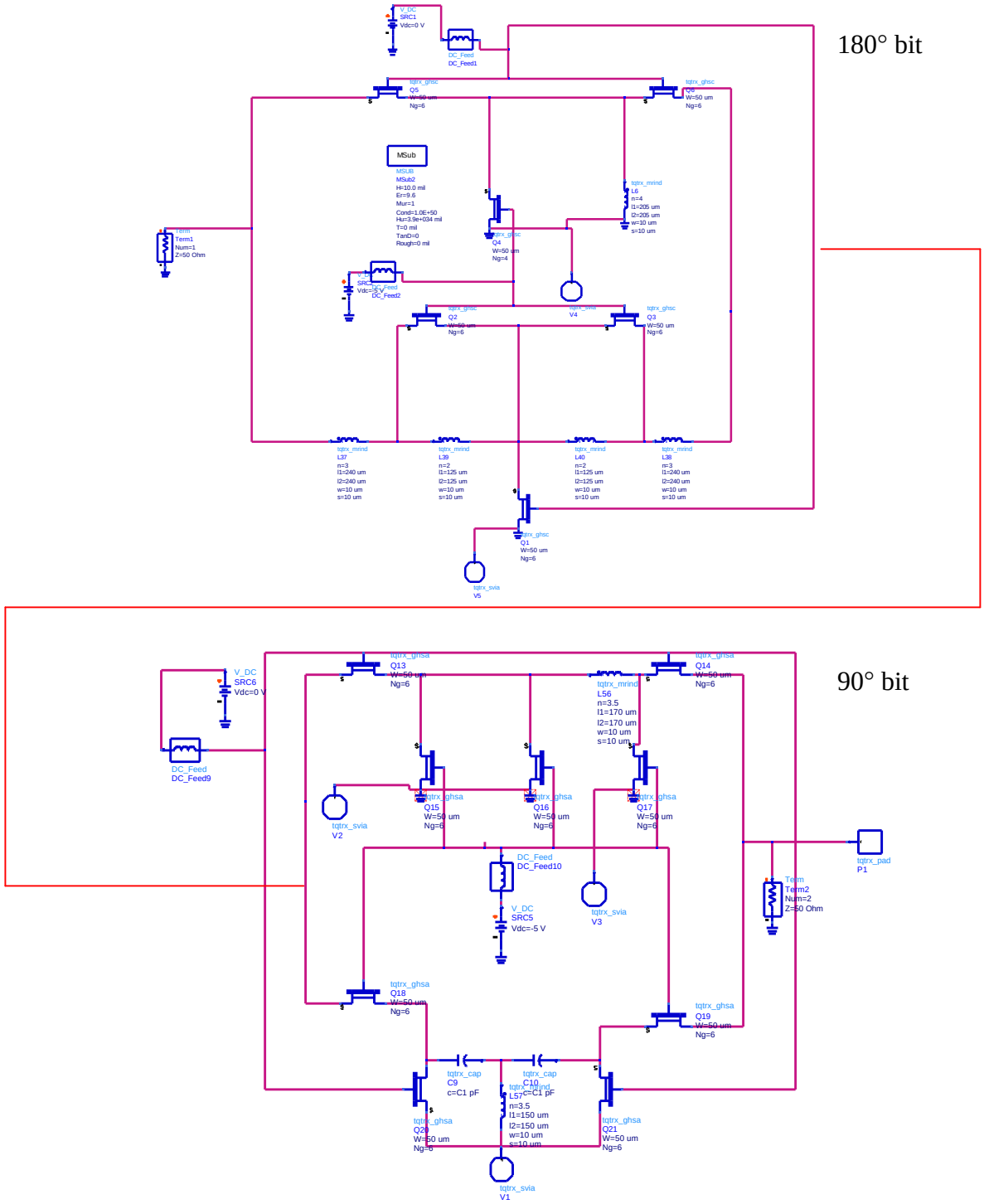


Return Loss of the 270° state



Schematic

This is the completed schematic using TriQuint parts.

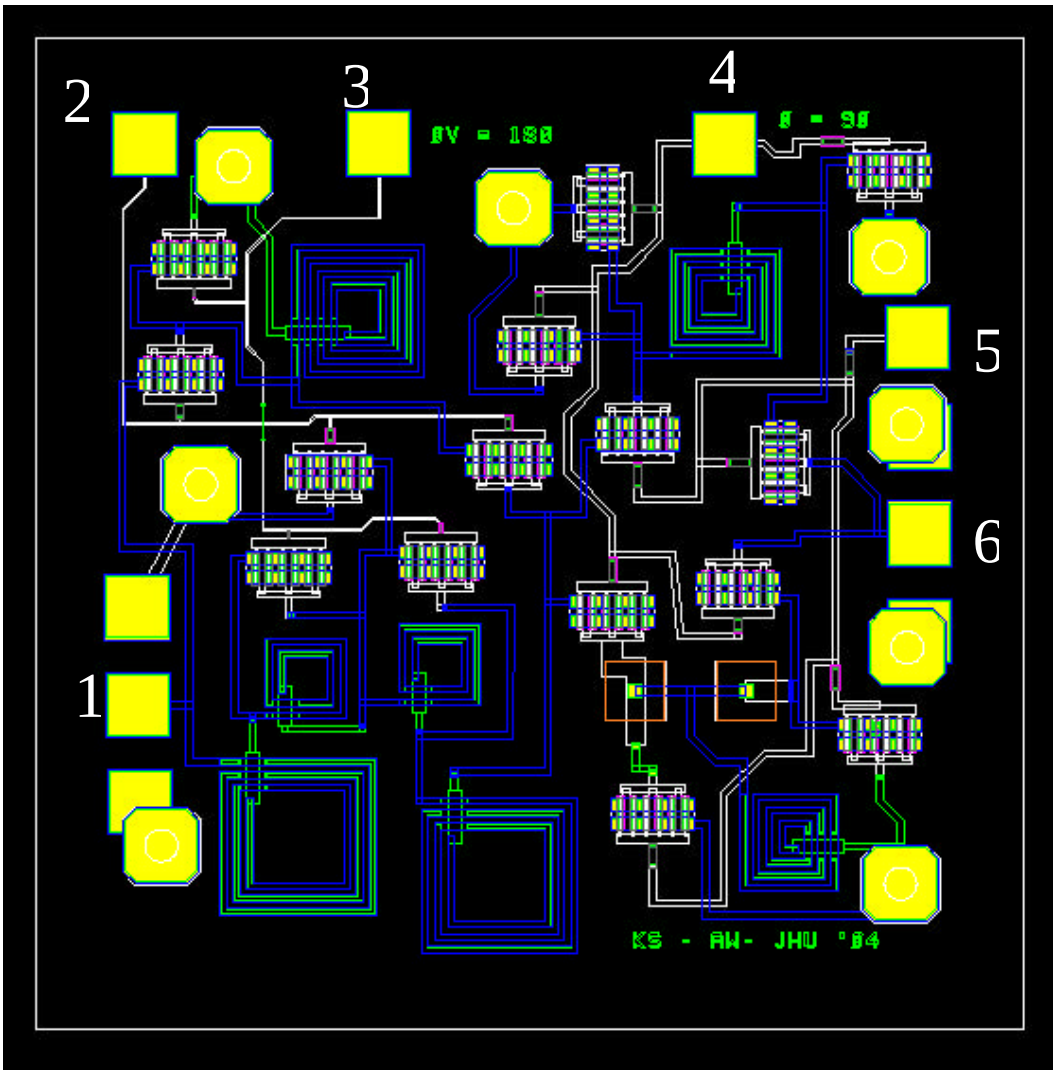


The DC voltages were toggles between 0V and –5V to change phase states.

Layout

The layout is designed to be fabricated on the TriQuint Oregon process. The RF is routed on metal layer two to reduce loss. The inductors are on metal layer 1 and 2 to reduce loss even further. The gate lines are the only signals routed on metal layer 0 since there is no current on these lines. These lines are also narrower then the other since the gate draws no current. G- implant resistors are used because of their high resistance per square allowed the resistors to be small. This type of resistor can not handle much current, but it is acceptable to use them on gate lines where there will be no current.

Pin Number	Pin Name
1	RF In
2	180 -
3	180 +
4	90 +
5	90-
6	RF Out



Test Plan

The phase shifter is designed to be tested using a probe station. For the RF connections (Pins 1 and 6), gnd-signal-gnd probes should be connected to a network analyzer to measure return loss, insertion loss, and phase. This type of probe is used to provide the most accurate measurements. A DC voltage (0V/-5V) must be applied to the other 4 pins using the chart below to dictate what phase state the phase shifter is in. Pins 2 and 5 are compliments and pins 4 and 5 are compliments. The design does not include any DC blocking capacitors on the MMIC, so external ones must be used if they are required.

Phase state	Pin 2	Pin 3	Pin 4	Pin 5
0°	0V	-5V	-5V	0V
90°	0V	-5V	0V	-5V
180°	-5V	0V	-5V	0V
270°	-5V	0V	0V	-5V

Conclusions

The phase shifter MMIC designed should meet the needs of the transceiver system that it is intended to be used in. When designing a phase shifter, a lot of trade-offs must be looked. We found that improving one of the parameters, such as phase accuracy, often meant sacrificing one of the other parameters, such as loss. In general we found it import to use the least amount of series components as possible- in the RF path to help keep the insertion loss to a minimal.

The design was only simulated using the schematic part of ADS. If time allowed, it would be recommended to simulate some of the RF structures in a EM simulator to enough there is no unwanted coupling or interaction between parts.

Once the design has been fabricated, comparing the measured data to the predicted performance will allow the design to be verified. If more space were available, it would be advantage to provide a break out for each of the bits so they could be characterized separately and this would provide more opportunity for troubleshooting.

A C-Band Power Amplifier for HiperLAN Wireless Applications

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[2]Johns Hopkins University: Applied Physics Laboratories, Laurel, MD USA

ABSTRACT — **A 2-Stage C-Band MMIC Class-AB power amplifier (PA) was designed as part of a receiver array for the HiperLAN wireless local area network (WLAN) and industrial, scientific and industrial (ISM) frequencies. The designed was implemented for the TriQuint Oregon TQTRx 0.5-um MESFET process. Good performance in the frequency band of 5.15 to 5.875 GHz (BW = 800.0 MHz) was achieved. The PA had small-signal gain >22.0 dB across the band with an output power > +24.0 dBm and PAE of >30% at the 1dB compression point, for center frequency (f_c) 5.5125 GHz. The input, interstage and output matching networks were designed for a 50.0 Ohm system. VSWR of 1.2 and 2.1 was achieved for the input and output, respectively.**

Index Terms **— Power amplifier, Class AB, WLAN, MMIC, Efficiency, 2-stage, C band.**

I. Introduction

The initial goal was a class F design. However, with the chip size restriction of 60 x 60mil and the marginal improvement in efficiency of the class F design using these device sizes at the design frequency, it was decided that the class AB design was a better choice to meet all the design goals. The overall design goals are listed in table 1.

TABLE 1
SUMMARY OF DESIGN SPECIFICATIONS

Frequency	5150 MHz to 5875 MHz
Bandwidth	>800 MHz
Gain	>13 dB
Gain Ripple	+/- 0.5 dBmax
Output Power	>+20 dBm @ 1dB Compression
Efficiency	>20% @1dB Compression; goal = 25%
VSWR	<1.5:1 (input, output)
Supply Voltage	+/- 5 volts
Size	60 x 60 mil

The power amplifier is a 2-stage cascaded design with a pre-amplifier stage designed around a 6x50um FET and a driver stage designed around an 8x75um FET. The 300um FET in the pre-amplifier and the 600um FET were both biased for class AB operation. The 2-stage design was employed since a single stage was unable to meet the gain and power specification at the design frequency.

II. PA CIRCUIT DESCRIPTION

In consideration that this amplifier will be fabricated as a MMIC and that the layout of the amplifier is challenging, the amplifier was broken up into the sub-circuit topology shown in figure 1.

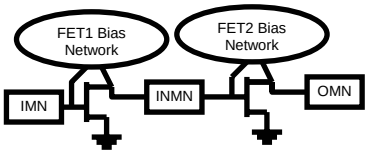


FIGURE 1: 2-Stage Amplifier Topology

This approach simplifies the layout and design optimization process tremendously. In figure 1 FET1 represents the 300um FET and FEt2 represents the 600um FET. The biasing networks utilized individual bias supply for the gate and drain of each FET.

III. Design Philosophy

The design of each sub-circuit component of the PA was first done using ideal lumped elements. Those ideal elements were replaced using the corresponding models from the TQTRx design kit. Resistors and capacitors were easy to synthesize, but inductors had to be carefully modeled using an iterative tuning process. Connection of these foundry components were accomplished using microstrip lines and junctions available in the simulator (Microwave Office ™).

A. Device Selection

A 300um GFET was chosen for the pre-amplifier stage to provide high gain and good power amplification.

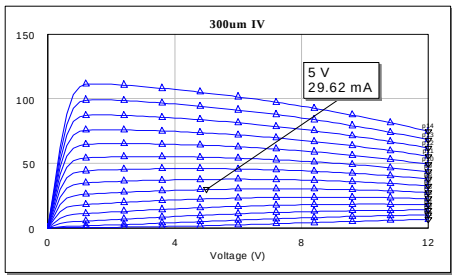


FIGURE 2: 300um GFET Operating Point

The operating point is shown in figure 2.

A 600um GFET was used for the second stage to efficiently boost the power of the pre-amp stage. Figure 3 shows the operating point for the 600um FET.

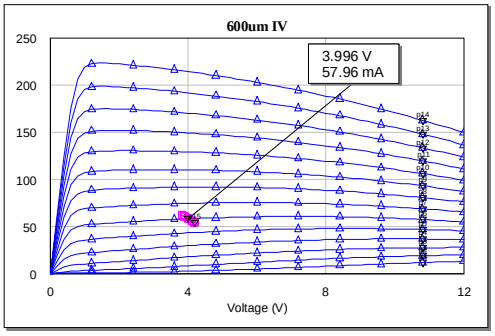


FIGURE 3: 600um GFET Operating Point

It is noteworthy that the bias points for the FETs were chosen to balance gain, power and efficiency. Another subtle goal was to allow for bias tuning. So for drain voltages between 4 volts and 5 volts should tweak the respective drain currents only slightly.

B. Biasing Networks and Stability

The biasing networks were combined with elements used to stabilize the FET. This is illustrated in figure 4.

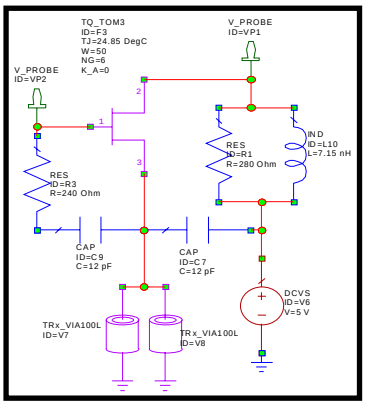


FIGURE 4: Stability/Biasing Network

The inductor on the drain side is chose to provide a convenient RF short while the shunt resistor helps to stabilize the device. The resistor on the gate side plus the small blocking capacitor on the left ensure that the supplied gate bias (shown in section C) current flows to the gate.

C. Input Matching Network (IMN)

The IMN was designed for narrow band (i.e. shortest path from generator to load). However, the path that included a shunt inductor was desired and used since this inductor can be used as the DC feed for the FET gate bias. Since it's large enough, it also provided an RF short.

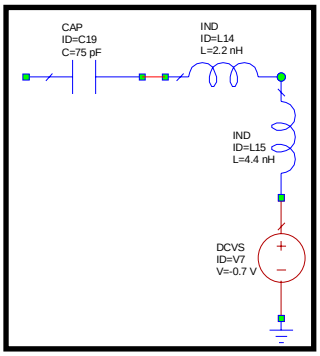


FIGURE 5: Input Matching Network (IMN)

Figure 5 shows the matching network used at the input. This was designed for a conjugate match at the input after the output matching network was designed and connected. The blocking capacitor is also included.

D. Interstage Matching Network (INMN)

The interstage match was designed as a combination of matching the output of the 300um FET and the input of the 600um FET. This technique yielded a network that was then simplified to minimize the number of elements.

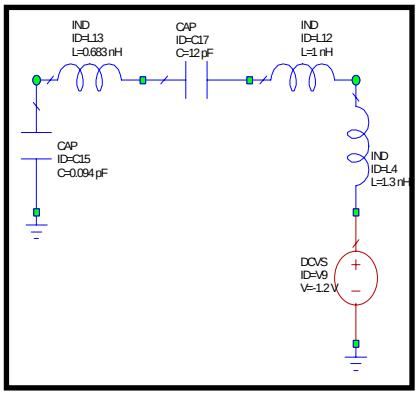


FIGURE 6: Intersatge Matching Network (INMN)

Notice (from figure 6) that the network was chosen such that the shunt inductor on the right can be used as the DC feed for the gate of FET2. A small blocking cap is inserted to direct the current from the supply to the gate of FET2.

E. Output Matching Network (OMN)

Contrary to the order in which the networks are presented in this paper the output matching network was the first to be designed. The procedure is based on the Cripps technique [1]. Rcripps was determined from the DC load line. An RC network was then tuned to model S22 from which Cds could be determined. This is illustrated in figure 7 below.

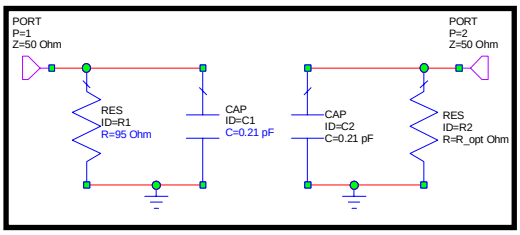


FIGURE 7: RC Network used for Power Match

The reflection coefficient at port 1 of the network on the left of figure 7 determines the optimum power match point. Notice that Rcripps is about 50 Ohms so a single shunt inductor was chosen for the match.

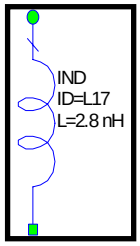


FIGURE 8: Output Matching Network (OMN)

The shunt inductor shown in figure 8 was also used as the DC feed for the drain of the 600um FET.

F. Converting to TQTRx Elements and Interconnects

Each subcircuit was converted an equivalent circuit using the TQTRx elements from the design kit and connected using microstrip lines, tees and crosses. The Microwave Office circuit simulator has an element called MTrace that models the bends when the trace is auto-routed in the layout of the circuit. This eliminated the need for including bends in the circuit. Each converted TQTRx subcircuit is then compared to the corresponding lumped element subcircuit used in the initial design.

IV. Simulation Results

Since each TQTRx element in each subcircuit has associated artwork the layout of the subcircuit is automatically generated at the touch of a button. Minor manipulations are required to position connections to other subcircuits.

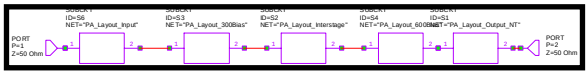


FIGURE 9: Subcircuit-Connected Power Amplifier

When all the subcircuits are connected as illustrated in figure 9 the entire amplifier can be simulated for small-signal and large-signal performance. Table 2 shows a summary of the performance of the amplifier at the two major stages of the design process.

TABLE 2
SUMMARY OF DESIGN SPECIFICATIONS

	Specifications	Pre-Layout	Post-Layout
Amplifier Class	F	AB	AB
Frequency	5150 MHz to 5875 MHz	yes	yes
Bandwidth	>800 MHz	yes	yes
Gain	>13 dB		>22 dB
Gain Ripple	+/- 0.5 dBmax	<0.5 dB	<0.5 dB
Output Power	>+20 dBm @ 1dB Compression	>23 dBm	>22 dBm
Efficiency	>20% @1dB Compression; goal = 25%	>33 %	>30 %
VSWR	<1.5:1 (input, output)	1.2, 1.9	1.2, 2.1
Supply Voltage	+/- 5 volts	+4, +5	+4, +5
Size	60 x 60 mil	NA	yes

The simulated performance of the amplifier was very encouraging. Figure 10 shows the small-signal performance (S11, S22 and S21).

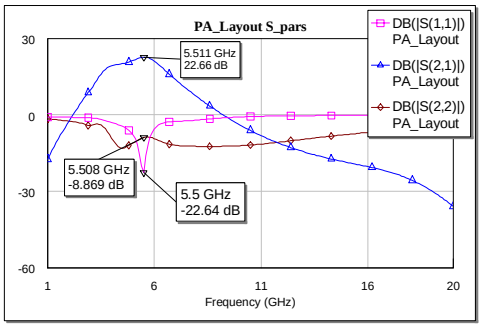


FIGURE 10: Small-Signal Performance of the Final PA

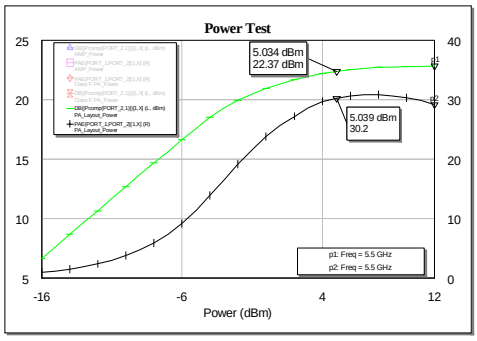


FIGURE 11: Large-Signal Performance of the Final PA

Figure 11 shows the Large-signal performance of the PA. Note that Output Power is displayed on the left y-axis and Efficiency is displayed on the right

V. Final Schematic and LAyout

The final subcircuit schematics of the power amplifier are presented as an attachment (see appendix A) since they are too large to be legible.

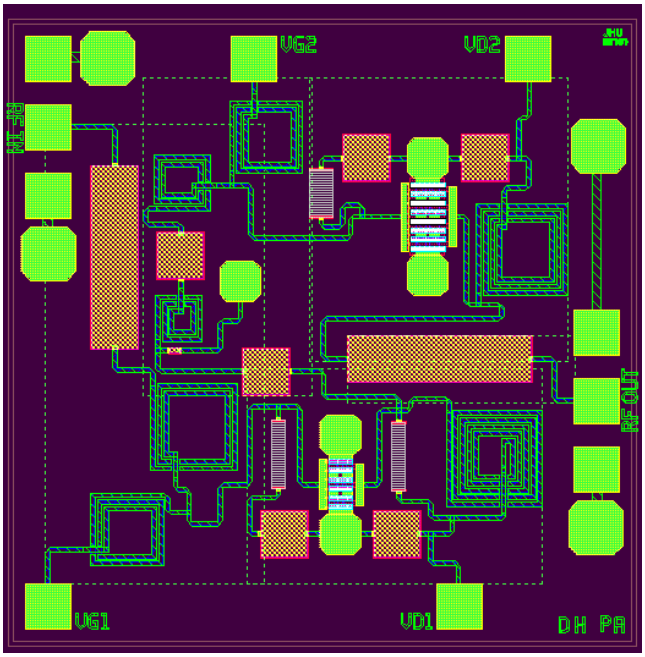


FIGURE 12: Layout of the Final PA

VII. Test Plan

In order to measure the amplifier after fabrication it was necessary to place DC and RF pads on all four sides of the chip. DC needle probes will be used to provide individual bias to the gate and drain of each transistor (top and bottom of chip as shown in figure 12). RF probes will come in from the left and right of the chip for input and output, respectively.

VII. Conclusion

The overall goals of the design were met, with the exception of the output VSWR. Since this was achieved with a class AB design and the performance was considerably higher than the specifications, the class F design was not necessary for this application. So a chip size trade-off was considered and consequently the class AB design was chosen. With this design It was not necessary to make any other performance trade-offs.

Acknowledgement

The authors wish to acknowledge the technical support of Applied Wave Research and Triquint Semiconductor for providing the Process Design Kit and fabrication services, respectively.

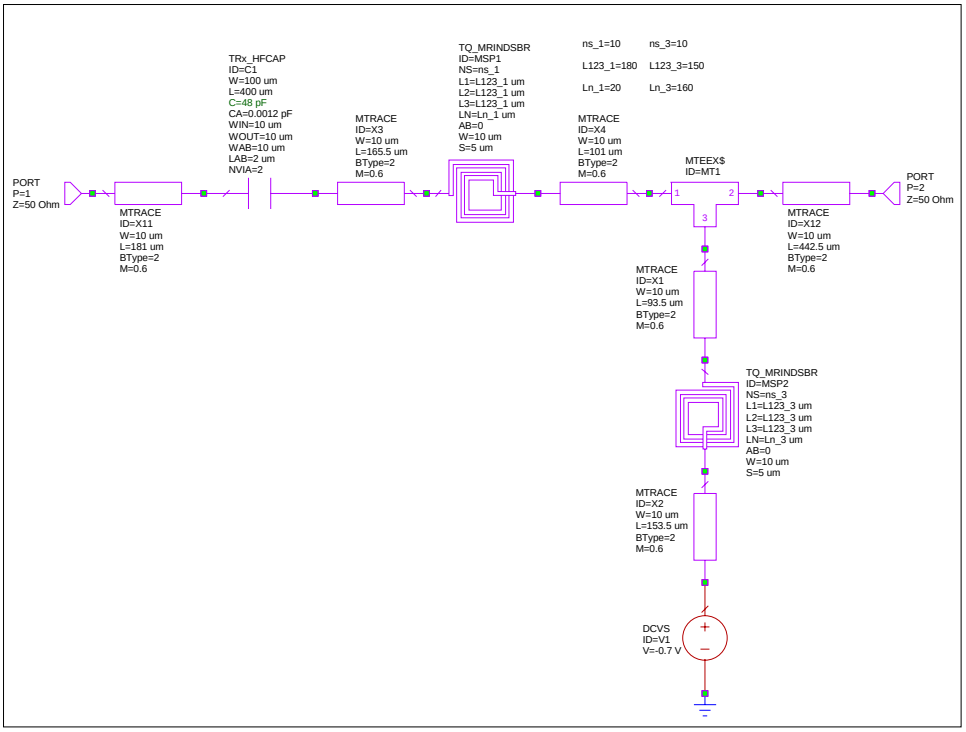
References

[1] S. Cripps, “RF Power Amplifiers for Wireless Communications,” Artech House, 1999, chapters 3, 5, 8.

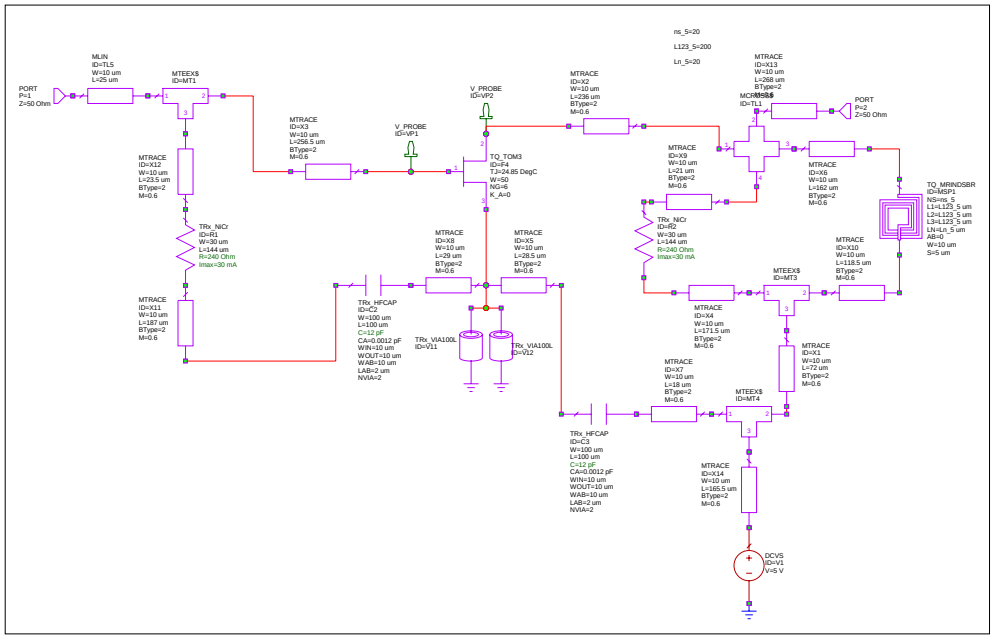
[2] F. H. Raab, “Maximum Efficiency and Output of Class-F Power Amplifiers,” IEEE transactions, Vol. 49, No. 6, June 2001, pp 1162-1166.

[3] C. Moore and J. Penn, “Microwave Monolithic Integrated Circuit Design”, Class Notes, Johns Hopkins University, Fall 2004

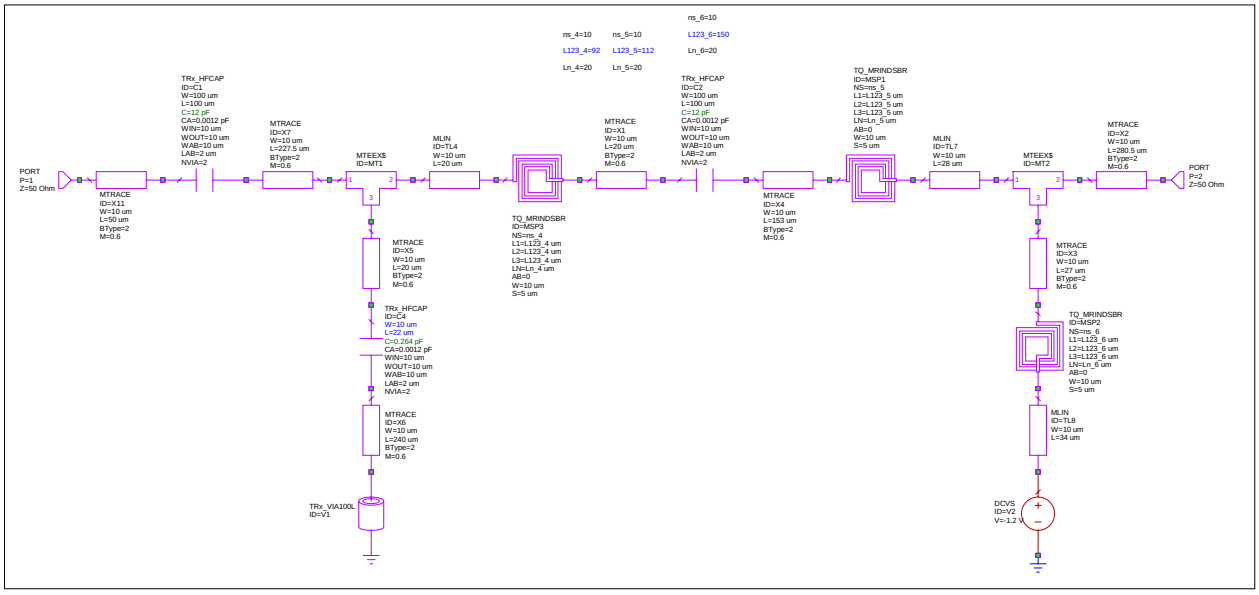
Appendix A



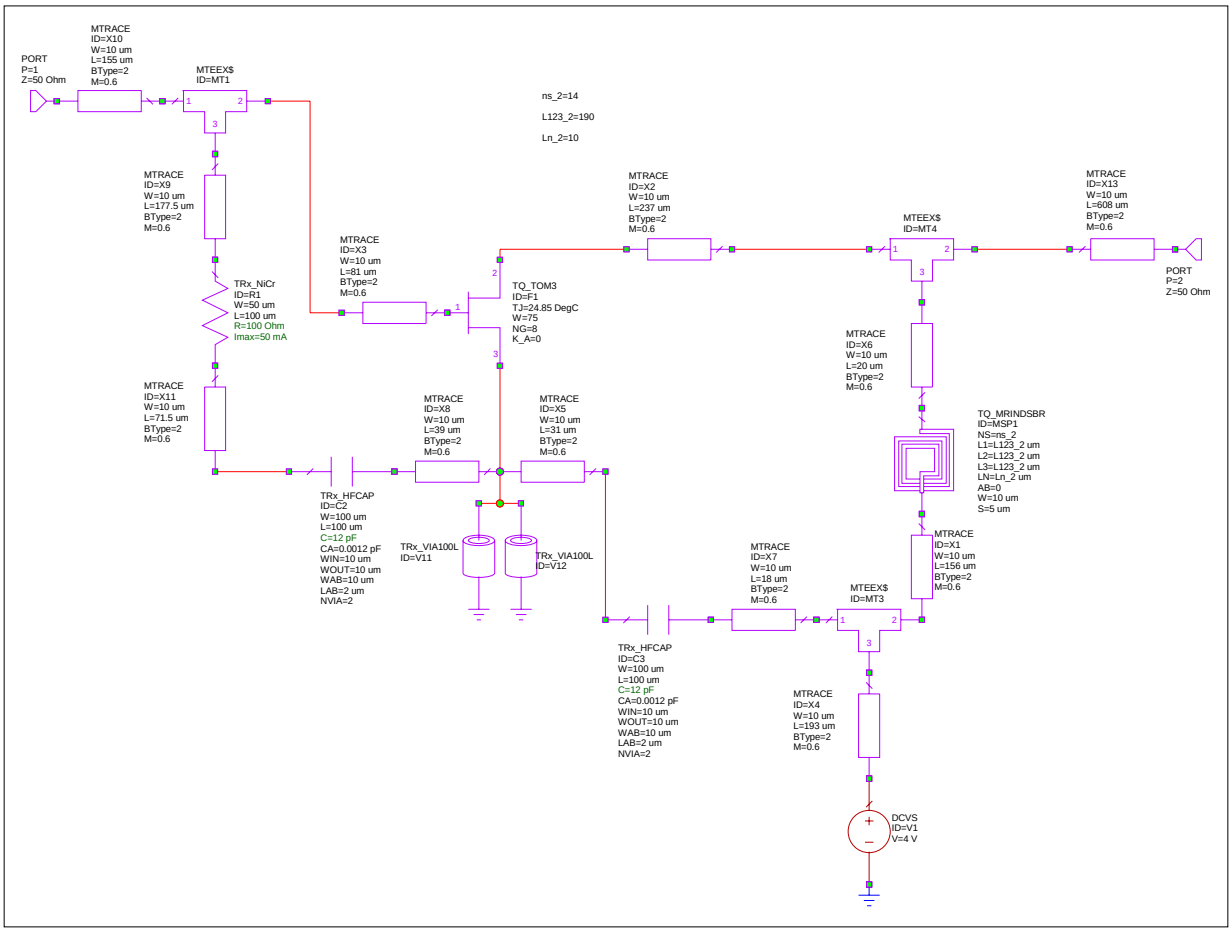
Input Matching Network (IMN)



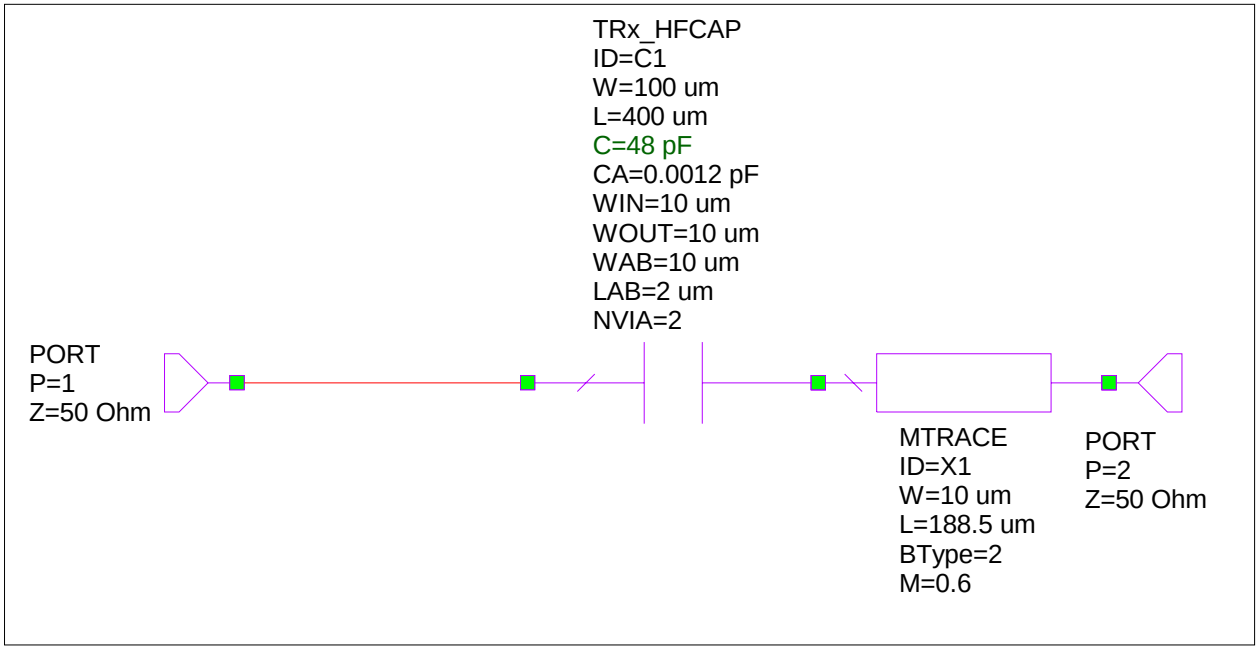
Biased 300um GFET



Interstage Matching Network

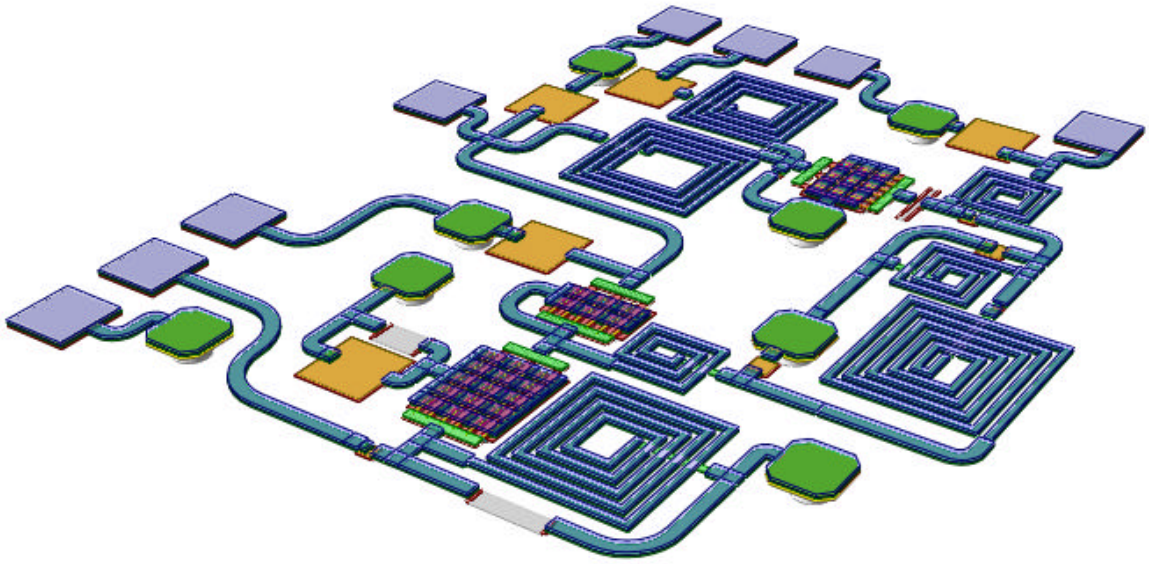


Biased 600um GFET



Output Blocking Cap (matching Inductor included in Biased 600um network)

S/C Band Frequency Doubler
Using Microwave Office
With the Triquint Library



Design by Andrew Zundel
Johns Hopkins University
EE525.787
MMIC Circuit Design
Fall 2004

Abstract

This report presents the design of an S/C band Frequency Doubler. The circuit was designed to be placed on a 60x60 mil GaAs chip using the Applied Wave Research Microwave Office development software in conjunction with the Triquint TQTRx library.

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RF Schematic *9*

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Procedure *13*

Conclusion **14**

Introduction

Circuit Description

The S/C band Frequency Doubler was designed for an input frequency range of 2.7125 to 2.8125 GHz and an output frequency range of 5.425 to 5.625 GHz. It was expected to receive a 10 dBm input signal and to output the 2nd harmonic of the input with no more than 3 dB of conversion loss, with a goal of 0 dB less. It is also desired to have at least 16 dBc of the fundamental and 20 dBc of the 3rd harmonic, as well as an output VSWR of no more than 2.5:1.

Design Approach

The doubler was designed using an initial amplifier biased close to the cutoff point of the GFET to maximize the non-linear effects of the transistor. This produces a waveform that contains an attenuated fundamental and significant amounts of both 2nd and 3rd harmonics. A filter is then used to further attenuate the fundamental as well as the 3rd harmonic, thus leaving the 2nd harmonic as the dominant portion of the waveform. A final stage amplifier was then used to amplify the resultant 2nd harmonic up to the desired level.

Input Amplifier

The input amplifier was designed using a 150x6 GFET with an active load consisting of a 75x6 GFET. The amplifier was biased at –2.0 V, 25 mA IDS, to try and force the transistor to operate near cutoff. The bias was produced using a self biasing structure, an 80 Ohm resistor was placed on the source of the GFET, lifting it to 2.0 V and the gate was connected to ground using a 200 ohm resistor. Matching networks were then created to try and maximize the resulting 2nd harmonic.

Butterworth Filter

To try and save space, a Butterworth bandpass filter was created with N=2. The resulting circuit used a series LC circuit followed by a parallel LC circuit to ground.

Output Amplifier

This amplifier was designed using Power Amplifier techniques. The circuit consists of a 100x6 um GFET biased at Vgs = –0.8 V and Ids = 110 mA. This required two separate bias voltages to be brought in through spiral inductors estimated to be 2 nH. Again matching networks were produced to maximize the output power over the range of 5.425 to 5.625 GHz.

Tradeoffs

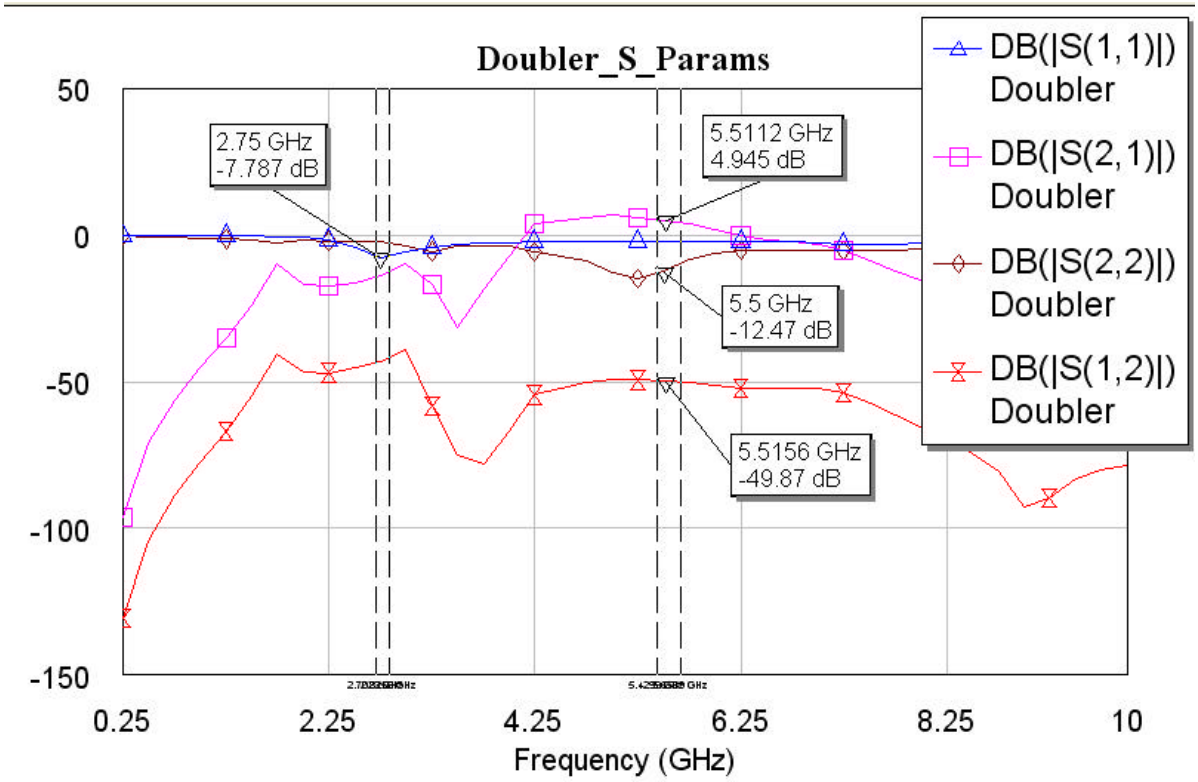
The main tradeoff that I encountered was dealing with size constraints. This controlled the design from concept all the way to the final layout. I found that a two stage filter would give me enough rejection with only 2 inductors and so this was picked over other possible designs, such as a balanced amplifier requiring a 180 degree hybrid coupler. Size also controlled how the various matching networks were designed, always opting for smaller inductor size.

There were various other tradeoffs that I encountered. I opted to sacrifice VSWR for output power at the 2nd harmonic. Also I encountered some stability problems when I tried to use a single DC source and a self biasing structure on the output amplifier. Thus, I had to bring in a second DC voltage source.

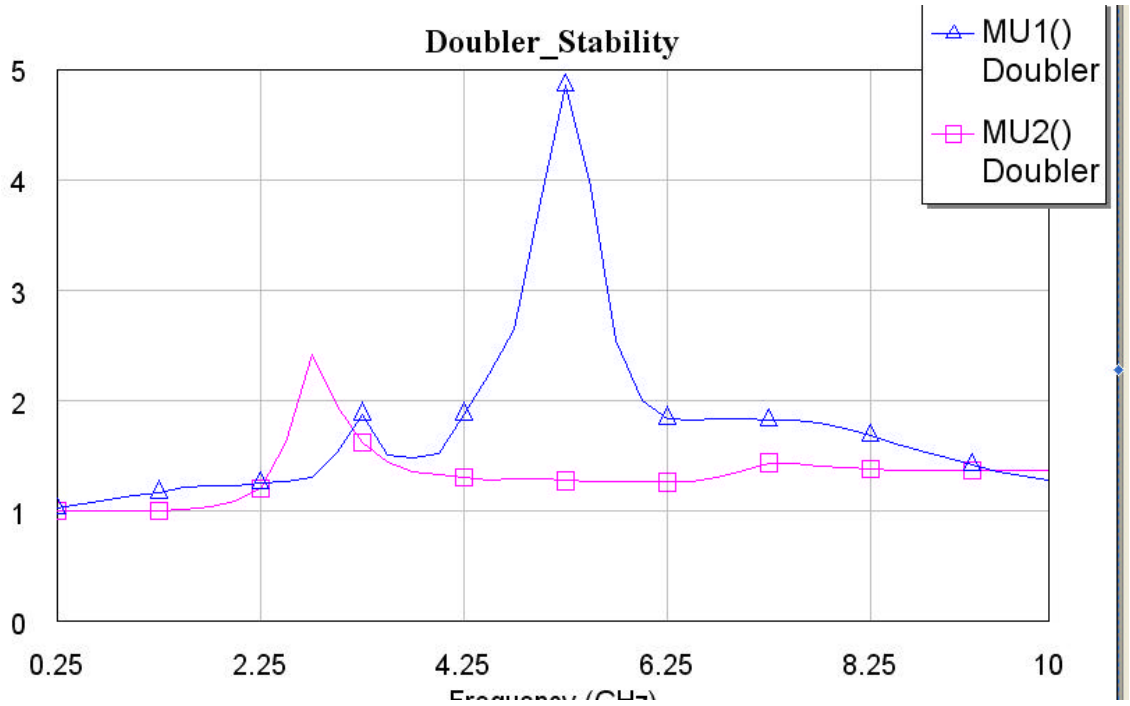
A comparison of the specifications with the results of the final simulations is shown below. This shows the results of some of the tradeoffs that were encountered.

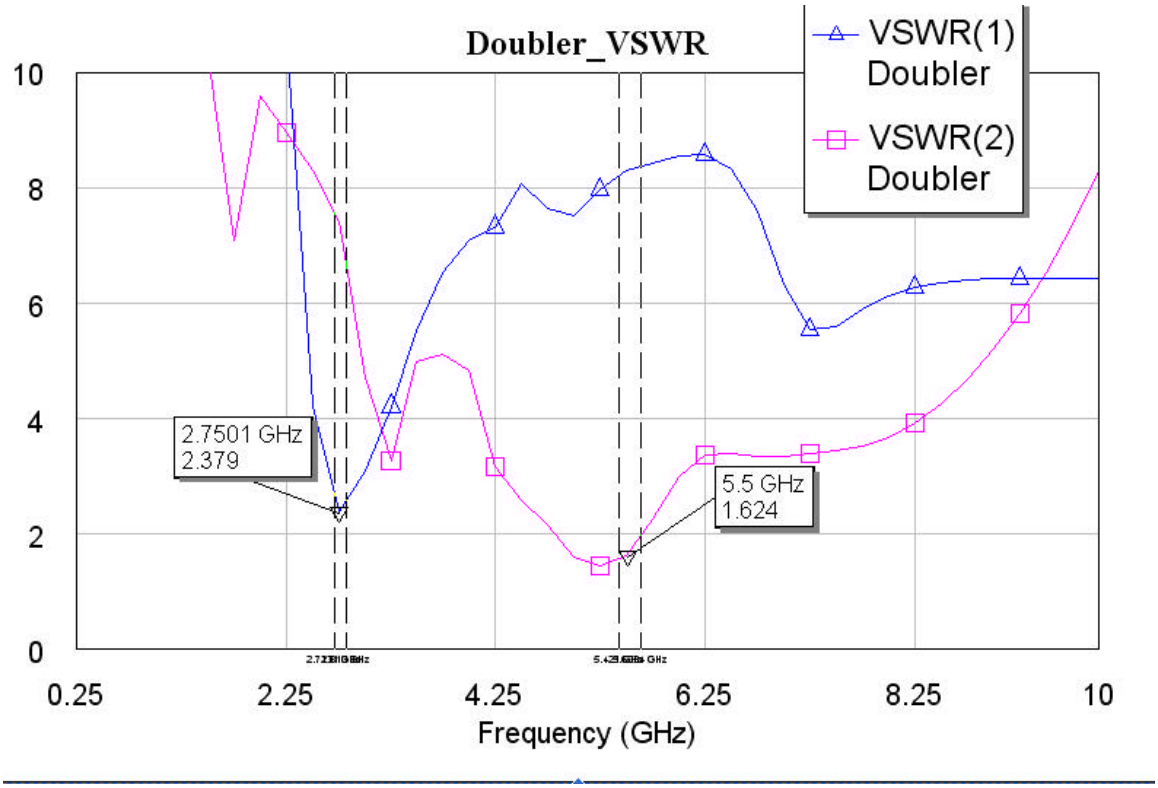
	Goal	**Simulated**
Input Frequency	*2.7125-2.8125*	*2.7125-2.8125*
Output Frequency	*5.425-5.625*	*5.425-5.625*
Conversion Loss	*3 dB (0 dB)*	*4 dB*
Input Power	*10 dBm*	*10 dBm*
Spurious (Fund)	*16 dBc (25 dBc)*	*18.2 dBc*
Spurious (3rd)	*20 dBc (30 dBc)*	*40.4 dBc*
Input VSWR	*2.5:1 (1.5:1)*	*2.3:1*
Output VSWR	*2.5:1 (1.5:1)*	*1.6:1*

Simulations

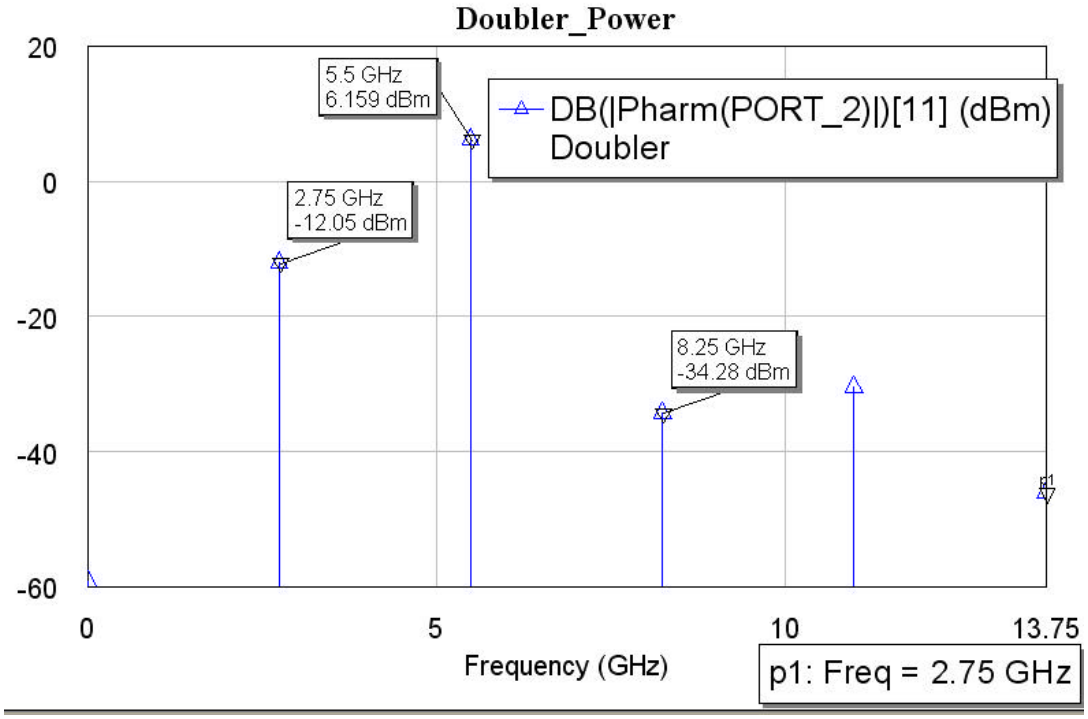


Linear Simulations





Non-Linear Simulations



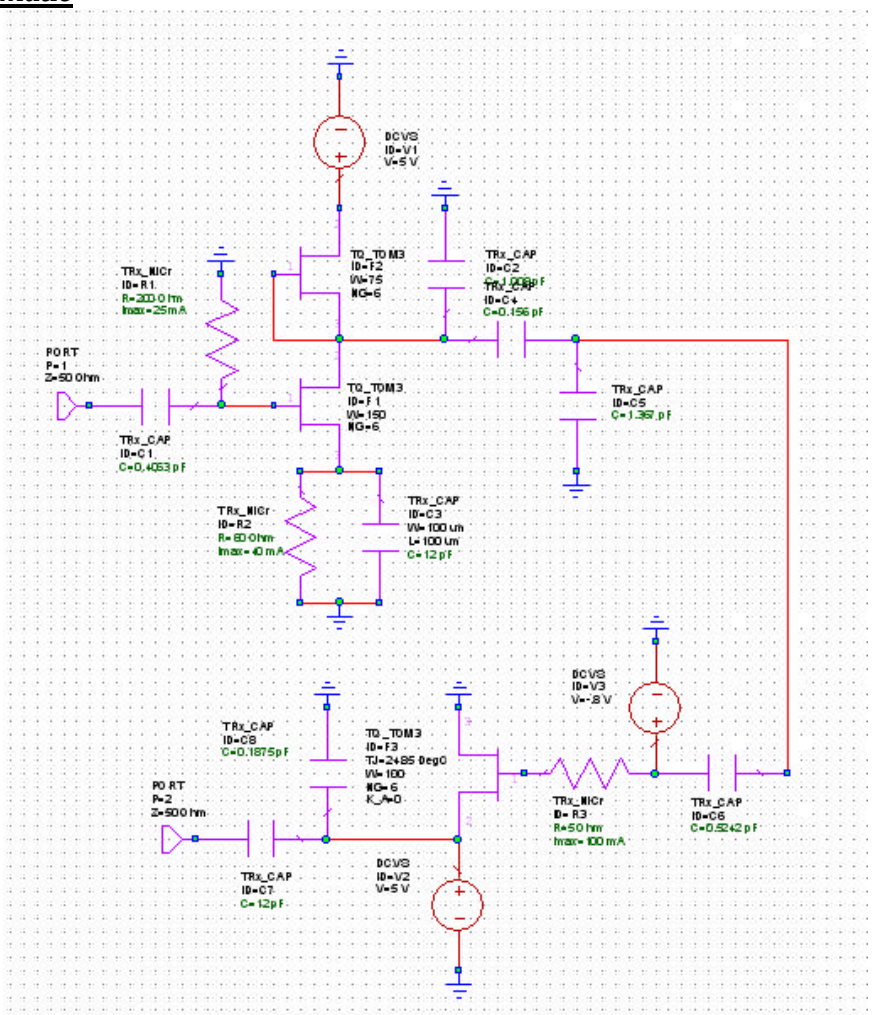
DC Analysis

Input Amplifier	
Vgate	1.53E-05
Vsource	1.78385
Vdrain	4.37505
Ids	22.2739

Output Amplifier	
Vgate	-0.7999
Vsource	0.00289
Vdrain	4.95069
Ids	91.2899

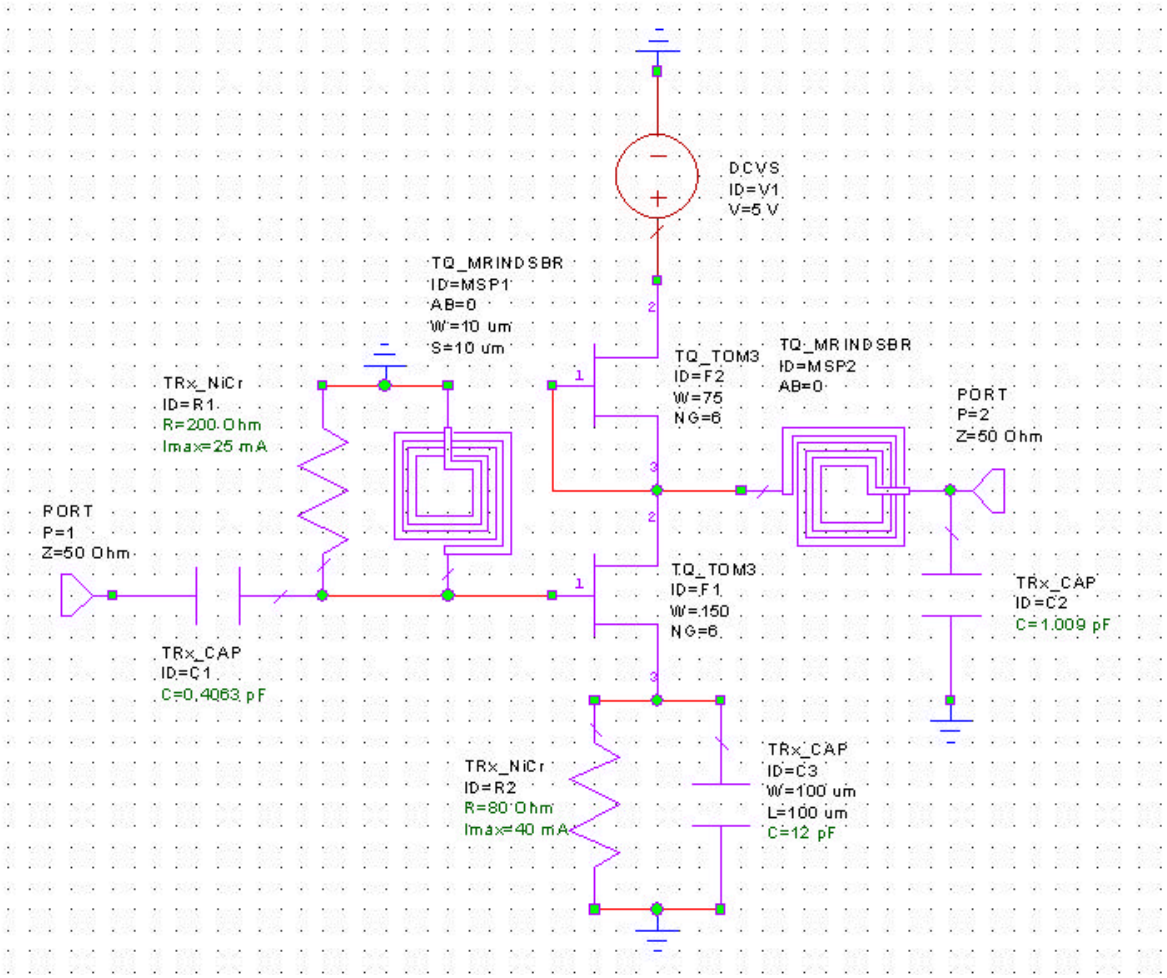
Schematics

DC Schematic

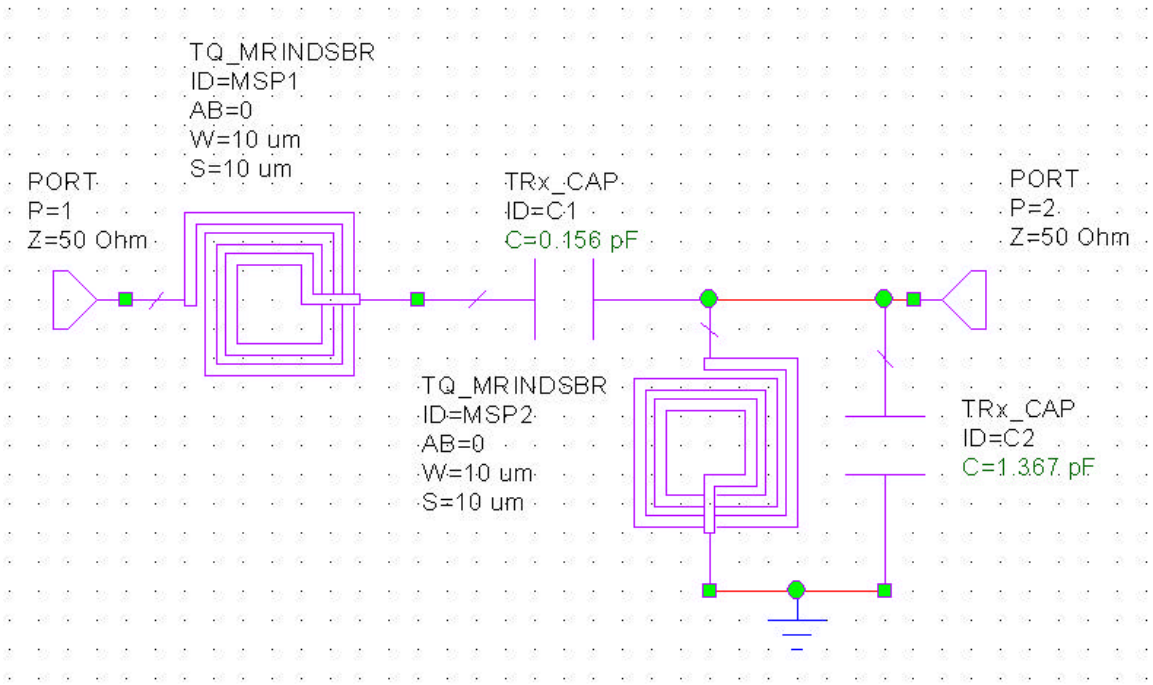


Above is the DC schematic of the entire S/C band Frequency Doubler. For simplicity all interconnect and inductors were replaced by wires.

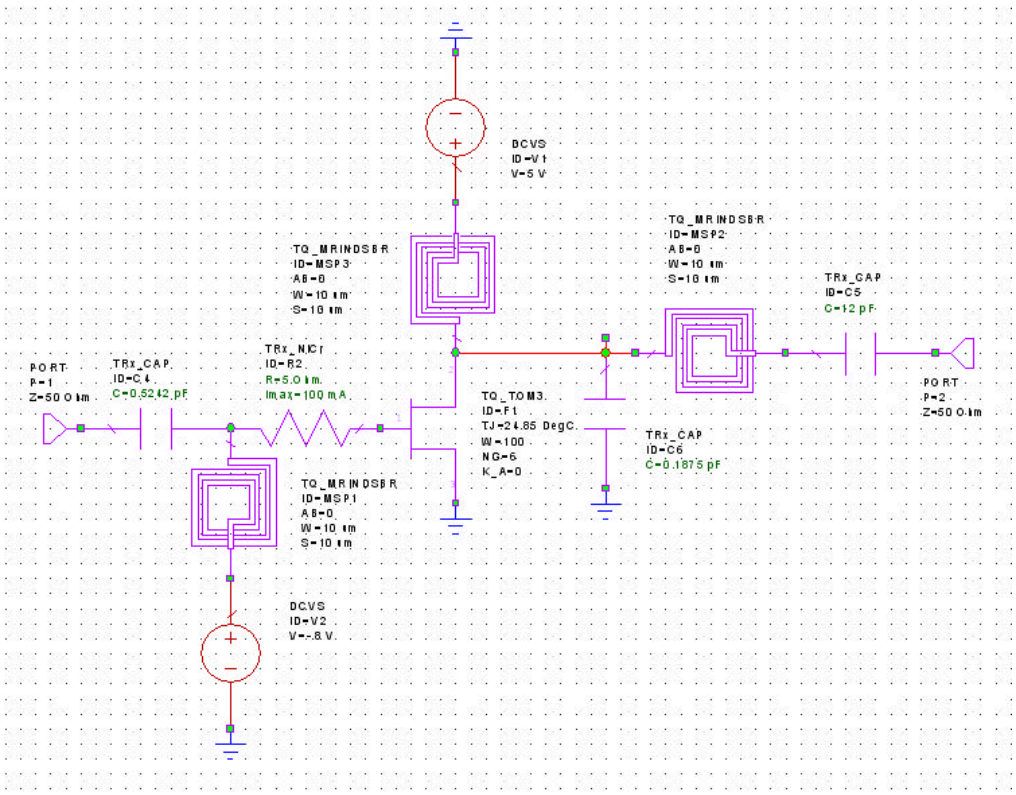
RF Schematics



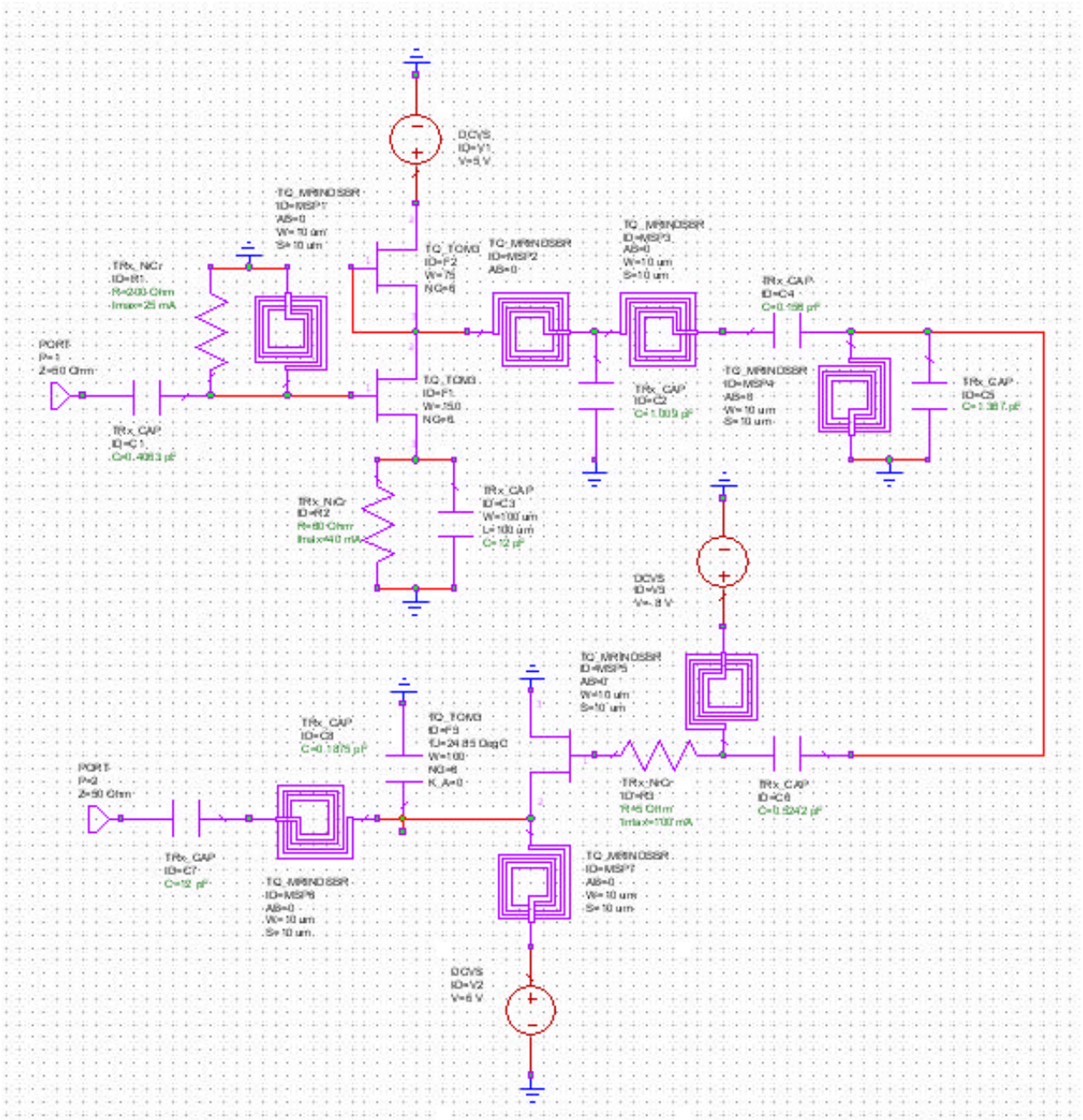
RF Schematic of the Input Amplifier that produces the 2nd Harmonic (interconnect not shown).



RF Schematic of the Butterworth Filter with N=2 (interconnect not shown).

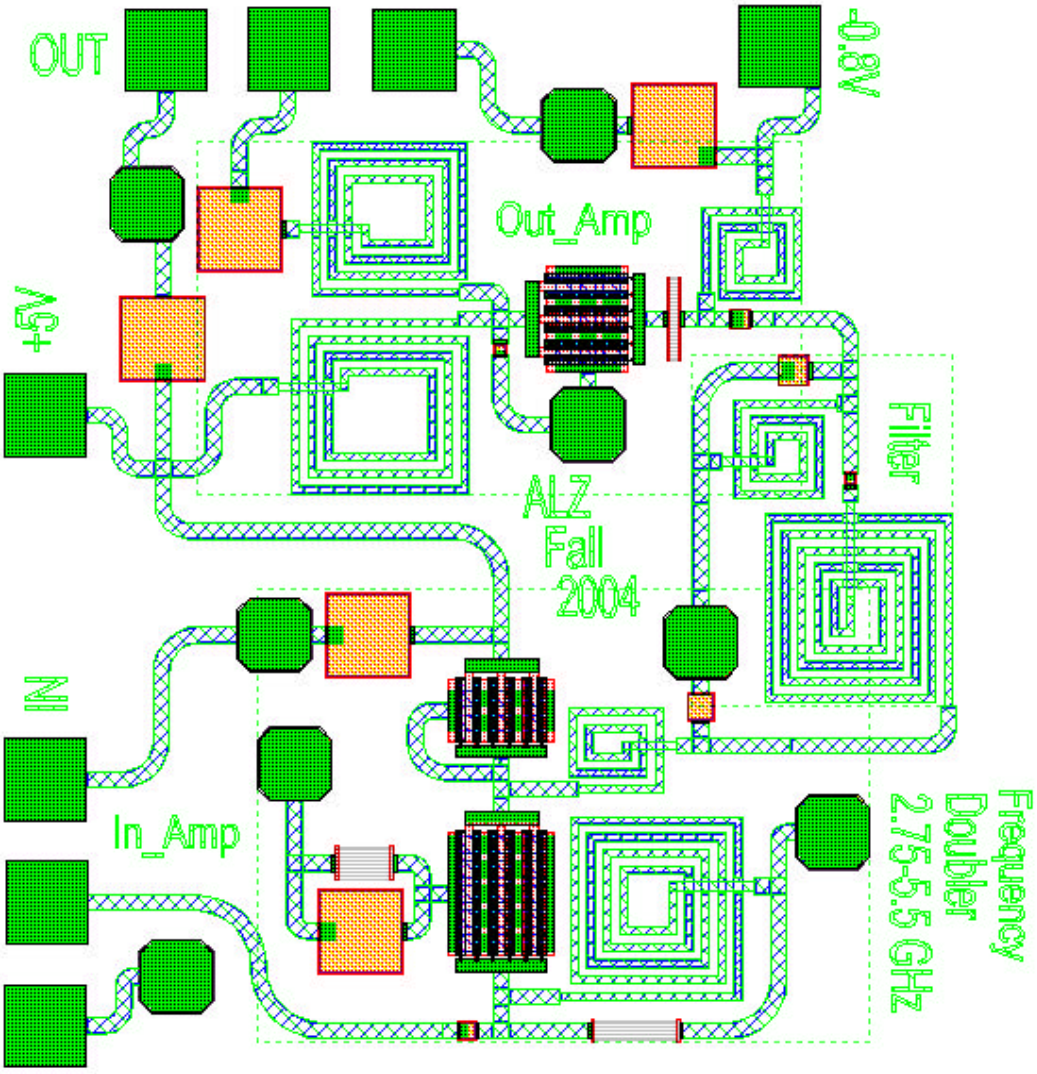


Above is the RF schematic of the Output Amplifier (interconnect not shown).



Above is the complete RF schematic of the S/C band Frequency Doubler (interconnect not shown).

Layout



The above diagram is the Final Layout of the S/C band Frequency Doubler.

Test Plan

Equipment Needed

- RF Signal Generator (2.7 – 2.8 GHz)
- Spectrum Analyzer (>= 6 GHz)/Attenuator may also be required to protect equipment
- 2 DC Voltage Sources (+5 V, -0.8 V)
- 2Needle Probes to connect DC bias
- 2 Ground-Signal-Ground probes to insert signal and measure output.

Procedure

1. Visual Inspection: Visually inspect the MMIC design to ensure that there are no obvious flaws in the chip, such as missing components or connections.
2. DC Bias Network: Connect DC Voltage sources and slowly increase the first source to 5V while checking the current draw. Then decrease the second source to –0.8 V again while checking the DC current draw.
3. Turn on the input signal at the center frequency, 2.75 GHz and 10 dBm, and measure the output at 5.5 GHz.
4. Sweep the input signal from 2.7125 to 2.8125 GHz and measure the output power of the second harmonic.
5. Sweep the input power from 5 dBm to 15 dBm, at 2.75 GHz and measure the output power at 5.5 GHz. If time permits also check the extremes (2.7125 GHz at 5 and 15 dBm, and 2.8125 GHz at 5 and 15 dBm).
6. If time permits connect the MMIC chip to a network analyzer and measure the input match from 2.7125 to 2.8125 GHz and the output match at 5.425 to 5.625 GHz.

Conclusion

Using the GFET biased near cut-off turned out to be a good way to generate the desired 2nd harmonic. Biased as mentioned above, the 2nd harmonic turned out to be only 3 dB below the resulting fundamental. Then using the filter, the fundamental and 3rd harmonics were attenuated further. A different filter design, possibly just increasing N to 3, would probably have resulted in fundamental rejection that better met the desired specifications. However this would have required finding room for another spiral inductor, which is the most space consuming component. Also, modifications of the output amplifier could be made to improve the output power. I was able to get approximately 12 dB of power gain through the final stage, but at least one more dB was needed to meet the specification. Overall the design went well, despite some stability problems with the final stage amp.

The layout went smoothly. There were few problems fitting the entire circuit on the 60x60 mil chip. However, most of the chip was filled, preventing further improvements this time around to improve the filter or to add another amplifier to increase the output power to the desired levels.

The Johns Hopkins University

Applied Physics Laboratory

Microwave Monolithic Integrated Circuit Design

Class # 525.787

Final Project: S-band VCO

By

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Adéyinka George

Abstract:

This paper describes the design of an S-band voltage controlled oscillator, VCO. The VCO is one of nine MMIC designs that make up an S-band transceiver. The design tool used for this project was Advanced Design System, ADS. The VCO's target of fabrication is TriQuint Semiconductor's Texas 0.6μm Gallium Arsenide fab. The target parameters for the S-band controlled oscillator include: a center frequency of 2762 MHz; a tuning range of +/- 50 MHz; minimum output power of +10dBm, desired output power of 13dBm; supply voltage of +/- 5 volts, desired supply voltage of +5 volts only, tuning voltage of 0-5 volts; output impedance 50 ohms, nominal; and sized to fit on the 60 X 60 mil TriQuint ANACHIP.

Introduction

A simplex MMIC transceiver implemented in the Triquint TQTRx process (4 mil thick GaAs) with simulation and layout in Agilent ADS has been designed for C-Band HyperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequency applications.

The system utilizes a C-Band Up-Down Converter with a 275MHz intermediate frequency (IF) that can be down-converted to baseband with a second 275MHz local oscillator (LO). The second LO is upconverted to the C-Band in TX mode and modulation can be introduced onto the second LO or through direct frequency modulation of the VCO in the transceiver. The dual band usage VCO with high side (HSLO/LSLO) injection to the mixer is specified for operation from 2712MHz to 2813MHz, which when doubled is between the WLAN and ISM frequencies.

Receive and transmit signals are routed by C-Band single-pole-double-throw (SPDT) switches. The receive chain consists of a cascaded low noise amplifier (LNA) and post amplifier. The transmit path employs a variable gain amplifier for level control and a driver amplifier preceding a 0.25 Watt power amplifier.

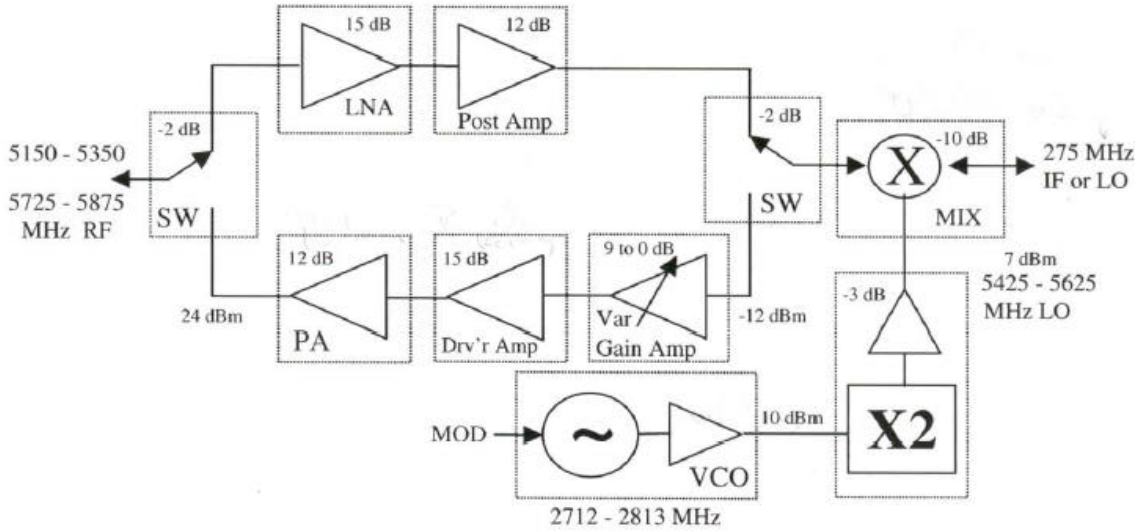


Figure 1. Chip-Set for the 5150 – 5350 MHz WLAN and 5725 – 5875 MHz ISM Bands.

Design Philosophy

The VCO architecture is based upon small negative impedance theory where the active circuit is represented by the impedance,

$$Z_a=R_a+jX_a$$

It can therefore be observed that

$$Z_l=R_l+jX_l$$

As shown in Fig. 3. Assuming that a steady state oscillation is occurring between the two networks then there must exist a loop current, I, that is non-zero. Using Kirchoff's law, the total loop voltage then must be zero which yields

$$Z_a + Z_l = 0.$$

It can therefore be observed that

$$Z_{a} = - Z_{l} \text{ (negative impedance)}$$

to ensure oscillation and hence the nomenclature of the theory and design technique. Furthermore, in small signal design, the imaginary portion of this relation is of particular interest and thus

$$X_a + X_l = 0$$

The large signal operation of the FET oscillator can then be predicted from its small signal characteristics since as the signal grows to steady state, the actual change of the imaginary portion of the active circuit is small.

The differential change in the active circuit impedance versus the operating point amplitude and frequency delta variations as described by Kurokawa is then,

$$[dR_a/dA][dX_l/d\omega] - [dR_l/d\omega][dX_a/dA] > 0$$

Where R_a is the active device's negative resistance, A is the steady state amplitude, and ? is the frequency. As stated earlier, the change in X_a with respect to amplitude is small and considered to be zero. However, for GaAs FET oscillators, R_a increases positively with respect to amplitude since the negative resistance of the circuit decreases in magnitude with increasing amplitude. Therefore applying these conditions, then

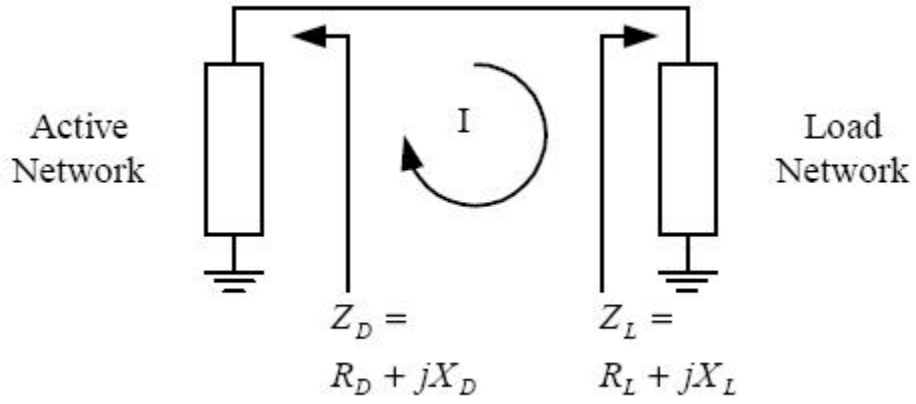
$$[dX_l/d\omega]_{\omega 0} > 0$$

which implies that stable oscillations are ensured when the reactive component of the load impedance has a positive slope versus frequency, and the frequency of the oscillation corresponds to the zero crossing of the frequency axis.

Additionally, it has been shown that for a series resonant oscillator that

$$|R_a| \sim\geq 3R_l$$

to approximate a power impedance match between the load circuit and the large signal steady state oscillations. The factor of 3 is itself a compromise based upon the experimental trade-off between start-up conditions and final oscillation frequency.



Design description

The VCO is powered by a 5 volt power supply. The 0 to -5 Volt voltage controlled oscillator operates from 2712-2813MHz with output power of 11.6 dBm. The VCO features a, W=100µm, N=6, TQTRx_GFET and was biased at the drain with 2 inductors for RF blocking. To destabilize the FET, we connect the FET to a series resistor to ground. Series source resistor provides a feedback path from drain current to gate voltage. To get MAXMP2 to be approximately 3, we adjust the source resistor. This feedback increases mainly the magnitude of the S_{12} parameter making the circuit more unstable (figure 1.1).

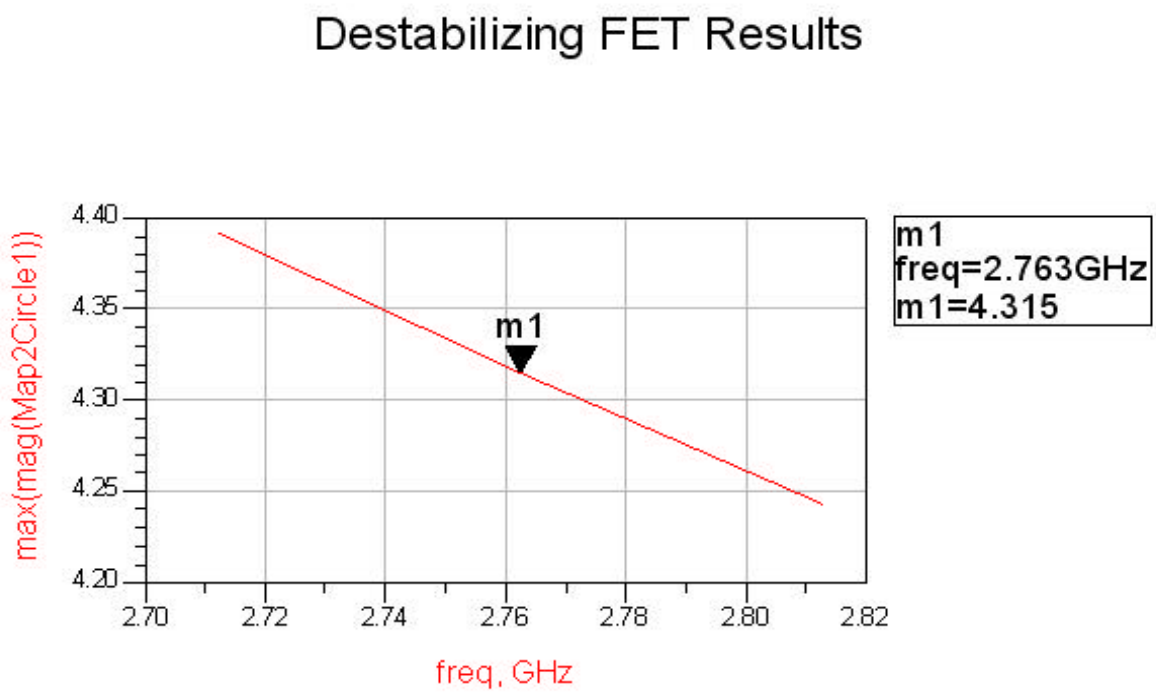


Figure 1.1

Now that the FET has been de-stabilized, the next step is to develop the necessary impedance for the active network. This was achieved by adding the input matching network which contained a varactor diode and lumped elements. The lumped elements were tuned such that the overall impedance of the active network has a negative real and imaginary part. This is illustrated in the figure below. Once the negative impedance of the active network is obtained, the next step is to develop the load network such that its impedance is the negative of the active network. This was obtained by first adding an inductor to the active network. The inductor was then tweaked such that the S_{11} and Z_{11} are totally resistive.

Schematic Prior to ¼ wave transformer

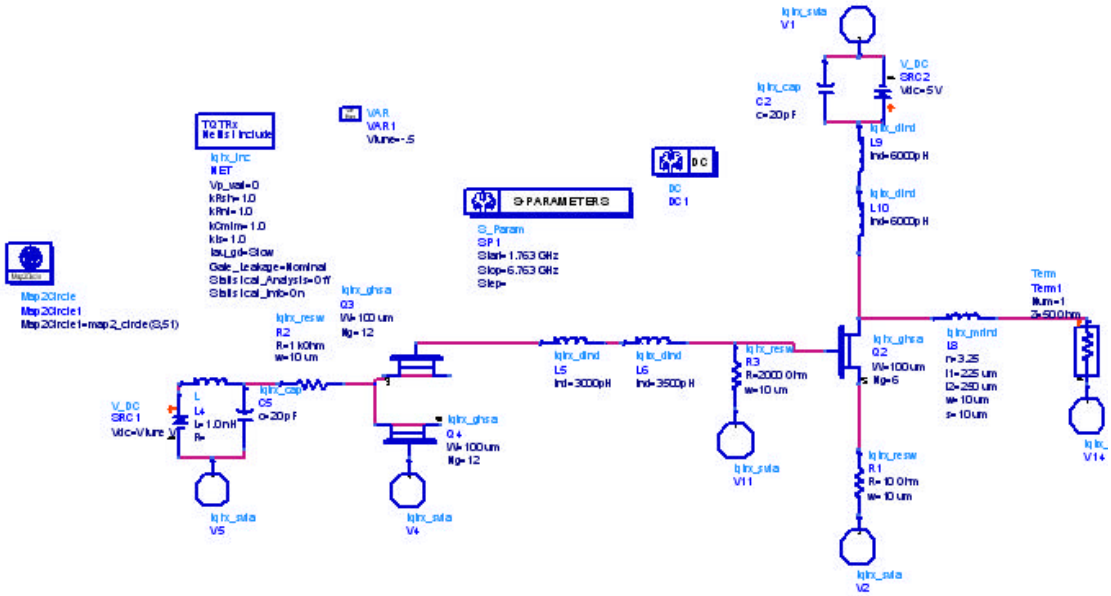


Figure 1.2

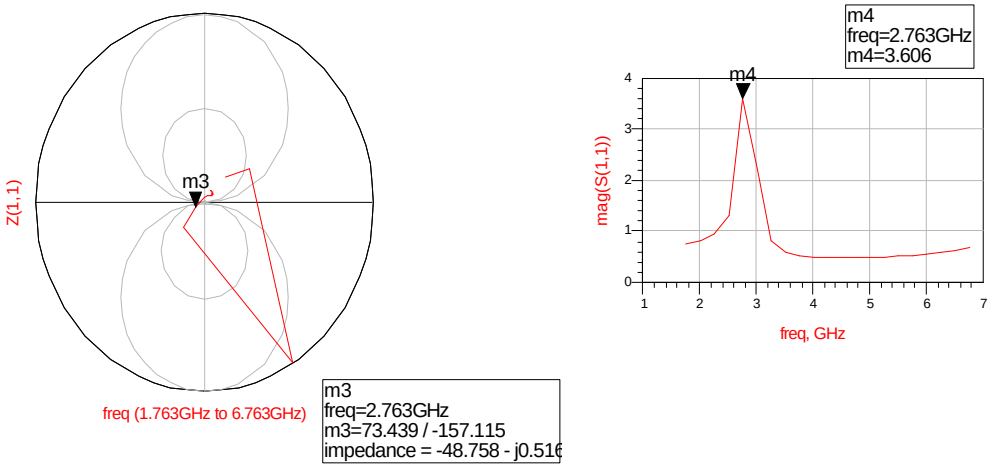


Figure 1.3

Once the reactive impedance of the active component was negated the next step was to transform the real impedance of the active network. This was achieved by using a ¼ wave transformer. The figure below shows how the start-up conditions was obtained comparing the impedance of the active network to the inductor and ¼ wave transformer.

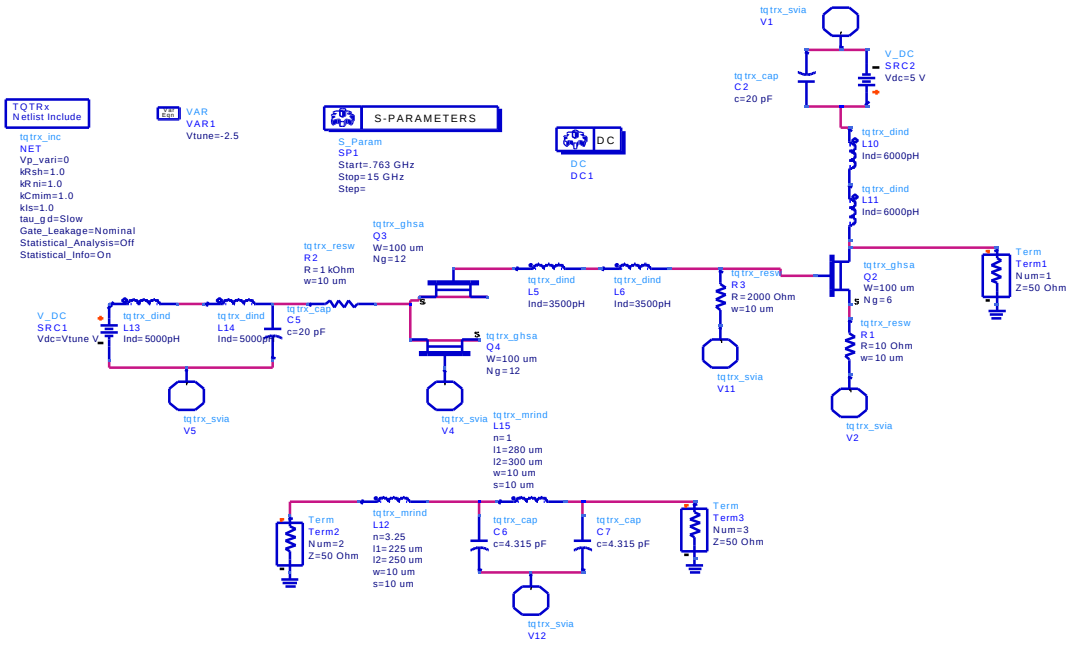
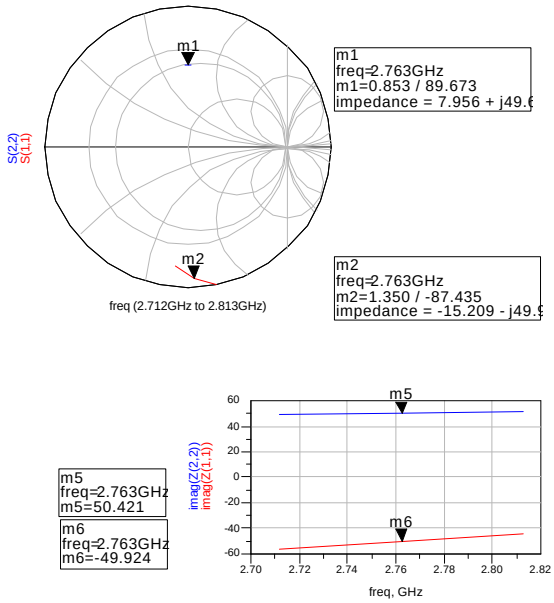


Figure 1.4



freq	Z(1,1)	Z(2,2)
2.712GHz	-22.007 - j56.459	4.511 + j48.915
2.763GHz	-15.209 - j49.924	4.628 + j50.421
2.813GHz	-9.245 - j44.410	4.761 + j51.962

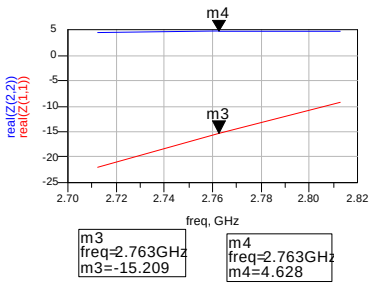
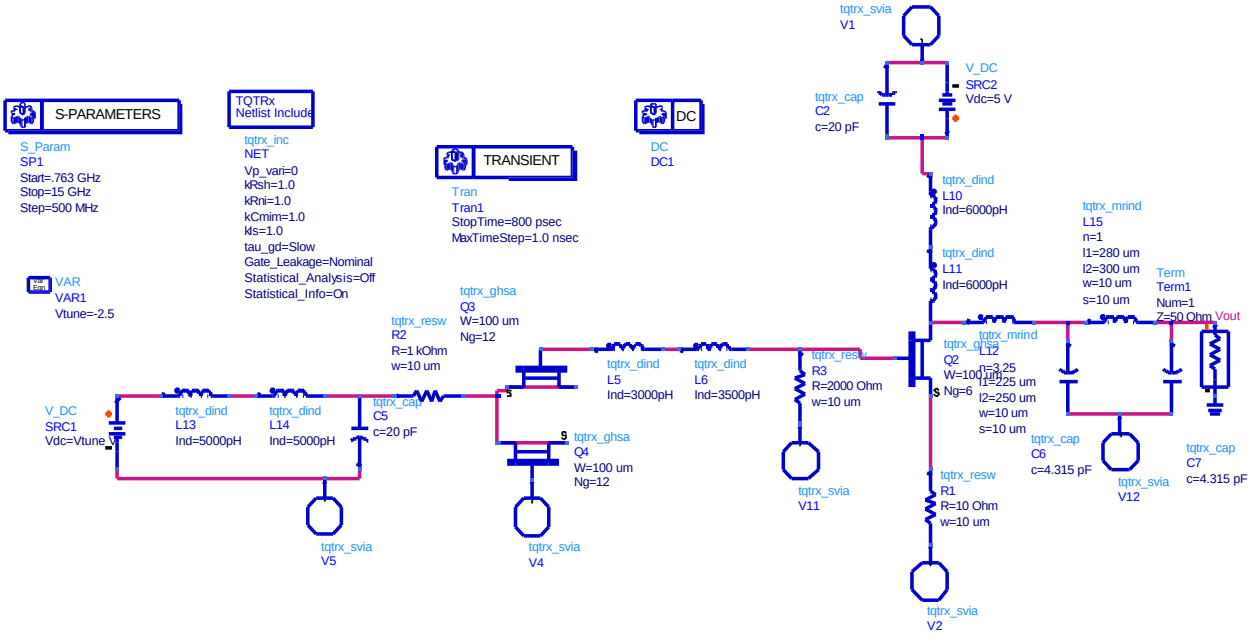


Figure 1.5


S-PARAMETERS
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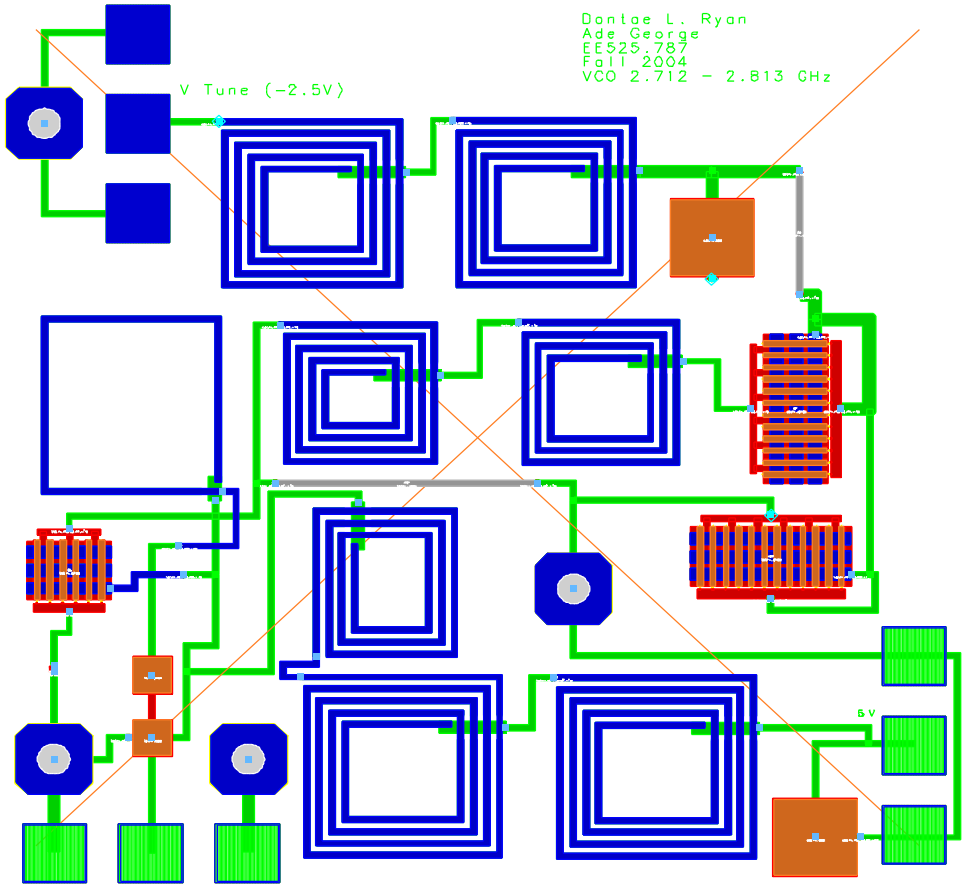
SP1
Start=.763 GHz
Stop=15 GHz
Step=500 MHz
TQTRx
Netlist Include
tqtrx_inc
NET
Vp_vari=0
kRsh=1.0
kRni=1.0
kCmim=1.0
kls=1.0
tau_gd=Slow
Gate_Leakage=Nominal
Statistical_Analysis=Off
Statistical_Info=On
TRANSIENT
Tran
Tran1
StopTime=800 psec
MaxTimeStep=1.0 nsec
DC
DC
DC1
VAR
VAR1
Vtune=-2.5
tqtrx_svia
V1
V_DC
SRC2
Vdc=5 V
tqtrx_cap
C2
c=20 pF
tqtrx_dind
L10
Ind=6000pH
tqtrx_dind
L11
Ind=6000pH
tqtrx_mrind
L15
n=1
l1=280 um
l2=300 um
w=10 um
s=10 um
Term
Term1
Num=1
Z=50 Ohm
Vout
tqtrx_ghsa
Q3
W=100 um
Ng=12
tqtrx_resw
R2
R=1 kOhm
w=10 um
tqtrx_dind
L5
Ind=3000pH
tqtrx_dind
L6
Ind=3500pH
tqtrx_resw
R3
R=2000 Ohm
w=10 um
tqtrx_mrind
L12
n=3.25
l1=225 um
l2=250 um
w=10 um
s=10 um
tqtrx_ghsa
Q2
W=100 um
Ng=6
V_DC
SRC1
Vdc=Vtune V
tqtrx_dind
L13
Ind=5000pH
tqtrx_dind
L14
Ind=5000pH
tqtrx_cap
C5
c=20 pF
tqtrx_ghsa
Q4
W=100 um
Ng=12
tqtrx_cap
C6
c=4.315 pF
tqtrx_cap
C7
c=4.315 pF
tqtrx_resw
R1
R=10 Ohm
w=10 um
tqtrx_svia
V5
tqtrx_svia
V4
tqtrx_svia
V11
tqtrx_svia
V12
tqtrx_svia
V2



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