

**Fall 2005 JHU EE787 MMIC Design Student Projects**  
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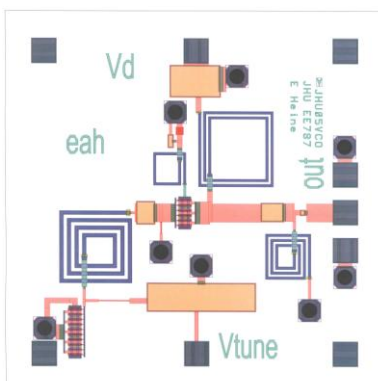
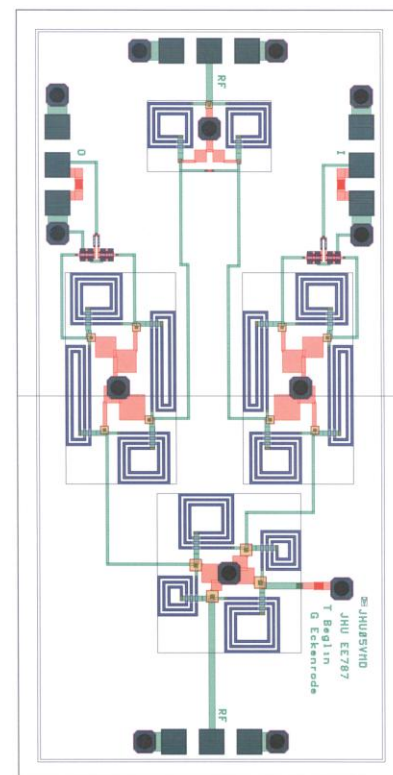
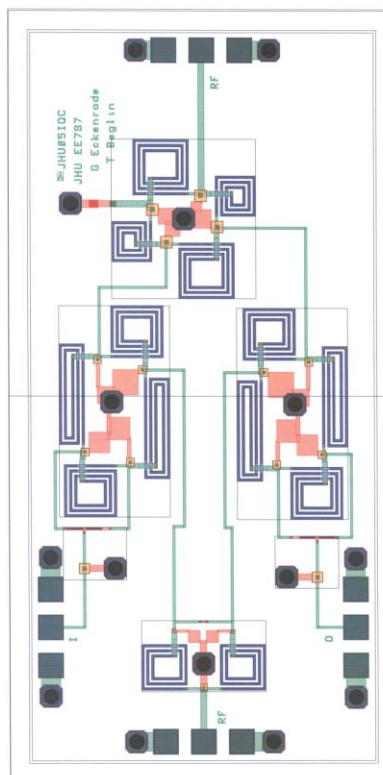
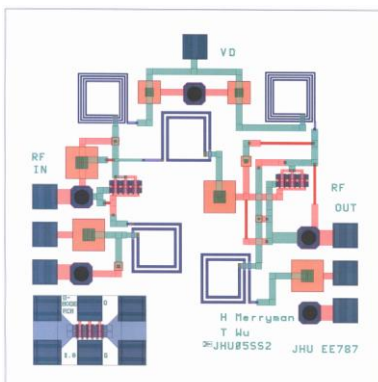
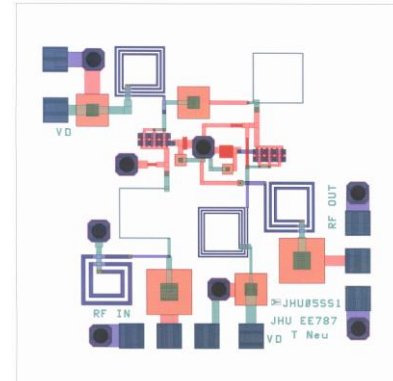
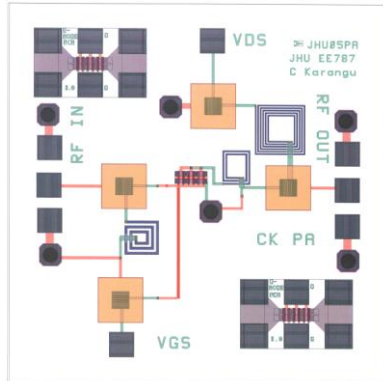
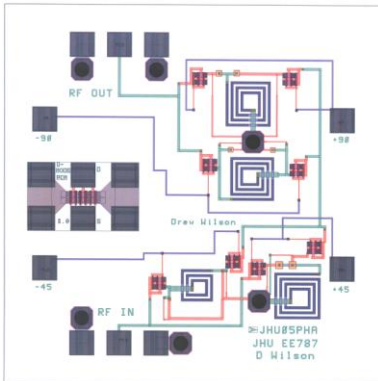
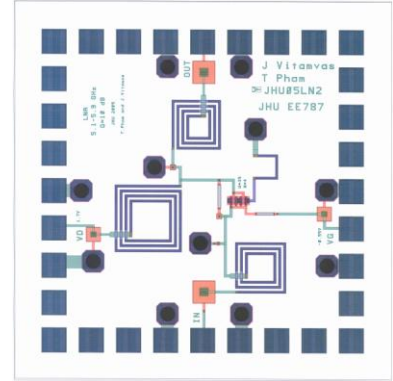
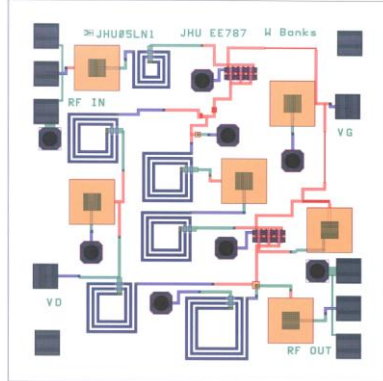
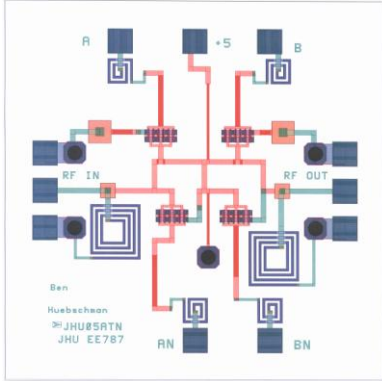
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Low Noise Amplifier - Wilart Banks

Phase Shifter – Drew Wilson

Power Amplifier – Caroline Karangu

Voltage Controlled Osc. - Ed Heine



# **Digitally Controlled C Band Attenuator**

By

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Microwave Monolithic Integrated Circuit (MMIC) Course  
Johns Hopkins University  
Fall 2005

## **Abstract**

A digitally controlled attenuator operating over a frequency band from 5150 MHz to 5875 MHz is described in this paper. The circuit was designed and modeled using the Advanced Design System (ADS) software package by Agilent. The design technique allowed for very precise selection of attenuation. The simulations of the circuit showed stable performance across a broad frequency band. A layout for a physical design was also completed as part of the project.

## Introduction

The description of this project will start with the list of specifications. I will then outline the designs considered for the project and the reason behind the one selected. The procedures used to finalize this design and implement the layout will be discussed. I will conclude with the simulation results and a plan for testing the circuit.

Numerous systems require precisely controlled power levels at different points in the system. One way to accomplish this is a variable attenuator. The specifications for the digital attenuator describe in this paper are shown below in Table 1.

FREQUENCY	5150 to 5875 MHz
BANDWIDTH	> 800 MHz
INSERTION LOSS	< 3 dB min IL (2 dB goal)
POWER HANDLING	> +10 dBm @ 1 dB compression
VSWR, 50 Ohm	< 1.5:1 input & output
SUPPLY VOLTAGE	$\pm$ 5 Volts
CONTROL	TTL
SIZE	60 x 60 mil ANACHIP

Table 1. Circuit Requirements

In addition to these listed requirements, the attenuation is required to range from 0 dB to 6dB in four 2 dB steps. It should be mentioned that the insertion loss of the system, which is a built in attenuation, will be added to the variable attenuation.

## Design Approach

Before discussing the mechanism for switching between attenuation levels, the method of attenuation must be looked at. A good attenuator should match perfectly to 50 Ohms and reduce the RF power by an arbitrary amount. Fortunately there are two well know designs for achieving these requirements shown in Figure 1.

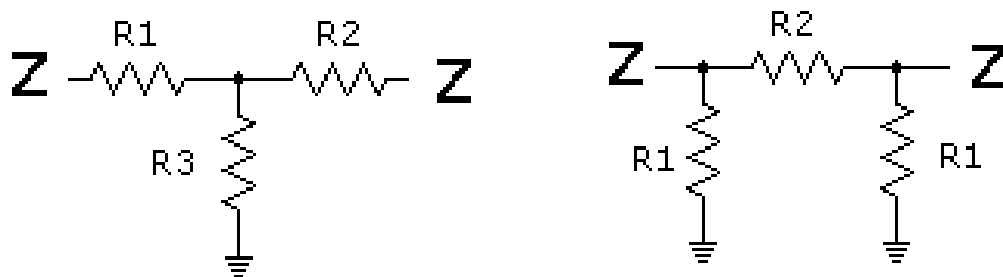


Figure 1. Designs for attenuators matched to 50 Ohms

The design on left was chosen because it requires only one via. These are the equations for determining R1, R2, and R3:

$$R1 = R2 = Z0 \frac{K-1}{K+1} \quad \text{Eqn. 1}$$

$$R3 = 2 * Z0 \frac{K}{K^2 - 1} \quad \text{Eqn. 2}$$

K is the attenuation level.

With the attenuator design we can move on to the method of control for the circuit. A number of designs were considered as possible mechanisms to allow for the switching between circuits. The first is shown in Figure 2. It is the most straight forward, but it also has a large number of components.

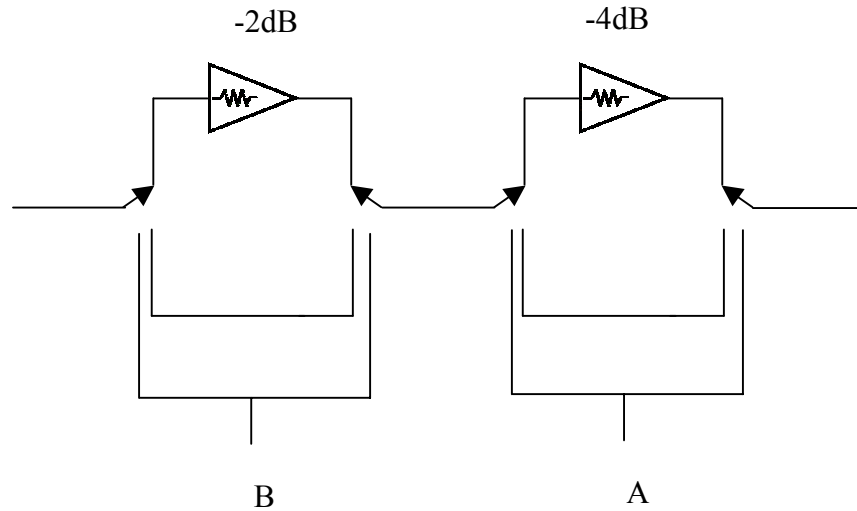


Figure 2. Possible designs for variable attenuator

Although this circuit might meet the requirements, it is needlessly complex and the large number of components could dissipate too much power to satisfy the insertion loss requirement. Figure 3 shows a much simpler design. Unfortunately, when the switch is closed, the 50 ohm line is in parallel with the attenuator. This has a resistance between one hundred and two hundred ohms. When put in parallel with the 50 ohm transmission line this results in an appreciable amount of attenuation. I was unable to meet the insertion loss requirements with this design.

This was overcome by inserting a switch between the attenuator and ground. The basic schematic for the switched is shown in Figure 4.

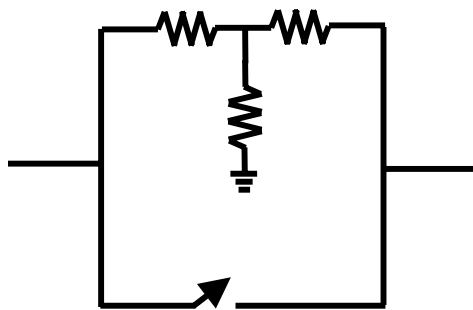


Figure 3. Simplified Circuit

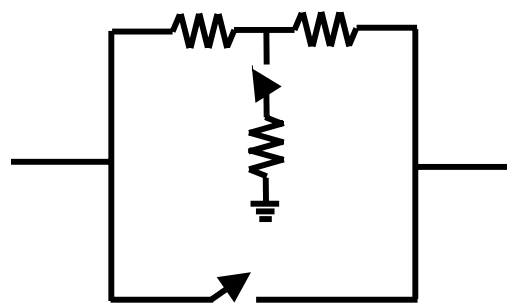


Figure 4. Final Attenuator

Prior to testing the circuit shown in Figure 3, the transistor was evaluated. The default transistor from the Triquint pallet showed low resistance, power handling over what is required by the circuit, and a small flat attenuation over the bandwidth of interest.

Using TTL logic, the on state has a minimum voltage of 2.0 V and the off state has a maximum voltage of 0.8 V. This means that there can be a maximum of 1.2 volts between the switch being open and into saturation. The circuit needs to perform well at these worst case values, and this performance cannot change significantly over the range of voltage allowed by the parameters of TTL logic. The transistor's S-parameters were measured at 0 volts and -1.2 volts. It turned out that it did perform well at the these values.

To meet all the requirements, the VSWR had to be made as small as possible. A simple two element matching network was added to the input and output. Blocking inductors were needed to isolate the gate from the RF line. A resistor that shifts the voltage into compliance levels for TTL was added. This elements are shown later in the report in the final circuit design.

The design and simulation of the circuit was an iterative process. The first simulation was done to verify the calculated values of the resistors. Several basic circuit layouts were simulated. The design gradually increased in complexity as more elements were added to comply with specifications. The next section will discuss the results of the simulation of the final circuit.

## Simulations

The circuit was simulated to determine its S-parameter characteristics in the four possible input states. The results of these simulations are shown below in Figure 4.

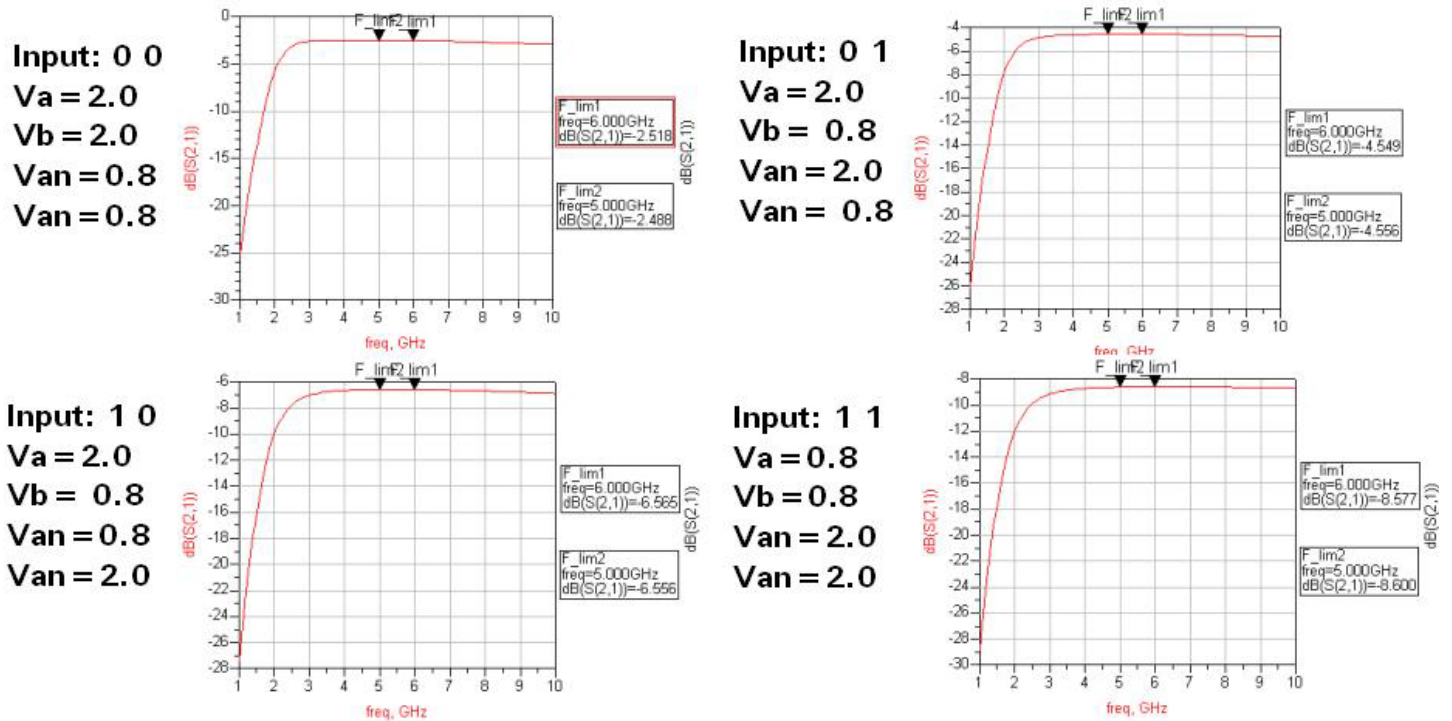


Figure 4. S-parameters of the attenuator in four logic states

As can be seen from this figure in the worst case scenario of voltages, the circuit easily meets the design specifications of four states separated by 2dB attenuation each. A typical value for the VSWR is shown in figure 5. The specifications call for a VSWR less than 1.5 which this circuit easily meets.

The final specification that has to be met is the power handling capabilities of the circuit.

The input RF power at 5.8 GHz was swept from a low value to 10 dBm. Figure 6 shows the results of this test.



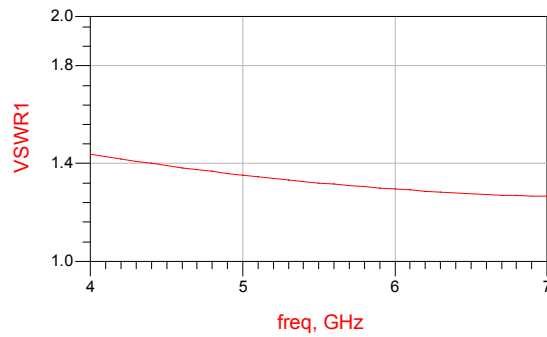


Figure 5. VSWR of the circuit

In figure 6, the linearity of the circuit begins to break down near the limit. It should be noted that the output power is plotted on the horizontal axis and that the input power should be increased by the attenuation level.

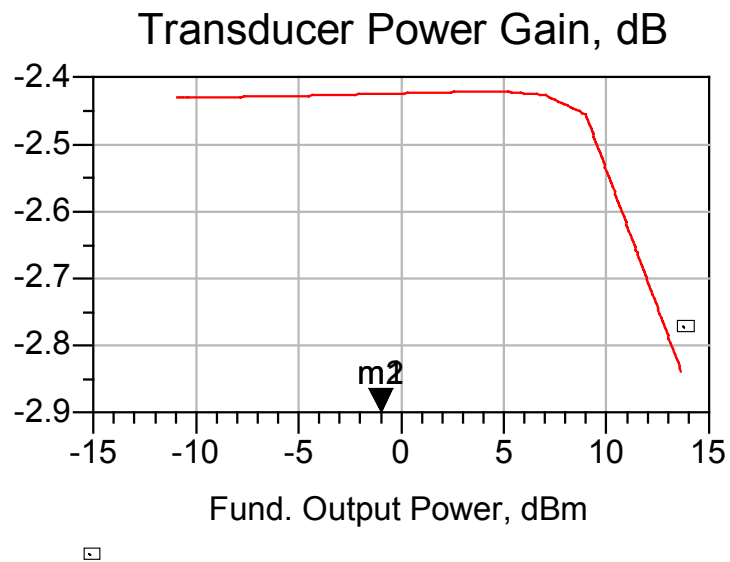


Figure 6. Power Sweep

The DC performance of the circuit was simulated. The circuit draws very little current. During the design, it became obvious that the voltage level of the circuit

would have to be shifted in order to allow it to be driven by TTL. The results of the DC simulation are shown in Figure 7.

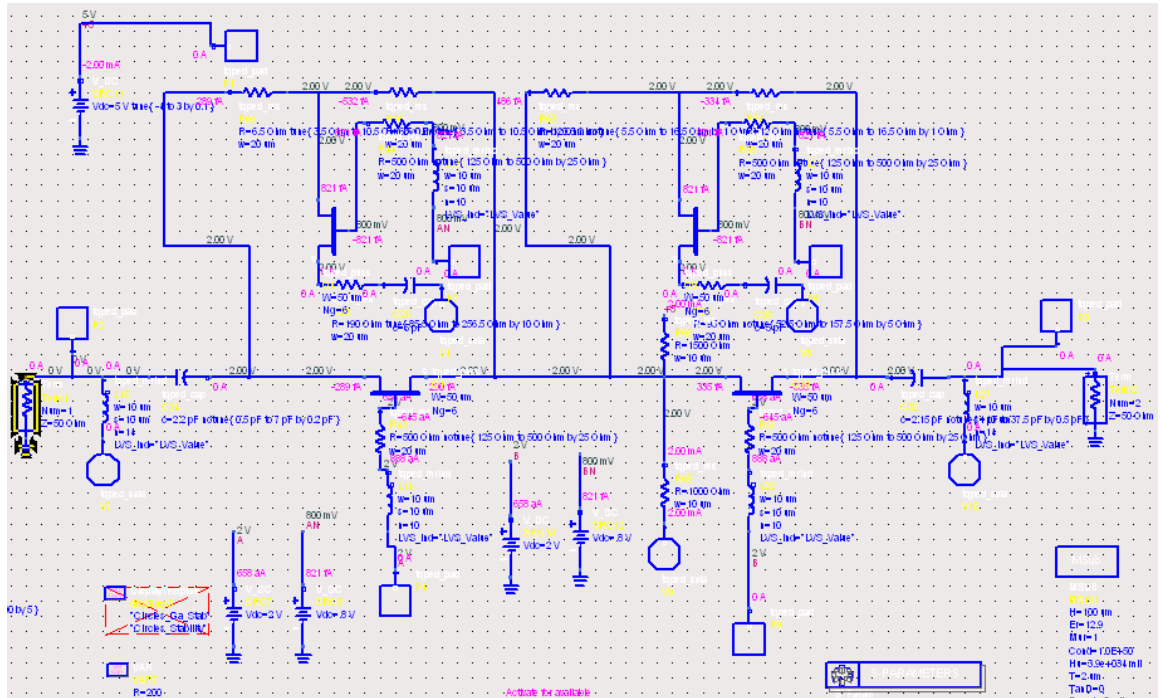


Figure 6. DC annotated Circuit layout.

The next section will discuss the components of the layout.

## Schematic

Figure 7 shows the annotated DC solution with the components of the circuit labeled.

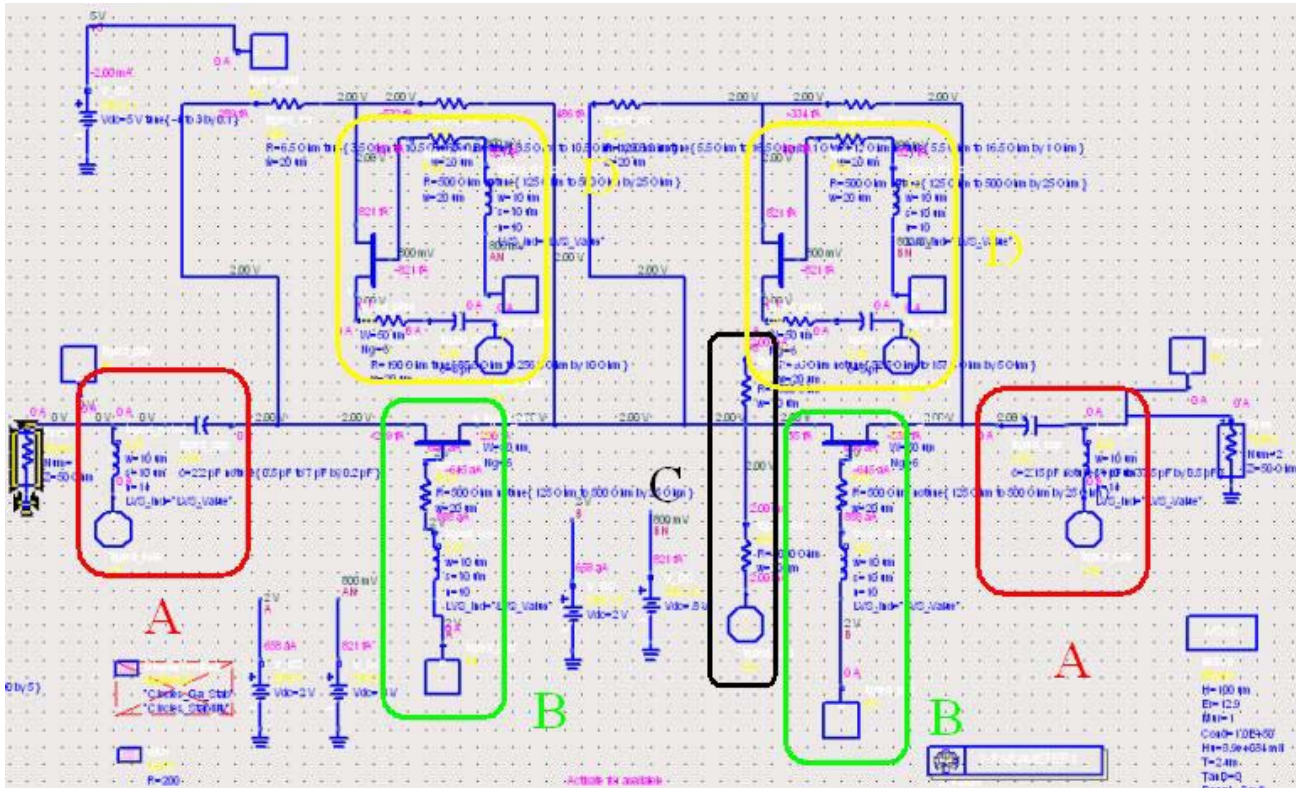


Figure 7. Annotated Layout of the circuit.

- A. Matching network
- B. Through switch and control pad
- C. Voltage shifter
- D. Attenuator switch and control pad

## Layout

Figure 8 shows layout of the circuit.

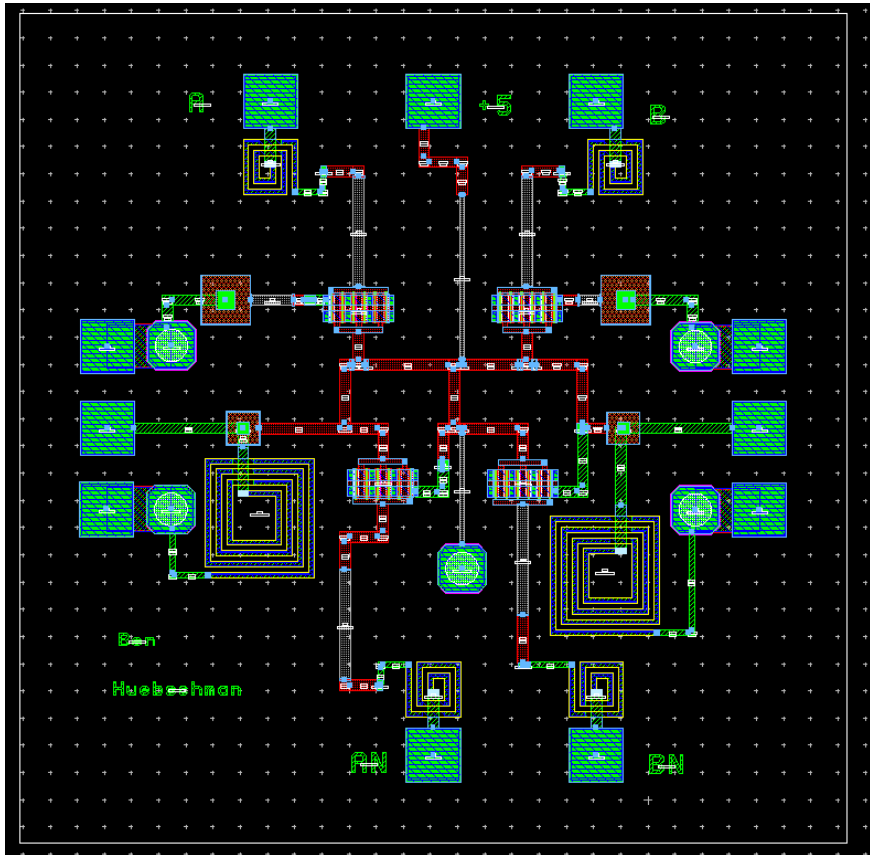


Figure 8. Circuit Layout

## **Test Plan**

To thoroughly test the circuit, we would need a vector network analyzer, a mechanism for measuring power, and DC power sources to bias the circuit. If we are just interested in validating the attenuation, the power measurement system is unnecessary. The test will begin by connect the DC bias and the network analyzer. S-parameters for each of the four logic states would be measured. From these we could extract attenuation and VSWR. To test the power response of the system, the vector network analyzer would have to be replaced by the power source at the desired frequency and a power meter. The power would then be increased until we began to observe changes in the attenuation.

## **Summary**

This paper describes the design procedure and layout of a digitally controlled variable attenuator. The circuit fulfills are design requirements and specifications. It consumes virtually no DC power. It uses as a power source a +5 V DC input, but this could be reduced to +2 V. The circuit could easily be redesigned to have any number of steps or an arbitrary attenuation level. As the voltage requirements for the transistors decreases, the required voltage of the DC power could be reduced appropriately. This basic design can be adapted to other attenuator requirements.

# C Band Low Noise Amplifier

Final Report

E525.787

Fall 2005

Students:

Trang Pham

John Vitamas

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## **Abstract**

The design described in this document is a C-band, low-power low noise amplifier (LNA). It has a DC power consumption of 6.34mW at 1.7V and 3.73mA drain bias. It is layed-out to use dual supplies to aid in-lab tweaking of the bias of the 140um depletion-mode FET. The LNA has an operating band of approximately 5.15GHz to 5.875GHz. Within this band the noise figure is less than 2.35dB. Gain is better than 8.5dB across the band with port match better than -15dB. The amplifier is unconditionally stable from near-DC to 10GHz. The amplifier layout is inserted into a 60 mil by 60 mil Anachip for ease of fabrication.

## **Introduction**

This LNA is designed the TriQuint TQPED process with vias. The LNA is part of the MMIC design class' duplex transceiver utilizing a receive array for the C-band HiperLAN wireless local area network (WLAN). It is one of nine unique MMIC designs which make up the C-band transceiver. Each design was to be contained on a 60 mil square die.

## **Circuit Description**

The LNA circuit design selected was a single-stage amplifier using a 35um x 4 (140um) depletion mode FET. A drain-gate resistor-capacitor feedback network was used to stabilize the amplifier and flatten the gain but restrict DC current flow from gate to drain. Dual sources are used to bias the amplifier. The DC sources are isolated from the RF network using on-chip inductors and filtering is provided by on-chip bypass capacitors.



## Design Philosophy and Design Tradeoffs

A single depletion mode FET was chosen because of the desire for an ultra-low-power amplifier with low noise figure. The goal was lower than 10mW of total DC power consumed with a secondary goal of 5mW. Better than 2.5dB noise figure was desired. The first cut design aimed for 5mW of total DC power while achieving 10dB of gain and an unconditionally stable circuit from DC to 10GHz.

The decision was made early on to not adopt a single-supply self-biased amplifier. The main reason for this is we suspected the design would be very sensitive to bias and process shifts and wanted the ability to tune in-lab to achieve best performance. Further iterations of this design could implement a self-bias scheme with a single supply to simplify integration.

The amplifier was designed to have a low noise figure and low DC power consumption. This dictates a very small device, which inherently will have low, narrow-band gain and be difficult to match (high VSWR). We mitigated this later in the design by bumping DC power slightly (by up-sizing the FET slightly) to improve VSWR. Initial designs showed high gain but very poor VSWR when using a drain-only resistive stabilization. A small series inductor on the FET source combined with an RC feedback stabilization network flattened gain (at the expense of peak gain) and achieved an unconditionally stable design.

The LNA is matched for optimum noise figure on the input side using an LC network. The output is matched for VSWR at 50 ohms using an LC network. Both networks are entirely on-chip and neither includes any DC paths to ground, maintaining a low-power operation.

Because this design was somewhat new, no hard specifications were provided so reasonable goals were set by the design team.

**Table 1 – Specification Matrix**

<b>Spec</b>	<b>Specification Goal</b>	<b>Layout Schematic</b>
<b>Frequency Bandwidth</b>	5150-5875	5150-5875
<b>Gain</b>	> 8dB	8.5dB minimum
<b>Gain Ripple</b>	+/- .5dB max	1.2dB
<b>VSWR, 50 ohm</b>	<1.5:1	<1.5:1, output < 1.78:1, input
<b>Supply Voltage</b>	None specified	Dual supplies
<b>Noise Figure</b>	< 2.5dB	< 2.32 dB
<b>DC Power</b>	<10 mW	6.34mW

## Predicted RF Performance

The following plots show the predicted performance of the amplifier as layed-out including interconnect, bond pads and bond wires to connect to external supplies. Performance is expected to be slightly better if the RF pads are probed using G-S-G probes and efforts are made to keep inductance to a minimum.

**Figure 1 – Noise Figure**

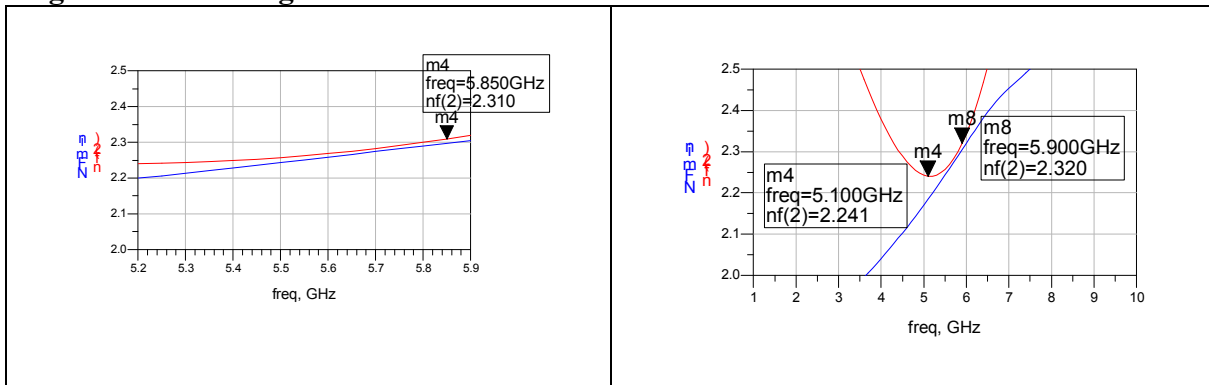


Figure 2a – S-parameters

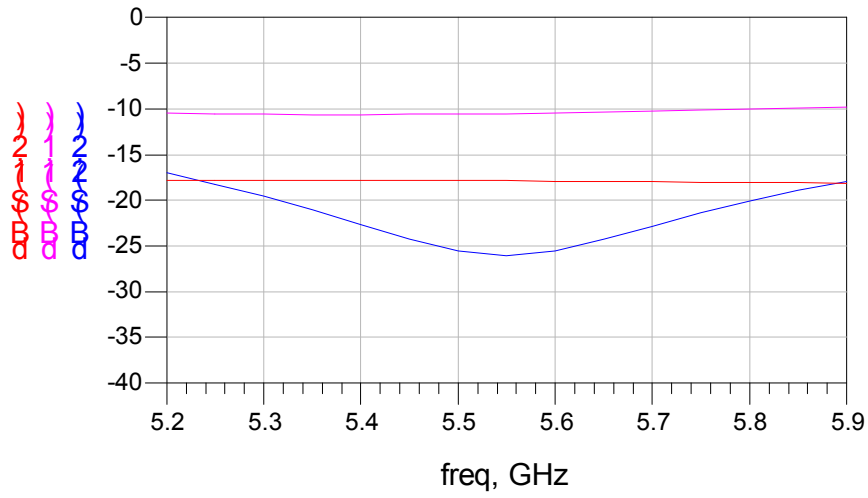


Figure 2b – S-parameters expanded

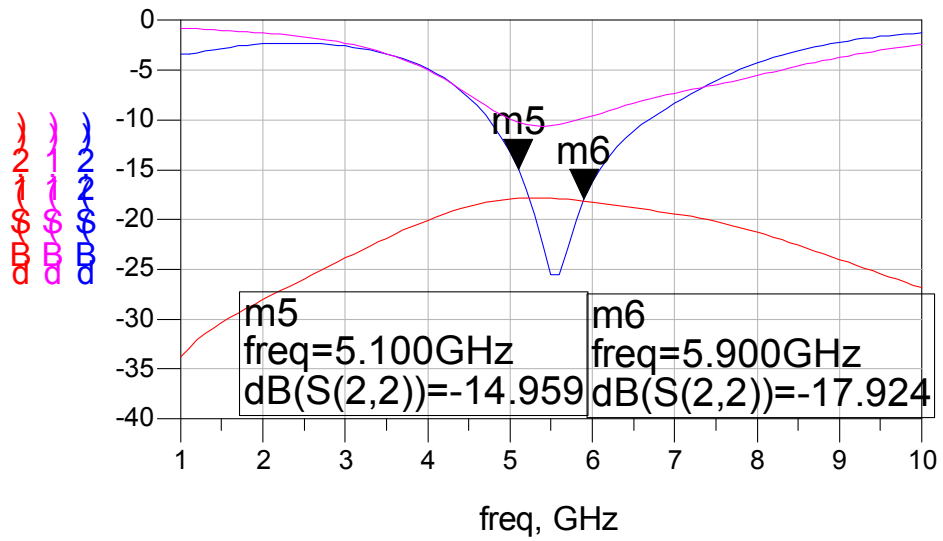


Figure 3a – In-band Gain

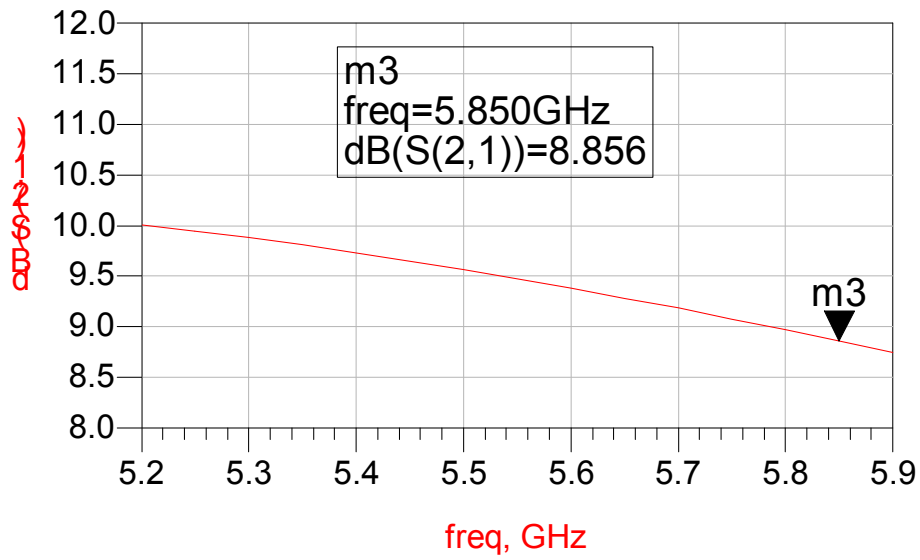
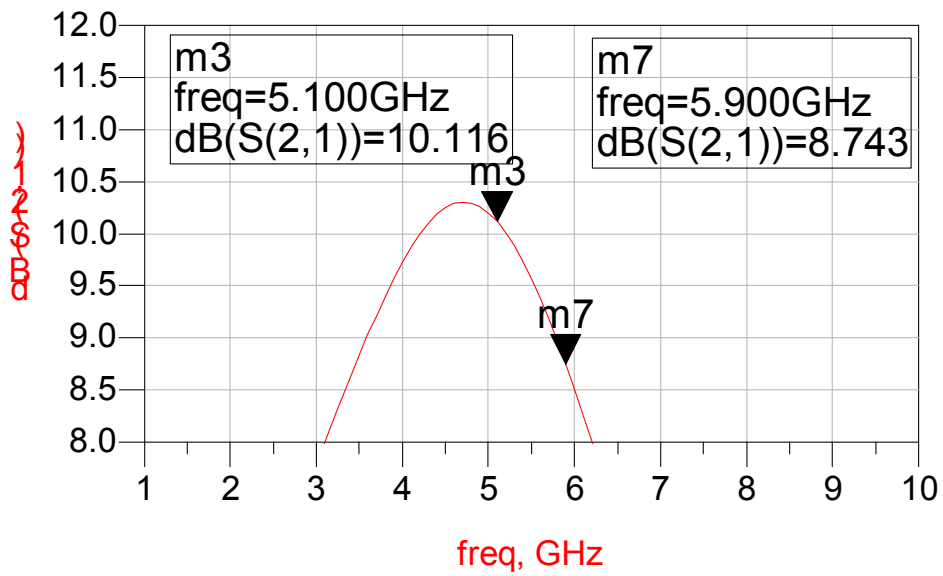
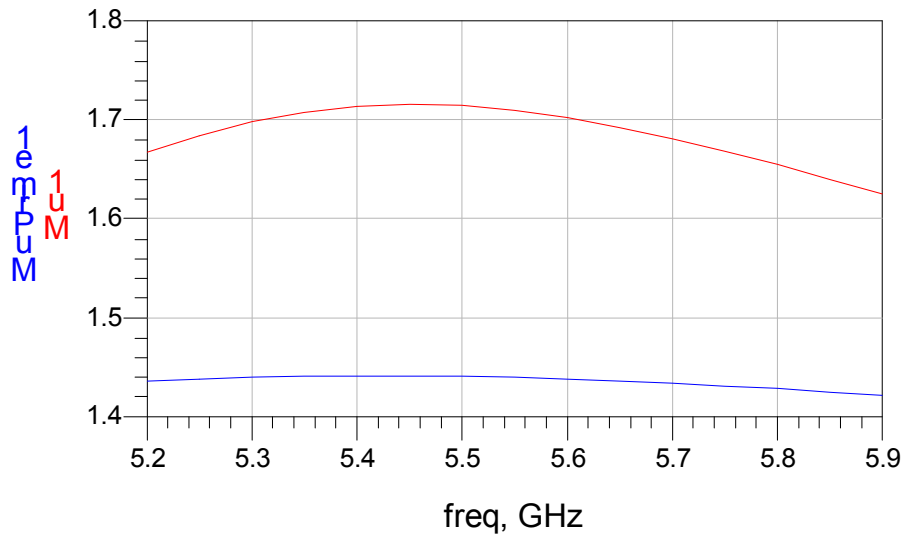


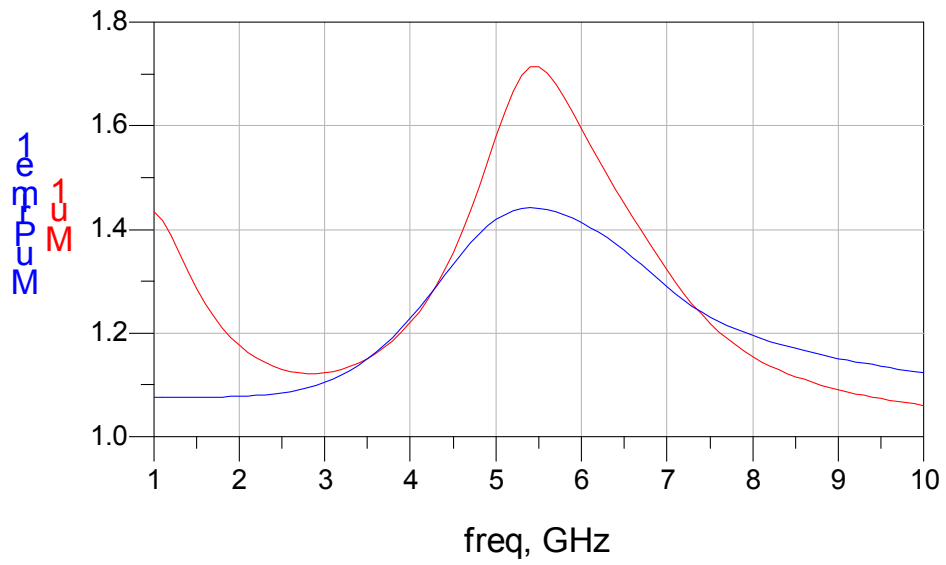
Figure 3b – Gain expanded



**Figure 4a – In-band Stability**

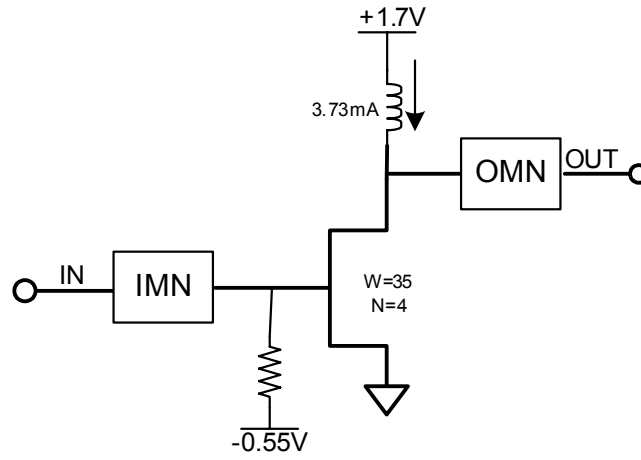


**Figure 4b – Stability expanded**



## Schematic Diagrams

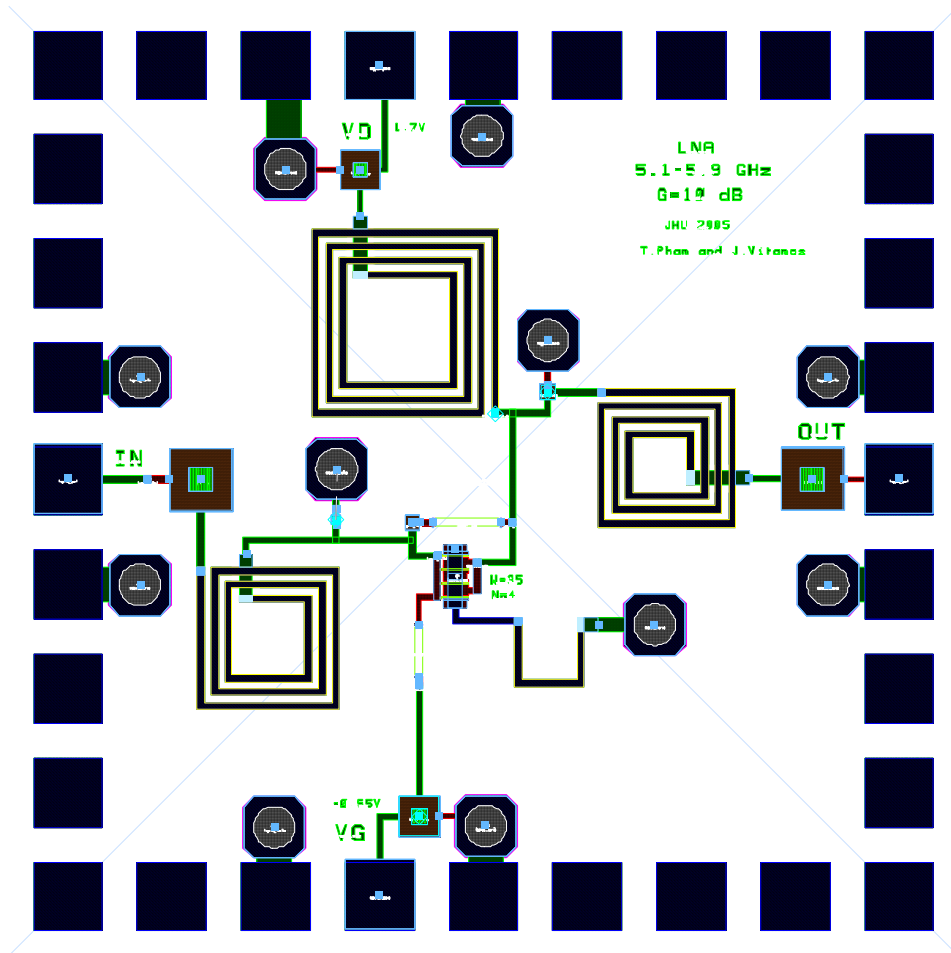
The following pages illustrate the simplified design schematics used for this LNA. They do not include interconnect for simplicity's sake.





## Final Layout

Final layout of the LNA was fixed perfect into Anachip and using TriQuint components.





## Test Plan

- Ground procedure: The signal ground, test equipment and DC ground shall be electrically connected in the test station.
- Voltage Requirement: All test voltages shall be measured with respect to signal ground unless otherwise specified.
- Test equipment: The following test equipment will be needed to fully characterize the LNA design.
  - Agilent Network Analyzer (or comparable 2-port VNA)
  - Signal Generators
  - Digital DC Power Supply (two)
  - Spectrum Analyzer
  - Agilent Power Meter
- Turn On Procedure:
  - Set Gate power supply to -2VDC.
  - Set Drain power supply to 1.7VDC.
  - While measuring drain current, bring gate voltage more positive.
  - Desired drive current is 3.83mA which should correspond to a gate voltage of approximately -0.55VDC.
  - Apply RF power to the device
- SS measurement:
  - Perform a full calibration on the network analyzer from 1 to 10GHz
  - Apply the DC power supply and record the DC current of device.
  - Measure S11, S22 and S21 of the LNA and store the data. Set frequency from 1GHz to 10GHz Step of 0.4GHz; input power -10dBm
  - Turn off power supply when finished
- Noise Figure Measurement:
  - Perform a calibration on the noise figure meter at 5.5 GHz.
  - Connect the input probe to the RF IN pad.
  - Connect the output probe to the RF OUT pad.
  - Apply bias and
  - Perform the Turn On Procedure.
  - Measure the noise figure of the LNA and store the measurement data.
  - Turn off power supply.

Compare the result with simulation data and record it.

## **Summary and conclusion**

We have completed the design, simulation and layout of a C-Band low-power LNA. Power consumption is 6.34mW. Expected noise figure is less than 2.32dB across the band of operation. Output VSWR is better than 1.5:1. Gain is better than 8.5dB across the band. The design has passed layout versus schematic (LVS) checks and passes a design rule check (DRC). Our primary compromise was trading VSWR and small-signal gain for low power operation while still maintaining a low noise figure.

# **C-Band SSA (Small Signal Amplifier)**

**Tom Wu  
Heather Merryman**

**Microwave Monolithic Integrated Circuit (MMIC)  
Design Class**

**Johns Hopkins University  
Fall 2005**

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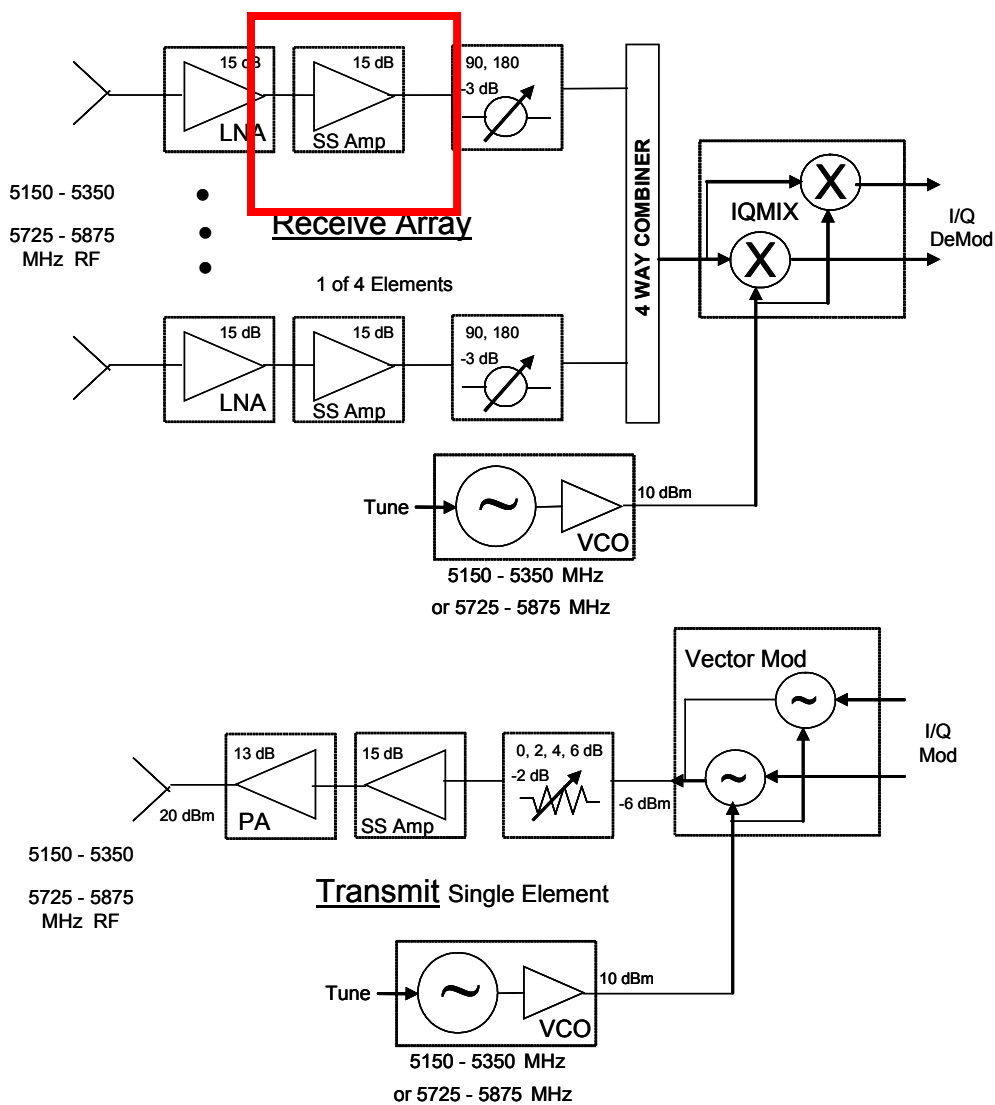
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## ABSTRACT

This paper describes the design of a small signal amplifier (SSA). The SSA operating at 5150 to 5875 MHz has been designed as part of a project for the MMIC design course at the Johns Hopkins University. This amplifier is part of a C-band duplex transceiver system for use in various industrial, scientific, and medical frequencies. Agilent's Advanced Design System (ADS) software was used to model and simulate the SSA, which is laid out on a 60 mil square ANACHIP die according to TriQuint's TQPED process.

## 1.0 INTRODUCTION

This paper illustrates the design methodology, the simulation results, the layout, and the test plan for the small signal amplifier. The small signal amplifier is a cascaded two stage amplifier to provide signal amplification across an 800MHz bandwidth. The circuit utilizes two 300um DFETs (6 fingers x 50um). The stages are biased by a single +5V supply. Matching networks are created to ensure the maximum power is transferred through each amplifier. The single supply voltage enables a self-biasing technique for easier testing of the MMIC chip.



Chip Set for the 5150 - 5350 MHz WLAN and  
5725 - 5875 MHz ISM Bands

## 2.0 DESIGN

### 2.1 Design Approach

Using the self-bias technique, the design decision to tie the amplifiers' source to ground allowed the usage of only a single bias at the drain and have a less number of components at the source for layout purposes. The following chart summarizes the bias levels and currents.

Parameter		Value
Stage 1	Vgs (mV)	< -10
	Vds (V)	4.82
	Ids (mA)	67.6
Stage 2	Vgs (mV)	< -10
	Vds (V)	4.81
	Ids (mA)	67.6

The initial design approach was geared towards meeting the gain. Each amplifier was conjugately matched to insure maximum power transfer. The matching networks for the input and the output were conjugately matched based on the s-parameters of the amplifier. The interstage matching network between the amplifiers was initially composed of four passive components to ensure the maximum power output. This did not present a major challenge, thus allowing the designers to focus on matching the two amplifier stages (implementing only ideal components). After the input match for the first amplifier and the output match for the second amplifier were established, the inter-stage matching network was defined, again, using ideal elements. The input, output, and interstage matching networks are composed of simple series inductor and shunt capacitors. After the input/output VSWR was satisfied, the stabilizing resistors were installed and tuned to provide unconditional circuit stability from 50 – 10000 MHz. There is a set of shunt resistors at the gate and drain of each of the two stages. To satisfy the gain ripple requirement, a feedback network was applied between the drain and gate of the second stage.

After the ideal element design was simulated to show maximum compliance, real components were installed to replace the ideally modeled inductors, capacitors, resistors, and grounds. The design was simulated again, and as expected, the changes in the performance of the SSA caused another iteration of component tuning. After the performance was optimized, the components were laid out in the ANACHIP model, allowing microstrip interconnects to be added.

The layout process proved to be a delicate and iterative task. After interconnects were installed in the model, simulation results warranted changes in passive component parameters, like the number of inductor turns and repositioning of other interconnects and components. After multiple rounds of layout and component optimizations, a favorable compromise was achieved in the layout that provided a design that now meets the requirements in all the critical parameters of gain, bandwidth, input/output VSWR, single supply biasing, and packaging.

## 2.2 Requirements

The table below shows the system requirements and compliance matrix.

Parameter	Specification		Expected Performance
	Desired	Goal	
Frequency (MHz)	5150-5875		
Min Bandwidth (MHz)	800		
Min Gain (dB)	15	16	19
Max Gain ripple (dB)	0.5		1.2
Noise (dB)	NA		5.4
Min OIP3 (dBm)	20		32
Max input/output VSWR	1.5:1.0		1.49:1.0
Supply Voltage (V)	+/-5	+5	+5
Size/Packaging	60 mil ANACHIP square		

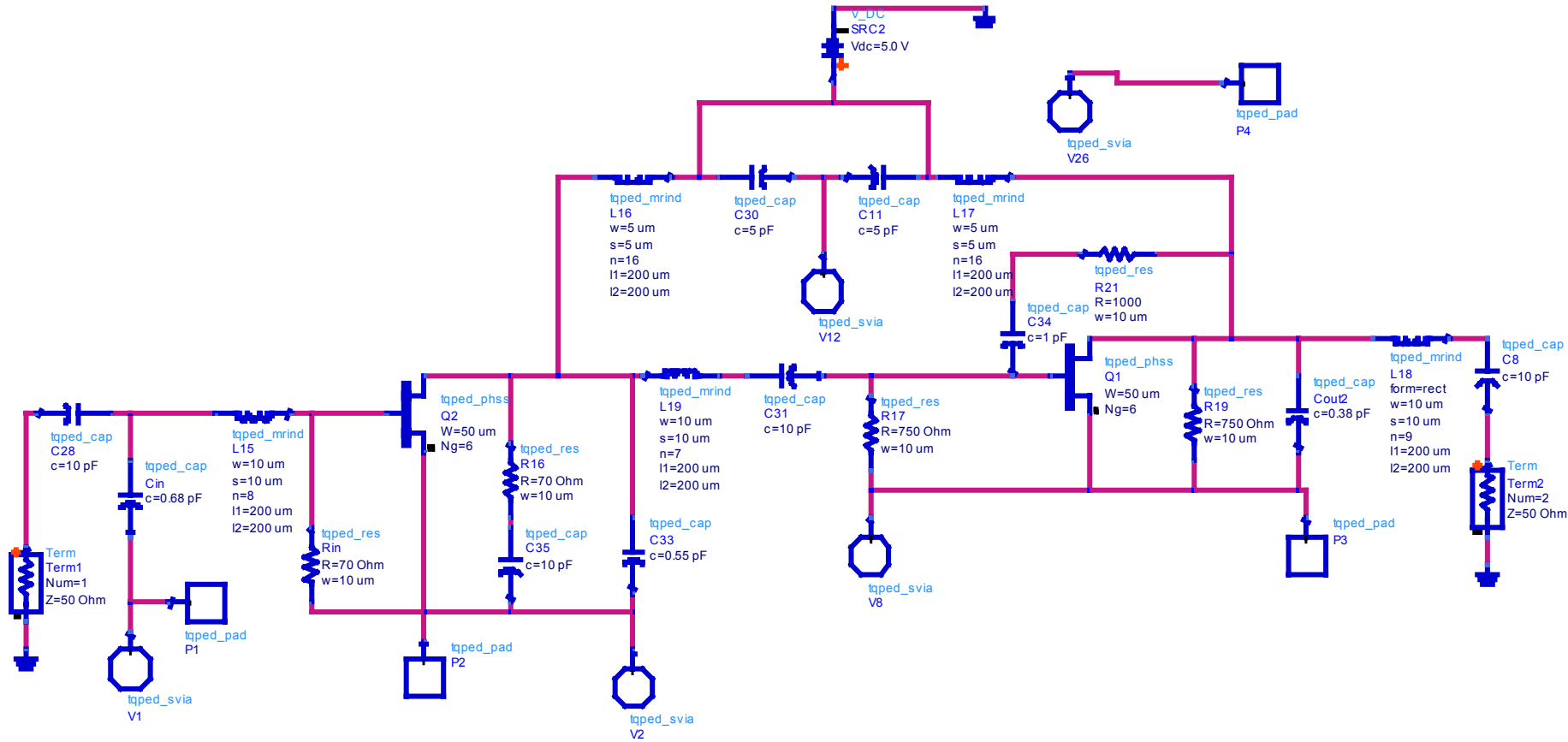
## 2.3 Tradeoffs – points of optimization

The primary tradeoff during the design process was in optimizing the gain ripple. The feedback network was optimized repeatedly to achieve the least amount of ripple over the 5150 – 5875 MHz bandwidth, but was still deficient in meeting the specification. Since the gain performance proved to be more than adequate, we were able to trade gain for gain ripple. The original gain ripple performance was > 2dB, but through optimization, gain ripple was quietly reduced to a minimum of 1.2dB over the operating bandwidth.

The layout was optimized to withstand the current from the 5V power supply. The PHEMT traces according to the TriQuint libraries were routed on layer Metal 0. The Metal 0 traces can only withstand 1.5mA/um. Our initial layout had too much current draw on the amplifiers' source connection to ground (about 200mA). A capacitor was placed in between the source resistor 0and the ground for the first stage amplifier to decrease the current through that path. Additionally, the PHEMT connections off each of the amplifiers were upgraded to a Metal 1 connection using a metal 0 – metal 1 via. The Metal 1 traces allow for more current handling at 9mA/um.

### 3.0 CIRCUIT - SCHEMATIC

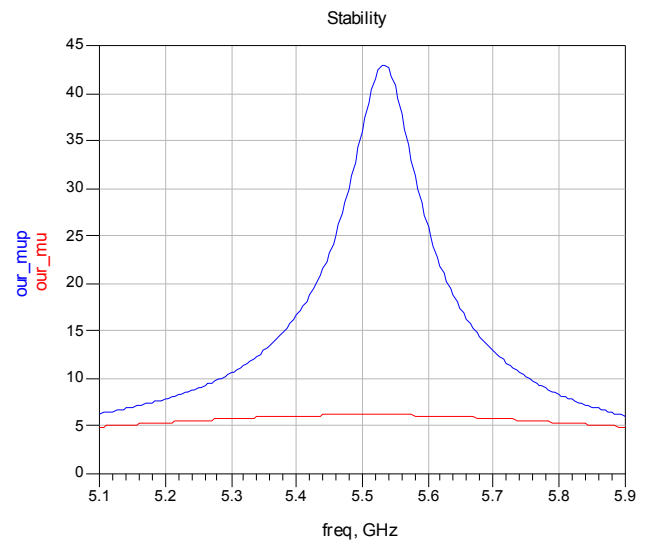
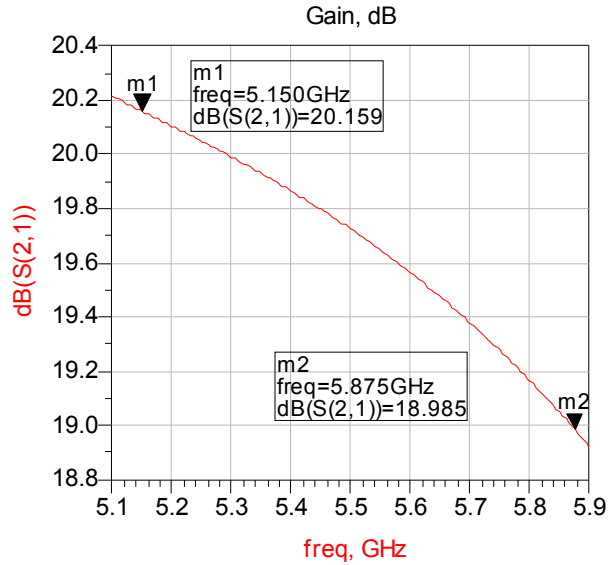
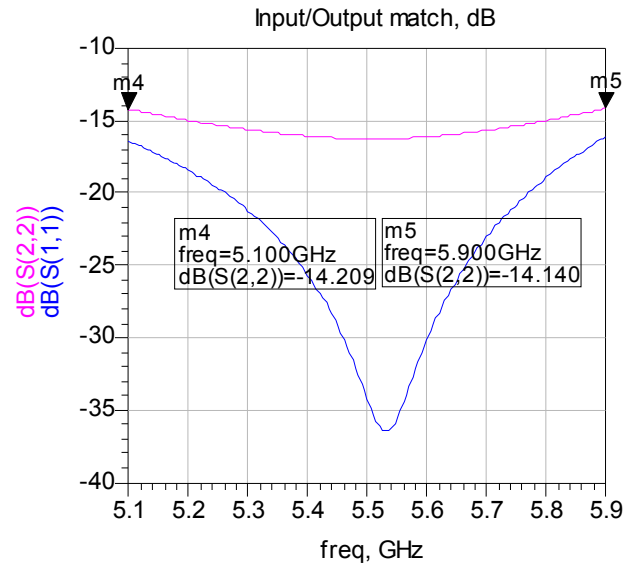
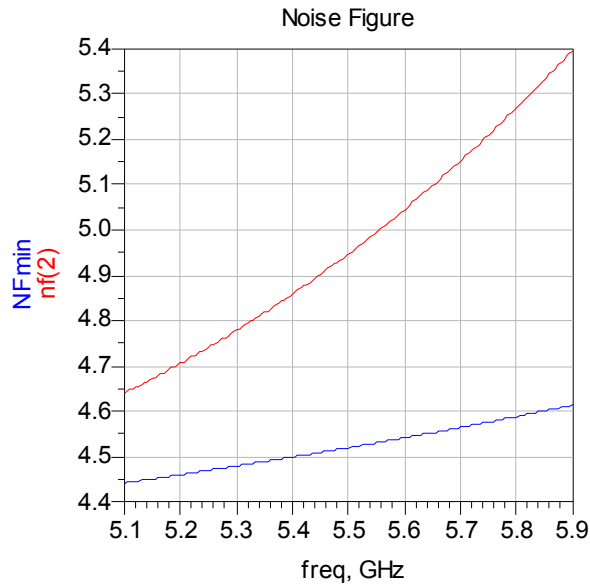
#### 3.1 Simple





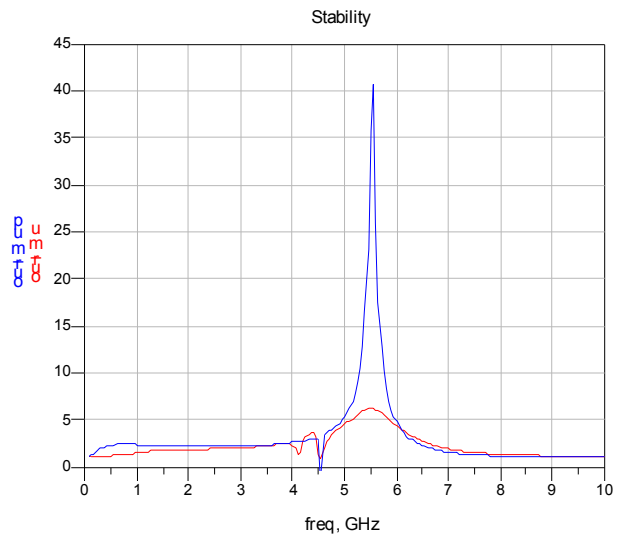
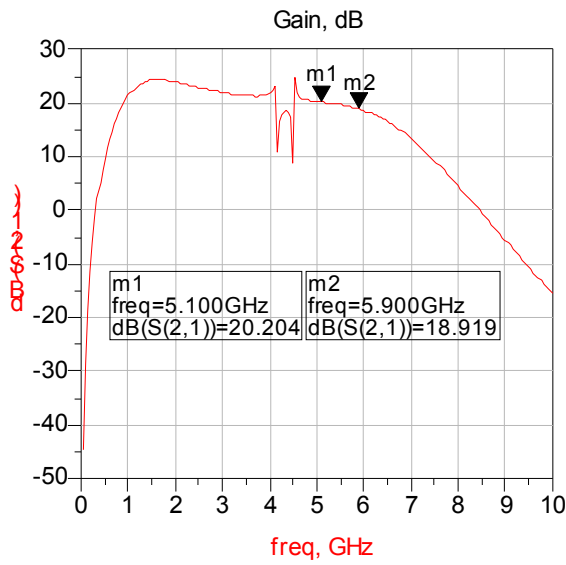
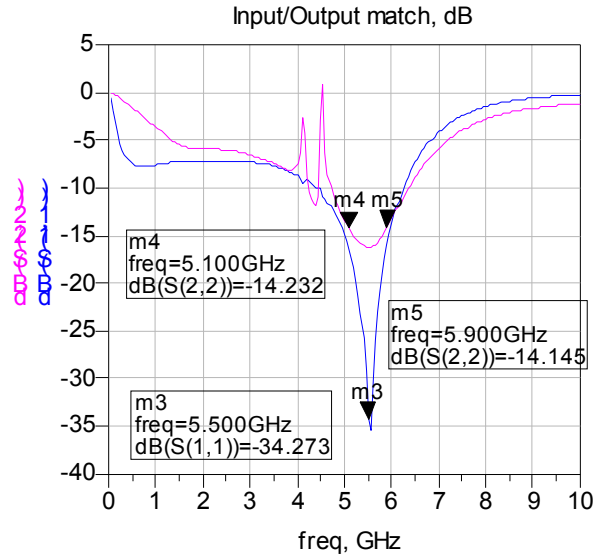
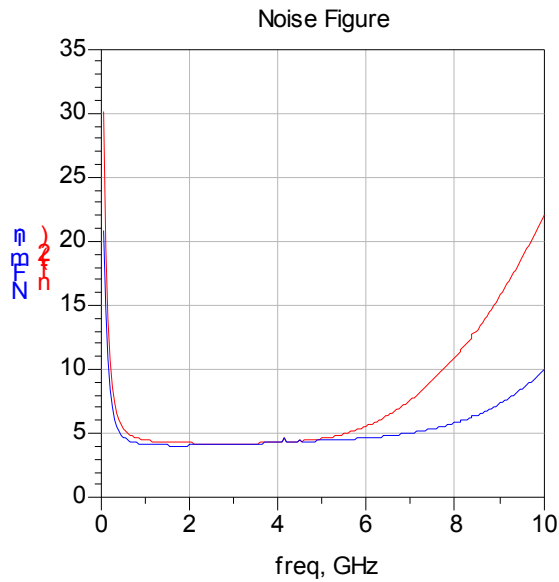
## 4.0 SIMULATION

### 4.1 Linear (Narrowband)

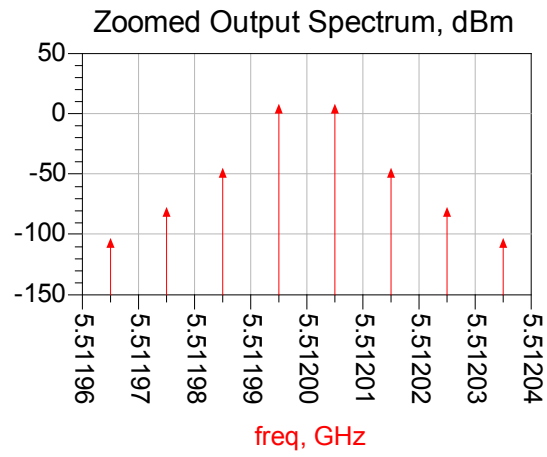


4.2

Linear (Broadband)

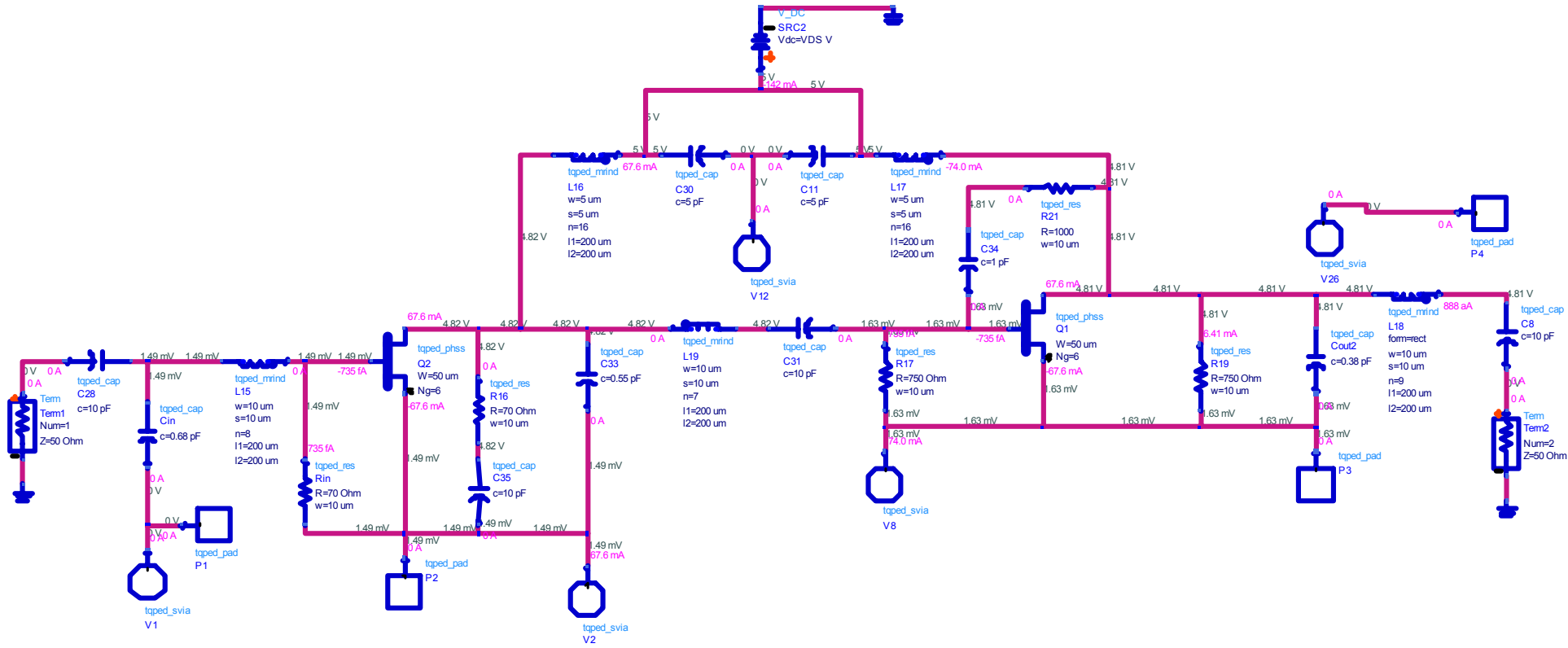


### 4.3 Non-linear (Narrowband)

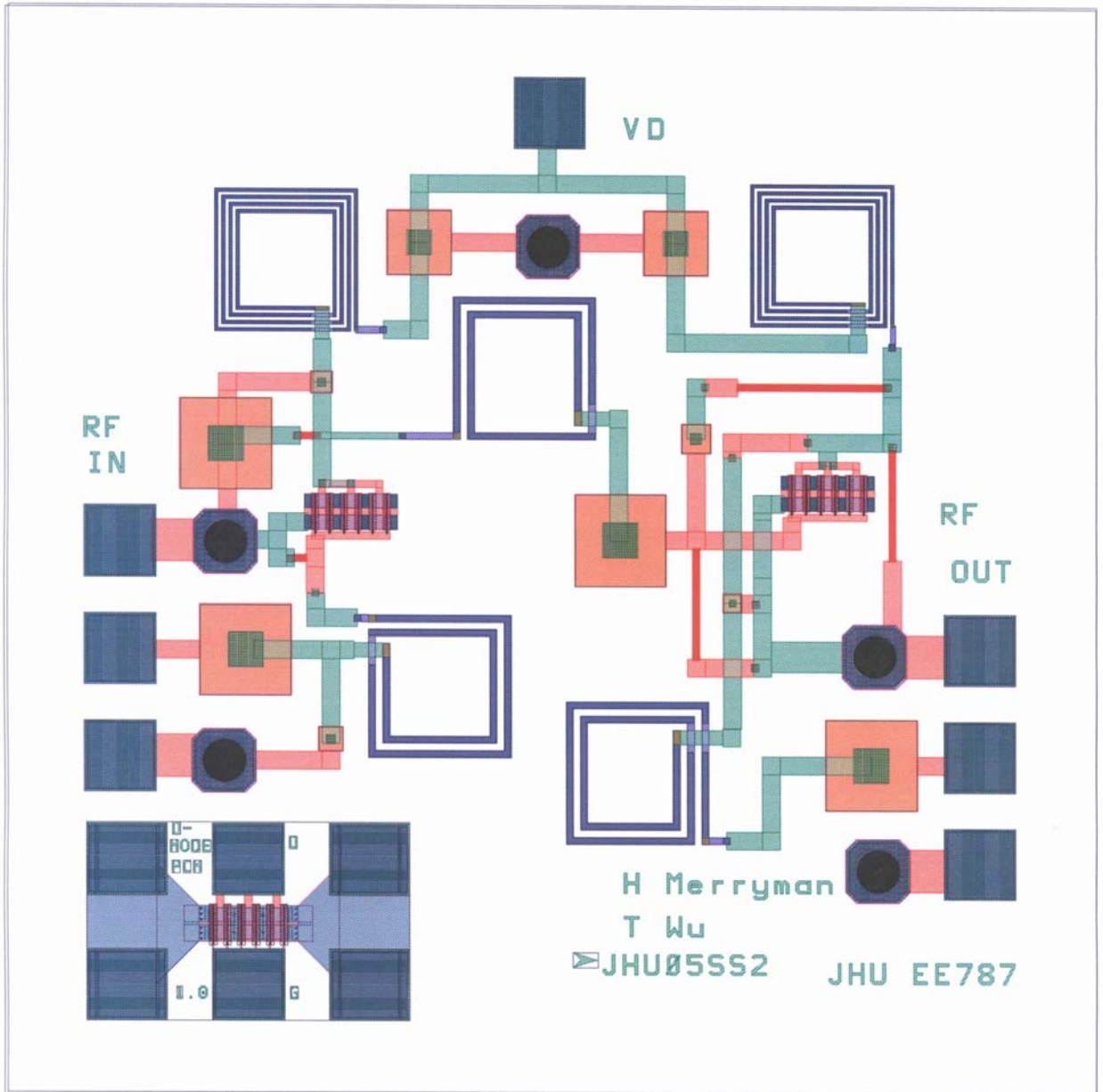


Center Freq of Test Tones (MHz)	IIP3 (dBm)	OIP3 (dBm)
5150	13.7	33.9
5512	13.6	33.2
5875	13.5	32.5

## 4.4 DC Simulation



5.0 LAYOUT



## 6.0 TEST PLAN

A test circuit was added to the bottom left area of our layout to test the process variation for the PHEMT amplifiers.

### Test Equipment

5V Power Supply with Needle Probe  
Agilent 8510 Network Analyzer  
Cables and Ground Signal Ground (GSG) Probes  
Calibration Substrate for MMIC Testing

### Test Procedure

Calibrate the network analyzer from 1 GHz to 10GHz.

Connect the 5V needle probe to the DC pad on the MMIC labeled "VD".  
Slowly increase the voltage to 3V (a safe initial voltage to see if the amplifier is working).  
Connect the input GSG Probes on the "RF IN" pads on the chip.  
Connect the output GSG Probes on the "RF OUT" pads on the chip.  
Measure the S-Parameter data measurements and save them to a disk.

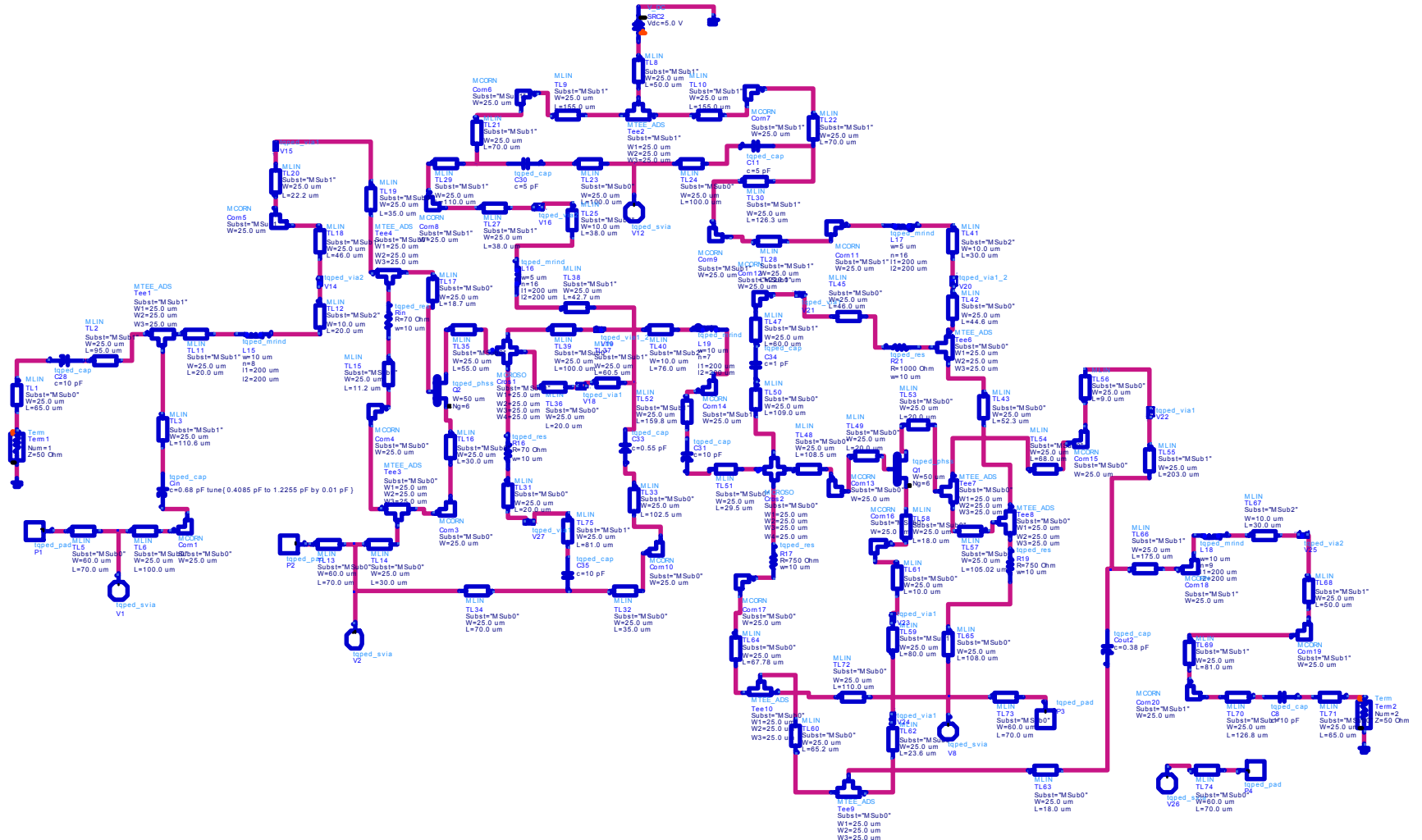
If SSA amplifier performance is not as expected, turn the power supply voltage up slowly (max design voltage is +5V and the current draw should be ~67mA for the amplifiers) to see if the gain increases on the network analyzer and the return loss improves. Re-measure the S-parameters and save the data to a disk.

## 7.0 CONCLUSION

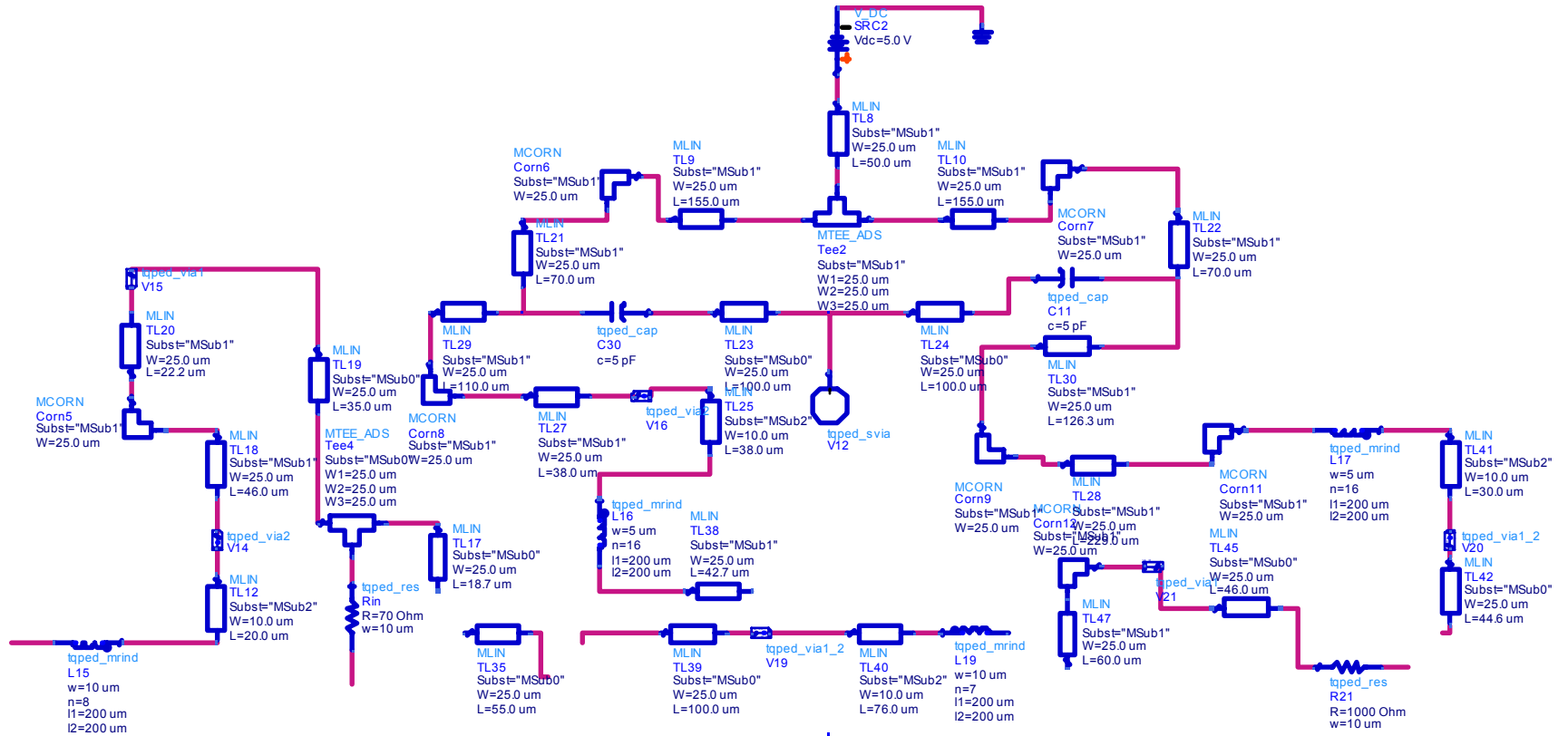
In the system, the SSA should perform as expected. The SSA should produce at least 18dB gain with at least -15dB rejection across the band of interest, and a 32dBm IP3 during a two-tone IMD test. The gain ripple of 1.2 dB may affect the sensitivity of the system, but should not sufficiently degrade the system performance.

However, if the process variation shifts, the amplifier performance may be affected. If the band of interest were to shift down by 500MHz, then we may see issues in amplifier performance, namely an oscillator instead of an amplifier.

8.0 APPENDIX  
8.1 Complex schematic – with interconnects (full view)



## 8.2 Complex – with interconnects (top center view)









# MMIC Design Project Small Signal Amplifier

Thomas Neu  
11/24/2005

## Abstract

This paper covers the design, results and conclusions of the MMIC final project. The goal for this project was to design a small signal amplifier (SSA) using a TriQuint MMIC process. The SSA is part of a larger system designed to receive and transmit signals from 5.15 to 5.85GHz. Our GaAs substrate was defined by the TriQuint MMIC process and the design was to fit on a 60 by 60 mil area.

The amplifier was designed using the 'Advanced Design System' (ADS) software from Agilent which included the TriQuint elements library and was laid out in a 60 by 60 mil Anachip. The amplifier is intended to be used in the transmit as well as receive chain and will be used in a conjunction with other projects designed in this class.

Specification	Goal	Actual Result
Frequency:	5.150 to 5.875 GHz	4.7 to 6.1 GHz
Bandwidth:	>800 MHz	1.4 GHz
Gain (small signal):	>15 dB (16dB, goal)	17.7 dB
Gain Ripple:	+/- 0.5 dB	+/- 0.05 dB
Output IP3:	>20 dB	~30 dB
VSWR, 50Ohm:	< 1.5:1 input & output	<1.5:1 input & output
Supply Voltage:	+/- 5V (+5 V goal)	+ 5V

# Introduction

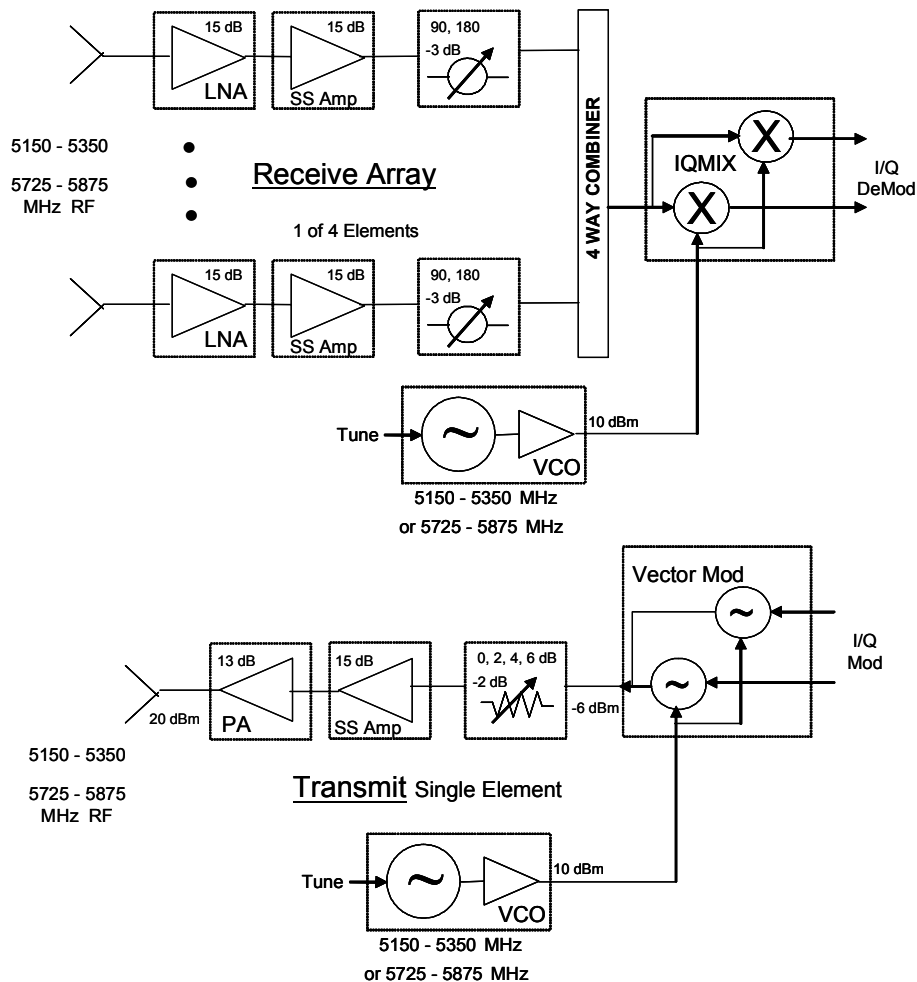
## Circuit Description

The small signal amplifier is part of a larger system as shown below and therefore was designed to cover a very wide frequency range – from 5.1 to 5.9GHz.

In order to cover this wide frequency range with a gain of at least 15dB, a two stage topology was chosen for this amplifier design. The first stage was designed for a gain of ~11dB while second has ~7dB with a feedback resistor to flatten out the gain. The two cascaded FET transistors are biased for class A operation and both FETs are the same size for design simplicity.

The two transistors are configured as self biased to ease power supply requirements. Both stages draw about 30mA each from the supply which overall makes a fairly low power design considering a SSA gain of 17.5dB.

Input and output matching networks are used to maximize the gain but also to get the best input and output match.



Chip Set for the 5150 - 5350 MHz WLAN and  
5725 - 5875 MHz ISM Bands

## 1. Design Approach

### 1.1 Transistor selection:

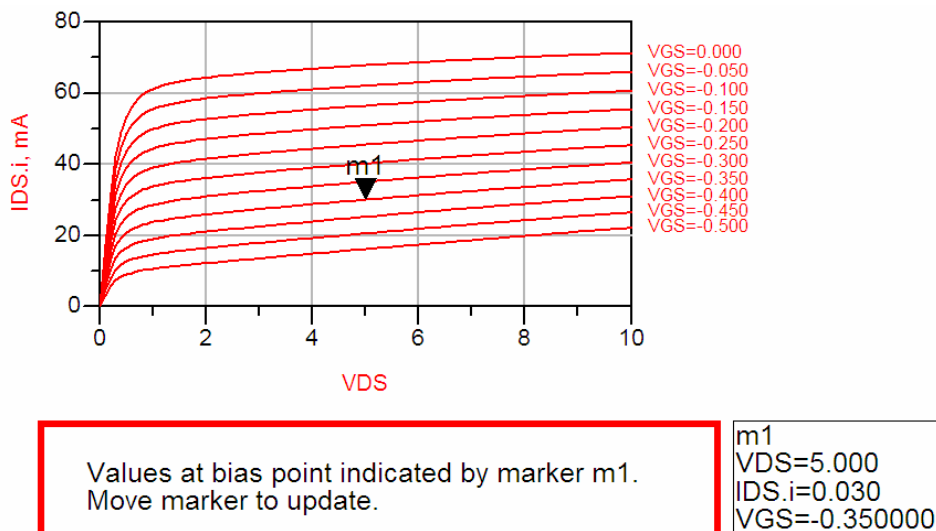
The small signal amplifier consists of two cascaded transistor stages and both stages use a 300um DFET transistor. Initially only one stage was considered, however the gain was fairly narrow band. A feedback resistor 'flattens' and widens the RF gain but also attenuates it significantly.

Therefore a two stage approach was chosen where the first stage provides most of the gain while the second stage with feedback resistor turns the circuit into a wide band amplifier.

### 1.2 Biasing:

First the  $I_{dss}$  (saturated drain source current) was determined at  $V_{gs}=0V$  using the FET tracer tool and it came out to about 68mA as shown in figure 4. For best linear output power,  $I_{ds}$  should be about 55-60% of  $I_{dss}$ , so roughly 36mA.

Both transistors are configured as self biased transistors (resistor at FET source controls drain current) and for  $I_{ds}$  of ~35mA,  $V_{gs}$  should be ~ -0.35V as shown in the simulation below. Bypass capacitors at the source resistors help controlling the gain a little more.



### 1.3 Matching Networks:

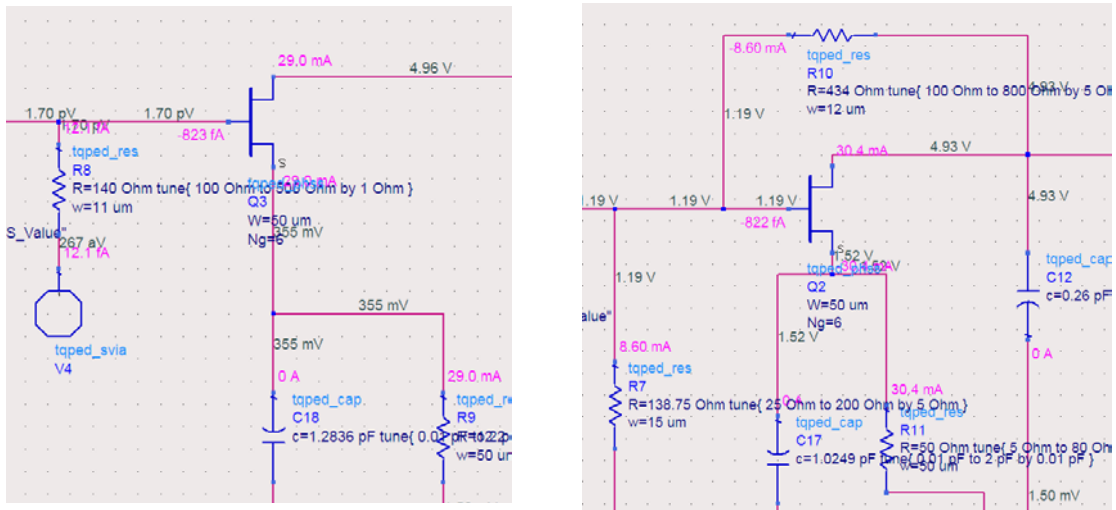
For optimum gain and VSWR, the input and output of the SSA are typically matched with a conjugate complex match to a 50 Ohm impedance. In this design, the input was tuned with a shunt and series inductor while the output was matched with a shunt capacitor and a series inductor.

Another critical element in this design is the connection between first and second stage. A large capacitor is used as a DC block to separate the DC bias of 1<sup>st</sup> and 2<sup>nd</sup> stage and a series inductor matches the output of stage one to the input of stage 2.

## 1.4 Design Tradeoffs - Optimizations:

Originally the SSA gain (S21) showed a lot of ripple (+/- 1dB) in the bandwidth of interest when using  $I_{ds} = 36\text{mA}$ . Therefore the gain was lowered by increasing the source resistors as well as tuning the feedback resistor value. As a result, S21 dropped about 2dB but now shows about +/- 0.1dB ripple. Furthermore the drain current was reduced due to the higher source resistance to roughly 30mA which lowered the overall power consumption by ~20%.

The two schematic snapshots below show  $I_{ds}$  of the first stage around 29mA ( $V_{gs} = -0.355\text{V}$ ) and  $I_{ds} = 30.4\text{mA}$  ( $V_{gs} = -0.33\text{V}$ ) for the second stage. Also in the 2<sup>nd</sup> stage the current through the feedback resistor raises gate voltage to 1.19V.



Secondly, after adding all the transmission line elements, all the matching elements (input, output and between stages) were tuned for minimum VSWR and maximum gain flatness (minimum ripple).

## 2. Simulations:

The SSA performance was simulated and tuned using ADS from Agilent as well as TriQuint transistor and lumped element models.

An overview of the simulation results of the final circuit is shown in figure 1. S11 as well as S22 show a very broad match with a VSWR better than 1.375 from 5 to 6GHz. The amplifier gain (S21) is ~17.7dB with a ripple of ~0.1dB across a BW of 1GHz and a maximum ripple of 0.5dB from ~3.7 to 6.8GHz (also shown in figure 2). Furthermore the simulation predicts unconditional stability from 3 to 8 GHz.

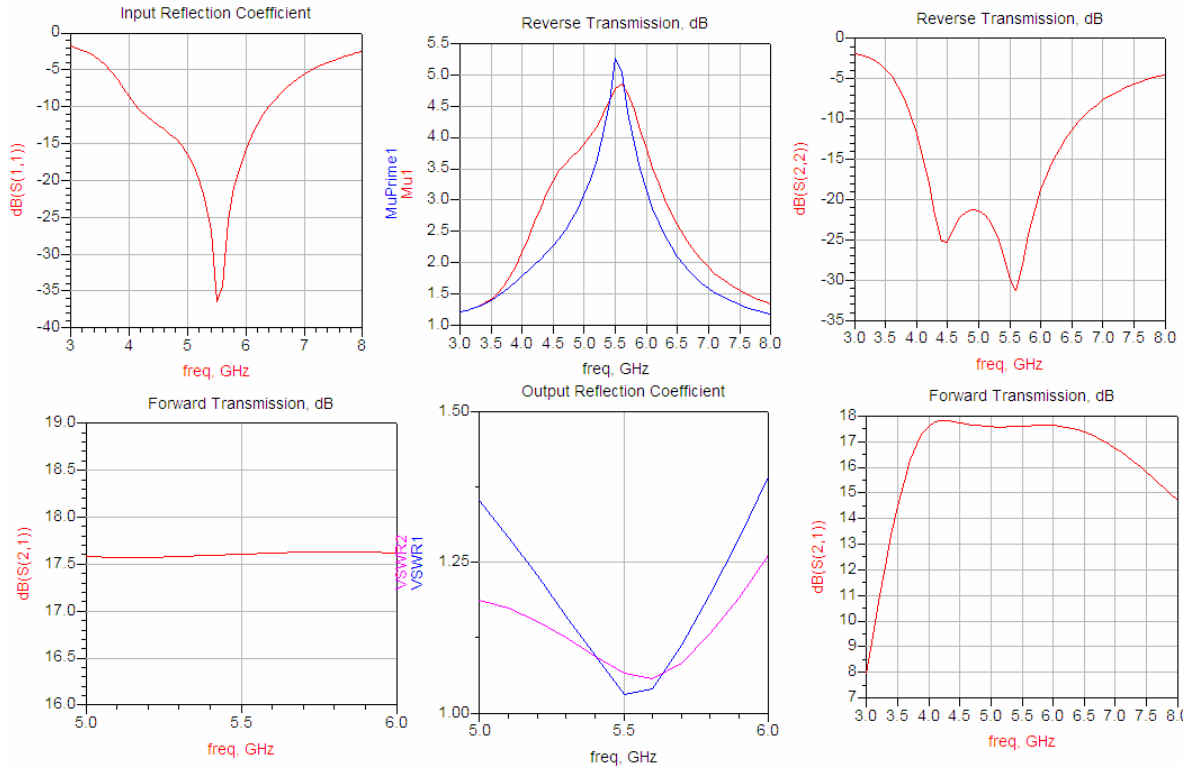


Figure 1: Simulation overview of S11, Mu1 & MuPrime, S22, S21, VSWR1&2 and S21.



Figure 2: Simulation of S21 showing +/-0.5dB ripple from 3.7 to 6.8GHz.



Figure 3 illustrates that the input and output show a very good match (VSWR<1.5) from ~4.7GHz to ~6.1GHz – a 1.4GHz bandwidth.

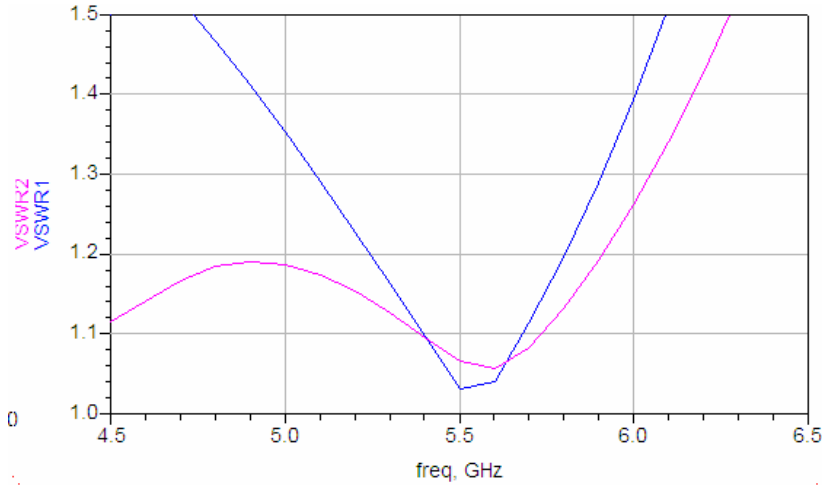


Figure 3: Input and Output VSWR of the SSA

A simulation of the FET tracer estimates a  $I_{dss}$  of ~68mA for  $V_{gs}=0V$  as demonstrated in figure 4. In order to maximize the linear output power capability, the drain-source current should be approximately in the middle of the range, around 34mA. For this design, an  $I_{ds}$  of ~30mA was selected to lower the gain ripple but also to lower the power consumption a little more.

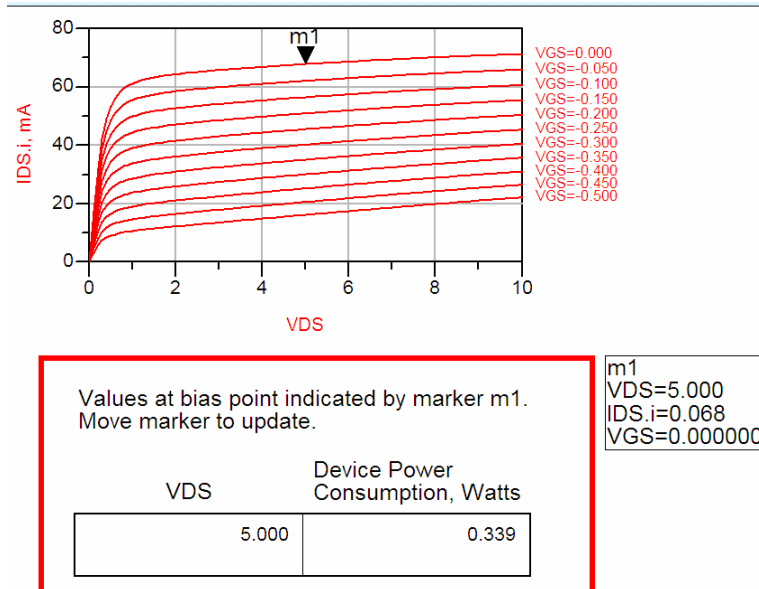
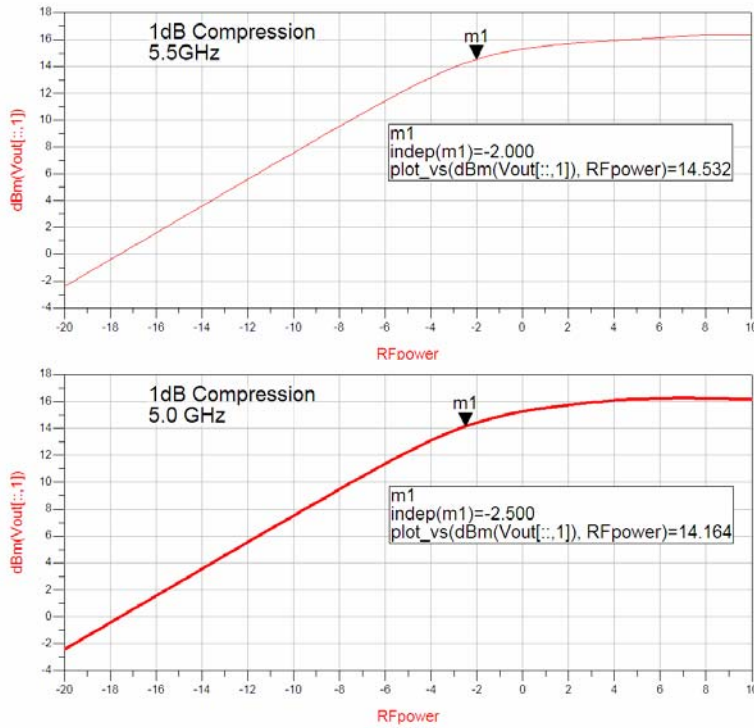
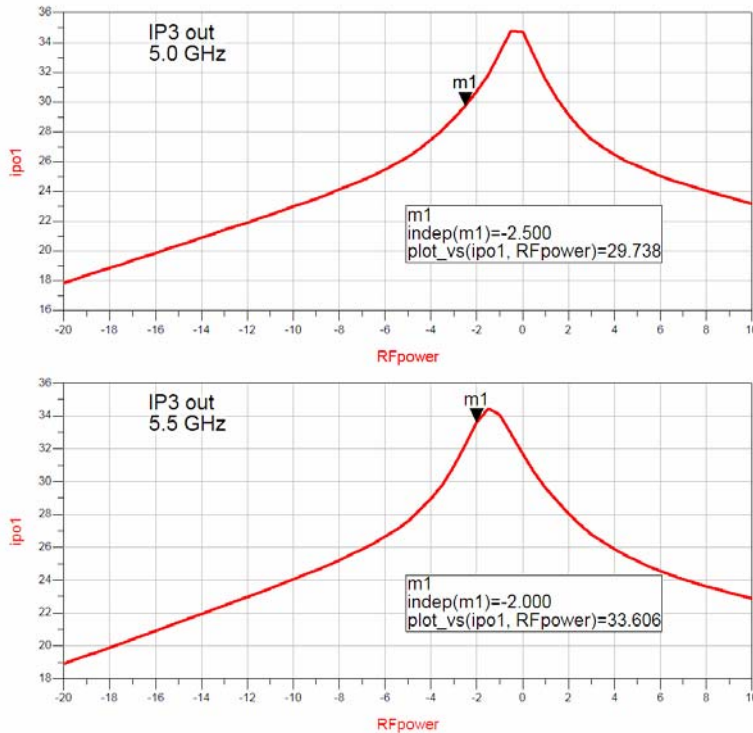


Figure 4: Vgs & Vds sweep of the FET.

At 5.5GHz input, the 1dB compression point is around -2dBm input power, at 5.0GHz it is around -2.5dBm input power as shown below.



The output IP3, measured at the 1dB compression point, is about 29.7dB at 5.0GHz and about 33.6dB at 5.5GHz as shown in the simulation plots below.



### 3. Schematic

At first the schematic was created only with the lumped elements. After adding all the connecting transmission line elements, the circuit had to be retuned to compensate for all the interconnects.

Figure 5 shows the final schematic of the entire amplifier while figure 6 shows the simplified schematic without the connecting elements.

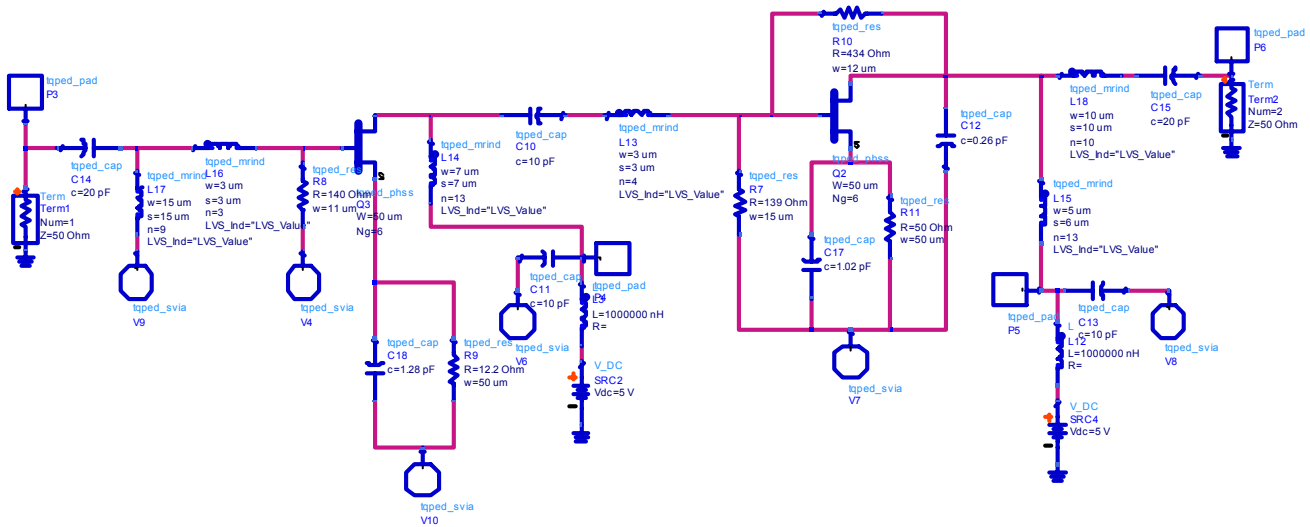
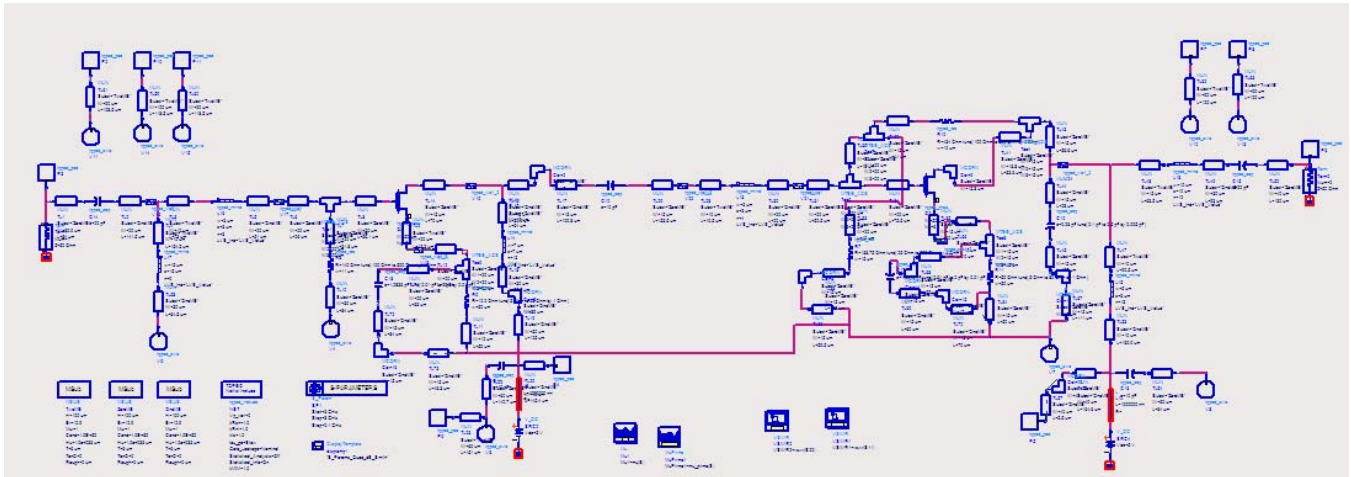
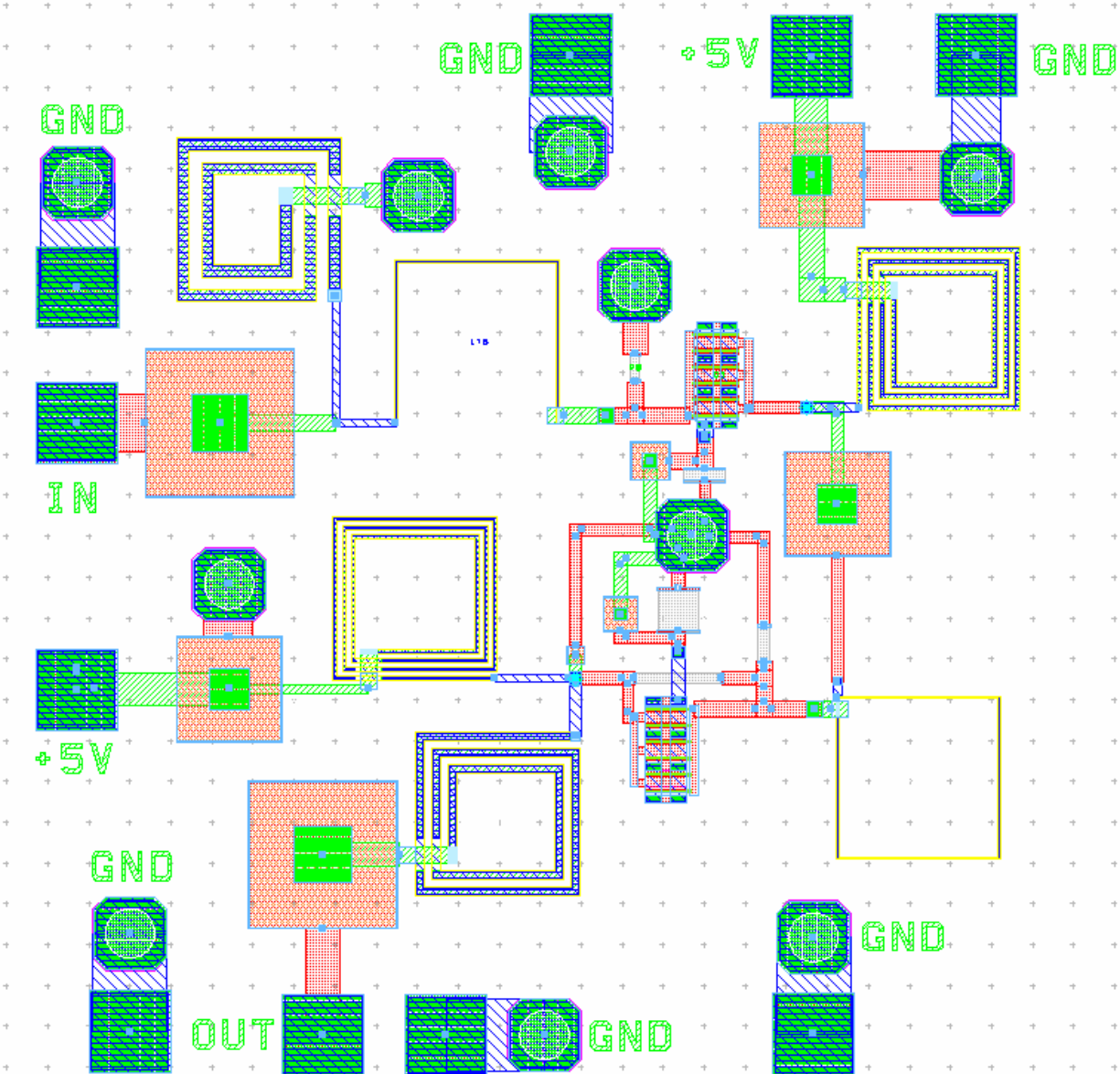


Figure 6: Simplified schematic without the interconnects.

## 4. Layout

A plot of the layout is shown below. The connecting transmission lines on the three metal layers are shown in red (Metal0), green (Metal1) and blue (Metal2).



## **5. Test Plan**

Design verification of the SSA requires measuring s-parameters ( $S_{11}$ ,  $S_{21}$ ,  $S_{22}$ ) as well as output IP3 and DC parameters (power consumption).

### **5.1 Test Equipment:**

The following test equipment will be needed to characterize the SSA:

- Agilent 8510 network analyzer
- Cascade Model 43 wafer probe station with 2 RF probes and 4 DC needle probes
- Synthesized signal generator up to 10GHz
- Spectrum analyzer up to 10GHz
- Simple DC power supply

### **5.2 Turn-On Procedure:**

The SSA requires two 5V supplies – one for each transistor but the SSA can be powered by just one DC power supply. In order to protect the MMIC SSA, the current limit on the power supply should be set to 1.5 times the nominal DC current which is about 90mA  $((30\text{mA}+29\text{mA}) \times 1.5)$ .

### **5.3 S-Parameter Measurements:**

After calibrating the network analyzer, connect the DC and RF probes to the MMIC SSA as shown with the labels on layout. After setting the current limits on the DC power supply,  $S_{11}$ ,  $S_{21}$  and  $S_{22}$  can be measured with the VNA. The drain currents can be measured with a simple multimeter.

### **5.4 1dB Compression Point:**

Since the frequency spectrum of interest is so wide (1GHz), the 1dB compression point measurement should be performed at three frequencies (5.0, 5.5 & 6.0GHz).

The signal generator provides the input signal at the desired frequency to the SSA and the output power level can be recorded with the spectrum analyzer. The initial input power level should be relatively low, around -15dBm. The measured output power minus the provided input power level should equal the small signal gain ( $S_{21}$ ). By raising the input power level and subtracting the gain from the output power, the 1dB compression point can be determined. According to simulation the 1dB compression should  $\sim +2\text{dBm}$  input power.

### **5.5 Output IP3 Measurements:**

For the IP3 measurement, two signal generators are the necessary. The input tones should be spaced  $\sim 10\text{MHz}$  (e.g.  $f_1 = 5.50\text{GHz}$  and  $f_2 = 5.51\text{GHz}$ ). This should ensure that the amplitudes at the transistor input are identical since the attenuation should be the same for such close frequencies. The power levels for both input tones should be set to the same level as well.

The first measurement should be at a very low input power level, e.g. -15dBm. Using the spectrum analyzer, the output tone level as well as third order output ( $2*f_2-f_1$ ) level need to be recorded. The delta between the third order products and the fundamental tones is the third order intercept (TOI) value.

This measurement can be repeated two or three more times (e.g. -15dBm, -10dBm, -5dBm and 0dBm) and the TOI values recorded. The TOI values can be plotted against input power and the intersection of TOI and  $P_{out}$  is the output IP3 point.

## **6 Summary and Conclusion**

The small signal amplifier was designed and simulated using ADS from Agilent with TriQuint semiconductor DFET transistor and lumped element models. The simulation of the final schematic shows a gain of ~17.5dB with exceptionally good gain ripple (~ +/- 0.1dB) and very good input and output match (VSWR < 1.4).

The amplifier itself promises fairly low power consumption with roughly only 60mA from a single +5V supply.

# C-Band Vector Modulator and I/Q Demodulator

Tom Beglin and Greg Eckenrode  
December 10, 2005

*Abstract – This paper details a C-Band .5um pHEMT Vector Modulator and I/Q Demodulator with an I/Q frequency of 50 MHz. The design was simulated using Agilent's Advanced Design Systems along with models supplied by TriQuint. The simulations predict the Vector Modulator to have a minimum insertion loss of ~5dB and the I/Q Demodulator has a conversion loss of ~3dB.*



## Table of Contents

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Design Approach	4
Simulations	5
Schematics	8
Layout	10
Test Plan	11
Conclusion	12

# 1. Introduction

## 1.1 Circuit Description – Vector Modulator

The vector modulator design consists of a 90-degree hybrid to split the RF input into I/Q components, two attenuators to control the amplitude and sign of the I and Q components, and a combiner to sum the two signals. Because of the limited amount of space, the 90-degree hybrid was realized using a lumped element equivalent circuit. Reflective attenuators were designed using the same 90-degree hybrid along with two transistors biased as variable resistors by the I and Q inputs. The combiner is a simple lumped element Wilkinson design.

## 1.2 Circuit Description – I/Q Demodulator

The I/Q Demodulator uses the same architecture except for the replacement of the variable resistors with diode connected FET's. The RF and LO signals are fed into the two RF pads (they can be interchanged), and the 50 MHz I/Q outputs will vary in amplitude depending on the relative phase of the RF signal with respect to the LO signal. The diodes are driven on by the LO input, which was simulated at an input level of +12 dBm to the entire chip.

## 2. Design

### 2.1 Lumped Element 90 degree hybrid

The 90 degree hybrids used in both circuits are a simple lumped element design optimized at a center frequency of 5.5 GHz. For this frequency, a distributed network was unrealizable in the given area. The ideal hybrid was converted to a lumped element circuit by replacing the quarter wavelength sections with equivalent low pass networks.

### 2.2 Wilkinson Divider

Similarly to the 90 degree hybrid, the Wilkinson divider/combiner was realized with equivalent lumped elements at C-band due to size constraints.

### 2.3 Transistor Sizing for Vector Modulator

For the Vector Modulator, the range of the variable resistors is the determining factor in the range of the reflective attenuators. Ideally, a perfect short and a perfect open would yield an attenuation range of +1 to -1. A large resistance is easy to obtain by putting a large enough negative bias on the gate of the FET. Creating a good short requires a large FET, but a large FET also adds parasitic capacitance that can skew the constellation of the vector modulator. A 105  $\mu\text{m}$  FET turned out to be a good compromise. With a gate bias of +.5 volts, the FET had a series resistance of about 10 ohms. The capacitance of the FET was negligible at the frequency of interest. Assuming I/Q inputs of -.7 to +.5 volts, our total range of resistance is approximately 10 to 250 ohms.

### 2.4 Diode Sizing for I/Q Demodulator

For the I/Q Demodulator, we used diodes sized to be approximately 50 ohm loads. This was done to minimize the effects of the diodes on the 90 degree hybrid. With a 12 dBm input, the diodes should be operating near the threshold voltage, so the diodes were sized based on a bias of .7 volts. Diode connected FETs with a single finger of 50  $\mu\text{m}$  turned out to be about 50 ohms at this bias level.

### 2.5 Layout Design

The layout of the 90 degree hybrid circuits was done to minimize the interaction of the two reflective attenuators and any possible cross-talk between the I and Q components. The 90 degree hybrids and the Wilkinson were then re-optimized to compensate for the interconnect within the individual components. The next step was to interconnect the hybrid circuits and Wilkinson and then add in the FETs. Another iteration of tuning was necessary to compensate for this lengthy interconnect. See figures 1 and 2.

### 3. Simulations

#### 3.1 Vector Modulator

The vector modulator was simulated with swept DC inputs for the I and Q signals. Careful considerations were made to ensure that this circuit would work at the specified 50 MHz as well.

Figure 1 shows a polar plot of the output constellation with gate biases swept from -.7 to +.5 volts. As you can see, it has a usable range out to an amplitude of .3, or just over 5 dB of loss. This complies with the specified loss goal of no more than 7 dB. It should be noted that the output is highly nonlinear with respect to the I/Q voltages. It is assumed that this will be compensated by the back end of the system.

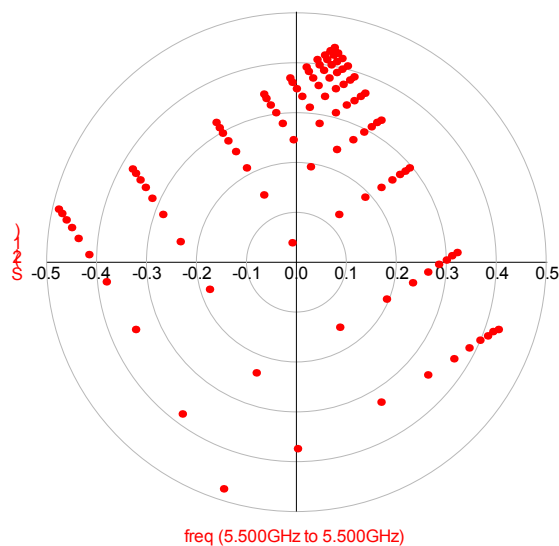


Fig 1 – Vector modulator output constellation

Figure 2 shows the RF input and output vswr, both of which meet the spec of 2.5:1. The output vswr comes close, but does not meet the goal of 1.5:1 at the upper edge of the band. The I/Q input vswr is nearly perfect due to the 50 ohm shunt resistor at these inputs.

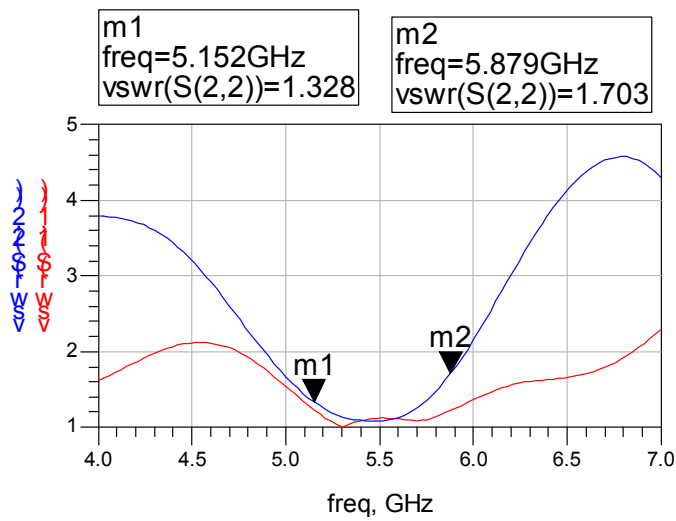


Fig 2 – Input and Output vswr

To evaluate the power handling capabilities of this circuit, the input power and the I/Q inputs were all swept together. It was determined that this circuit has the lowest 1 dB compression point when all of the FET's are biased to look like 50 ohm loads (approximately -0.4 volts). The plot in figure 3 shows the compression of the circuit at this bias level.

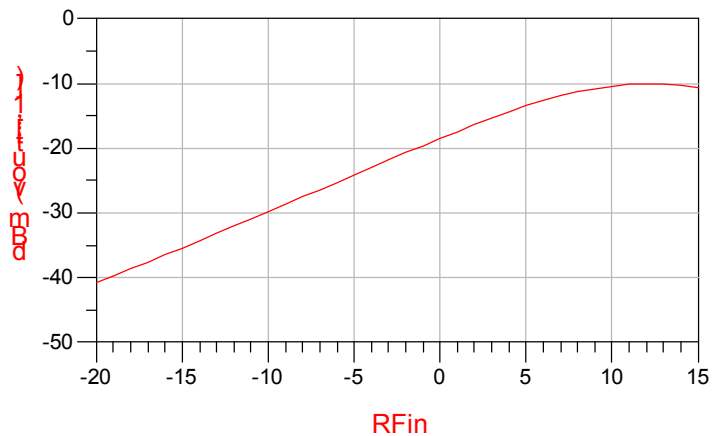


Fig 3 – Vector Modulator compression

### 3.2 I/Q Demodulator

The I/Q Demodulator was simulated using the ADS harmonic balance simulation tool. To vary the I/Q input, an ideal phase-shifter was placed at the RF input, and the phase was swept from 0 to 360 degrees. As figure 4 shows, the I and Q outputs (50 MHz) each have two peaks and are offset by close to 90 degrees. The simulation was done with an LO input power of +12 dBm to drive the diodes, and an RF input power of 0 dBm. These simulations show that there is only ~2dB of insertion loss in the circuit.

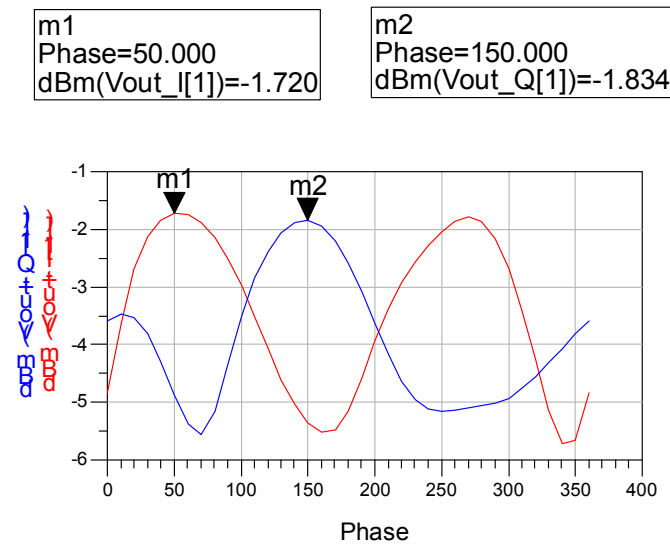


Fig 4 – I/Q Demodulator output vs. RF input phase

Similar to the vector modulator, the I/Q demodulator has good vswr, but it does not quite meet the goal of 1.5 at the upper edge of the band.

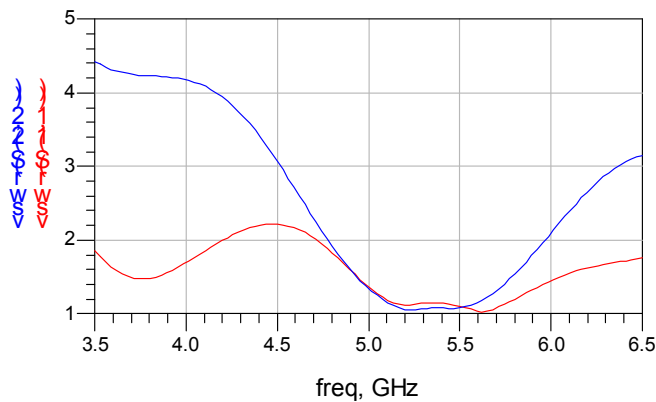
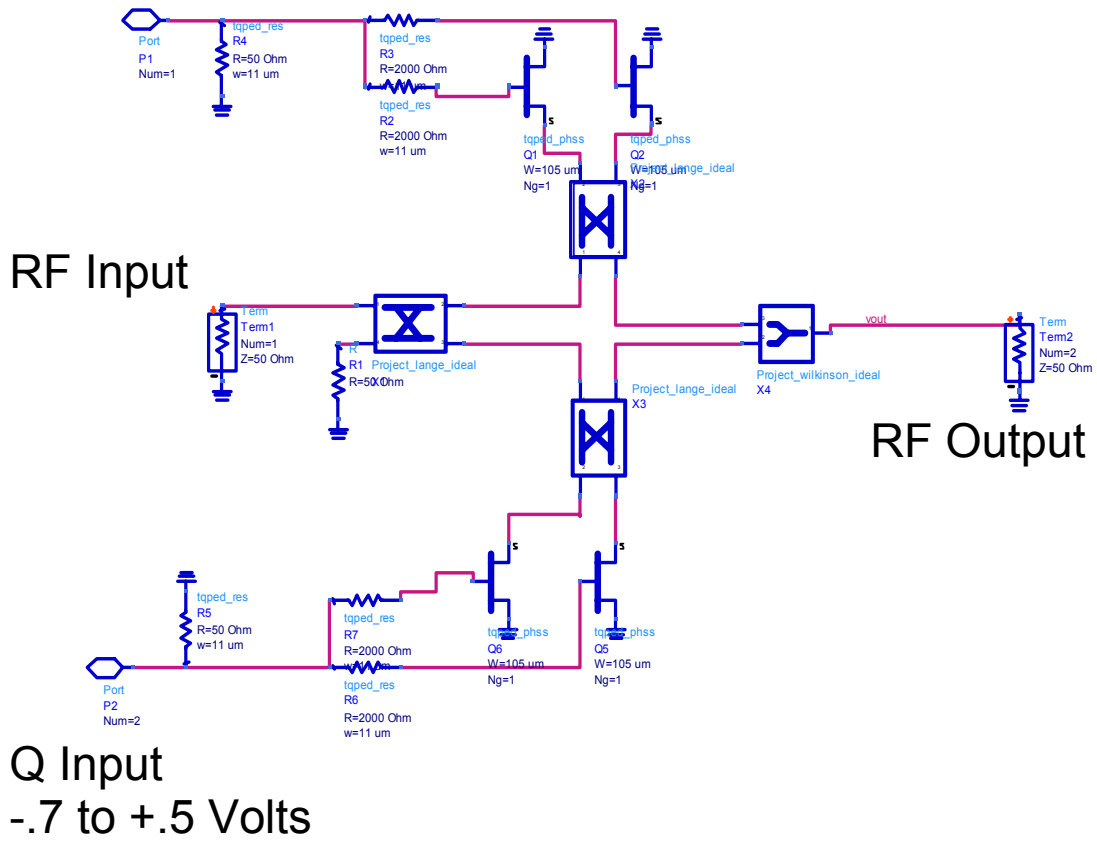


Fig 5 – I/Q Demodulator RF and LO vswr

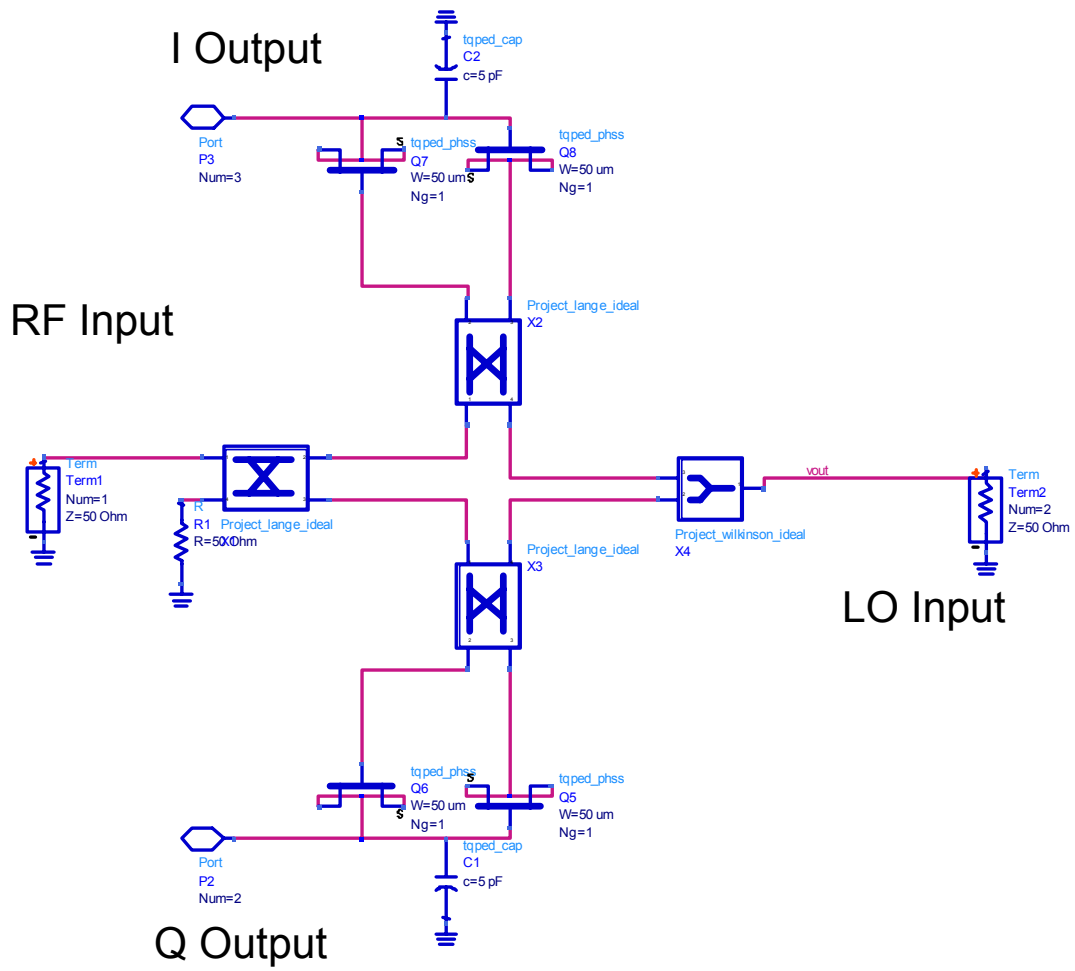
## 4. Schematics

### 4.1 Vector Modulator Schematic

I Input  
-.7 to +.5 Volts



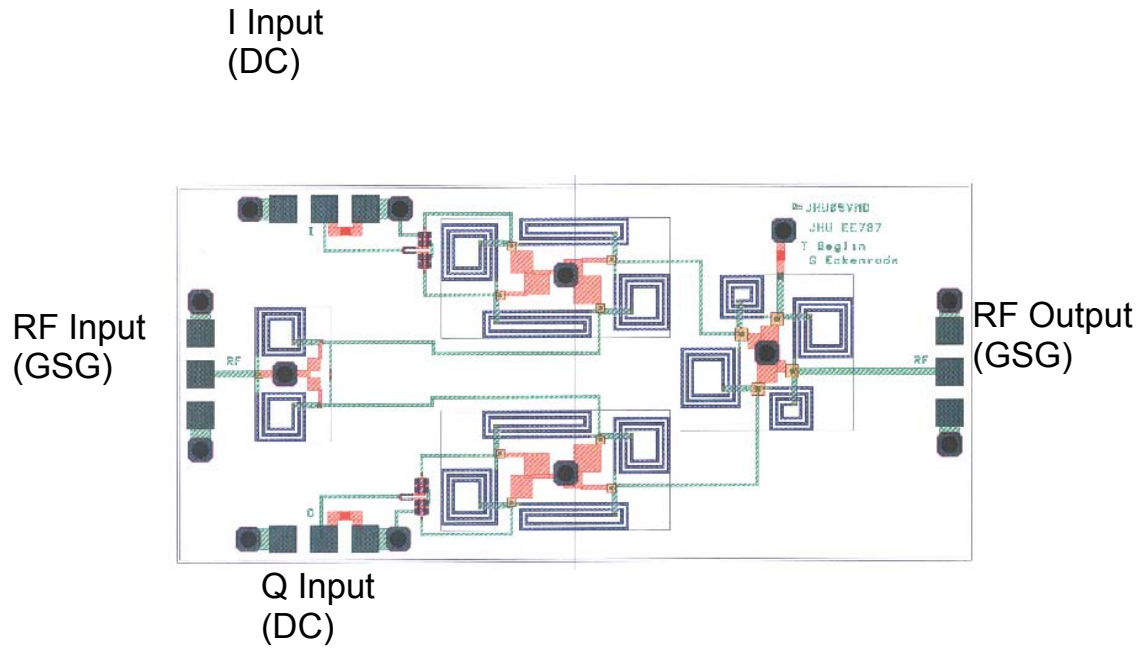
## 4.2 I/Q Demodulator Schematic



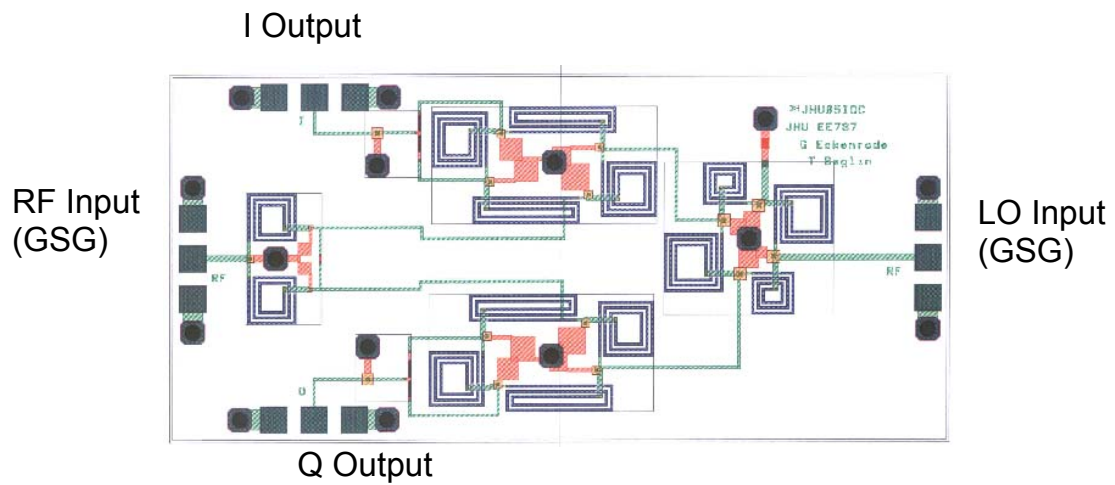


## 5. Layout

### 5.1 Vector Modulator Layout



### 5.2 I/Q Demodulator Layout



## 6. Test Plan

### 6.1 Test Equipment

- Agilent 8510 Network Analyzer
- DC power supply
- Two signal generators with phase-locking capability
- Spectrum analyzer

### 6.2 Test Procedure

#### 6.2.1 Vector Modulator Test Procedure

The Vector Modulator can be easily tested by measuring the RF input to RF output on a network analyzer. First, a calibration from 5 to 6 GHz should be performed on the network analyzer. Measurements of the device should then be taken with each of the bias settings listed in the table below. After the data has been taken, single frequency points can be plotted on a polar chart across bias settings to verify a good constellation of RF output magnitudes and phases.

Input Voltages	
I	Q
-.7	-.7
-.7	-.3
-.7	.1
-.7	.5
-.3	-.7
-.3	-.3
-.3	.1
-.3	.5
.1	-.7
.1	-.3
.1	.1
.1	.5
.5	-.7
.5	-.3
.5	.1
.5	.5

### 6.2.1 I/Q Demodulator Test Procedure

The I/Q Demodulator will require two RF sources phase locked together with an offset of 50 MHz. These signals should be input into the RF and LO GSG pads on the device, and the I/Q outputs should be observed on a spectrum analyzer. The input power should be 0 dBm on the RF input and 12 dBm on the LO input. To test that the I and Q components are being separated out of the RF signal, a relative phase shift will have to be inserted between the RF source and the device.

This can be realized by lengthening the cable between the RF source and the device in small increments (possibly with several RF connectors in a row). The relative changes in phase of this cable should be measured on a network analyzer prior to beginning this test. The amplitude of the 50 MHz I/Q outputs should then be measured and plotted versus the relative phase shift (see simulation plot in section 3.2).

## 7. Conclusion

The design of a C-Band Vector Modulator and I/Q Demodulator have been described. The simulations were performed using ADS and they showed that the vector modulator will have an insertion loss of ~5 dB while the I/Q demodulator will have a conversion loss of ~2 dB. The designs will be fabricated at TriQuint using the .5um pHEMT process.

## 8. References

1. Penn, John E. "A Balanced Ka-Band Vector Modulator MMIC." *Microwave Journal*, June 2005.



EE525.787 – Microwave Monolithic Integrated Circuit (MMIC)  
Engineering and Applied Science Programs for Professionals

Instructors: John Penn & Dr. Michel Reece

# **C-Band Low Noise Amplifier (LNA)**

## **Microwave Monolithic Integrated Circuit (MMIC)**

**Designer: Wilart Banks**  
**December 12, 2005**

## 1 Abstract

This report gives the detail description for a GaAs Low Noise Amplifier (LNA) Monolithic Microwave Integrated Circuit (MMIC), designed for use in a duplex transceiver as part of the first stage of a receive array operating in the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies.

## 2 Introduction

As the first stage of the receive array of the duplex transceiver, the LNA receives signals in the WLAN and ISM frequencies. It then processes these signals and outputs to the next stage as input with 15 dB gain and a noise figure of less than 2 dB.

## 3 Design Approach

The initial approach was to design a LNA that would meet the design specifications. The first step was to select a linear transistor model to use. After the linear transistor was chosen, it needed to be stabilized. Three different stability circuits were looked at which was a series resistor, a series and shunt resistor, and a feedback resistor configuration. After running the simulation for each circuit configuration, it was apparent that the specifications could not be met with a single stage design and thus two stages were needed to meet or exceed the requirements. I decided to try each combination of the circuits cascaded and recorded the results for each one at 5.5 MHz. The results are tabulated below.

Circuit	Gain dB(S21)	Input Match dB(S11)	Output Match dB(S22)	Mu1	MuPrime 1	nf(2)	Nfmin
5a	20.391	-3.960	-29.202	1.858	1.212	2.630	2.374
5b	19.983	-8.083	-11.643	2.505	1.866	2.607	2.369
5c	12.068	-2.663	-5.250	1.743	1.325	2.601	2.353
5d	13.064	-11.668	-4.993	1.714	3.461	2.602	2.361
5e	15.437	-2.581	-13.842	3.345	1.282	2.561	2.324
5f	15.385	-9.872	-12.095	3.637	2.868	2.586	2.342
5g	24.714	-0.023	-13.520	0.009	0.737	0.999	0.997
5h	9.124	-3.584	-7.969	2.401	1.487	3.788	3.237
5i	0.097	-3.514	-4.800	1.734	1.496	4.203	3.538
5j	2.463	-3.503	-4.669	1.706	1.493	3.913	3.329
5k	2.138	-3.540	-12.172	4.020	1.500	4.066	3.439
5l	3.944	-3.529	-11.406	3.669	1.497	3.914	3.331
5m	12.516	-2.825	-11.289	3.171	1.347	2.604	2.311
5n	13.804	-2.884	-8.999	2.410	1.338	2.470	2.223
5o	4.783	-2.674	-4.870	1.738	1.355	2.615	2.320
5p	7.374	-2.701	-4.813	1.724	1.357	2.493	2.239
5q	6.988	-2.728	-12.326	3.985	1.363	2.526	2.258
5r	9.128	-2.715	-11.491	3.576	1.357	2.470	2.223

I chose the circuit 5n because I felt this gave me the best tradeoff between gain, match, stability and noise figure and allowed me enough room to optimize the circuit.

After the linear circuit was stable and it met the requirements, I replaced the linear model with the non-linear TriQuint model and tuned the circuit to get the final results.

### 3.1 Specifications vs. Goals

For the design, the following specifications to design to were also my goals to achieve.

	Specifications	Goals
Frequency	5150 – 5875 MHz	5150 – 5875 MHz
Bandwidth	> 800 MHz	> 800 MHz
Gain	> 15 dB	> 15 dB
Gain Ripple	$\pm 0.5$ dB	$\pm 0.5$ dB
Noise Figure	< 3 dB	< 3 dB
Input IP3	> + 5 dBm	> + 5 dBm
VSWR, 50 Ohm	< 1.5:1	< 1.5:1
Supply Voltage	+ 5 Volts	+ 5 Volts
Size	60 x 60 mil ANACHIP	60 x 60 mil ANACHIP

### 3.2 Tradeoffs

The LNA design has many tradeoffs associated with it such as balancing gain, stability, match and noise figure. This particular design has its major tradeoff between gain and noise figure. Care was taken to not over compensate for one by sacrificing the other. By tuning the output matching circuit of the second stage, I was able to achieve my goal of 15 dB gain while also achieving a noise figure less than 2 dB.

### 3.3 Circuit Description

The LNA is a two-stage design with two transistors cascaded using the output from the first stage as the input to the second stage. Each stage was designed to fulfill different purposes. The first stage for low noise and the second stage for output match and gain bandwidth. Both stages of the LNA utilize a TriQuint 6x50 0.5 $\mu$ m PHEMT biased at 3V of drain voltage and 15 mA drain current.

The first stage of the LNA utilizes a series and shunt resistor for stability. Because this particular design has very low noise, it is used in the design as the first stage since this stage sets the overall noise figure.

The second stage of the LNA utilizes a feedback resistor for stability. This design is used in the second stage to improve output match and increase the gain bandwidth of the amplifier.

## 4 Simulations

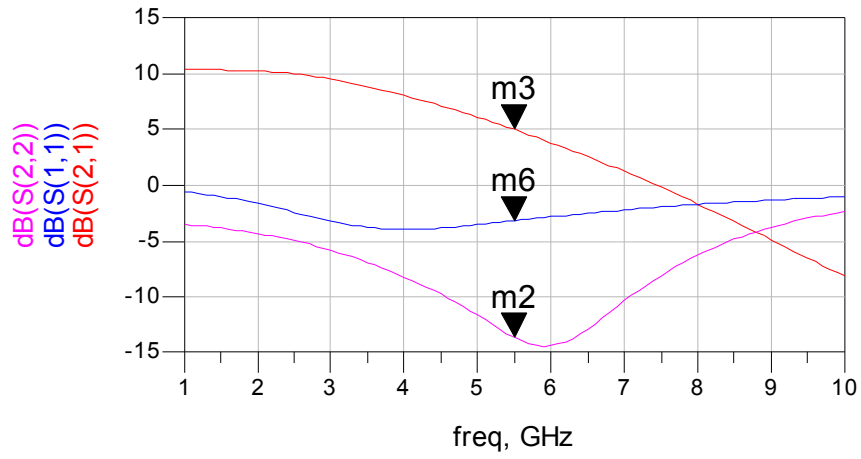
## 4.1 Linear

### 4.1.1 First Stage Gain $S(2,1)$ , Input Match $S(1,1)$ , Output Match $S(2,2)$

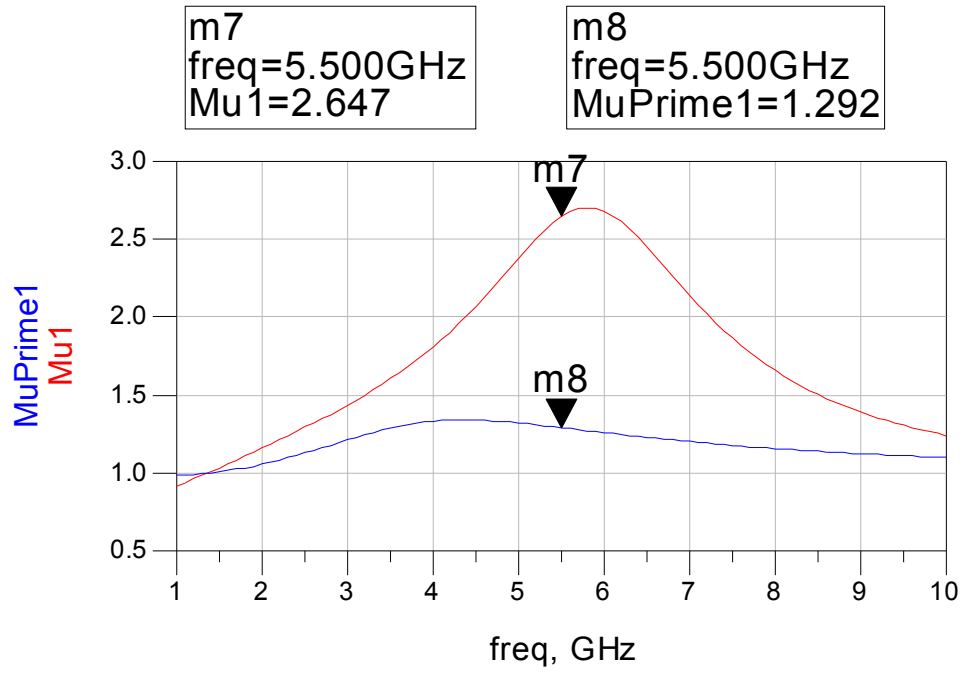
m3  
freq=5.500GHz  
dB(S(2,1))=5.001

m6  
freq=5.500GHz  
dB(S(1,1))=-3.157

m2  
freq=5.500GHz  
dB(S(2,2))=-13.616



### 4.1.2 First Stage Stability

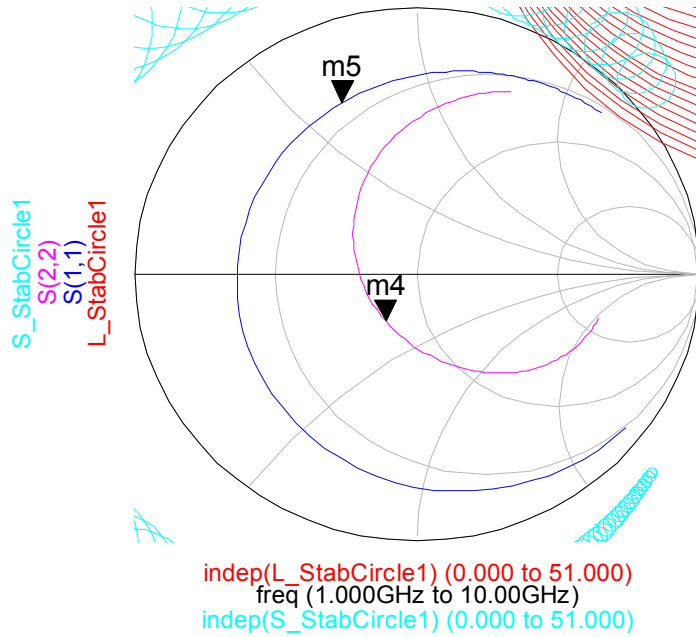




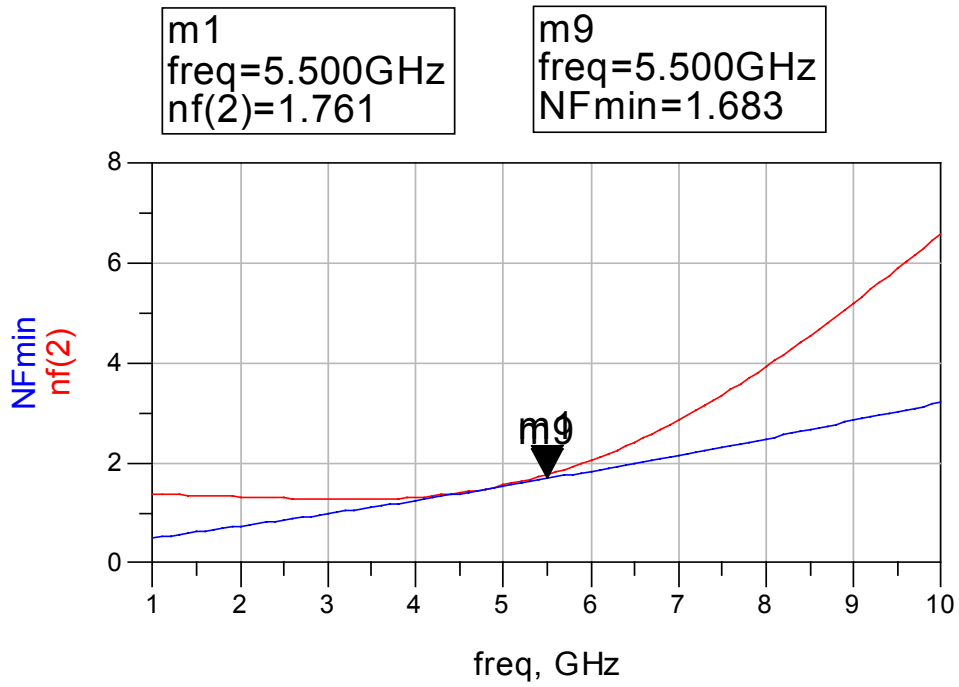
### 4.1.3 First Stage Stability (Smith Chart)

m4  
freq=5.500GHz  
S(2,2)=0.209 / -121.677  
impedance =  $Z_0 * (0.758 - j0.281)$

m5  
freq=5.500GHz  
S(1,1)=0.695 / 112.269  
impedance =  $Z_0 * (0.257 + j0.640)$



#### 4.1.4 First Stage Noise Figure $nf(2)$ , Minimum Noise Figure (Nfmin)

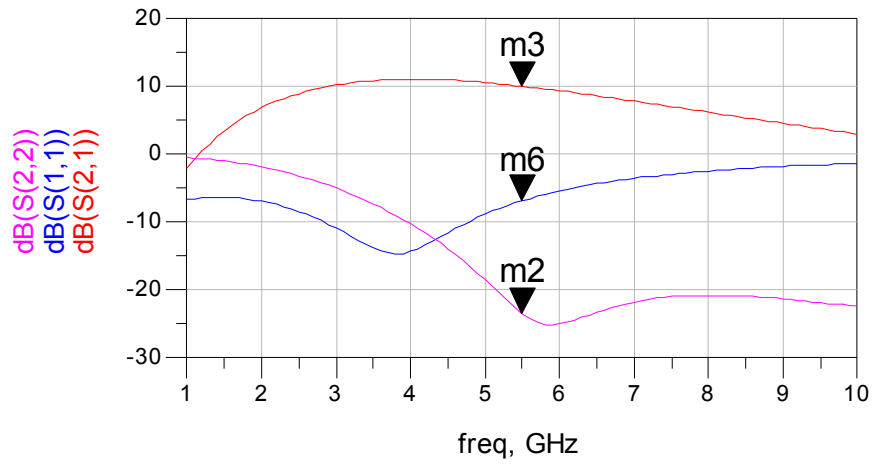


#### 4.1.5 Second Stage Gain $S(2,1)$ , Input Match $S(1,1)$ , Output Match $S(2,2)$

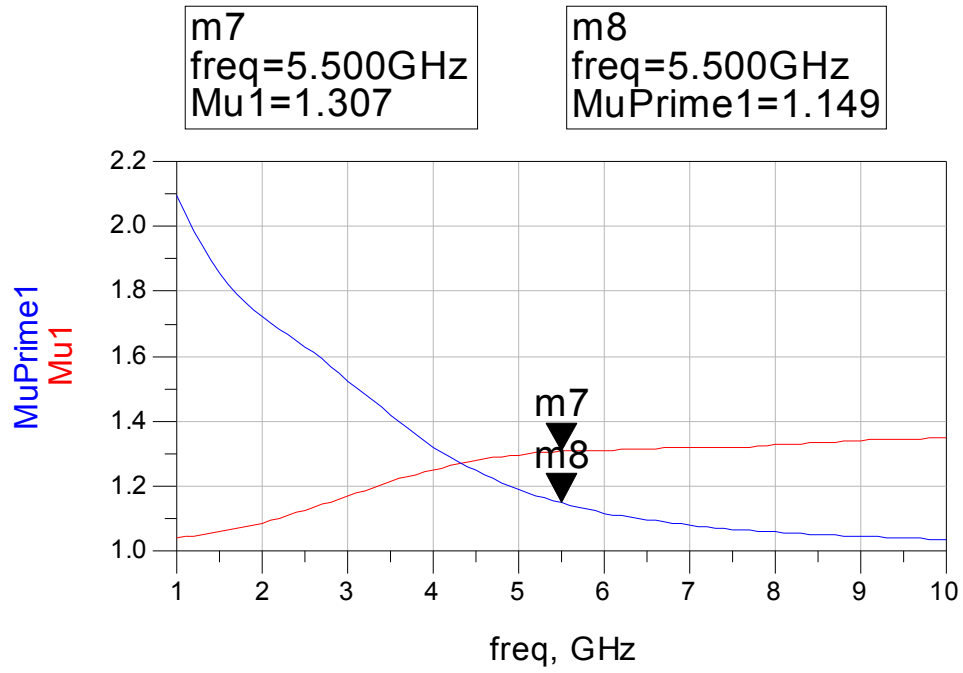
m3  
freq=5.500GHz  
dB(S(2,1))=10.019

m6  
freq=5.500GHz  
dB(S(1,1))=-6.804

m2  
freq=5.500GHz  
dB(S(2,2))=-23.397



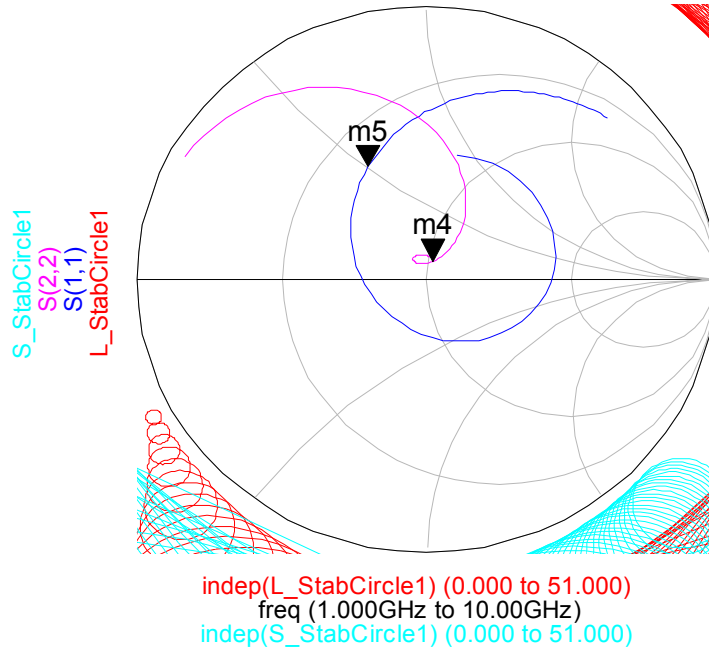
### 4.1.6 Second Stage Stability



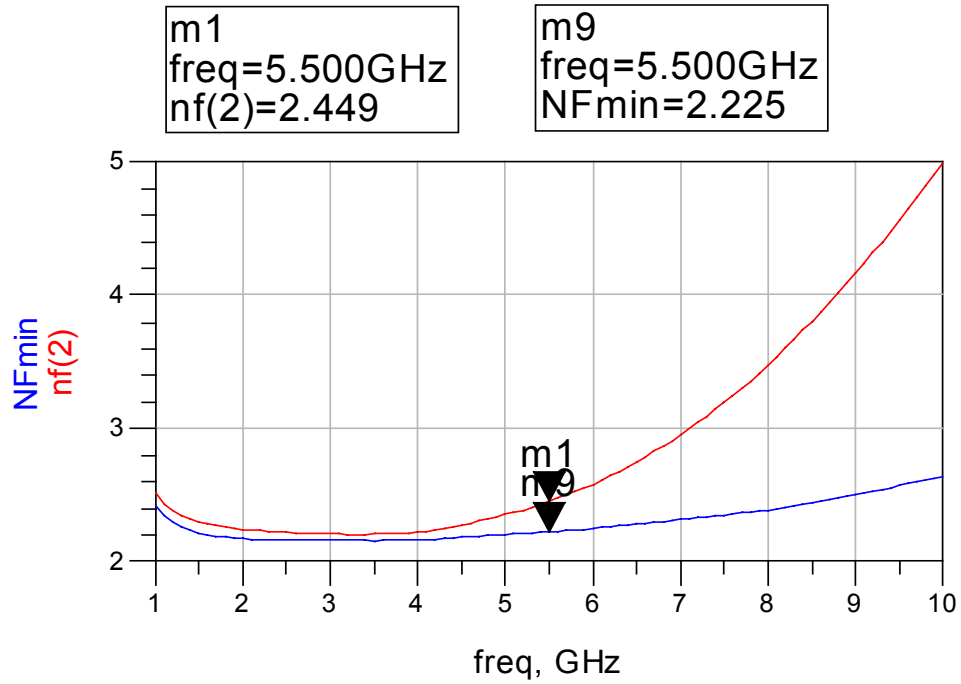
### 4.1.7 Second Stage Stability (Smith Chart)

m4  
freq=5.500GHz  
S(2,2)=0.068 / 71.084  
impedance = Z0 \* (1.036 + j0.133)

m5  
freq=5.500GHz  
S(1,1)=0.457 / 116.374  
impedance = Z0 \* (0.490 + j0.507)



### 4.1.8 Second Stage Noise Figure $nf(2)$ , Minimum Noise Figure (Nfmin)

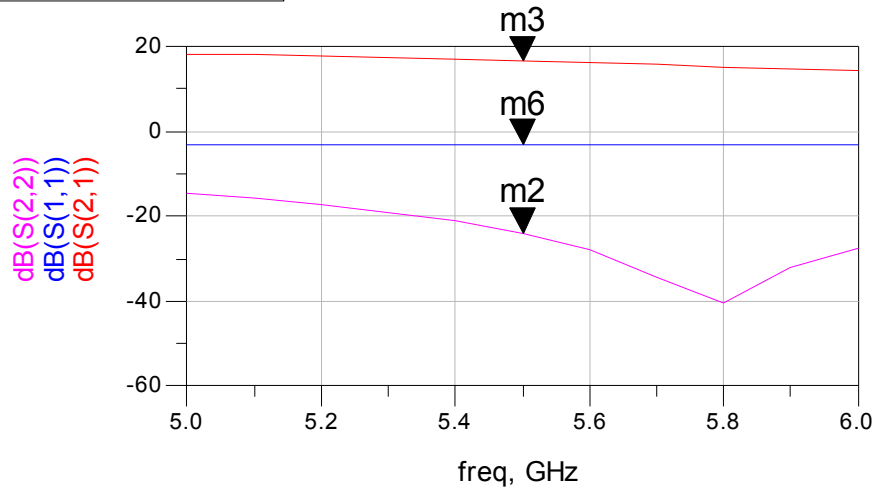


### 4.1.9 Both First and Second Stage Gain $S(2,1)$ , Input Match $S(1,1)$ , Output Match $S(2,2)$

m3  
freq=5.500GHz  
dB(S(2,1))=16.550

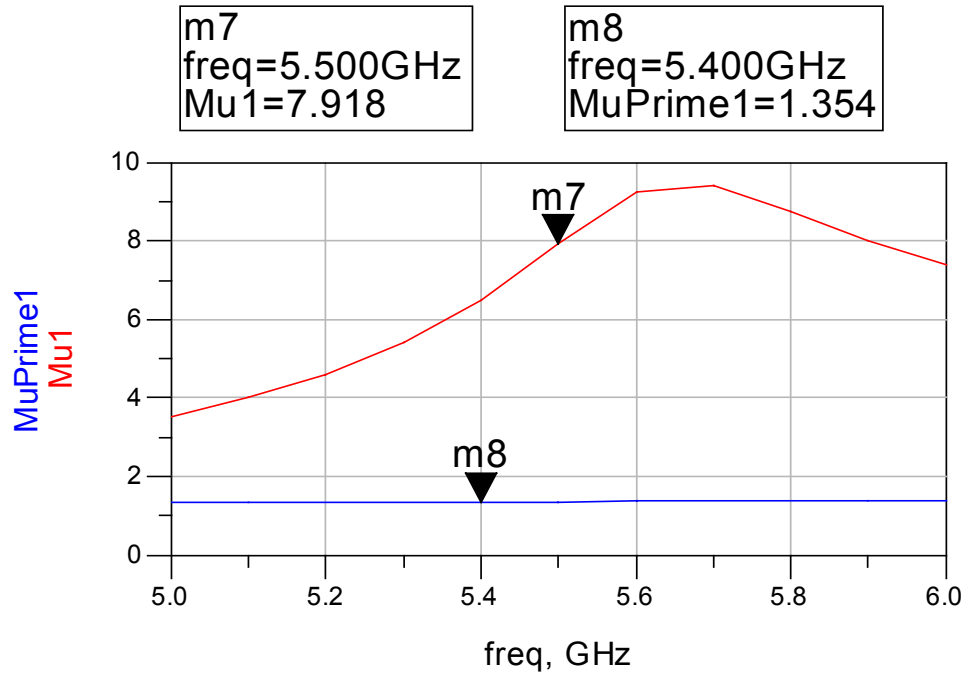
m6  
freq=5.500GHz  
dB(S(1,1))=-3.171

m2  
freq=5.500GHz  
dB(S(2,2))=-24.006



#### 4.1.10

#### Both First and Second Stage Stability

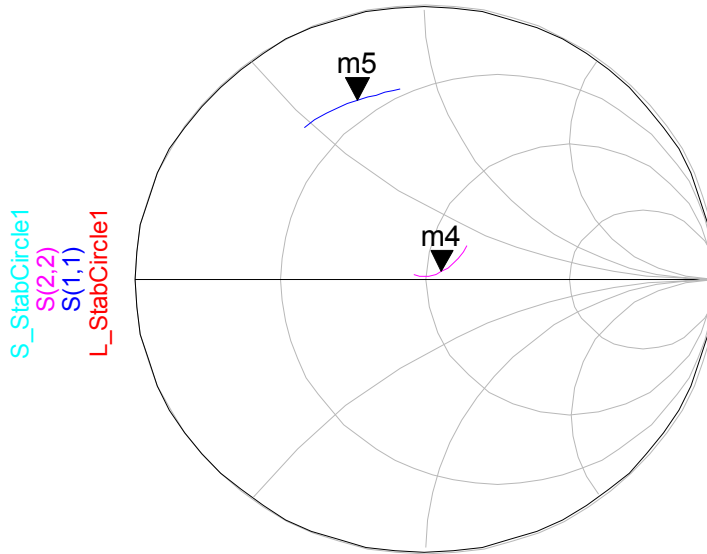




#### 4.1.11 Both First and Second Stage Stability (Smith Chart)

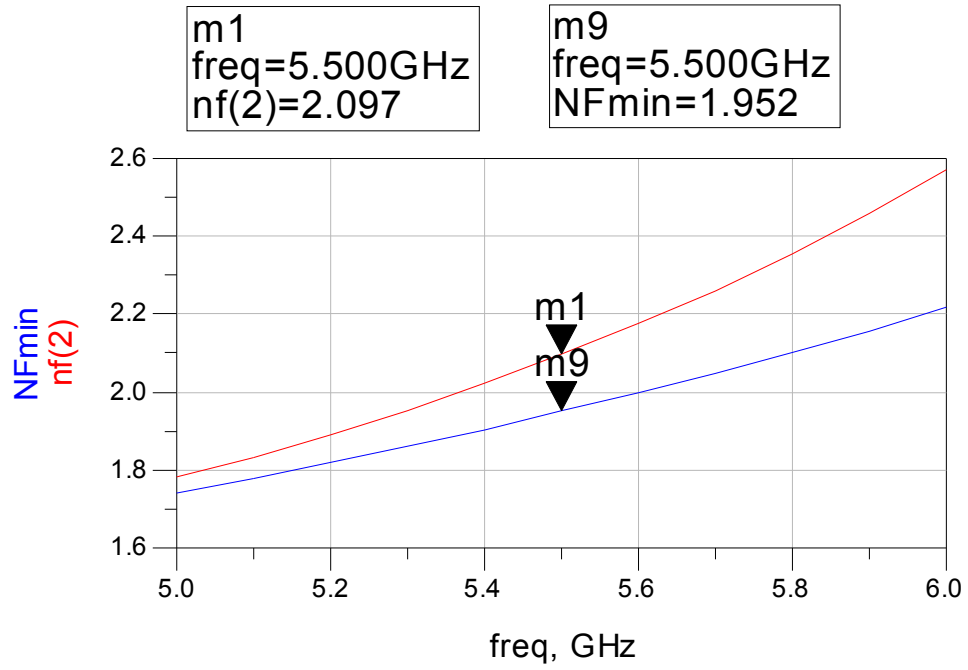
m4  
freq=5.500GHz  
S(2,2)=0.063 / 24.453  
impedance = Z0 \* (1.120 + j0.059)

m5  
freq=5.500GHz  
S(1,1)=0.694 / 109.534  
impedance = Z0 \* (0.266 + j0.672)



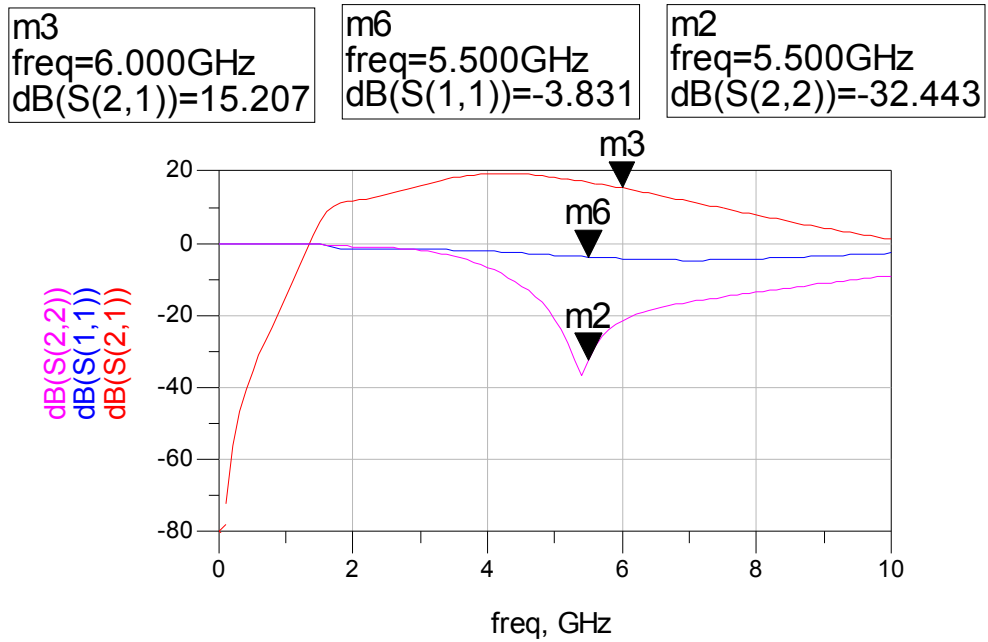
indep(L\_StabCircle1) (0.000 to 51.000)  
freq (5.000GHz to 6.000GHz)  
indep(S\_StabCircle1) (0.000 to 51.000)

### 4.1.12 Both First and Second Stage Noise Figure $nf(2)$ , Minimum Noise Figure (Nfmin)

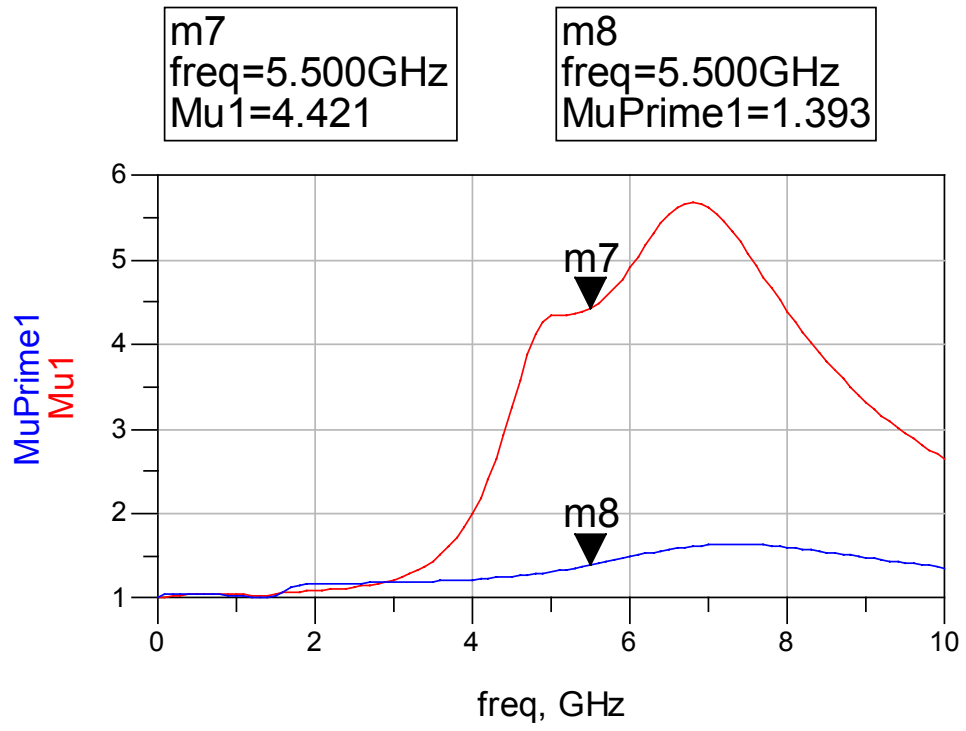


## 4.2 Non-Linear

### 4.2.1 Gain S(2,1), Input Match S(1,1), Output Match S(2,2)



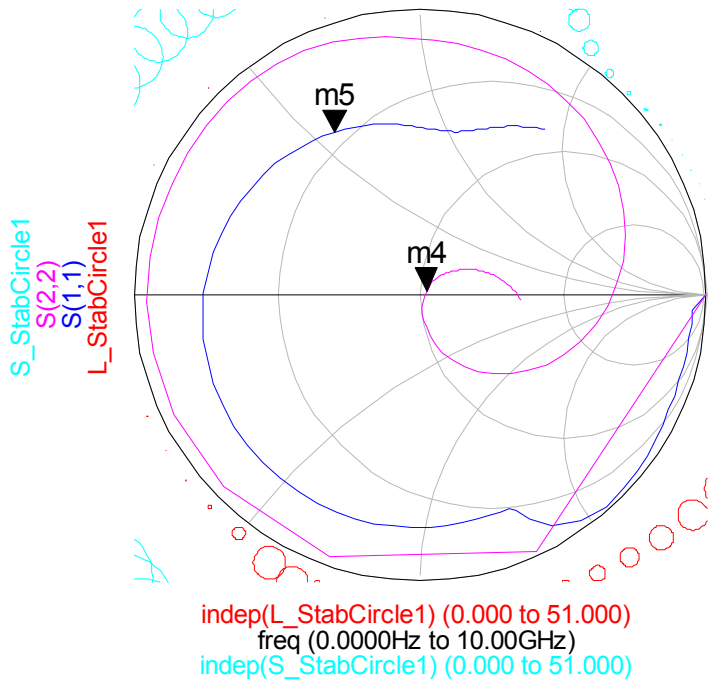
## 4.2.2 Stability



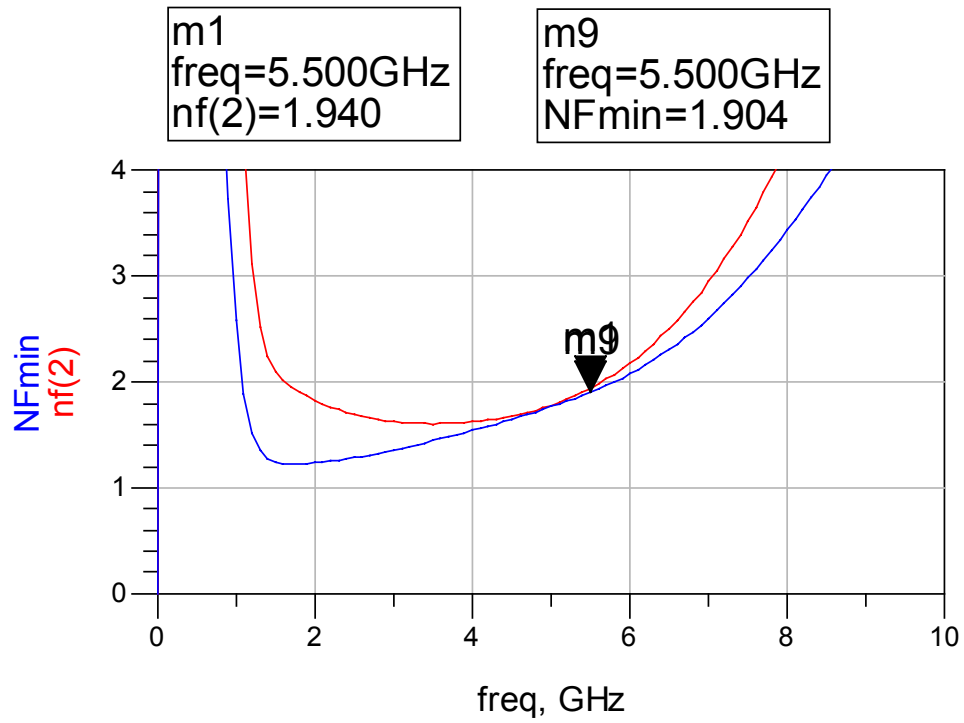
### 4.2.3 Stability (Smith Chart)

m4  
freq=5.500GHz  
S(2,2)=0.024 / 31.067  
impedance = Z0 \* (1.041 + j0.026)

m5  
freq=5.500GHz  
S(1,1)=0.643 / 117.824  
impedance = Z0 \* (0.291 + j0.565)



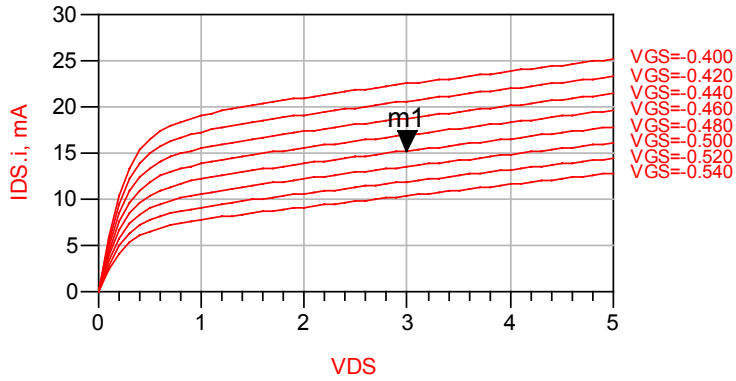
#### 4.2.4 Noise Figure $nf(2)$ , Minimum Noise Figure (Nfmin)



### 4.3 Bias

#### FET Bias Characteristics

Use with FET\_curve\_tracer Schematic Template



Values at bias point indicated by marker m1.  
Move marker to update.

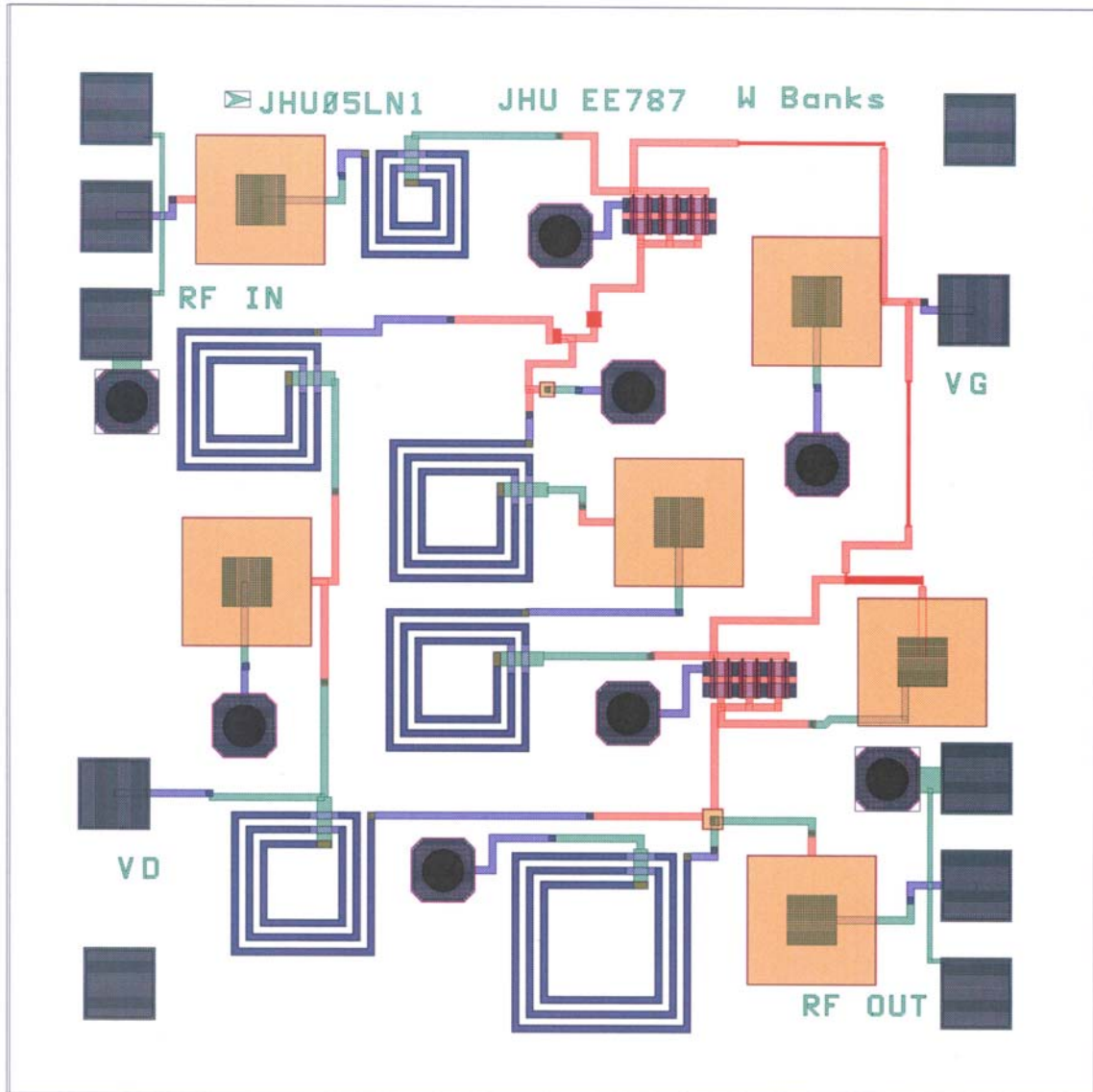
VDS	Device Power Consumption, Watts
3.000	0.046

m1  
VDS=3.000  
IDS.i=0.015  
VGS=-0.480000

### 5 Schematic







## 7 Test Plan

Verifying the design of the LNA MMIC will require the measurement of such parameters as the noise figure and S-parameters.

### 7.1 Test Equipment

The use of the following test equipment is required to measure the performance of the LNA.

- Spectrum Analyzer
- Network Analyzer
- 5 volt DC Power Supply
- Power Meter

## **7.2 Turn On Procedure**

Extreme caution should be used so as to prevent an excess of drain voltage and current from entering the circuit. The required voltage is +3 V DC and the required current is 30 mA for the LNA. Setting the correct limits on the DC supply is a must.

## **7.3 RF Measurements**

The test equipment should be calibrated prior to performing any test on the LNA MMIC. Calibrate the analyzer from 1 – 10 GHz. The noise figure meter should be calibrated as well.

## **7.4 S-Parameters Measurements**

After calibration of the test equipment, probes should be connected to the LNA and measurement of current and S11, S12, S21, S22 can be made and recorded.

## **7.5 Noise Figure Measurements**

After calibrating the noise figure meter, position the probes on the VD pad and IN input pads and record the noise figure over the band of frequencies.

## **8 Summary & Conclusion**

This report describes the design of a C-Band LNA MMIC designed to operate at 5.5 MHz using the TriQuint process. The design was simulated using Agilent Advanced Design System. The simulated model produced an LNA with gain of 15 dB or greater in the required frequency band and noise figure of less than 2 dB on a 300mm ANACHIP footprint. This designed was produced as part of the MMIC Design course taught at Johns Hopkins University of the Fall 2005 semester.

# Phase Shifter Final Report

Drew Wilson  
JHU 525.787 MMIC Design

December 12, 2005

## Abstract

A MMIC 2-bit phase shifter for the 5.8 GHz ISM band was designed using the Triquint Semiconductor TQPED process. Simulation and layout were performed with Agilent ADS. The phase shifter is one component of a duplex transceiver being built as a class exercise at Johns Hopkins University.

## Introduction

A phase shifter is a two-port microwave device whose phase response changes according to an external input. The phase shifter designed here accepts logical inputs to select from four phase states. This will be used in the signal path of each element of an antenna array. By changing the phase of the signals, the antenna array beam can be steered without physically moving the antenna.

The specifications for this phase shifter are as follows:

Frequency:	5150 to 5875 MHz
Bandwidth:	> 800 MHz
Insertion Loss:	< 4 dB (3dB Goal)
Insertion Loss Balance:	+/- 1 dB
Phase Shift:	Steps of 45 (Goal), 90, 180 Degrees
VSWR to 50 Ohms:	<1.5:1 on Input and Output
Supply Voltage:	+/- 5 Volts
Control:	TTL (Goal) or 0/-5 Volt
Size:	60 by 60 mil

## Design Approach

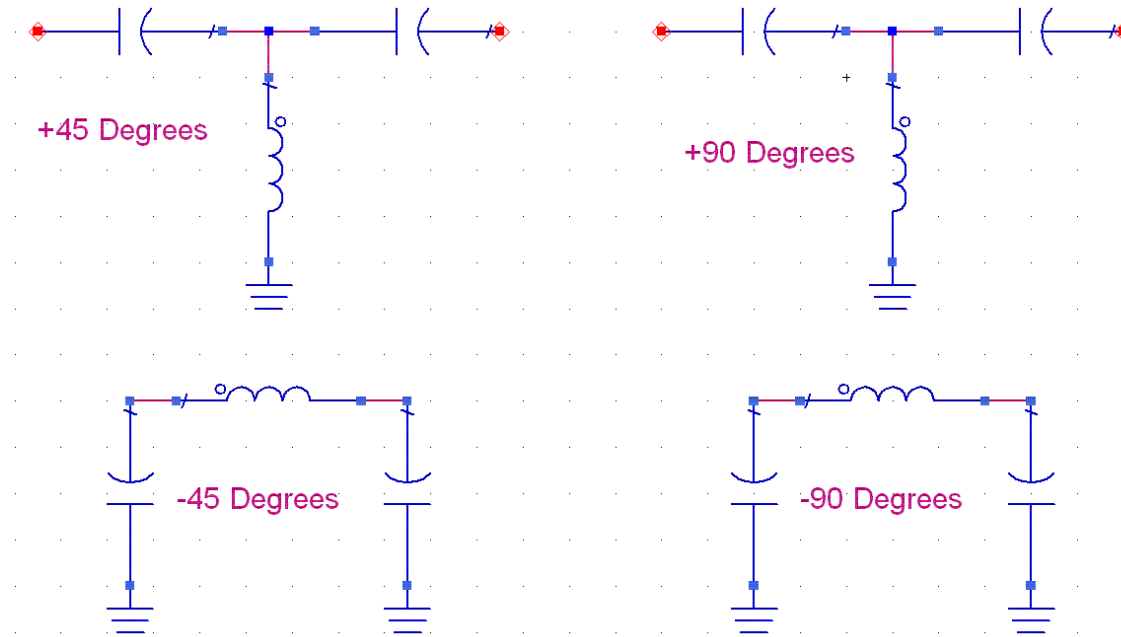
A straightforward topology was chosen to implement the phase shifter. The topology is a parallel combination of two phase filters in series with a second parallel combination of two phase filters. One filter from each parallel combination is selected with FET switches.

The first parallel combination is of filters with +45 degree and -45 degree phase shifts. The second parallel combination is of filters with +90 degree and -90 degree phase shifts. By selecting either +45 or -45 degrees and +90 or -90 degrees, the following relative phase shifts can be realized:

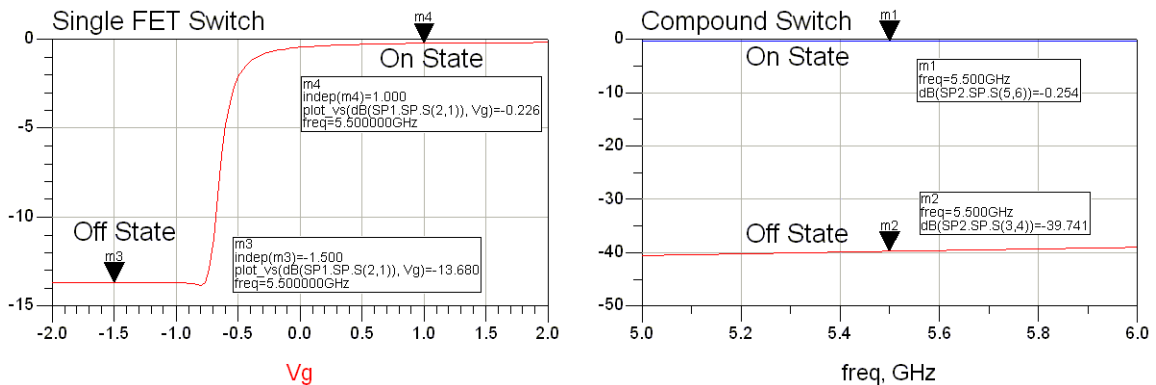
First Filter	Second Filter	Absolute Shift	Relative Shift (Subtract 45)
+45	+90	+135	+90
-45	+90	+45	0
+45	-90	-45	-90
-45	-90	-135	180

Once the general topology is chosen, the four individual filters and the switches had to be designed. For the filters, lumped elements were used to generate the required phase shift. The +90 and -90 degree filters implemented as lumped element quarter wavelength transformers. Copies of these were tuned to generate the +45 and -45 degree filters. The topology of each filter was

chosen to minimize die space usage. As can be seen in the figure below, the appropriate TEE or PI, high-pass or low-pass, topology was chosen to require only one inductor per filter.



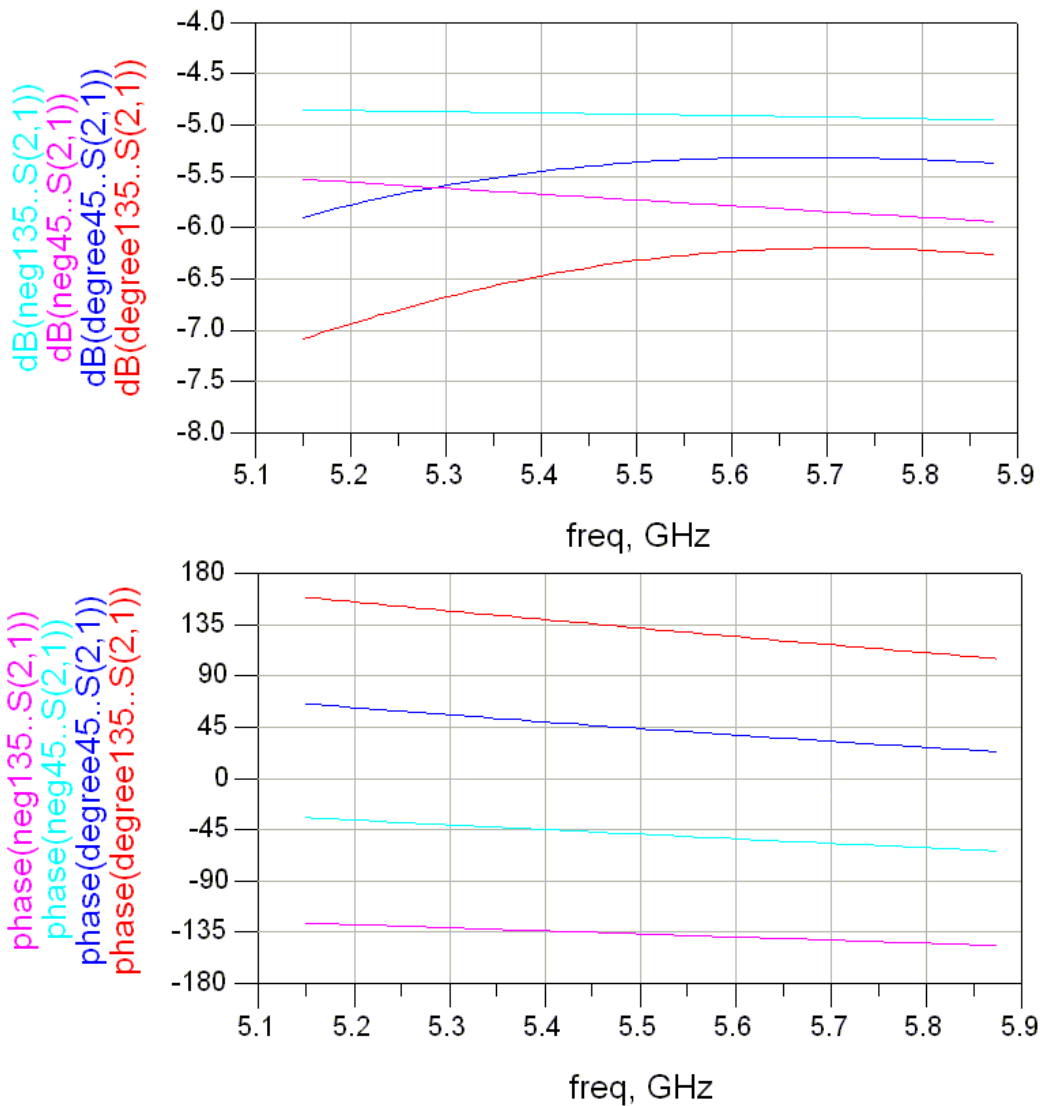
For the switches, an initial simulation of a single series FET and of a series-shunt combination was performed. Both configurations had similar insertion loss of 0.25dB. The off state of the single series FET provided 13dB of isolation while the series-shunt combination provided 40dB. For this application, the single series FET switch was chosen. It is smaller, easier to route the control voltages, and for this design the effects of the lower isolation can be absorbed into the filters. The following figure shows the on and off state performance of each configuration.

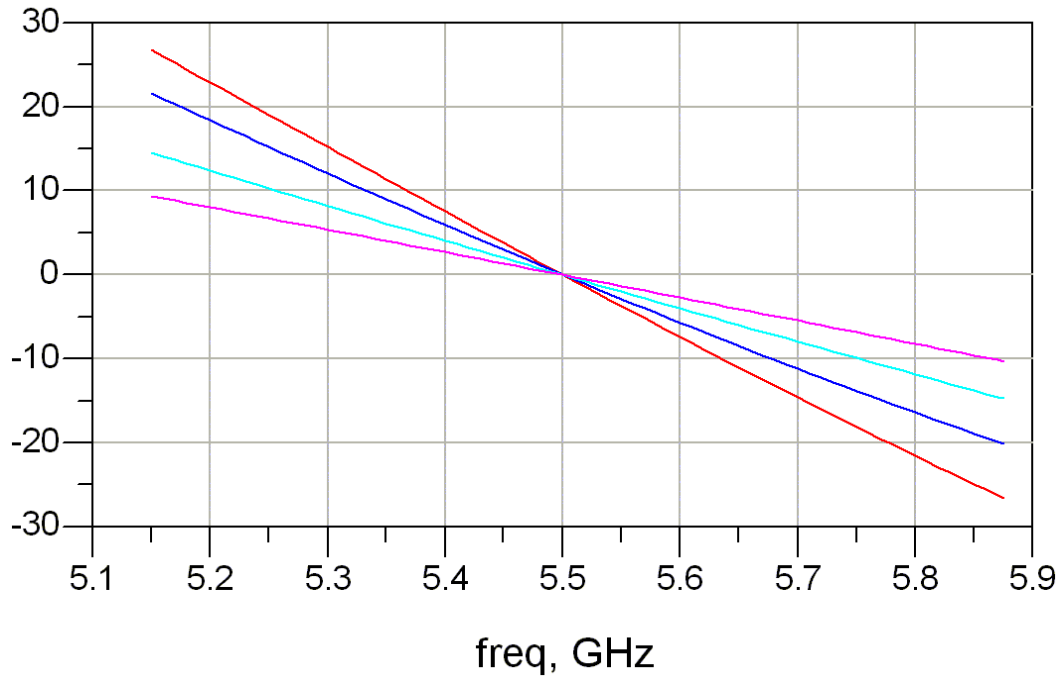


## Simulations

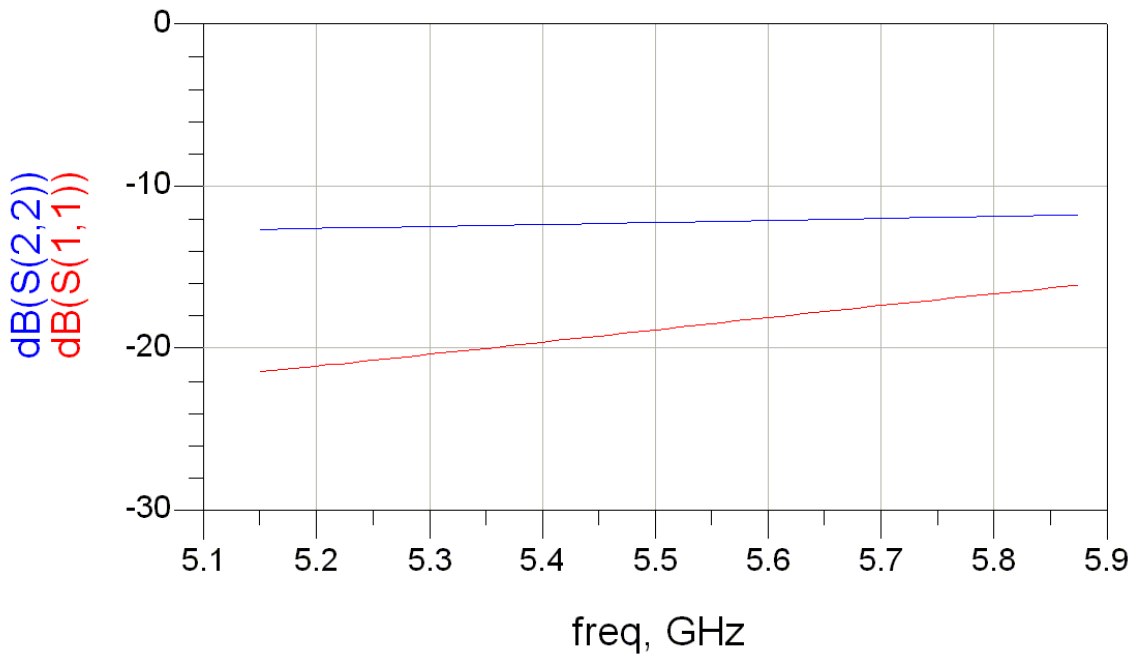
The following simulations are of the entire circuit including interconnecting lines generated in the layout. As seen in the first plot below, neither the insertion loss nor the insertion loss balance specifications were met. The mid-band insertion loss varies from  $-4.8$  to  $-6.4$  dB.

The phase of the four states are shown in the second figure below. The mid-band values show the expected absolute phase shift of  $-135$ ,  $-45$ ,  $+45$ ,  $+135$  degrees, as expected. However, the states with larger phase shift diverge from the desired value more quickly than the lower phase shifts. This is illustrated in the third figure below. In this figure the phases are normalized to zero at the center frequency. The divergence from the intended phase shift versus frequency is clearly more for the larger phase shift states. The result of this is undesired relative phase shifts at the band edges. A correction for this was not attempted in this design.





The input and output impedance match specification is VSWR of 1.5:1 on input and output. This corresponds to a return loss of  $-14\text{dB}$ . A plot of input and output port return loss is below. The impedance match specification was met on the input, but not the output. During the design only the input impedance match was monitored.

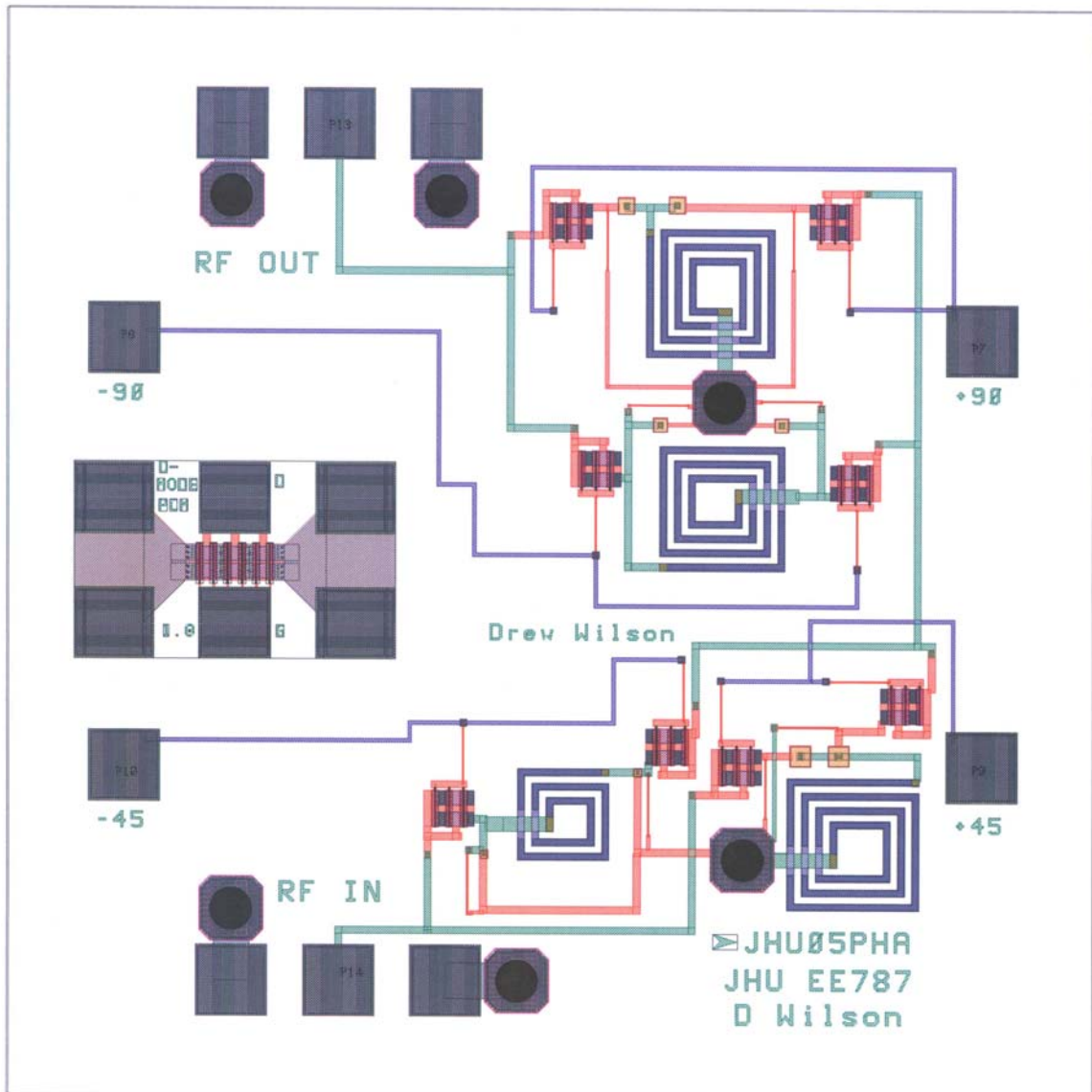






## Layout Plot

A plot of the layout follows. In this plot, the two RF ports are labeled RF IN and RF OUT. Each of these has ground-signal-ground pads on opposite sides of the die for testing on a wafer probe station. There are four DC connections to be made to the die. These are toward to four corners of the chip and spaced away from the RF connections. This is to simplify needle probe connections. These four ports are labeled -90, -45, +90, +45.



## Test Plan

### Connections

The die requires two RF connections. These are labeled RF IN and RF OUT on the die and in the layout plot above. Both ports are 50 Ohm.

Four DC connections are required for testing. DC levels are 0 and -5 Volts. Simulations show current draw for the entire die to be 1.6pA. The DC ports are 0/-5 Volt complementary pairs. One pair is labeled +45 and -45. The other pair is labeled +90 and -90. Select phase states by reading across the table below.

“-90”	“+90”	“-45”	“+45”	Absolute Phase
0 V	-5 V	0 V	-5 V	-135 Degrees
-5 V	0 V	0 V	-5 V	+45 Degrees
0 V	-5 V	-5 V	0 V	-45 Degrees
-5 V	0 V	-5 V	0 V	+135 Degrees

### Tests

S11 and S22 can be measure with any phase state. Phase and Amplitude (dB) of S21 for each of the four phase states should be measured and recorded. Measurements should be compared to the plots in the Simulations section of this paper.

## Summary and Conclusions

A 2-bit MMIC phase shifter was designed using the Triquint Semiconductor TQPED process and Agilent ADS. Specifications were given for the project. Simulations show the circuit meets some, but not all, of those specifications. The phase shifter did not meet the insertion loss or insertion loss balance specifications. The variation in insertion loss of any one filter is not more than 1dB. Therefore, attenuators could have been used to achieve the insertion loss balance specification. However, the insertion loss specification would not be satisfied. To achieve the insertion loss specification, more attention needed to be paid to impedance matching in the phase shifter. For instance, the parasitics of the switches and of the neighboring filter through the low-isolation switch need to be explicitly incorporated into the design. The method used here was to tune the filter components after the interconnecting lines were added in layout. The low switch isolation made this a difficult process because when one filter was tuned, it detuned the others. One solution to this would be to use compound FET switches, therefore better isolating the filters form one another.

# **C-BAND POWER AMPLIFIER**

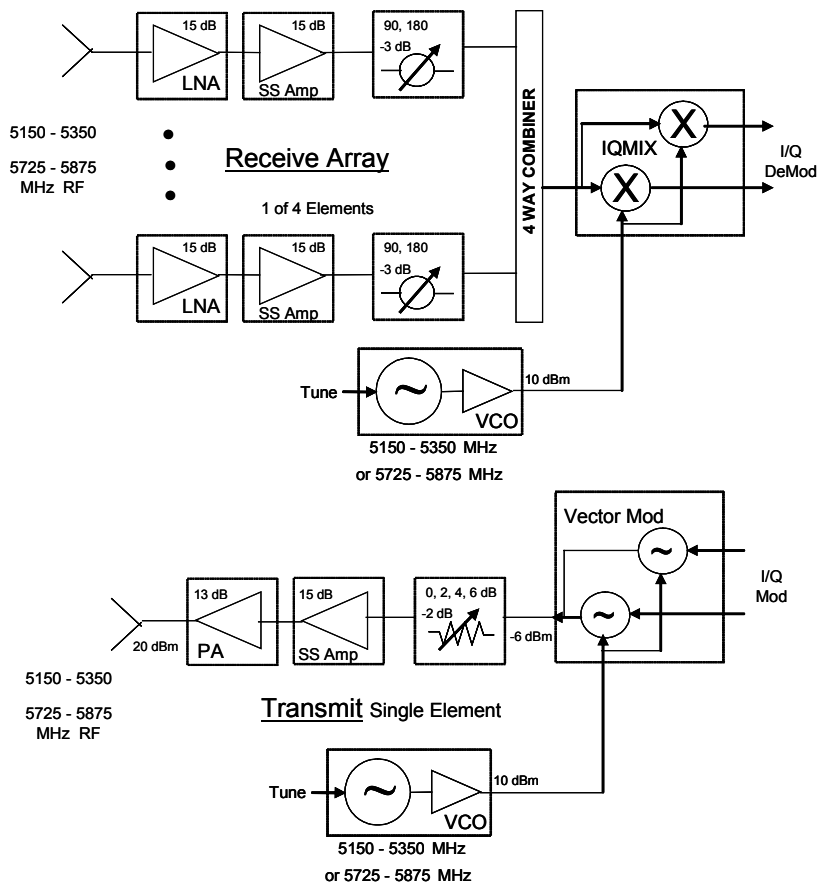
## **525.787 Microwave Monolithic Integrated Circuits (MMIC) Design**

### **Abstract**

The design of class AB MMIC Power Amplifier is described in this paper. This design is a part of a duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. The designed was implemented using TriQuint TQPED 0.5-um pHEMT process. Good performance in the frequency band of 5.15 to 5.875 GHz, center frequency 5.5125 GHz, was achieved. The PA results achieved are as follows: small- signal gain of 12.4 dB across the band; output power  $> +20$  dBm and PAE of  $>30\%$  at the 1dB compression point; VSWR of  $<1.5:1$  input and  $>1.5:1$  output was achieved.

## Introduction

The Power Amplifier designed in this project is part of duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies shown in Figure below. The PA is in the transmit chain and therefore requires to be highly efficient and linear as well. Class AB bias was chosen because it gives a good tradeoff between the 2 requirements: efficiency and linearity. The most important specification to meet is the output power level and power added efficiency.



Chip Set for the 5150 - 5350 MHz WLAN and  
5725 - 5875 MHz ISM Bands

*Fig.1: C-Band duplex transceiver*

## Design Approach

Based on the specification given for this design as shown in table 1 below, the device size, topology, and bias was chosen. The chip size to be used was 60 X 60 Mil, which posed a challenge on layout of 2 stage amplifier. The first design approach was to design a single stage PA biased at class AB using Cripps design method [1]. The drain voltage was chosen based on the power supply limitation to 5 Volts. A previous PA design done in class using TriQuint 6X50 0.5  $\mu\text{m}$  Dmode PHEMT showed good results and therefore the same device size employed in this design.

	SPECS	Pre-Layout	Post-Layout
Frequency	5150 – 5875 MHz	Yes	Yes
Bandwidth	> 800 MHz	Yes	Yes
Gain (Small Signal)	>13 dB; goal 15 dB	13.36dB	12.4dB
Gain Ripple	$\pm 0.5$ dB max.	Yes	Yes
Output Power@ 1 dB compression point	>+20 dBm	21.003 dBm	20.226 dBm
Power Added Efficiency	>20 %; 25% goal	36.4 %	31.44 %
VSWR (50 $\Omega$ )	<1.5:1 input & output	1.309:1 input; 2.45:1 output	1.249:1 input; 2.379:1 output
Power Supply	+ 5 and – 5 V	Yes	Yes
Chip size	60 X 60 mil ANACHIP	Yes	Yes

*Table 1: Design specifications and goals for the PA*

The figure below shows the I-V Characteristics of the TOM3 model and a marker indicating the biasing for this device. The Gate Voltage,  $V_{gs}$ , is equal to -0.1 V at 56 mA and  $V_{ds}$  of 5 V.

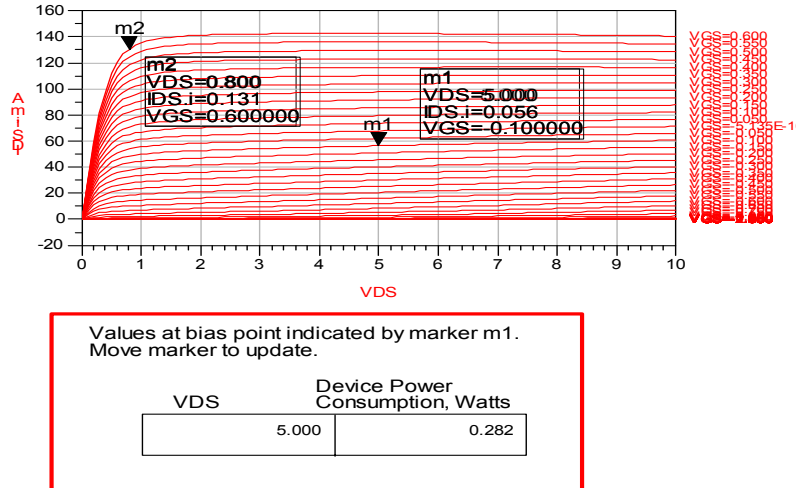


Fig.2: I-V Characteristics of the pHEMT model

The design of the PA was first done using ideal lumped elements. Those ideal elements were replaced using the corresponding models from the TQPED design kit. Resistors and capacitors were easy to synthesize, but inductors had to be carefully modeled using an iterative tuning process. Final layout was done using microstrip connections. The final design was then simulated to give the results shown in table 1.

### **Trade-off**

The trade-off for this design was directly associated with the design specifications that were the most important. In the case of PA design these specifications are output power and power added efficiency (PAE). Since PA consume most of DC power in a RF chain, hence require the PAE to be high. The higher this value is the better DC power consumption design is. The specification was >20 % and 25% goal. The final design was able to achieve 31.4 %. The output power goal of >20 dBm (20.2 dBm) was achieved. The small signal gain of 13 dB across the band was compromised to a final of 12.4 dB. The gain would have been achieved by either increasing device size or using a second stage but since output power and PAE goals were met the extra mile was not taken due to complexity of network for the 2 stage layout. The input VSWR was met because the input match is conjugately done to give the best match at the input, while the output VSWR was not met due to the nature of output match, which is done for the best power as supposed to the best match.

## Schematics

The figure below shows the final PA design using Triquint elements without the microstrip interconnections. The DC bias is also displayed. The intended bias of 56 mA  $I_{ds}$  and  $V_{ds}$  of 5 V was slightly changed by the use of real elements to 67 mA and 4.72 V respectively, which can be lived with. The design includes input matching network, L22, stabilizing resistor, R3, output matching network, L21 and C16, blocking capacitors, C11 and C13, DC feeds, L20 and R4, at the drain and gate respectively. The ideal inductors L10 and L19 represents bond wires to the DC power supplies. The capacitors C15 and C12 provide RF ground to avoid the RF interference with the DC supply.

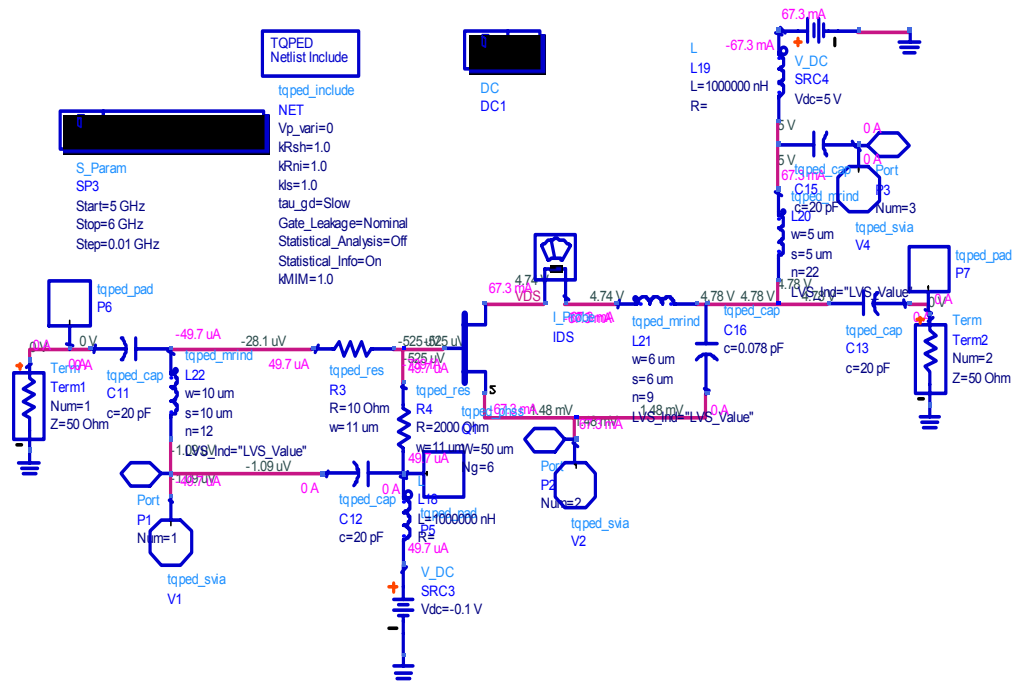


Fig.3: Schematic showing bias of the device.

## Output Matching Network (OMN) using Cripps Method

Output matching network is the first network to be done in the PA design. The Cripps method [1] is employed.  $R_{cripps}$  was determined from the DC load line (load line dictated by markers m1 and m2 in the Figure 2 plot).  $R_{cripps}$  was calculated to be 67.8  $\Omega$ . An RC network was then tuned to model S22 from which Cds could be determined. The final load used according to Cripps is  $R_{cripps} || C_{ds}$ . Figure below shows the model for S22 of device (Term1 network) and Cripps load (Term2 network).

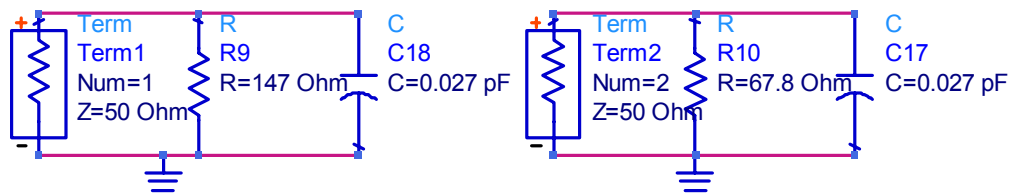


Fig. 4: RC network for Power match

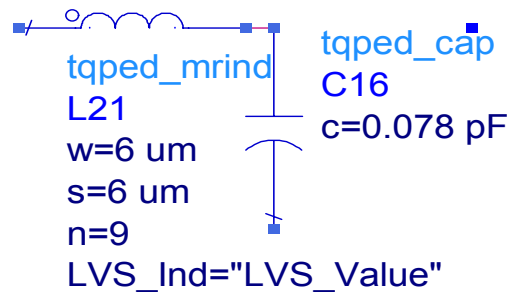


Fig. 5: Final Triquint Element OMN

## Input Matching Network (IMN)

The input matching network was a conjugate match to avoid the loss of any more gain within the design. The network determined was made up of 2 elements as shown below, but it produced a very narrow band. A compromise of one element (L22 in figure 3 above) was done and the value was optimized to give a broader frequency response.



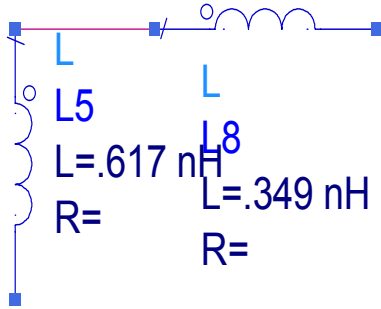


Fig. 6: original Ideal IMN

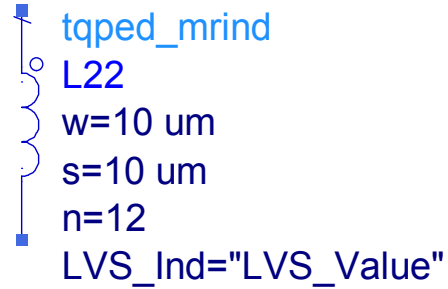


Fig. 7: Final Triquint Element IMN

### Final PA design

Once all the networks are put together, the final design requires the microstrip interconnections for a fair comparison between the schematic and layout. The figure below shows the final schematic with interconnects and matching networks tuned to compensate for the microstrip interconnects losses. The schematic also includes the Ground-Signal-Ground (G-S-G) pads and DC supply pads.

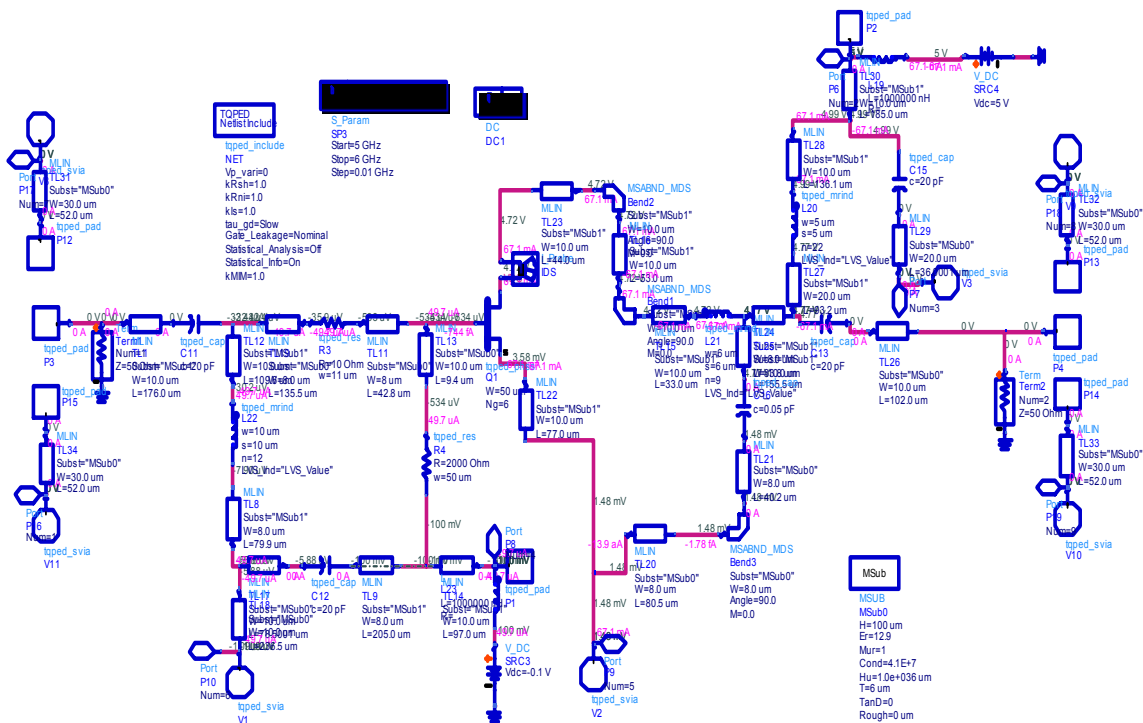


Fig. 8: Final Schematic with Microstrip interconnections

## Simulations

Linear simulations were done across 0.5 – 10 GHz. The stability plot below shows stability across the whole band. The Linear simulation results were done both before and after microstrip interconnections. The displayed linear results include S21, S11, S22 and VSWR (with a closer look at the frequency band of interest).

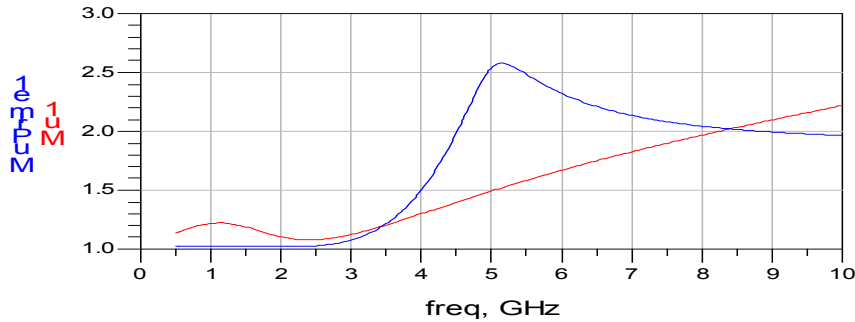


Fig.9: Stability factor plot

## Pre-Layout results (Before microstrip interconnections)

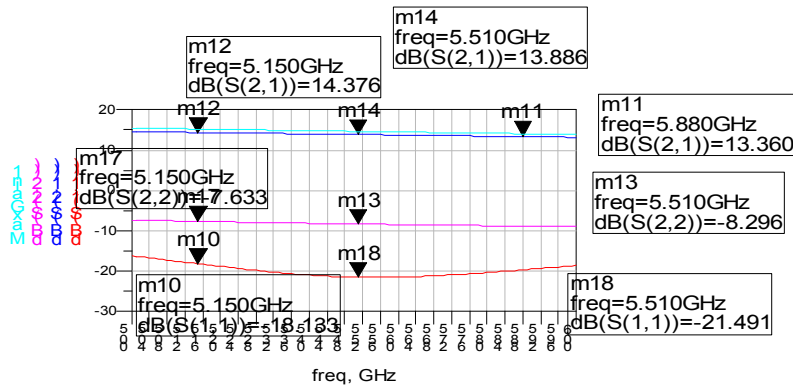


Fig.10: S-parameter simulations

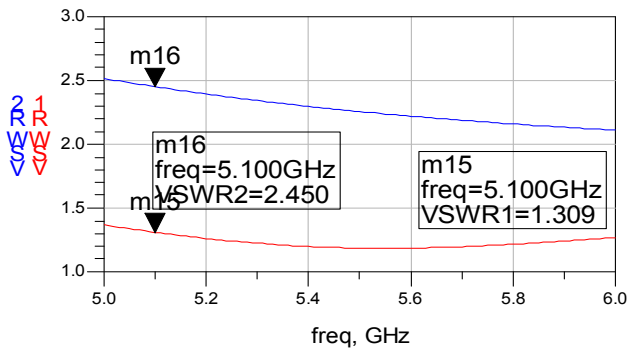


Fig.11: VSWR (blue=output; Red=input)

Post-Layout results (after microstrip interconnections)

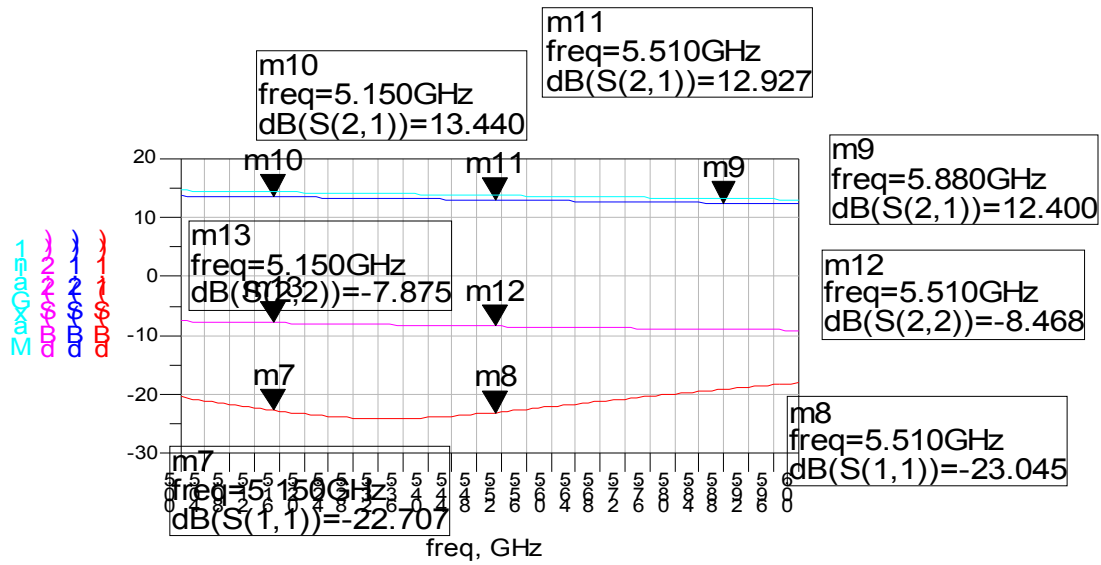


Fig.12: S-parameter simulations

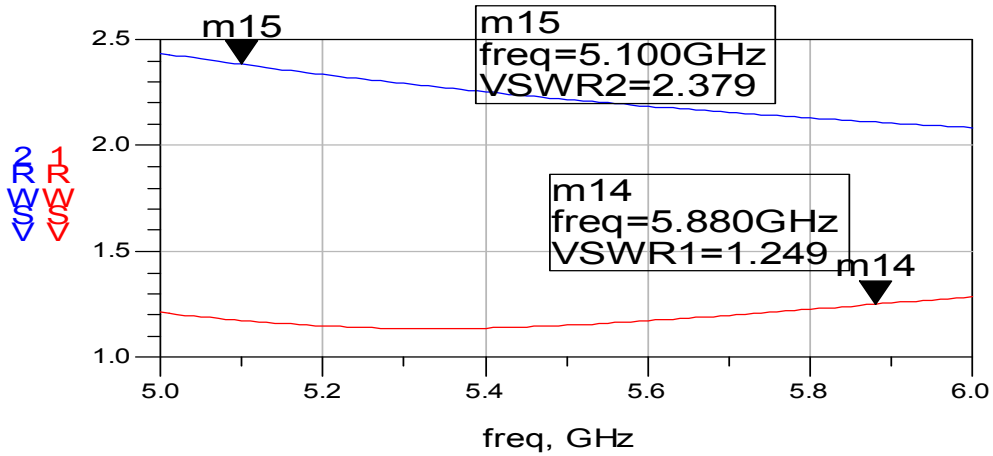


Fig.13: VSWR (blue=output; Red=input)

It can be noted that before the microstrip interconnections, figure 10, that the gain requirement had been met, but slightly changed with the interconnections added, figure 12. The VSWR improved with interconnections.

## Non-Linear Simulations

Harmonic balance simulation was done to display non linear results, Output power and Power Added Efficiency. The results are also displayed for pre- and post- layout. These plots also include a gain plot, and a linear plot for determining 1 dB compression point given as 8.2 dBm input power. The left y-axis scale is for Output power, gain and linear plot, while the right y-axis shows the Power Added Efficiency scale.

### Pre-Layout results (Before microstrip interconnections)

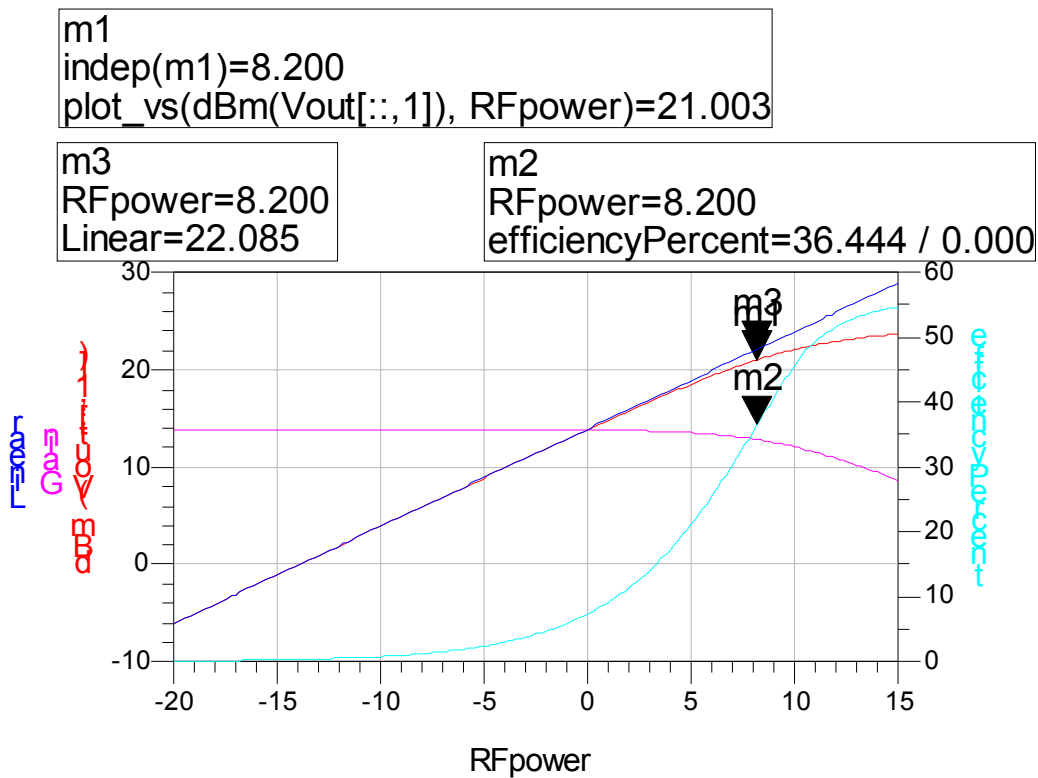


Fig.14: non-linear simulations

Post-Layout results (Before microstrip interconnections)

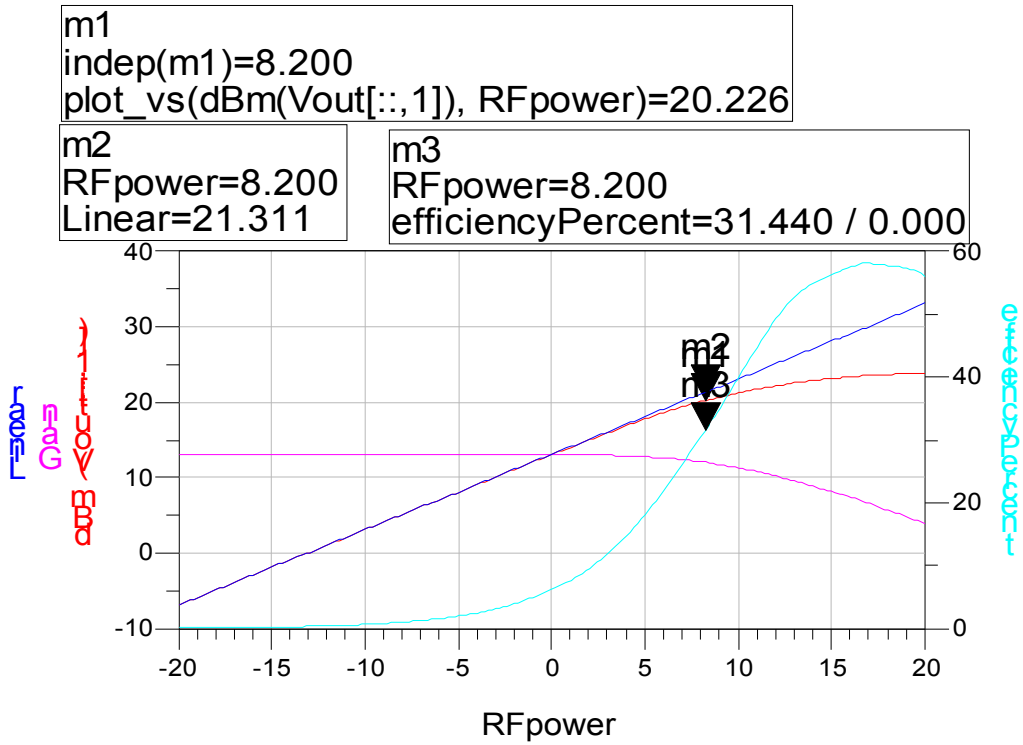


Fig.15: non-linear simulations

Finally dynamic load line is displayed in the figure below.

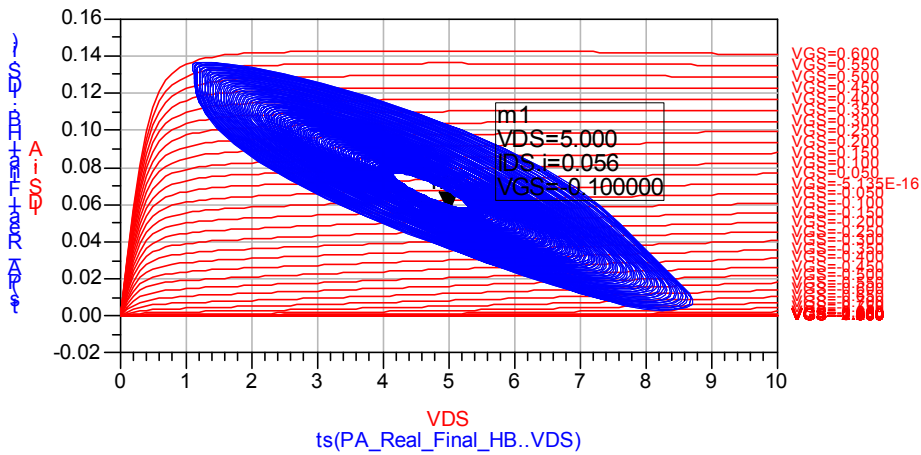
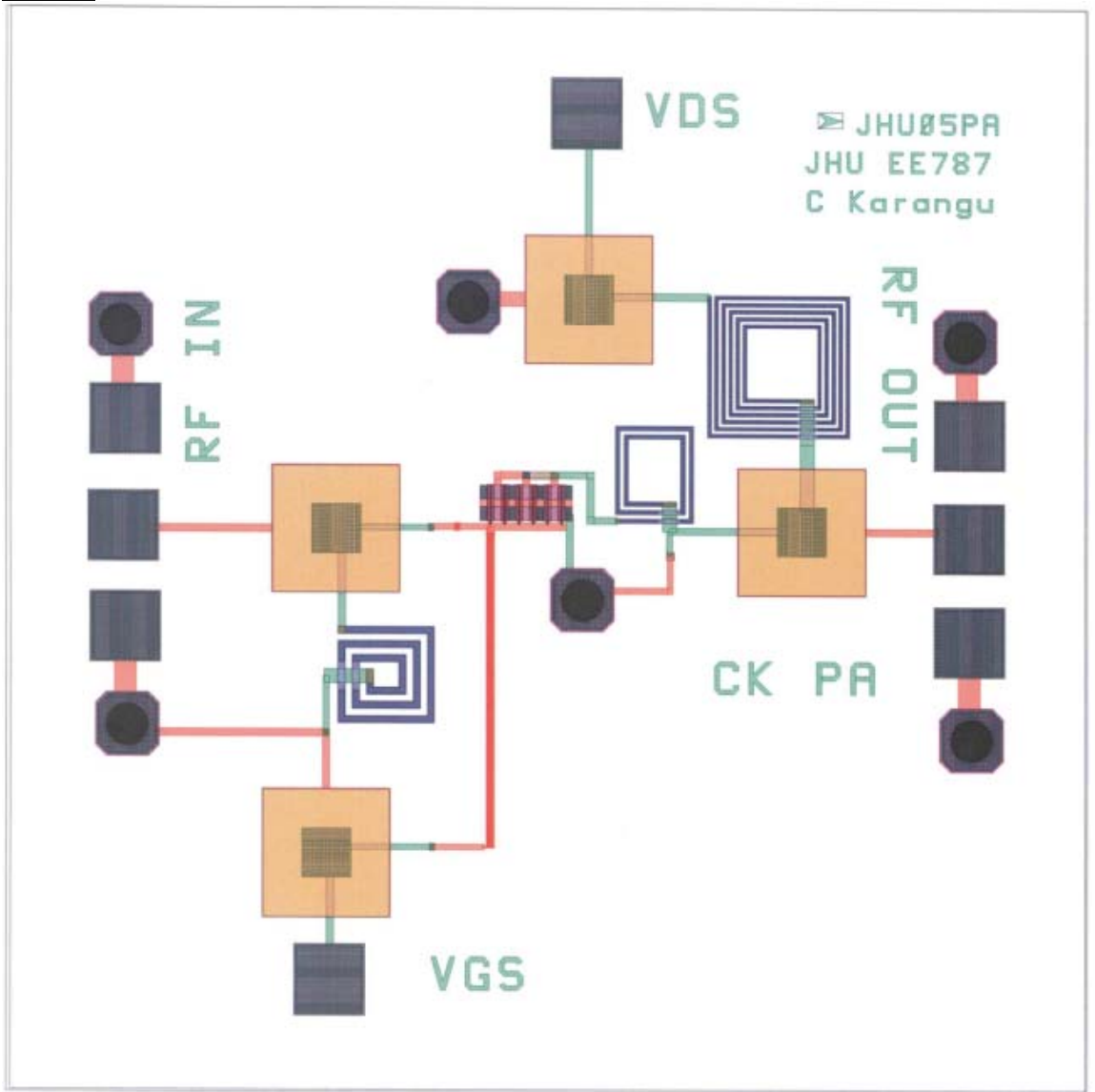


Fig.16: Dynamic Load Line

Layout



## **Test plan**

Ground-Signal-Ground (G-S-G) pads are required in order to perform RF measurements using the HP 8510 Vector Network Analyzer and Cascade probe station. These pads are shown in the Final Layout figure above and are labeled RFIN and RFOUT for the RF input and output respectively. RF probes will come in from the left and right of the chip for input and output, respectively as shown in the layout.

For the DC bias, pads are put on top and bottom of the chip for VDS and VGS bias respectively. 5 and -0.1 volts supplies will be connected to the VDS and VGS pads respectively.

The VNA 8510 will be used to measure all linear measurements while the spectrum analyzer will be used to perform non linear measurements.

Below is a list of all equipment to be used.

### **Test Equipment:**

- Agilent 8510 VNA (45 MHz to 26 GHz)
- Cascade Model 43 wafer probe station with up to 4 RF probes & 4 DC needle probes
- Synthesized signal generators to 26 GHz
- Spectrum analyzer to 18 GHz

## Conclusion

The design of PA for the C-Band Transceiver was successfully done. All the goals were not met but the most important ones were met, namely Power Added Efficiency and Output power of, 31.4 % and 20.226 dBm respectively. The input VSWR of 1.2 was achieved meeting the requirement of  $<1.5$ . The specifications that were not met were not far off, hence the settling of the final design. One of these specifications was the small signal gain. It was supposed to be 13 dB across the band but the design yielded 12.4 dB gain across the band. A difference of 0.6 dB was not that critical to make the decision to do a 2 stage design. Output VSWR achieved was 2.37 but this was expected to be off due to the nature of the output matching design. The design and layout were both done using ADS circuit simulator. This exercise was very informative and enabled tremendous growth towards becoming RF MMIC designer.

## References

1. Steven C. Cripps, "RF Power Amplifiers for Wireless Communications," Artech House, 1999, chapters 3, 5, 8.
2. Penn, John and Reece, Michel. *Class Handouts*. JHU/APL. 2005.



## Making Microwaves MMIC VCO Design Via Impedance Matching

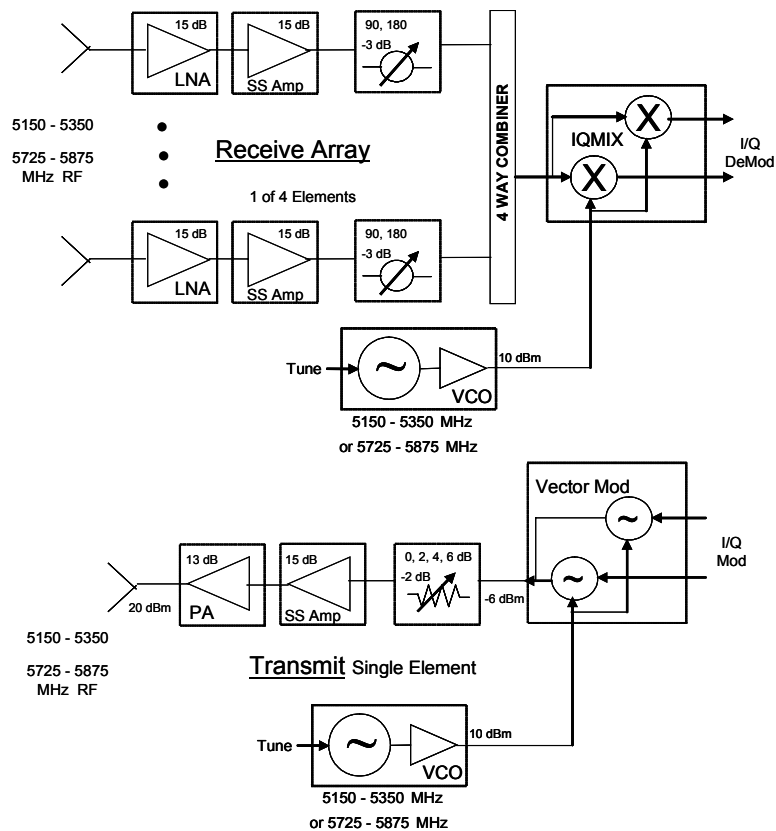
Edward Heine

### Abstract

This final design report for the John Hopkins University Fall 2005 MMIC Design course details the design of an MMIC VCO. The MMIC VCO is designed on the TRI-Quint TQPED process. The VCO design goals are a tuning range of 5150 to 5350 MHz or 5725 to 5875 MHz, maximum 5 volt supply, 0 to 0.6 volts for control, lowest phase noise and an output power greater than +7 dBm. The emphasis of this report is on making the VCO cover both tuning ranges and choosing the varactor. An on chip Emode PHEMT device is used for the varactor. Microwave Office is used for the simulation and layout.

## 1. Introduction

The design project for the Fall 2005 MMIC Design class at The Johns Hopkins University is a duplex transceiver employing a receive array for the C-band HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequencies. For transmission, a direct vector modulator is used to transmit data onto the carrier. For downlink, an I/Q down converter is used to derive modulated data. The frequency carrier consists of a VCO. The VCO operates from 5150 to 5350 MHz, or



Chip Set for the 5150 - 5350 MHz WLAN and  
5725 - 5875 MHz ISM Bands

Figure 1 Project block diagram

5725 to 5875 MHz, to cover the WLAN and ISM frequencies. A phase shifter chip implements a 2 bit phase for the receive array. Transmit level control is implemented with the MMIC attenuator chip. Each element of the receive chain array consists of an LNA and a driver amplifier in cascade, followed by a phase shifter. The transmit path employs a driver amplifier feeding a 100 milliwatt power amplifier. Nine unique MMIC designs make up the S-band transceiver. Each design is to be contained on a 60 mil square die in the TQPED process. The proposed block diagram is shown in Figure 1.

The emphasis of this report is on the VCO design and test procedure. The VCO is designed on the Tri-Quint TQPED process. Microwave Office is used for the simulation and layout. Utilizing the device's small signal parameters, the oscillator is designed using the reflection method. A non-linear simulation was ran to check the output power and phase noise. No optimization is done based on the non-linear simulation. The drain and source of an Emode PHEMT is grounded to make varactor using the TQPED process. The design chronicles the design process. Using the available 60x60 mil die area the circuit is laid out. A test procedure is detail in the test section and the expected results are summarized in the conclusion section

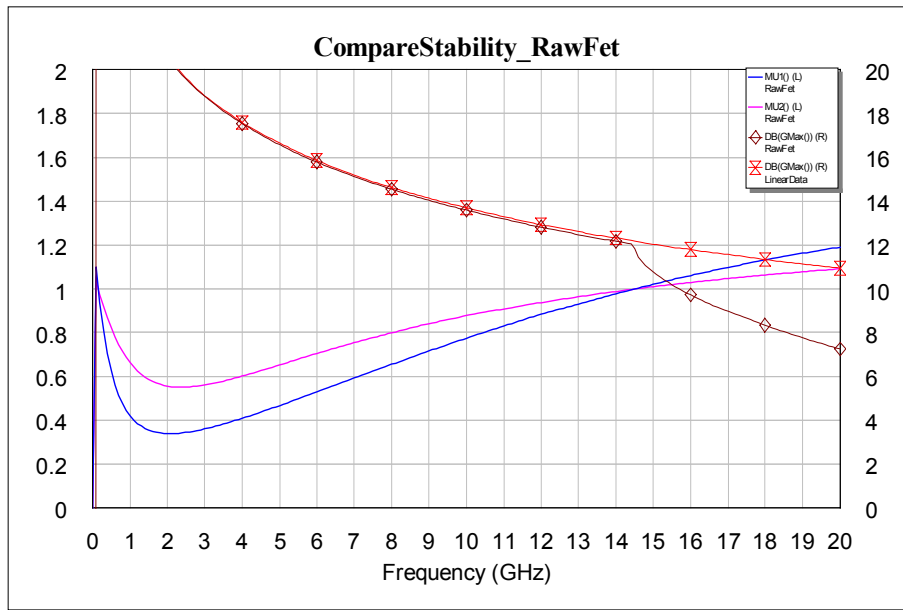
## 2. Design

The VCO is designed using the reflection method (often called negative impedance method) of oscillator design. The essence of this method is to reduce a non-linear three terminal device to a linear two port equivalent circuit and match the two ports appropriately. In this instance the PHEMT (3 terminal device) gate is taken as one port and the drain is taken as the other port. It is accepted that if the device is oscillating in one port, it must also be oscillating in the other port. The output can be taken at either the drain or the gate. To achieve maximum output power the drain is chosen for the output. This leaves the gate for the resonant circuit. Now that the function of each port is identified, like most other microwave designs, the linearized circuit is now an impedance matching task. Unlike other microwave designs, choosing the proper terminating impedance is not a strait forward task and requires iteration. The details of the VCO impedance matching are chronicled below.

The operating point was chosen to meet the power requirement ( $V_d=3.0$  volt,  $I_d=15$  mA) and reduce the noise.

### 2.1. Examine FET to determine topology

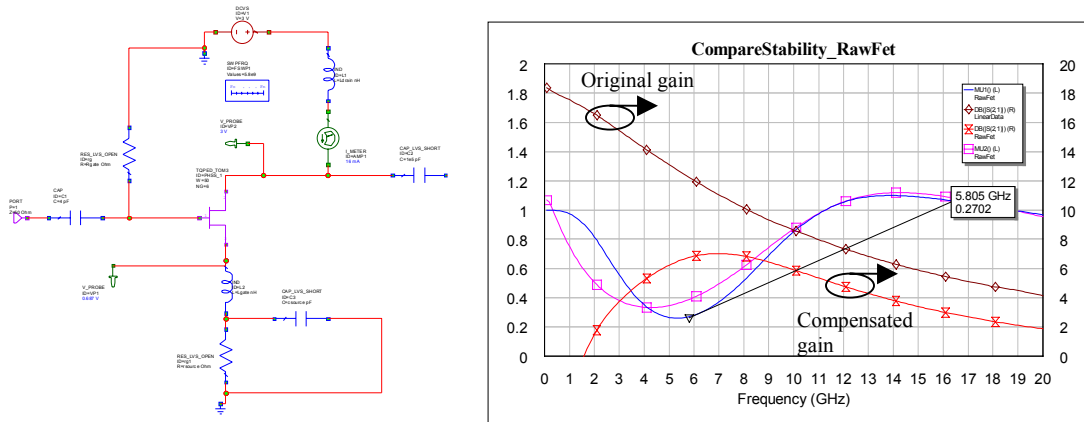
The gain and stability factor of the non-linear PHEMT model is plotted in Figure 2. The PHEMT's measured s-parameter data is also plotted to increase confidence in the non-linear model. The non-linear and linear model agree up to ~14 GHz. This is sufficient for this design.



**Figure 2** Gain and stability of PHEMT. Gain and stability shown for linear and no-linear model.

The device has a lot of gain at the lower frequencies and is conditionally stable. Compensation must be added to the device to reduce the lower frequency gain and stabilize the device outside the desired oscillation frequency range. This must

be done to insure the oscillation occurs at the desired frequency. The compensated device and its response is shown in Fig. 3. The device is compensated in the source. This works out splendidly because a bias resistor must be added to utilize a single supply bias.

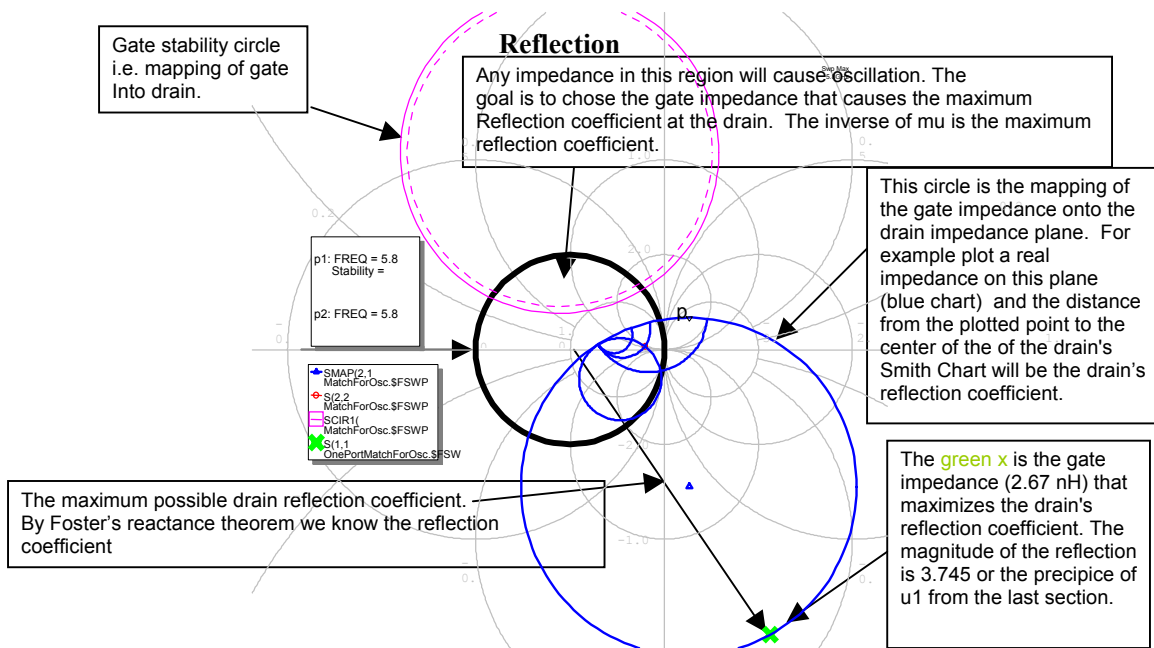


**Figure 3** On left the compensated device. Plotted on right is the compensated device's response

Referring to Fig. 3, notice the stability factor is 0.27 at 5.8 GHz. The stability factor relates to the magnitude of the reflection coefficient. As a rule of thumb this should be  $\sim 0.33$  (the smaller the coefficient the less stable the device.) Because of the varactor loading effects, the device is made slightly more unstable than usual.

## 2.2. Choosing the gate load for oscillation

Now that the device is compensated and biased the gate matching requirement can be determined using the 2 port circuit response. Figure 3 will be used extensively to determine the proper gate matching requirement.



**Figure 4** Plot showing the drain's reflection coefficient.

Figure 3 is a plot of the drain's (output) reflection coefficient at 5.8 GHz. The heavy black circle is the boundary of the unit Smith chart. The pinkish circle is a stability circle mapping the gate's impedance. Choosing a gate impedance in the overlapping region can cause the drain reflection coefficient to be greater than unity i.e. oscillate. The problem is choosing the best gate impedance. A reasonable criterion is to select the impedance which maximizes the drain's reflection coefficient. Recall we know the maximum drain reflection from the last step,  $1/u_1=3.745$ . A convenient way to determine the gate impedance is to map all possible gate impedance's onto the drain's reflection coefficient's plane. The blue circle is this mapping (very nice feature of Microwave Office). The green X on the mapping (blue circle) represents the maximum drain reflection coefficient. This is verified by replacing the gate with the requisite gate impedance (2.67 nH) and plotting the drain reflection coefficient. As expected

the drain reflection coefficient is 3.7. The gate impedance should be 2.67 nH for a maximum drain reflection coefficient.

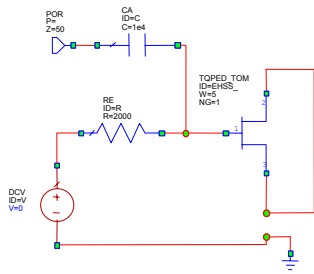
### 2.3. Designing the varactor

The source and drain of a PHEMT is grounded to a make varactor. The critical parameters are the available tuning range and the Q. Two varactor configurations were considered, a 6 finger device or a 10 finger device. The equivalent circuit model for each device is determined and used for comparison.

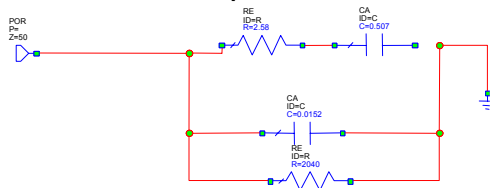
The equivalent circuit model and the matching between the model and the actual device are shown in Figure 4. Notice the model accurately matches the device over .1 to 20 GHz. This indicates the model is good.

Table 1 shows the capacitance and ESR for a 6 finger and a 10 finger device over the tuning voltage. The 10 finger device has a lower ESR. The 10 finger device will be used in this design.

### Varactor test circuit



### Varactor equivalent



### Model

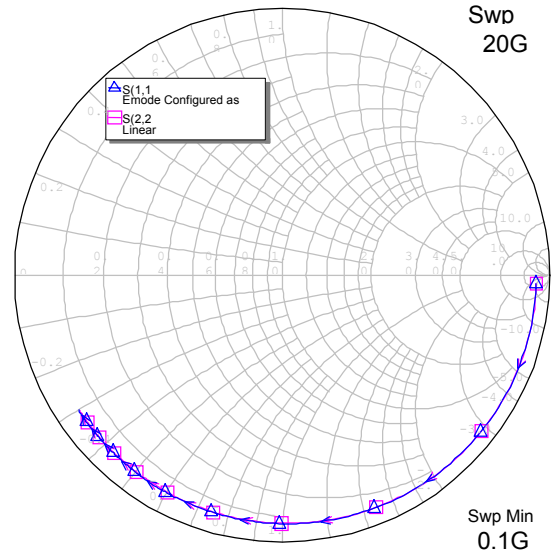


Figure 4 Varactor model

Table 1 Table of varactor capacitance and ESR for a 6 finger and 10 finger device.

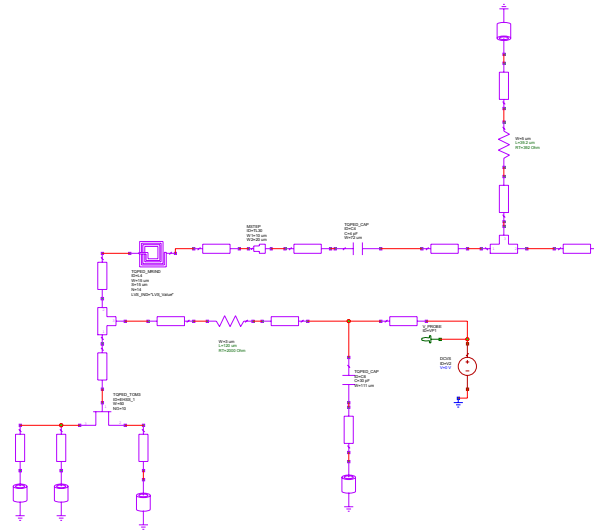
Vtune	6 Finger (pF)	6 Finger (ohms)	10 finger (pF)	10 finger (ohms)
0	0.249	6.9	0.507	2.58
0.2	0.381	5.8	0.78	2.58
0.4	0.7	4.9	1.29	2.58
0.6	1.32	4.3	2.3	2.25



#### 2.4. Design the gate matching network.

Now that the varactor model and the desired gate match has been determined, the gate matching network can be designed. The gate circuit is shown in Figure 5.

The ideal gate match was an inductor. The limited Q of the inductor and varactor

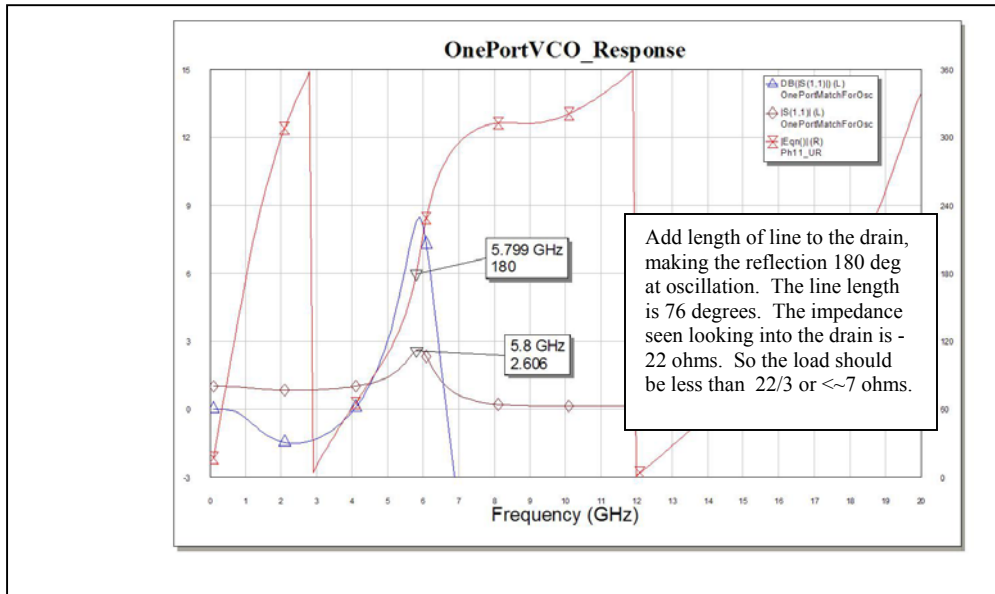


**Figure 5 The gate circuit with varactor.**

make realizing this match over a wide frequency range difficult.

#### 2.5. Drain/load matching

The load circuit should present the correct phase rotation and loading as determined in Figure 3. The correct phase is 180 degrees i.e. rotating the reflection coefficient to resonance. The resonance type can be read off the Smith chart. The resonance is series. Note the gate match from the previous step is used to determine actual matching values. A rule of thumb is to make the loading impedance one third the negative impedance.



**Figure 6. Drain reflection with gate and source match. The output is and ideal match.**

The ideal match was converted to a 2 element match at a single frequency. This simple matching circuit may not be sufficient, because the reactance slope has not been matched. At this point in the design the circuit was laid out and design rule checked. A more complex output matching circuit was designed. The more complex matching circuit had trouble fitting into the available space. Due to time requirements the decision was made to go with the simple output matching circuit that had passed the design rule check. The circuit passed design rule checking and no further iterations were performed.

## 2.6. The VCO response

The completed matched circuit is shown in

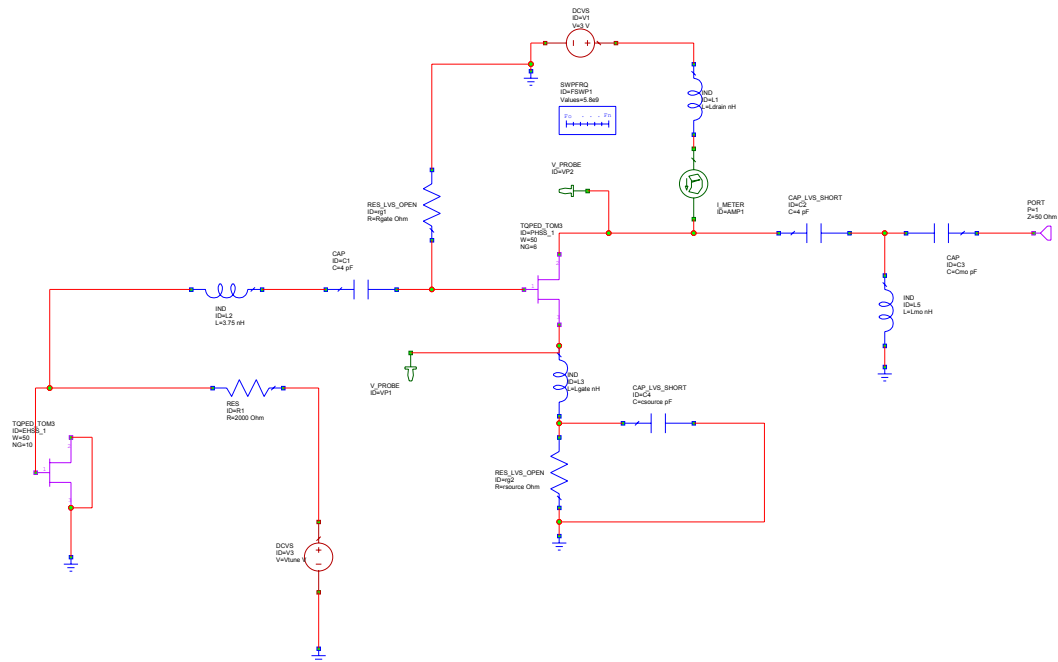


Figure 7. The VCO

The output reflection coefficient for  $v_{tune}=1$  and  $0$  volt is shown in Figure 9 and Figure 8. The VCO should operate over the full range. The reflection coefficient is small at the lower end on the range and may not oscillate.

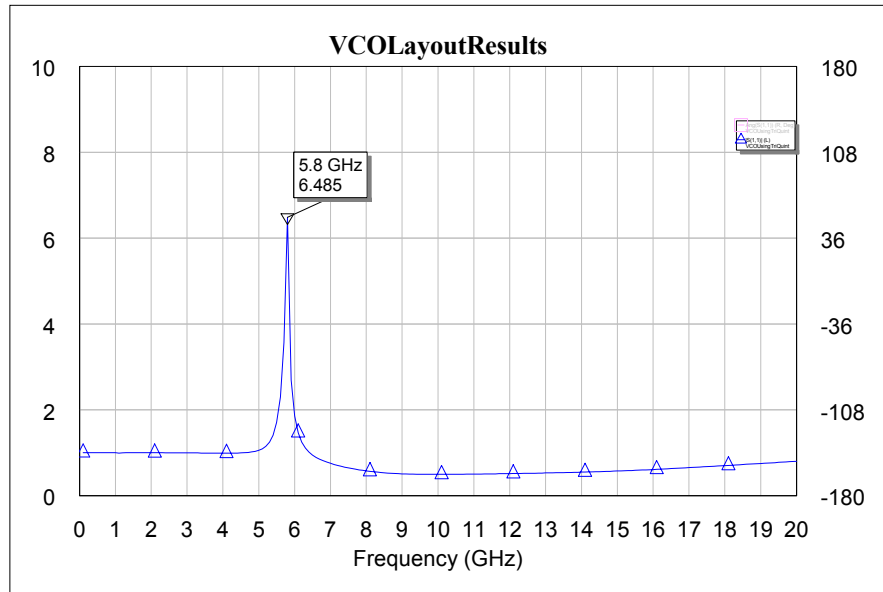
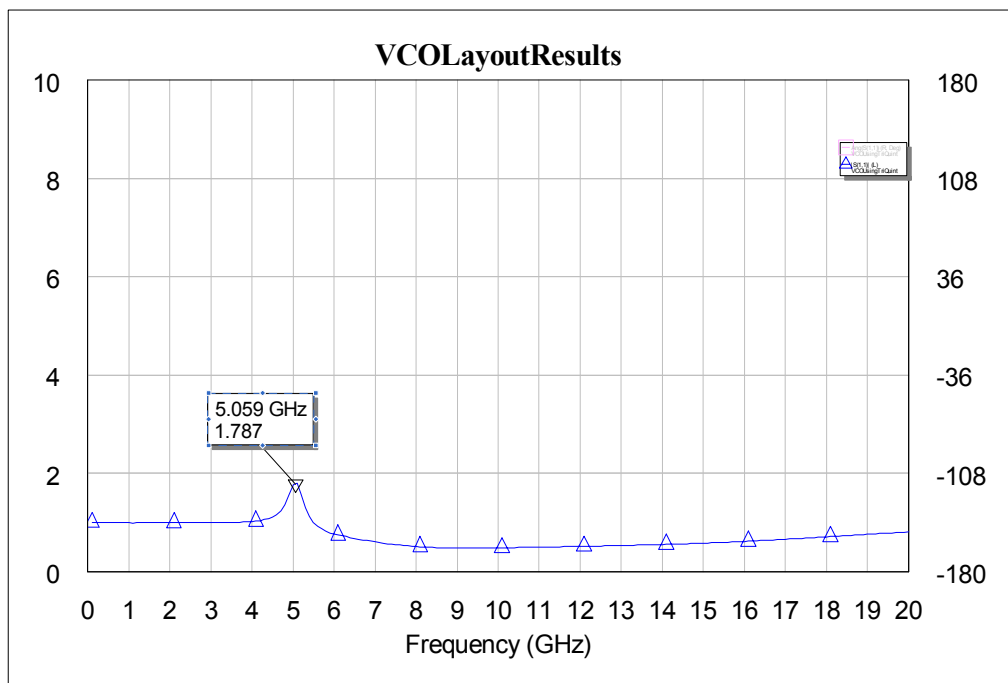


Figure 8. Drain reflection of VCO vtune=0 volts



Notice the reflection coefficient in Figure 9 is only 1.7. The rule of thumb was to have a reflection coefficient of ~3. In Figure 8 the reflection coefficient is 6.4, much greater than the desired 3. The phase is not 180 for either response. In

the middle of the tuning range the phase aligns and the reflection is 3. The phase across the tuning range and the magnitude of the reflection coefficient was comprised to increase the tuning range of the VCO. The output matching requires more optimization. When the layout passed the rule checking the next iteration of optimization was halted. The thought being these are rules of thumb and the non-linear response of the oscillator will compensate the phase.

Using the oscillator probe in MWO, a harmonic balance simulation was run. The predicted spectrum and phase noise is shown in Figure 10 and Figure 11.

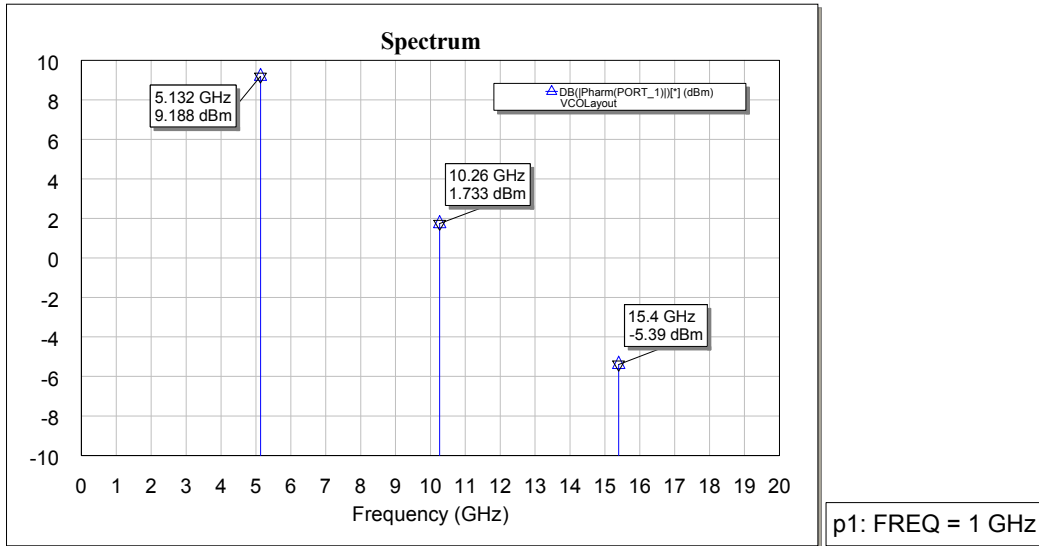
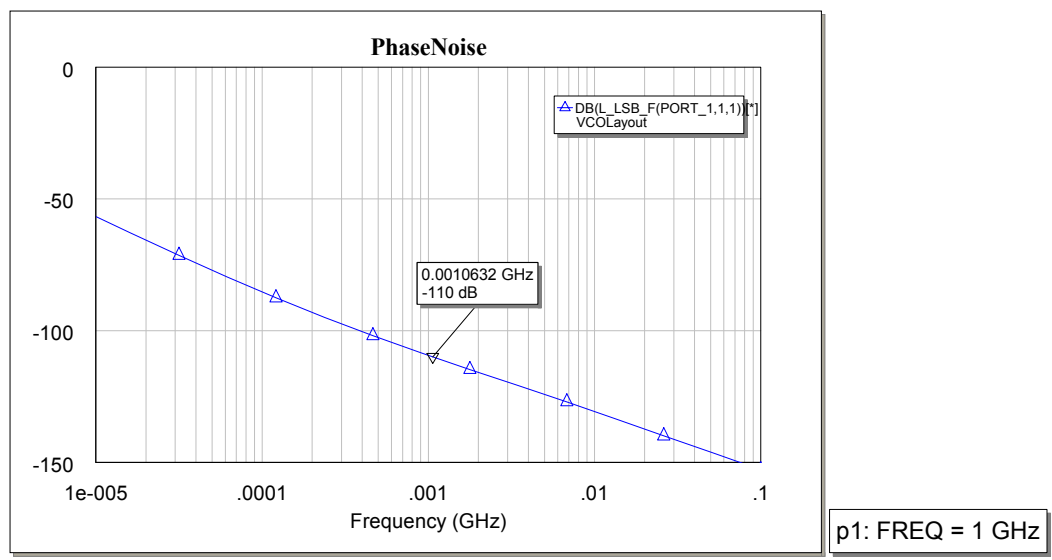


Figure 11

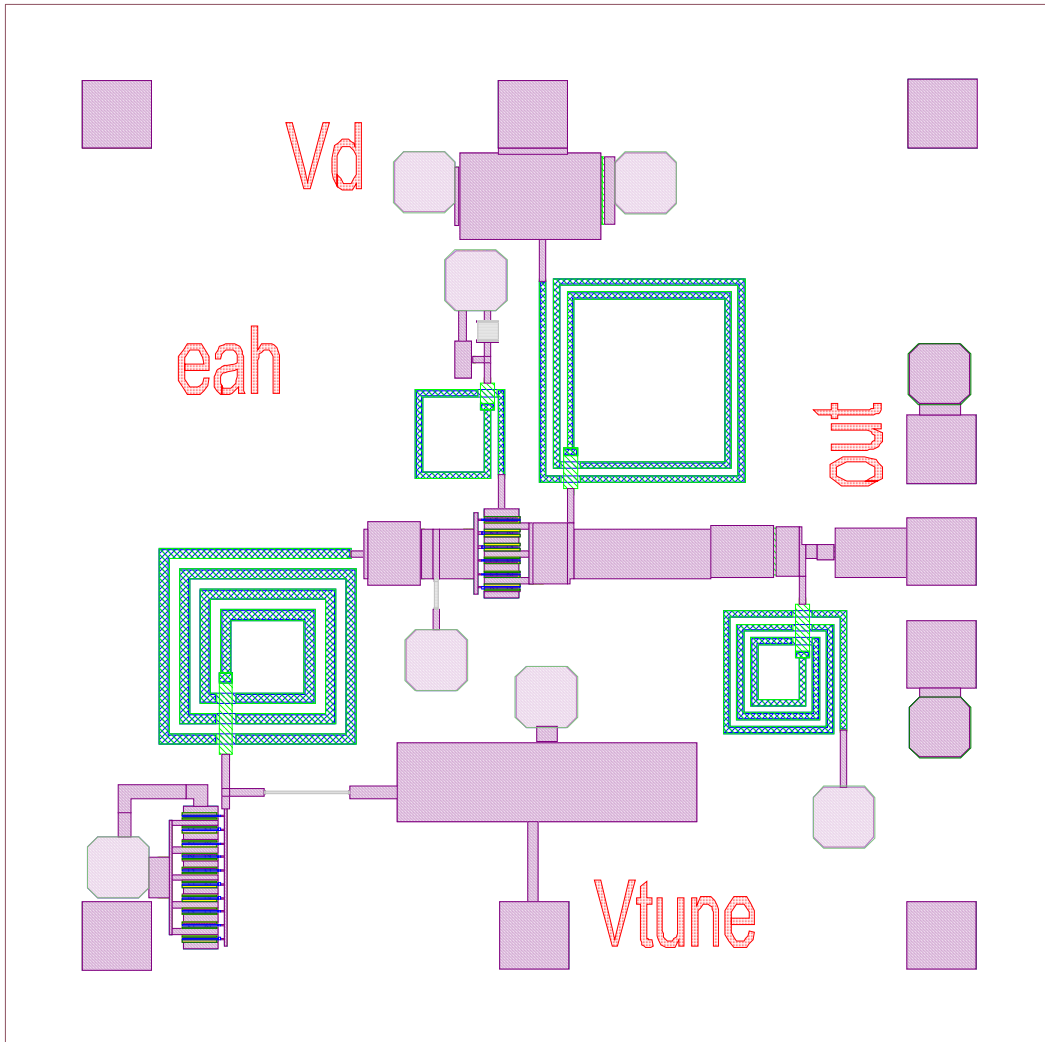


**Figure 11. Predicted phase noise of the VCO using the MWO oscillator port, vtune=0.25 volts.**

The non-linear simulation indicates the VCO will be low in frequency (4.9 to 5.3 GHz). The non-linear simulation oscillation frequency depends on the probe placement and the initial start and stop values. Measurements will indicate the truth.

### 3. VCO Layout

The layout is shown below.



#### 4. Test Plan

Place the circuit in the probe station. Apply the bias voltage of 3 volts to the terminal labeled Vd. Verify the circuit is drawing ~15 mA. Apply a second DC probe to the terminal labeled Vt. This port should control the oscillation frequency. Apply a third RF probe to the labeled RFout. This port should be connected to a spectrum analyzer similar to the HP 5668E. With the spectrum analyzer on full span verify the oscillation is present. If present swing the tune voltage between 0 and 1 volt and verify the oscillation movement is continuous. Fill out the table below.

Vtune	fo (GHz)	Power @ fo (dBm)	2xfo (dBc)	@ 100 kHz (dBc/HZ)	@1M (dBc/HZ)
1.0					
0.8					
0.6					
0.4					
0.3					
0.2					
0.1					
0.0					



## 5. Conclusion

An MMIC VCO was designed using the Tri-Quint TQPED process. Microwave office was the tool used to simulate and layout out the circuit. The reflection method (negative impedance) method as used to design VCO. The VCO is expected oscillate. According non-linear simulation the oscillation will be low and have a reduced tuning range. Linear simulation also indicates a sluggish VCO response due to excessive loading in the output circuit. The output loading was not reduced in an effort to increase the VCO tuning range. Another iteration of output matching could possibly improve the oscillator performance.

According to the linear simulation the oscillator should oscillate from 5.0 GHz to 5.8 GHz. Using the linear simulation and the load line the output power should be  $\sim +7$  dBm. The expected results from the non-linear simulation are summarized

Vtune	Fo	dBm	dBc/Hz
1.0	4.908	4.9	-112
0.8	4.952	4.9	-112
0.6	4.971	8.4	-112
0.4	5.063	8.9	-111
0.3	5.123	9.2	-110
0.2	5.161	9.2	-109
0.1	5.22	9.5	-109
0	5.284	9.6	-109