

# Fall 2006 JHU EE787 MMIC Design Student Projects

Supported by TriQuint, and Agilent Eesof

Professors John Penn and Dr. Michel Reece

Low Noise Amplifier 1 (Low Power)–N. Hughes & L. Macejka

Phase Shifter – Dave Wendland

Power Amplifier 2 – Ben Myers & Niral Patel

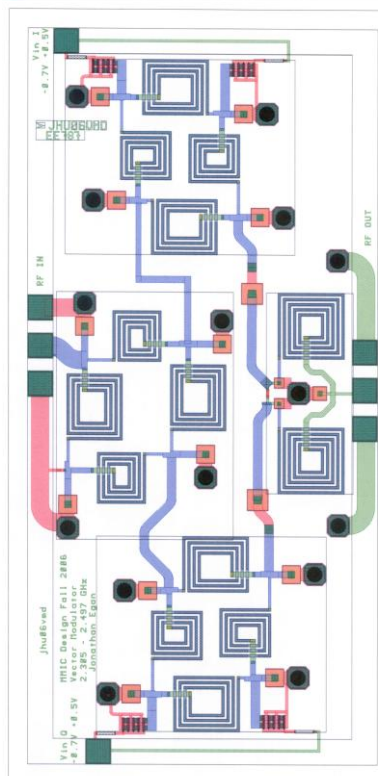
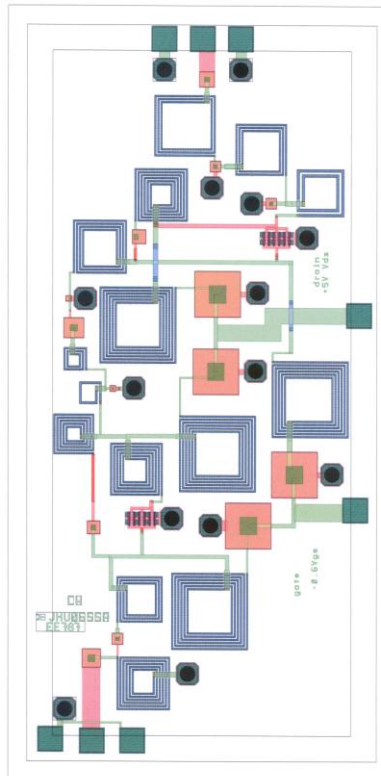
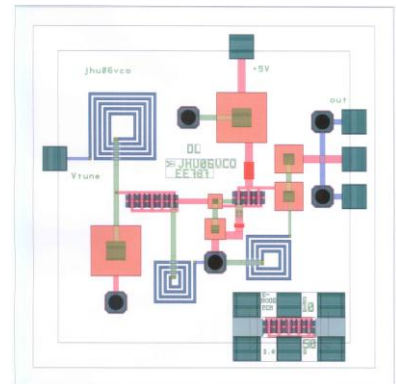
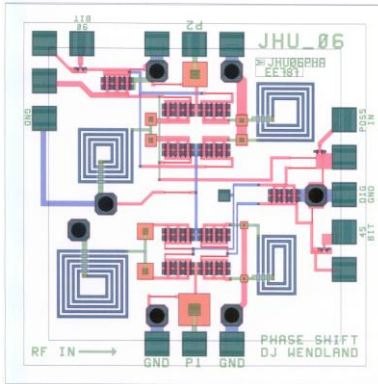
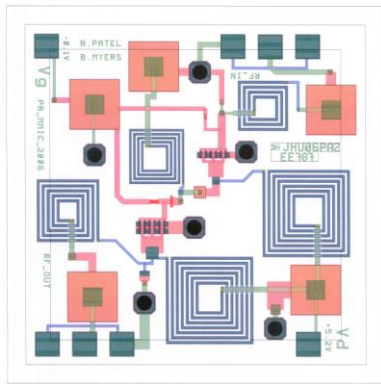
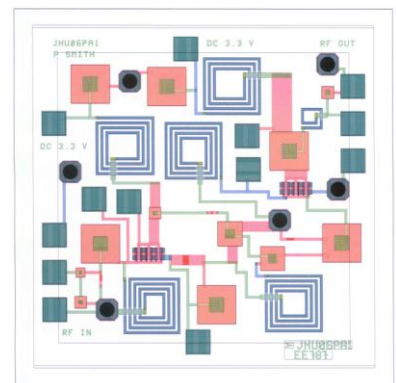
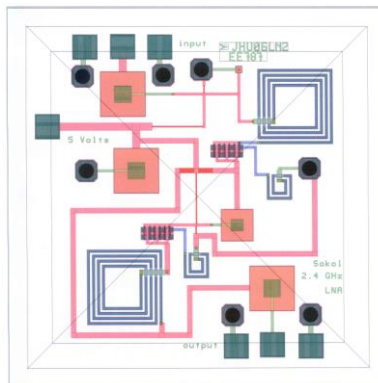
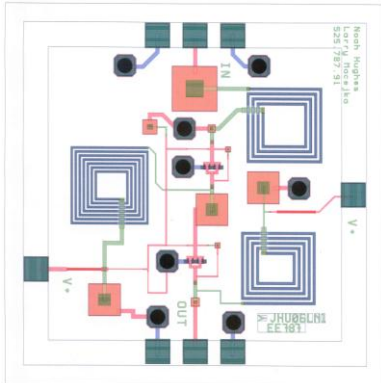
Voltage Controlled Osc. – Dimitrios Loizos

Low Noise Amplifier 2– Dave Sokol

Small Signal Amp – C. Wedderburn

Power Amplifier 1 – Peter Smith

Vector Modulator – Jonathan Egan



# **S-Band Low Power Low Noise Amplifier**

**By: Noah Hughes  
Larry Macejka**

**Microwave Monolithic Integrated Circuit (MMIC)  
Design Class**

**Johns Hopkins University  
Fall 2006**

## TABLE OF CONTENTS

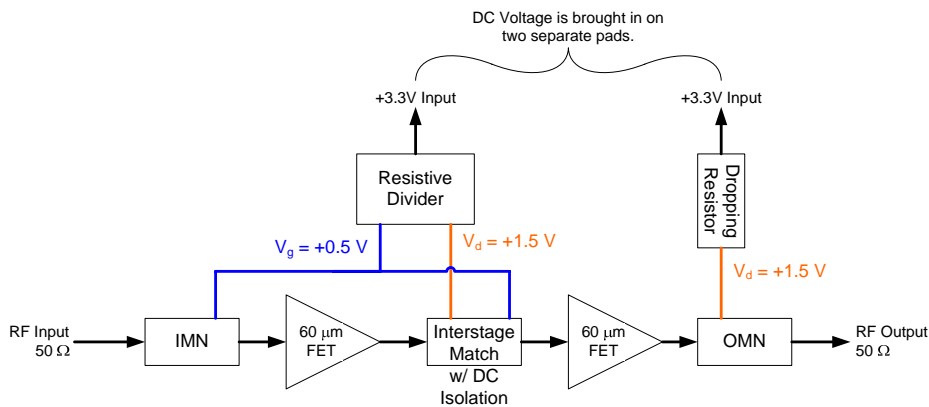
<b>Abstract</b> .....	3
<b>Introduction</b> .....	3
<b>Design</b> .....	4
<b>Requirements&amp; Trade-Offs</b> .....	5
<b>Schematic</b> .....	7
<b>Linear Simulations</b> .....	8
S_Parameters.....	8
Noise Figure.....	8
Stability.....	9
DC Annotation.....	11
<b>Non-Linear Simulation:</b> .....	12
Power Output .....	12
<b>Layout</b> .....	13
<b>Test Plan</b> .....	13
Test Procedures.....	14
<i>S-parameter Measurement</i> .....	14
<i>Noise Figure Measurement</i> .....	14
<i>Compression Point Measurement</i> .....	14
<b>Conclusion</b> .....	14

## Abstract

The design of a MMIC low power low noise amplifier (LNA) circuit will be described in this paper. The amplifier design is based on the requirements of an S-band duplex transceiver and designed to operate with very low power. The LNA operates with a DC power consumption of approximately 17mW drawing 5.14mA at 3.3 V. The amplifier has a 1dB bandwidth of ~500MHz around the required 2305 to 2497 MHz operating range. The noise figure of the LNA is less than the design requirement of 3dB and the gain reaches 27dB under the operating bandwidth. In addition the output port match exceeds  $-15\text{dB}$  and the input port match is better than  $-10\text{dB}$ . The stability of the amplifier is unconditionally stable between 0.5 and 5 GHz. This design is placed in the 60 X 60 mil Anachip layout as required the Triquint for fabrication.

## Introduction

This report will focus on the design, simulation, layout, optimization and test plan for the low power low noise amplifier. The LNA is at the front end of the S-band receiver providing the first stage of amplification after the antenna and adding as little noise as possible, shown in Figure 2. The design consists of a two-stage amplifier design powered by two positive 3.3V sources, shown in Figure 1. Two 4 X 15um (60um) EMODE FETs are used in the amplifier due to their higher gain and lower noise figure. The output and intermediate matching networks are used to ensure a proper match and maximum gain, while the input-matching network sets the noise figure for the amplifier. Finally a feedback network is used on each of the amplifier stages to broaden the gain, stabilize the amplifier and reduce power consumption.



Block Diagram of Low Power LNA MMIC Design

Figure 1: Two Stage Low Power LNA

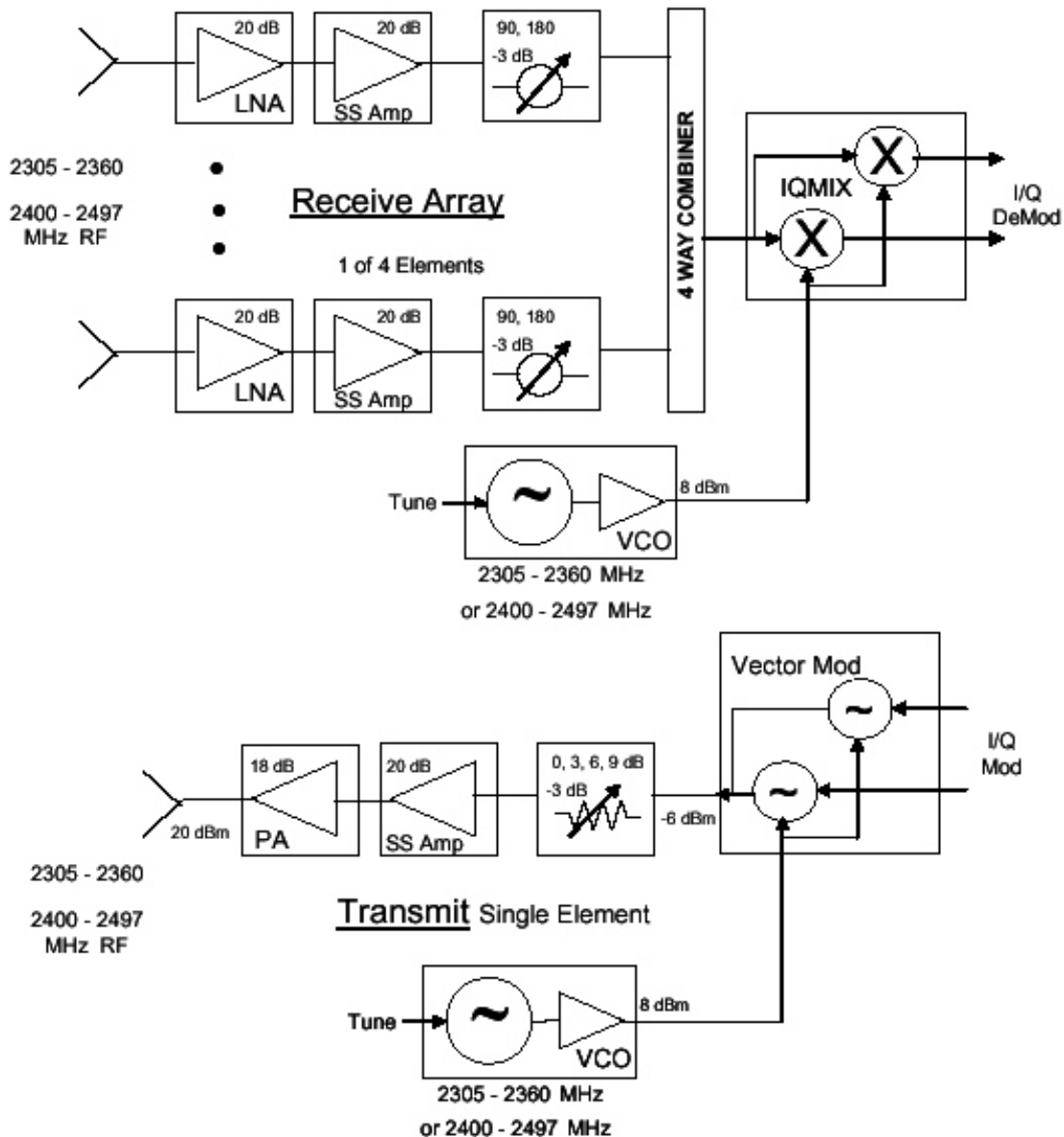


Figure 2: Duplex Transceiver System

## Design

Originally the LNA design was focused on reducing the power consumption of the amplifier to a level where it could be powered by a battery. To achieve this both stages of the amplifier were stabilized using a resistor and capacitor to provide a feedback path between the drain and gate. Initially there was concern the feedback path on the first stage of the amplifier would increase the noise figure above the

requirement, but we later found this to be not the case. With the two FET's stabilized two identical single stage LNAs were designed using ideal components. The input matching circuit of amplifier was tuned to produce the best noise figure possible, while the output matching circuit was tuned to the best VSWR. As an initial cut at the design the two stages were cascaded together. The results of this initial simulation were favorable resulting in a noise figure of ~1.8dB and a gain of ~30dB across the design band, which removed our concern of the feedback network. At that point the number and size of components in the matching networks was taken into account especially the intermediate matching network, which consisted of 2 inductors and 2 capacitors. Both the intermediate and output matching networks were retuned to a shunt inductor and series capacitor topology. This provided an effective RF disconnect between the power input and the RF trace and reduced the number of components to two apiece.

After the ideal design produced favorable simulation results, the ideal components were replaced with Triquint components and simulated again. Initially the circuit had to be retuned due to differences between the Triquint and ideal models. The extra resistance in the Triquint models also increased the noise figure slightly to ~2dB and reduced the gain to ~27dB, but still remained well within design margin. At this point a flaw in the design was discovered. The two drain power supplies could not be combined together on the chip without causing the amplifier to become unstable. To alleviate this problem a resistive divider was installed on one of the drain sources allowing it to provide both gate voltages as well as one of the drain supplies. This allowed the amplifier chip to only require two 3.3V power supply lines from the same power supply.

With this problem out of the way, the iterative layout and interconnect simulation process began. The two stage LNA was initially layed out with just the components. The amplifier's interconnect was added in later according to the orientation and placement of the components. Special consideration was taken to ensure the trace width of the amplifier's interconnect did not violate any current carrying restrictions, given that most of the circuit was routed on Metal 0. Once a reasonable layout was created, the microstrip interconnect was placed in a simulation along with the rest of the amplifier. This resulted in multiple iterations of tuning the circuit in the simulation and then changing the layout accordingly. In the end, a favorable compromise was achieved that resulted in an error free layout and a simulation that passed all of the design requirements.

### Requirements & Trade-Offs

<i>Parameter</i>	Requirement		<b>Expected Performance</b>
	<b>Desired</b>	<b>Goal</b>	
<i>Frequency</i>	2305 – 2497MHz		2305 - 2497
<b>Bandwidth</b>	800MHz		800 MHz
<b>Gain</b>	>20dB		27.5 dB

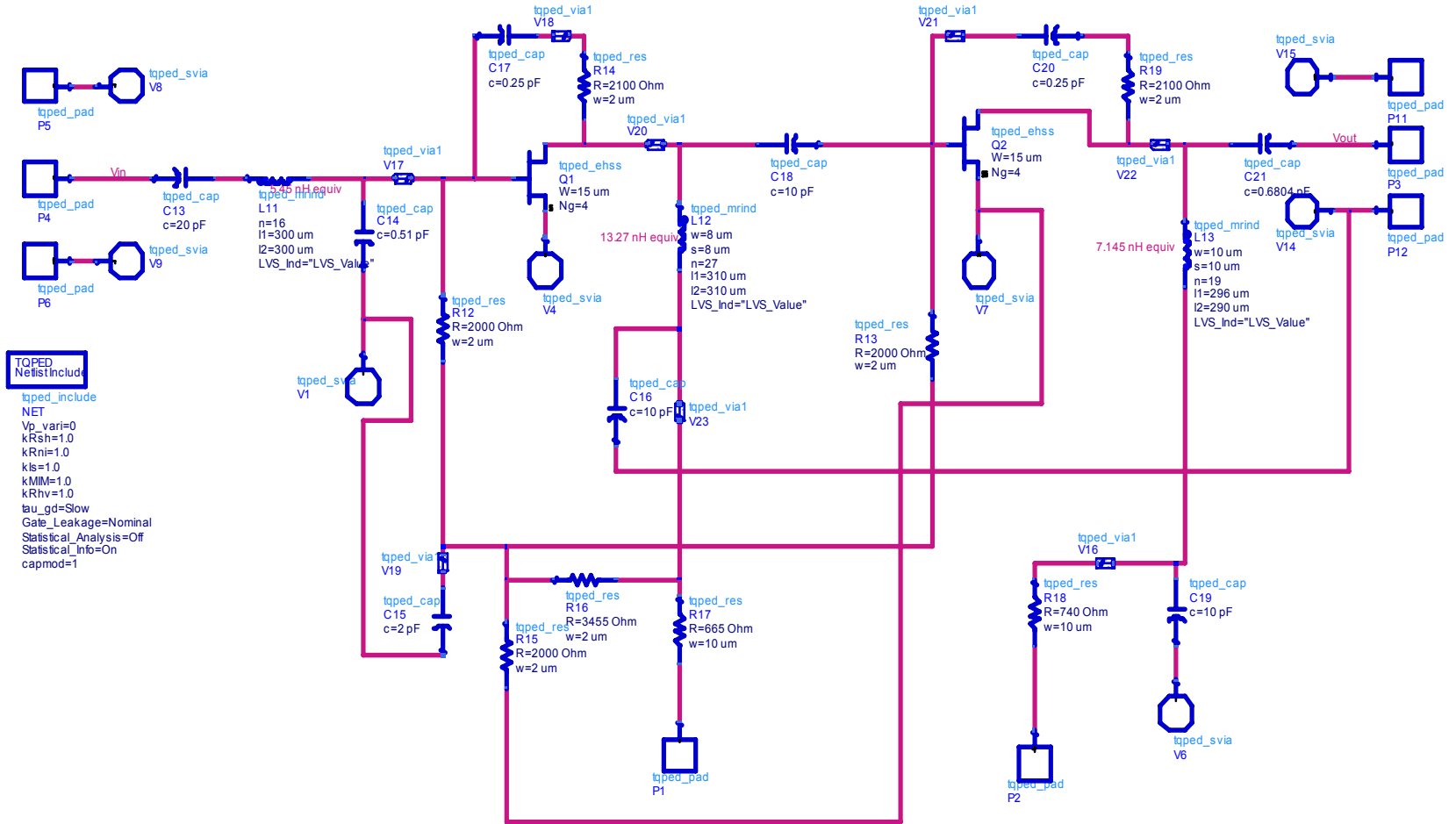
<b>Noise Figure</b>	< 4dB	3dB	2.258 dB
<b>Gain Ripple</b>	+/- 1dB		+/- 1dB
<b>Input/Output VSWR</b>	1.5:1		Input VSWR: 1.78:1
			Output VSWR: 1.01:1
<b>Voltage Supply</b>	3.3V		3.3V
<b>Power Dissipation</b>	10mW per stage		16.96mW two stage Amp
<b>Size/ Packaging</b>	60 X 60 mil Chip		60 X 60 mil Chip

### Trade Offs/ Optimization

Many trade offs in the design were required even in the early stages. While stabilizing the FET in the design, we had many choices including using series or shunt resistors as well as an inductor between the FET source and ground. Unfortunately all of these forced us to drop voltage across resistors and thus increase the power consumption of the amplifier drastically. In order to avoid this, a feedback structure was used using a resistor and capacitor in series between the gate and drain of the FET. The downside of the feedback stability method was the additional noise that would be “fed back” to the input of the LNA. Fortunately after finishing the design, the noise figure increased only slightly and was well below the 3dB requirement.

The other major trade off dealt with the bias structure in the amplifier. Originally the LNA required 4 separate voltage supply inputs of +0.5V and +1.5V (2 each). The design became unstable if the voltage inputs were connected together on chip. To overcome this design flaw, resistive dividers were added to the input of the voltage supply to serve a dual purpose. First the resistive dividers reduce the 3.3V input supply to the required 1.5V for the drain bias and second it taps off the 1.5V and reduces it to the required 0.5V gate bias. Using this method the number of supply voltages required was reduced to two inputs of +3.3V. The remaining two voltage supplies could have been combined on chip via a resistor, but after performing a preliminary layout the two voltage supplies were on opposite sides. This prohibited the combination of the last two voltage supplies on chip.

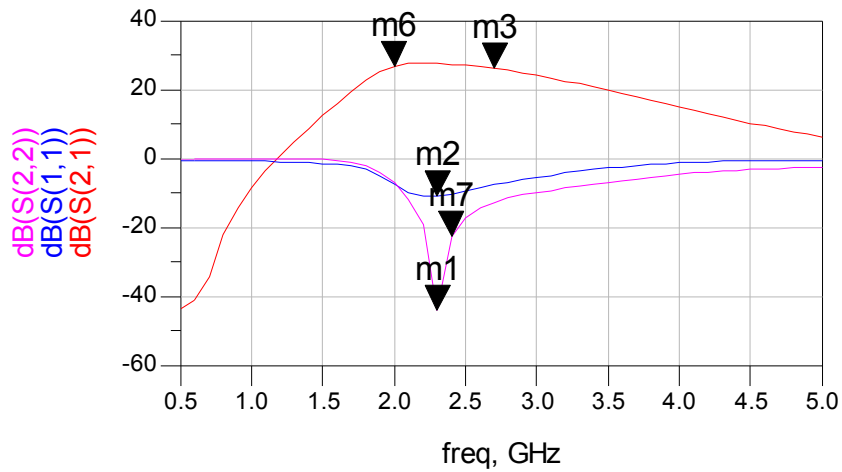
# Schematic



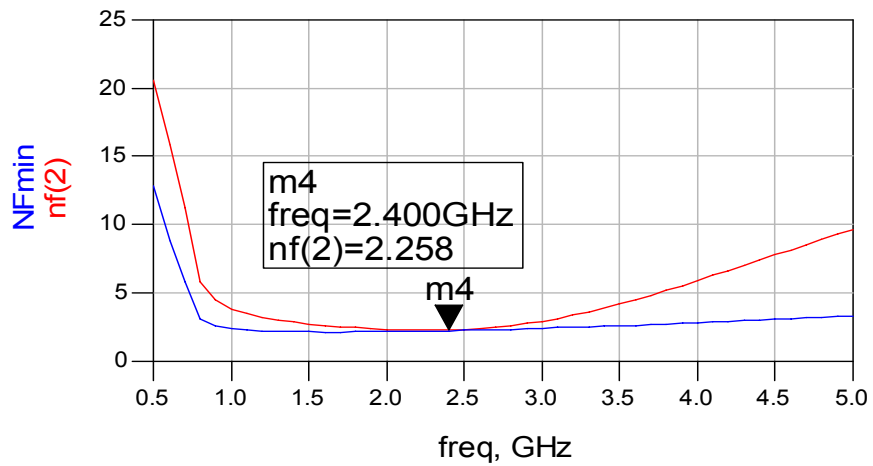


## Linear Simulations S\_Parameters

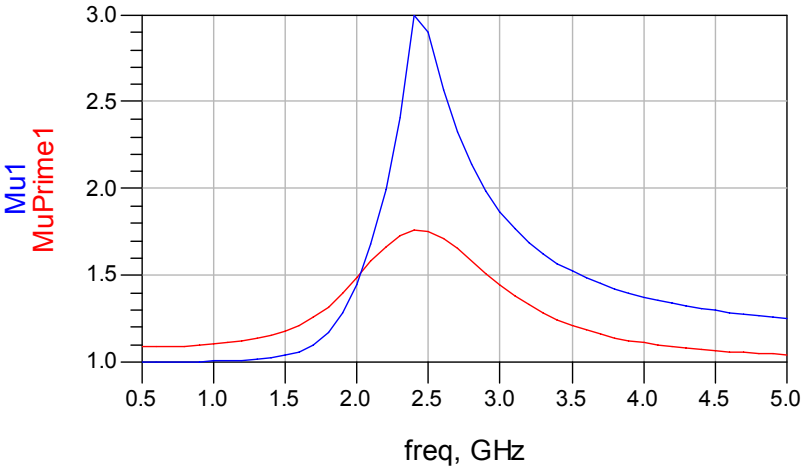
m7 freq=2.400GHz dB(S(2,2))=-22.626	m3 freq=2.700GHz dB(S(2,1))=25.988	
m6 freq=2.000GHz dB(S(2,1))=26.740	m2 freq=2.300GHz dB(S(1,1))=-10.985	m1 freq=2.300GHz dB(S(2,2))=-44.148



## Noise Figure

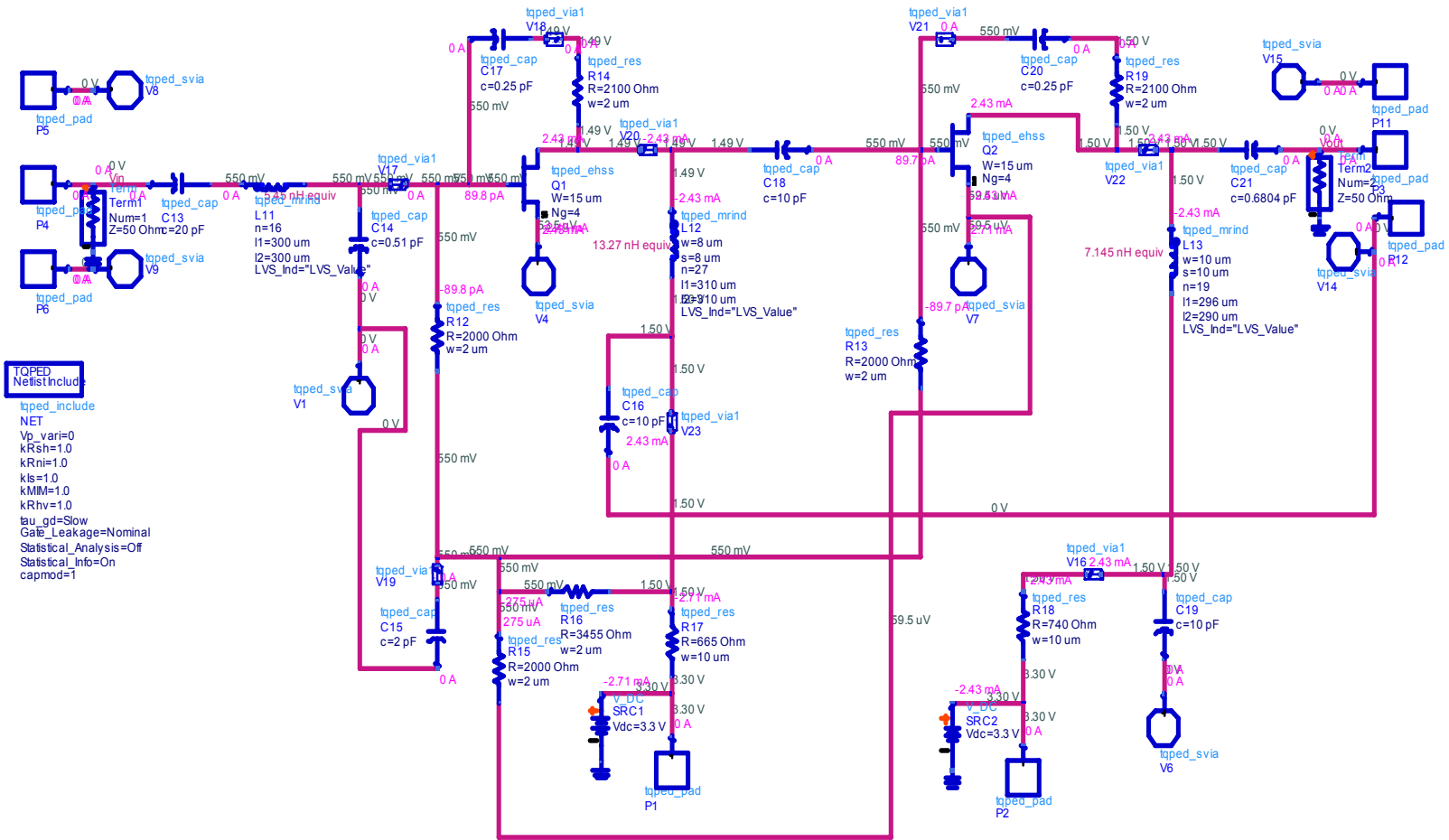


**Stability**

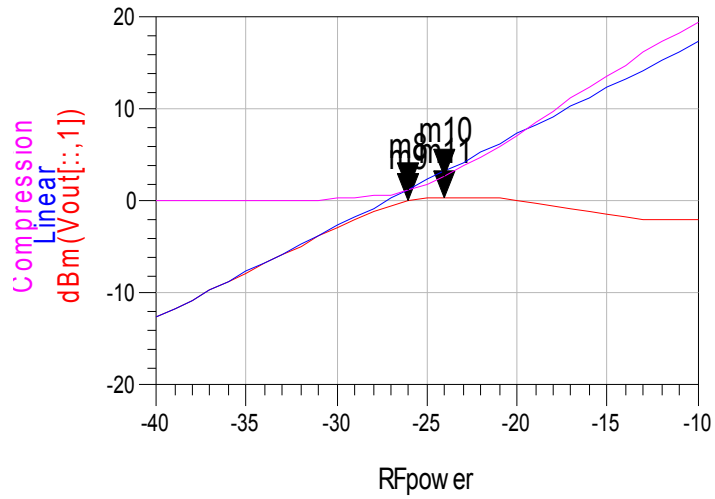




# DC Annotation



**Non-Linear Simulation:  
Power Output**



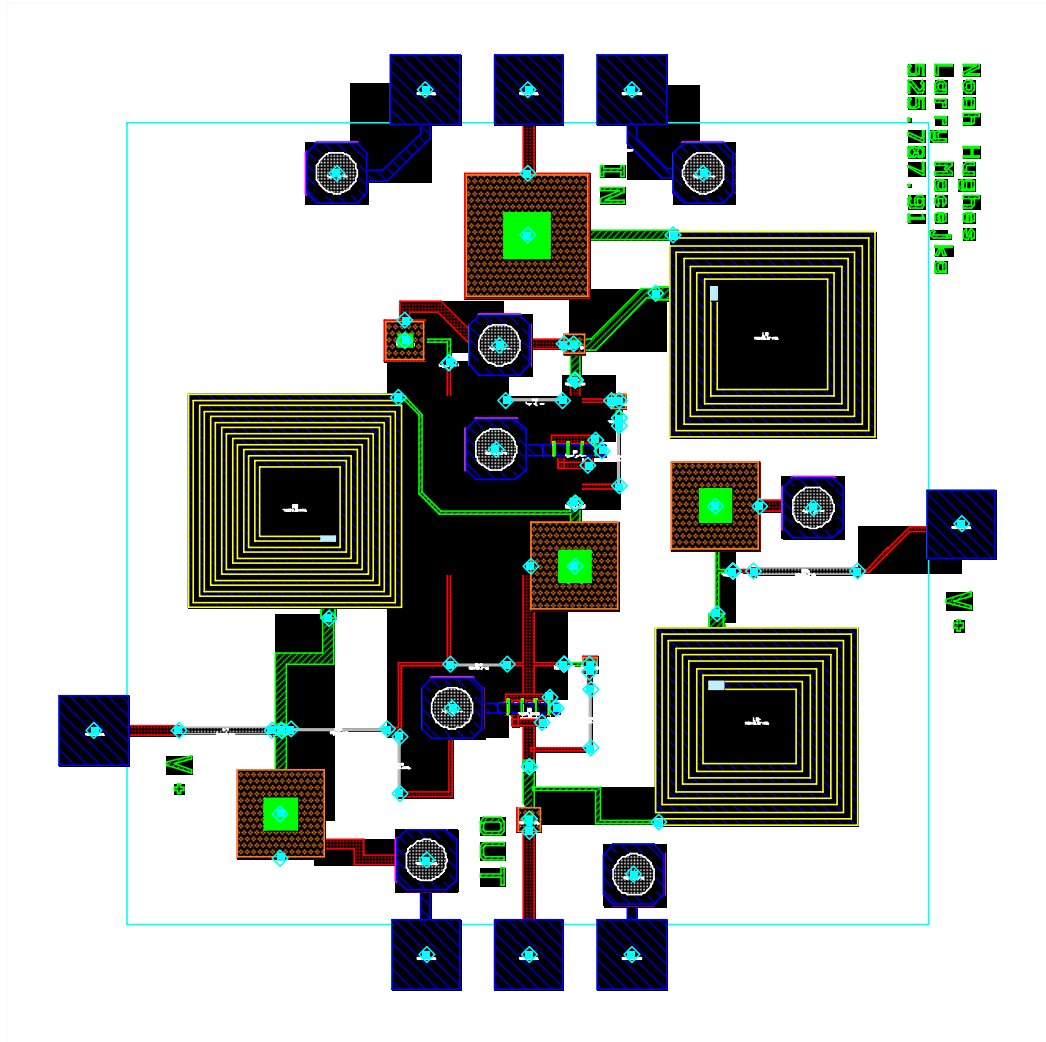
m10  
RFpower=-24.000  
Compression=2.816

m8  
RFpower=-26.000  
Compression=1.253

m9  
indep(m9)=-26.000  
plot\_vs(dBm(Vout[:,1]), RFpower)=0.064

m11  
indep(m11)=-24.000  
plot\_vs(dBm(Vout[:,1]), RFpower)=0.500

## Layout



### Test Plan

The following test equipment is necessary to test the full extent of this Low Power LNA Design:

- 3.3V Power Supply with Needle Probe

- Network Analyzer

- Cables and Ground Signal Ground (GSG) Probes

- Calibration Substrate for MMIC Testing

- Noise Figure Meter

- RF Signal Generator (capable of generating frequencies in 2-3 GHz range)

- Power Meter or Spectrum Analyzer

## Test Procedures

### *S-parameter Measurement*

- 1.) Calibrate the network analyzer from 1 GHz to 10GHz.
- 2.) Connect the 3.3V needle probe to the DC pads on the MMIC labeled “V+”.  
The order in which they are connected is not important.
- 3.) Slowly increase the voltage to 3.3V to determine that the amplifier is working correctly.
- 4.) Verify that the total current draw on the power supply is around 5.13 mA.
- 5.) Connect the input GSG Probes on the “IN” pads on the chip.
- 6.) Connect the output GSG Probes on the “OUT” pads on the chip.
- 7.) Measure the S-Parameter data measurements and save them to a disk.

### *Noise Figure Measurement*

Using the configuration of the MMIC mentioned in the S-parameter measurement, proceed to do the following:

- 1.) Remove the SMA cable from the port labeled “OUT” on the GSG Probe.
- 2.) Connect the Noise Figure Meter to the SMA port on the GSG Probe.
- 3.) Remove the SMA cable from the port labeled “IN” on the GSG Probe.
- 4.) Connect the noise source to the GSG Probe on the “IN” side of the MMIC.
- 5.) Use the Noise Figure Meter to take a measurement.

### *Compression Point Measurement*

Using the configuration of the MMIC mentioned in the Noise Figure Measurement, proceed to do the following:

- 1.) Remove the SMA cable from the port labeled “OUT” on the GSG Probe.
- 2.) Connect the Power Meter to the SMA port on the GSG Probe.
- 3.) Remove the SMA cable from the port labeled “IN” on the GSG Probe.
- 4.) Connect a signal generator to the GSG Probe on the “IN” side of the MMIC making sure that the RF output of the device is off or around  $-80$  dBm.
- 5.) Set the signal generator to 2.4 GHz.
- 6.) Beginning at  $-40$  dBm, sweep the power input at 1 dB steps. Measure the power output at each interval.
- 7.) Whenever the output does not increase by 1 dB with respect to the input power, you have reached the 1 dB compression point. Determining what exact value this compression point occurs at can be either done using interpolation or Microsoft Excel.

## Conclusion

Testing the low power LNA should have at least 20dB gain. The gain flatness should be less than 1 dB over a band of 500 MHz measured from the center frequency (2305 to 2497 MHz). Also, the Input match should have around  $-10.9$ dB of loss at 2.4 GHz and the output match should have around  $-44$ dB of loss at 2.3 GHz. The power consumption should be somewhere around 16.96 mW (taking the measured current and multiplying it by the supply voltage).

# Two Bit Phase Shifter

JHU MMIC Project

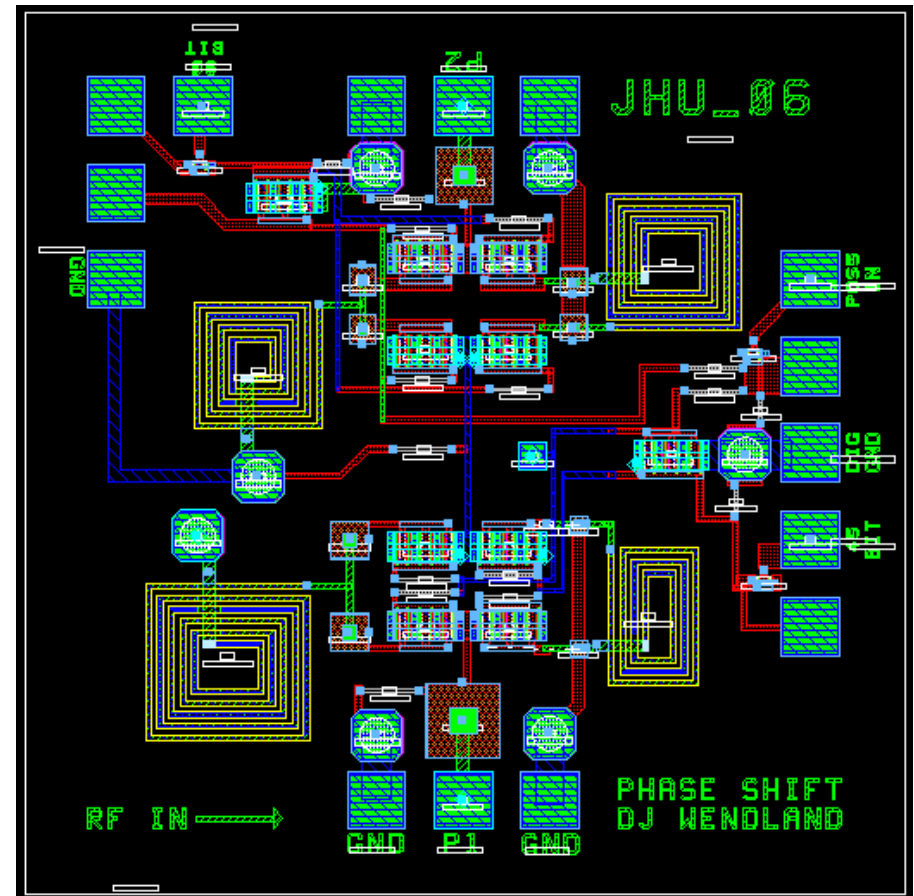
EE525.787 FALL 2006

David J. Wendland



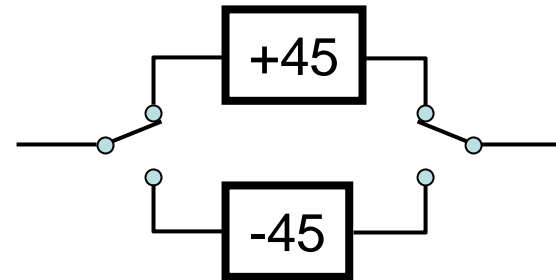
# Introduction

- A MMIC two bit phase shifter was designed, simulated and laid out on a 60 mil x60 mil GaAs substrate.
- The circuit will be fabricated by TriQint.

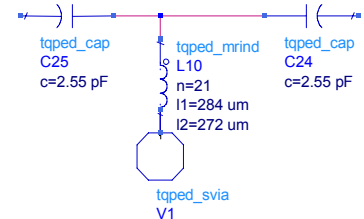


# Design Philosophy

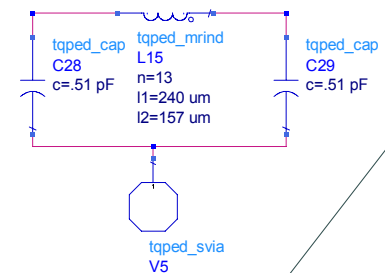
- The topology of the design was set such that there was a relative phase shift through the net work when compared to the zero or through path. The phase shifter consist of three sections.
  - Control
  - 90 degree shift
  - 180 degree shift
- The control section consist of circuitry to convert positive 5 volt control voltage to the appropriate voltages to the phase switches.
- The 90 and 180 degree shift sections are the same except for the amount of phase shift provided by each section.
- Each phase shift section consists of a positive phase network and a negative phase network.
- The through path passes through the positive phase network of each section.
- Lets walk through the 90 degree phase section.
- The 90 degree phase shift section consists of a positive 45 deg. phase shift network and a negative 45 deg. phase shift network. If the through path is set through the positive phase shift network. There will be a 90 degree relative phase when the path switches, from the +45 degree network to the -45 degree network.
- With the above described topology, the phase of the through path is arbitrary and is not important for the relative phase shift.
- The 180 degree phase shift is achieved the same way but using +/-90degree networks



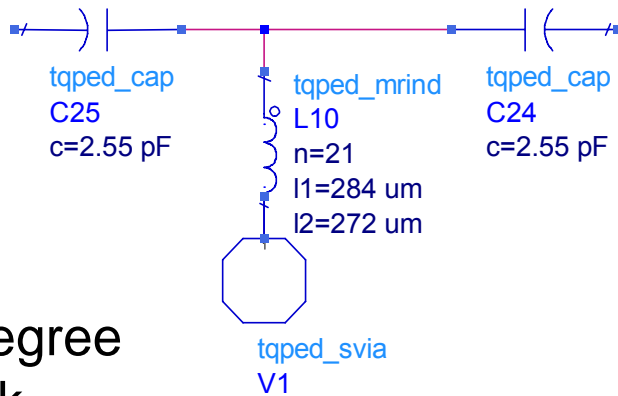
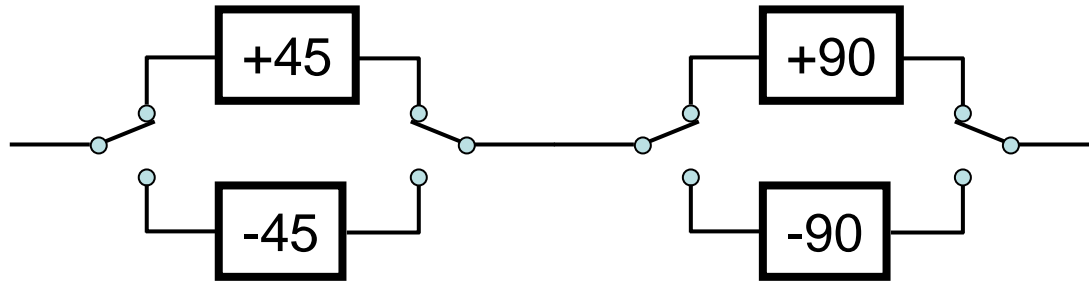
## + 45 Degree Network



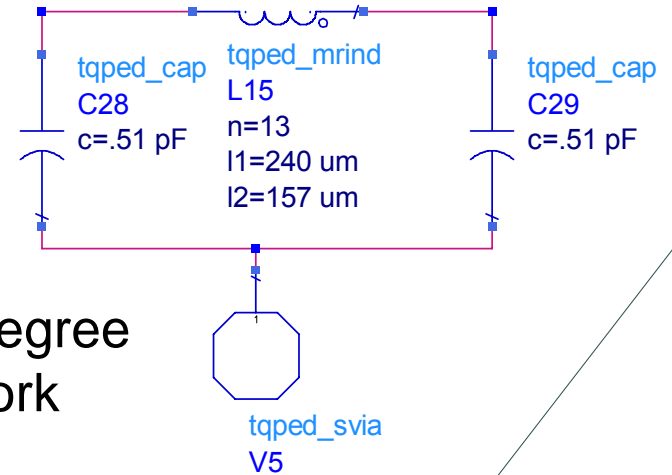
## -45 Degree Network



# Design Philosophy



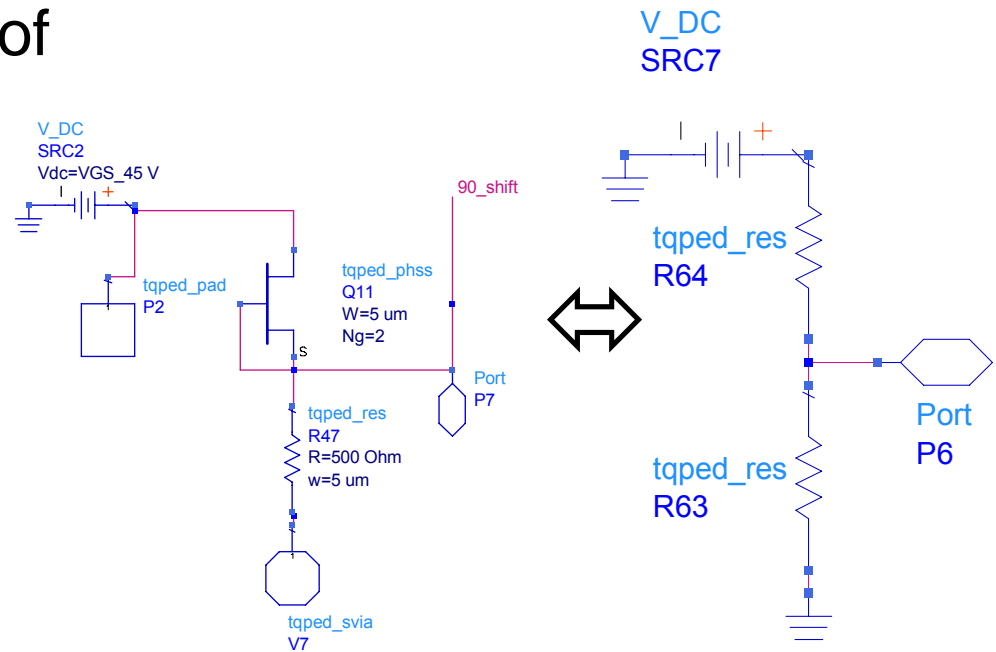
+ 45 Degree Network



-45 Degree Network

# Design Philosophy

- Emode transistor were used to take advantage of the positive gate bias
  - Can use single positive supply
- Dmode transistor were used to convert +5V to the desired gate voltage
  - Smaller than resistors
  - Save space in voltage dividers.
  - FET sized to provide:
    - 2mA for 45/90 bit
    - 4mA for +5V bias



Dmode FET in voltage divider

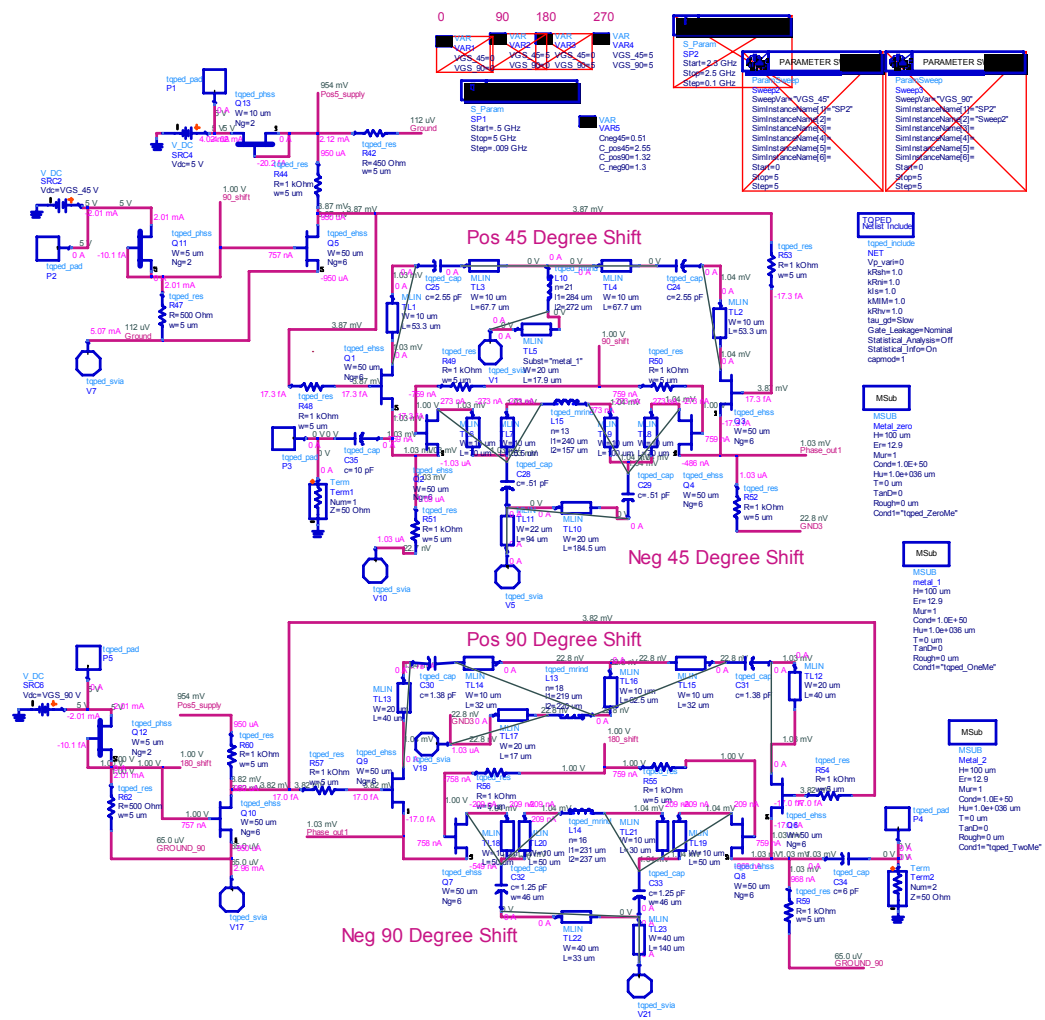
# Logic Table

Phase Shift	Bit 45	Bit 90
0	0	0
90	5	0
180	0	5
270	5	5

# Simulation/Layout

- The phase shifter was first developed with ideal components
- TriQuint components were then substituted and retuned
- The components were then inserted into the layout, positioned and interconnects added
- The interconnects of the critical paths were simulated using microstrip elements in the schematic.
- Critical interconnects consist of:
  - Connections between switches, capacitors and inductors of the phase shift elements.
- Interconnect between the 90 degree phase shift section, 180 degree section and pads were not simulated since those paths do not affect the relative phase shift.

# Two Bit Phase Shifter Schematic with Interconnects



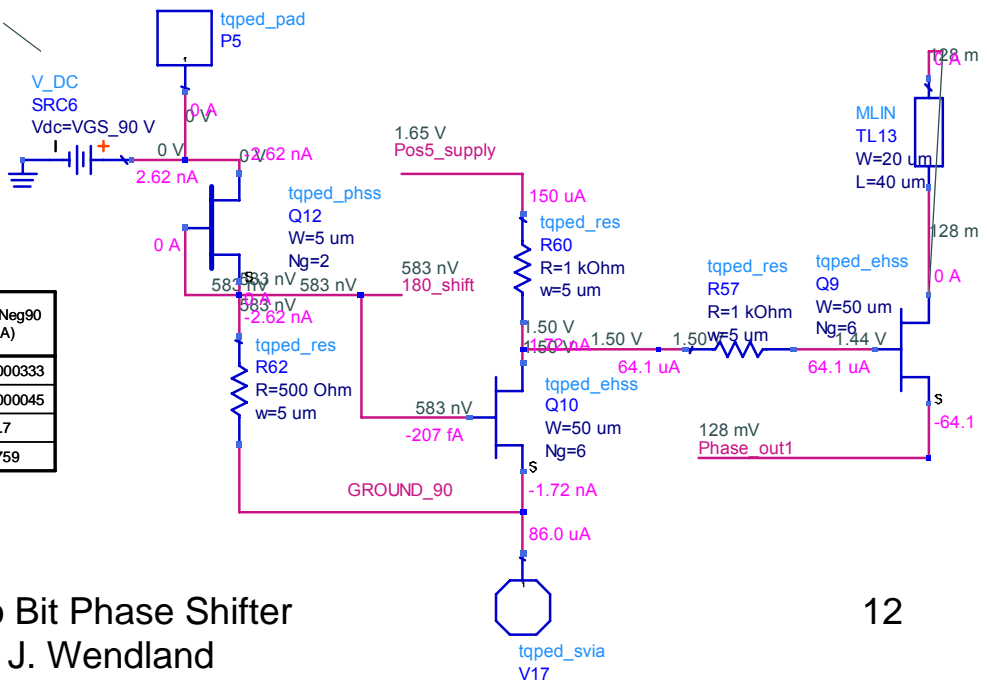
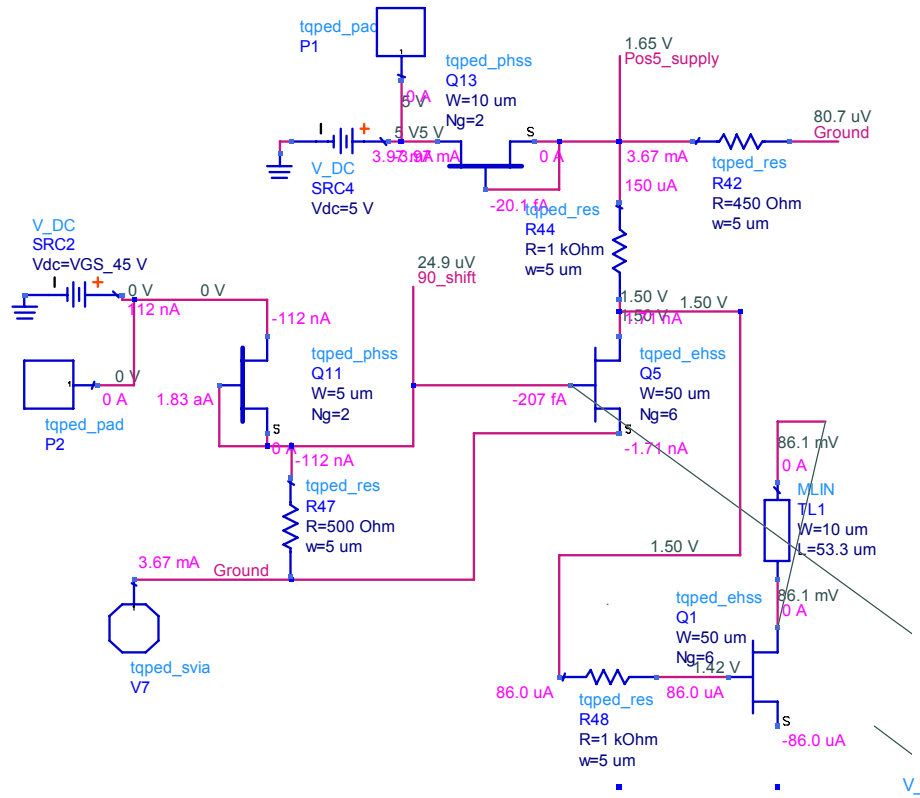






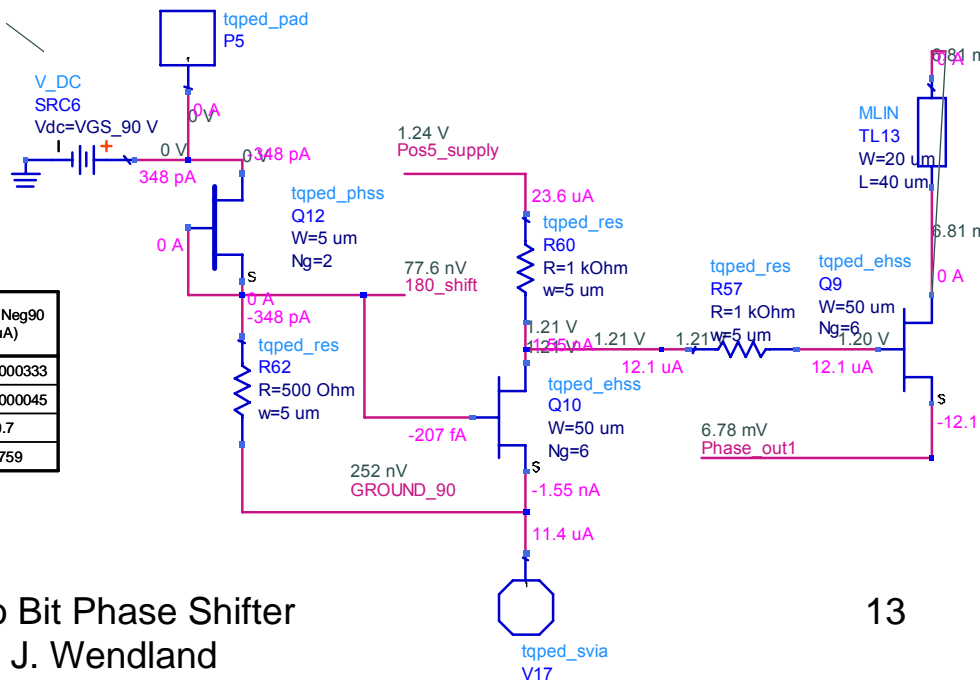
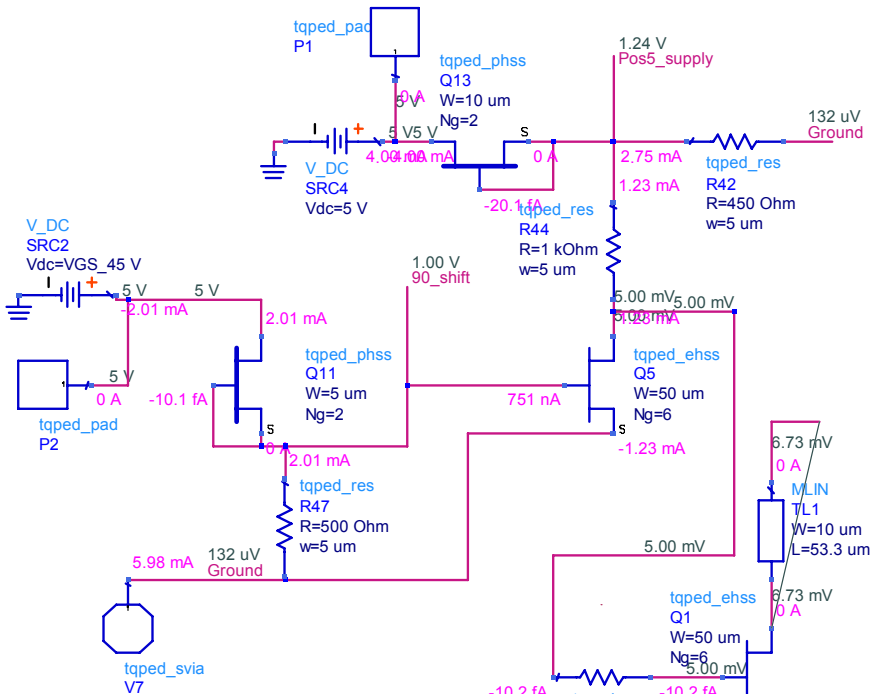


# DC Switch Bias Zero Degrees/Ref



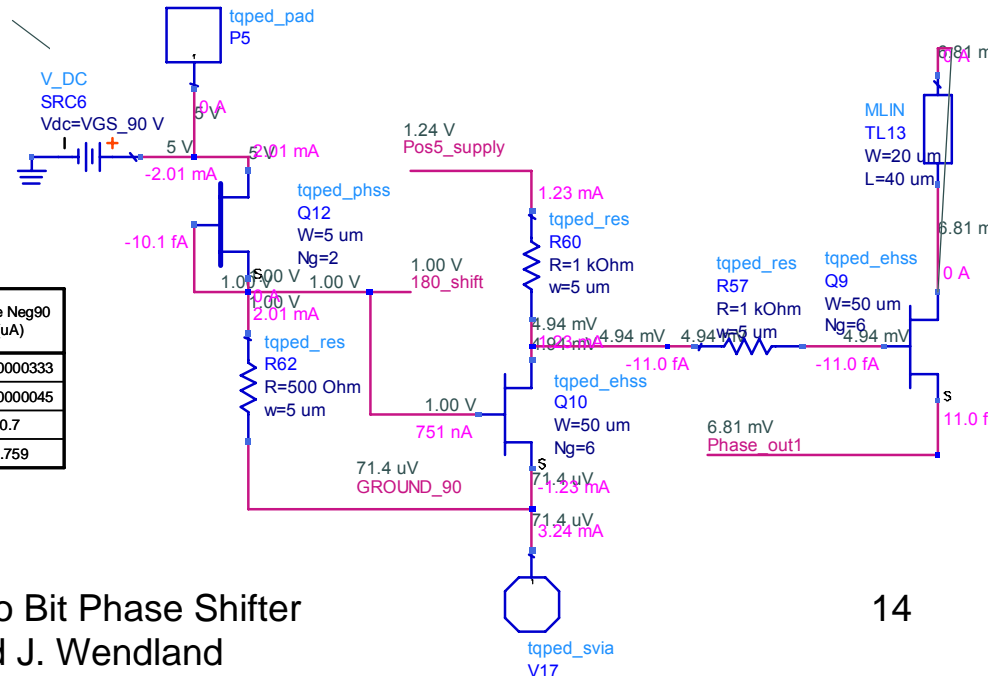
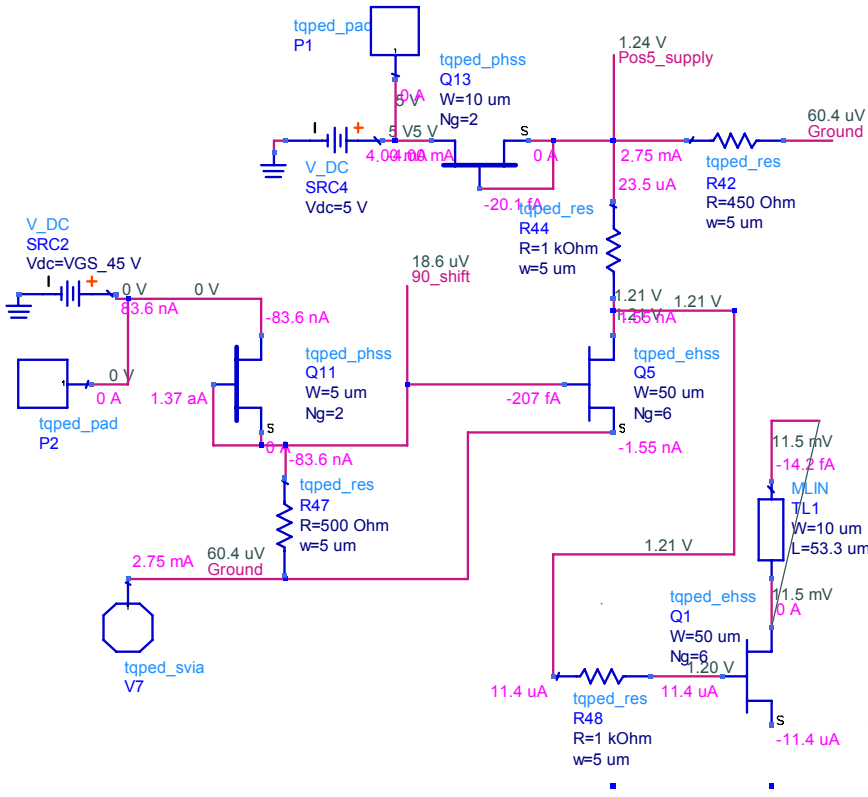
Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90 (V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	0.000000045	0.000000011	0.7	
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

# DC Switch Bias 90 Degrees



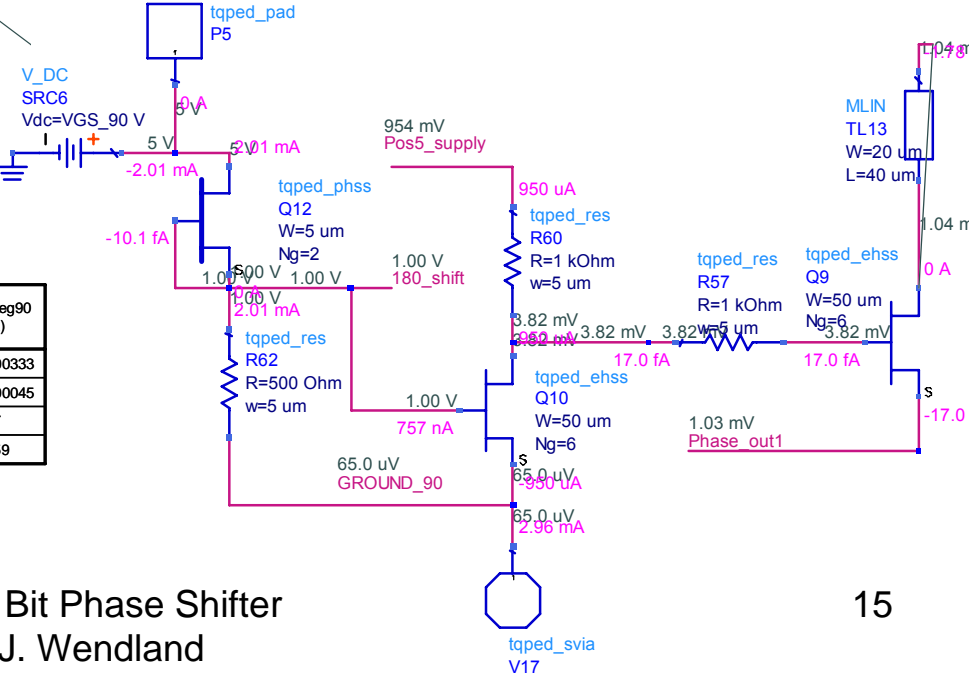
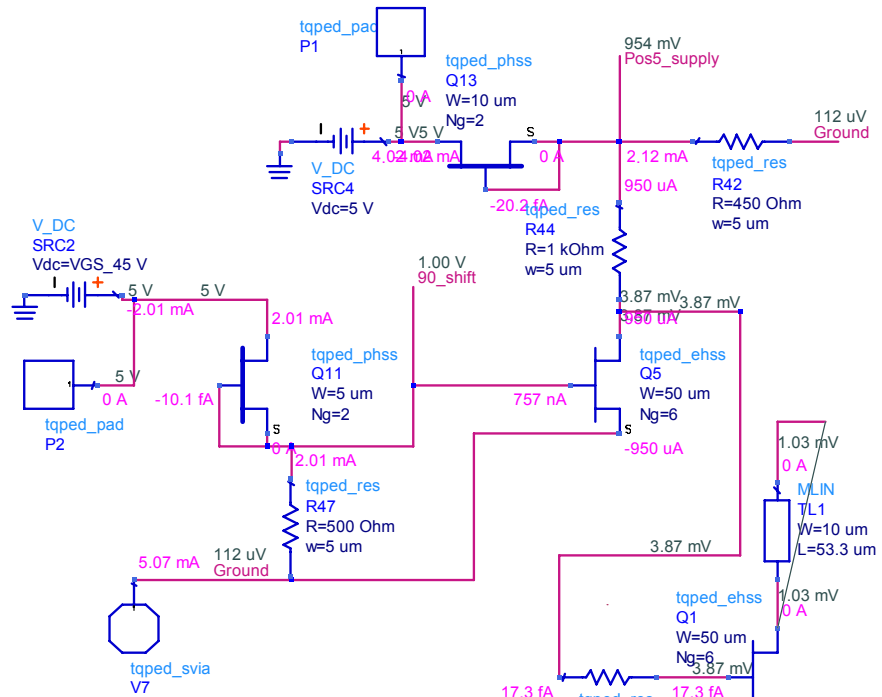
Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90 (V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	11	0.000000045	0.000000011	0.7
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

# DC Switch Bias 180 Degrees



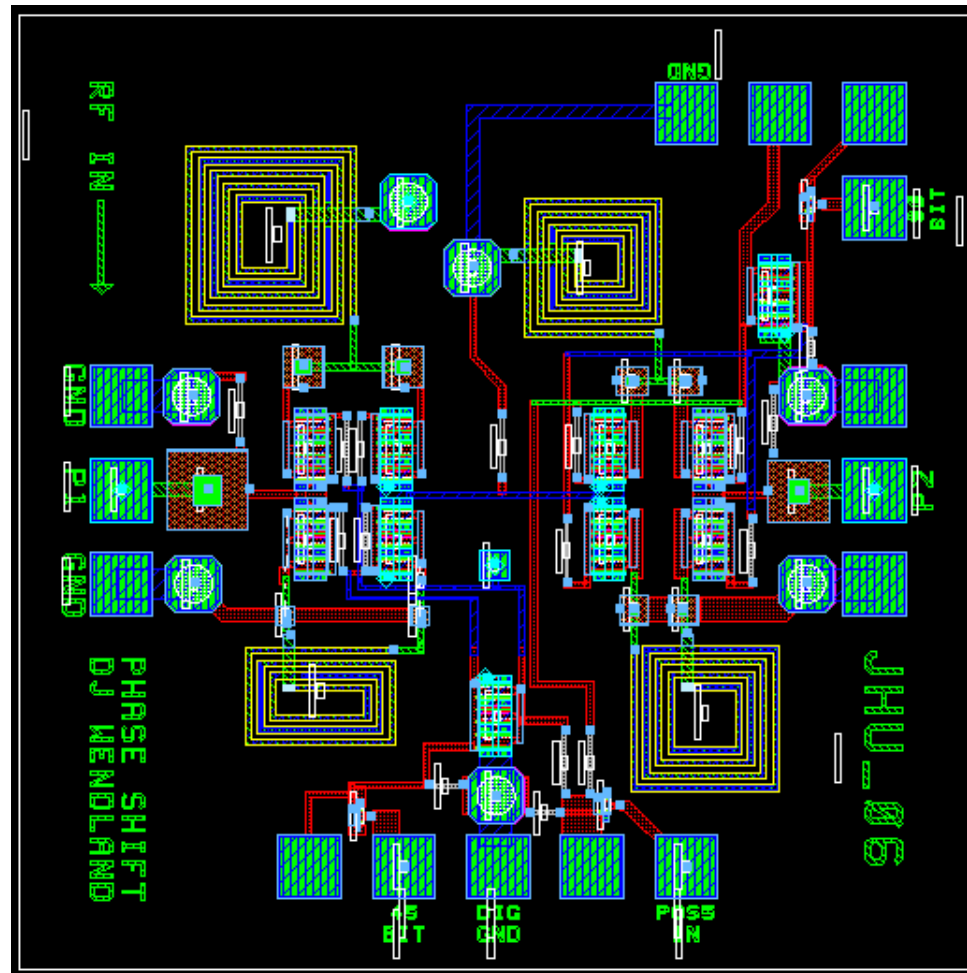
Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90 (V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	11	0.000000045	0.000000011	0.7
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

# DC Switch Bias 270 Degrees



Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90 (V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	11	0.000000045	0.000000011	0.7
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

# Two Bit Phase Shifter Layout on 60mil x 60 mil GaAs Substrate



# Design Specification

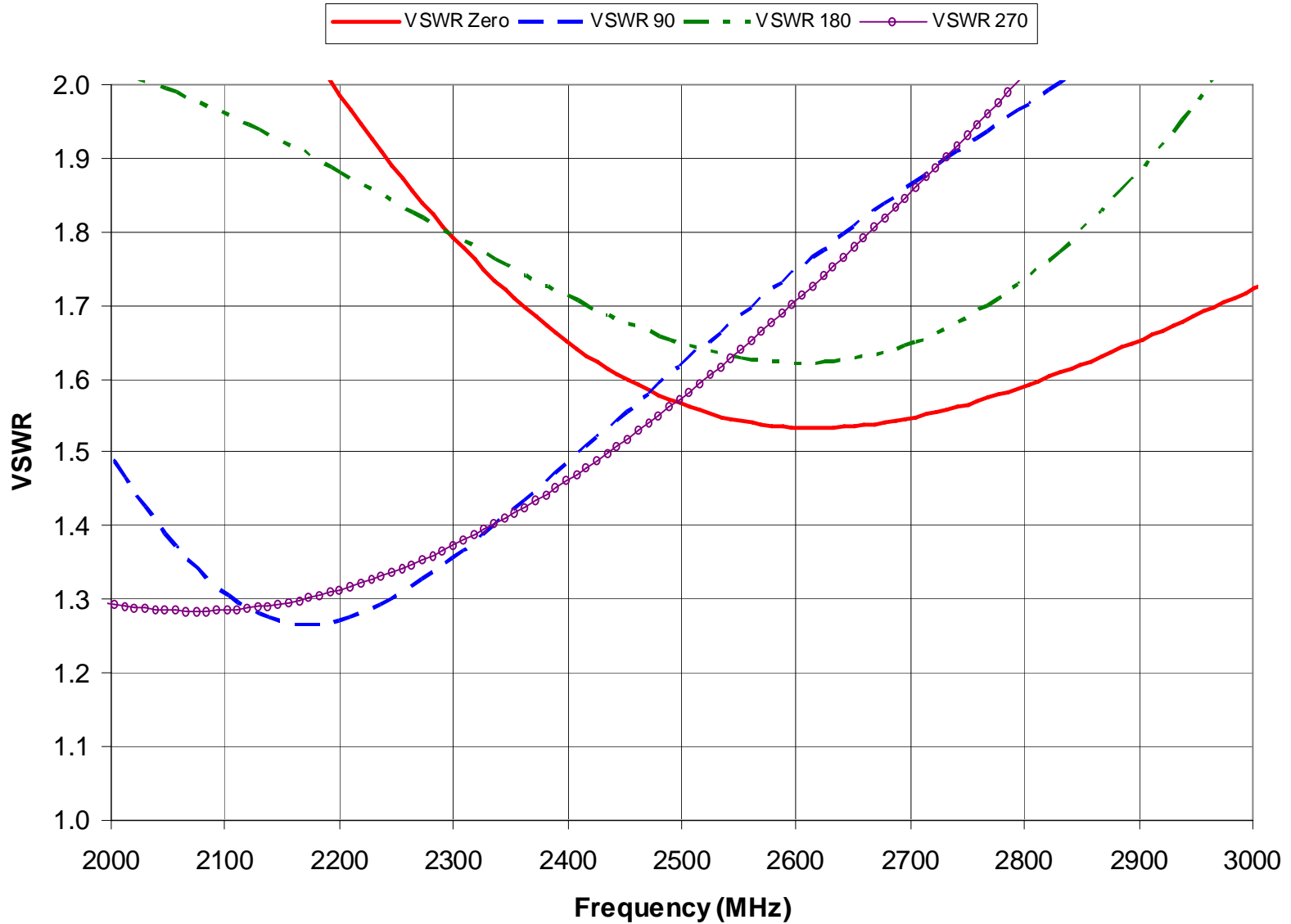
- Frequency: 2305 MHz to 2497 MHz
- Insertion loss: Less than 4dB (3dB Goal)
- Insertion Balance: +/- 1dB
- Phase shift: 90 and 180 degrees steps
- VSWR, 50 Ohms: Less than 1.5:1
- Supply Voltage: +/- 5 Volts
- Control Voltage: TTL(goal); or 0, -5V
- Size: 60x60 mil ANACHIP



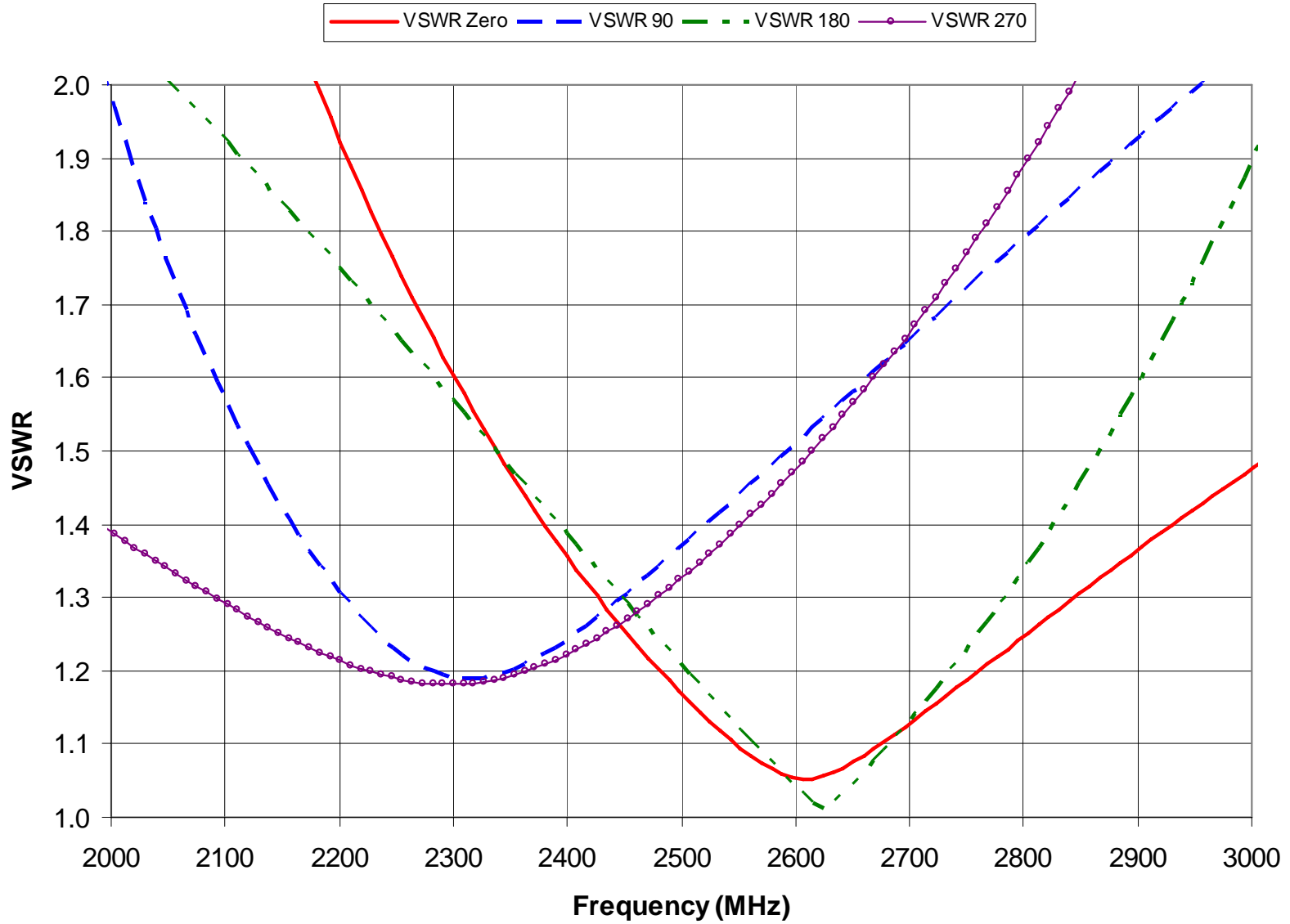
# Achieved Specification

- The Specification of VSWR better than 1.5:1 was not achieved.
- A VSWR better than 1.8:1 was achieved
- Frequency(1.8:1 VSWR): 2300 MHz to 2642 MHz
- 1.8:1 VSWR Bandwidth: 342 MHz
- Insertion loss: 3.77 dB (2300 to 2500 MHz)  
3.96 dB (2300 to 2642 MHz)
- Insertion Balance: 0.45 dB (2300 to 2500 MHz)  
0.68 dB (2300 to 2642 MHz)

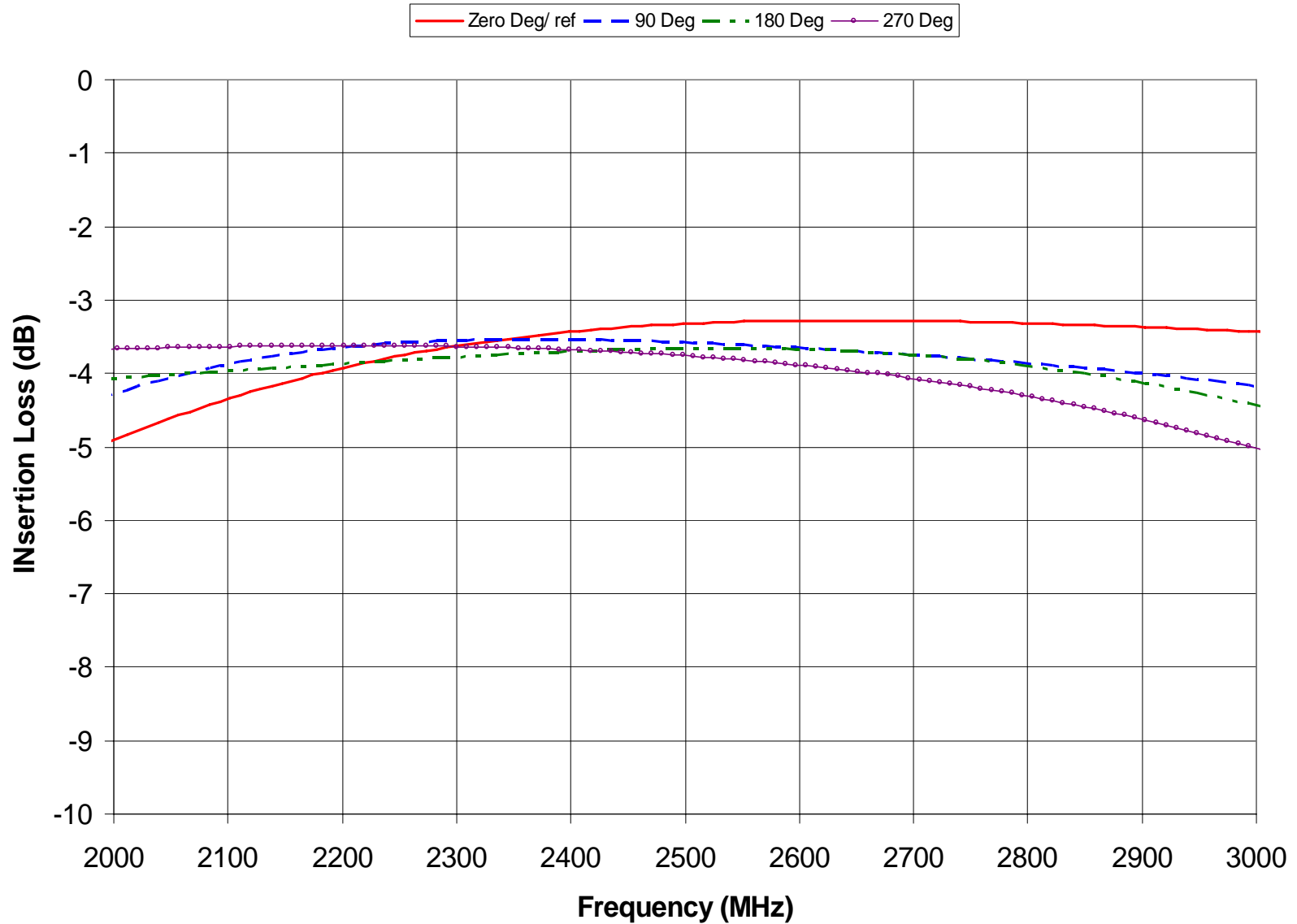
# Two Bit Phase Shifter Input VSWR



# Two Bit Phase Shifter Output VSWR



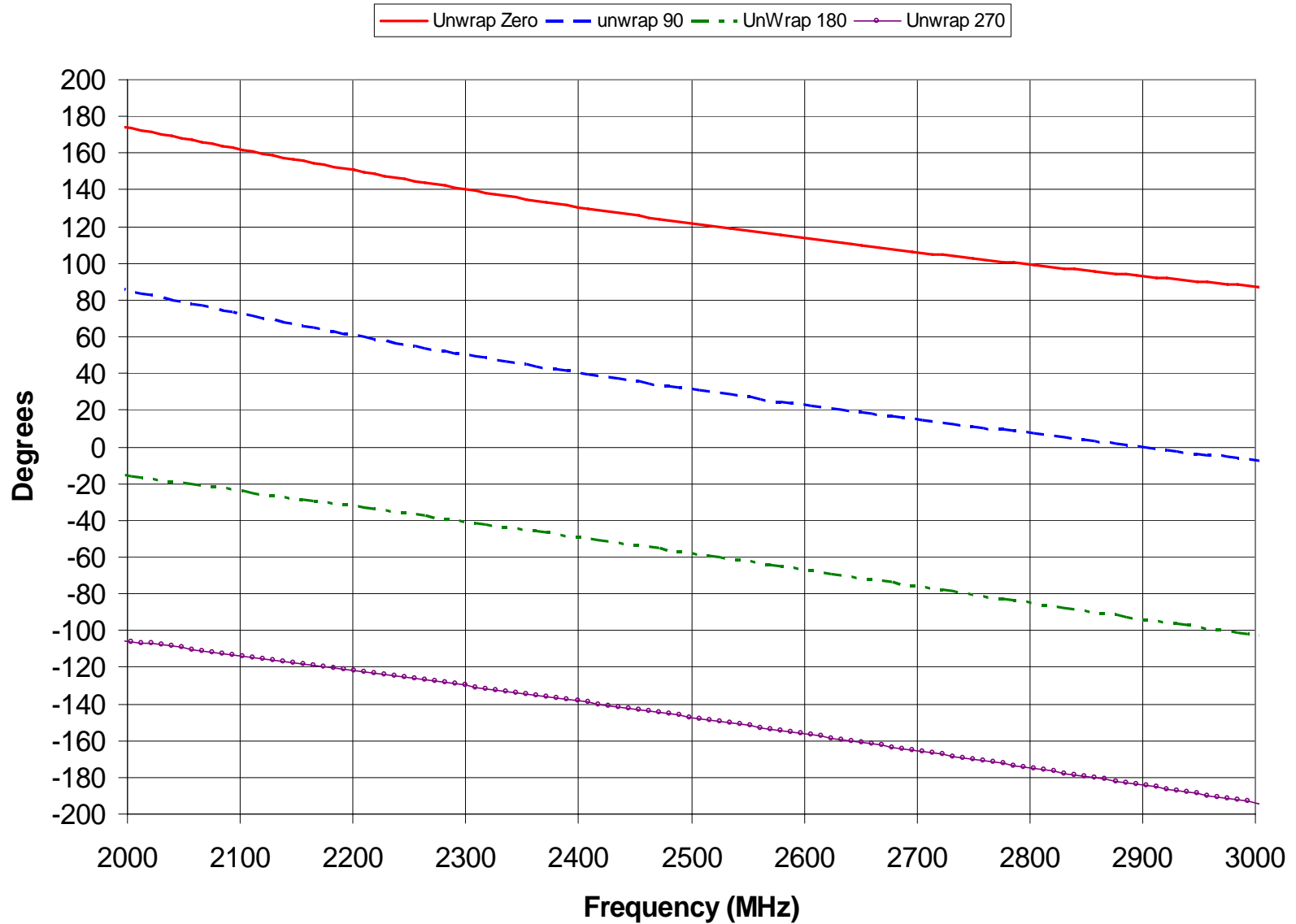
# Two Bit Phase Shifter Insertion Loss (S21)



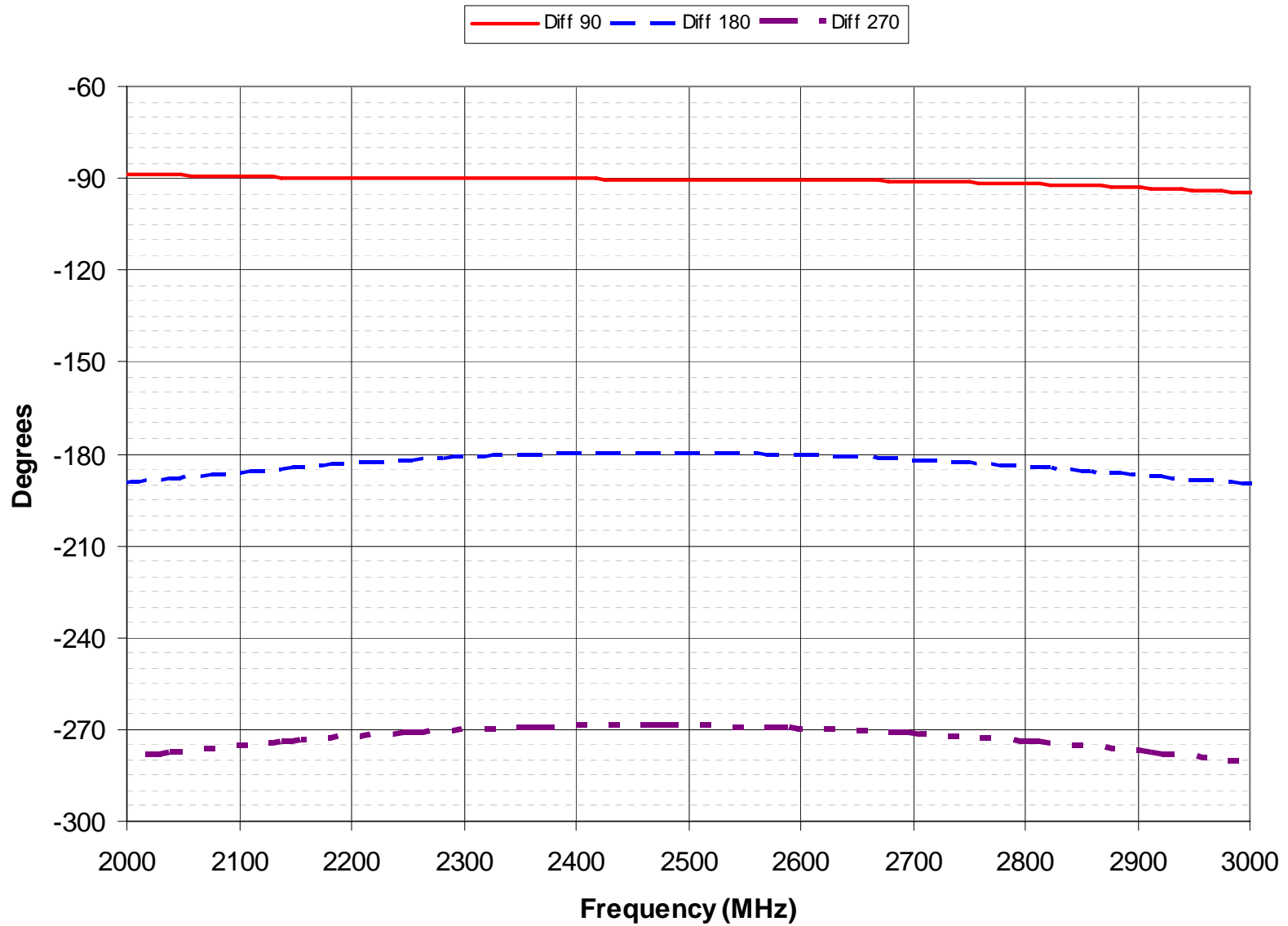
# Achieved Specification

- Phase Shift: 90 and 180 degrees step
- Phase Flatness (2300 to 2500 MHz):
  - 90 Degree Shift -- 0.15 Deg.
  - 180 Degree Shift -- 1.4 Deg.
  - 270 Degree Shift -- 0.15 Deg.
- Phase Flatness (2300 to 2642 MHz):
  - 90 Degree Shift -- 0.53 Deg.
  - 180 Degree Shift -- 1.40 Deg.
  - 270 Degree Shift -- 0.49 Deg

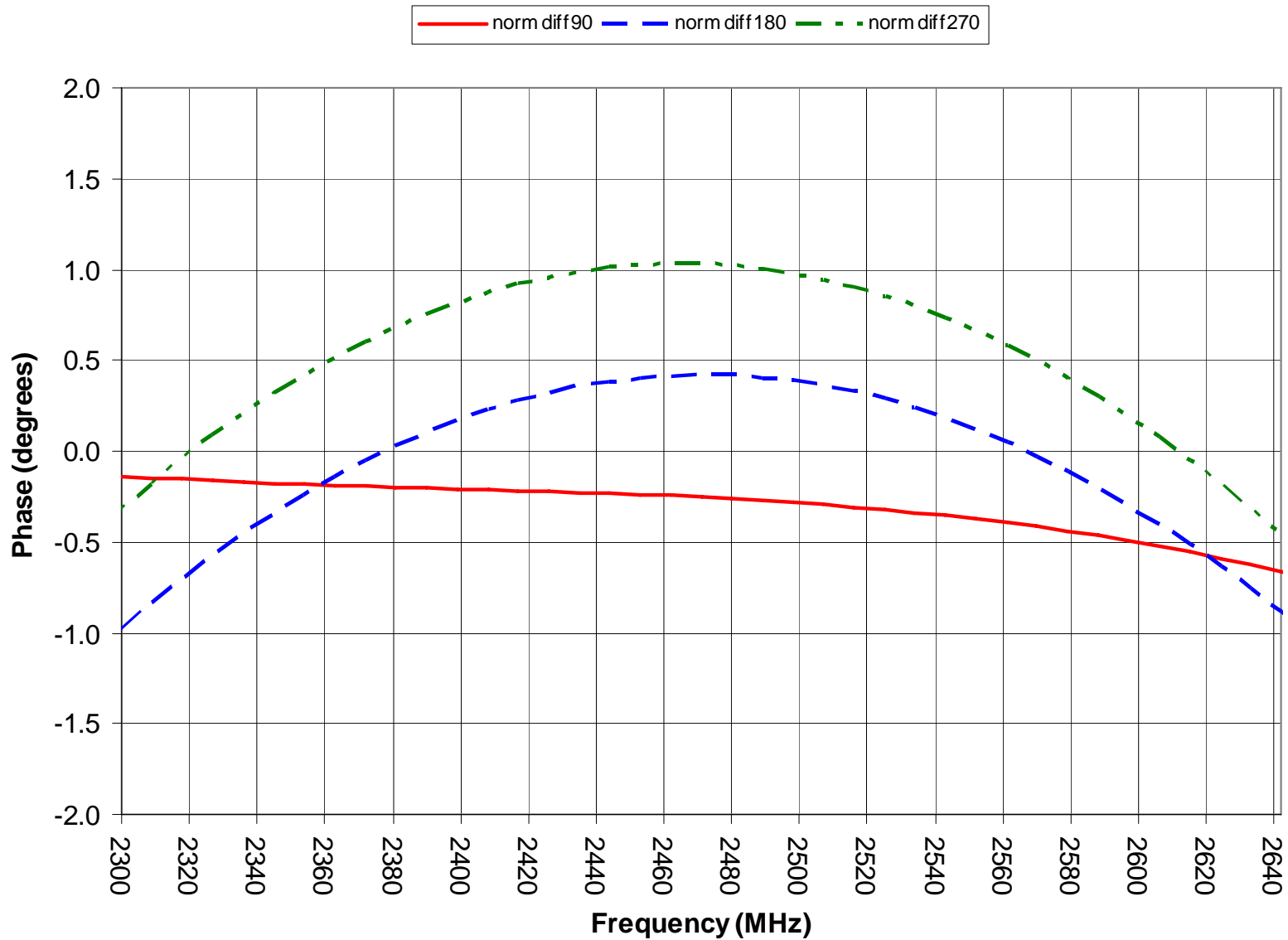
# Two Bit Phase Shifter Unwrap Phase (S21)



## Two Bit Phase Shifter; Phase Difference

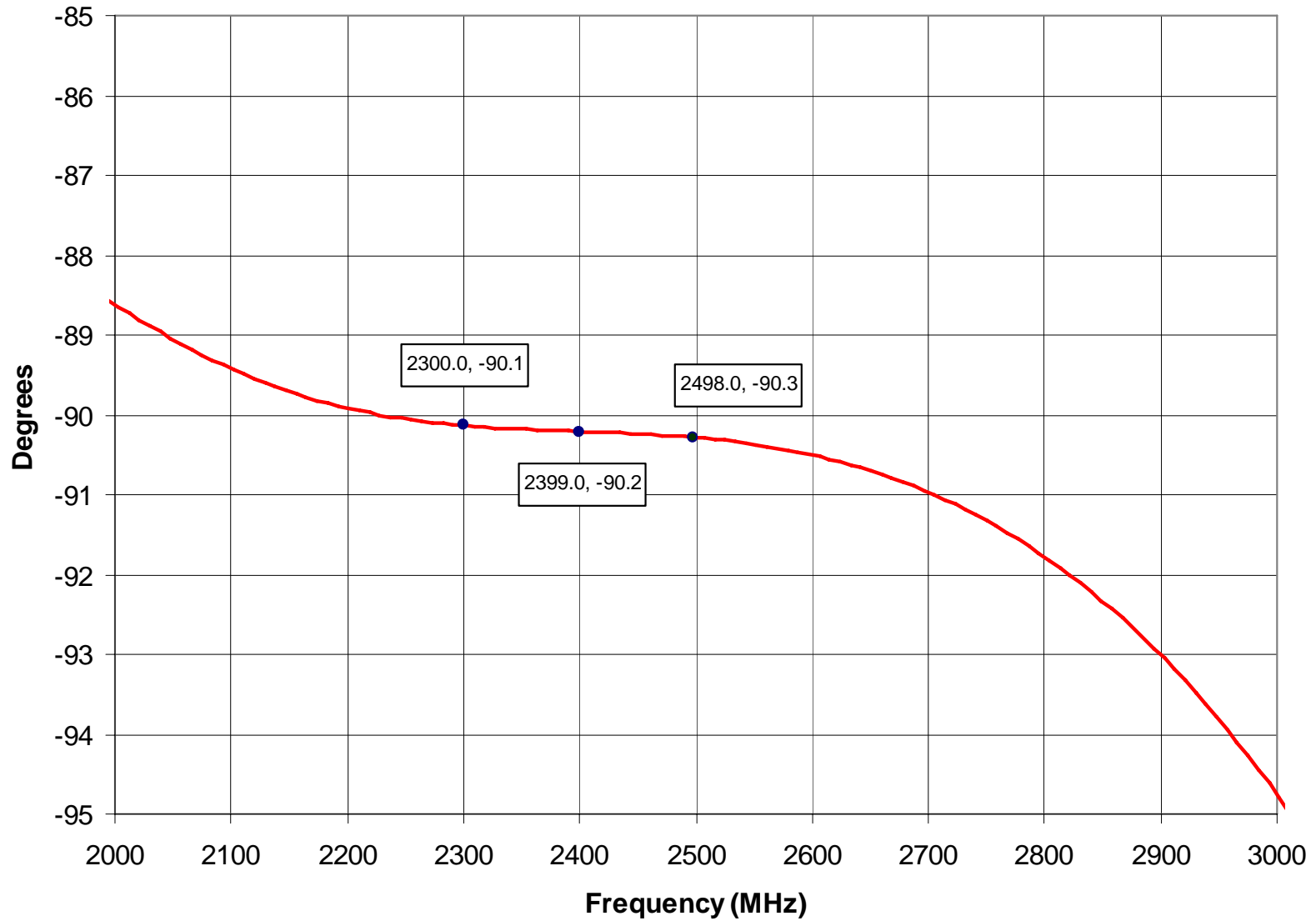


## Two Bit Phase Shifter: Normalized Phase Difference

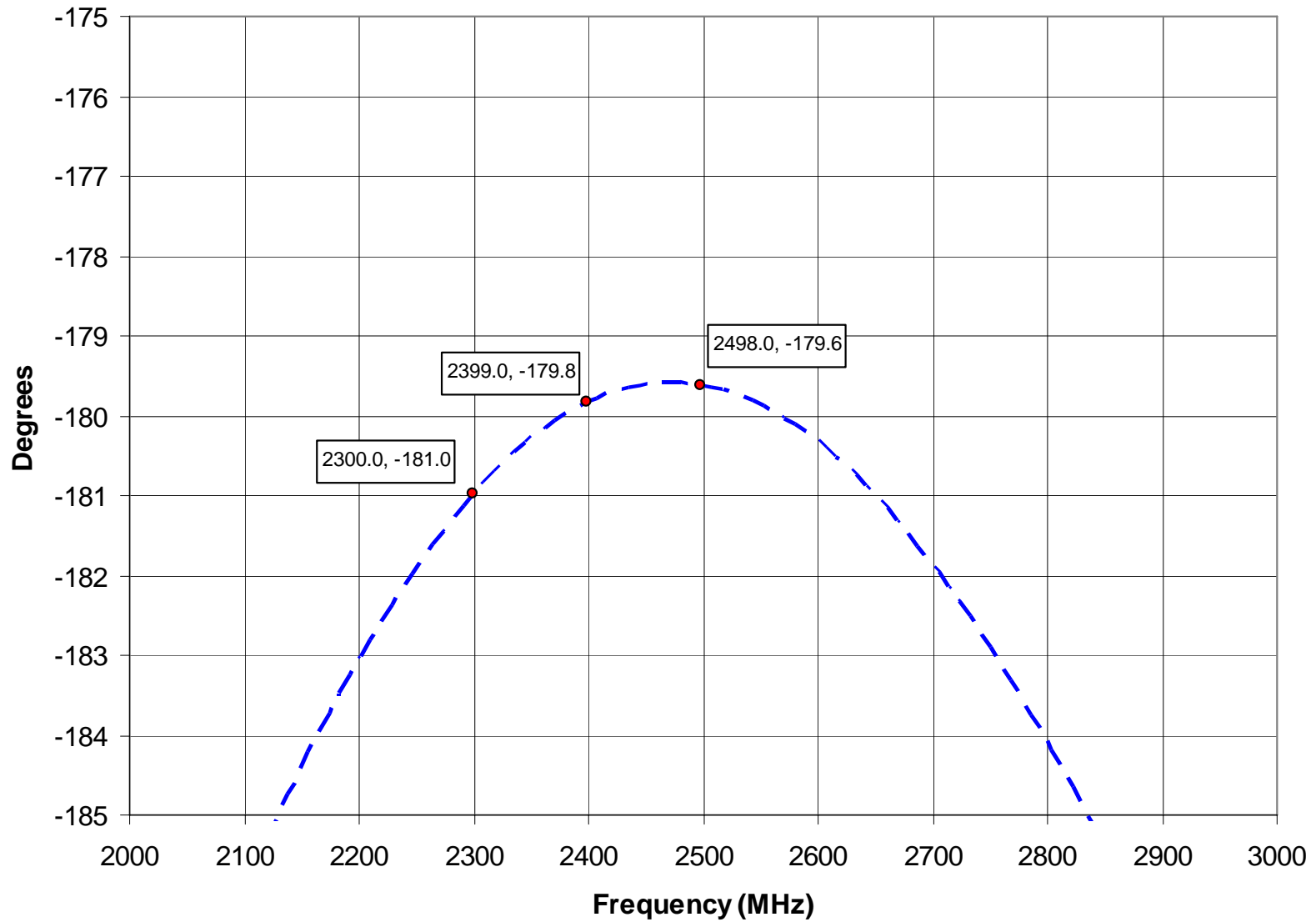




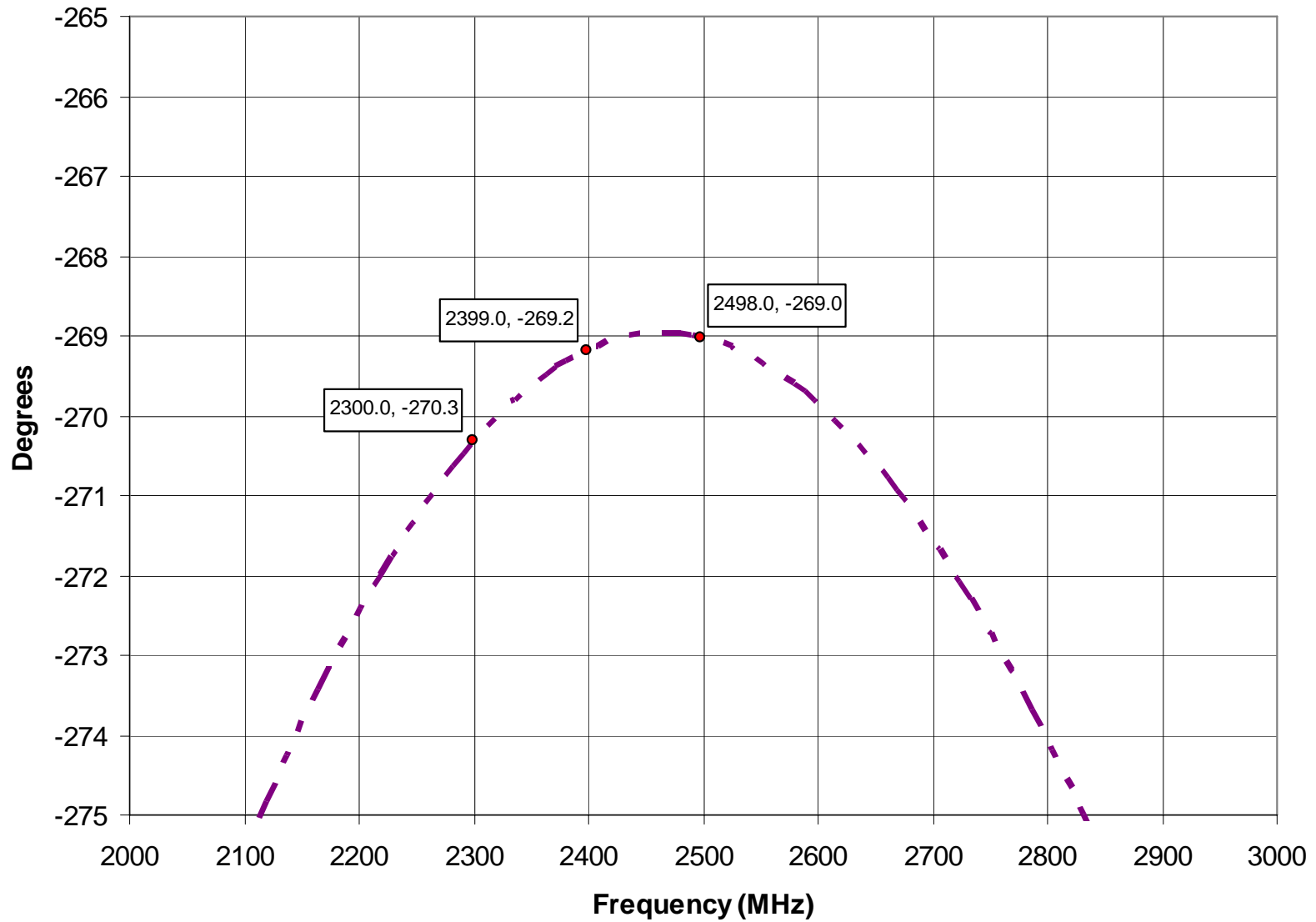
## Two Bit Phase Shifter; Phase Difference = 90 Degrees



## Two Bit Phase Shifter; Phase Difference = 180 Degrees



# Two Bit Phase Shifter; Phase Difference = 270 Degrees



# Achieved Specification

- Control Voltage is TTL (zero and +5V)
- Supply Voltage is +5 Volts
  
- Design fit on the 60 x 60 mil ANACHIP

# Things to look at

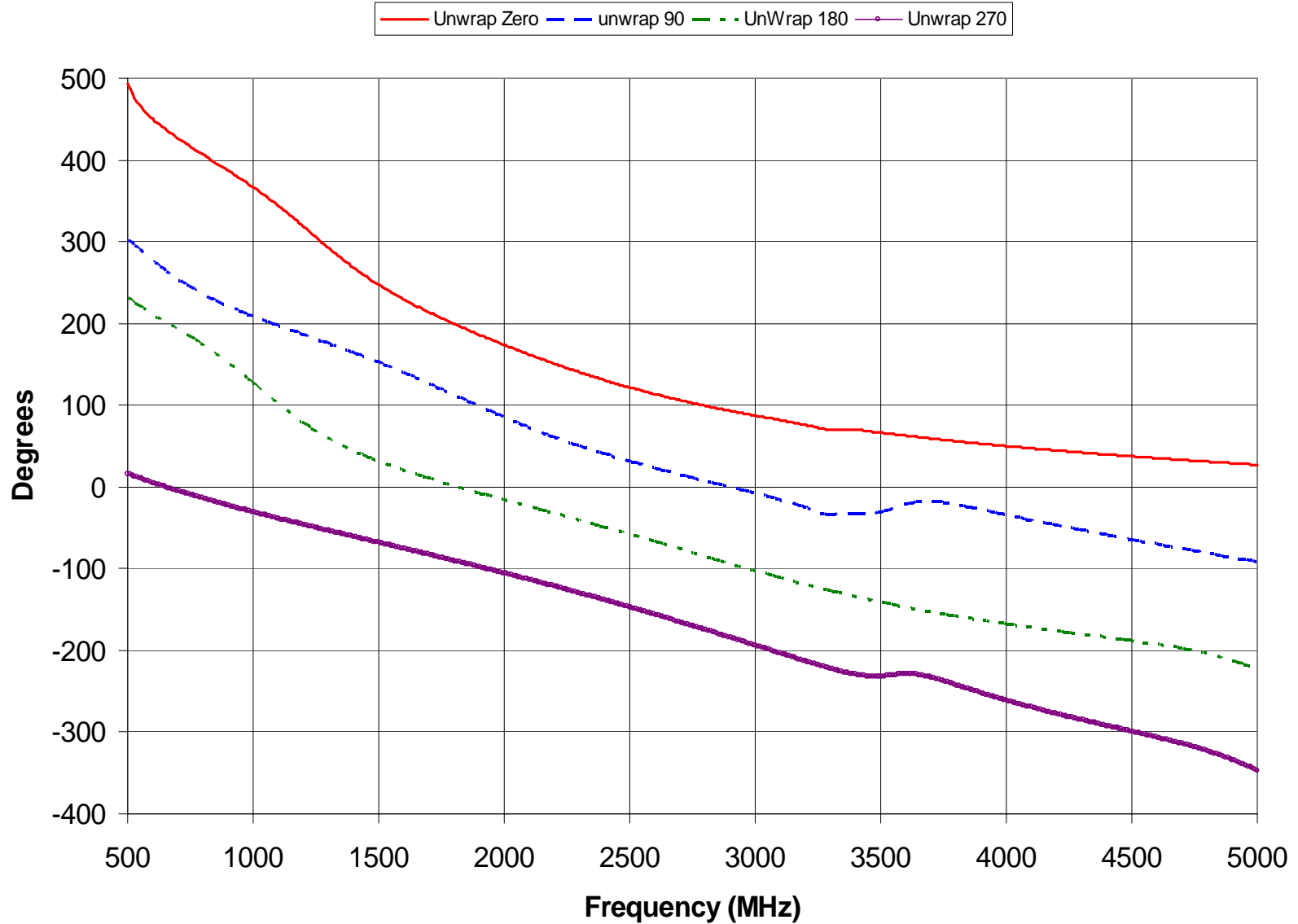
- Pay more attention to input VSWR
  - Concentrated on phase and insertion loss
- Switch size
  - Used default transistor size
  - A smaller switch may work as well while conserving space
- Wide Banding
  - Use two series 45 Deg element instead of a single 90 deg. element
- Switch gate voltage
  - Changed depending on phase selected

# DC Gate Bias

Phase Shift	Bit 45	Bit 90	Vgate Pos45 (V)	Vgate Neg45 (V)	Vgate Pos90 (V)	Vgate Neg90 (V)	Igate Pos45 (uA)	Igate Neg45 (uA)	Igate Pos90 (uA)	Igate Neg90 (uA)
0	0	0	1.42	2.50E-05	1.44	5.8E-07	86	0.000000306	64	0.000000333
90	5	0	0.005	1	1.2	7.8E-08	0.00000001	0.7	12	0.000000045
180	0	5	1.2	1.90E-05	0.005	1	11	0.000000045	0.000000011	0.7
270	5	5	0.0039	1	3.82E-07	1	0.000000017	0.759	0.000000017	0.759

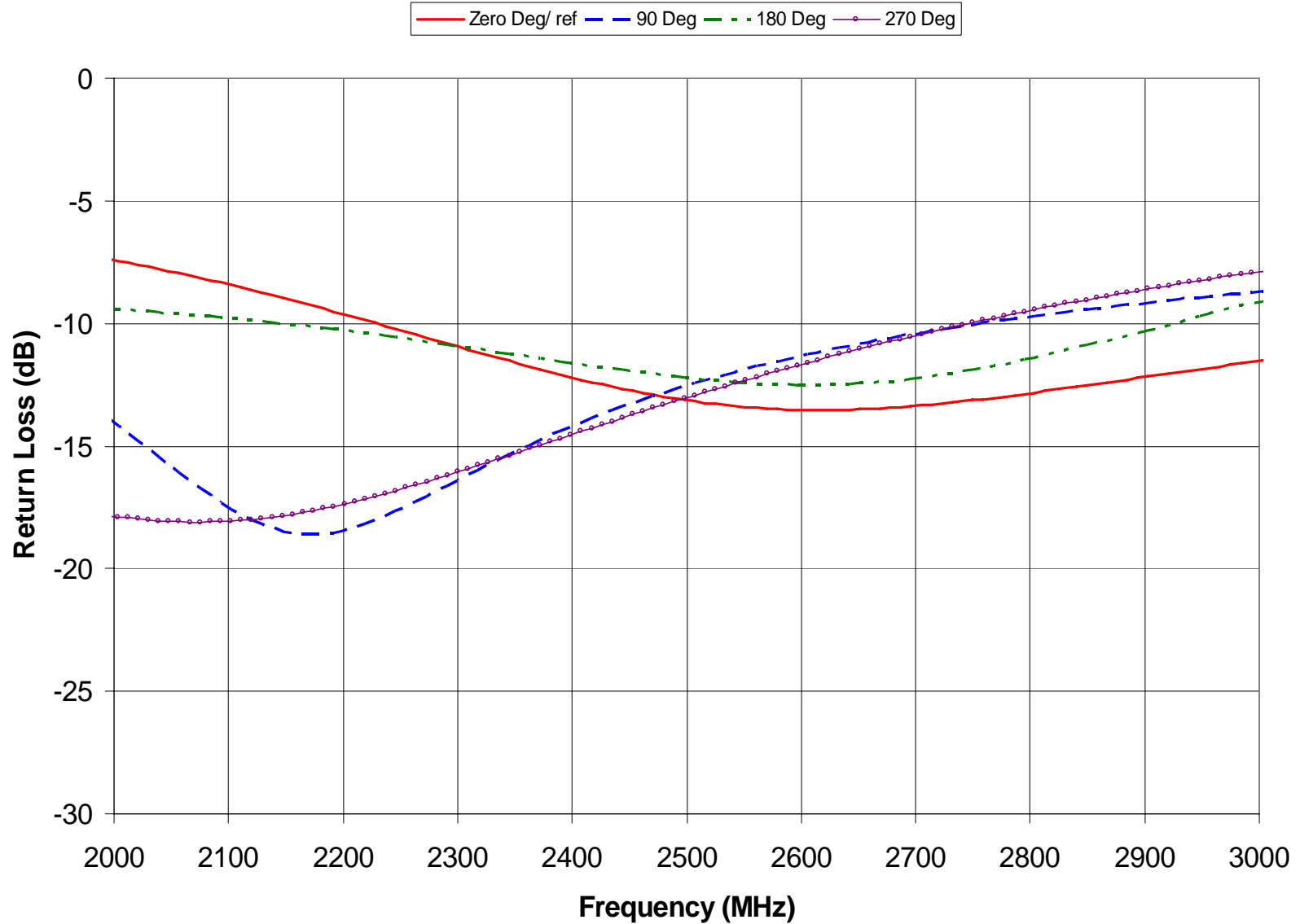
# Backup Slides

## Two Bit Phase Shifter Unwrap Phase (S21)

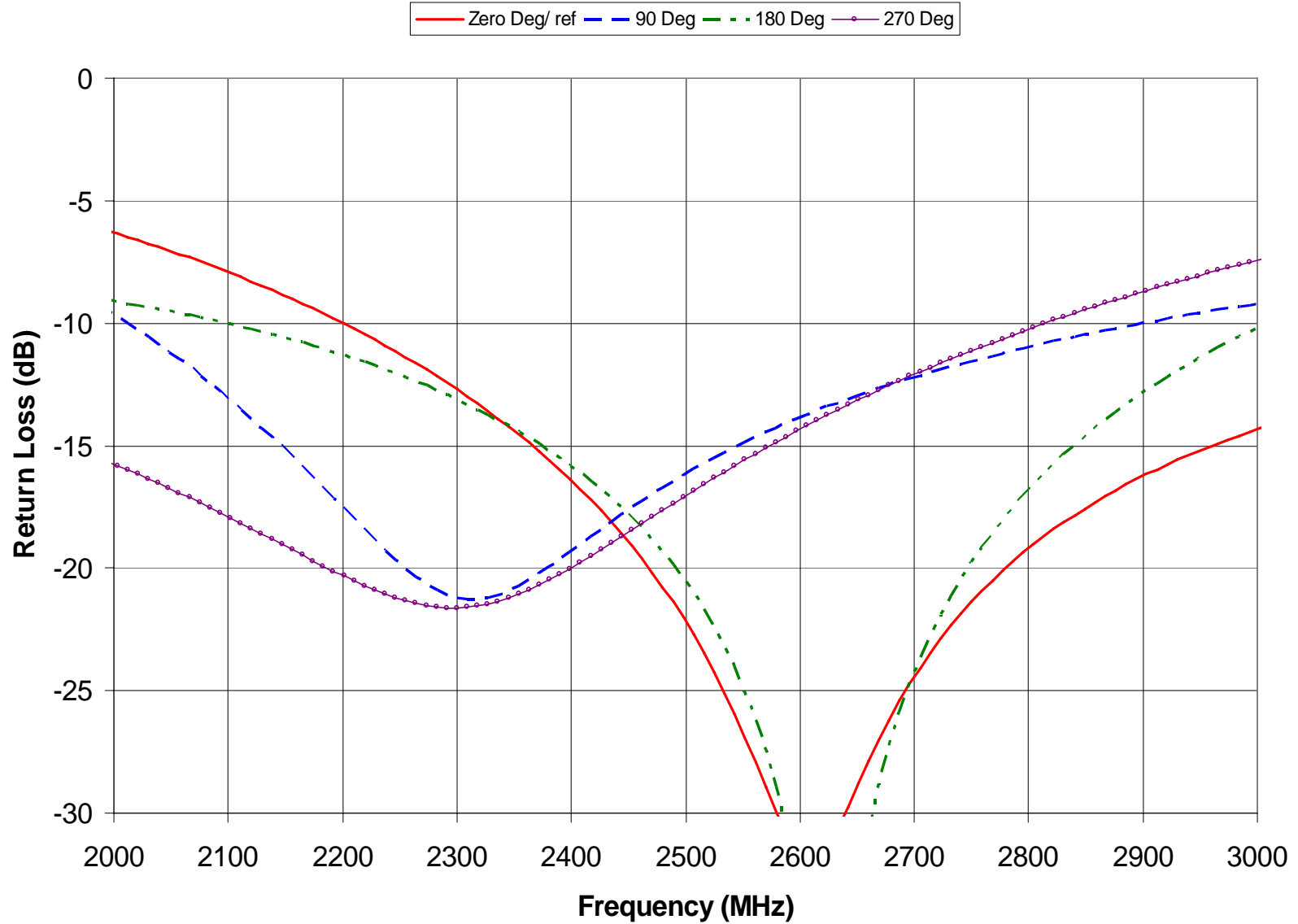




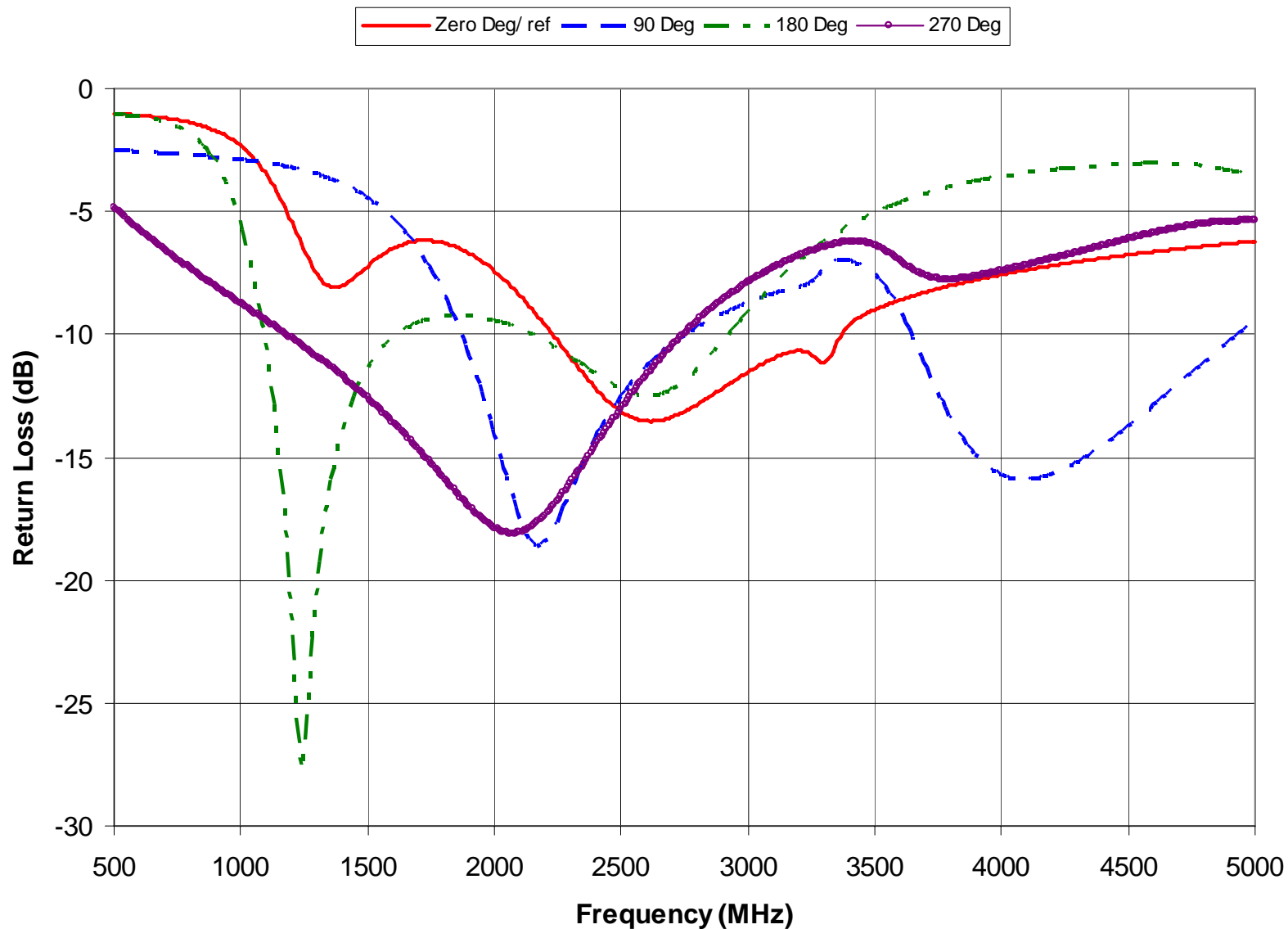
# Two Bit Phase Shifter Input Return Loss (S11)



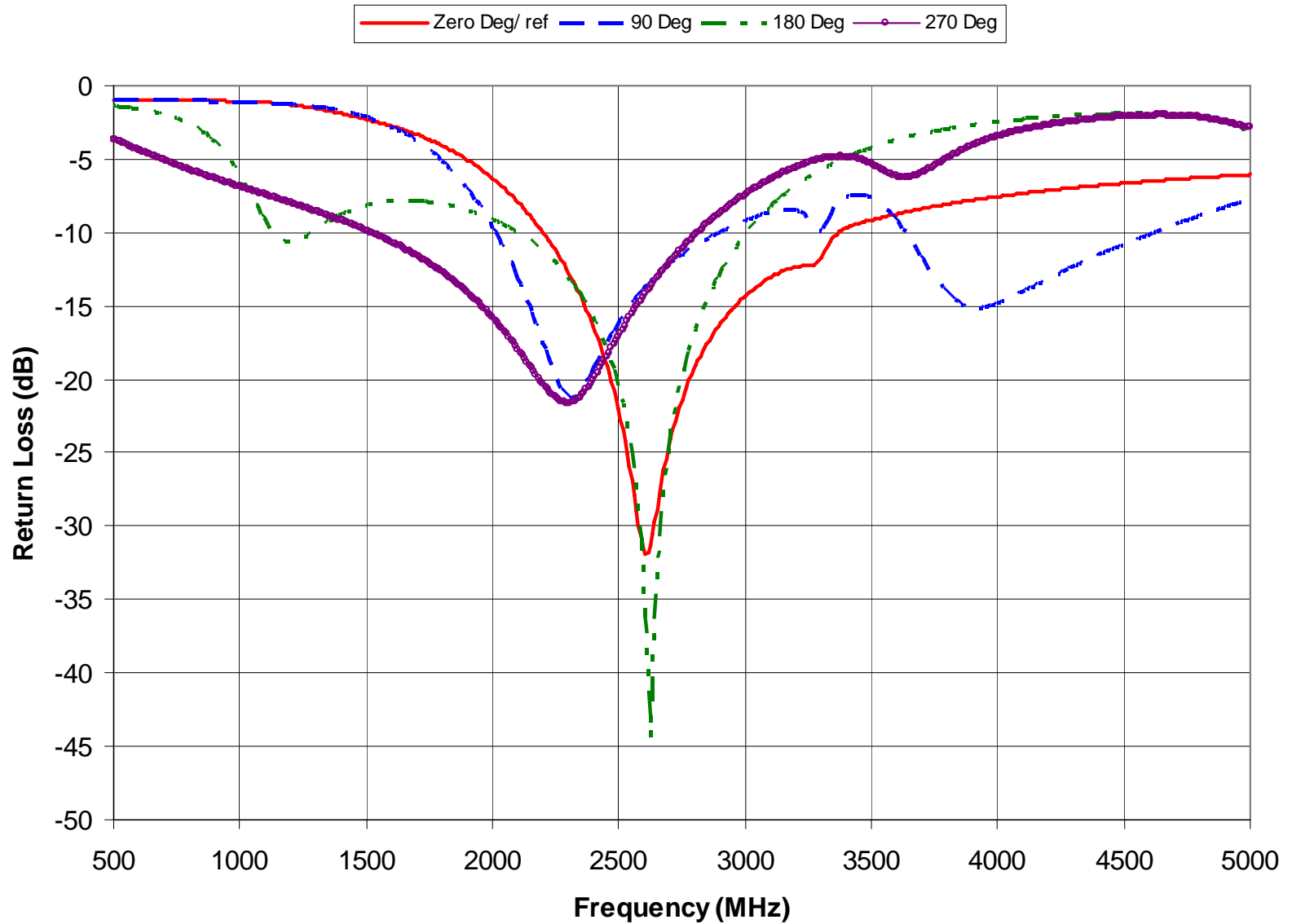
# Two Bit Phase Shifter Output Return Loss (S22)

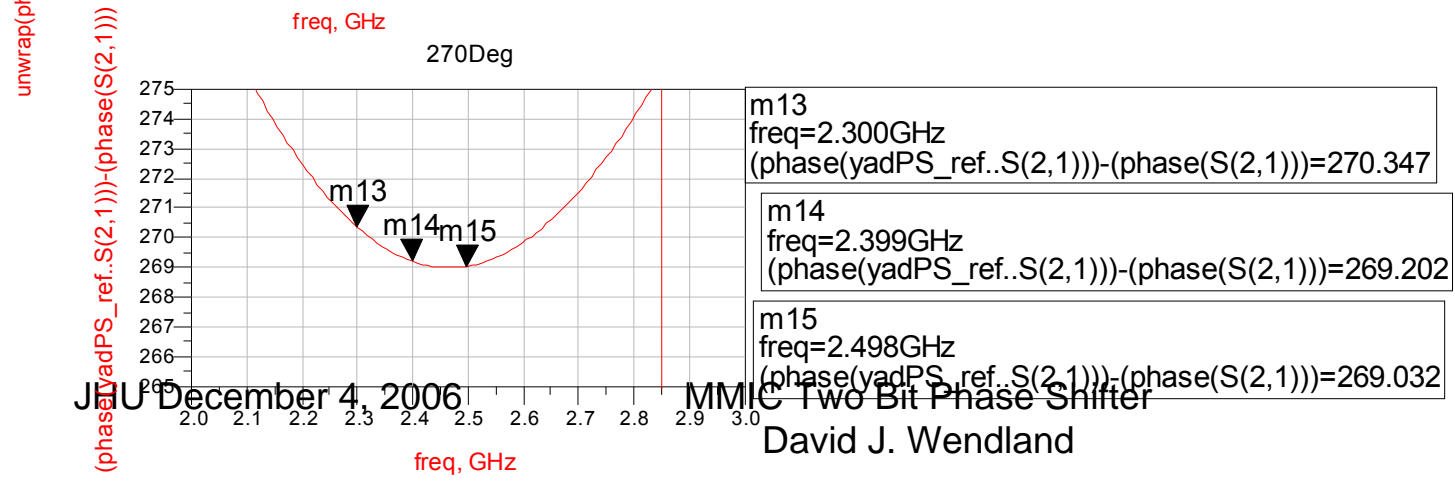
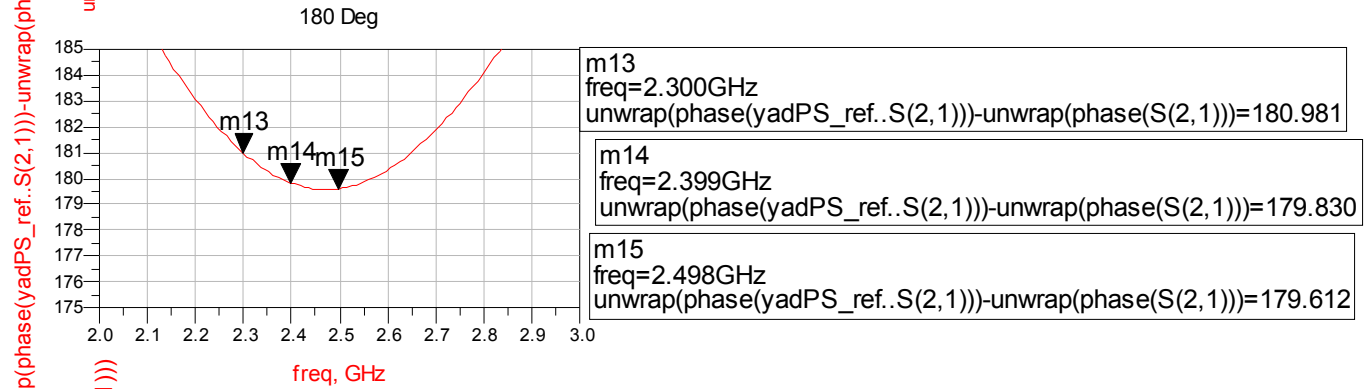
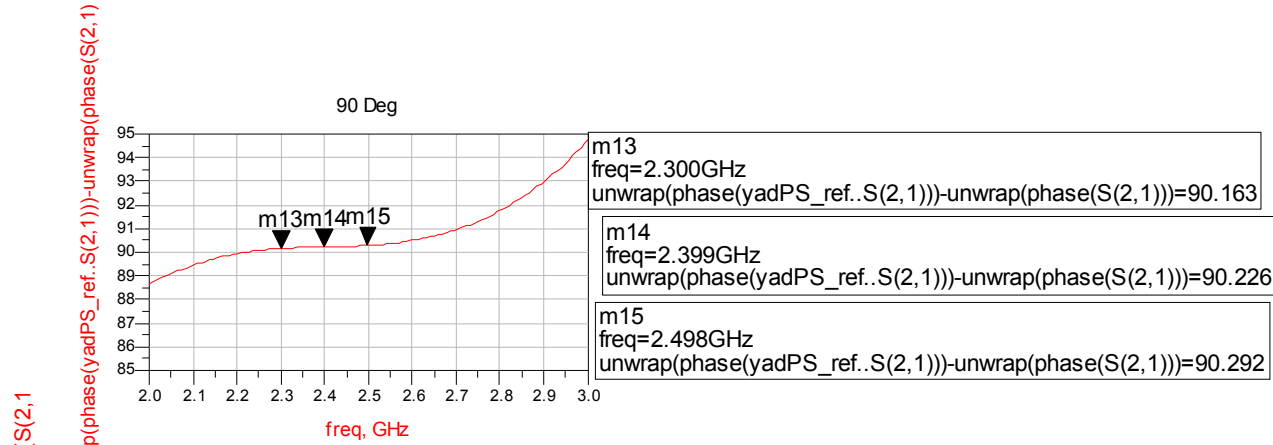


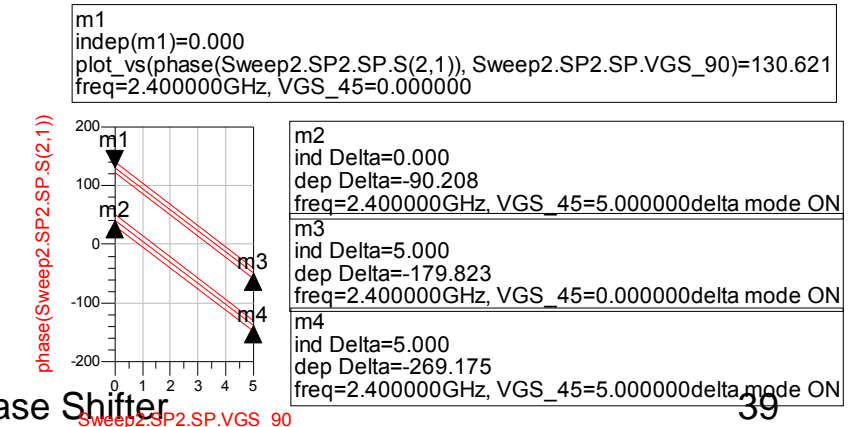
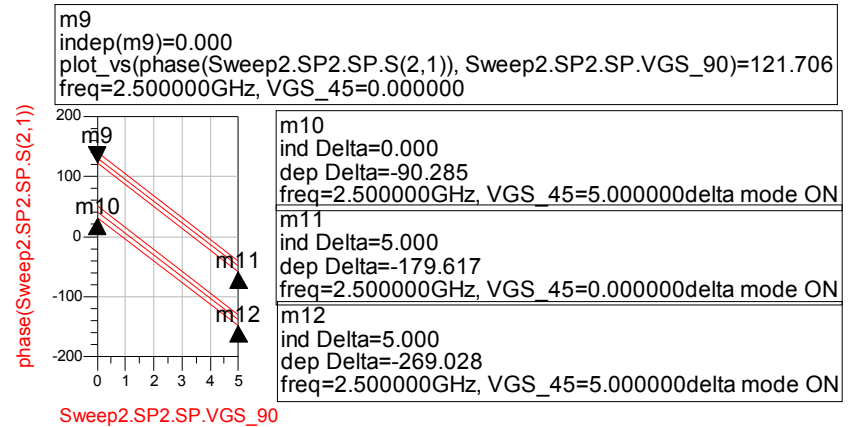
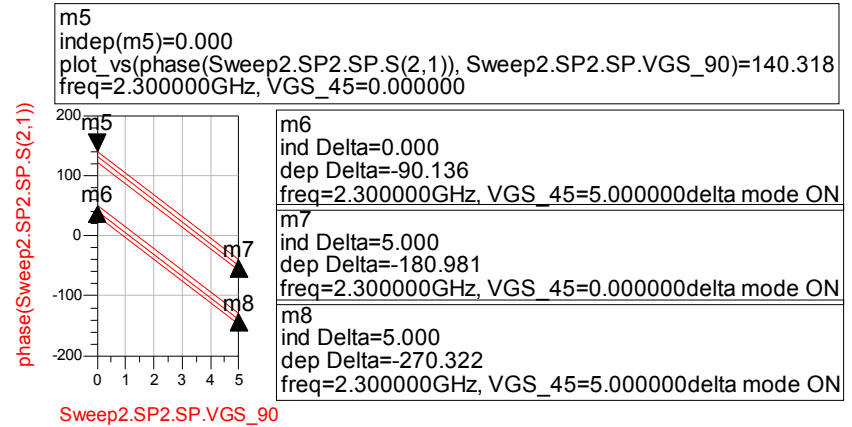
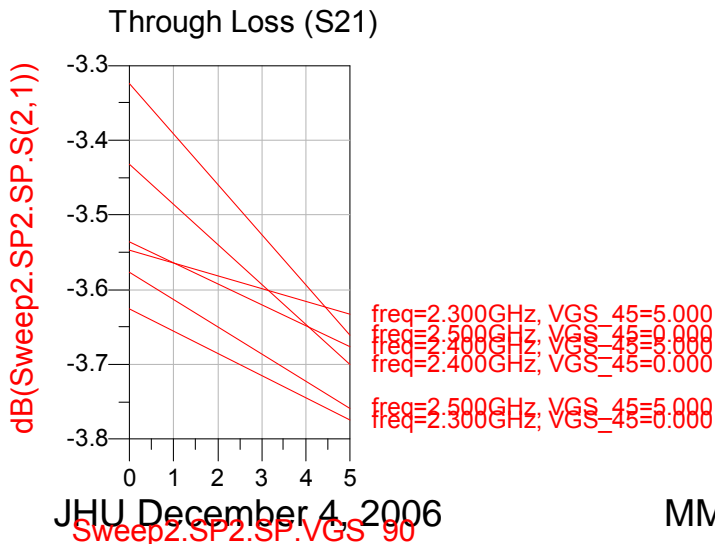
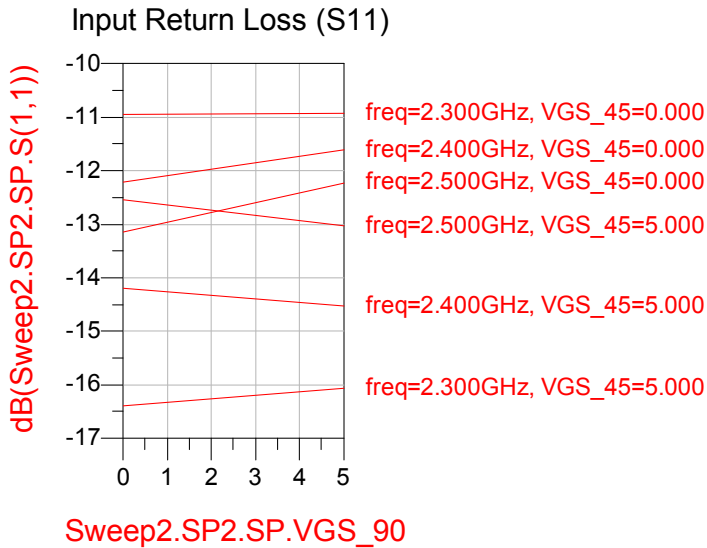
## Two Bit Phase Shifter Input Return Loss (S11)



## Two Bit Phase Shifter Output Return Loss (S22)







# **S-Band Power Amplifier MMIC**

**Ben Myers  
Niral Patel**

**525.787  
MMIC Design  
Prof. Penn, Dr. Reece**

**JHU Fall 2006**

## **Abstract**

This report describes the design, simulation and layout of a two-stage GaAs MMIC power amplifier, operating at S-band from 2.305 to 2.497 GHz as the final pre-radiator element of a transmit chain which forms part of a wireless communications (WCS) transceiver system. The power amplifier design was a class project for Johns Hopkins University's MMIC Design Course (525.787), Fall 2006. The GaAs process used was Triquint Semiconductor's TQPED process.

### **1. Introduction**

Typical modern RF and microwave transmitter designs feature an integrated-circuit power amplifier directly behind the radiating element (whether single-antenna or phased-array element), for maximum RF power output and efficiency. For the power amplifier design described here, the power output specified was 20 dBm with 18 dB of stage gain and > 20% power-added efficiency (PAE).

The initial circuit design was carried out in Agilent's Advanced Design System software. The designers at first hoped to use a single TQPED 50um x 6 gain stage. It became apparent, however, that while the 18 dB gain spec could be met with a single stage, it was not possible to simultaneously achieve 20 dBm of output power, 20-25% PAE at 1dB compression, and maintain unconditional stability in this way. Therefore the designers shifted to a two-stage topology, a 25um x 6 pre-driver followed by a 50um x 6 power output stage, which was the final choice of DFET transistor selection.

### **2. Circuit Design**

Turning to the details of the design, the designers considered a single bias voltage input but ultimately rejected this option in order to avoid complications in the layout. Both stages' drains are biased at +5.2 V and both gates at -0.1 V.

To meet the power-output and PAE specifications, the designers traded against output matching, resulting in an output VSWR of 4:1-6:1 (S22 of 3-4 dB), which though exceeding the input and output VSWR spec of 1.5:1, did not present a significant system performance risk since the PA output will "see" only the transmit radiator, which can be matched to a specific impedance more easily than other system components. A load-pull analysis of the power-amp output is included with this report, which illustrates where on the Smith Chart the best Pout and PAE performance was achieved in terms of impedance seen by the design.

Once the designers settled on the two-stage configuration, they created ideal input and output stabilization and matching networks in ADS for each stage, using TriQuint's models. Stringing the stages together and verifying the gain and PAE performance, the



designers noted that the interstage matching (pre-driver OMN, power stage IMN) totaled two inductors and two capacitors but provided a relatively small impedance transform in terms of the Smith chart. Eliminating both inductors and retaining one small interstage capacitor, they obtained a significant layout area savings.

With the ideal-element circuit created, the designers began the process of inserting TriQuint TQPED inductors, capacitors and resistors while at the same time initiating the layout on a 60 mil x 60 mil ANACHIP die. Large-value RF choke inductors on the bias lines, and DC blocking capacitors at the input and output, consumed the most real estate. Fortunately, the designers had been able to use relatively small capacitors and inductors for input, interstage and output matching, allowing for compaction of the active stages in the center of the layout.

Working iteratively between ADS's Schematic and Layout windows and making use of its design synchronization feature, the designers completed the layout in the 60 mil x 60 mil area with relatively few DRC and LVS errors. Some issues that the designers corrected included: drain voltage traces that needed to be widened for current-handling capacity (changed from metal0 to metal1) and making sure that all substrate vias matched up between the schematic and layout.

**Table 1: Simulated Design Performance**

<b>Spec</b>	<b>Spec Value</b>	<b>Simulated (TQPED)</b>
Operating Band	2.305 – 2.497 GHz	2.3 to 2.5 GHz
Bandwidth	0.8 GHz	“ “ “
Output Power	20 dBm	21.6 dBm
Gain	18 dB	~ 28 dB over band
PAE	> 20% @ 1dB compression, goal 25%	23.2% @ 1 dB compression
VSWR	< 1.5:1, input and output	Input ~ 1.05:1, output ~ 5:1
Supply Voltage	+5 / -5 V	+5 V, -0.1 V
Size	60 x 60 mil	60 x 60 mil

Design is unconditionally stable, 0.5 to 5 GHz.

Full charts for all simulated parameters are attached to this report.

## Schematic

A schematic of the final design is shown below in Figure 1. The first stage consists of a 150um periphery. Two stabilizing resistors are used on the input so as to minimize loss in power. Single L-C network stage is used on the input, while on the output, an interstage match was adopted to improve bandwidth and reduce components. The second stage consists of a 300um periphery part. Again, two stabilizing resistors are used on the input and an L-C matching network on the output of the transistor.

For both parts, approximately 5V is connected to the drain and -0.1V on the gate.

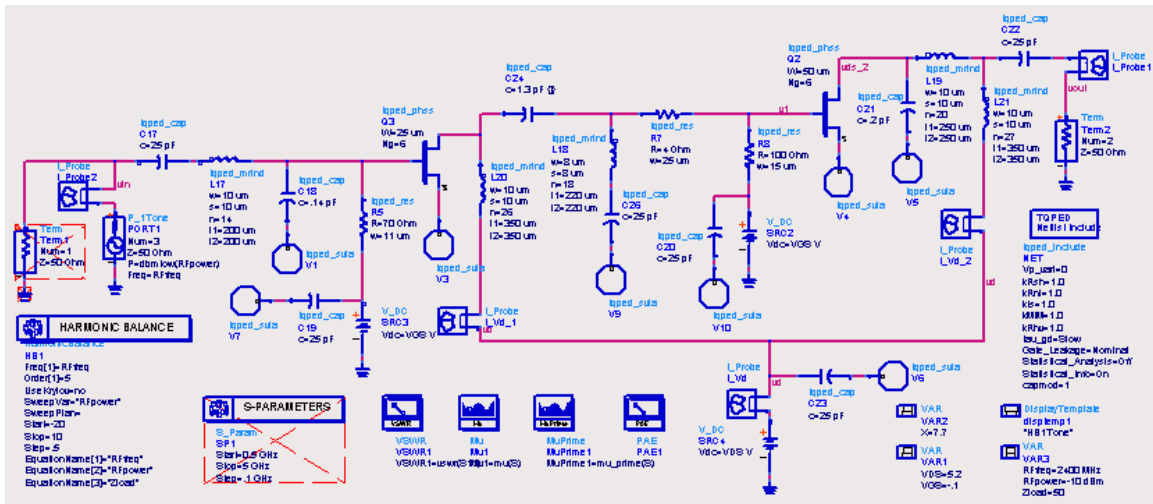


Figure 1. Final Schematic with Triquint Elements

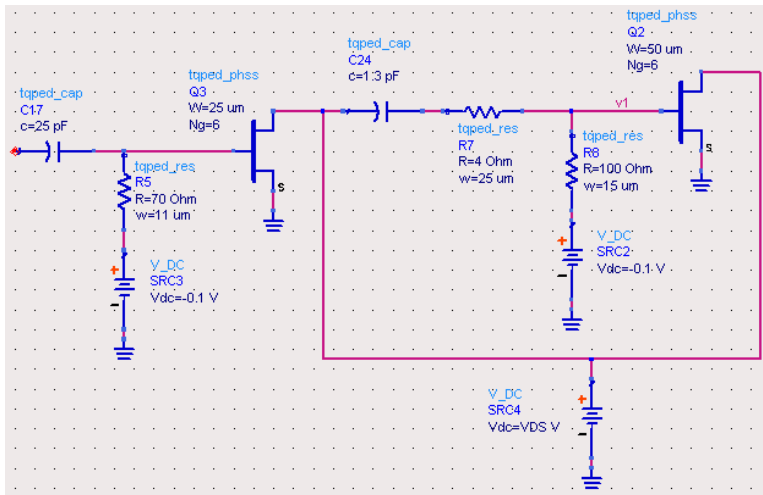


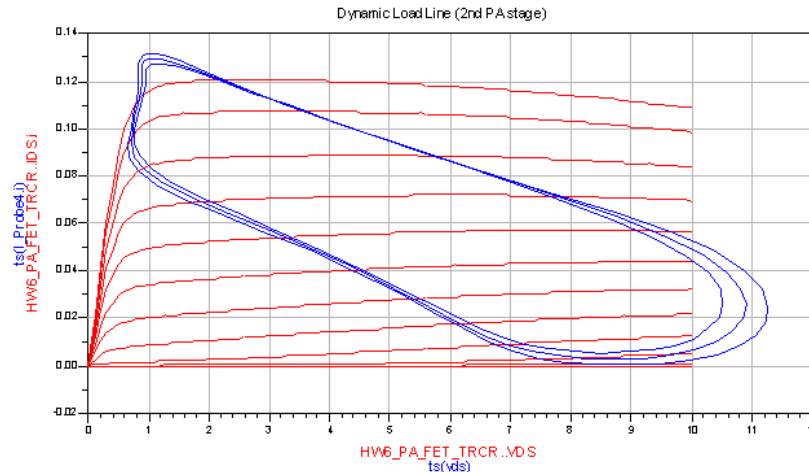
Figure 2. DC Schematic

## Simulations

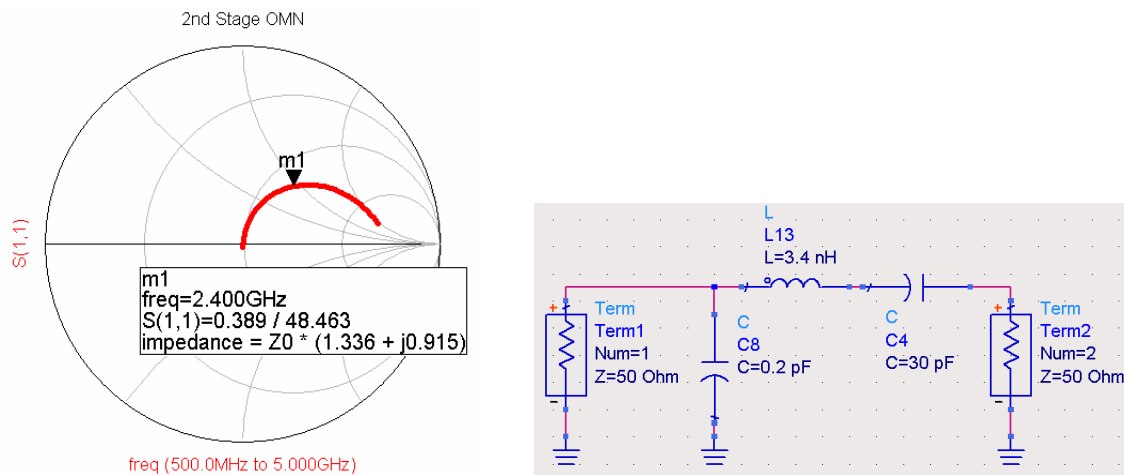
The second stage is critical as far as getting maximum power out. The first stage as mentioned before is really just for meeting the gain requirement. Since the heart of this design is the power amplifier, special attention is given to the second stage of this power amplifier MMIC. We will start by looking at this second stage, show in the schematic above.

We matched the output of the power amplifier using Cripps method. That is, we determine the Cripps resistance from the DC load line. We find this to be around  $70\Omega$ . The real part of our output match needs to match this resistance and we must resonate out the imaginary part. Upon doing so, we obtain values similar to what's in the schematic.

A simulation of the second stage verifies that we are achieving the maximum power out of the part. The require output power is at 21.3dBm with ideal parts and 20.5dBm after the power amplifier is complete with real components.



**Figure 3.** Second Stage's Dynamic Load Line showing maximum power out



**Figure 4.** Stage 2: OMN obtained using Cripps method

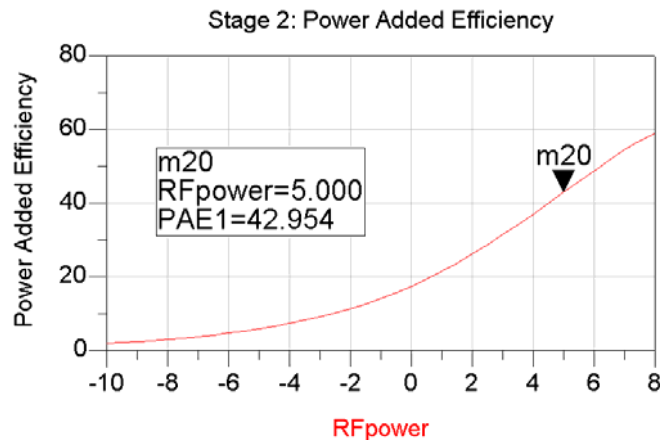


Figure 5. Second Stage's PAE

With some spare time we wanted to demonstrate ADS's Load Pull Analysis capability and see how close our match using Cripps method was to it. In previous design courses, the designers had use G-CAD, a design/layout software which allowed one to look at contours of constant power on the Smith Chart. A similar attempt is made here with ADS. We start out with the schematic shown below, which can be obtained from ADS's Design Examples.

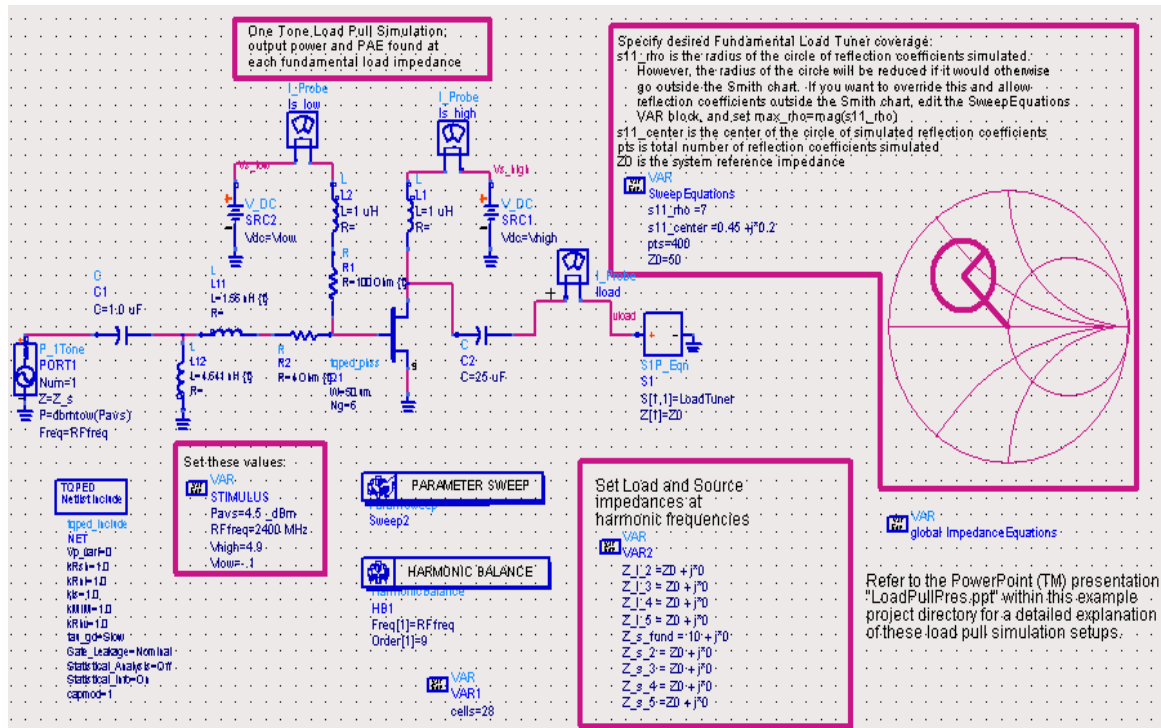
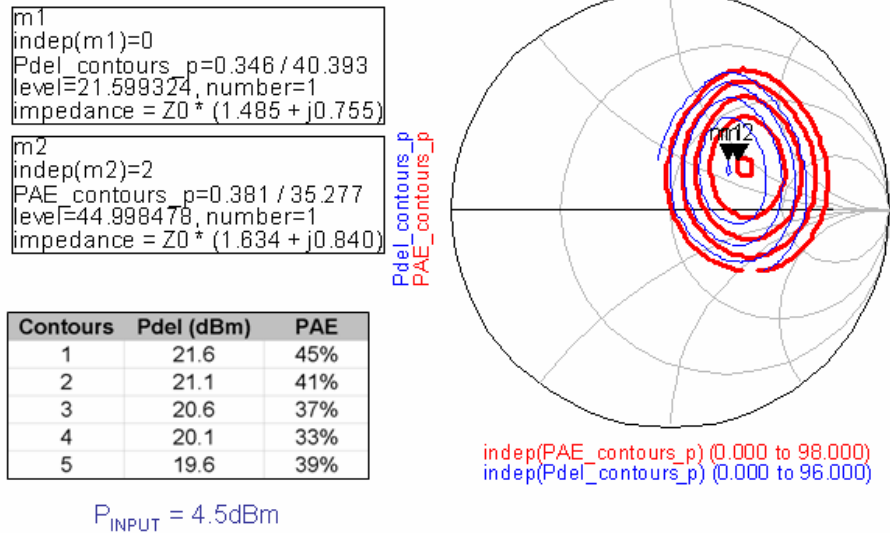


Figure 6. ADS Load Pull Schematic Modified from Design Examples



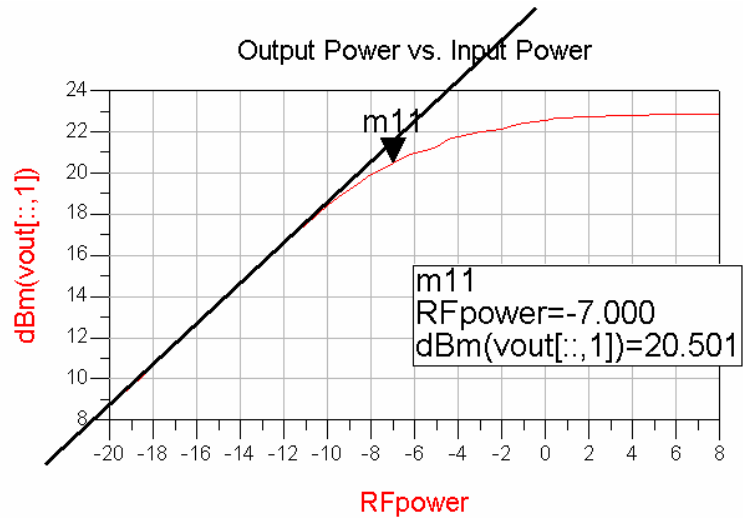
**Figure 7.** *2<sup>nd</sup> Stage Match from Load Pull Simulation*

We show that both methods of matching for maximum output power correlate reasonably well in ADS software. The load pull shows a power match at normalized impedance of  $1.49+j0.76$  ohms, and the Cripps method showed a power match at normalized impedance of  $1.34+j0.92$  ohms. The PAE is off slightly, since it is very sensitive to power level, as evident for the slope of the curve. While plotting the contours is a quicker method in terms of the number of steps and the amount of time needed to synthesize a match, they are both useful in verifying performance. However, since the Cripps method is more of an approximation, if the models were correct, the load pull analysis would probably be more trustworthy.

Now that we have completed giving an overview of the highlights of the power amplifier design, we will present the final simulations verifying the power amplifier design.

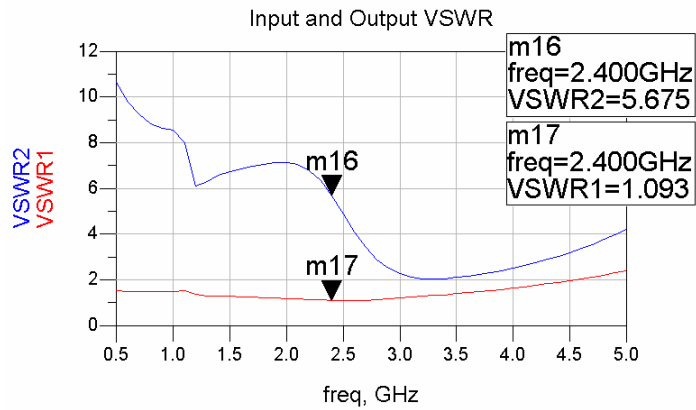
We show from the below simulations, the 1dB compression is at an output power of 20.5dBm, as hoped to be over 20dBm. The PAE here is 28%, which shows we passed the goal of 25%.

The overall performance is expected since we are using a part that just meets the needs of our power requirements. If DC power usage is not a critical parameter, one can certainly use larger parts. However, the designers found large VSWR issues with a larger part.



**Figure 8.** Final Power Amp-Output Power curve

Figure 8 shows the challenge of achieving the 1.5:1 VSWR spec on the output. For a power amplifier this is expected. With more matching components, this can be improved or made closer to 50ohms. Using a larger part to improve match and gain can be done, however this is at the expense of maximum power, which is not always desirable, but is certainly an option based on system needs.



**Figure 9.** Input and Output VSWR

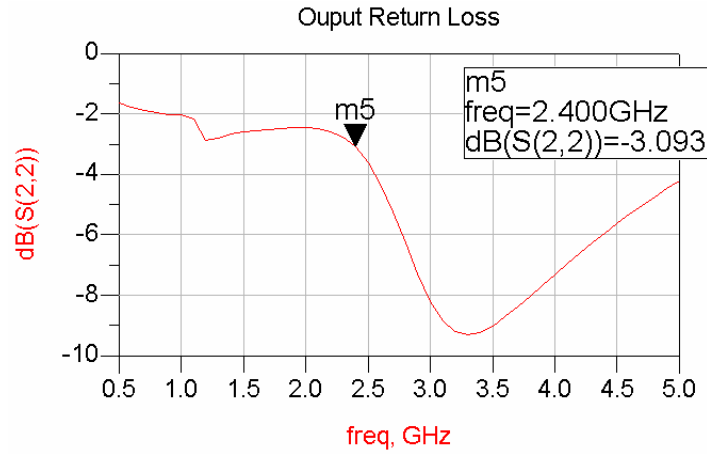


Figure 10. Output Return Loss

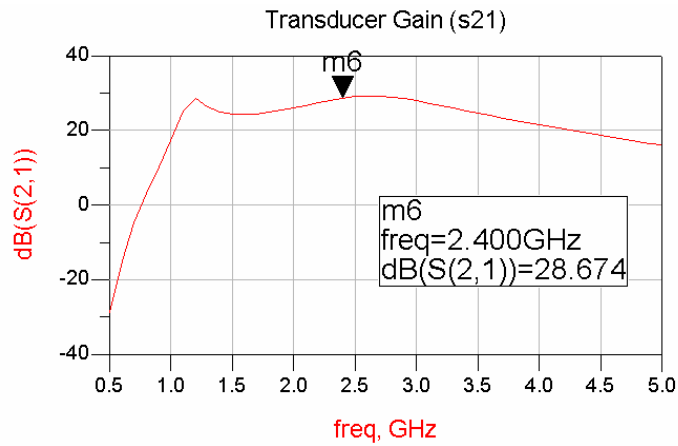


Figure 11. Amplifier Gain

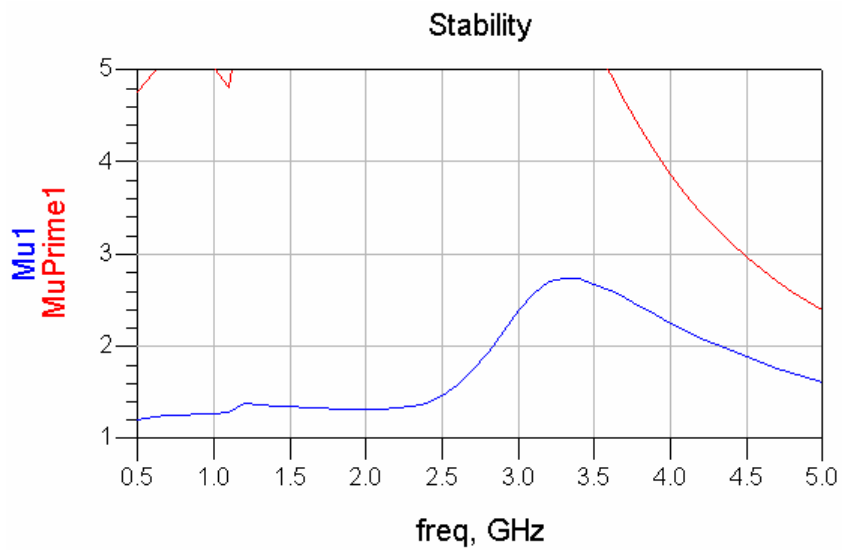


Figure 12. Stability Analysis showing unconditional stability

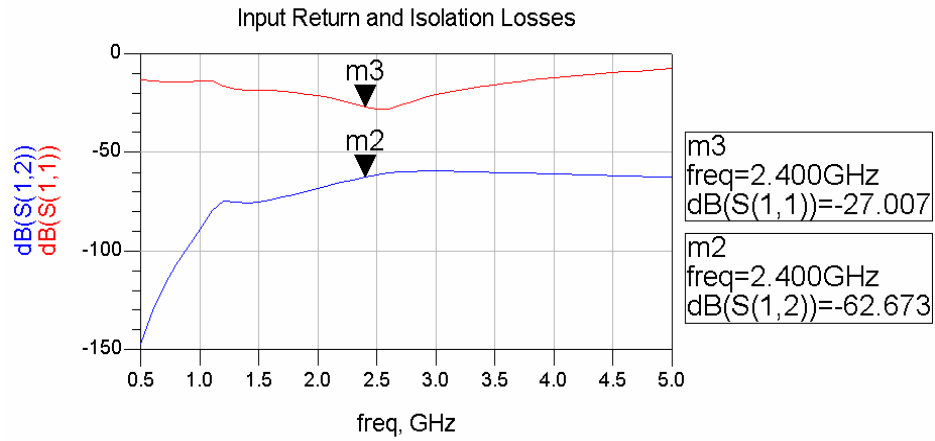


Figure 13. Input Return Loss and Isolation

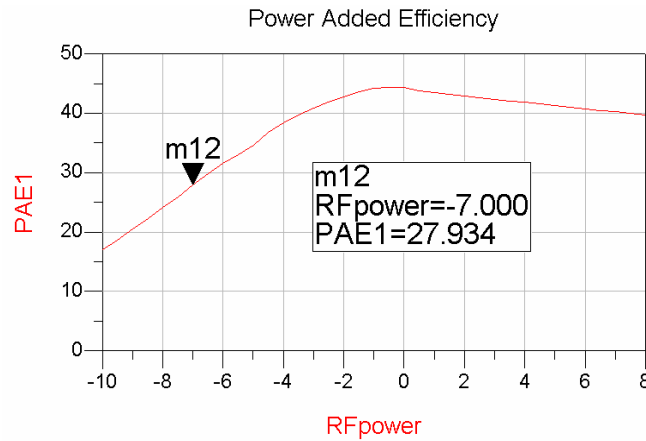


Figure 14. Power Amplifier PAE

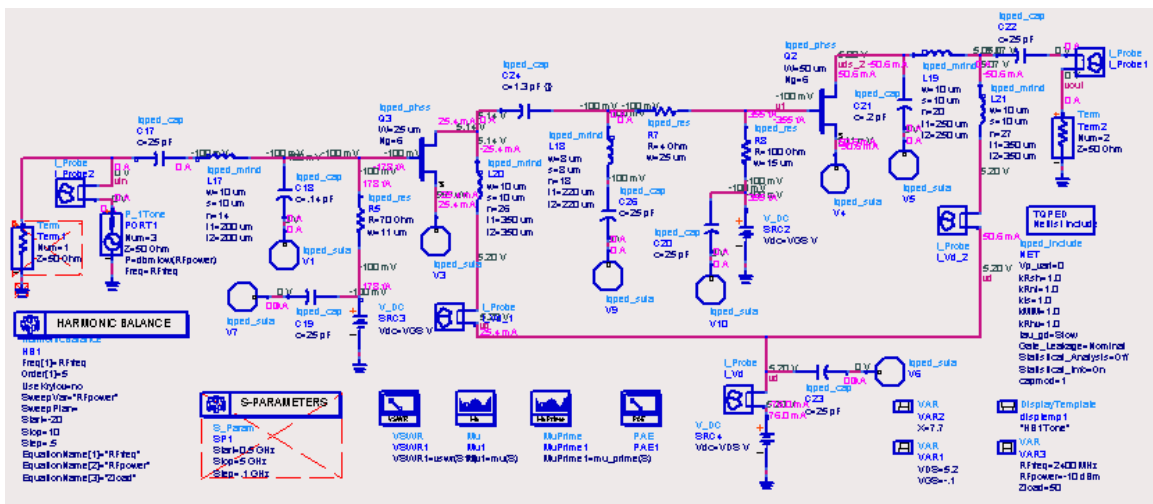
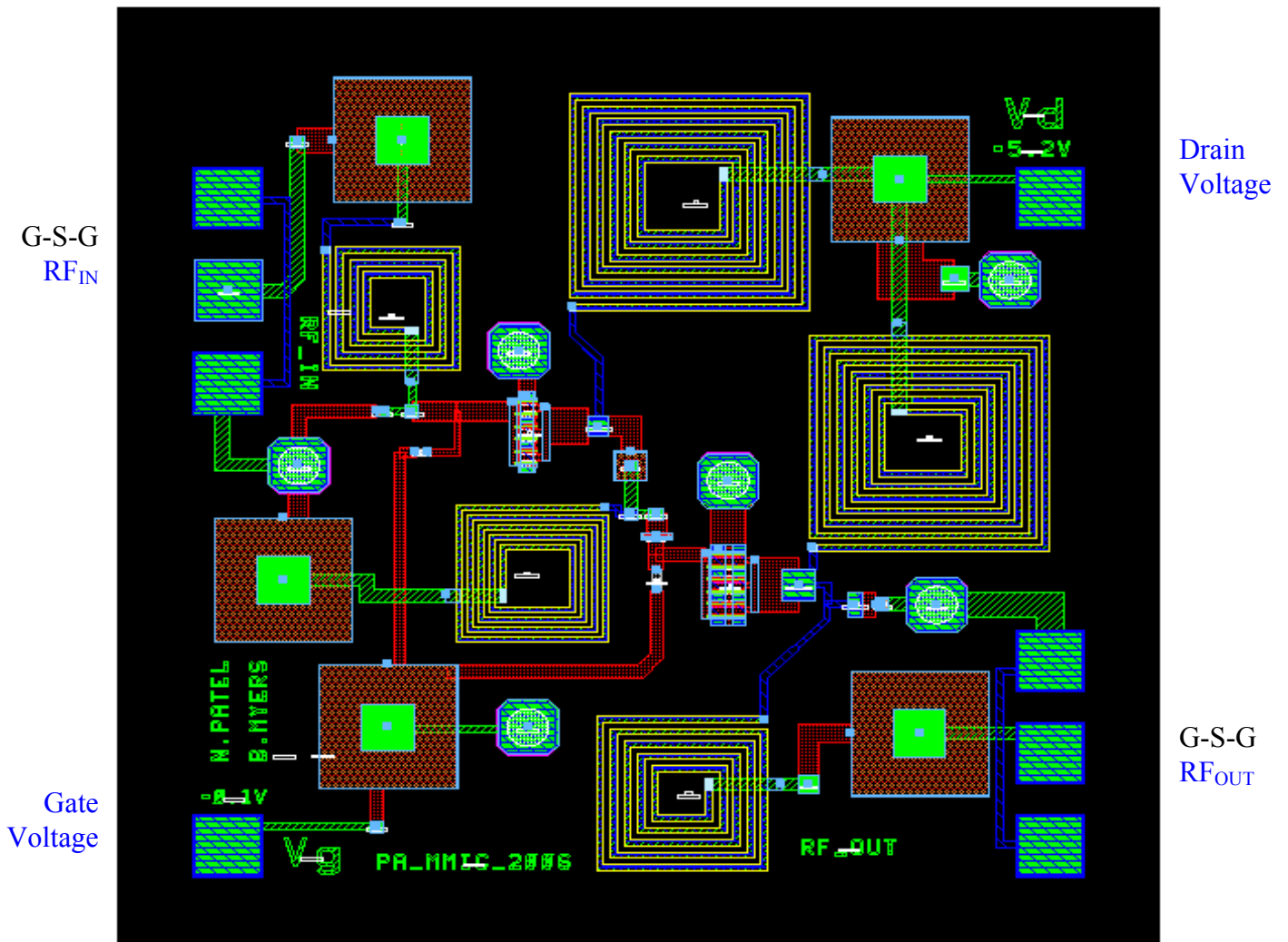


Figure 15. Final Schematic showing DC currents and voltages



**Table 2.0.** *Summary of Performance*

	I <sub>5V</sub> (mA)	V <sub>d</sub> (V)	DC power (mW)	RF <sub>IN</sub> (dBm)	RF <sub>OUT</sub> (dBm)	Gain (dB)	PAE
Stage 1	25.4	5.14	131	-7	5	12	2%
Stage 2	50.6	5	253	5	20.5	15.5	44%
Total	76	5.2	395	-7	20.5	27.5	28%



**Figure 16.** *Layout*

## Test Plan

After MMIC chips are fabricated by Triquint, laboratory testing will begin.

The Ground-Signal-Ground pads for RF<sub>INPUT</sub> and RF<sub>OUTPUT</sub> should be compatible with the test probe leads. We will make our measurements using the Cascade probe station and the HP8510 network analyzer.

DC bias pads are labeled with the appropriate voltages required: +5.2V for drain voltage and -0.1V for gate voltage.

### **Test Equipment**

2 Power Supplies ( $V_{\text{DRAIN}}=5.2\text{V}$ ,  $V_{\text{G}}=-.1\text{V}$ )  
Agilent 8510 Network Analyzer  
Cascade Model 43 wafer probe station  
Spectrum analyzer

### **Test Procedure**

It is safe practice to terminate RF ports before DC power up

Power up device in proper sequence

Calibrate network analyzer to desired range (including 2.3-2.5GHz) using proper calibration standards (SOLT: short, open, load, thru). Note that attenuation may be needed for output port. Network analyzers can be damaged with high power inputs

Measure S-parameters.

Use spectrum analyzer to look at power level of fundamental and harmonics

### **Conclusion**

In summary, we were able to design and lay out on a 60mil x60mil chip, a 2 stage power amplifier with 20.5dBm output power (at 1dB compression) and 28dB gain. Some areas to look out for are process variation shifts. Not a lot of margin is available if one truly needs a minimum of 20dBm output power. However, gain should not be a problem. Also, output match was a significant struggle and neglected in this design since we did not want to stray for an ideal match for maximum power out. To solve some of these troubles, a larger transistor can be used

Other than this, we the power amplifier should work as expected and performance should be solid across the band. The design was shown to be unconditionally stable from .5-5GHz.

There were some lessons learned and things to try out if more time were available. If we had to do this again, here are a few things to look into:

- Create match from load pull and compare performance
- 1st stage was treated more as a gain stage
  - We could have done more of a power match than a match for 50ohms.
  - This would have helped efficiency while maintaining gain requirements
- Improve OMN
  - Reconfigure layout
  - Add more components/matching stages to improve VSWR
- Look at performance variation due to process variation

- Sensitivity of performance on component changes
- Is the design robust?

All in all, we were able to learn a lot in MMIC design and layout and many issues of consideration when laying out a circuit. Also, very useful was the load pull analysis, which is something we would recommend this powerful technique to use in the Power Amplifier homework for future students to take advantage of.

# MMIC VCO Design

Dimitrios Loizos

## Abstract

This report describes the design of a MMIC VCO, meant to operate at a frequency range of 2305 to 2497 MHz, with output power higher than +7dBm, a control voltage between 0 and 0.4V and a single voltage supply of 5V. The design process used was the TQPED, offered from TriQuint and layout and simulations were done using Agilent's ADS package. The report goes through the steps required to design a VCO using the reflection method and presents simulations results that predict operation according to the design specifications. Care has been also taken to keep phase noise low.

Instructors: Dr. Michel Reece  
Mr. John Penn

Dorsey Center  
December 2006

# 1. Introduction

The MMIC VCO has been designed to be part of a duplex transceiver system meant to be used for the S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies. A schematic of the architecture can be found in Fig. 1. More specifically, the design specifications for the VCO require that it operates between 2305 and 2497 MHz. In the transmitter part, the VCO is used to generate the carrier frequency of the transmitted signal, whereas in the receiver part it is used for demodulation. In the transmitter end the VCO drives an I/Q Vector Modulator, whereas in the receiver part an I/Q Vector Demodulator. More details about the architecture of the transceiver can be found in [1].

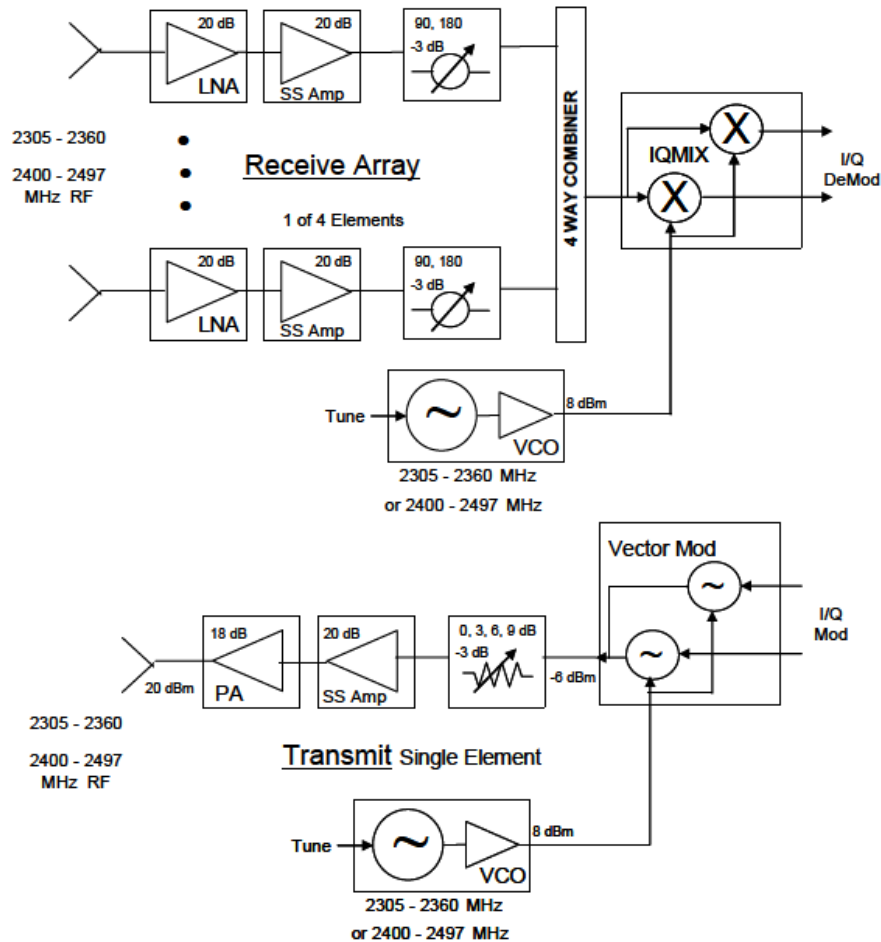


Figure 1. Architecture of the duplex transceiver system operating at WCS and ISM frequencies

Emphasis on this report is given mainly to the steps needed to design the VCO. As will be discussed in the next Section, the first step is the choice of the architecture. Then, a varactor with a widely tunable capacitance and a fairly small parasitic resistance is needed to achieve a wide frequency tuning range without deteriorating the quality factor of the resonator, parallel to which it is attached. The choice of the resonator is probably the most important part in the VCO, since it is the network that will determine the phase noise of the oscillator. Appropriate biasing is then needed to achieve the desired output power. Finally, a good output matching network is needed to provide an interface with next stages that will guarantee oscillation.

## 2. Design approach

Several architectures exist for designing VCOs. Based on the application and the specifications of the specific MMIC VCO, the Colpitts architecture was chosen, because of its simple design and fairly good characteristics. Moreover, the use of only one transistor in the topology was appealing in keeping the phase noise low. The Colpitts topology can be seen in Fig. 2, with two possible configurations: one with the feedback from source to gate, and the other with feedback from drain to source. Either topology can be used, however notice that the feedback needs to be positive, i.e., feedback from drain to gate will not lead to oscillations.

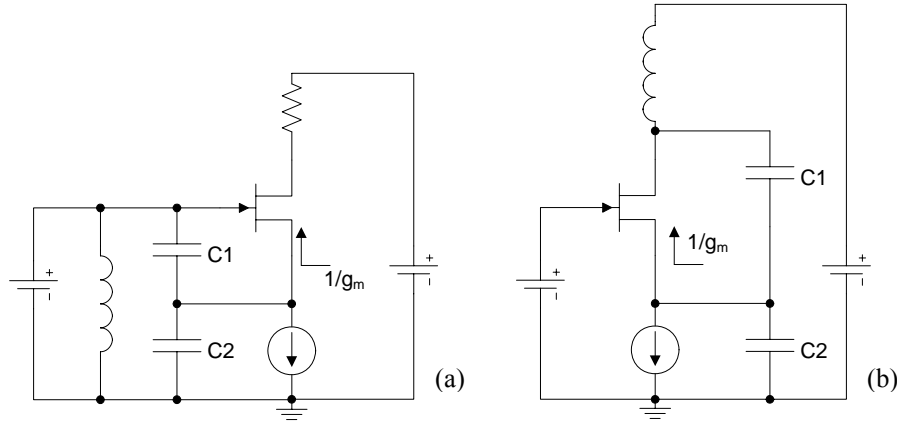


Figure 2. Basic Colpitts configurations

The FET effectively decouples the resonator from the load. In the case of feedback from source to gate the output has to be taken at the drain, whereas for drain-source feedback, the load should be connected at the gate. Since a specification of the design was to maximize the output power, the load had to be connected to the drain, and this is why the topology of Fig. 2(a) was chosen.

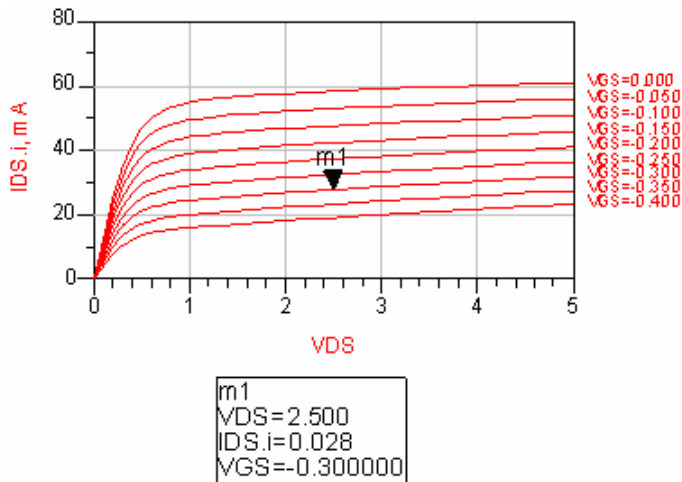


Fig.3 FET biasing

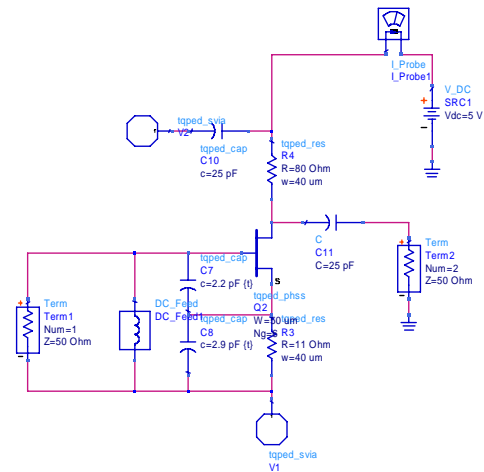


Fig. 4. Basic Colpitts topology

A D-mode pHEMT was used for the design, so as to simplify biasing; just a resistor parallel to C2 suffices. If an E-mode pHEMT were to be used, either a second voltage source would be

needed, or a resistive divider at the gate had to be incorporated, increasing noise in the architecture. In order to maximize the output power while keeping noise low, the FET was chosen to operate at  $I_{DSS}/2$  and a  $V_{DS}$  of 2.5 (half that of the voltage supply). In order to find the value of the resistor that had to be connected parallel to  $C_2$ , a dc analysis of the FET was performed, providing the  $I_{DS}$  vs  $V_{DS}$  curves of the device. As shown in Fig. 3,  $I_{DSS}$  is around 56mA ( $V_{GS}=0$ ), and for  $I_{DSS}/2$  and  $V_{DS}=2.5V$ , a  $V_{GS}$  of -0.3V is required. In order to achieve a  $V_{DS}$  of 2.5V, an extra resistor was connected at the drain, providing the appropriate voltage drop. A schematic with the basic topology and the two biasing resistors can be seen in Fig. 4.

The inductor has not been yet added to the design and the 0V dc voltage at the gate is provided through a dc feed element. The first step in building the oscillator will be to maximize instability of the design. A figure of instability, as described in [2], is the farthest point of the output mapping circle, called MaxMP2, which is equal to  $\mu'$ , the load stability factor. The output mapping circle basically shows the maximum degree of instability in the circuit, assuming that an appropriate load (the load that maximizes instability) has been connected to the input port. Therefore, the first step in the design is to tune capacitors  $C_1$  and  $C_2$ , so as to achieve a maximum value at the output mapping circle, for the center frequency of 2.4GHz. The initial values of these capacitors were chosen such as to provide oscillations at 2.4GHz when connected to an inductor of value around 3-4nH. Note also that the equivalent capacitance connected to the inductor is the series combination of  $C_1$  and  $C_2$ .

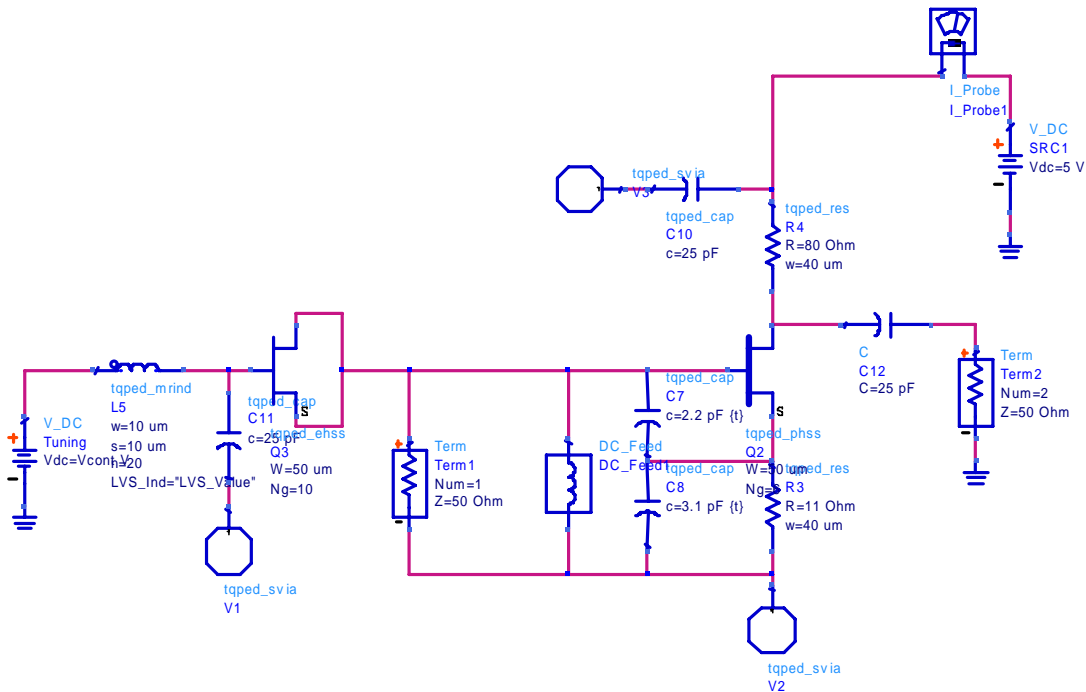


Fig. 5. Schematic with the varactor added

Next step was to add the varactor to the design, as shown in Fig. 5. The varactor had to be implemented on chip and therefore a diode connected pHEMT, reversely biased was used. As known, diodes operate as variable capacitors when reversely biased. The capacitance is nonlinearly controlled by the bias voltage. Objective here was to find an appropriate device that would have a small capacitance so that the final oscillation frequency does not divert considerably for the center frequency of 2.4GHz, but also with as low as possible losses. Ideally, the tuning voltage range has to be large, so that a small variation in the voltage does not result to

a big variation in capacitance. Several devices were simulated, however, the one with the better response was found to be the E-mode pHEMT with 10 fingers of 50 $\mu$ m each (Fig. 6). The response of this device is shown in Fig. 7 for a frequency range of 0.5 to 2.4GHz and for a bias of 0V, along with the response of its equivalent model, that of an RC network. As can be seen from Fig. 6, the losses are fairly small. Simulations at different voltage biases (up to -1V) demonstrated even smaller losses.

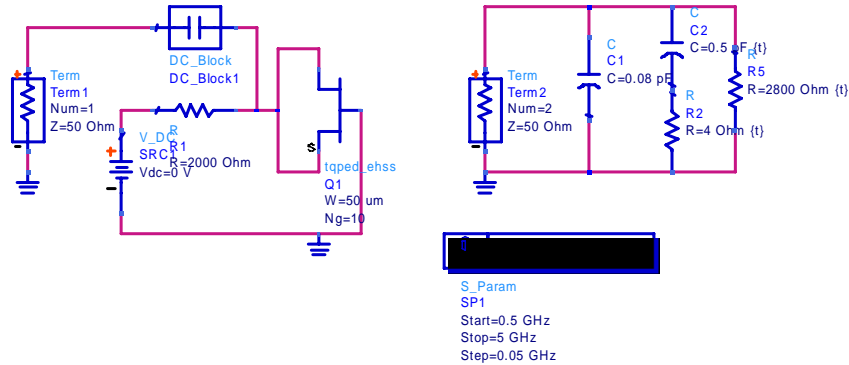


Fig. 6. E-mode varactor and equivalent model

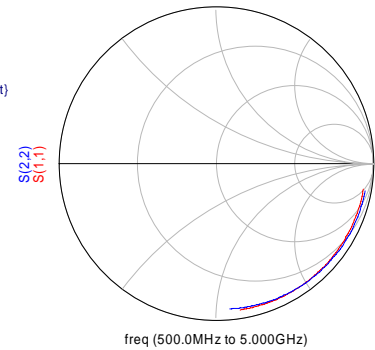


Fig. 7. Varactor frequency response

The varactor was placed parallel to the C1-C2 network and tuning of C1-C2 was done so as to achieve a maximum value for MaxMP2. The bias of the varactor was set at 0.24V (note that the varactor has been connected in a way inverse to that of Fig. 6 and that is why positive voltages are used), which was the bias at which we would like to have our center frequency. It should also be noted that the bias voltage at the gate of the varactor was applied through a big inductor instead of a resistor. This was done so as to reduce the noise introduced by the bias feed network.

Then, the inductor was added to the design in place of the dc feed (Fig. 8). The choice of the type of resonator is very important when designing a VCO, since it is the main part that affects phase noise [3-5]. Crystals and ceramic resonators have excellent phase noise; however these are devices that need to be added externally to the MMIC and therefore could not be used. For on chip implementation, two basic topologies were considered. One was the only-C network, basically a gyrator with a capacitance on one end, seen as an inductance on the other end, and connected in parallel to a capacitor, and the simple LC tank. The only-C network although smaller in size and very common in CMOS design, has the drawback of high phase noise. This is the main reason that the simple LC tank was finally implemented.

The topology was simulated as a one port element, and tuning of the C1-C2 capacitors and the inductor was performed so as to achieve the highest S11 at a frequency of 2.4GHz. Assuming a purely resistive load at the drain, we would like S11 to be purely real. This can be done by adding an output matching network at the drain that will rotate S11 to a real value. In general, oscillations will start at the point where the imaginary parts of the drain impedance and the load impedance are opposite and the real part of the negative drain impedance is absolutely greater than that of the real part of the load impedance. For our design, we chose not to add the extra matching network, knowing that oscillations will start at a frequency slightly different than where S11 has its maximum value.

Having designed the resonator part of the oscillator, we have to consider the values of its negative impedance and determine the output matching network so as to guarantee that when a 50 $\Omega$  load is connected, oscillations will start and will be sustained. The output matching network was the equivalent T of a  $\lambda/4$  transmission line, that would transform the 50 $\Omega$  load to a lower



impedance at the drain of the FET. Usually, the negative resistance needs to be at least 3 times larger than that of the load. For this case the matching network shown in Fig. 9 was employed and tuning of the L and C values was done until the condition for oscillation was met.

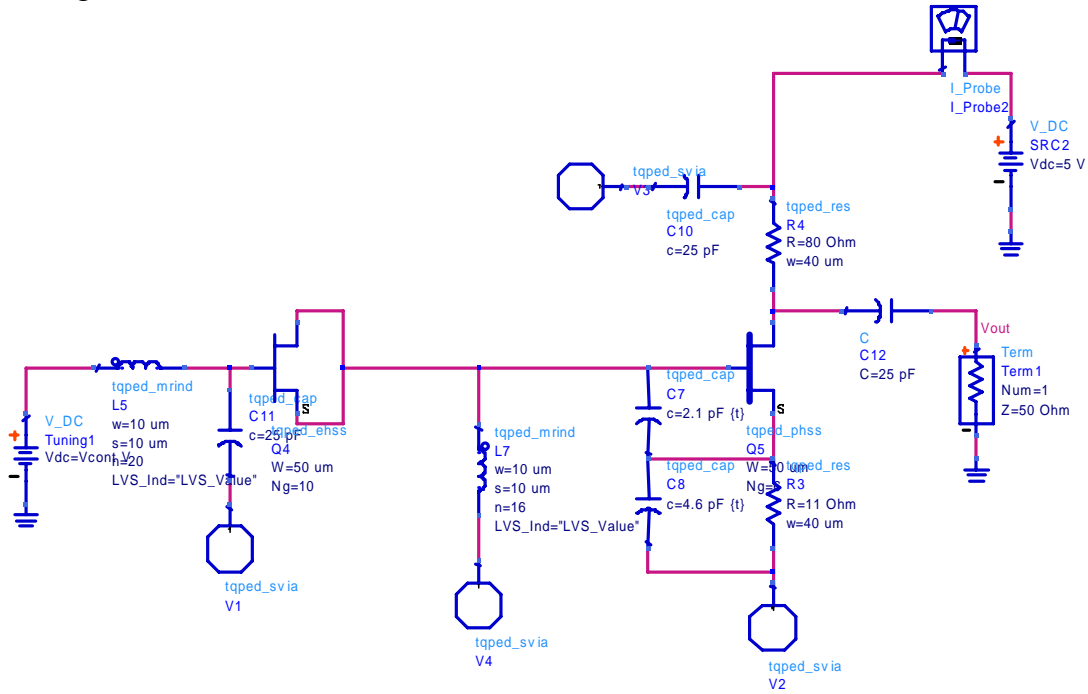


Fig. 8. Topology with the dc feed replaced by an inductor

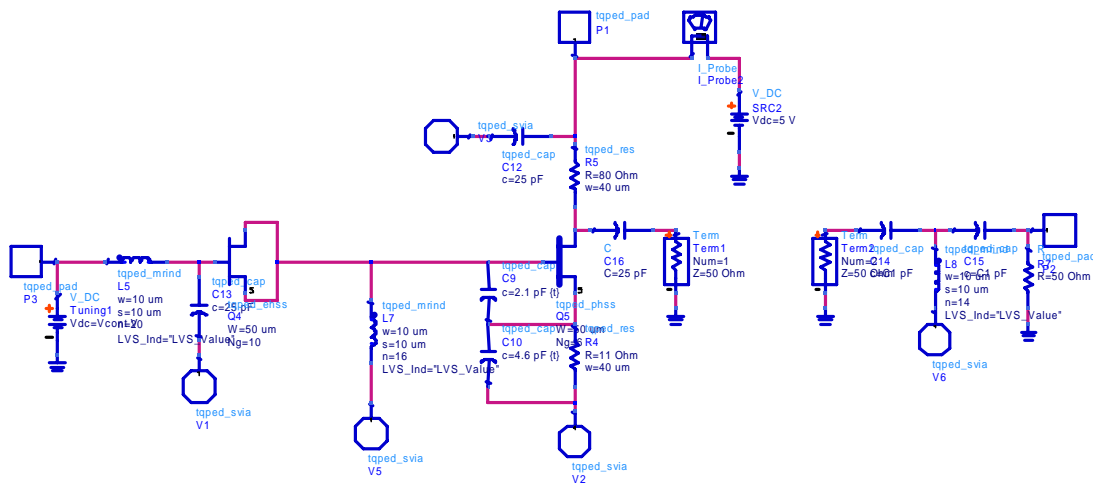


Fig. 9. Topology with output matching network

### 3. Simulation Results

Simulation results from several steps of the VCO design, as well as of the whole topology are provided in this section. Maximization of the output mapping circle for the frequency of 2.4GHz is shown in Fig. 10, after appropriate tuning of the values of capacitors C1 and C2, for the schematic of Fig. 5. Fig. 11 shows maximization of the value of S11 after adding the inductor to the design (Fig. 8).

In order to check that oscillations will start, at several frequencies, the schematic of Fig. 9 was simulated for different values of the biasing voltage of the varactor. Using the notation of Fig. 9 for the numbering of the ports, the objective here was that for the frequencies where  $\text{imag}(Z_1+Z_2)=0$ ,  $\text{real}(Z_1+Z_2)$  had to be negative. This means that at the frequencies where the reactive part of the impedance of the load is cancelled from the impedance of the FET network, the overall resistance is negative and voltage starts to build up.

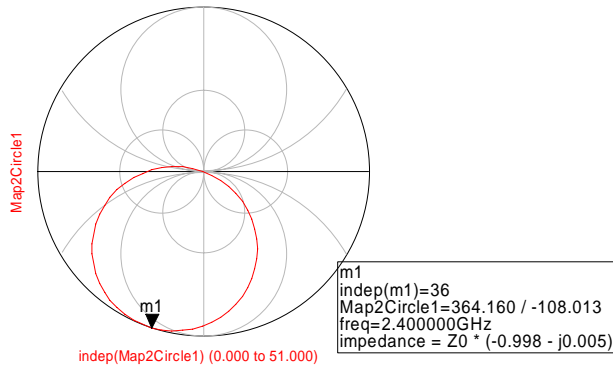


Fig. 10. Maximizing MaxMP2

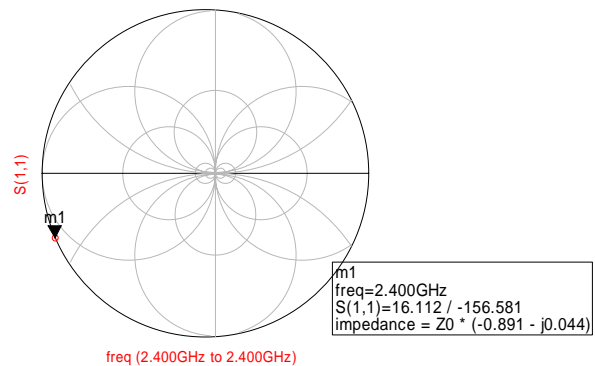


Fig. 11. Maximizing output reflection coefficient

Fig. 12(a) shows simulation results for a varactor biasing voltage of 0.28V. The sum of the imaginary parts is 0 close to 2.4GHz and at that frequency the sum of the real parts is negative; therefore, oscillations will start and will be sustained close to that frequency. Fig. 12(b) depicts simulation results for the case of a varactor biasing voltage of 0.4V and indicates that simulations will start around 2.24GHz. Finally, Fig. 12(c) corresponds to a biasing voltage of 0V and indicates oscillations around 2.56GHz. Note that in all these plots, the sum of the imaginary parts becomes zero only at one point in the range between 0.5 and 5GHz. In Fig. 12(c), the sum of the imaginary parts is very close to 0 also at 1.8GHz. However, even if it crossed the 0 point, oscillations would not start since the sum of the real parts at that point is positive.

Simulations, so far, have been performed using the nonlinear simulator built-in ADS. Another set of simulations was performed using the Harmonic Balance Simulator of ADS. The concept in that simulator is slightly different than the non-linear one. Here, oscillation at an unknown frequency  $\omega$  is assumed and the nonlinear parts of the design are represented by their describing functions [6]. An *osc-port* element is introduced at some point of the closed loop and the solver finds the point at which the total phase of the loop is  $360^\circ$  and checks if the gain is positive. If it's not, then no oscillations are sustained; if it is, then we have oscillations and the solver can provide estimates of the output power, harmonics, output waveforms, phase noise and other desired values.

An interesting point when using the Harmonic Balance solver is that the result for the oscillating frequency was different than that gotten from the nonlinear simulator. This can be due to several reasons. The first and probably the most possible is that the nonlinear simulator finds the frequency at which oscillations will start. However, the actual frequency where oscillations will be sustained is slightly different. The second reason is that in harmonic balance simulation there are several assumptions made in order to derive the describing functions, and this might hide phenomena that the nonlinear simulator is taking into account. Testing of the actual MMIC might help reveal which approach is more correct.

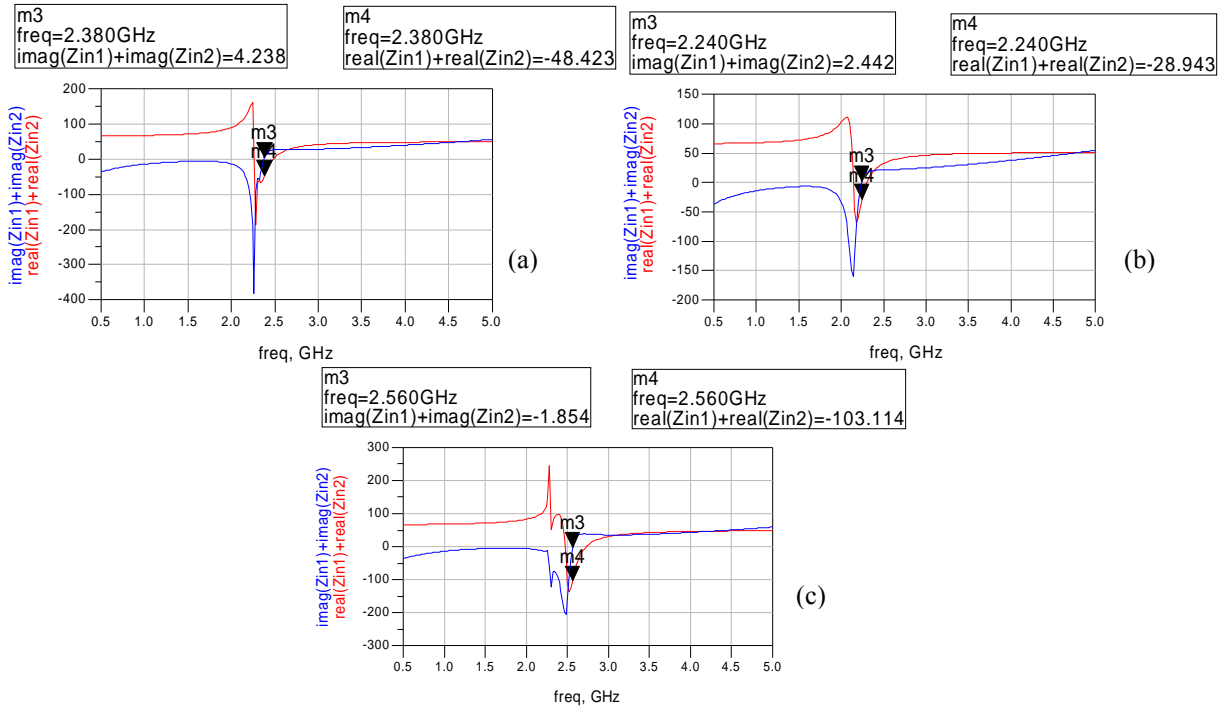


Fig. 12. Simulation results using the nonlinear solver for varactor biasing voltages of (a) 0.28V, (b) 0.4V and (c) 0V

Fig. 13(a)-(c) depicts simulation results using the harmonic balance simulator. Frequencies are shifted down by 200MHz compared to the non-linear simulator. Output power is always greater than 7dBm and for several biases greater than even 10dBm. Phase noise is also good, being less than -110dBc at 1MHz for all oscillating frequencies.

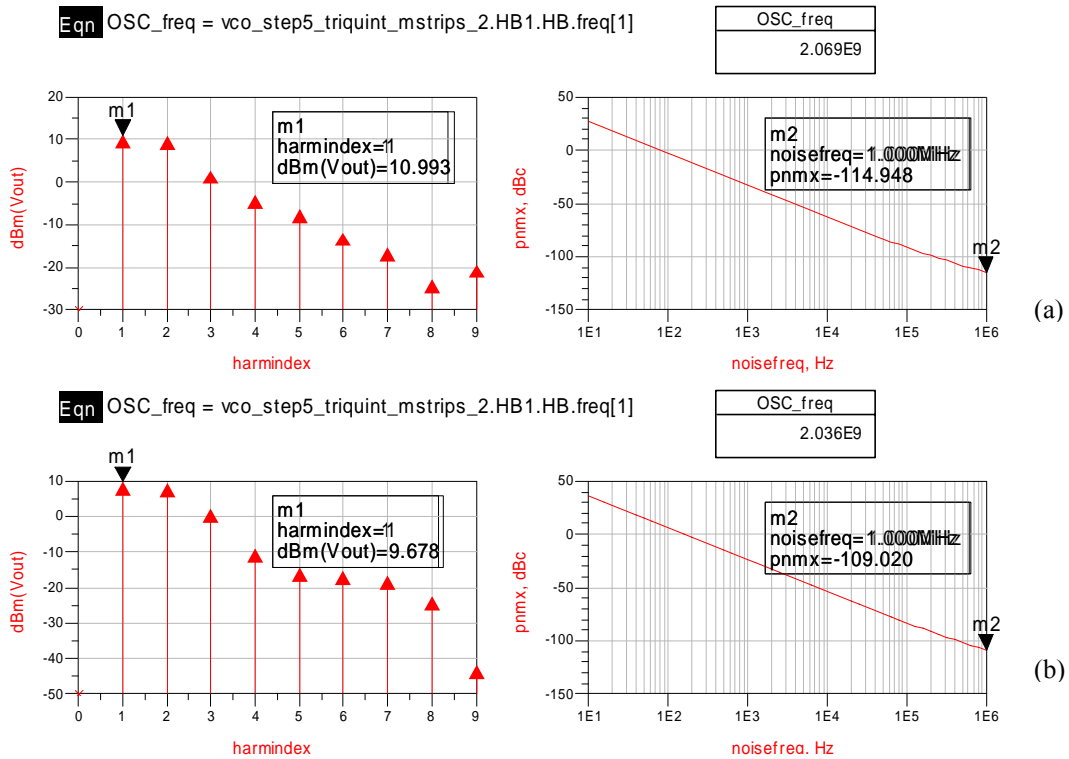


Fig. 13. Simulation results using the harmonic balance solver for varactor biasing voltages of (a) 0.28V and (b) 0.4V

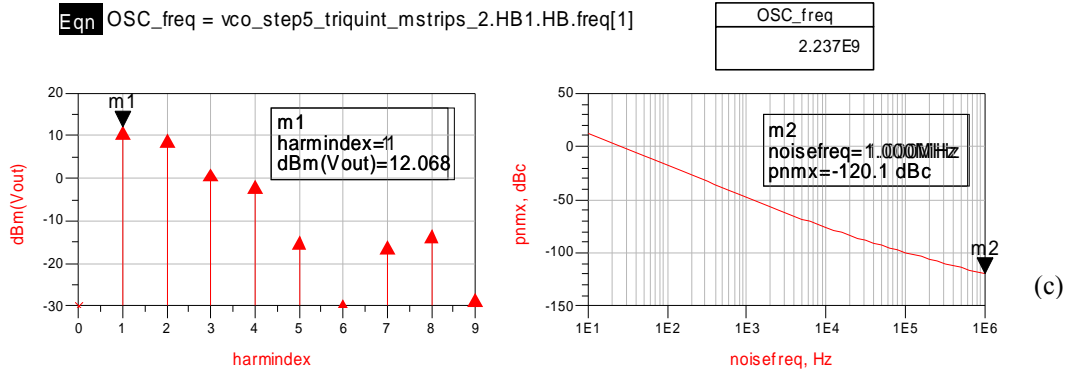


Fig. 13. Simulation results using the harmonic balance solver for varactor biasing voltage of (c) 0V

#### 4. Schematic and Layout

The total schematic, without the  $\tau$ lines representing the interconnects, is shown in Fig. 14. The dc solution has been annotated.

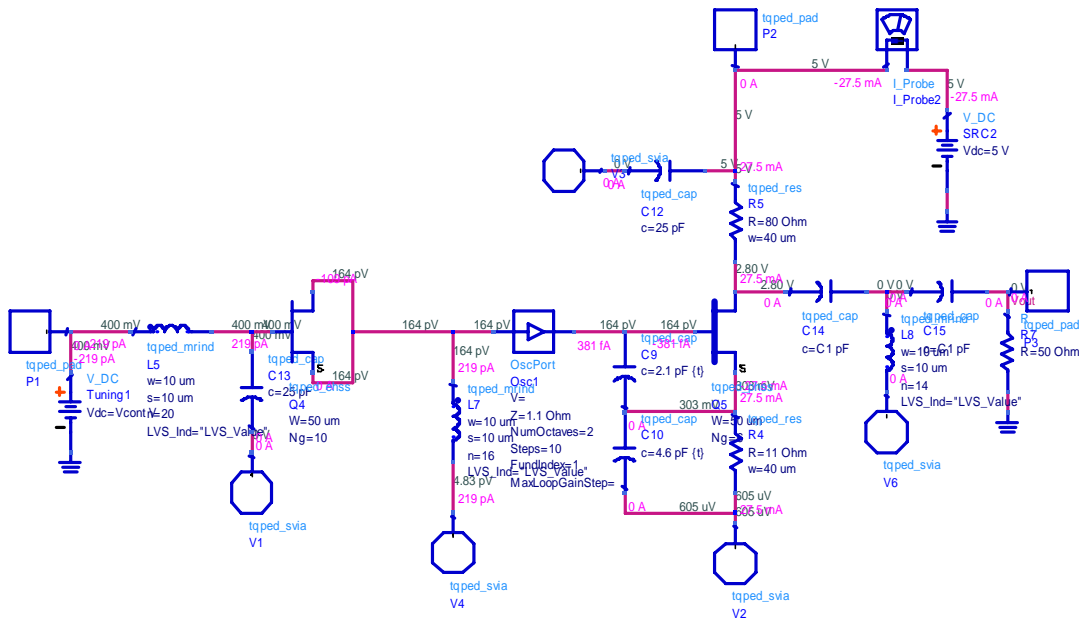


Fig. 14. Overall schematic

The layout of the circuit is shown in Fig. 15. DRC and LVS checks were performed and passed.

#### 5. Test Plan

For testing, 2 DC probes and 1 RF probe are needed. Place a DC probe to the terminal labeled “+5V” and apply 5V of voltage. Place a second DC probe to the terminal labeled “Vtune”, and apply a voltage ranging from 0V to 0.4V. Connect an RF probe (GSG) to the terminal labeled “out” (output of the oscillator) and measure the signal on a Spectrum Analyzer. Once the center frequency has been found, limit the span to 5-10MHz and measure the power at



## 6. Conclusion

A MMIC VCO has been designed using the reflection method. The steps towards designing the VCO have been outlined starting from the architecture, then the choice of the resonator and varactor and finally the output matching network. Simulations have been performed both with the nonlinear simulator and the harmonic balance one. Differences in the results have been found and possible reasons for that have been provided. The final schematic and layout have been demonstrated as well as a plan for future testing. Testing will be critical in determining the actual oscillation frequency as well as output power and noise figure, and check the how well these figures compare to the simulation results.

## References

- [1] M. Reece, J. Penn, "MMIC Design EE 525.787 Fall 2006 Student Projects", Part time Engineering Program for Professionals, The Johns Hopkins University, 2006.
- [2] M. L. Edwards, S. Cheng, "Gee-Cad Tutorials: Voltage Controlled Oscillator (VCO)".
- [3] U. L. Rohde, A. K. Poddar, G. Bock, "The Design of Modern Microwave Oscillators for Wireless Applications Theory and Optimization", J. Wiley & Sons, June 2005.
- [4] B. Razavi, "RF Microelectronics", Prentice Hall, 1997.
- [5] T. H. Lee, "Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits", Cambridge University Press, 2004.
- [6] H. Khalil, "Nonlinear Systems", Prentice Hall, 2001.

# **2.4 GHz MMIC LNA Design Project**

**Designer: David C. Sokol**  
**Date: December 3, 2006**

## **1 Abstract**

This report describes the design of a 2.4 GHz monolithic microwave integrated circuit (MMIC) low noise amplifier (LNA). This amplifier is the first stage of a receive array for the S-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies.

## **2 Goals**

The purpose of this project was to design a 2.4 GHz MMIC LNA based on the following performance criteria:

Center Frequency: 2.4 GHz

Noise Figure: 2dB

Gain: 20dB

DC Voltage Supply: single +5V

VSWR: <1.5:1 input and output (-14dB)

Input IP3: >+5dBm

The layout must also fit on a TriQuint 60 mil by 60 mil die with a substrate thickness of 100 microns. The circuit must be designed and simulated using the ADS with the TriQuint TQPED component library.

## **3 Specifications**

The circuit, as designed, will operate with the following specifications:

Center Frequency: 2.4 GHz

Noise Figure: 1.868dB

Gain: 25.9dB

DC Voltage Supply: single +5V

VSWR: better than -17dB

Input IP3: >+5dBm

## **4 Tradeoffs**

Gain and stability are traditionally the tradeoffs in any microwave amplifier design. Also, the noise figure may be increased, depending on the DC resistance configured at the input for DC biasing.

## **5 Design Approach**

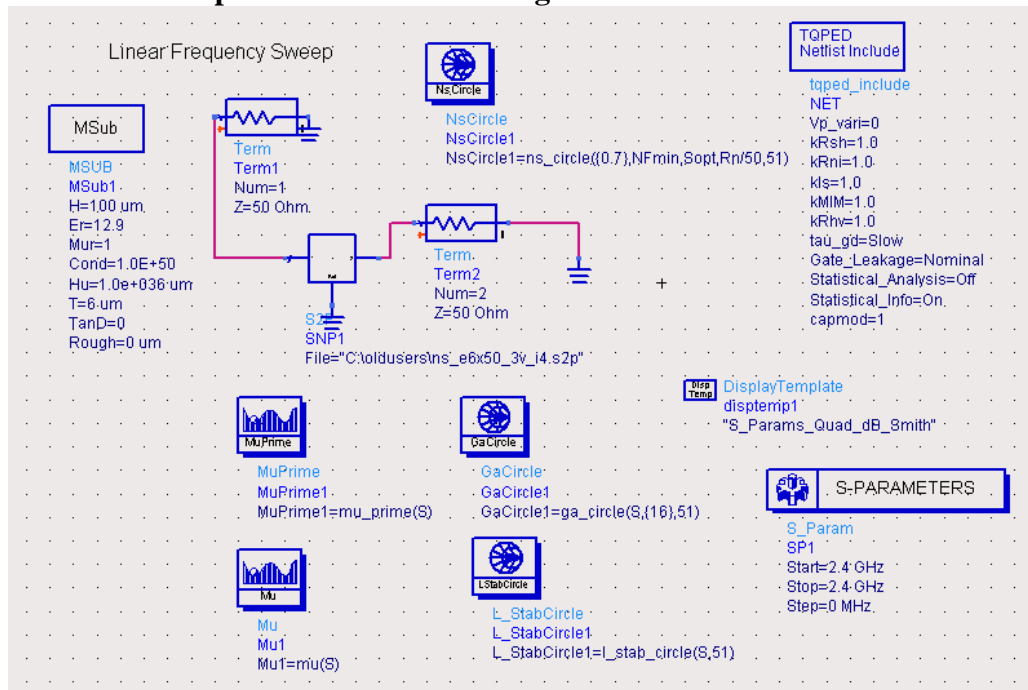
The E-mode (EHSS) FET topology was chosen because of the single, positive voltage design criterion. The D-mode FET topology, which is the only other choice, would have required both a positive and negative voltage supply. The E-mode FET topology was also



chosen due to the lower noise figure and higher gain when biased under comparable conditions, as compared to the D-mode FET topology.

The primary parameter of interest is achieving a low noise figure and, secondarily, a high gain. The following graphic (Figure 1) illustrates the circuit used to determine the appropriate input matching reflection,  $S_{11}$ , to attain these amplifier characteristics:

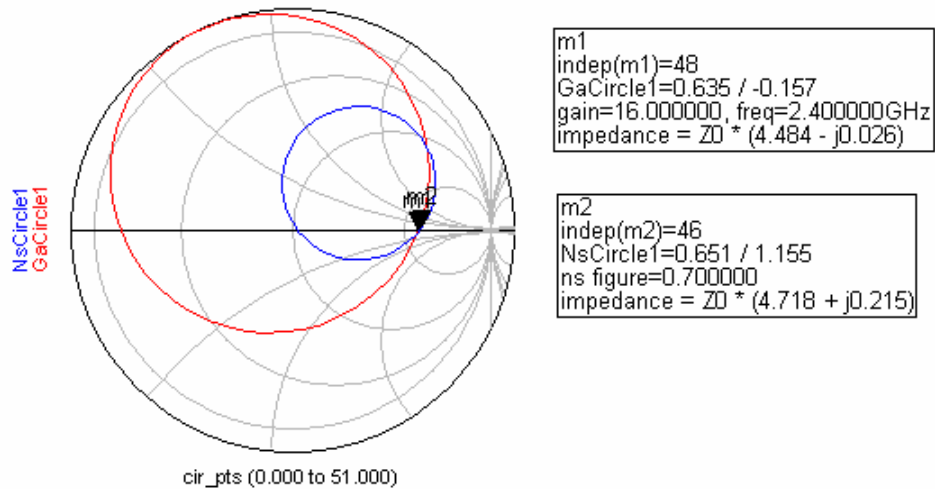
**FIGURE 1 – Optimum Gain / Noise Figure Simulation Circuit**



The following graphic (Figure 2) illustrates the results of the noise figure/gain simulation:

**FIGURE 2 – Optimum Gain / Noise Figure Circles**

Gain and Noise Figure Circles - Emode FET - Single Stage

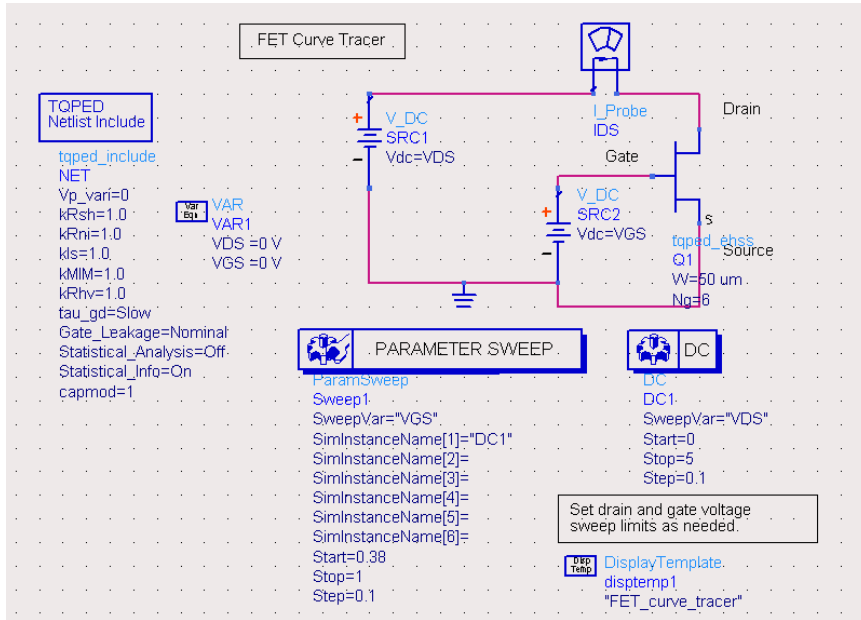


The optimum trade-off between low noise figure and gain occurs when the input matching circuit matches the impedance near the two markers listed above. It is shown that we will expect a gain of 16 dB or 39.8 and a noise figure of 0.65 dB or 1.16 for a single stage implementation. In cascade, the theoretical gain and gain of the cascade of two identical stages would be 32 dB and  $1.16 + [(1.16 - 1) / (39.8)] = 0.66$  dB. The replacement of ideal components with real components will increase the noise figure of the circuit.

Clearly the design goals will not be met for the gain criterion with a single stage. Therefore, a two-stage design will be designed and implemented.

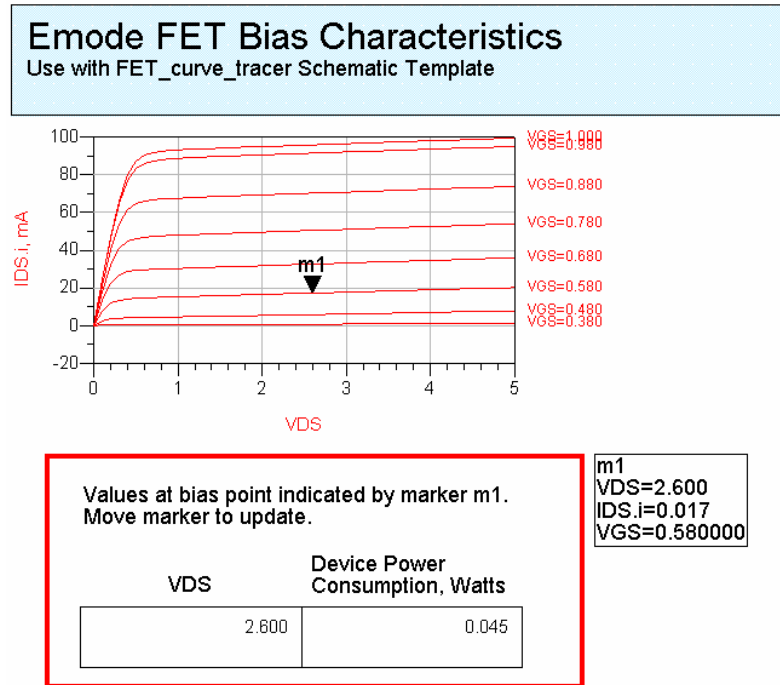
The IV curves for the E-mode FET were simulated using ADS. These curves gave insight into the current and voltage swings typical of these FETs usage in an amplification scenario. The following graphic (Figure 3) illustrates the ADS circuit used to test the FET's IV mode characteristics:

**FIGURE 3 – E-mode FET IV Curves Schematic**



The following graphic (Figure 4) illustrates the results of the IV simulation:

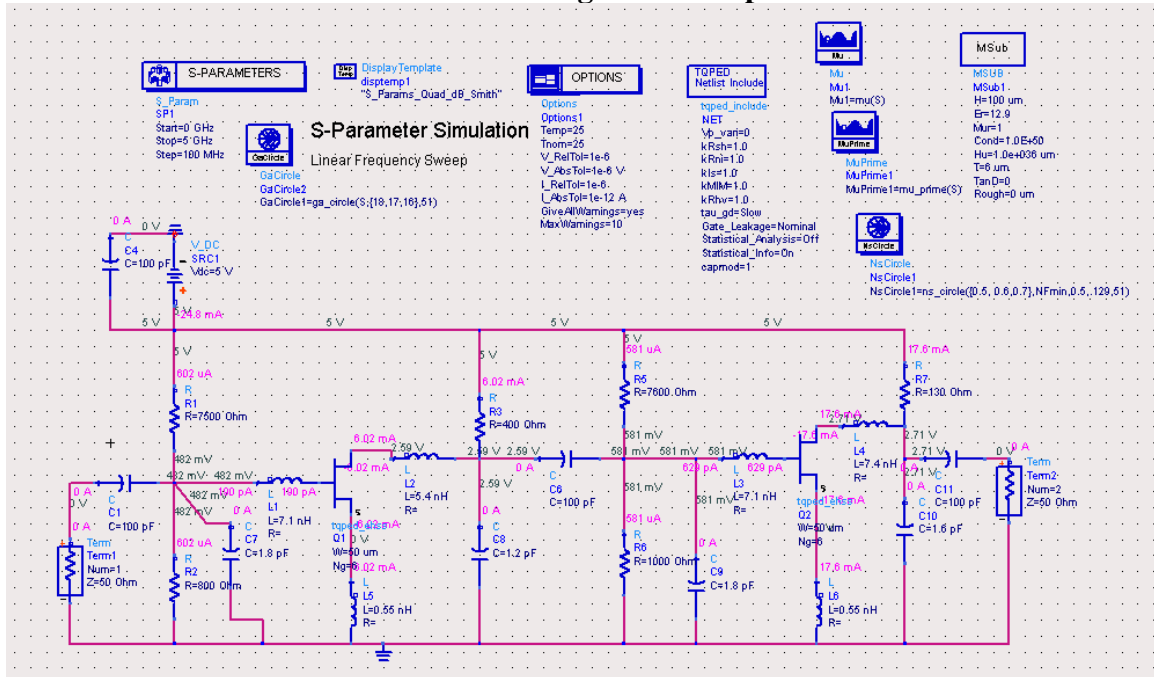
**FIGURE 4 – E-mode FET IV Curves**



These results show that a drain-to-source voltage (VDS) of 2.6V with a gate-to-source voltage of 0.58V would be a good choice to allow the FET to operate in the saturation region – a necessary condition for amplification. Typical drain-to-source currents would be around 0.017 A at the operating point. These values allow the DC characteristics of the LNA to be known for design purposes.

With an understanding of the input matching characteristics of the LNA design and the DC voltage characteristics needed to operate the amplifier, a two-stage design was implemented. The following graphic (Figure 5) illustrates the two-stage design:

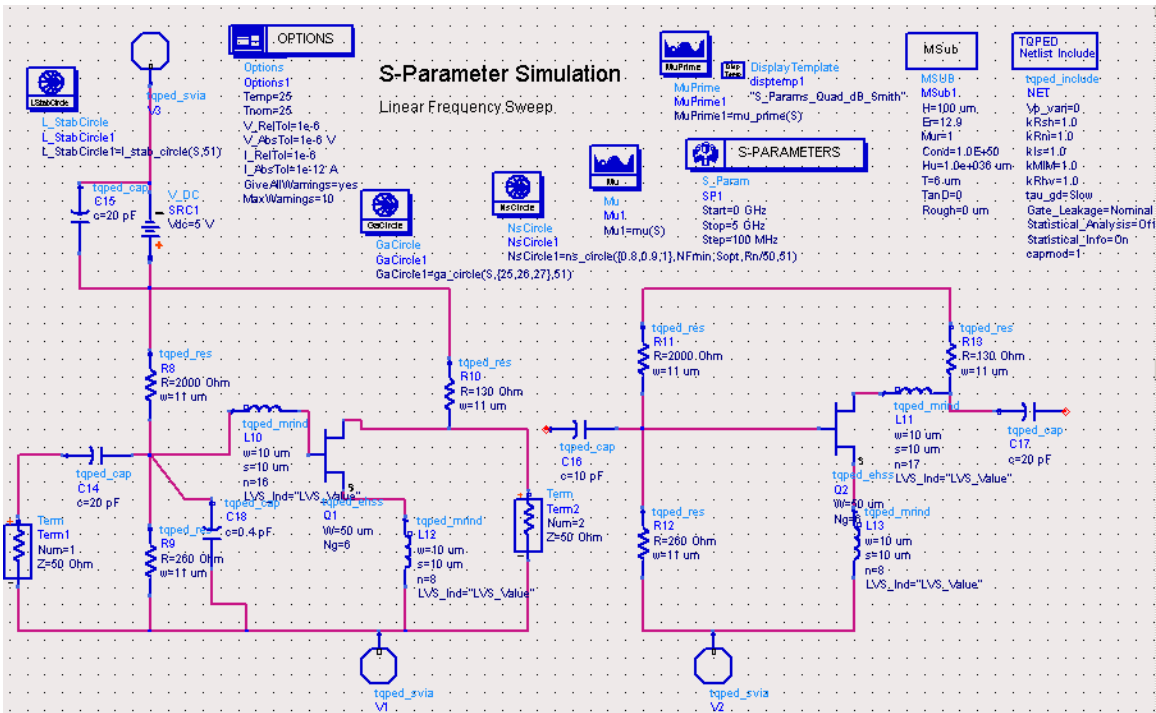
**FIGURE 5 – MMIC LNA Schematic Using Ideal Components**



The EHSS (E-mode) FETs employed in the circuit are the standard  $300\ \mu\text{m}$  ( $6 \times 50\ \mu\text{m}$ ) package. A  $100\ \text{pF}$  capacitor was used to isolate DC between the two stages. An output matching circuit was also designed to match the conjugate of the output reflection coefficient for each stage. With further analysis, the output matching network of the input stage, the input matching network of the output stage and the  $100\ \text{pF}$  blocking capacitor were replaced with a single  $20\ \text{pF}$  blocking capacitor to reduce the complexity of the circuit.

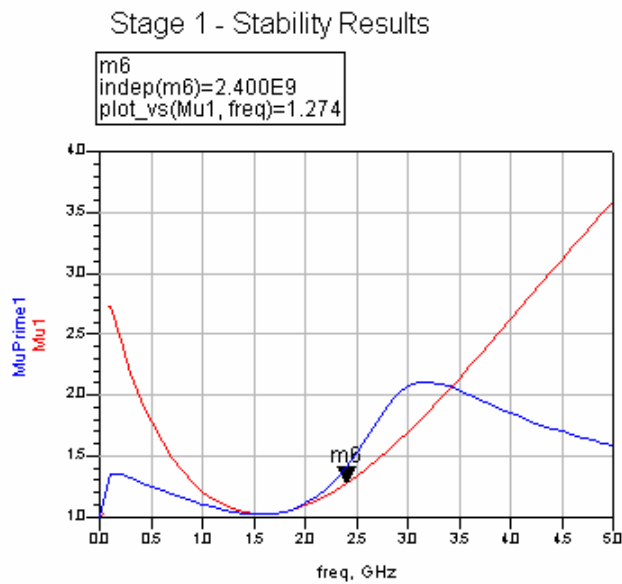
The source inductors connected to both sources were replaced with TriQuint spiral inductors and tuned such that unconditional stability was insured for each individual stage. Therefore, the cascade of the two stages would be unconditionally stable. The following graphic (Figure 6) illustrates the test circuit:

**FIGURE 6 – Input Stage Stability Schematic**



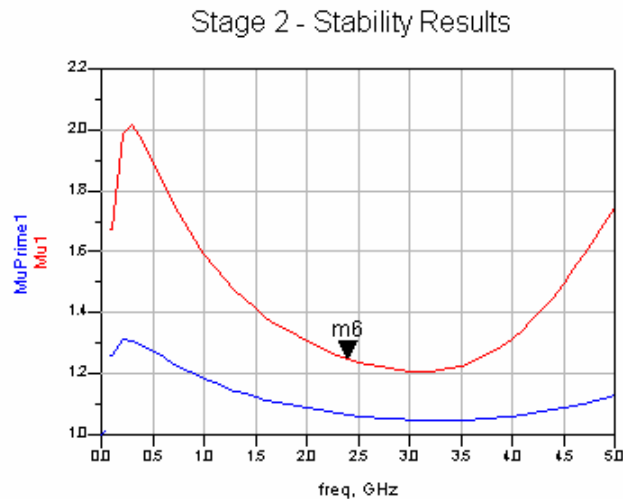
Note that the second stage has been disconnected and the 50 ohm termination placed at the output of the first stage. The following graphic (Figure 7) illustrates the results when a 100 x 100 micron, 8-loop spiral inductor was used as the source inductor:

**FIGURE 7 – Input Stage Stability Simulation Results**



The input stage circuitry is therefore shown to be unconditionally stable when using this source inductor. The same inductor was used for a stability analysis of the second stage. The following graphic (Figure 8) illustrates the results:

**FIGURE 8 – Output Stage Stability Simulation Results**

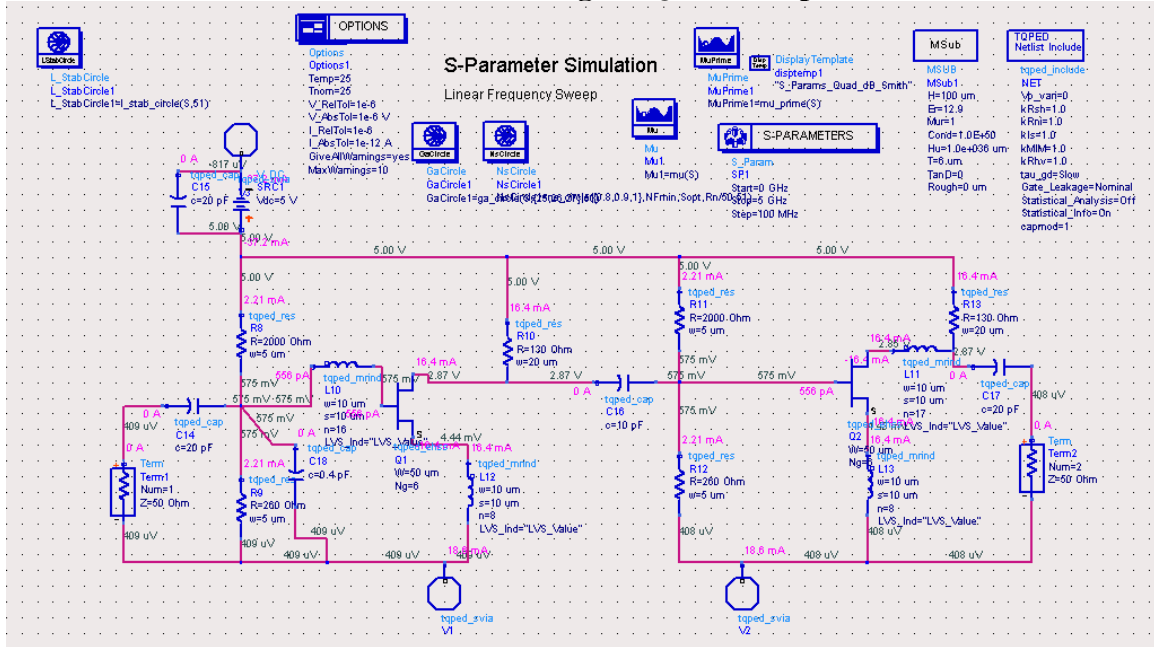


The output stage circuitry is also shown to be unconditionally stable with the 100 x 100, 8-turn spiral inductor connected at the source of the FET.

While the resistor divider networks at the input of each stage produced a minimal noise figure of 1.6 dB overall, an initial layout of the circuit showed that the 7800 Ohm resistors would cause placement of the other components to be difficult. The 7800 and 800 ohm resistors were replaced with 2000 and 260 ohm resistors at the input. This can be seen in the previous single-stage stability simulations. Also note that the drain resistor was reduced from 400 ohms to 130 ohms to maintain the DC current through the drains, as noted in the IV curves.

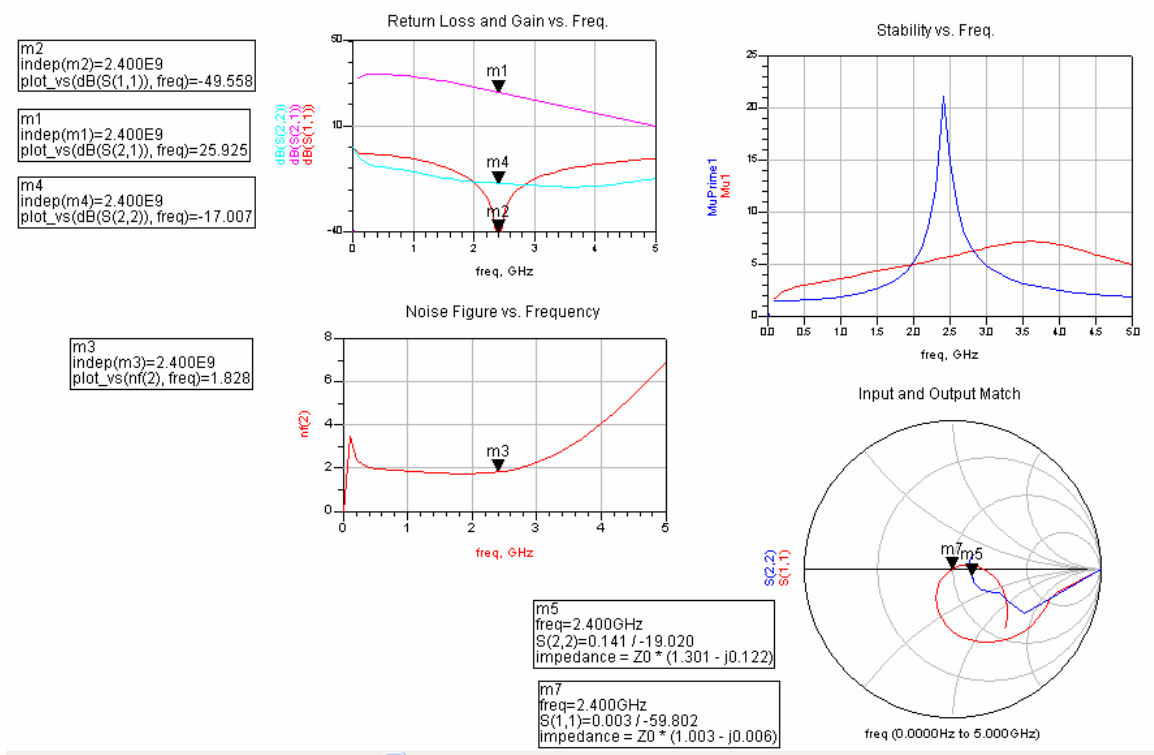
The next graphic (Figure 9) shows the final two-stage LNA circuit with the previous enhancements implemented:

**FIGURE 9 – MMIC LNA Schematic Using TriQuint Components**



To conserve space, the blocking capacitors were reduced to 20pF and the inter-stage matching capacitor was also reduced to 10pF. The shunt capacitor was reduced to 0.4pF for input matching purposes. The following graphic (Figure 10) illustrates the return loss (S11 and S22), gain (S21), stability, noise figure and input/output match:

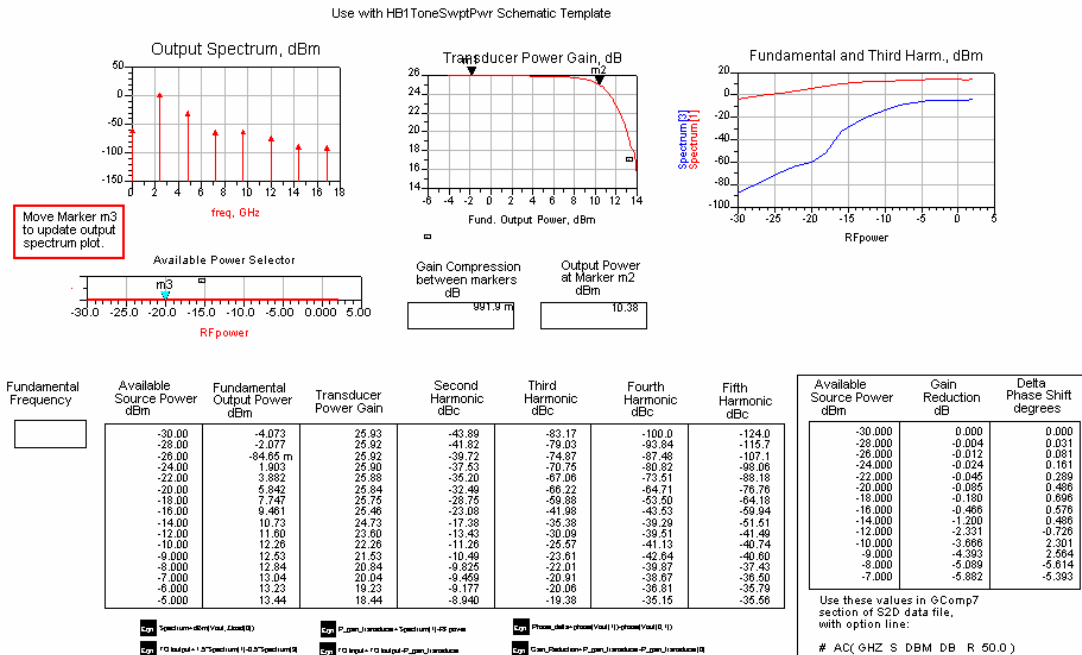
**FIGURE 10 – MMIC LNA Simulated Return Loss, Gain, Noise Figure and Stability**



It can be seen that with real TriQuint components used, the previous circuit will meet both the noise figure (1.828 dB) and gain (25.9 dB) requirements of the project. The circuit will also have an input VSWR of -49.6 dB and an output VSWR of -17 dB. The optimal input VSWR was obtained by adjusting the shunt capacitor size at the input. It is also shown that the circuit will also be unconditionally stable across the frequency band from 2 to 3 GHz.

The input power of the LNA circuit was swept from -30 to 2 dBm while the output was terminated with a 50 ohm resistance. The following graphic (Figure 11) illustrates the results of the sweep:

**FIGURE 11 – Swept Power Response of MMIC LNA**

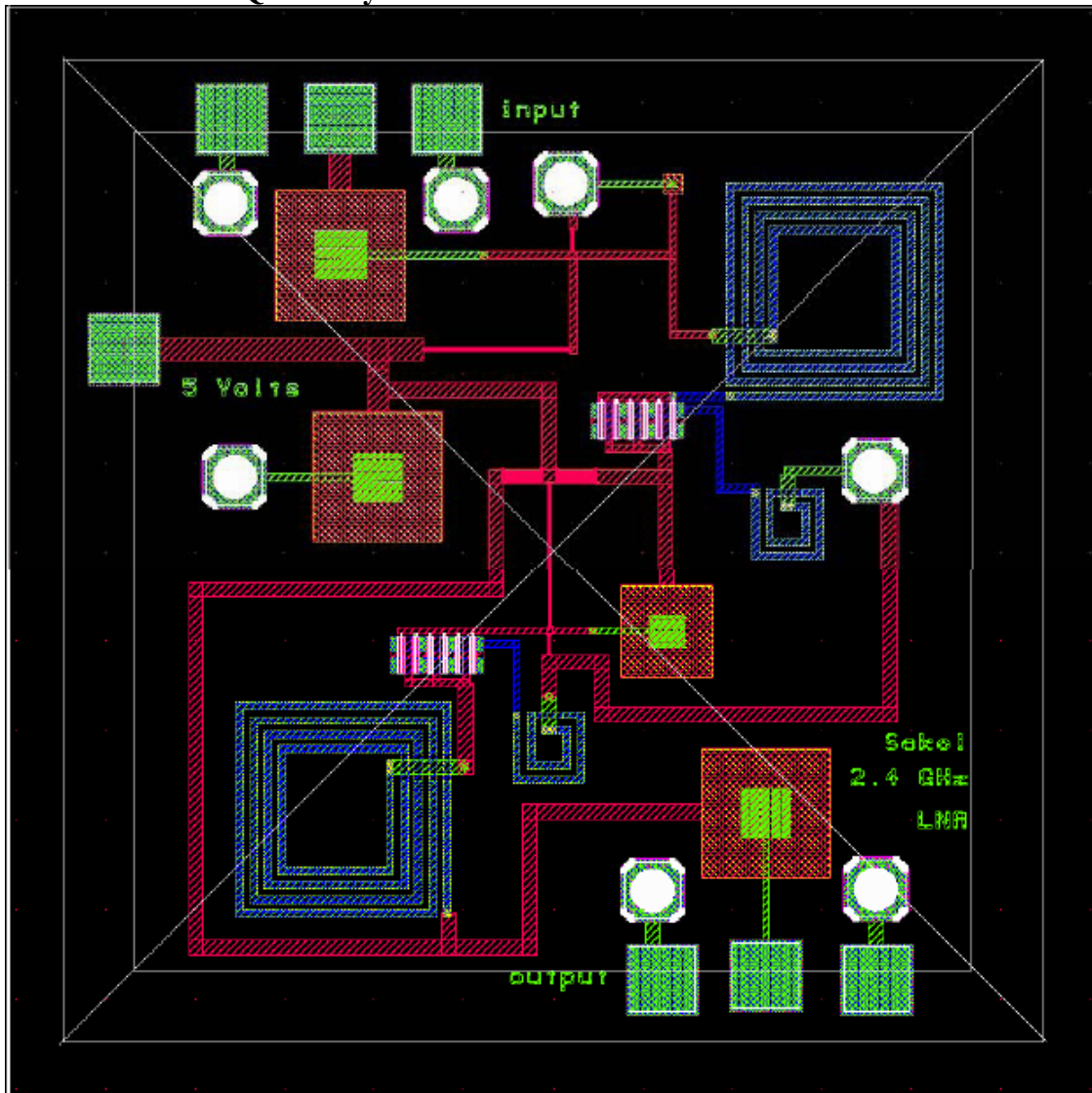


It can be seen the input third order intercept point will be greater than +5dBm. The results from +2 to +5dBm could not be simulated as the simulation did not converge, however the trend in the chart in the upper right-hand corner indicates that the convergence point will be beyond +5dBm.

The following graphic (Figure 12) illustrates the final layout of the aforementioned two-stage LNA design:



**FIGURE 12 – TriQuint Layout of MMIC LNA**



The line widths for the Metal0 layers (appearing in red) were increased to allow for the current levels predicted in the DC annotation of the simulated circuit. +5 Volts is applied to the green pad labeled “5 Volts” in the upper left-hand corner of the circuit. The input to the LNA is the green ground-signal-ground pad area shown in the upper left-hand corner of the circuit. The output of the LNA is the green ground-signal-ground pad area in the lower right-hand corner of the circuit.

## **6 Test Procedure**

The input frequency should be swept from 2.0 to 3.0 GHz. The input power level should be kept between -30 and -8dBm to assure that the higher order harmonics do not overtake the strength of the fundamental. Within this frequency band and input power level, the gain should be between 20 and 25dB, as simulated. After the network analyzer is calibrated, the S11, S22 and S21 parameters should be measured when the frequency is

swept from 2 to 3 GHz. The noise figure should also be measured across this frequency band to corroborate the design.

## **7 Conclusion**

The previously described MMIC LNA circuit should meet the requirements specified at the beginning of the report. One source of improvement would be if the input bias circuits' impedances could have been increased. This would effectively improve the noise figure of the circuit without any noticeable degradation in any of the other performance parameters. These resistor values were optimized so that the circuit could fit within the die region.

**The Johns Hopkins University  
Whiting School of Engineering**

*525.787 MMIC Design, Fall 2006*

Instructors John Penn and Dr. Michel Reece

High Efficiency, Medium Power Amplifier

Peter L. Smith

## Table of Contents

<b>1. Abstract</b>	<b>3</b>
<b>2. Introduction</b>	<b>3</b>
<b>3. Design Approach</b>	<b>4</b>
<b>3.1. Power Amp</b>	<b>4</b>
<b>3.1.1. Determine Bias Point, PAE, and RCripps</b>	<b>4</b>
<b>3.1.2. Add Bias Circuitry</b>	<b>5</b>
<b>3.1.3. Stabilize</b>	<b>5</b>
<b>3.1.4. Matching Network</b>	<b>6</b>
<b>3.2. Driver Amp</b>	<b>8</b>
<b>3.2.1. Determine Bias Point</b>	<b>8</b>
<b>3.2.2. Add Bias Circuitry</b>	<b>9</b>
<b>3.2.3. Stabilize</b>	<b>9</b>
<b>3.2.4. Matching Network</b>	<b>10</b>
<b>4. High Efficiency Medium Power Amplifier</b>	<b>12</b>
<b>4.1. Schematic</b>	<b>13</b>
<b>4.2. Simulations</b>	<b>14</b>
<b>4.3. Layout</b>	<b>16</b>
<b>4.4. Test Plans</b>	<b>16</b>
<b>5. Lessons Learned, Summary</b>	<b>17</b>
<b>6. Conclusion</b>	<b>17</b>

## Table of Figures and Tables

<b>Figure 1.</b> Dmode FET IV Curves with Power Amp Bias	<b>4</b>
<b>Figure 2.</b> PA Bias Circuitry	<b>5</b>
<b>Figure 3.</b> Power Amp Schematic	<b>6</b>
<b>Figure 4.</b> Voltage Domain Performance of the Power Amp	<b>7</b>
<b>Figure 5.</b> Power Domain Performance of the Power Amp	<b>7</b>
<b>Figure 6.</b> Bias and Load Line for the Driver Amp	<b>8</b>
<b>Figure 7.</b> Driver Amp Bias Circuitry	<b>9</b>
<b>Figure 8.</b> Driver Amp Schematic	<b>10</b>
<b>Figure 9.</b> Voltage Domain Performance of the Driver Amp	<b>11</b>
<b>Figure 10.</b> Power Domain Performance of the Driver Amp	<b>12</b>
<b>Figure 11.</b> Two Stage Power Amp Schematic	<b>13</b>
<b>Figure 12.</b> Voltage Domain Performance of the Amp 2 Stage	<b>14</b>
<b>Figure 13.</b> Power Domain Performance of the 2 Stage Amp	<b>15</b>
<b>Figure 15.</b> 2 Stage Power Amp Layout	<b>16</b>
<b>Table 1.</b> Summary of Two Stage Power Amp Performance	<b>17</b>

## 1. Abstract

This paper describes the design and simulated performance of a two stage power amp. The simulation was performed using ADS. The associated layout is also provided. The critical design parameter is power added efficiency (PAE). A PAE of 21% was attained.

## 2. Introduction

Design a high efficiency, medium power amplifier using TriQuint 6x50 0.5 $\mu$ m Dmode PHEMTs (TQPED PHSS). Use on chip drain and gate bias networks, output matching network, and input matching network. The goal is efficiency to get the most RF output power for a given DC consumption (i.e. battery life). Try to attain the following specified values.

REQUENCY: 2.305-2.497 GHz

GAIN, small signal: threshold 18 dB, objective 20 dB

GAIN RIPPLE:  $\pm 0.5$  dB max

OUTPUT POWER: > TBD

POWER ADDED EFFICIENCY: > threshold 20 % @ 1 dB compression,  
objective 25 % @ 1 dB compression

VSWR, 50  $\Omega$ : < 1.5:1 input & output

SUPPLY VOLTAGE: signal voltage supply at +3.3 V, goal (3 to 3.6 V range)

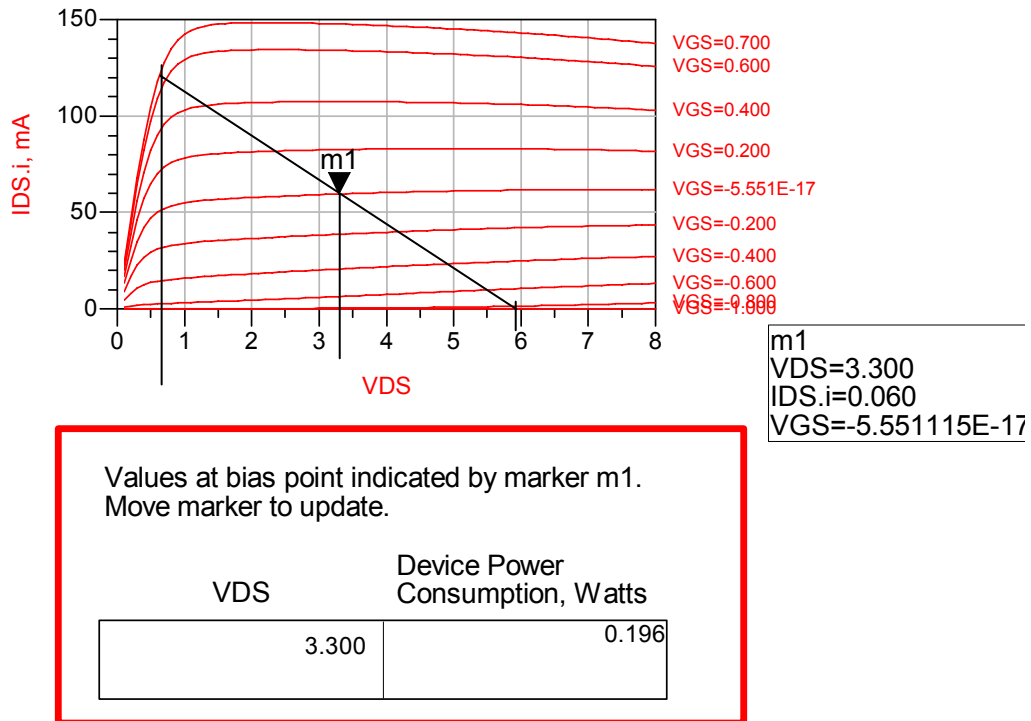
### 3. Design Approach

The overarching design strategy will be to use two stages. We'll begin by designing the output stage, biased at approximately  $I_{\max}/2$  (~ 55 mA). This will be the power amp. Next we'll add a second stage biased to attain spec (~ 15–20%  $I_{\text{dss}}$ ). This will be the driver amp. Finally we'll put the two stages together and simplify the inter-stage topology as much as possible.

#### 3.1. Power Amp

##### 3.1.1. Determine Bias Point, PAE, and RCripps

Setting  $V_{\text{ds}}$  to 3.3 V we see in Figure (1) that  $V_{\text{gs}}$  equal 0 V is a reasonable bias point. It also has the advantage of very simple bias circuitry.

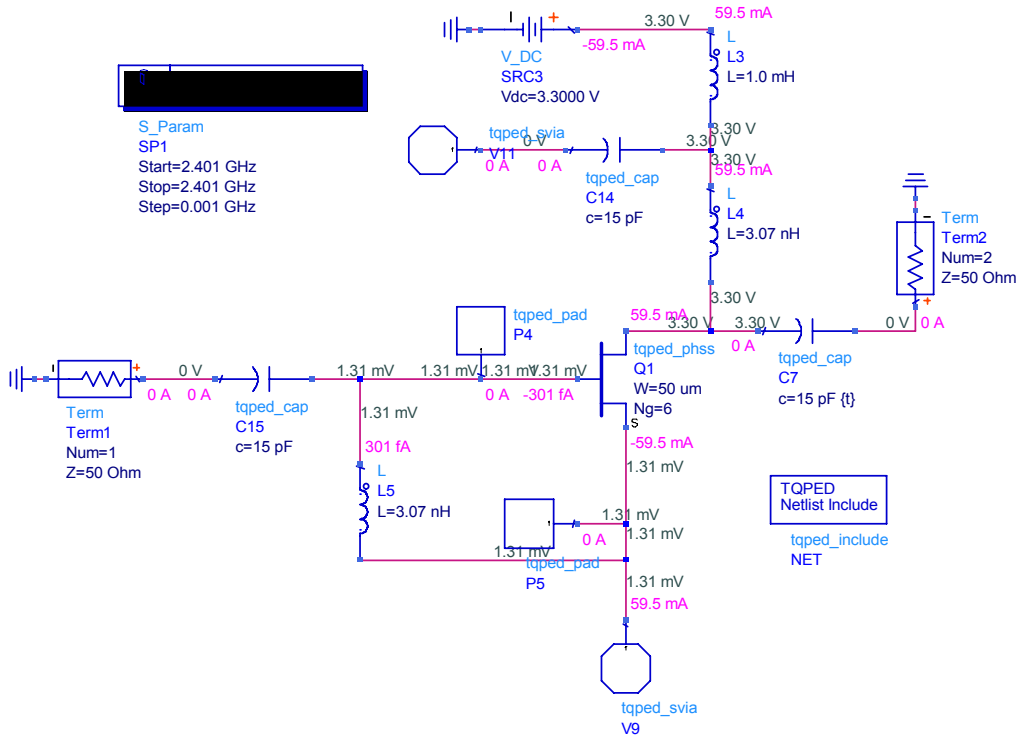


**Figure 1.** Dmode FET IV Curves with Power Amp Bias

From the load line we see that  $\Delta V_{\text{DS}}$  is  $2 \times (3.3 - 0.65) \text{V} = 5.2 \text{V}$  and  $\Delta I_{\text{DS}}$  is about 120 mA. So the RF output power should be around 78 mW. The device power consumption is 196 mW, giving a Power Added Efficiency (PAE) of approximately 39%.  $R_{\text{cripps}}$  is given by  $\Delta V_{\text{DS}} / \Delta I_{\text{DS}}$  which equals  $43.3 \Omega$ .

### 3.1.2. Add Bias Circuitry

In the design of the bias circuits we want to use the largest inductance and capacitance feasible. For our application feasibility is determined by the percentage of chip area an element requires. After some bitter experience it is found that a 15 pF capacitor and 3 nH inductor are close to the larger end of what will fit on the square chip. (If we had more time we would have experimented with what fits on the largest chip, just to allow for the largest possible inductor and capacitor values; but that actually takes much more time than one would at first think – at least for a neophyte such as myself) This bias circuitry is illustrated in Figure (2).



**Figure 2.** PA Bias Circuitry

Note the pads will be used for testing the DC bias on the chip.

### 3.1.3. Stabilize

Using the tuner, we find that a 120 Ω shunt resistor on the input stabilizes the device from 0.1 GHz to 20 GHz.

### 3.1.4. Matching Network

We use “Cripps Method” to get the output matching circuit. The impedance looking into the output of the amplifier is equivalent to a 2.9 nH shunt inductor ( $L_{ds}$ ) in parallel with a 323  $\Omega$  shunt resistor ( $R_{ds}$ ), which gives a  $Z_{22}$  of  $5.866 + j43.159 \Omega$ . We want to resonate out the reactance and add a load resistance of  $R_{cripps}$  as determined in (3.1.1). Doing this causes the  $Z_{22}$  looking into the circuit to be  $21.976 - j21.648 \Omega$ . That is, we will use the Smith chart to select the circuit corresponding to the path going from  $21.976 + j21.648 \Omega$  to 50  $\Omega$  and which uses the most reasonable values while avoiding the edges of the Smith chart. Using the smith chart program we find that a 206.8 pH series inductor followed by a 1.502 pF shunt capacitor provide that Cripps output matching circuit. We place these in the ADS schematic and then find that  $Z_{11}$  is given by  $57.693 + j46.875 \Omega$ . We conjugate match this value. That is, design the input matching circuitry to map  $57.693 + j46.875 \Omega$  to 50  $\Omega$ . Doing this yields 1.223 pF shunt capacitor followed by a 3.172 nH series inductor. At the first pass, the output VSWR shows a problem. It is found to be 6.45. Changing the output match in order to lower the output VSWR to 1.5, results in an unacceptable PAE of around 1.5 %. Adding an output matching circuit results in a VSWR of at least 3.5 and decreases the PAE from around 30% to 15%. As PAE is the critical parameter, we’ll accept whatever VSWR we get and assume the chip is connected to an isolator on the output. With the 100 Ohm shunt resistor and matching circuitry we arrive at the power amp illustrated in Figure (3).

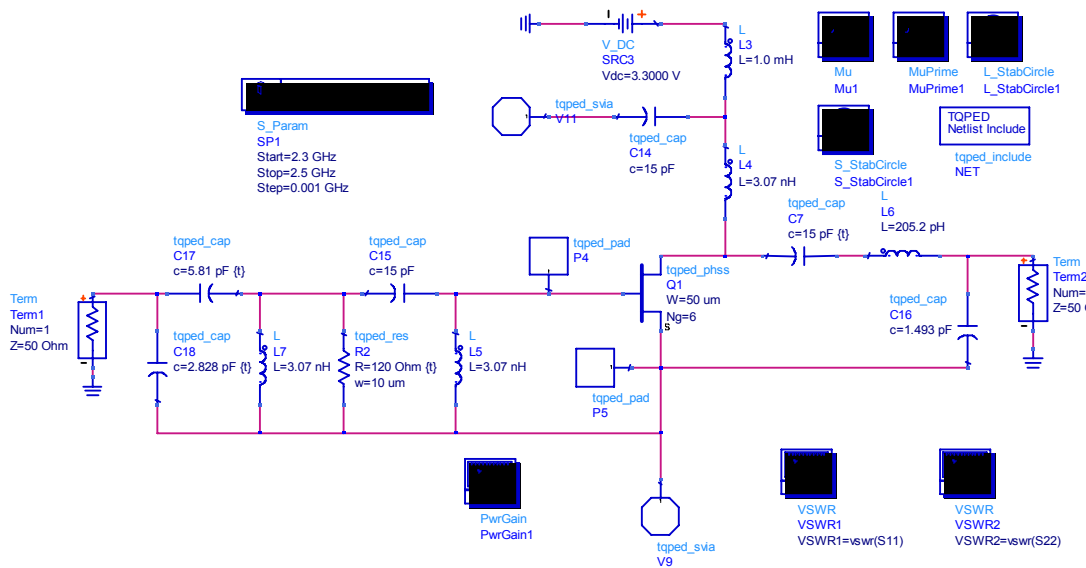
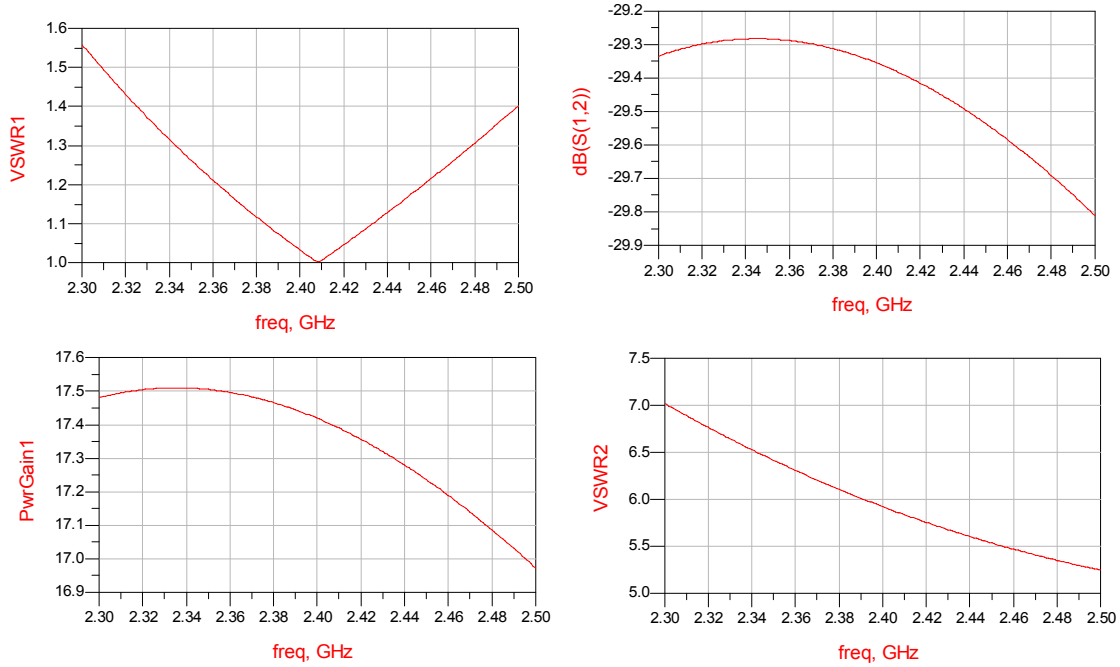


Figure 3. Power Amp Schematic

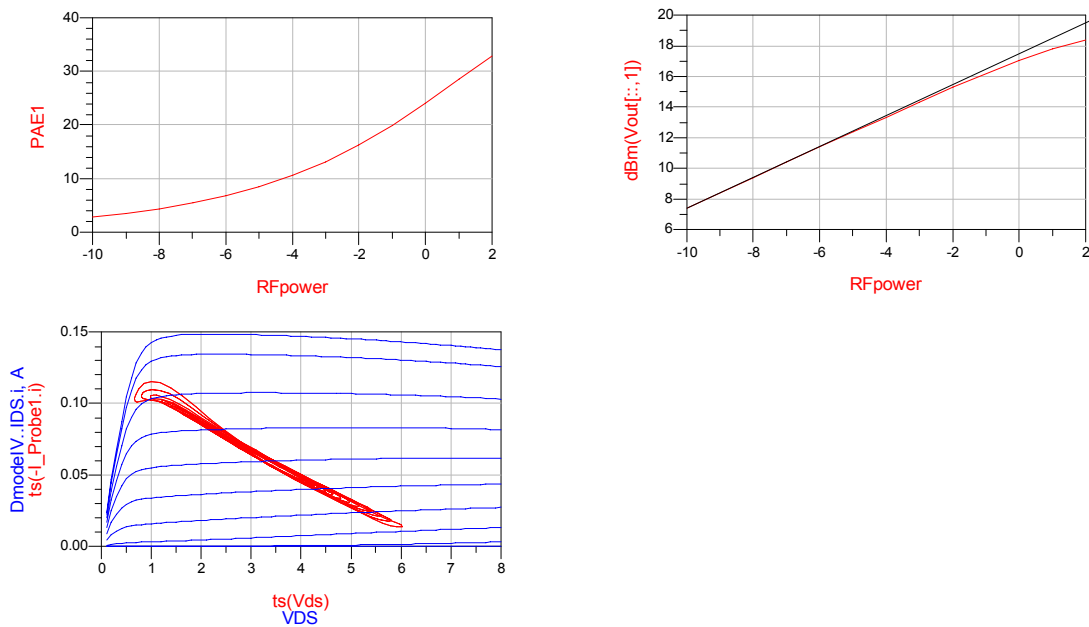


The VSWR, S12, and power gain are provided in Figure (4).



**Figure 4.** Voltage Domain Performance of the Power Amp

Note, VSWR1 is input VSWR and VSWR2 is output side VSWR (looking into the output). Note that we have insufficient gain, hence the need for the driver amp. The load line, power out, and PAE are provided in Figure (5).



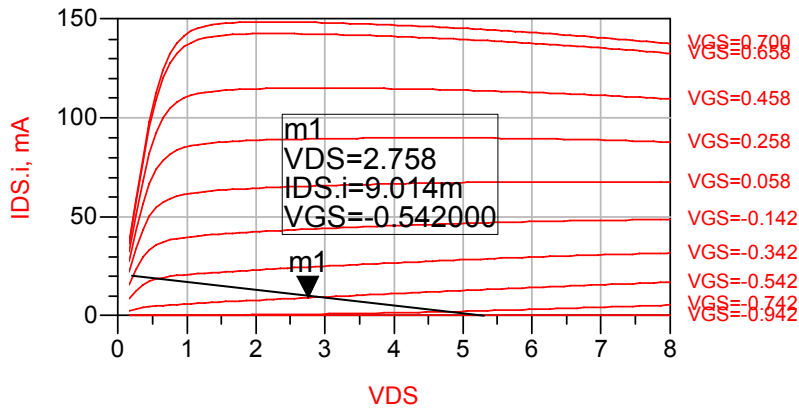
**Figure 5.** Power Domain Performance of the Power Amp

Note that the 1 dB of compression occur at approximately at 2 dBm RF power in. At this point RF power out is 18 dBm, and PAE is 31%. Thus, we would like the drive amp to be linear up until a little beyond 2 dBm, since we don't want it to compress before the power amp.

### 3.2. Driver Amp

#### 3.2.1. Determine Bias Point

For the driver amp we will seek gain with minimal DC power. This may be accomplished with the load line shown in Figure (6).



Values at bias point indicated by marker m1.  
 Move marker to update.

VDS	Device Power Consumption, Watts
2.758	0.025

**Figure 6.** Bias and Load Line for the Driver Amp

From the load line we see that  $\Delta V_{DS}$  is  $2 \times (2.758 - 0.25) V = 5.0 V$  and  $\Delta I_{DS}$  is about 20 mA. So the RF output power should be around 12.54 mW. The device power consumption is 25 mW.

### 3.2.2. Add Bias Circuitry

We will accomplish this bias with the circuitry illustrated in Figure (7).

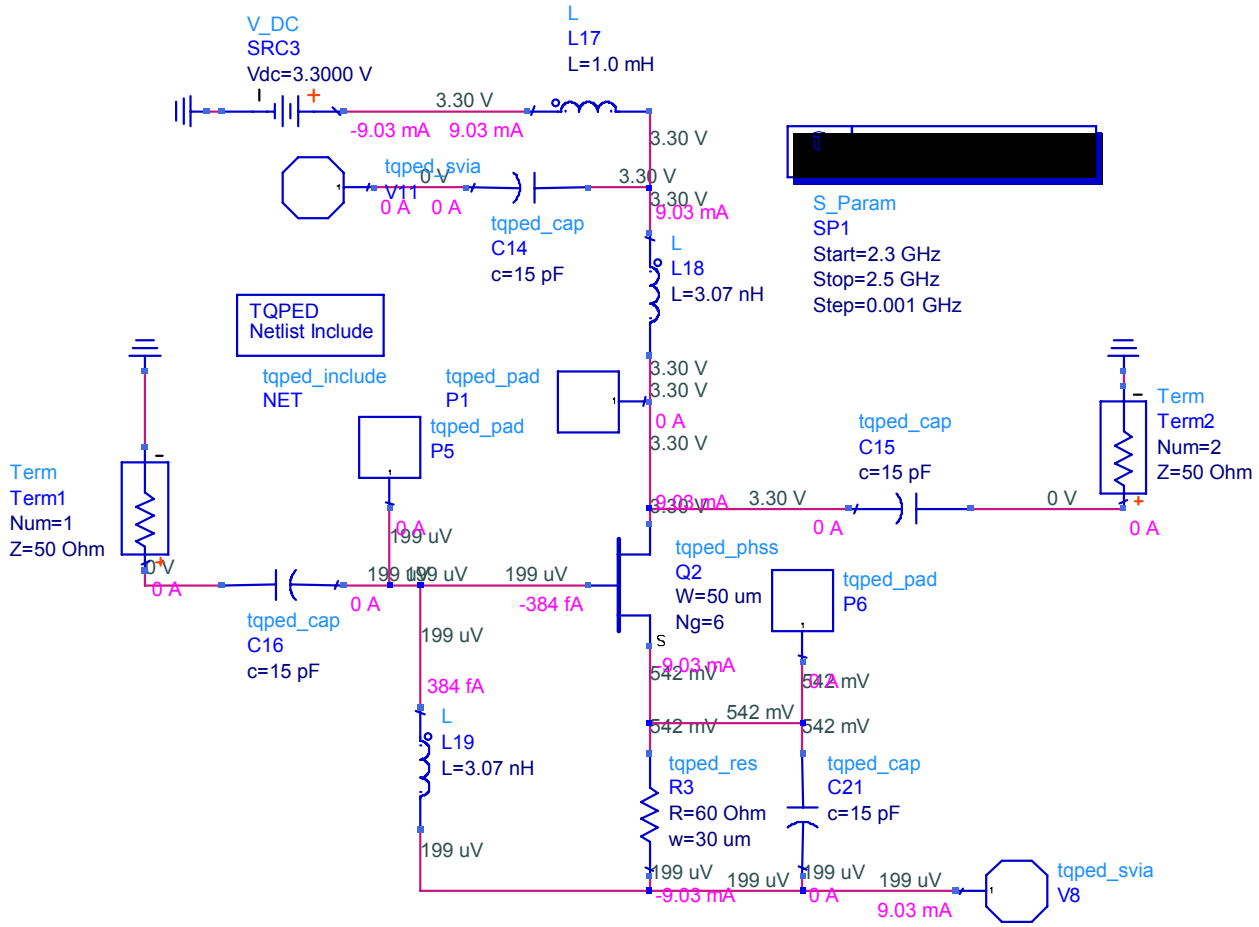


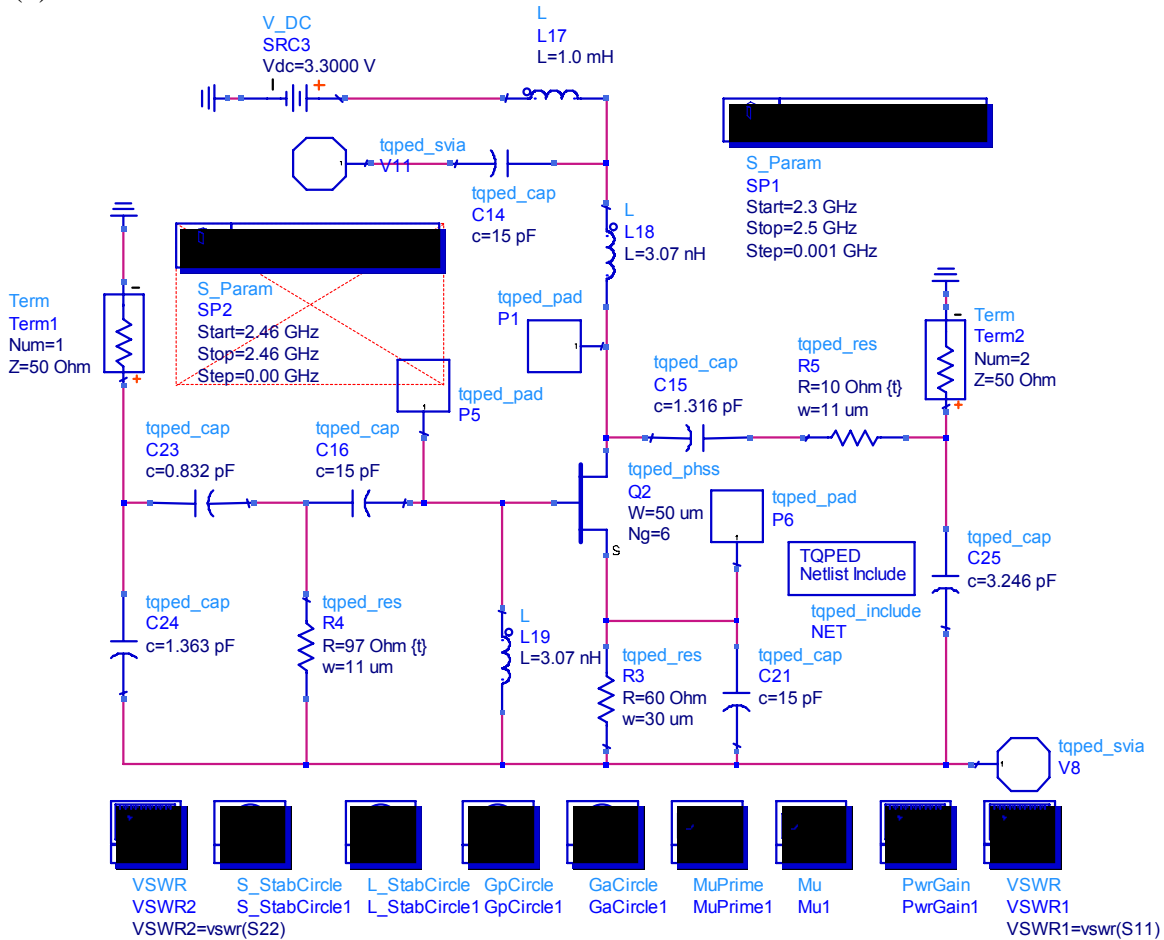
Figure 7. Driver Amp Bias

### 3.2.3. Stabilize

We will use two different stabilizing topologies. In the first topology a drain feed back consisting of a 15 pF capacitor and a 270  $\Omega$  resistor to stabilize the driver from 2.3 to 2.5 GHz. In the second a topology a 97  $\Omega$  shunt resistor on the gate and a 10  $\Omega$  series resistor on the drain.

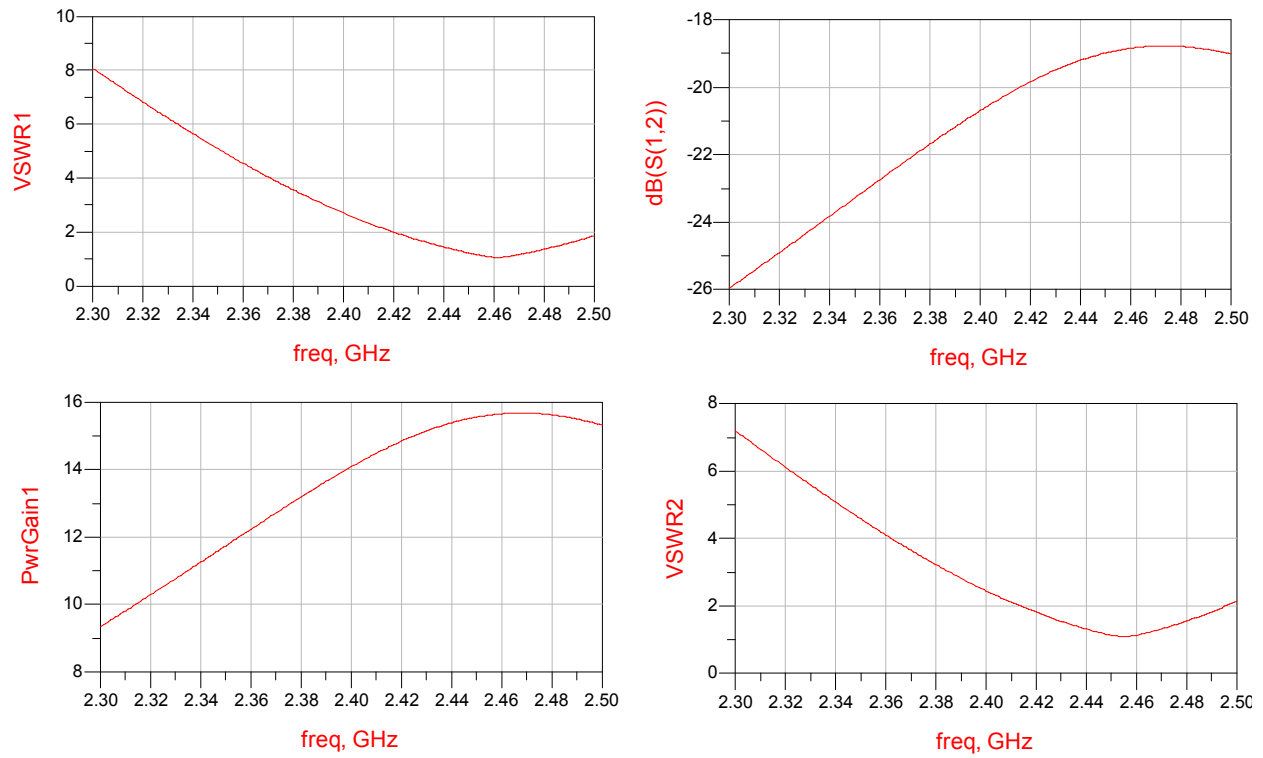
### 3.2.4. Matching Network

Notice that the gain for the power amp peaks at approximately 2.34 GHz. So we will design the driver amp to have peak gain at 2.46 GHz. The combined gain will then have less ripple over the band. As we are designing for maximum gain, we will conjugate match the input and output. For the input we will match the conjugate the center of the available gain circle to 50 Ω. For the output we will match the conjugate the center of the power gain circle to 50 Ω. The resulting circuit is illustrated in Figure (8).



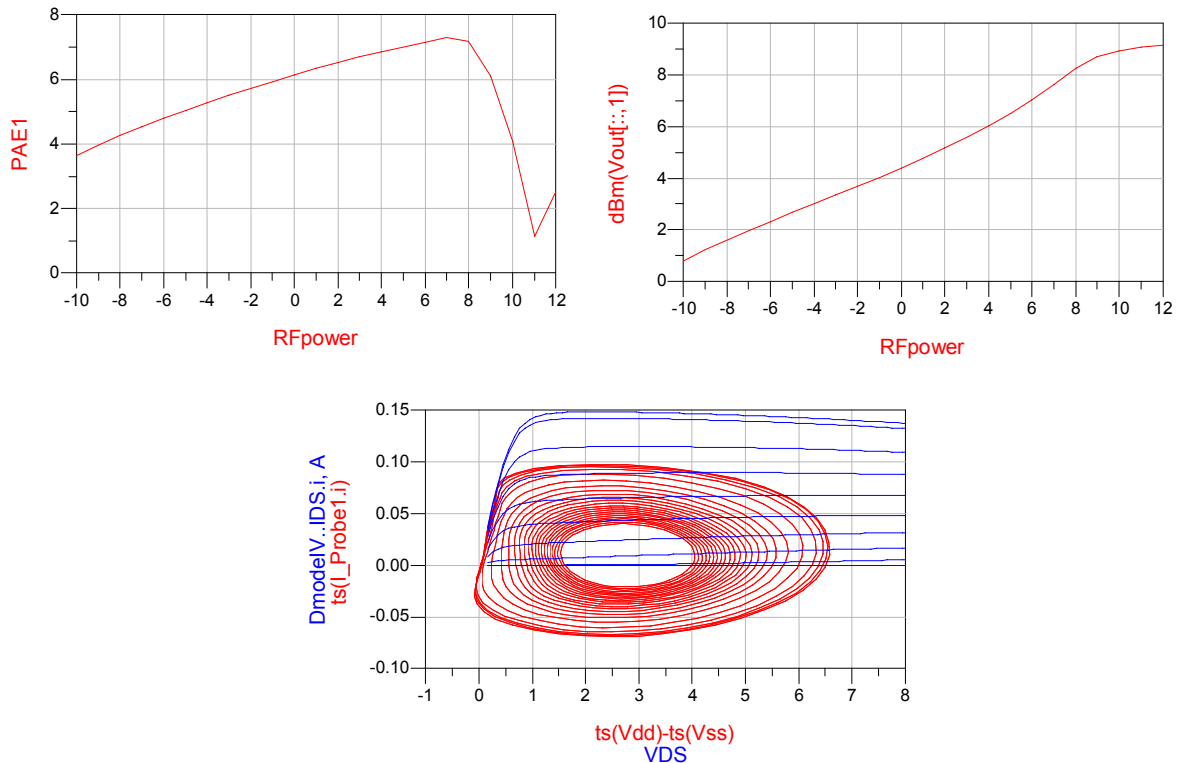
**Figure 8.** Drive Amp Schematic

Note that this is the second stabilizing topology. It turns out that the first topology had approximately the same VSWR, but 5 dB less gain. The voltage domain performance for our driver amp is provided in Figure (9).



**Figure 9.** Voltage Domain Performance for the Driver Amp with R3 Equal 60  $\Omega$

VSWR is larger than desired, but as we said above, we'll have to live with it. The peak power gain is at the correct frequency. The power domain performance is provided in Figure (10).



**Figure 10.** Power Domain Performance for the Driver Amp with R3 Equal 60  $\Omega$

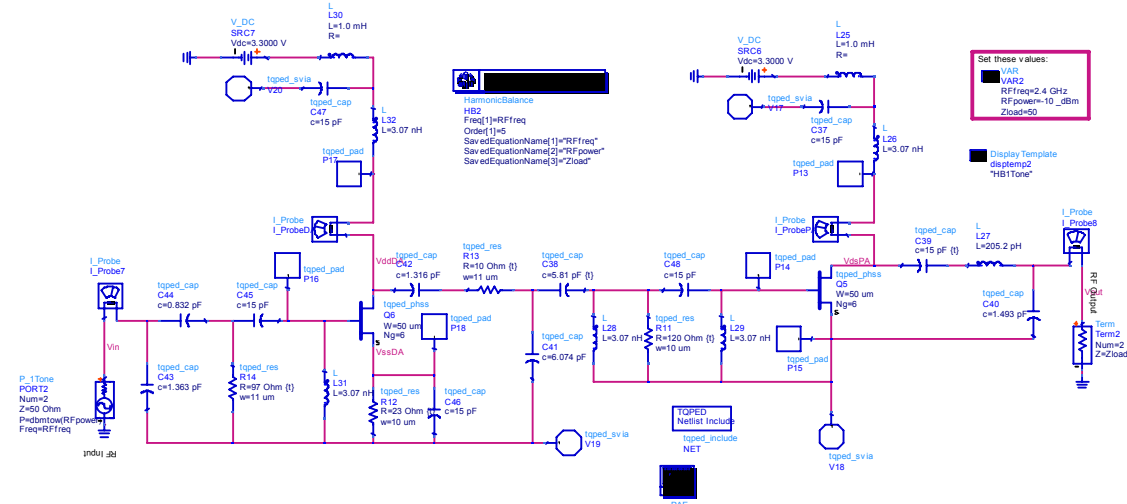
Note that we don't get into compression until beyond 8 dBm. This can be adjusted by changing R3. It was found that while the power domain performance was greatly affected by the value of the source resistor, R3, the voltage domain performance was not. Hence, this will be the major parameter for tuning the composite, 2-stage amplifier. I'm not sure that this load line is as healthy as it could be. I was expecting it to be more linear. I'm not sure what affects this will have on the two-stage performance.

#### 4. High Efficiency, Medium Power Amplifier

We put the driver amp before the power amp in a schematic and simplify. We add together the two parallel intermediate capacitors. When we try to remove the power amp's gate blocking capacitor we encounter stability problems so we'll leave it in. We experiment with the driver amp's source resistor to ground in order to maximize the PAE. We find the 28  $\Omega$  performs the best.

### 4.1. Schematic

The schematic for the final design is given in Figure (11).

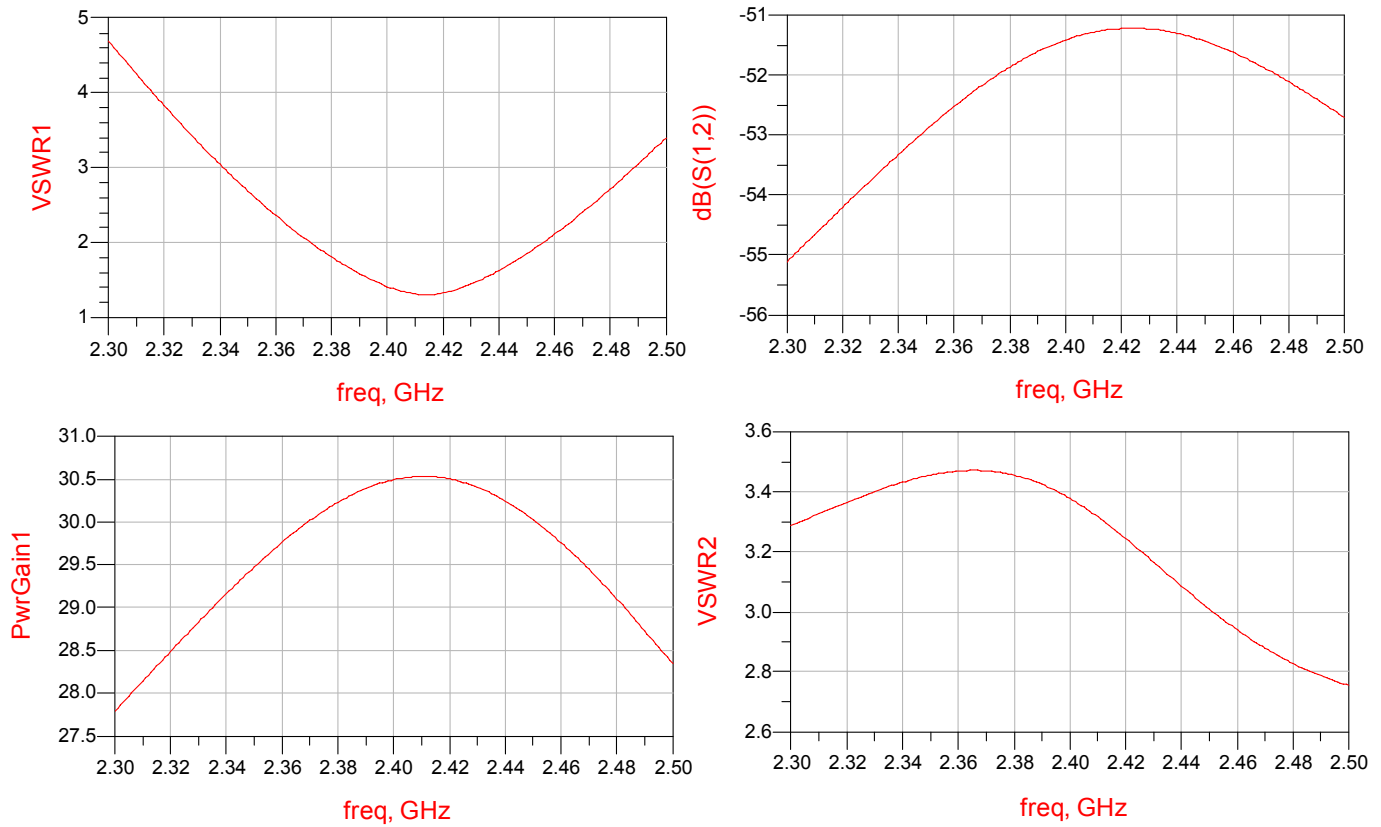


**Figure 11. Two Stage Power Amp Schematic**

In the next stage of development we'll combine the two DC sources into one DC source. Currently, when I do this, the design becomes extremely unstable. Even if the shunt capacitor is increased to 60 pF and the series inductor is increased to 1 H. Note that the PAE DC current is the sum of both sources.

## 4.2. Simulations

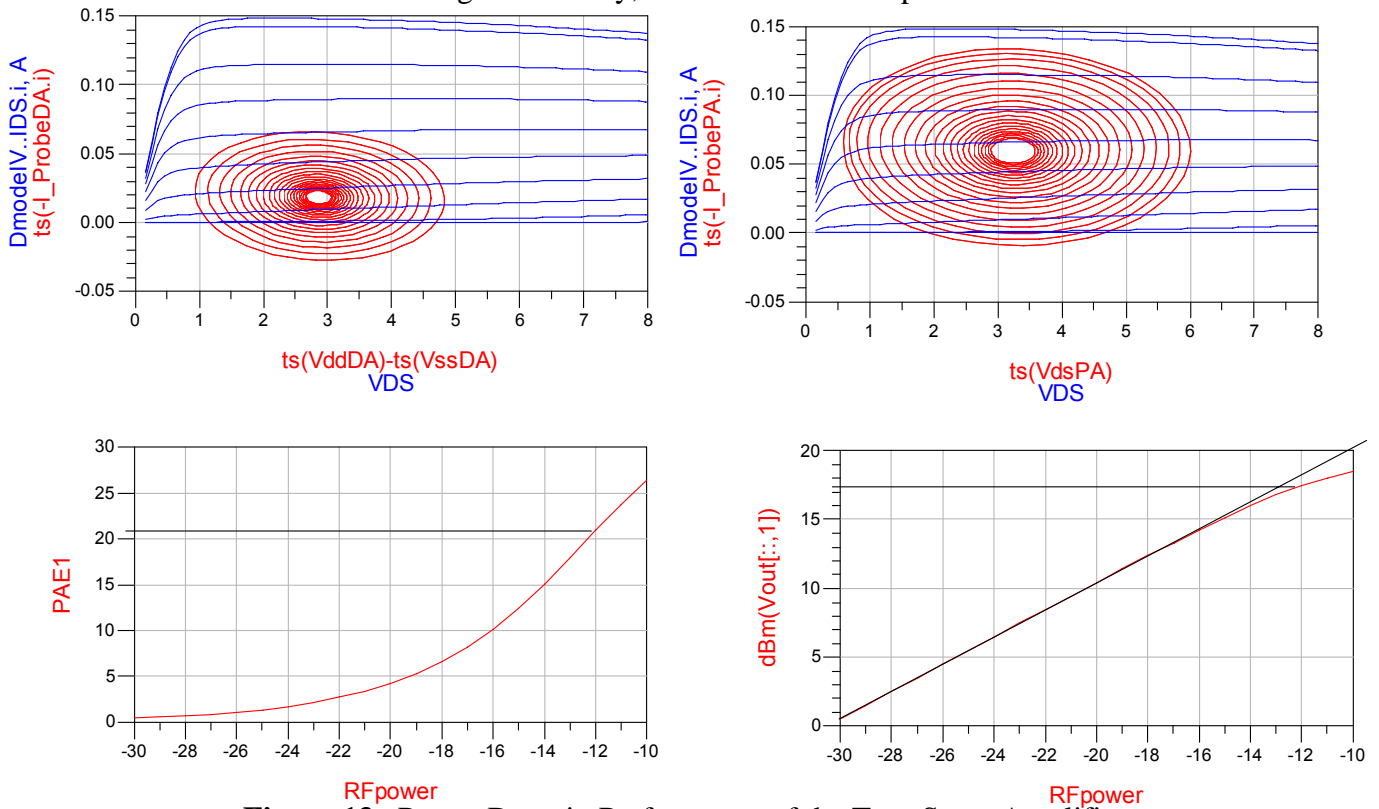
The voltage domain simulation is provided in Figure (12).



**Figure 12.** Voltage Domain Performance of the Two Stage Power Amplifier

The VSWRs are out of the desired performance bounds. There is more than enough gain now. There is 2.5 dB of ripple instead of the desired 0.5 dB. The power domain performance is provided in Figure (13).



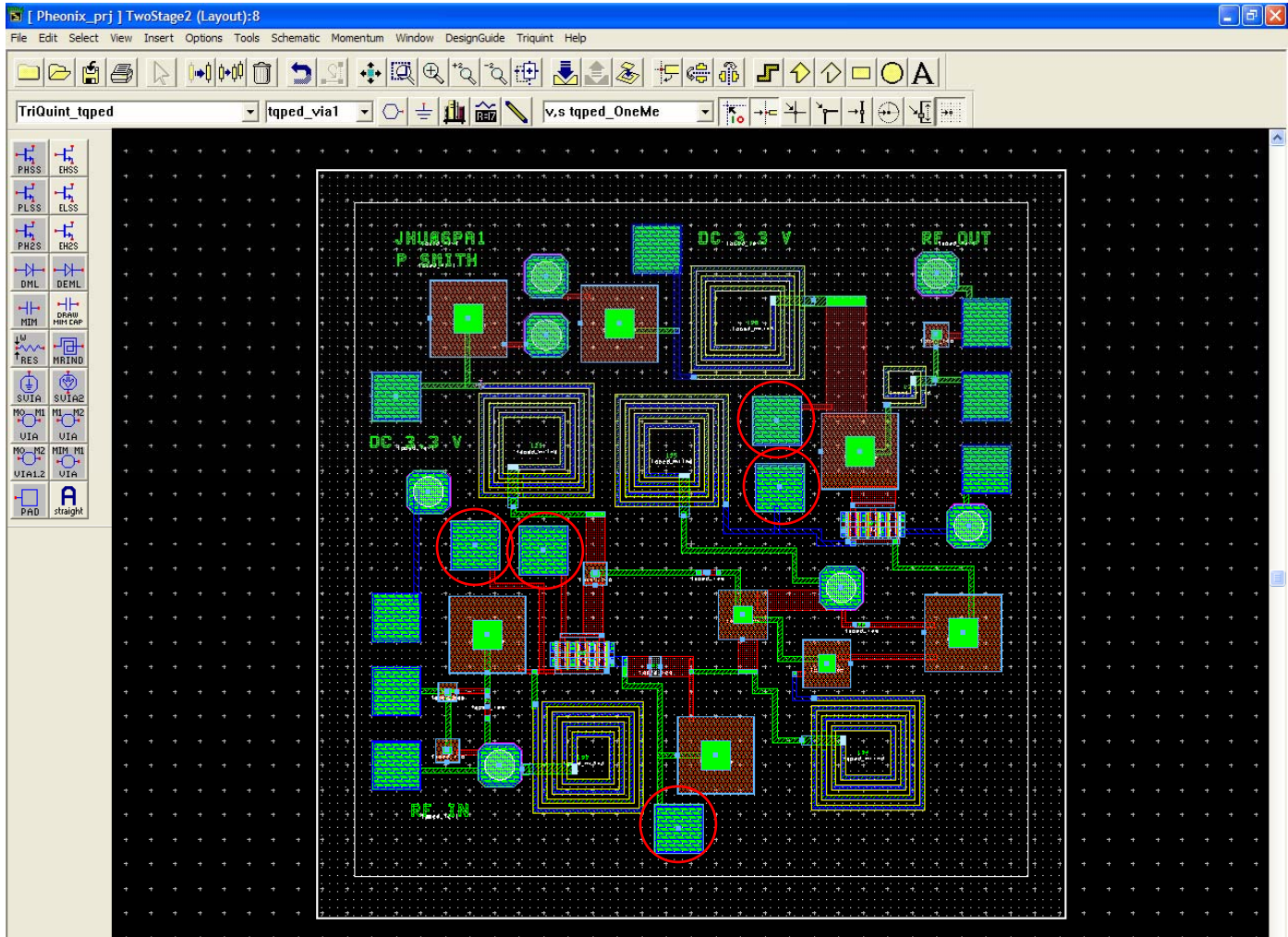


**Figure 13.** Power Domain Performance of the Two-Stage Amplifier

Note that the driver stage is not compressing. This performance produced the best ratio of RF power out to DC power in, through tuning the source resistor to ground on the driver amp. The output power at the one dB compression point is 17 dBm. The PAE 21%.

### 4.3. Layout

The layout is illustrated in Figure (14).



**Figure 14.** Two Stage Power Amp Layout (The bias checking pads are circled in red.)

### 4.4. Test Plans

Assuming that I can acquire suitable matching circuitry I will proceed as follows. First I will set the DC inputs to 3.3 V with no input RF power and measure the VSWRs. Next, I will use the extra pads to check the bias to see if it is correct. Then I will slowly increase the input RF power while measuring the power out and gain to see how closely, if at all, it matches the expected power out and gain.

## 5. Lessons Learned and Things I Would Have Done If I Had More Time

1. In the next stage of development we'll combine the two DC sources into one DC source. Currently, when I do this, the design becomes extremely unstable.
2. I need to consider another method of minimizing gain ripple.
3. I would like to vary the various parameters, such as input voltage, capacitance values, inductance values, resistance values, in order to test for sensitivity.
4. I would like to implement the microstrip to get a better estimate of performance.
5. I would like to try the Emode transistor.
6. I would like to find a better biasing scheme.

## 6. Conclusion

A high efficiency, medium power amplifier was designed using TriQuint 6x50 0.5 $\mu$ m Dmode PHEMTs (TQPED PHSS). On chip drain and gate bias networks, output matching network, and input matching networks were implemented. The goal was maximum efficiency to get the most RF output power for a given DC consumption (i.e. battery life). The resulting performance is summarized in Table (1).

<b>Table 1. Summary of Two Stage Power Amp Performance</b>		
	Desired	Attained
REQUENCY	2.305-2.497 GHz	2.305-2.497 GHz
GAIN	threshold 18 dB, objective 20 dB	30.5 dB peak, 28.8 dB min
GAIN RIPPLE	0.5 dB	2.5 dB
OUTPUT POWER	TBD	17 dBm, 1 dB compression
PAE	threshold 20% @ 1 dB, objective 25% @ 1 dB	21%
VSWR, 50 $\Omega$	1.5:1 input & output	4.8 max input, 3.5 max output
SUPPLY VOLTAGE	+3.3 V signal voltage supply at, goal (3 to 3.6 V range)	+3.3 V

# Vector Modulator

## Final Report

MMIC Design EE787  
Fall 2006

Design Name: jhu06vmd

Jonathan Egan

## 1. Abstract

*A 2.4 GHz vector modulator using TriQuint's 0.5 $\mu$ m PHEMT process was designed and simulated. This MMIC vector modulator is capable of outputting a QPSK modulated signal with as low as 6dB of insertion loss. Two voltage supplies, one for in-phase (I) and one for quadrature (Q), are used to modulate the signal. The device is able to handle an input power greater than 0dBm. It has a VSWR of less than 1.4:1.*

## 2. Introduction

The vector modulator that is described in this paper provides a compact, low power, and moderate loss way to QPSK modulate a signal. It is designed to operate in the S-band using wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies (2.305 – 2.497 GHz). The states of the vector modulator are achieved by changing the voltage of the I and Q inputs to different combinations of +0.5V and -0.7V. For example by setting the I and Q inputs both to +0.5V there will be a  $45^\circ$  phase shift. Though any point inside the four corners can be obtained as well. The corner points fall at  $\pm 45^\circ$  and  $\pm 135^\circ$  with a constant amplitude for QPSK.

The design was done on GaAs using TriQuint's  $0.5\mu\text{m}$  PHEMT process. The simulations and layout were done using Agilent's Advanced Design System (ADS). All the data presented in this paper is simulated using TriQuint's design kit components. All the components in the design are lumped elements, because of the size of a wavelength relative to the chip dimensions. Much more detail will be provided including expected performance plots throughout the paper.

### 3. Design Approach

The goal for the vector modulator design was to QPSK modulate a signal to be transmitted. The basics of the design came from a paper written by J. Penn, see references. The design uses a  $90^\circ$  hybrid at the input to split the signal in I and Q with the isolated port terminated. Then a variable attenuator is used to adjust the amplitude of the I and Q signals independently. As described in Penn's paper, the variable attenuators are reflective attenuators using a  $90^\circ$  hybrid and two FET transistors as the variable resistors. Then the two signals are added together yielding a phase and amplitude shifted signal. Though for QPSK the amplitudes are the same, but the phases are  $90^\circ$  apart starting at  $45^\circ$ .

I started the design by creating a simulation of the basic building blocks of the vector modulator. I used ADS system passive components for the  $90^\circ$  hybrid and Wilkinson splitter as is similar to the simple schematic shown in section 5. I used this to explore the learn how to operate the vector modulator. I discovered that the vector modulator can be used for any amplitude and phase based modulation schemes, since any point inside most extreme points can be used. The downfall of using point closed to the origin than the corners is the loss is very high. This is explained in more detail in the following paragraphs.

From there I designed the blocks using ideal lumped elements. Because of the limitation of space and the small size of a MMIC, transmission lines could not be used. So I converted the design of the  $90^\circ$  hybrid and Wilkinson splitter to lumped elements using the Pi network model.

At this point I chose a transistor size that was a compromise between resistance and capacitance for the variable attenuator. The transistor acts as variable resistor using the gate voltage to tune it.

The reflective attenuators are key to changing the amplitude and phase of the signal. They work by adjusting the amount of mismatch-induced reflection caused by the variable resistors. The signal enters the  $90^\circ$  hybrid then splits equally with a  $90^\circ$  phase shift on the one port. When the resistor is an open circuit or a short circuit all the power is reflected back to the hybrid. It is then combined at the isolated port, theoretically having no loss. When the resistors are  $50\Omega$ , assuming this is a  $50\Omega$  system, none of the power is reflected the resistor dissipates it all. Therefore there is maximum attenuation when the resistors are  $50\Omega$ . In the case of this design the transistors have a nominal resistance and a maximum resistance. This is why the insertion loss of this design is a minimum of 6dB. Also the capacitance of the transistors causes the insertion loss to vary with frequency. The balance of resistance and capacitance in the transistors is explained in section 3.2.

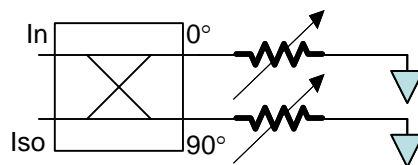


Figure 3-1: A diagram of a reflective attenuator using a  $90^\circ$  hybrid and two variable resistors.

I then replace the ideal components with TriQuint models and converted ideal inductors to spiral inductors. I then optimizing each piece of the design for insertion loss, return loss, and phase in the case of the 90° hybrid. I paid special attention to the phase flatness of the 90° hybrids, because the accuracy of the phase is important to avoid excess loss in the reflective attenuators. If the two signals are not 90° apart they will not complete combine at one port and completely cancel at the other.

When adding interconnect, I used metal 2 where ever I could. Because of metal 2's thickness it would be the lowest loss metal without stacking two layers. Since the frequency is only 2.4GHz the skin depth is quite large relative to the metal thickness. Metal 2 would give the maximum amount of skin depths to avoid excess attenuation. Also when connecting the pieces of the design together I used 35µm wide line, where possible, to reduce loss and lower inductance.

At this point in the design I decided to add capacitors between the reflective attenuators and the Wilkinson splitter. These caps simply, rotate the phase of the constellation so that the corners are at ±45° and ±135°.

Finally I made modifications required to properly layout the design to fit on the 60 x 120 mil chip. During layout I chose to share some vias to conserve space. I chose to keep the layout symmetric putting the input and output on the 120µm sides of the chip and the I and Q on the 60µm sides. I also needed to put vias at the ground pads at the edge of the chip for the input and output. This is described further in section 3.2.

### 3.1 Specifications vs Goals

All specifications are met or the expected performance is better.

Specs	Specified Performance		Expected Performance from Simulation
	Goal	Max	
Frequency	2.305 - 2.497 GHz		> 2.305 - 2.497 GHz
Isolation	16dB	10dB	> 20dB
Loss	7dB	10dB	10dB Max
RF Input Power	0dBm		0dBm Min
VSWR	1.5:1	2.5:1	1.4:1
Supply Voltage	0 - 5V Variable		+0.5V, -0.7V

### 3.2 Tradeoffs

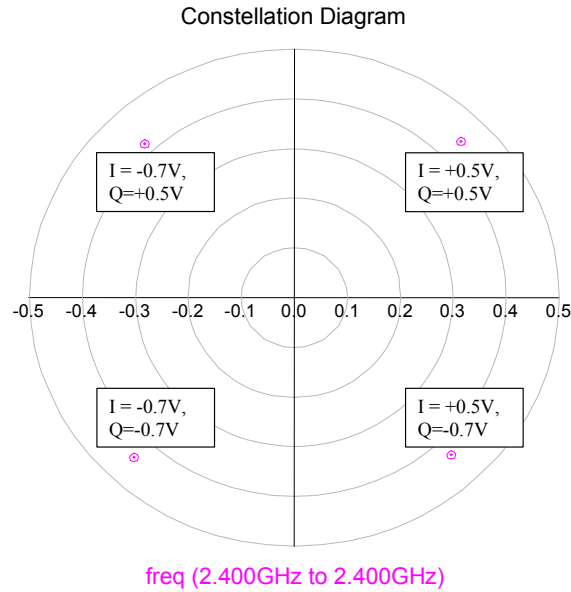
When picking a transistor for the variable attenuator part of the vector modulator, there was a tradeoff of the drain to source resistance and capacitance. As the size of a transistor gets larger, resistance reduces, thus lower loss, but the capacitance get larger as well. The converse is true for a small sized transistor.



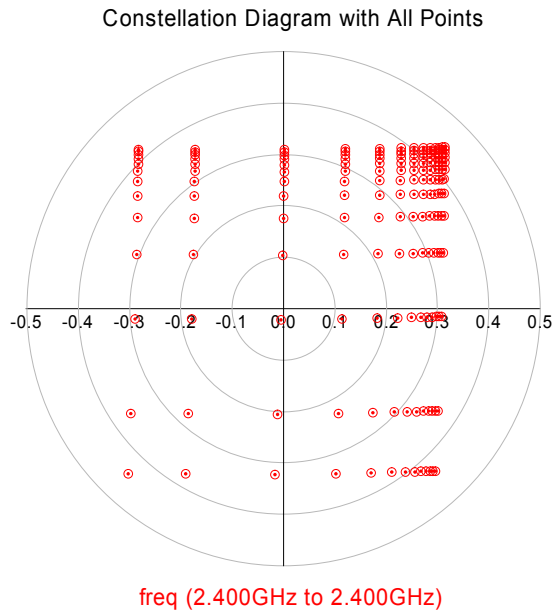
Another tradeoff I dealt with was in the layout. A design rule for vias is that they can not be as close to the edge of the chip as the pads. At the input and output of the layout I did not have room to put vias on the inside of the ground probe pads. The trade off was making room by moving the input 90° hybrid and Wilkinson splitter closer together, increasing the chance of coupling of the input to the output bypassing the attenuators or running long lines from vias to the pads. I opted for the latter choice for two reasons. One is that the lines required to connect the vias to the pads are long, they are still a tiny fraction of a wavelength at 2.4GHz and since I used 50Ω line there shouldn't be any extra inductance causing a problem. The second reason is that since we have vias, when the chip is mounted in a package the ground pads do not need to be used. So the risk is coupling weighted much heavier than moving the vias.

## 4. Simulations

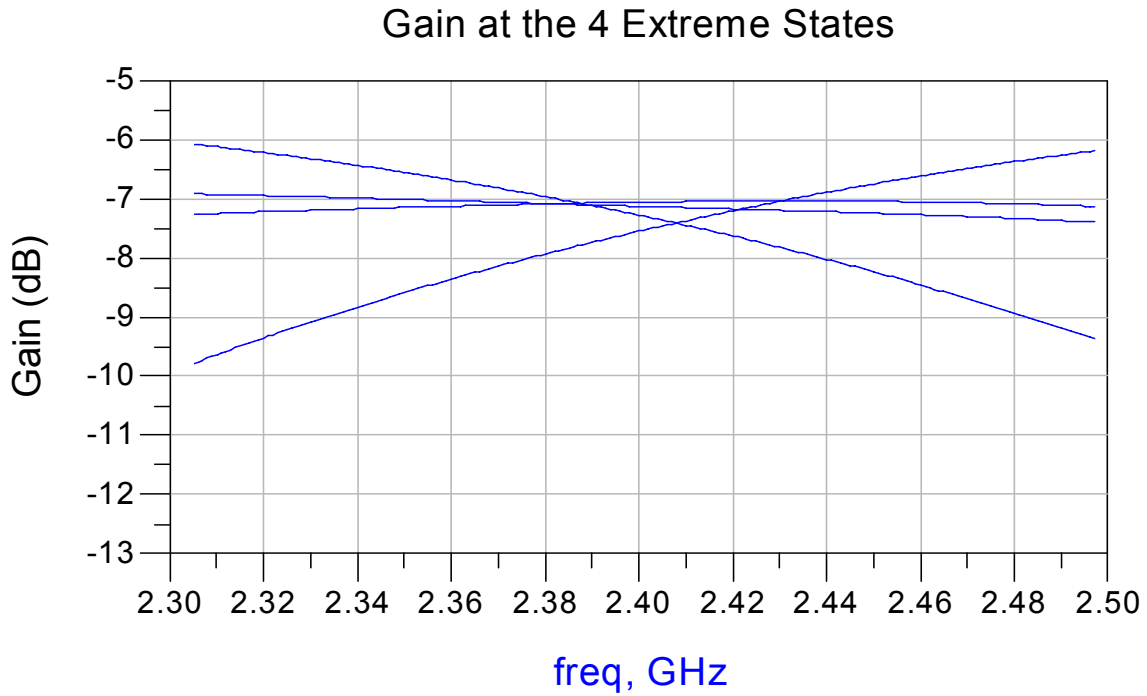
In the design of the vector modulator I ran three different simulations. One is a single 2.4GHz small signal S-parameter simulation to generate a constellation diagram. Two is a swept frequency small signal S-parameter simulation to check the loss and VSWR of the device. The third is a harmonic balance simulation to measure the output power.



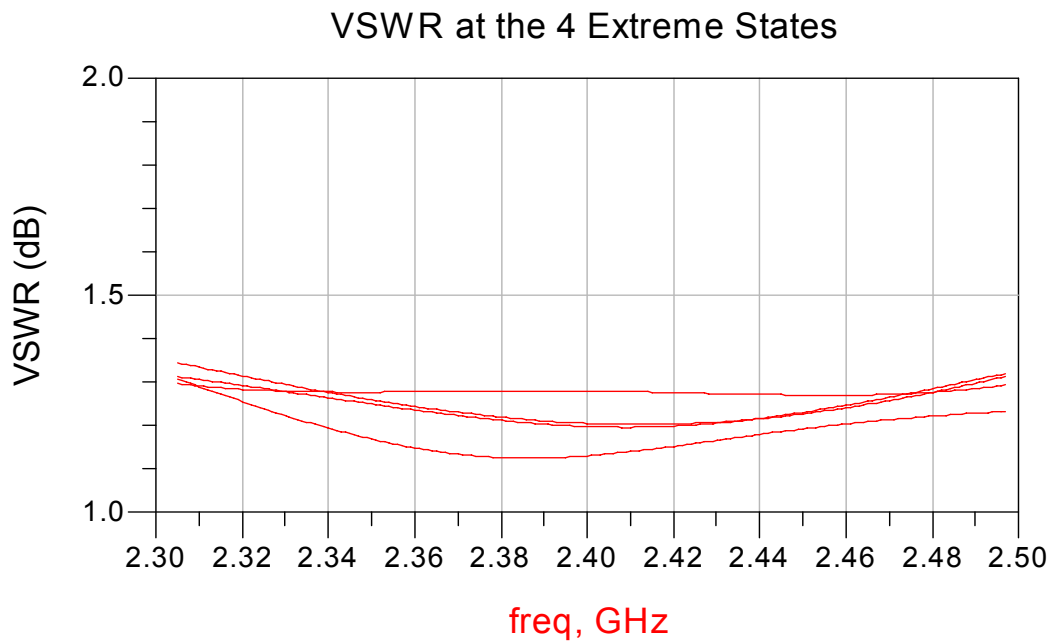
**Figure 4-1:** The constellation diagram shows the QPSK modulated output signal. Displayed is S21 on a polar plot at 2.4GHz.



**Figure 4-2:** Since the input to the I and Q ports is a DC voltage, any point inside the corners is possible.



**Figure 4-3:** The insertion loss of vector modulator plotted over frequency shows the amplitude slope when the transistors are at a high impedance state because of the capacitance. The greatest loss is less than 10dB, which is within the spec.



**Figure 4-4:** The VSWR of the vector modulator in all states is less than 1.4:1, which is better than the spec.

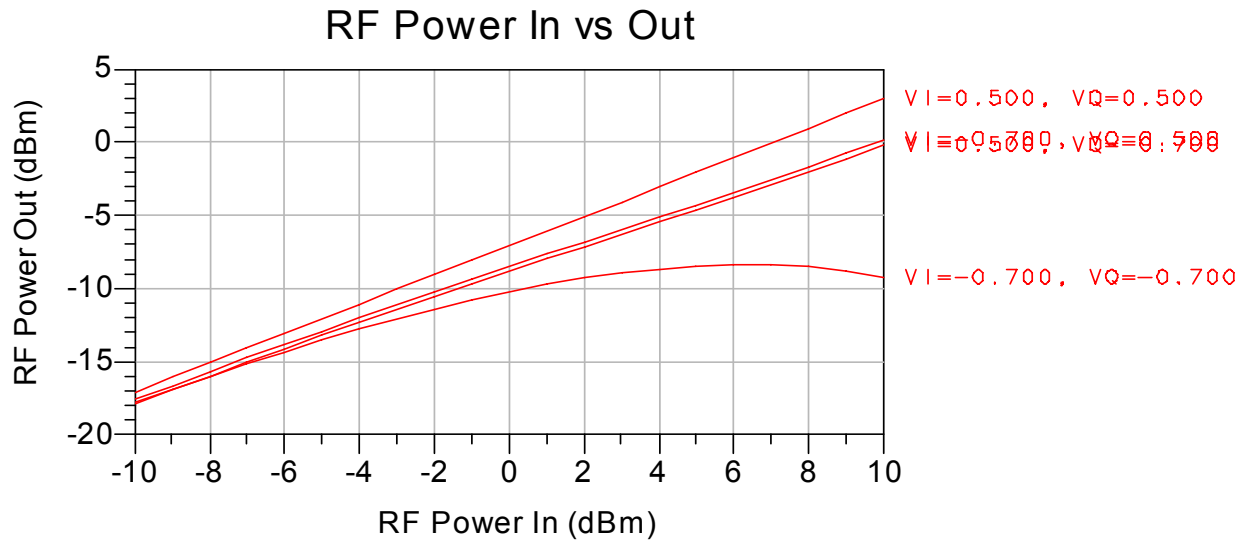


Figure 4-5: The vector modulator can handle an input power of 0dBm as stated in the spec. Only the I=-0.7V, Q=-0.7V case has any gain compression over this input range.

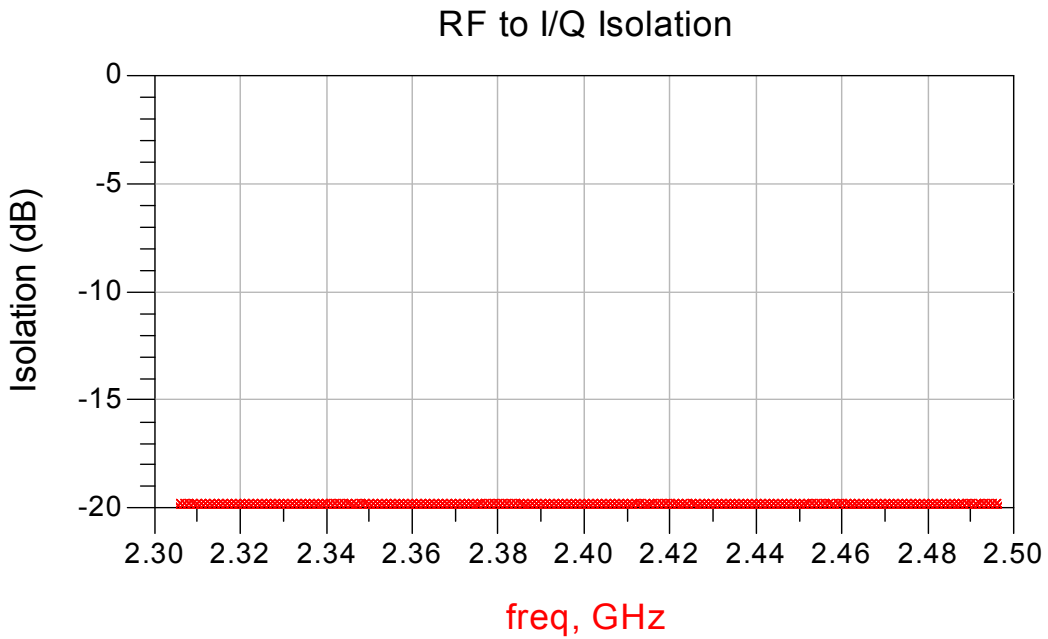
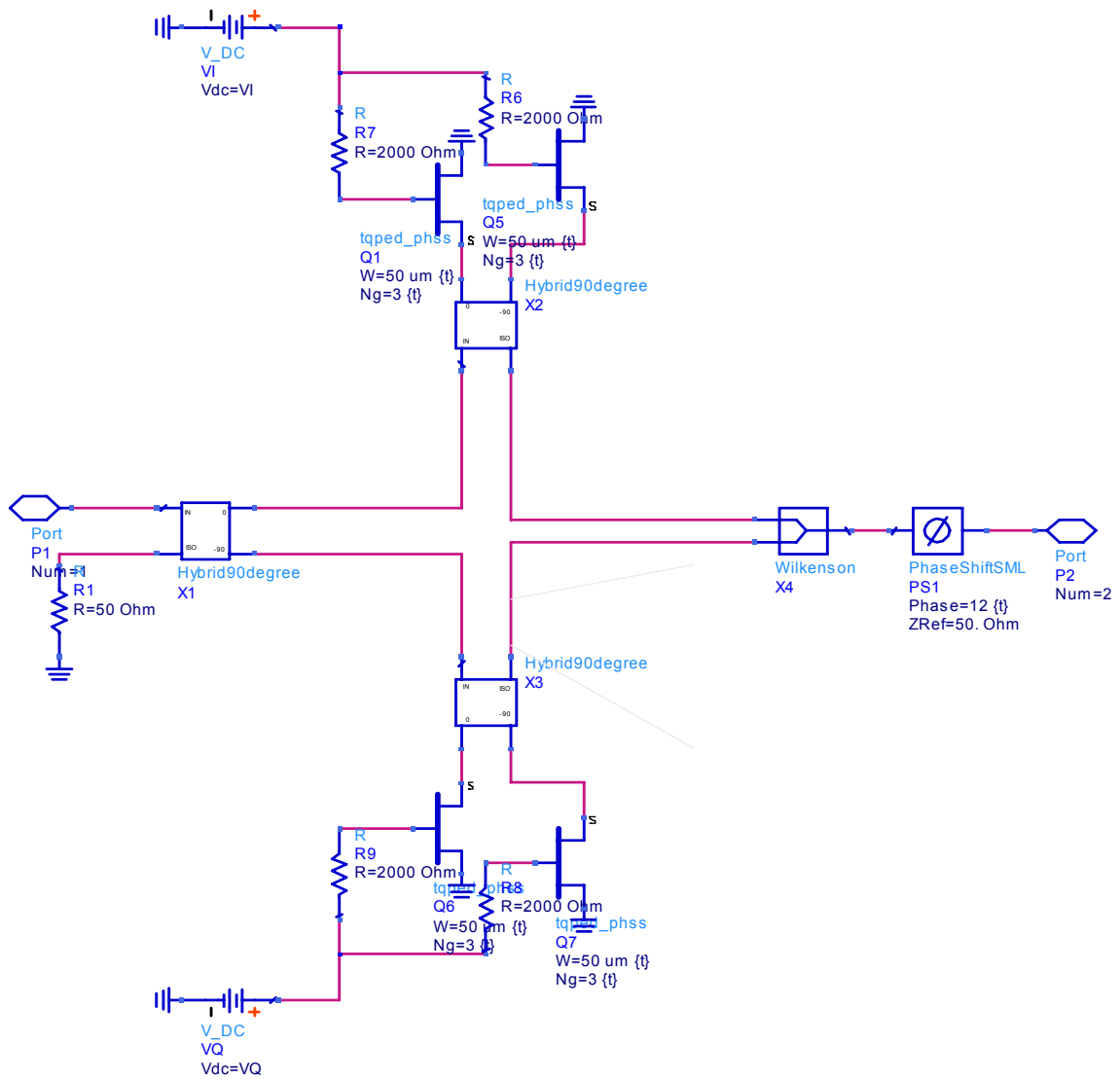


Figure 4-6: The RF to I/Q isolation is too high for ADS to calculate it. So it should be better than the spec of 16dB.

# 5. Schematic

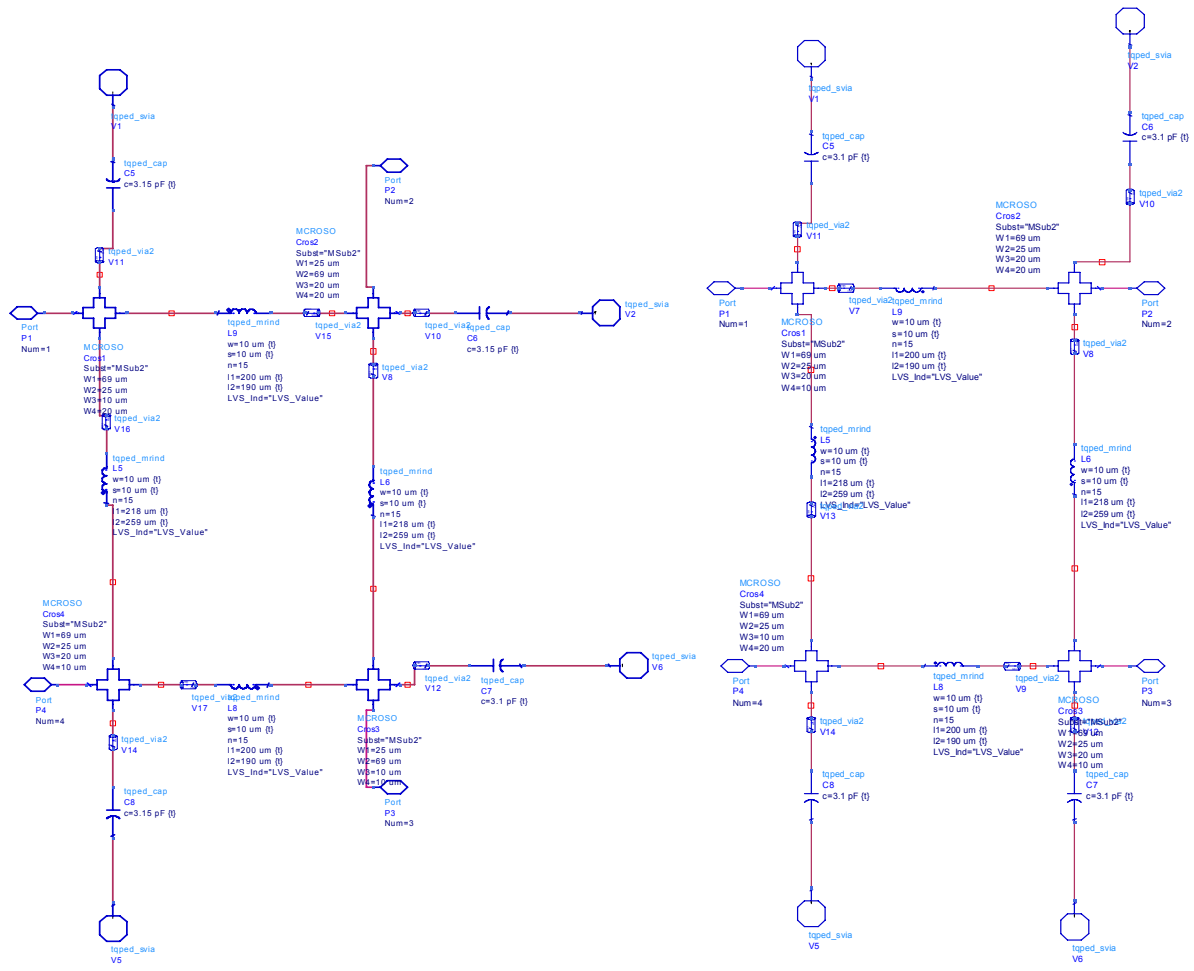
## Simple Schematic



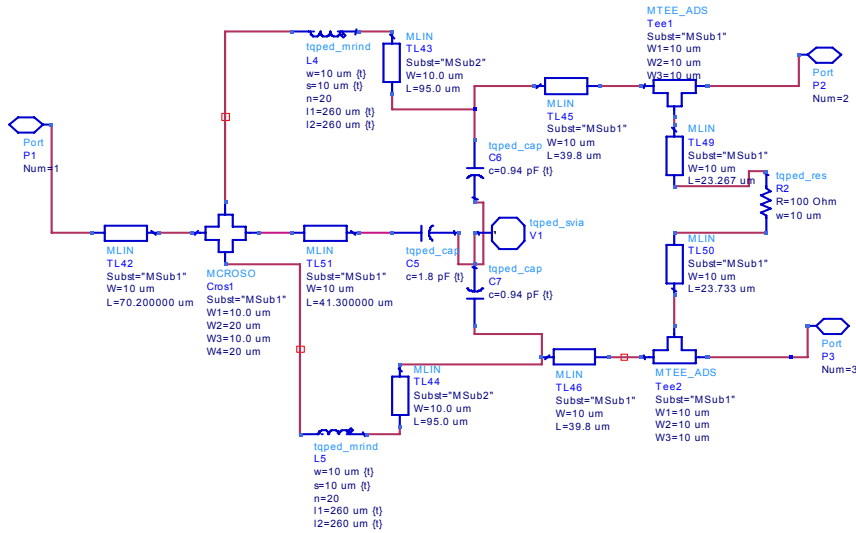


# Input 90° hybrid

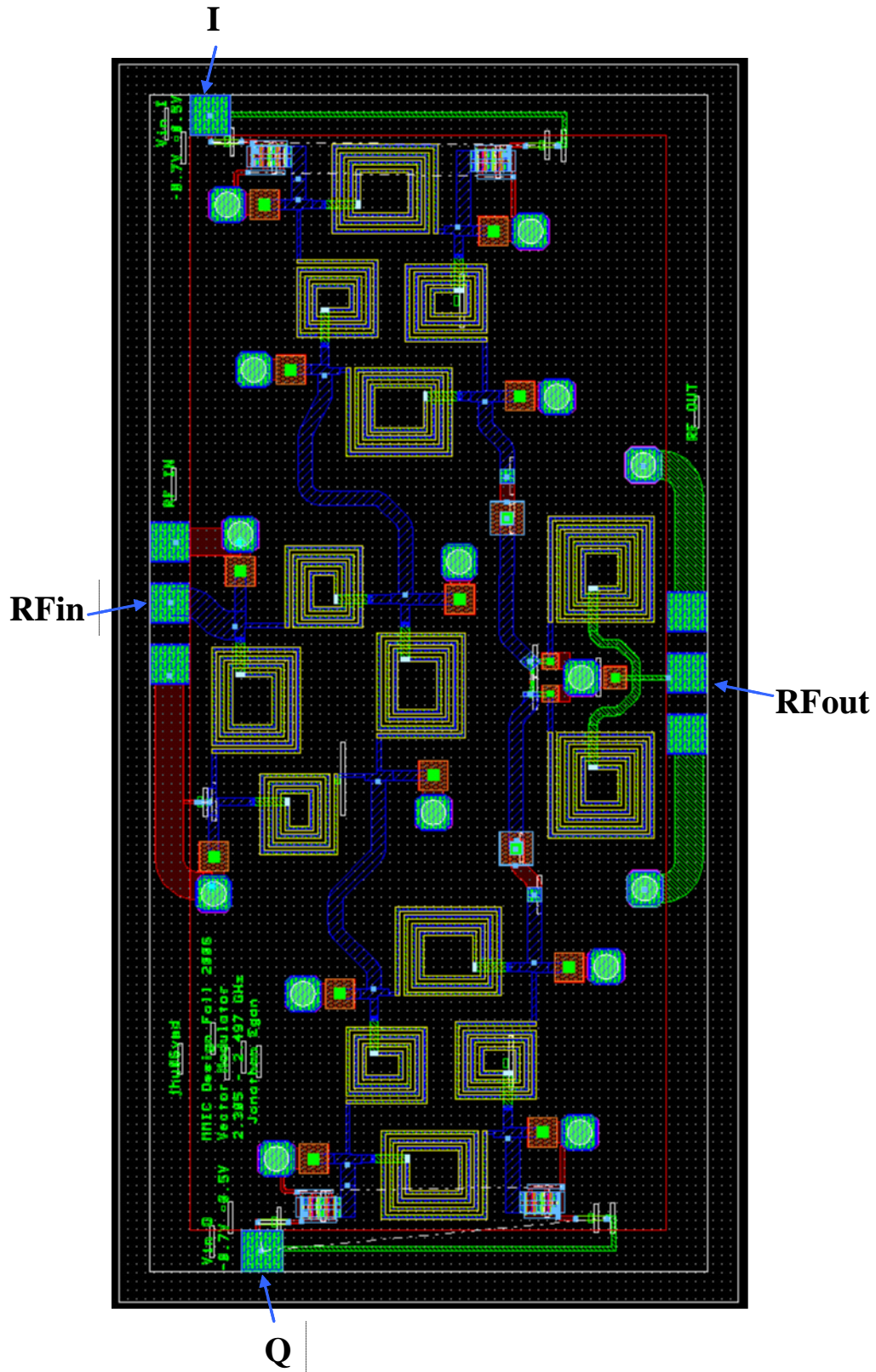
# Variable Attenuator 90° hybrid



# Wilkinson splitter



## 6. Layout





## 7. Test Plan

### 7.1 Equipment list

Vector Network Analyzer  
2 DC supplies

### 7.2 Test Procedure

- 7.2.1 Calibrate the network analyzer from at least 2.3 to 2.5 GHz with 201 points.
- 7.2.2 Set up the chip on the probe station using two GSG probes and two single pin DC probes. The placement of the probes is labeled on the layout see section 0.
- 7.2.3 Apply voltage to the I and Q ports using the table below. Other voltages, between +0.5V and -0.7V for either port, can be investigated.

Phase Table		
Voltage I	Voltage Q	Phase shift (degrees)
0.5	0.5	45
-0.7	0.5	135
-0.7	-0.7	-135
0.5	-0.7	-45

## **8. Summary and Conclusions**

The vector modulator described in this paper is capable of QPSK modulating a signal from 2.305 to 2.497 GHz. It makes use of FET transistors to vary the phase and amplitude of the signal. The I and Q inputs to the vector modulator range from +0.5V to -0.7V. The small size and frequency range should make this a chip an important component of an S-band wireless system.

## **9. References**

Penn, John E. "A Balanced Ka-Band Vector Modulator MMIC." *Microwave Journal*, June 2005.

# **MMIC Design of a Small Signal Amplifier**

**Cosburn Wedderburn jr**

**12/11/2006**

## **Abstract**

IN this design we are interested in developing a small signal amplifier (SSA). The design will encompass a two stage topology. Each stage will use 300um devices. The goal is to reach a gain 20dB. All design simulations will be accomplished in ADS 2005. In this paper there will be a step by step short discussion of the approach to the final design. Each stage will be discussed in detail. We will discuss the order of development for stage one followed by the development of stage two.

## **Introduction**

There is a need to create a small signal amplifier that will put of a gain requirement of 20dB. It appears that our single device is capable of delivering more that 20 dB of small signal gain. It appears that the first attempt at designing an SSA for 20dB would be to use a single stage to accomplish this task. We will discuss later on in the conclusion that it is not a good idea to squeeze the life out of one device. This SSA will use two stages. We arbitrarily use a 300um triquint device that we got from school. (in a real world application the device would be measured and characterized such that the small signal gain is obvious. To start the design, the device is biased with Vgs of -0.5v and Vds at 5v. See fig1 for IV curves.

## **Design Approach**

To start we simulate GMax of the 300um device. It appears that we can get more than enough gain for designing the first stage. A series RLC feedback network is inserted between the gate and drain to reduce the gain to a level of about 15 dB. See fig1b. In this attempt at lowering the gain, we realize that some gain will be lost when the stages are cascaded. The large resistor value (~700ohm) in the series RLC feedback helps control the level of the low frequency gain and stability of the device. See fig1c & fig1d. The there is also a resistor at the gate of stage one device. This resistor helps with stability as well as raising and lowering the high end gain. Observing figure 1d we clearly have enough gain in our frequency band of interest (10dB). Our next step is to design the matching networks.

Looking at the device drain impedance we see approximately  $56+j44\text{ohm}$ . We want to match to the conjugate or  $56-j44\text{ ohm}$ . Observing the location of the drain impedance on the smith chart we can match the drain to 50 ohm with a series inductance and some shunt capacitance. See fig 2a.

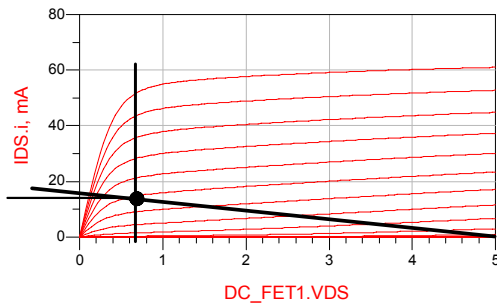


Fig1a

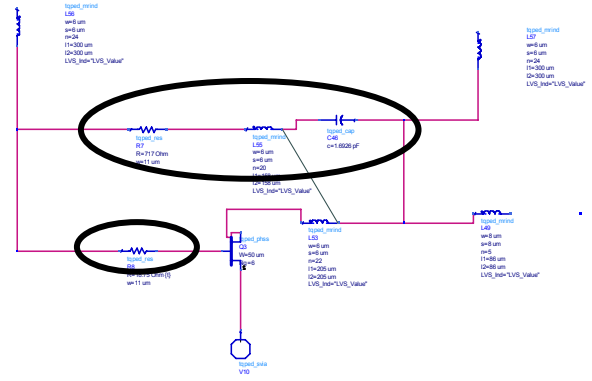


Fig1b

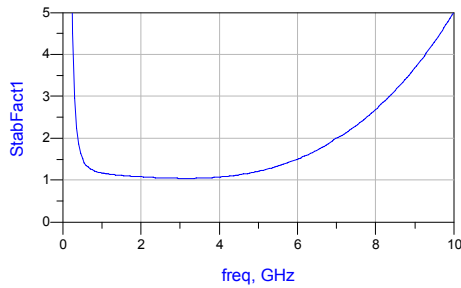


Fig 1c

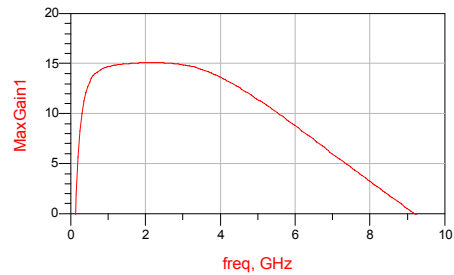


Fig 1d

The results of the series inductor can be shown in the figure below.

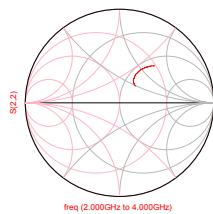


Fig 2a

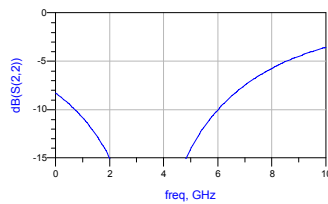


Fig2b

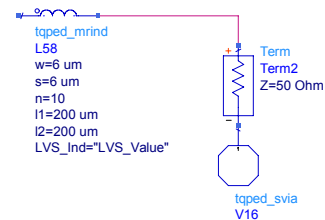
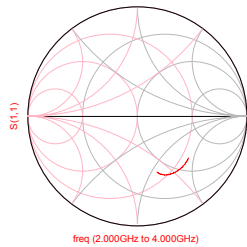
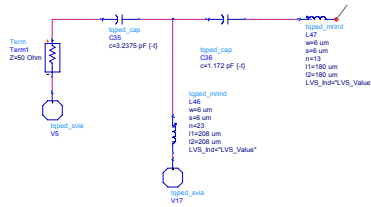


Fig2c

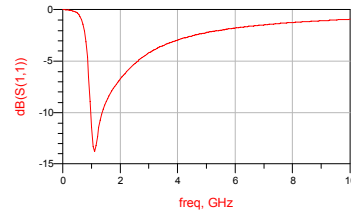
We are now interested in matching the input of our device to 50 ohm. The impedance of the gate with the feedback and stability resistor attached reads 39.7-j67ohm. See fig3a.



**Fig 3a**

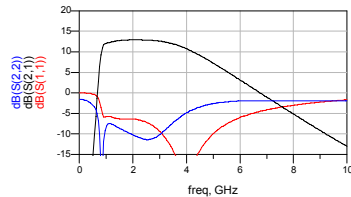


**Fig3b**

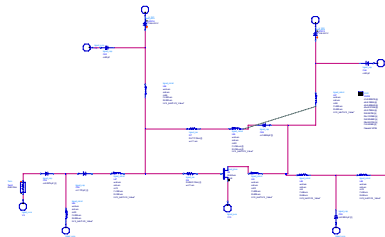


**Fig3c**

The conjugate impedance transformation from the gate to 50ohm can be accomplished with a series inductor and capacitor and some shunt capacitance. See fig3b. The response of the first single stage amplifier is showed in fig 4a and fig 4b.



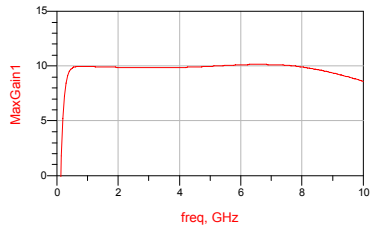
**Fig 4a**



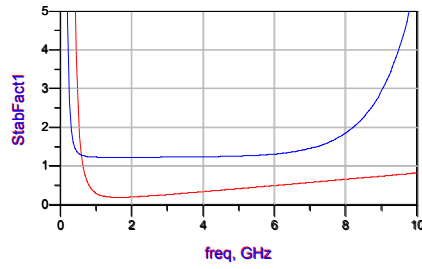
**Fig4b**

This first stage has a gain of approximately 12~13dB and bandwidth of 2-4GHz. At first glance the response of input and output matching networks appears to need tuning. Since the second stage will be cascaded the elements of the matching networks will be optimized as a last step. The first stage OMN needed two additional elements to facilitate the impedance match to the second stage. At this point we will begin the design of the second stage.

The second stage is treated like a new single stage amplifier design. The device is biased at the same bias points as stage one. A series RLC feedback network is employed in the second stage also. The feedback network for the second stage is used to lower the gain further to approximately 10dB. The shape of the response of the entire two stage cascaded amplifier is governed by the second stage device. The resistor in this feedback network is approximately 265ohm which lowers gain more than the 700ohm resistor in stage one feedback. There is also a series resistor at the gate of device 2. Resistor is added to the gate as an initial attempt to stabilize the device. It is observed that the resistor also helped flatten the gain response at the high end when tuned (looking at Gmax). The stability in this design is primarily controlled by the feedback. In the plot below shows the device with out any stabilizing network. Adding an RLC feedback network between the gate and drain stabilizes the device. Observing figure 5b we can see the effects of the feedback on stability.

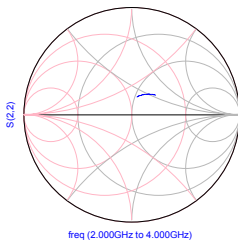


**Fig5a**

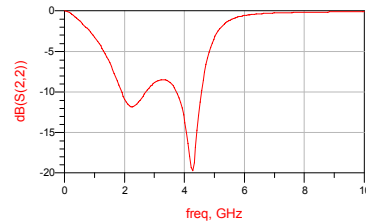


**Fig5b**

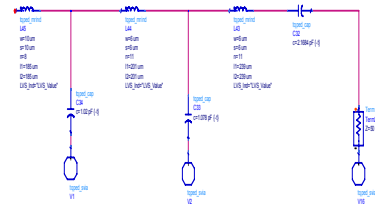
In designing the matching networks for stage two we follow the same procedure for stage one. The impedance is observed at the gate and drain of the device. Looking at the drain of the device the impedance is approximately  $59 + j23.6$  ohms. The impedance necessary to transform the device drain to 50 Ohms can be in any combination of series inductors/ capacitors, shunt caps/inductors.



**Fig6a**

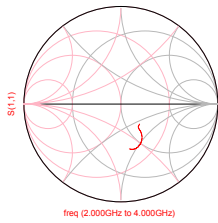


**Fig6b**

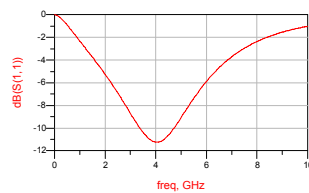


**Fig6c**

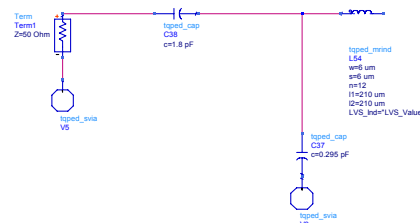
In this approach I chose a low pass configuration that transforms the conjugate of the drain to 50ohms. At this point the impedance at the gate is observed to read  $58 + j46$  Ohm. This impedance can be viewed in fig 7a below on the smith chart.



**Fig 7a**

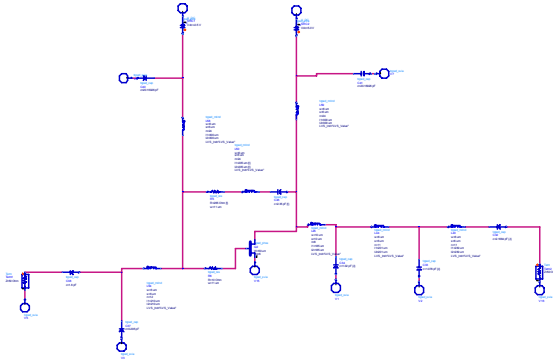


**Fig 7b**



**Fig 7c**

To transform the conjugate of this impedance to 50ohm, a series inductance and shunt capacitance is used. The single stage as well as the results is shown in figure 8a and figure 8b. At first glance we can see that the total gain between stage one and stage two will give us the gain and bandwidth that we need.

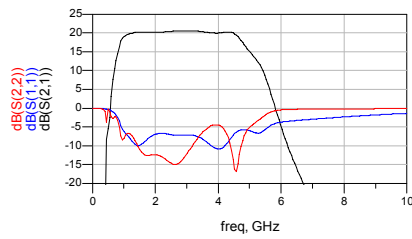


**Fig 8a**

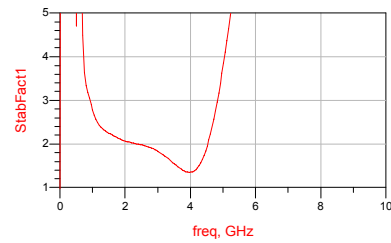


**Fig8b**

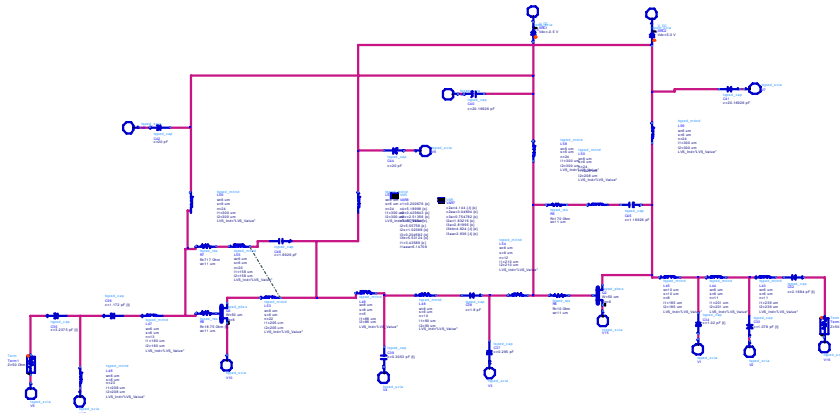
In order to meet our design specification the stage one and stage two amplifiers are cascaded. The final two stage circuit is optimized to improve on the overall response.



**Fig 9a**

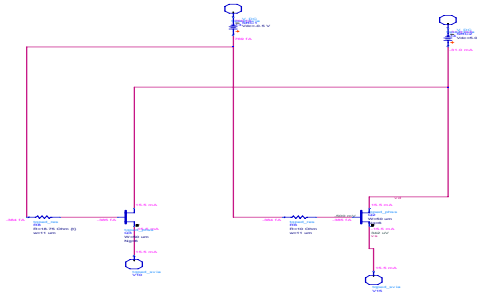


**Fig 9b**

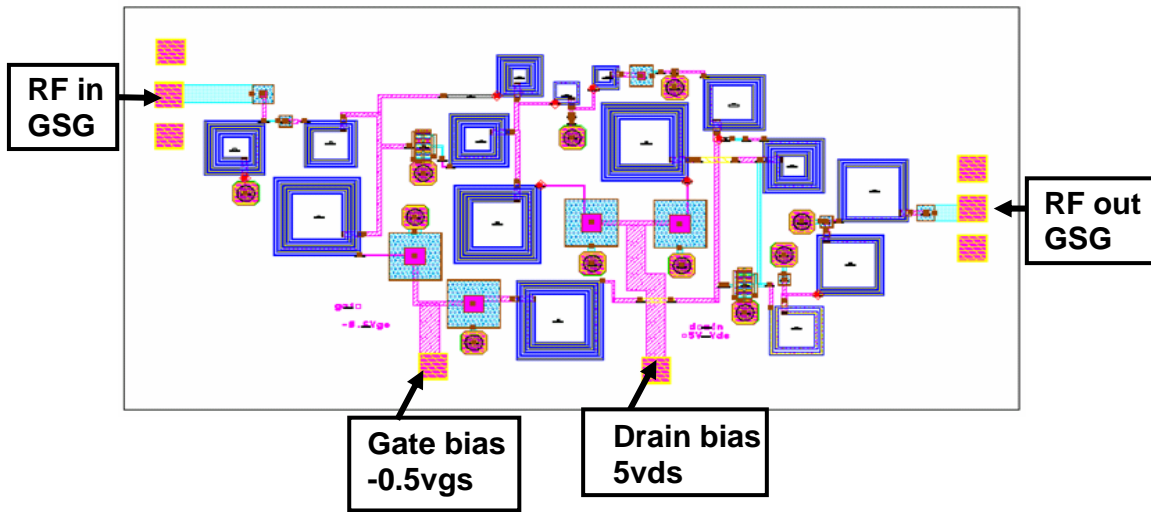


**Fig 10**





DC schematic



Layout

**Test Plan**

RF testing 100 MHz to 10GHz 100MHz steps  
 S11, S12, S21, S22

DC Bias  
 Vds 5V  
 Vgs -0.5V

In summary, we designed an SSA with a small signal gain of 20dB. Each stage is designed individually and integrated into one amplifier. The input and output return loss could be better. The trade-off is the bandwidth.

In conclusion, there were a few lessons learned in the design of the SSA of which only the most important one will be discussed here. One important consideration is that it is easier to use two devices instead of one device when maximum gain as well as bandwidth is important. This design we were successful in meeting the design requirements for a two stage SSA.