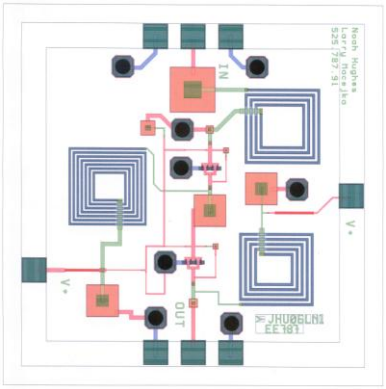
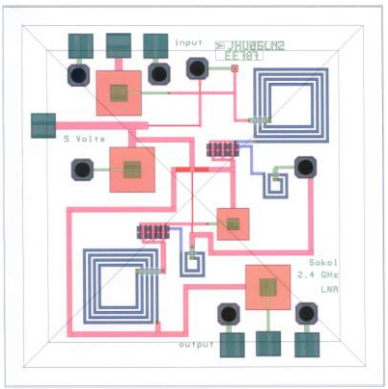
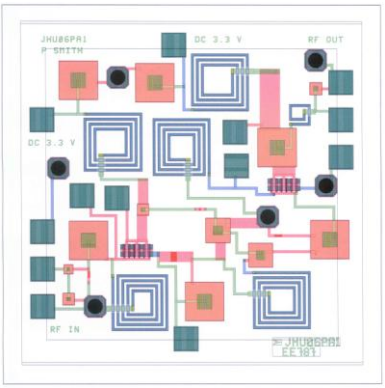
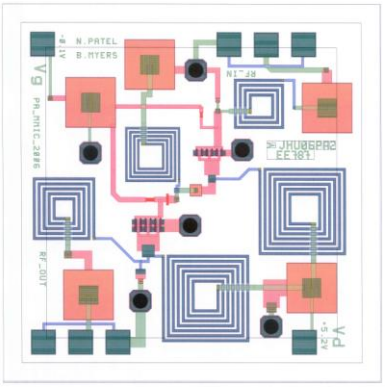
# Fall 2007 JHU EE787 MMIC Design Student Projects
## Supported by TriQuint, and Agilent Eesof
## Professors John Penn and Dr. Michel Reece

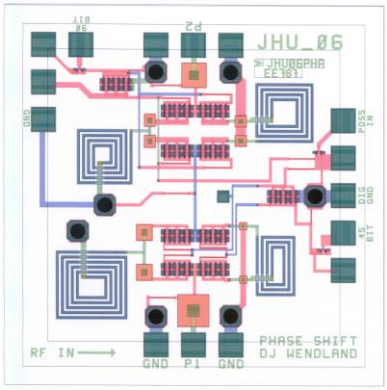
Low Noise Amplifier C-band—J. Olah & B. Wallace
Phase Shifter – Alan Yu
Mixer S-Band – John Tinsley
Power Amplifier C-band – J. Treadway & Syed Ali
Broadband Amplifier – Jeremy Stampfly
Low Noise Amplifier S-band-E. Simcoe
Mixer C-Band – Alex Mendes
Power Amplifier S-band – D. Kenney
Vector Modulator C-band– Shawn Seman

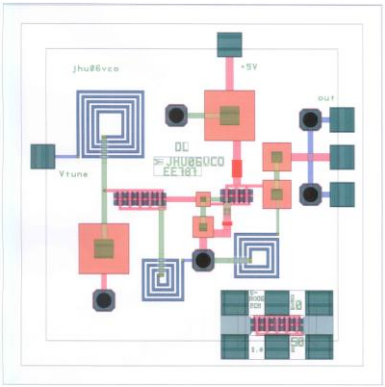


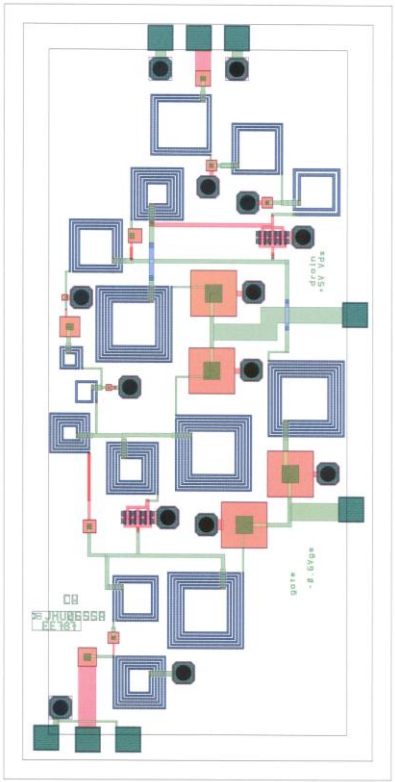



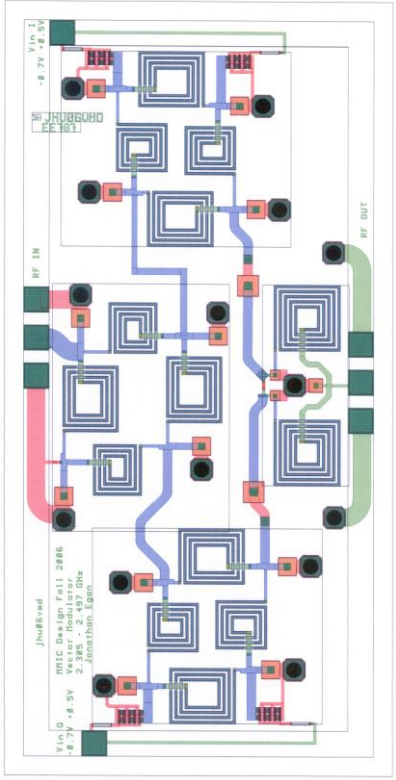



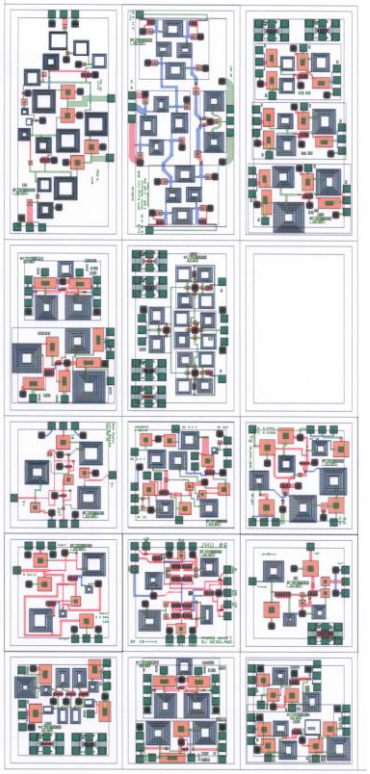




**EE 525.787 – Monolithic Microwave Integrated Circuit (MMIC) Design**
**Engineering and Applied Science Programs for Professionals**

**Instructor: John Penn**

# Design of a C-Band Low Noise Amplifier (LNA) GaAs Monolithic Microwave Integrated Circuit (MMIC)

**Jack Olah  William W. Wallace**

**Fall 2007**

# Table of Contents

## Abstract

LNA's are usually used as the front end of a receiver system. The purpose of an LNA is to amplify the weak signals that are received. It is usually located at the focal point on the antenna, so it can receive and amplify the weak signals so they can overcome the system losses of the receiver. The LNA must have the lowest noise, so it doesn't add noise to the microwave system. The purpose of this design is to design, simulate, layout, and test a two-stage GaAs MMIC LNA, which will operate in the C-band. We will use a GaAs substrate as part of the TriQuint Semiconductor's TQPED process for the MMIC fabrication.

## Introduction

This LNA was designed to operate on low DC power. One of the primary objectives of this project was that the MMIC was intended to operate on battery power—typically 3.0 to 3.6 V, and to operate in the HiperLAN wireless local area network (WLAN) and industrial, scientific, and medical (ISM) frequency range (from 5150 to 5875 MHz). A DC battery power of +3.3 volts was chosen for VDS, and a frequency of 5500 MHz was chosen because it is in the middle of the C-band range. This LNA design consists of two similar stages with a matching network to separate the two stages. The LNA receives a 5.5 MHz input signal and passes it through the IMN to the gate of the 50 um E-mode FET. Each E-mode FET has a smaller 24 um D-mode FET on the Drain to supply current to the FET. The E-mode FETs are biased using a voltage divider network on the gate. The output of the first stage is sent to an intermediate matching network. This intermediate matching network acts as an OMN of the first stage and the IMN for the second stage. The signal is then amplified again with the second stage and passed through the OMN as RF OUT. The entire LNA was designed (schematic, simulation, and layout) using Agilent's Advanced Design Suite (ADS). The final schematic used all TriQuint components. The MMIC will be fabricated using the TriQuint TQPED Process (with vias) on a 4 mil (100 micron) thick wafer and will fit on a 60 x 60 mil ANACHIP die.

## Design Approach

The initial decision that had to be made was to determine the battery power required and the size of the FETs to meet the DC power requirements of the project. Next, the Noise Figure circles and the Gain circles were plotted on the Smith chart. A tradeoff between minimum NF and maximum gain was determined. Since this design is a two-stage low noise amplifier, the NF of the first stage essentially determines the overall NF; therefore, the NF of the first stage needed to as low as possible. The stability of the FET had to be checked. It was determined to add a stabilizing resistor to the output, to avoid amplifying additional noise. From here, the IMN could be designed. Finally, S22* of the first stage could be determined and matched to S11 of the second stage. Up to this point, all of the components have been ideal components. The next phase is to incorporate the TriQuint capacitors, resistors and inductors and compare the simulation results with the ideal components; retune the design if necessary. Create the layout, and then add the MLIN to compensate for the line lengths of the traces.

## *Specifications vs Goals*

The goal of the C-band Low Noise Amplifier is to use small PMode PHEMTs (<50 microns) to achieve at least 20dB of gain, with a maximum NF of 3 dB and a goal of a 2dB NF. Ideally, it should consume no more than 5 mW per stage; however, it can have a specification of 10 mW per stage. Since the DC power criteria of this LNA is very low power, each FET should be biased at IDSS/4 and 1.0 to 2V VDS to achieve some gain.

*The goals of this Low Noise Amplifier are as follows:*

| Parameter | Specification | Goal |
|---|---|---|
| FREQUENCY RANGE | 5512.5 MHz | 5150 to 5875 MHz |
| BANDWIDTH (S21) | 1GHz | > 800 MHz |
| GAIN | 24.25 dB | > 20 dB |
| DC POWER CONSUMPTION | 35 mW | 10 mW/stage; 5 mW/stage, goal |
| NOISE FIGURE | 2.692 dB | < 3 dB; 2 dB, goal |
| INPUT IP3 | -5dBm | > 0 dBm |
| VSWR, 50 Ohm | | < 1.5:1 |
| SUPPLY VOLTAGE | +3.3 Volts | + 3.3 Volts only, goal (3 to 3.6V range) |
| SIZE | 60 x 60 mil ANACHIP | 60 x 60 mil ANACHIP |

## *Tradeoffs*

Because this is a battery powered LNA, the size of the FET must be appropriate for the DC power requirement. Since this is a LNA, there is the fundamental tradeoff between minimum Noise Figure with the most gain. FET stability must also be considered while performing the tradeoff between minimum NF and maximum gain. The FET should be stable across the operating band, to avoid oscillations within the operating band.

## *Simulations*

## Linear Simulation

| index | Vs | ...ource.SP_DCOP.Power |
|---|---|---|
| 1 | 3.300 | -0.035 |

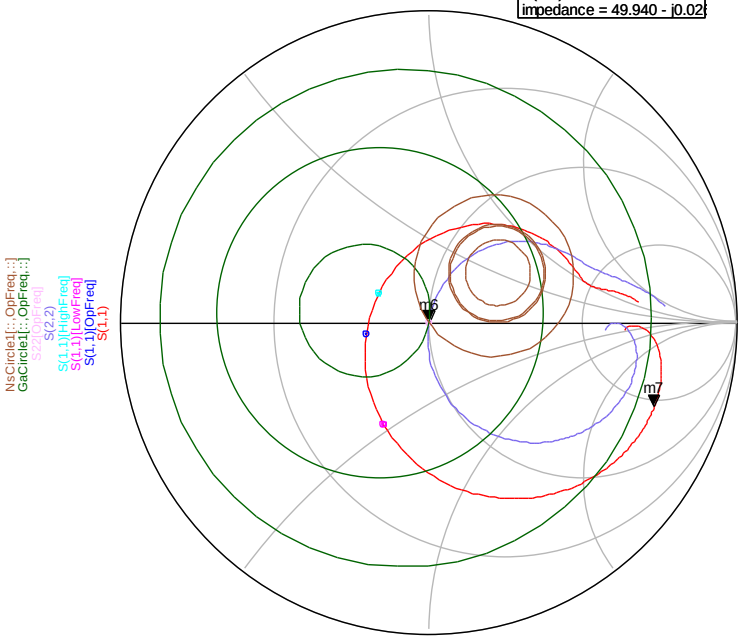
Entire LNA Power Consumption

| Zin1[OpFreq] | Zin1[LowFreq] | Zin1[HighFreq] |
|---|---|---|
| 33.003 - j2.703 | 38.316 / -36.742 | 36.053 / 10.753 |

| S(2,1)[OpFreq] | S(1,1)[OpFreq] | S(2,2)[OpFreq] |
|---|---|---|
| 24.251 / 80.846 | -13.671 / -169.099 | -63.653 / -156.189 |

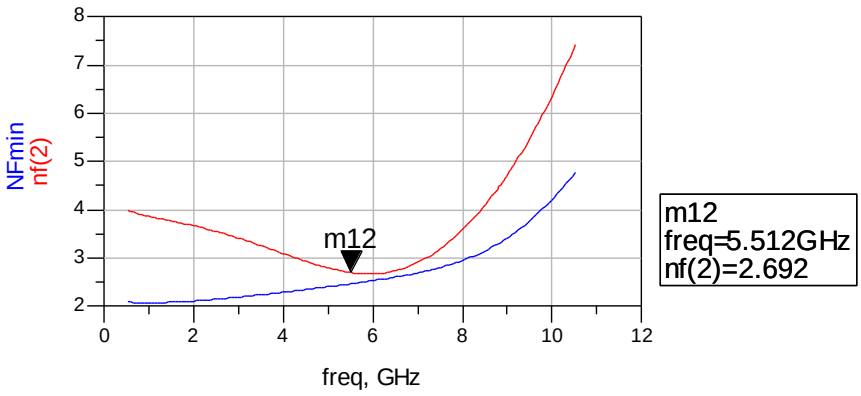
| NFmin[OpFreq] | nf(2)[OpFreq] |
|---|---|
| 2.464 | 2.692 |

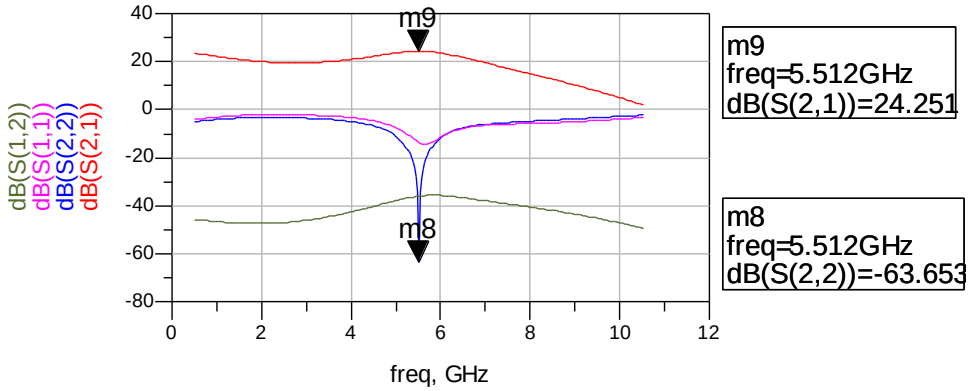
m6
freq=5.512GHz
S(2,2)=6.567E-4 / -156.189
impedance = 49.940 - j0.02

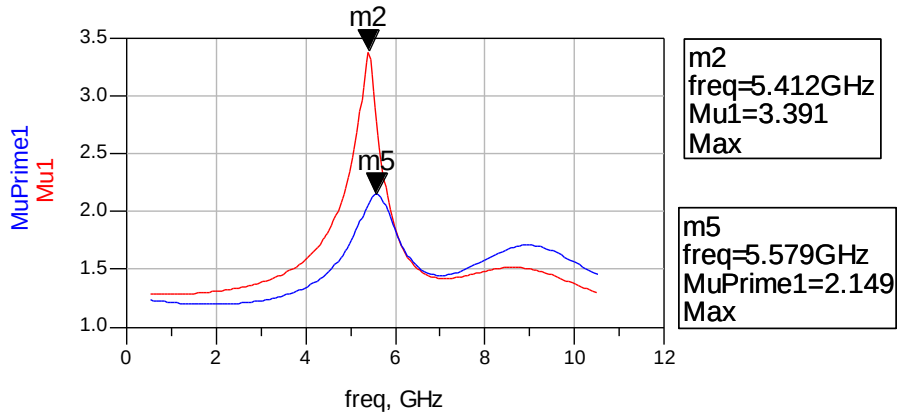



freq (512.5MHz to 10.51GHz)
(0.000 to 0.000)
cir_pts (0.000 to 51.000)

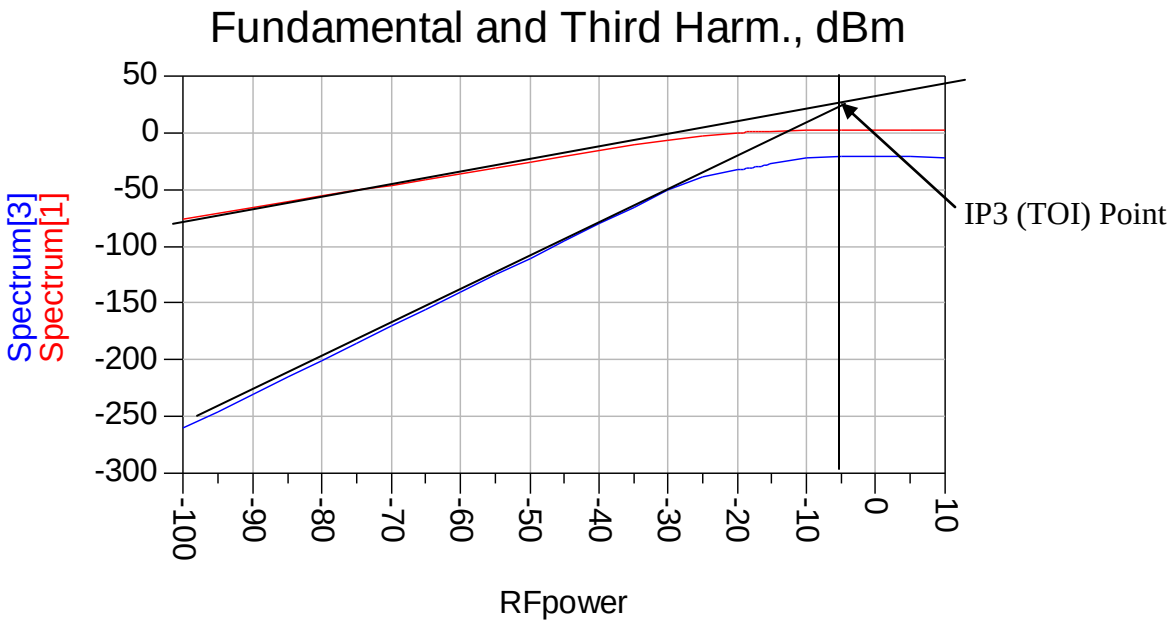
m7
freq=2.41250GHz
S(1,1)=0.77874 / -20.20443
impedance = 135.905 - j185.75


NFmin
nf(2)
m12
freq=5.512GHz
nf(2)=2.692
freq, GHz


dB(S(1,2))
dB(S(1,1))
dB(S(2,2))
dB(S(2,1))
m9
m8
m9
freq=5.512GHz
dB(S(2,1))=24.251
m8
freq=5.512GHz
dB(S(2,2))=-63.653
freq, GHz


MuPrime1
Mu1
m2
m5
m2
freq=5.412GHz
Mu1=3.391
Max
m5
freq=5.579GHz
MuPrime1=2.149
Max
freq, GHz

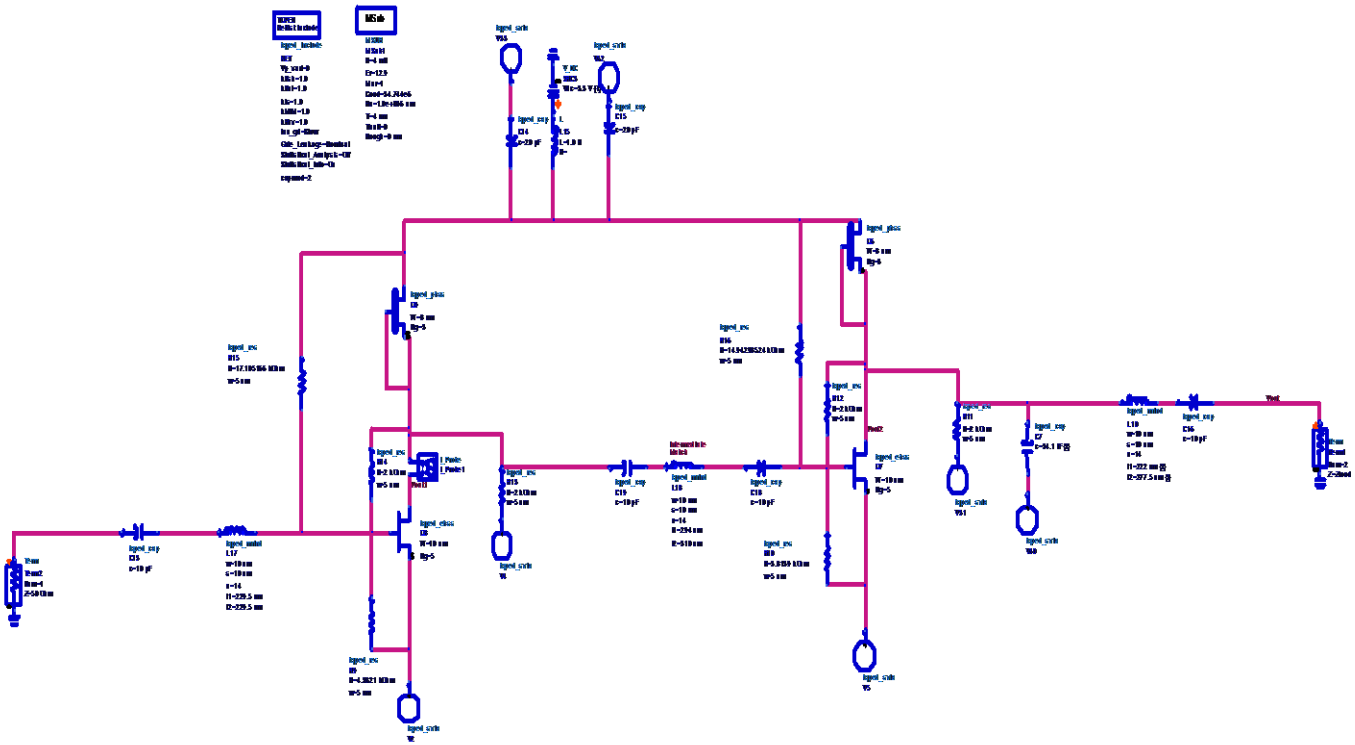
**Non-Linear Simulation**
**IP3**



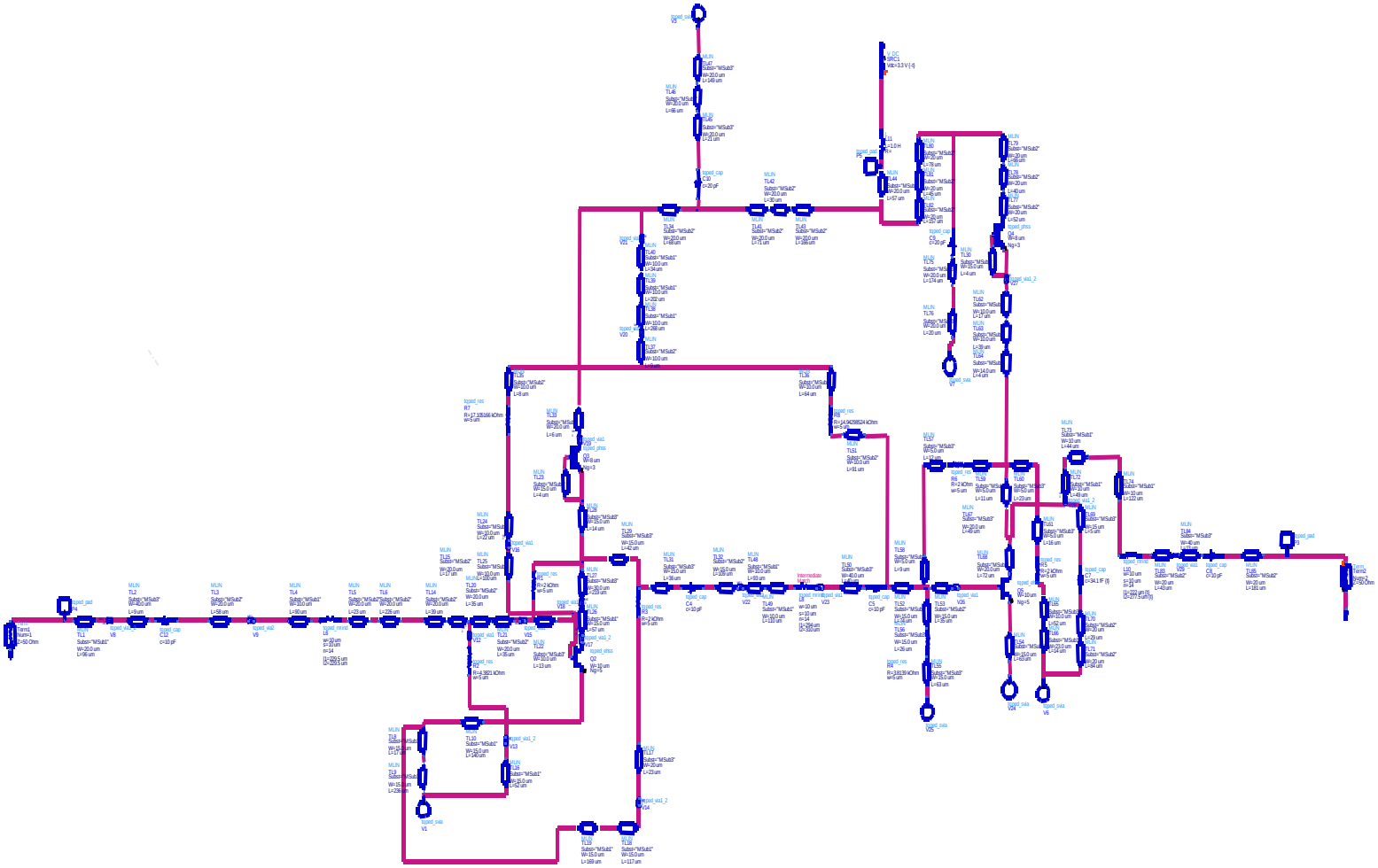

IP3 (TOI) I/O levels: Input power level = -5dBm & Output power level = ~25dBm.

## Schematic

RF (without MLIN)

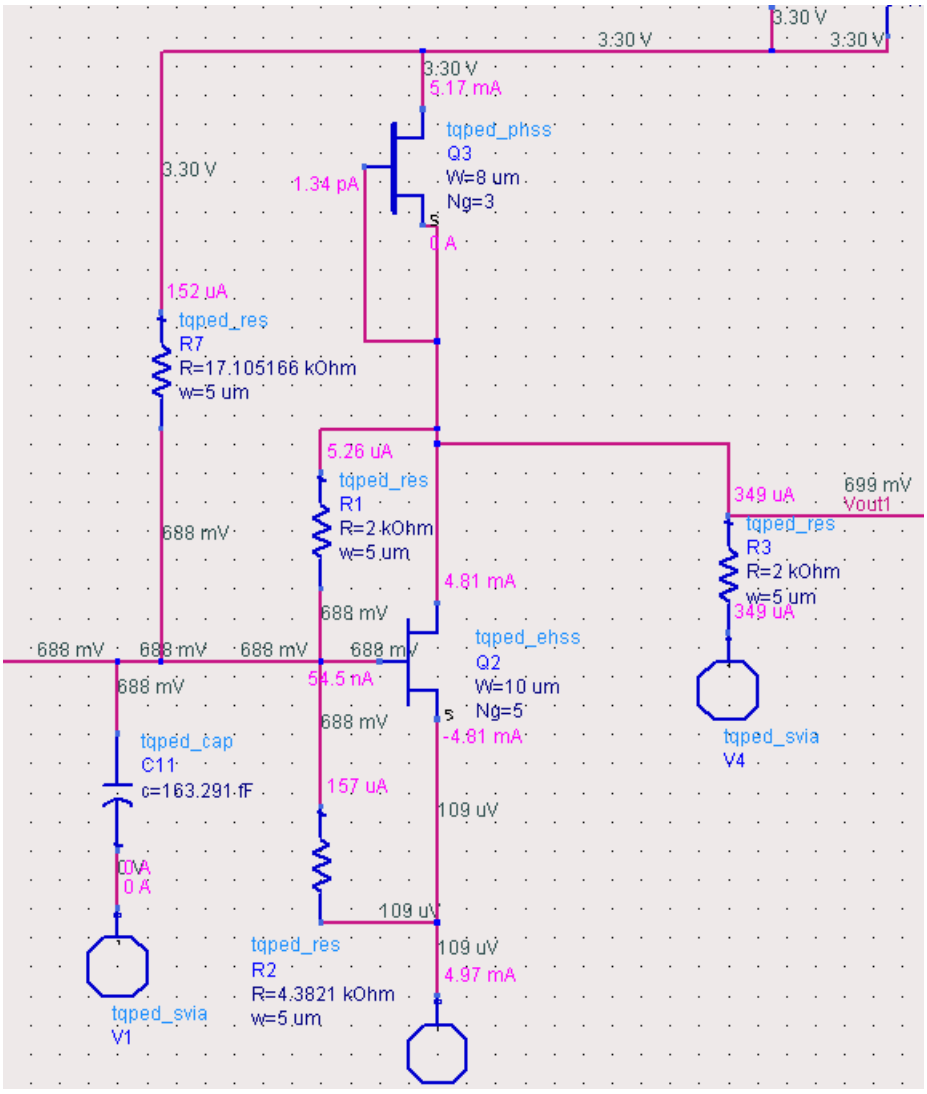


RF (w/MLIN)



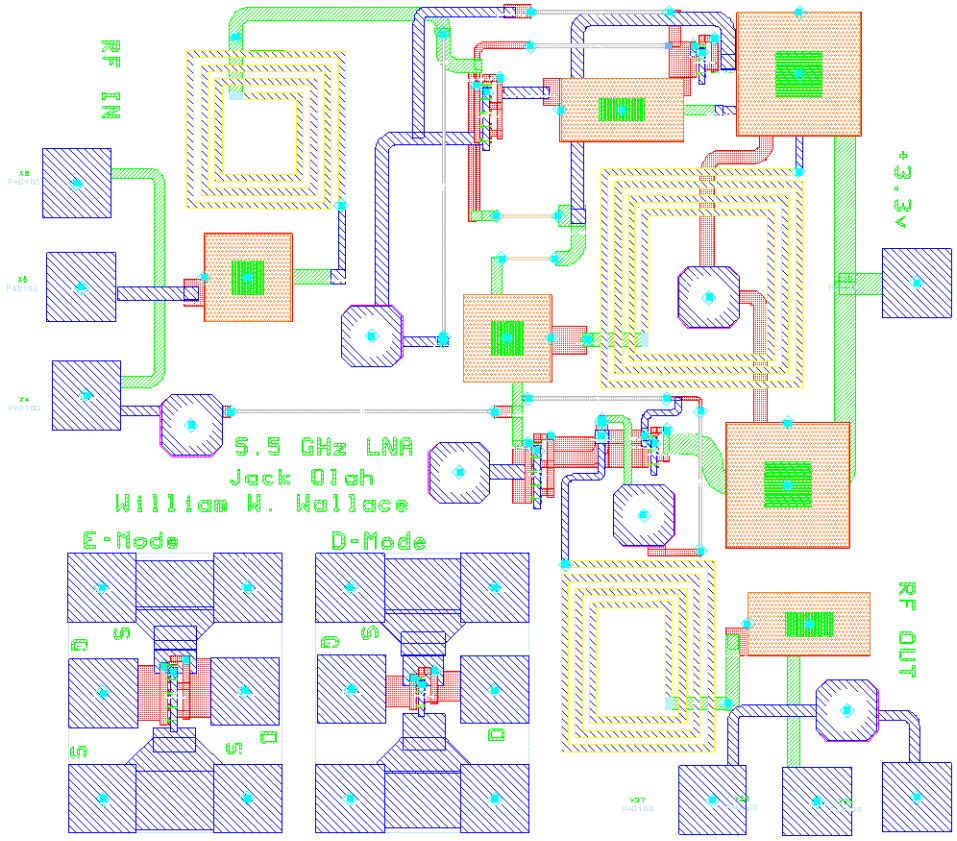
**DC Annotation**

Note: Only one stage is shown because the FETs are essentially identical for each stage.

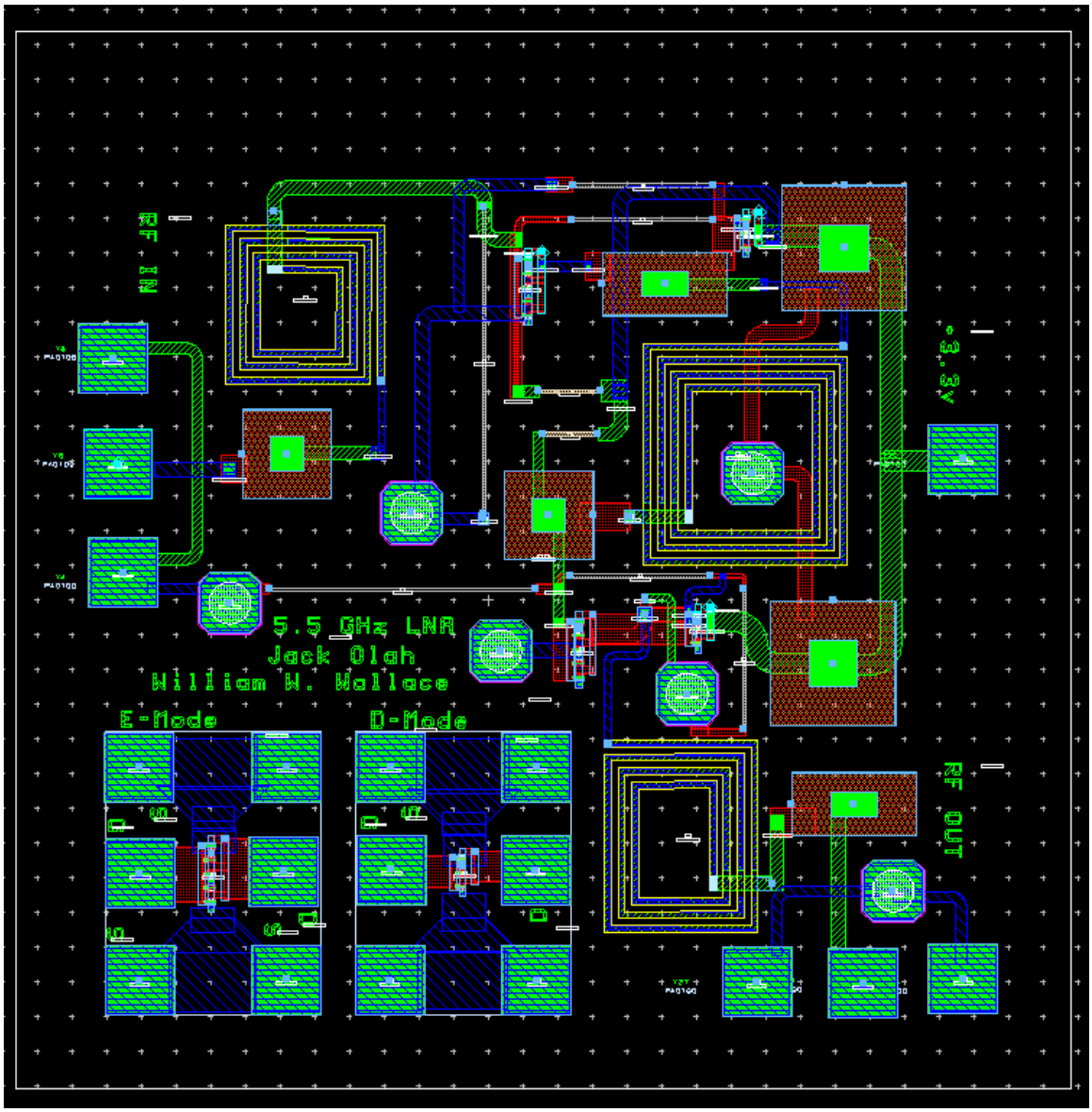


## Layout

*Plot of layout*



*Screen shot of layout*




## Test Plan

Since the MMICs will not be available for a few months after the class has ended, the testing phase of the project cannot begin until that time. The C-band LNA will be tested using an Agilent 8510 (45 MHz to 26 GHz) Vector Network Analyzer (VNA), a Cascade Model 43 wafer probe station with up to 4 RF probes (GSG), 4 DC needle probes, synthesized signal generators (26 GHz), a Noise Figure meter, and an 18 GHz Spectrum analyzer. This test plan should be used as a guide for testing, not as an official test procedure.

**Turn On Procedure**
To protect the design from excessive current draw due to possible layout errors or defects, set the current limit of the supply to twice the nominal current pull. Increase the drain voltage of the DC supply slowly up to the required +3.3V (VDS) operating voltage. Record the current draw off the power supply

**RF Measurements**

**S-Parameter Measurements**
The VNA must be calibrated prior to making any measurements; however, the VNA in the lab as probably been calibrated at the beginning of the lab. After calibrating the VNA, connect the RF and DC probes up to the LNA. Make the measurements of S11, S21, S12, and S22.

**Noise Figure Measurements**
Once again, calibrate the noise figure test set. Connect the input probe to the RF IN pad. Connect the output probe to the RF OUT pad. Measure the noise figure of the LNA and store the measurement data.

**IP3 Measurements**
Set the test bench for two tones. Start with the power levels set to a low level, i.e. –30 to –20dBm. Using a spectrum analyzer, increase the power levels of the two tones and look for the third order products. Record the delta between the third order products and the fundament tones – these are the third order intercept (TOI) values.

## Summary & Conclusions

Overall, the design meets the key requirements proposed in the project objectives. The gain and NF are relatively constant across the specified operating band. The LNA simulation yielded a gain (S21) of 24dB, an S22 of –63dB, an S11 > -10dB and a NF of 2.7dB at the center frequency. It uses about 35mW of power from the 3.3V source for the entire design. Unfortunately, this LNA consumes 15mW more power than the specification of 20mW (10mW/stage, two stages).

This report described the design, simulation and layout of a two-stage GaAs MMIC low noise amplifier, operating at C-band from 5.150 to 5.875 GHz as the initial amplification section of a wireless communications (WCS) transceiver system. The low noise amplifier design was a class project for Johns Hopkins University's MMIC Design Course (525.787), Fall 2007. The GaAs process used was TriQuint Semiconductor's TQPED process on a 4 mil (100 micron) GaAs substrate.

# THREE BIT PHASE SHIFTER

MMIC Project Final Report

EE525.787 Fall 2007

By Alan Yu

12/10/07

**Abstract**
A three bit phase shifter was designed for frequencies 2.305 GHz to 2.497 GHz, with delay bits of 45, 90, and 180 degrees. Each delay bit is switched between reference and delay using two control lines, either -2V and 0V, to shut off and turn on a path, respectively. Depletion, or D mode, FETs were used for switching. The circuit was fit into a 60 mil x 60 mil GaAs chip, to be fabricated by TriQuint Semiconductor Inc.

**Introduction**
A three bit phase shifter has been designed for the John Hopkins University Fall 2007 MMIC design class, EE525.787. The phase shifter was designed as a part of an S-band duplex transceiver, and is used in the receive mode, as depicted in Figure A. The frequency band of interest falls between 2.305 GHz to 2.487 GHz, which covers the wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies.

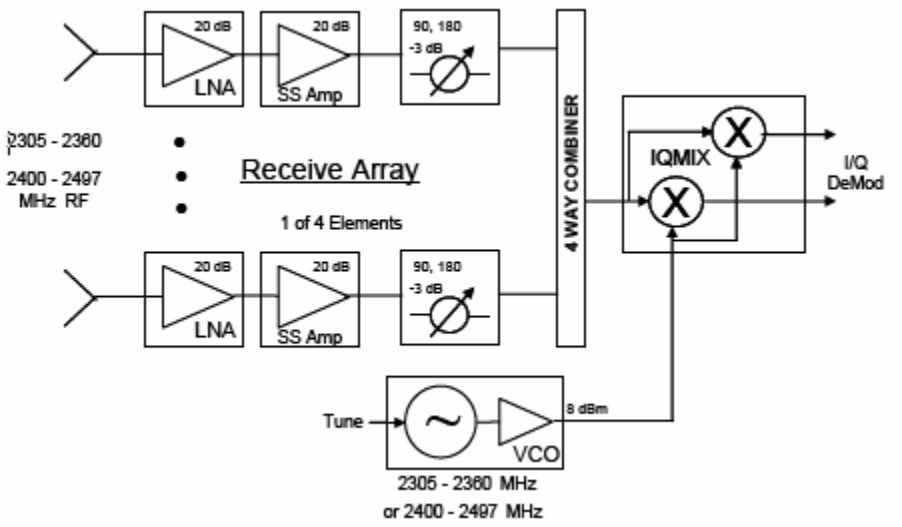



**Figure A. S-band duplex transceiver for JHU EE525.787 MMIC design class, receive path**

The phase shifter comprises three individual phase shift units, 45°, 90°, and 180° bits, which provides phase shift levels from 0° to 315° in 45° increments. Each bit would require two switches according to the configuration in Figure B.

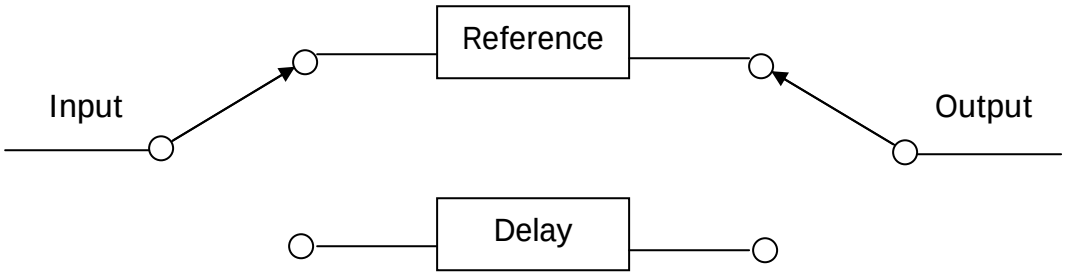



**Figure B. General phase shift bit configuration**

This report details the design, simulation, layout, and test plan for this phase shifter design.

## Design Approach

*Phase delay circuits*

An important aspect to remember when designing a phase shifter, or any sort of delay circuit, such as a digital time delay unit, or a digital attenuator unit, is that it is the relative difference between the reference and delay circuits that is important. In other words, when designing, for example, a 90° phase shifter, it is not important that the reference circuit produces 0° of phase shift while the delay circuit produces precisely 90°. It only matters that the phase of the reference circuit subtracted from the phase of the delay circuit equals 90°. There may be applications that dictate the absolute values of the sub-circuits in addition to the relative difference, but in this instance, as well as in most applications, the absolute values are not crucial. More crucial is usually size constraints of circuit components.

In this design I found that it was much easier to design the reference and delay circuits around 0 degrees of phase, for example, -45° and +45°, than it is to design say 0° and 90° degrees. In the latter case, additional effort is required to achieve an identical phase sloping in frequency for a flat relative difference. In my experience, if the reference and delay circuits are designed to deviate more or less equally from 0 degrees in opposite directions (e.g. -45° and +45°) the resulting frequency sloping of both circuits usually end up matching without any additional effort to make it so. This may or may not apply to wide-band applications of which this is not.

In this design I aimed for -90° and +90° to compose the 180° shift, -45° and +45° for the 90° shift, and -25° and +20° for the 45° shift. Those absolute numbers serve as an aim and as guidelines, but final values actually deviate slightly, so long as the relative values are maintained.

The general topology used for any phase shift is a T-network, with a parallel inductor between two series capacitors, where possible, to reduce the area required by the MRIND inductors. Some circuits needed series inductors and a parallel capacitor to meet performance requirements, and that was allowed so long as the sizing was reasonable. Figure 1 shows the circuit topology, with layout interconnects inserted, for the -25° phase shift (reference) used in the 45° shift bit. Notice that the via for the parallel capacitor is connected through Port 3 at a higher hierarchical level.

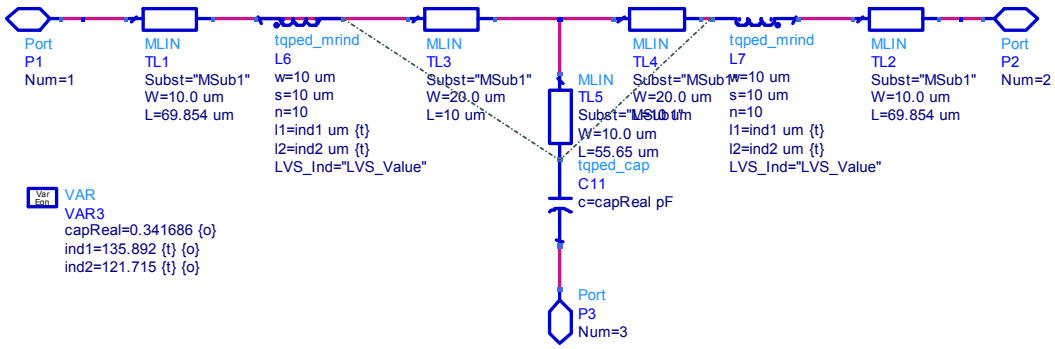



**Figure 1. -25 degree phase shift topology**

*Switches*

Initially the topology pursued for the switch was a parallel FET and then a series FET on each switch path (four FET's total). The rationale for the parallel FET was to pull the signal to ground when the path is switched off. However, when that topology introduced too much loss, the parallel FET's were removed. It turned out that two FET's alone could still perform the job well as a switch.

Since the goal was TTL for the control bits, initially enhanced mode FET's were used for the switches for more straightforward voltage control. But when that resulted in unpredictable and deviant behavior whenever multiple phase bits were turned on, the E mode FET's were switched to depletion mode FET's instead. D mode FET's produced more stable behavior for all phase shift levels. Figure 2 below shows the switch topology used.

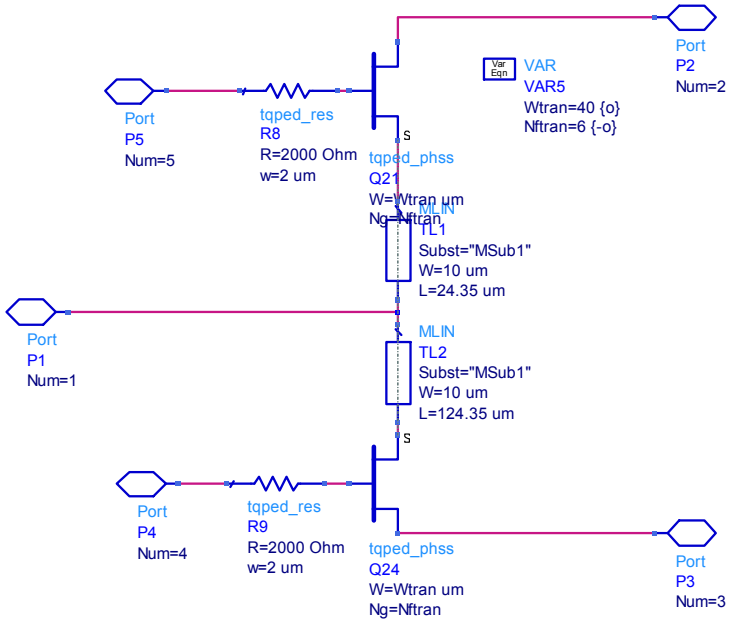



**Figure 2. Switch**

*Top Level Design*

Due to time constraints an inverter or voltage converter were not designed which would otherwise simplify the control bits for the phase shifter. Figure 3 shows the top level circuit topology. In the end each shifter bit required two complementary control lines of 0V and -2V, to switch on and off the paths, respectively.

Once the switches are connected with the reference and delay circuits to make all three delay bits (i.e. 45°, 90, or 180° bits), the order in which they are arranged impact the VSWR (or return loss) or the total circuit. Figure 3 shows that the order that was found to be most beneficial to reducing total VSWR is from RF in to first the 90° bit, then the 180° bit, and finally the 45° bit which connects to RF out.

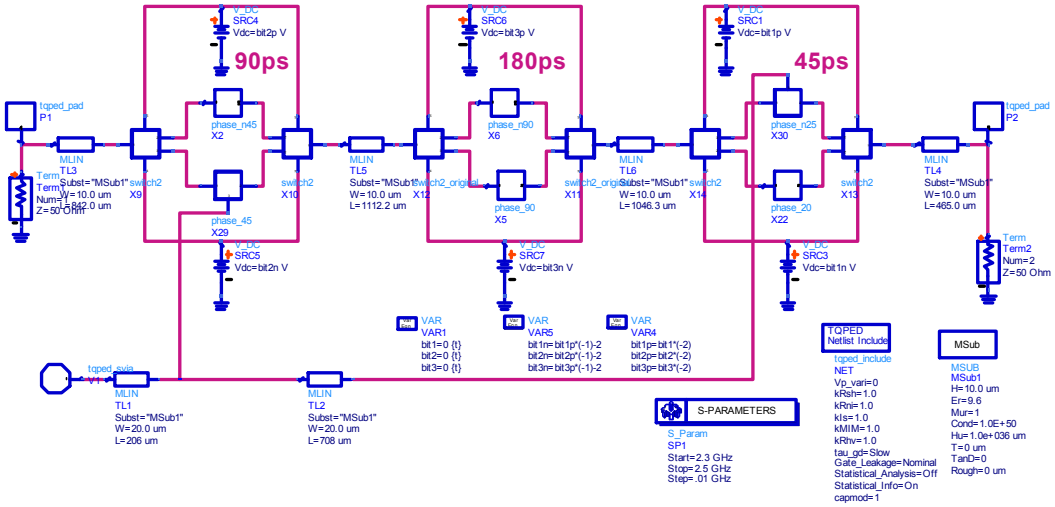



**Figure 3. Top level phase shifter topology**

Table 1 below shows the specifications for this design as well as the achieve simulation results with all layout interconnects included.

**Table 1. Specifications and simulated results**

| | ***Specification*** | ***Simulated Results*** |
|---|---|---|
| **Frequency** | 2305 to 2497 MHz | 2305 to 2497 MHz |
| **Insertion Loss** | < 5 dB | 5.6 < IL < 6.3 dB |
| **Insertion Balance** | +/- 1 dB | +/- 0.35 |
| **Phase Shift** | Steps 45°, 90°, and 180° | Steps 45°, 90°, and 180° |
| **VSWR, 50 Ohm** | <1.5:1 input and output | <1.59:1 for 180° shift<br><1.5:1 for all other degree shifts |
| **Control** | TTL | 0V, -2V |
| **Size** | 60 x 60 mil “ANACHIP” | 60 x 60 mil “ANACHIP” |
| **Phase accuracy** | ½ LS bit, or 25° | < +/- 3° |

## Simulations

Figure 4 shows the simulated results for the final phase shifter adjusted for all layout interconnects. Notice that the plot shows phase shifts starting from 360° (0°), so that-315° equals the 45° phase shift, 270° equals 90°, and so on. The results show a phase shift deviation of less than +/- 3 degrees per phase level. The plots also show that except for one phase step (which is not labeled but is the 180° shift level), all VSWR results meet the 1.5:1 spec. The switches, however, introduced more loss than desired, so that the total circuit insertion loss is more than 5dB. That reduction in performance for the insertion loss was accepted as a part of a tradeoff with return loss.

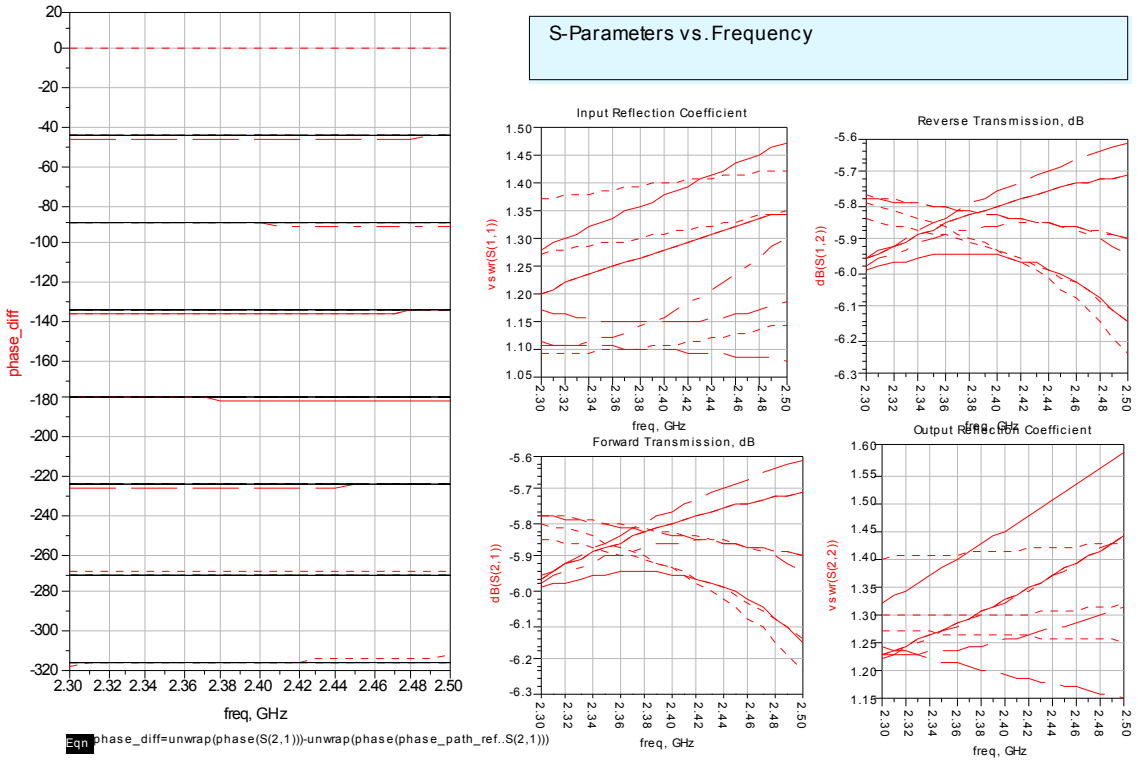



**Figure 4. Phase shifter S-parameter and phase shift simulation results**

Figure 5 shows simulated results for the switch used in the design project. It shows that for the active switch path, the switch gives both input and output VSWR's of better than 1.16:1. Switch loss is a little better than 1dB, and since there are 6 switches in the design, two for each of the three shift bits, there will be almost 6dB of loss just from the switches alone. As ensuing simulations will show, the switch loss is the major and primary contributor to the total circuit insertion loss. All phase shift circuits have but a fraction of a dB of insertion loss.

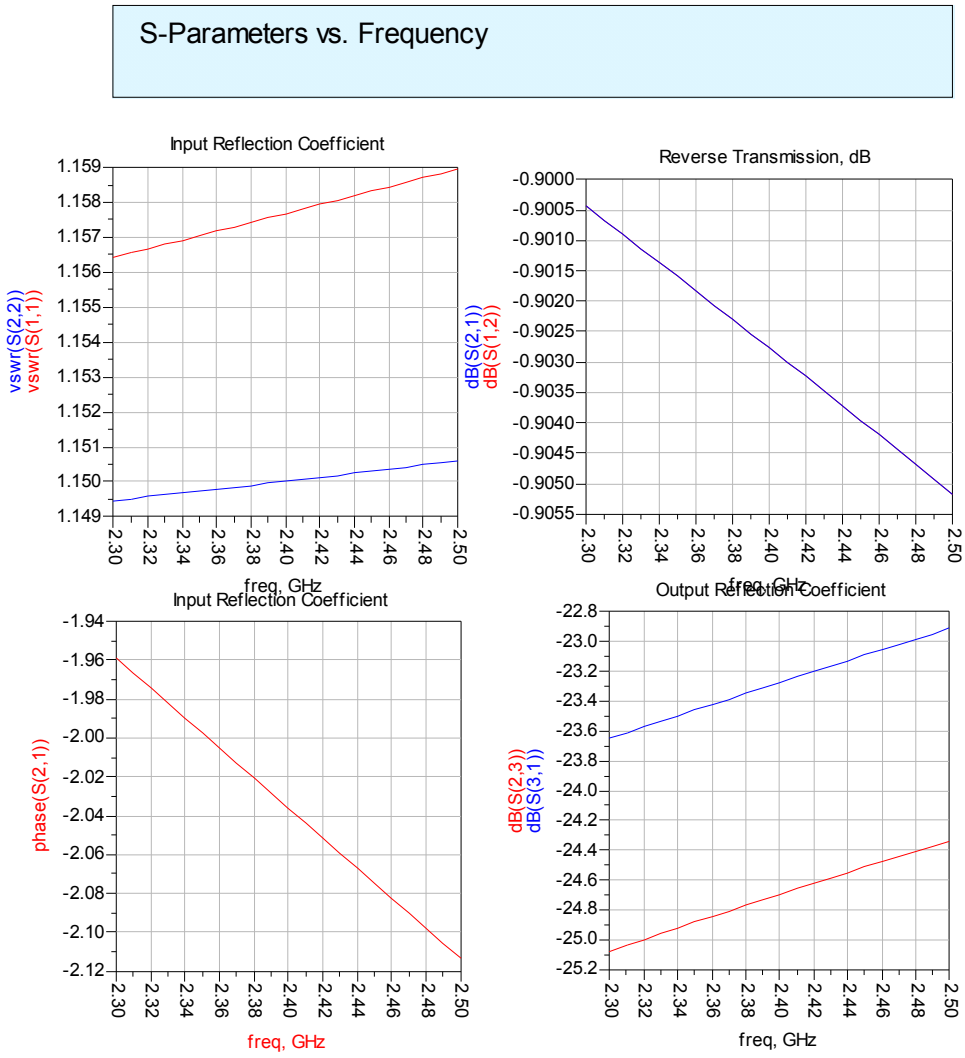



**Figure 5. Switch simulation results**

Figures 6 through 8 show simulated results for reference and delay circuits of the 90°, 180°, and 45° phase shift bits. The dotted lines represent the traces for the reference circuits. Notice that all VSWR plots are better than 1.2:1, and all insertion losses are but a fraction of a dB. The VSWR worsens once all shifter bits are combined.

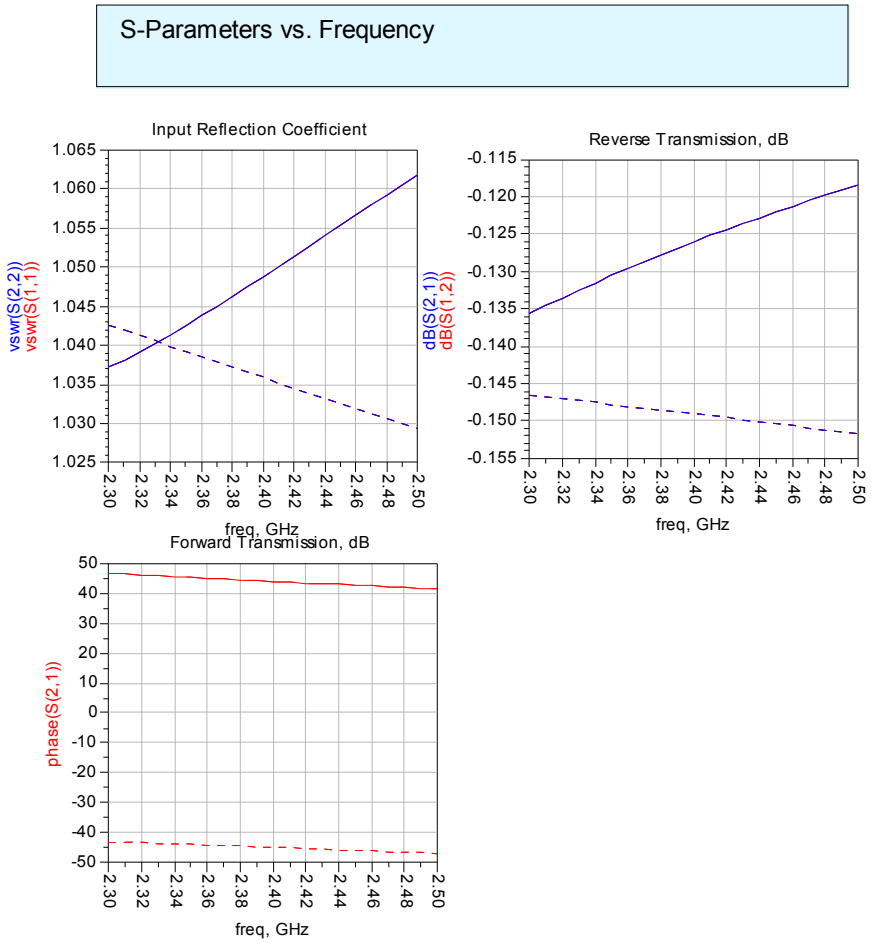



**Figure 6. Reference and delay simulation results for 90° phase shift**

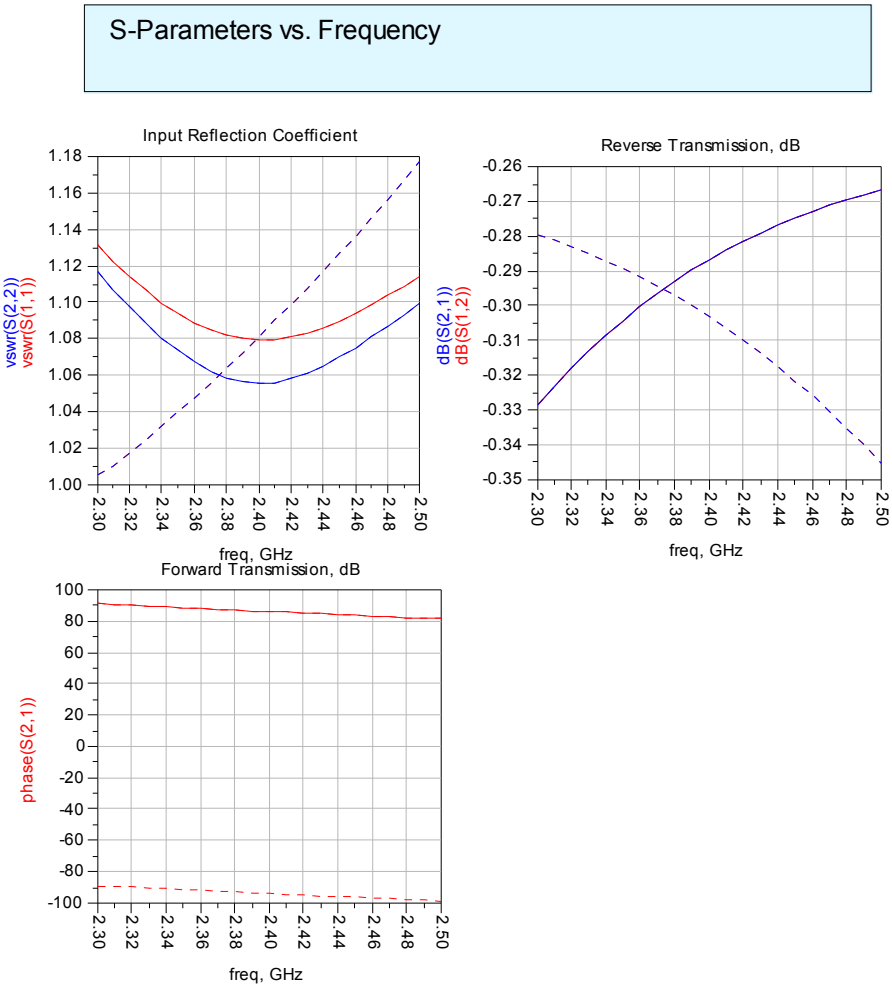



**Figure 7. Reference and delay simulation results for 180° phase shift**

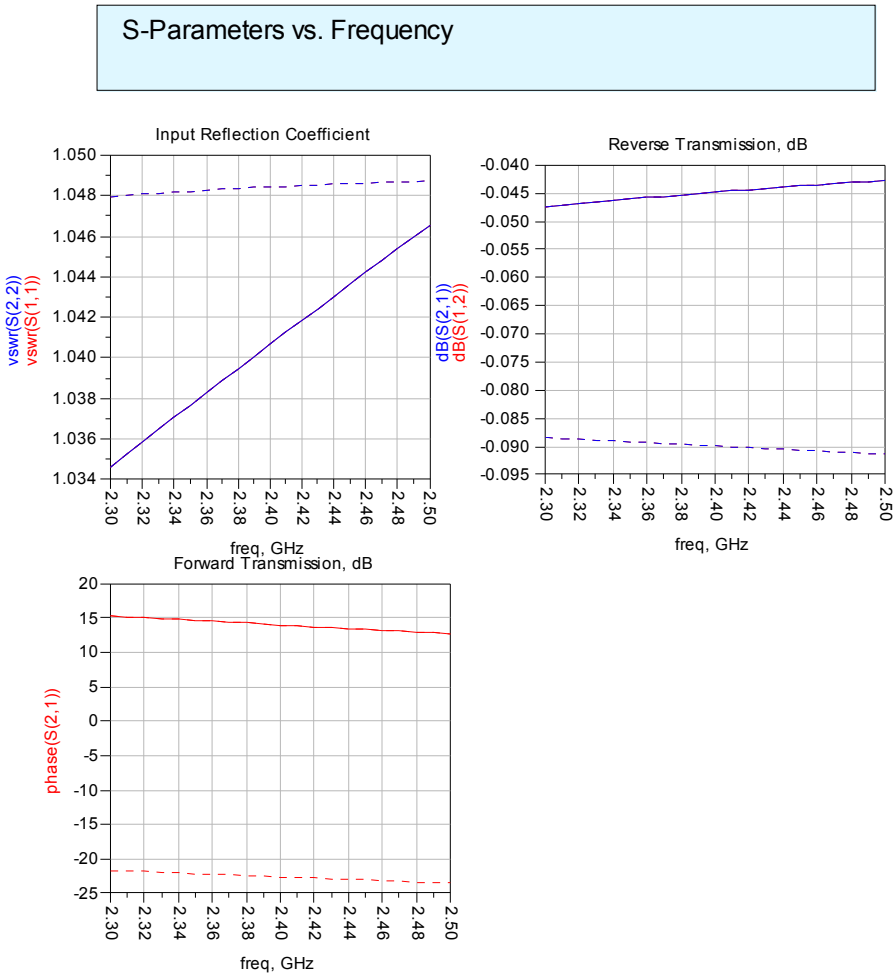



**Figure 8. Reference and delay simulation results for 45° phase shift**

**Schematic**

Please see Figures 1 through 3 for schematics of the -25° phase shift, the switch, and the top level layout. For the rest of the phase shift circuits, see below from Figures 9 through 13.

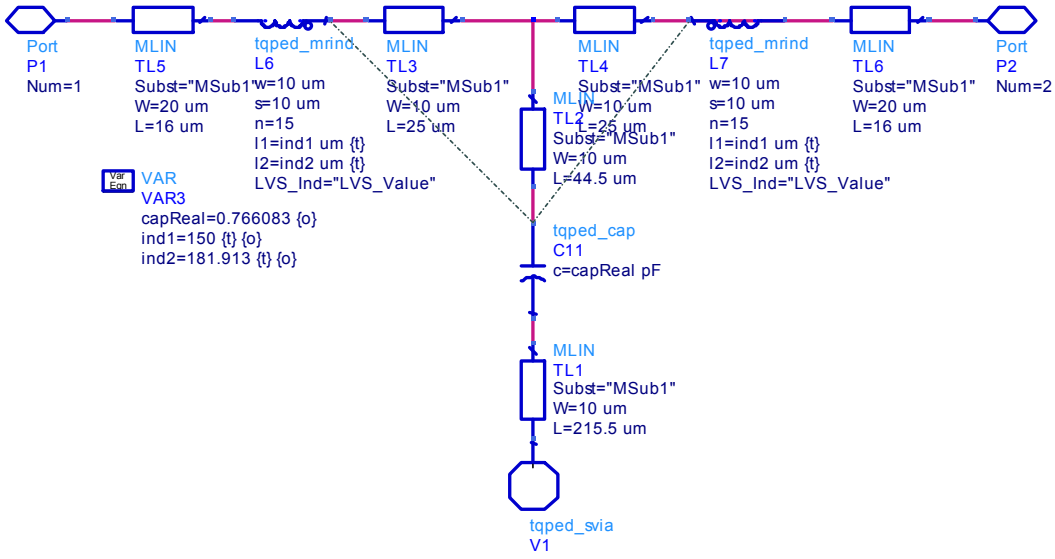



**Figure 9. -45° phase shift**

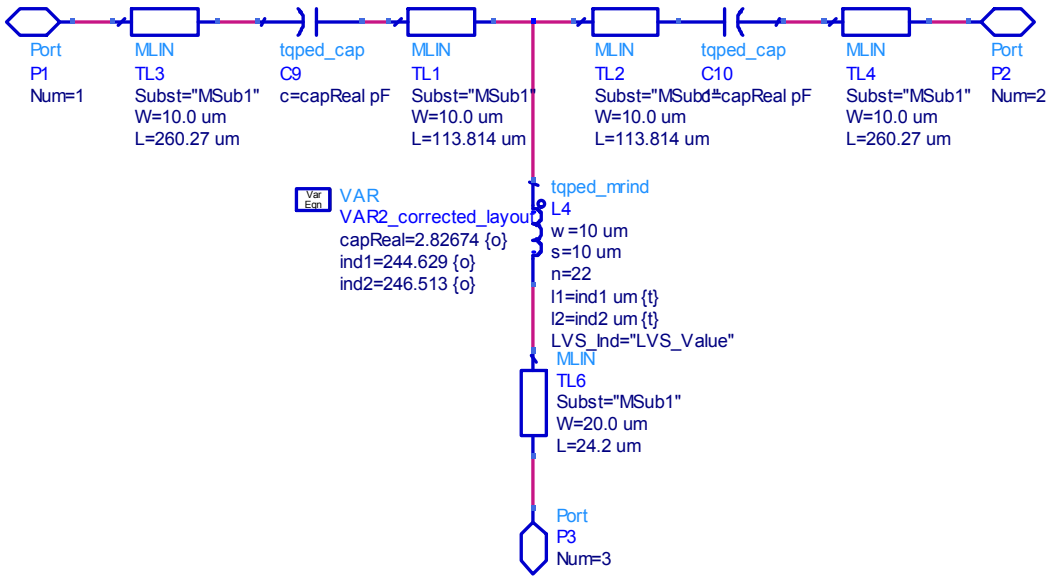



**Figure 10. +45° phase shift**

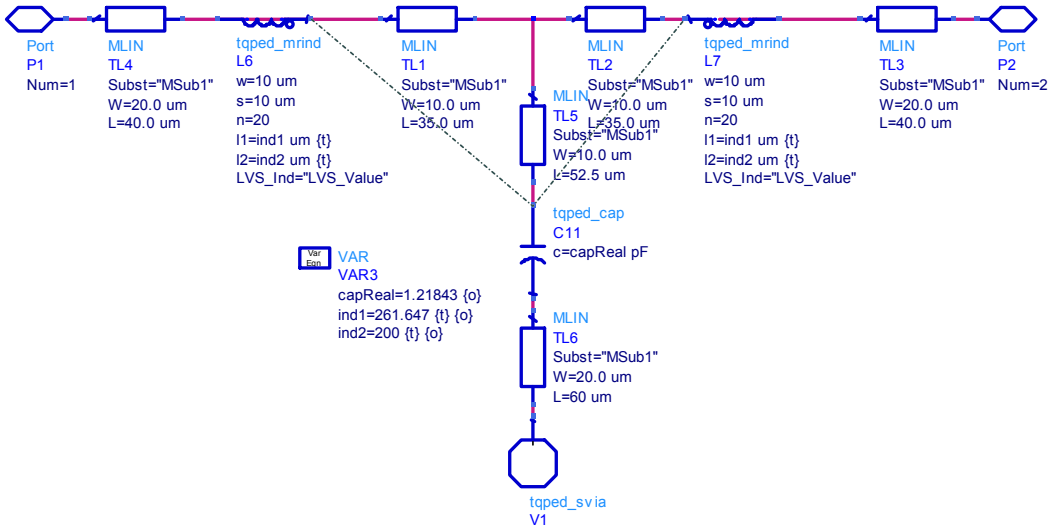



**Figure 11. -90° phase shift**

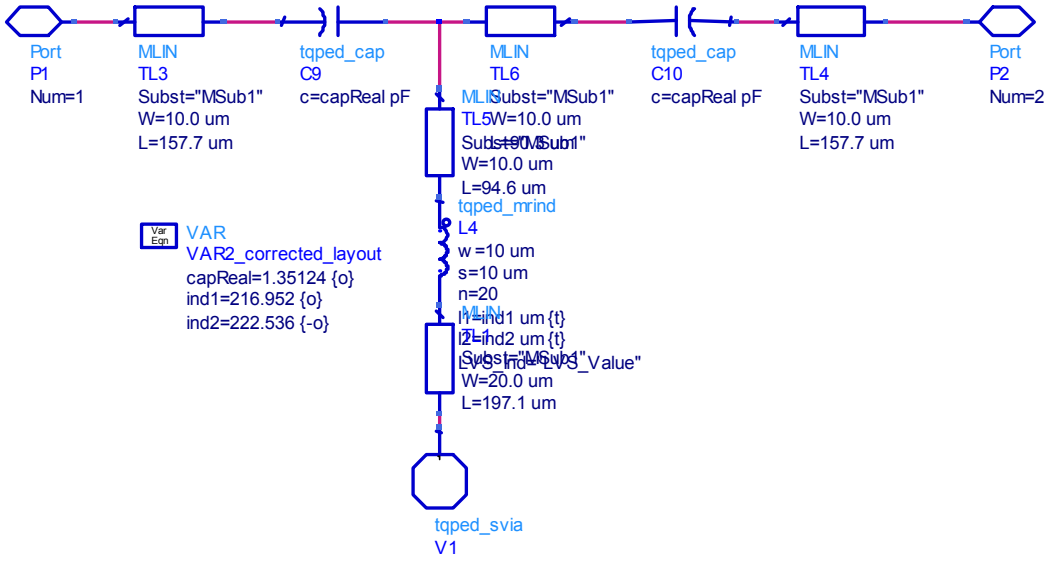



**Figure 12. +90° phase shift**

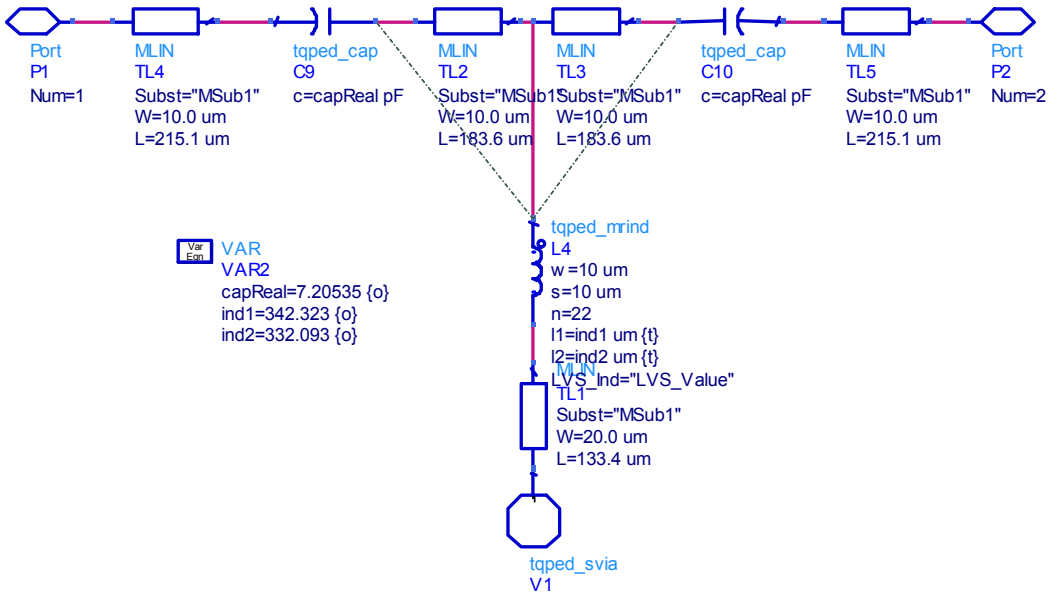



**Figure 13. +20° phase shift**

## Layout Plot

Figure 14 shows the final layout for the phase shifter on a 60 mil by 60 mil GaAs substrate. Notice that there are three white boxes outlining the perimeter of the chip, the inner most box signifies the boundary for all vias. The second innermost box represents the boundary for all other circuit components. You'll notice that there is an empty margin on the left and bottom of the chip where components are allowed. The reason for that is that I had previously been under the impression that the circuit boundary was smaller than it actually was.

The RF input and output GSG (ground-signal-ground) pads are on the top left corner and right side of the chip, respectively. The GSG pads have a pitch of 150um. There are three more pairs of pads for the control lines. Each pair has a pad labeled "R" for reference, and "D" for delay, depending on which path is desired to be switched on or off. In-between each pad pair is also the label for the phase shift (i.e. 45, 90, or 180).
Care was taken to compact the design, as well as to make everything symmetrical wherever possible. Additional vias were added whenever the addition could help avoid too many lines from crossing each other during routing, and at the same time they were kept to a minimum to conserve space.

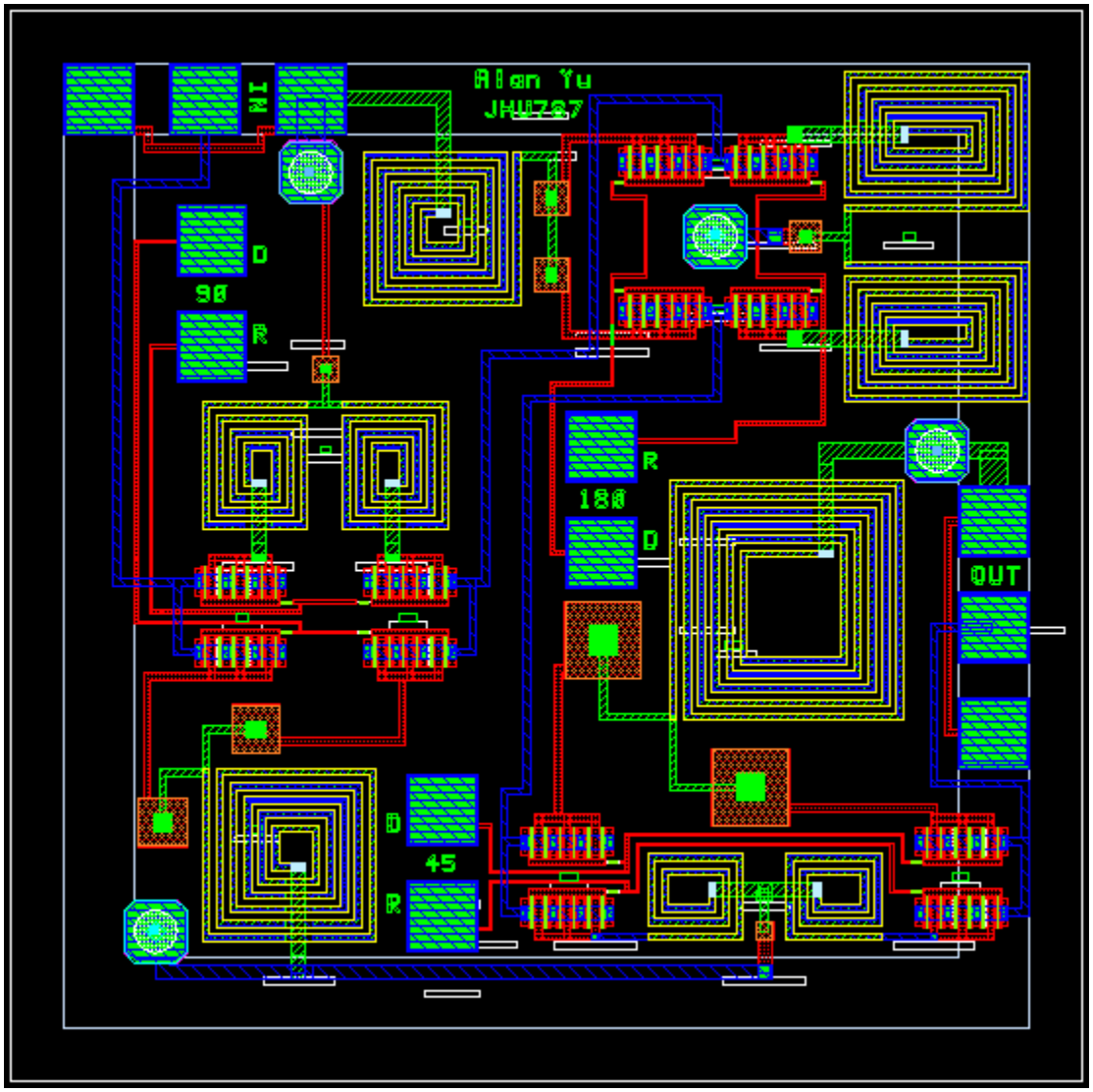



**Figure 14. Phase shifter final layout**

**Test Plan**

A network analyzer, probing station with two 150um pitch GSG probes, three single probes, as well as a power supply capable of providing -2V control voltages are needed to test the phase shifter.

*Steps*

─Connect a -2V supply to all three pads on chip labeled D (for delay). The other three reference pads should automatically float to 0V during measurement.
─Connect a 150um pitch GSG probe from the network analyzer to the RF input pads labeled "IN."
─Connect a 150um pitch GSG probe from the network analyzer to the RF output pads labeled "OUT."
─Measure the S-parameters of the RF ports using the network analyzer from 2.3 to 2.5 GHz in 10MHz steps.
─Save results to disk.
─Disconnect the -2V supply from the pad labeled D on the 45° bit, and place it instead on the pad labeled R on the 45° bit. The pad D should now automatically float to 0V during measurement.
─Measure and save as done previously
─Repeat this procedure for measuring and saving data until the -2V supply has been supplied to the control pads in all combinations as listed according to Table 2 below. Measure using the network analyzer and save all results to disk.
─When done measuring, disconnect, return, and turn off all equipment.
─Finally compare measure results verses simulation to assess accuracy of model.

| | 45° bit | | 90° bit | | 180° bit | |
|---|---|---|---|---|---|---|
| Shift | R | D | R | D | R | D |
| 0° | | -2V | | -2V | | -2V |
| 45° | -2V | | | -2V | | -2V |
| 90° | | -2V | -2V | | | -2V |
| 135° | -2V | | -2V | | | -2V |
| 180° | | -2V | | -2V | -2V | |
| 225° | -2V | | | -2V | -2V | |
| 270° | | -2V | -2V | | -2V | |
| 315° | -2V | | -2V | | -2V | |

**Table 2. Combinations for -2V connections for testing all phase shift levels**

**Summary & Conclusions**

In Summary, a three bit phase shifter was successfully designed for the S frequency band from 2.305 to 2.497 GHz. Phase shift accuracy exceeded specification requirements and had less than +/- 3° of variation in-band. Input and output VSWR achieved spec of under 1.5:1 for all but one out of 8 phase shift levels, which was the 180° phase shift that had close to a VSWR of 1.6:1 up towards 2.497 GHz. All three bits of the design were compacted into a 60 x 60 mil GaAs chip. The higher loss in the switches used in the design, however, caused the insertion loss of the total design to exceed the spec of 5dB. The insertion loss ended up getting as high as close to 6.3dB at certain phase shift levels towards 2.497GHz. Also, the choice for using 3 pairs of control lines for the shift bits requiring 0V and -2V permits testing to be done on the fabricated design, but does not meet the goal of TTL compatibility.

With additional time, some enhancement opportunities include the following,

—Look into creating a DC converter circuit that converts 5V to -2V.

—Look into designing an inverter between 0V and -2V or 0V and 5V to be used in conjunction with the converter circuit so that only three control bits are necessary externally for controlling the phase shift levels.

—Since a transmission line is modeled as a sequence of series inductors and parallel capacitors, a version can be created with larger real estate and more components to achieve a wider bandwidth design

—Look into the possibility of using different transistors and switch topologies to reduce the switch loss while keeping the VSWR performance the same or better.

—Look at measured transistor performance to better predict circuit behavior.

—Do a measure versus model fit of the fabricated chip

# S-Band Down Converter

Double Balanced Star Mixer

MMIC Design

John Tinsley

07-December-2007

# S-Band Down Converter

## Double Balanced Star Mixer

**Advantages:**

- Compact Design
- No DC Bias
- Low RF / IF conversion loss
- Simple design

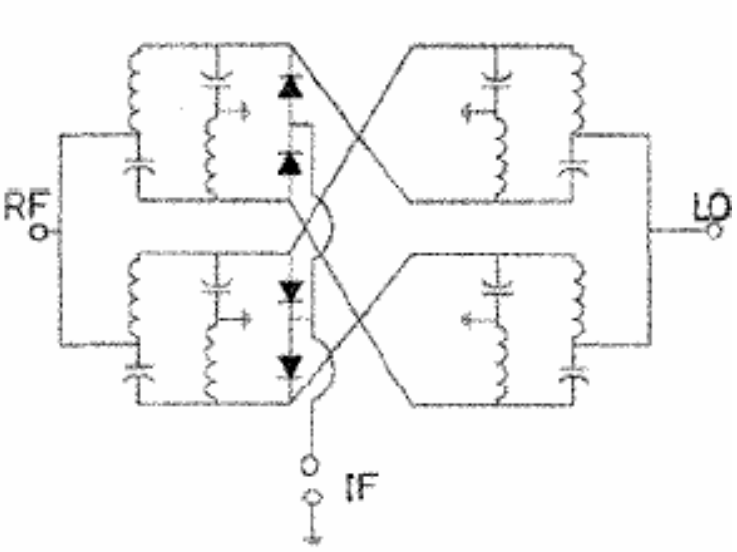



**Figure: Double Balanced Star Mixer Schematic**

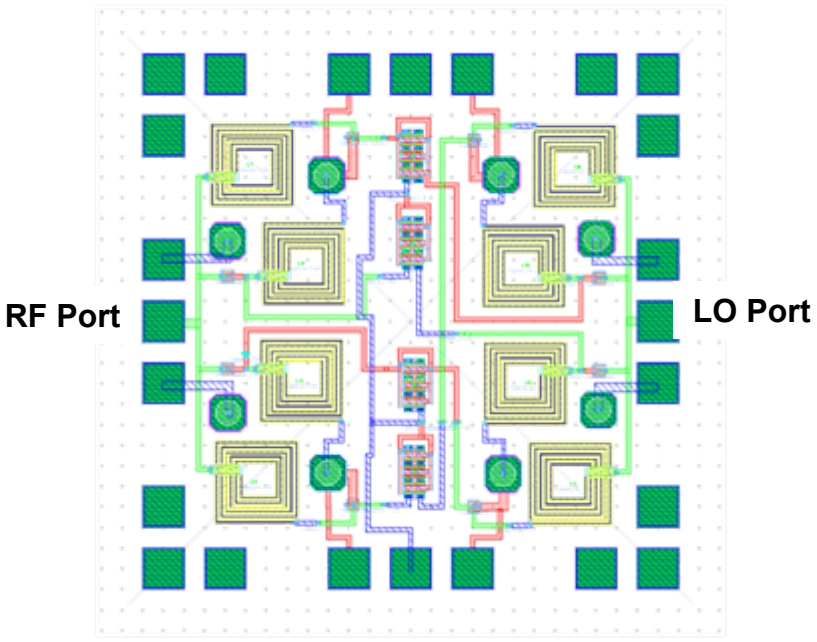
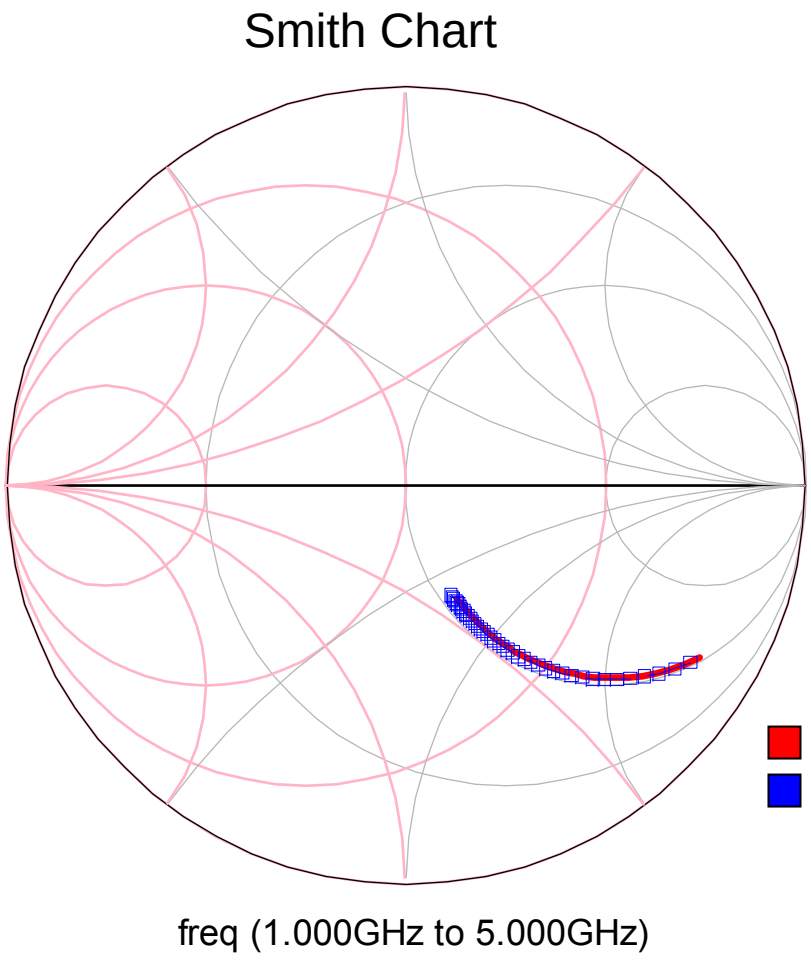
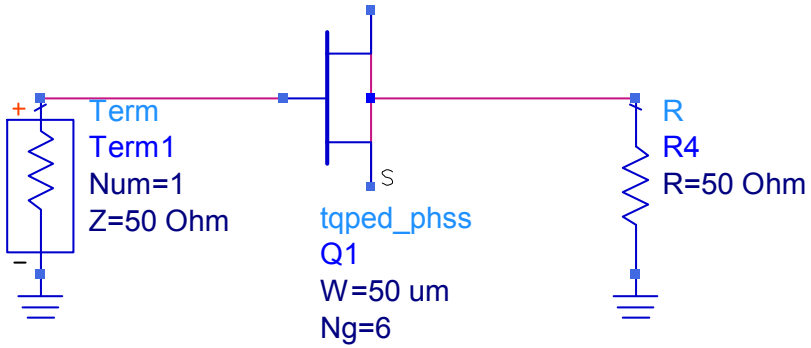
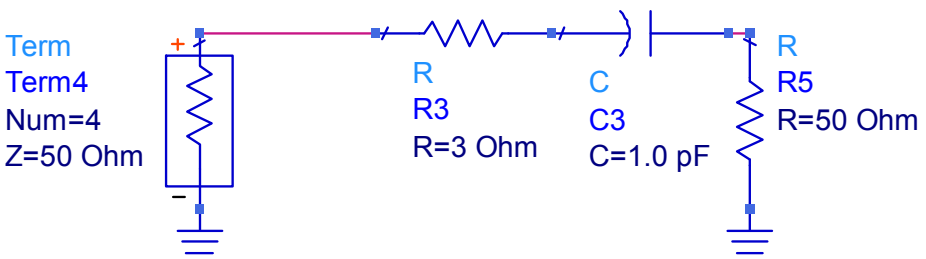



**Figure: Double Balanced Star Mixer Layout**

# Diode Modeling



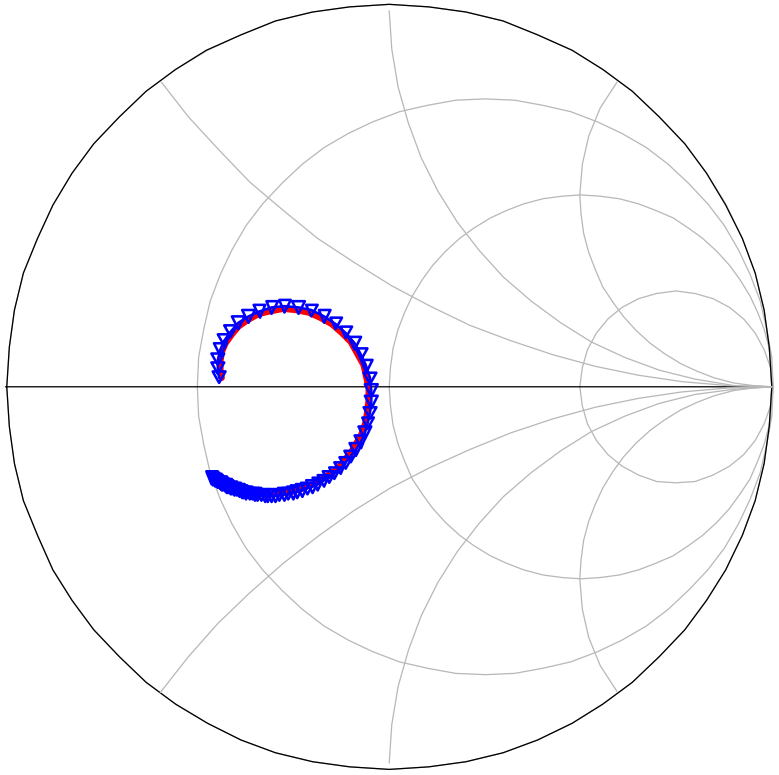

**Triquint PHEMT**
**Lumped Element Model**

**Diode Impedance: 3 + j66.31 Ω**

**Figure 1: Diode (PHEMT) Input Impedance**

# 180° Power Splitter

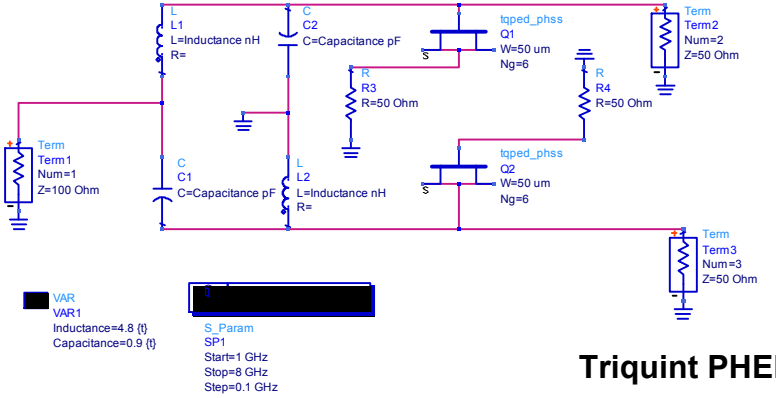
## Smith Chart



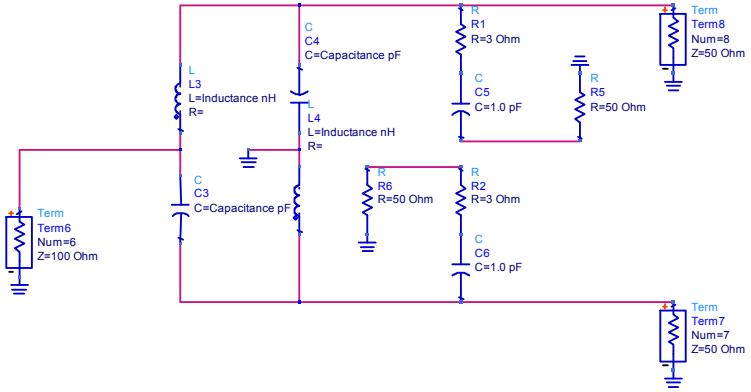
freq (1.000GHz to 8.000GHz)

**Triquint PHEMT**

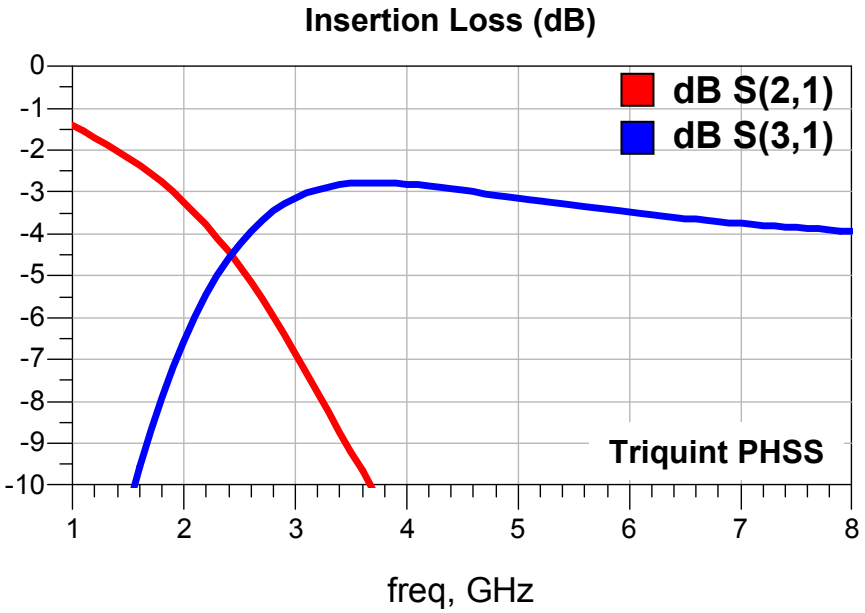
**Lumped Element Model**

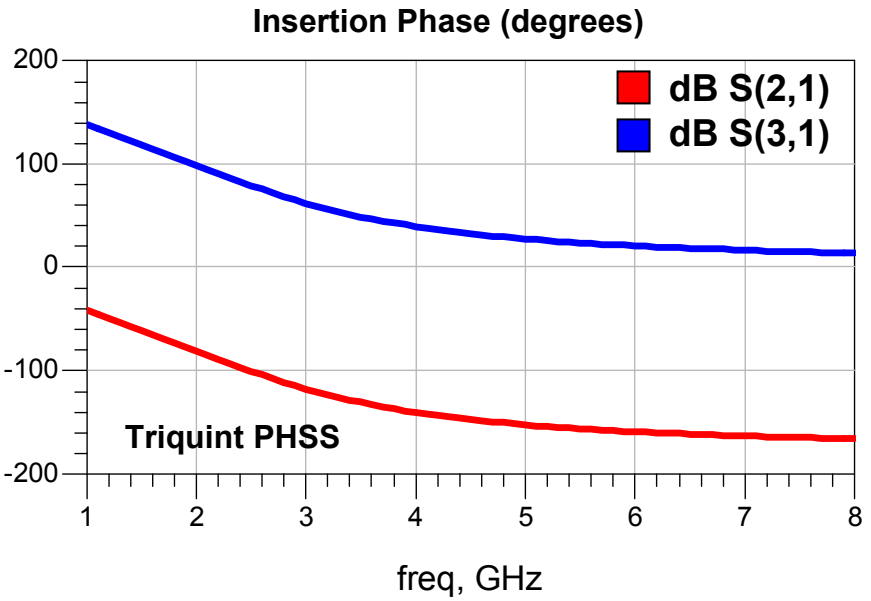



**Triquint PHEMT**

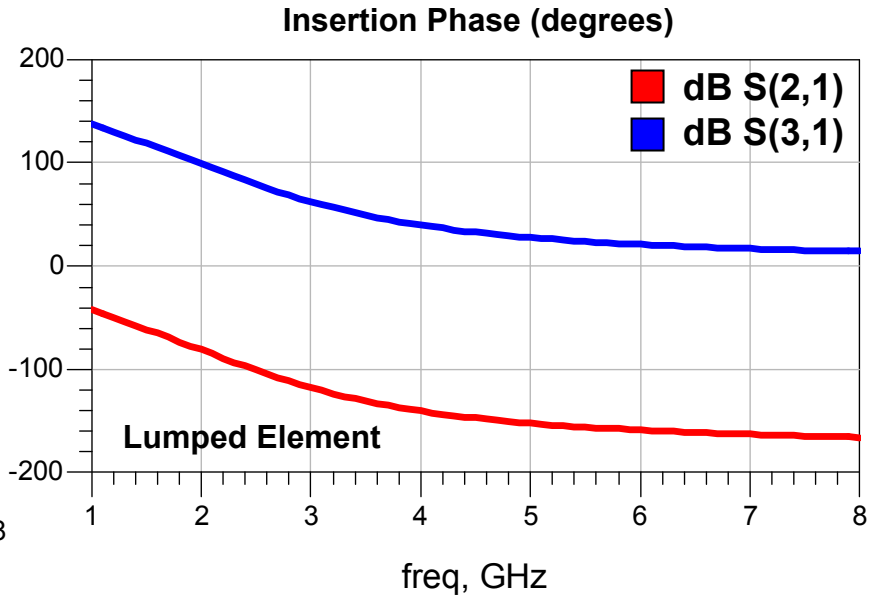



**Lumped Element Model**

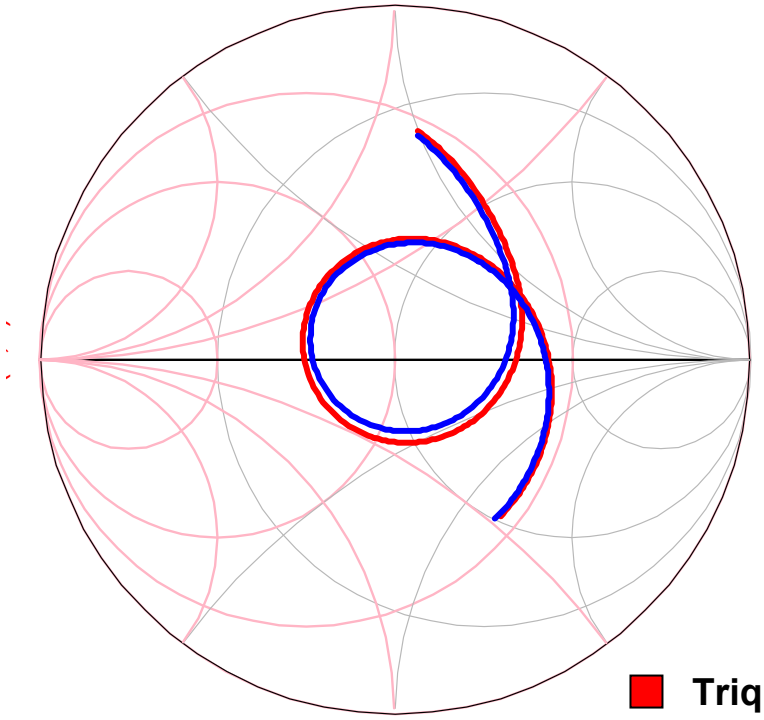

Insertion Loss (dB)
dB S(2,1)
dB S(3,1)
Triquint PHSS
freq, GHz


Insertion Phase (degrees)
dB S(2,1)
dB S(3,1)
Triquint PHSS
freq, GHz

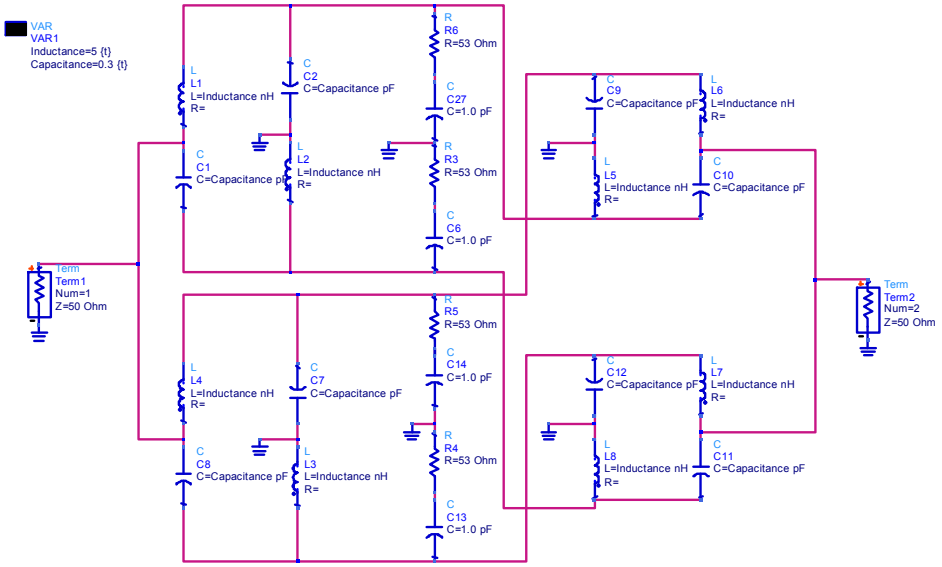

Insertion Loss (dB)
dB S(2,1)
dB S(3,1)
Lumped Element
freq, GHz


Insertion Phase (degrees)
dB S(2,1)
dB S(3,1)
Lumped Element
freq, GHz

# DBM Simulation and Tuning



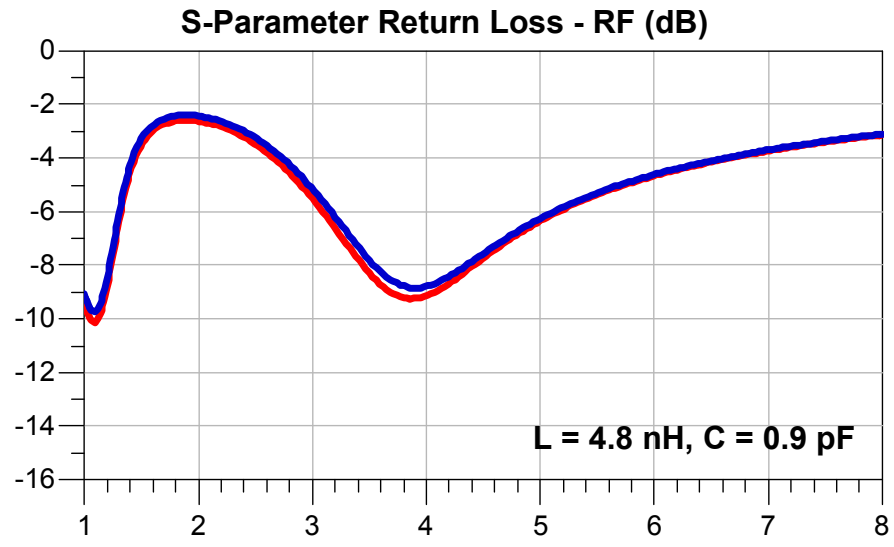
freq (1.000GHz to 8.000GHz)

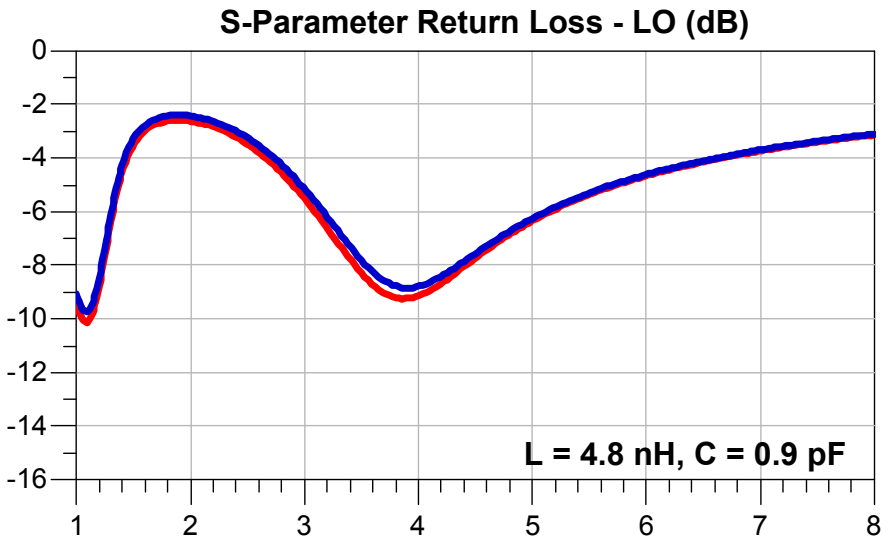


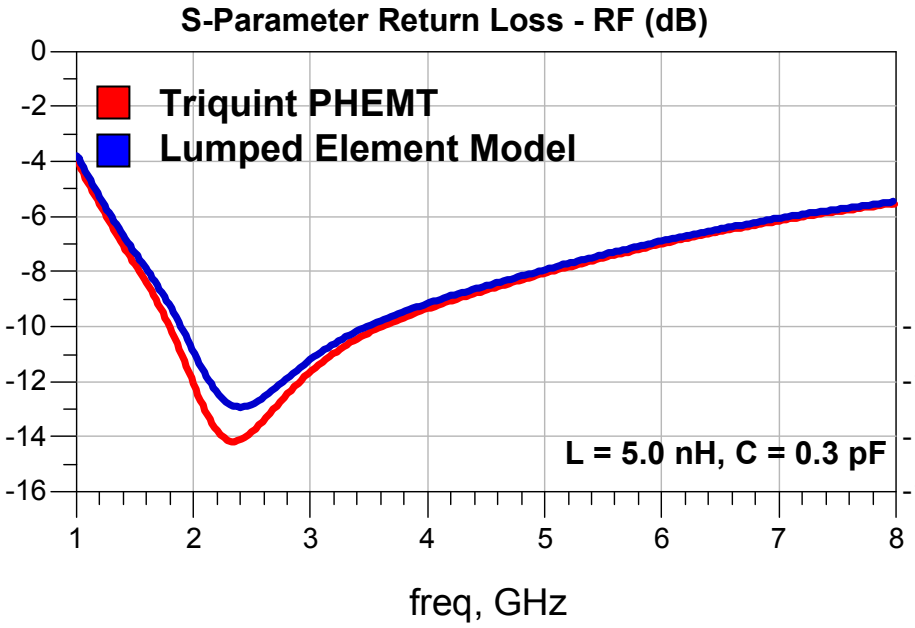

**Triquint PHEMT**
**Lumped Element Model**

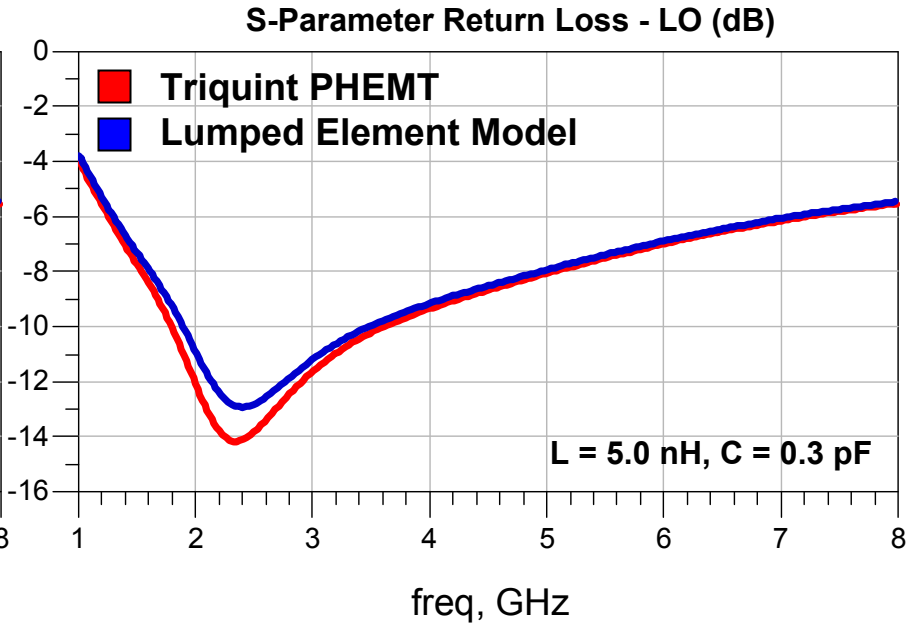
**Figure 3: DBM input impedance (normalized 50 ohm)**

# DBM Simulation and Tuning

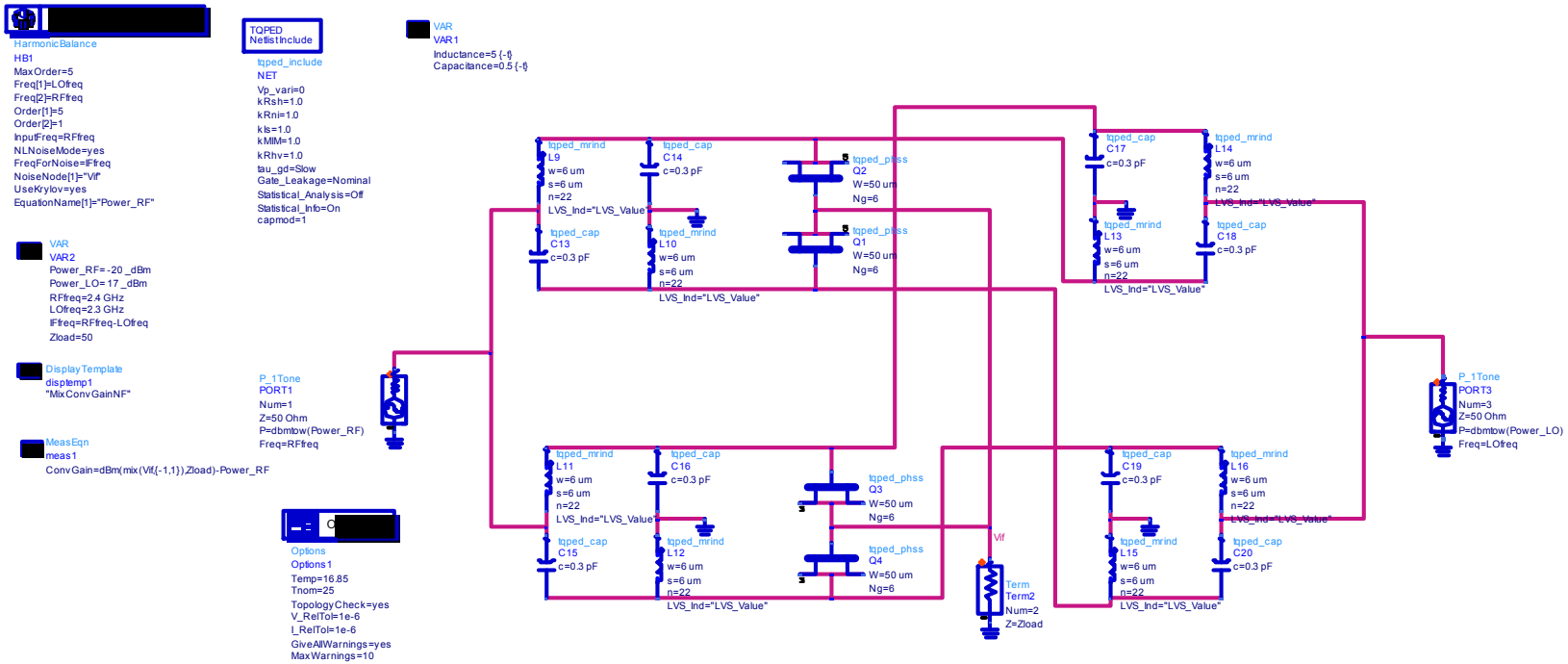


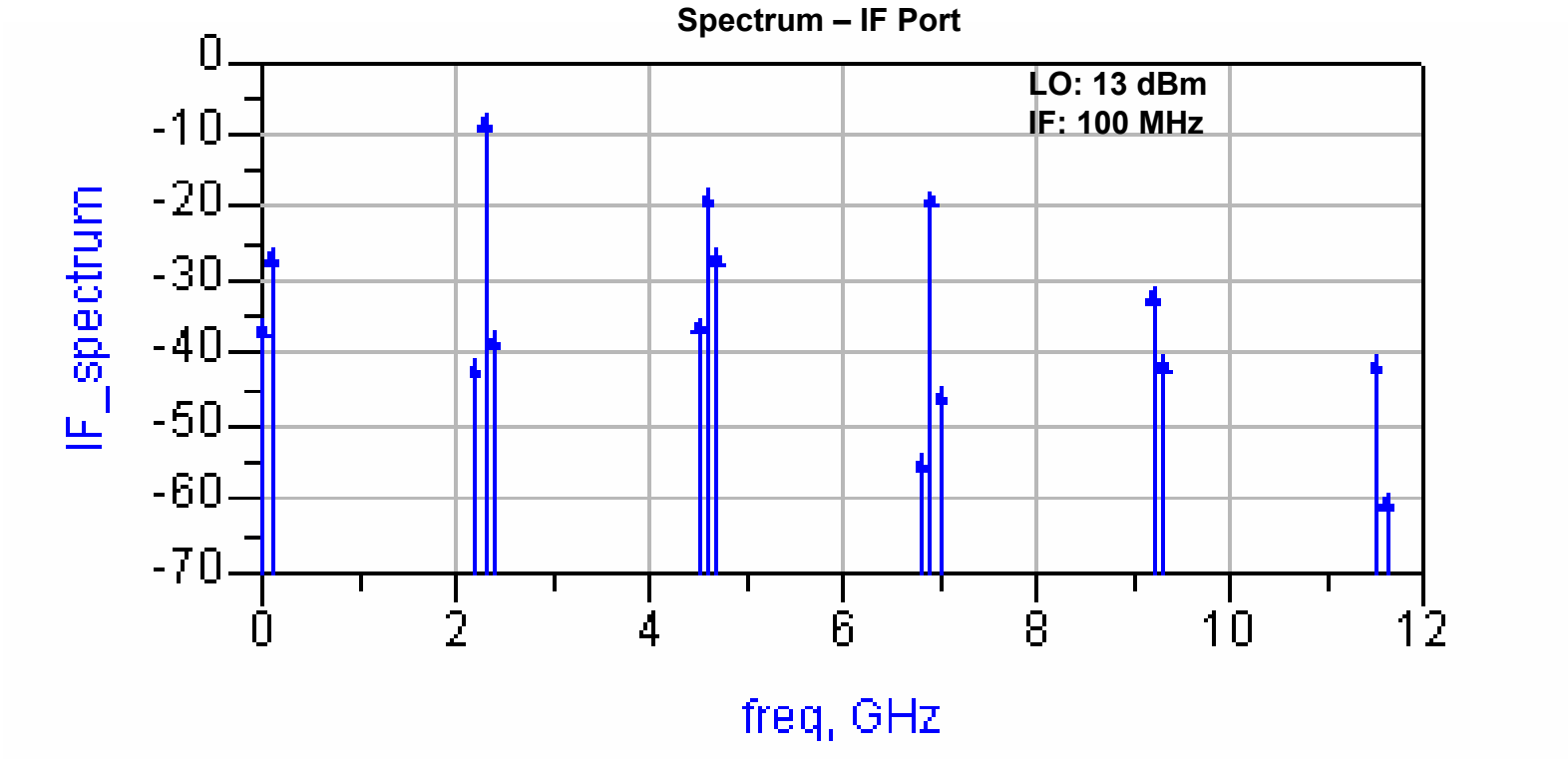



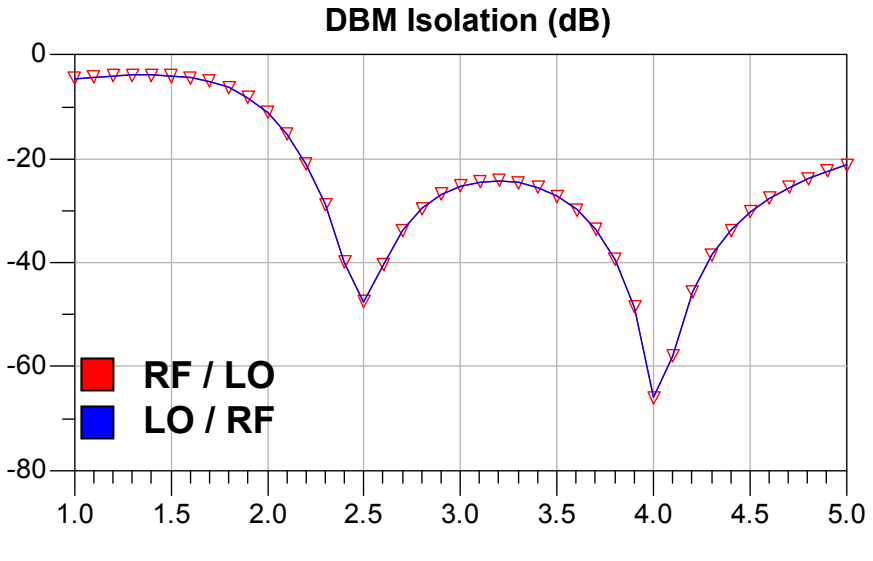



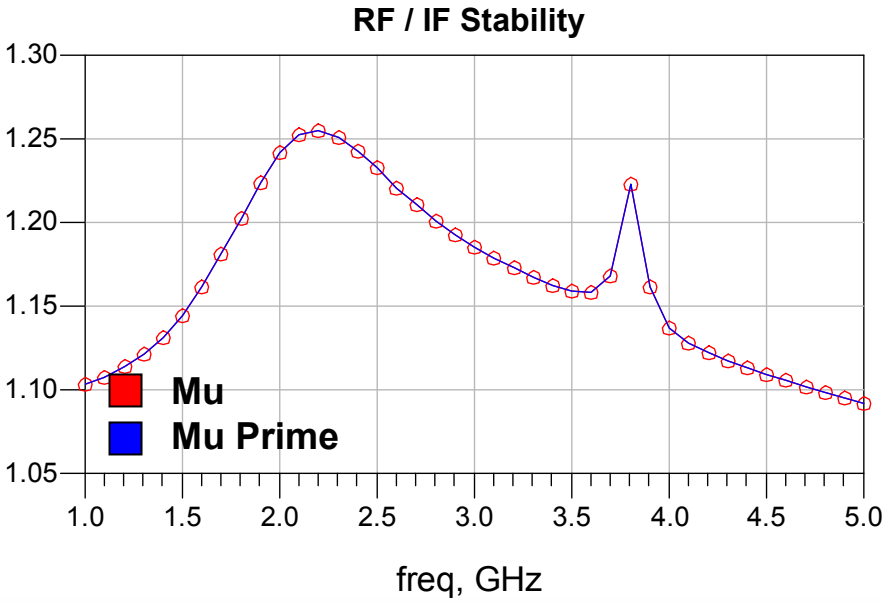
# DBM Non-Linear Simulation

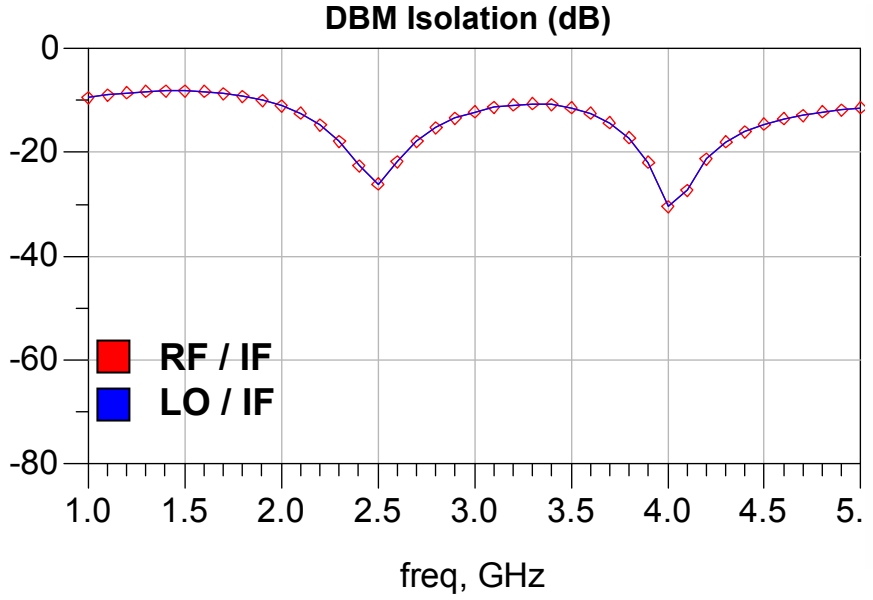


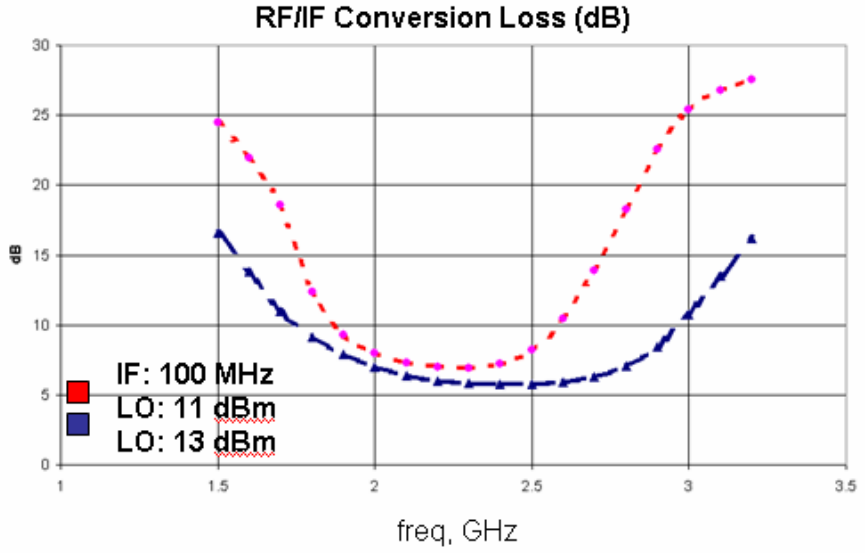
# DBM Non-Linear Simulation




DBM Isolation (dB)
0
-20
-40
-60
-80
RF / LO
LO / RF
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
freq, GHz


RF / IF Stability
1.30
1.25
1.20
1.15
1.10
1.05
Mu
Mu Prime
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
freq, GHz


DBM Isolation (dB)
0
-20
-40
-60
-80
RF / IF
LO / IF
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.
freq, GHz


RF/IF Conversion Loss (dB)
30
25
20
15
10
5
0
dB
IF: 100 MHz
LO: 11 dBm
LO: 13 dBm
1
1.5
2
2.5
3
3.5
freq, GHz

# C-Band Power Amplifier MMIC

By

Jacob Treadway
Syed Saad Ali

JHU MMIC Design, Fall 2007
Dr. John Penn

# Introduction:

This report describes the design, simulation, and layout of a MMIC power amplifier submitted for the final class project of Johns Hopkins University's MMIC Design Course (525.787), Fall 2007. The amplifier was designed using Triquint's TQPED GaAs process. This is a C-band design operating from 5.150 GHz to 5.875 GHz. Portable wireless devices are the intended application for this design, and efficiency is of prime importance to extend device operating time. Enhancement mode devices were used facilitate the use of a single positive bias voltage. PAE is better than 20%, reaching 27% at 2 dB compression. Simulation and layout was carried out in Agilent's Advanced Design System (ADS) software. The design was laid out in a 60x60 mil area.

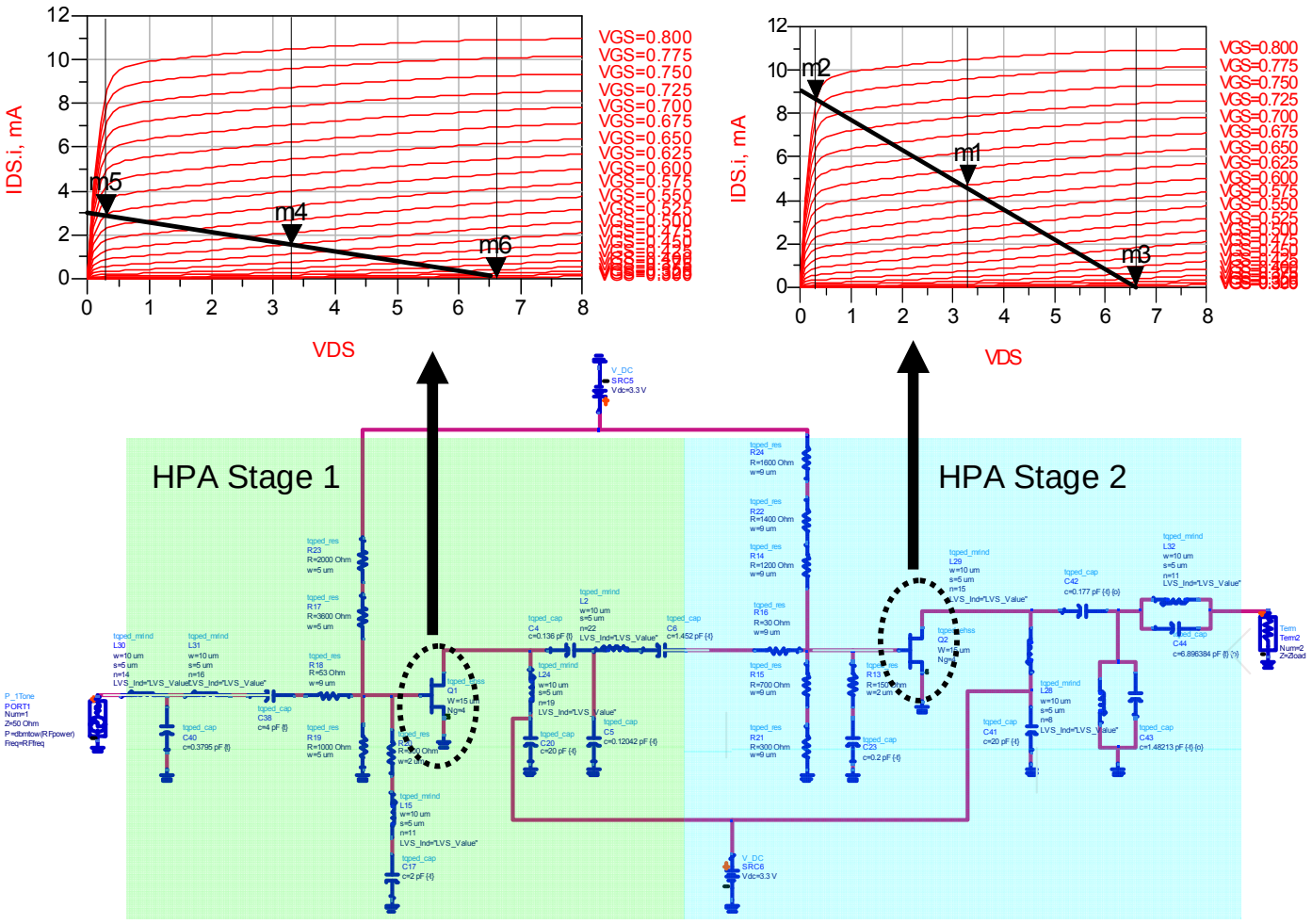
# Design Approach:

The requirements for this design are listed in the table below.

| Spec | Spec Value | Simulated |
|---|---|---|
| Operating Band | 5.150 – 5.875 GHz | N/A |
| Output Power | TBD | 8.85 dBm |
| Gain | 20 dB | ~ 21.5 +/- 0.3 dB over band |
| Gain Ripple | +/- 1 dB | +/- 0.3 dB |
| PAE | > 20% - 25% @ 1dB compression | 27% @ 2 dB compression |
| Input Match, 50ohms | < - 14dB, input and output | < -15 dB |
| Supply Voltage | +3.3 V | +3.3 V |
| Size | 60 x 60 mil | 60 x 60 mil |

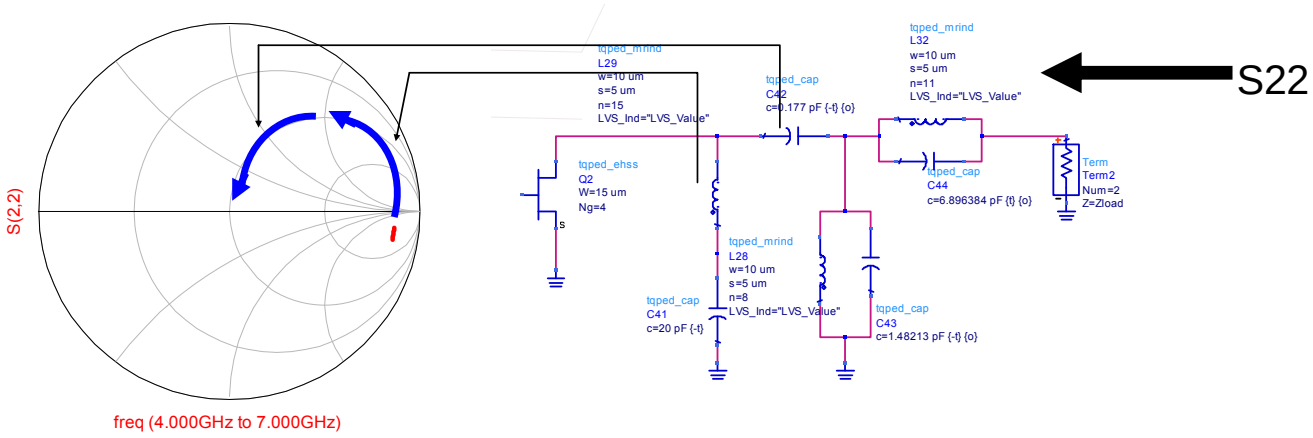
The highest priority requirement was PAE. A PAE of 20 to 25% is required at 1 dB compression. Large signal simulations predict a PAE of 23% at 1 dB compression. No lower limit was specified for output power. At 1 dB compression the design should produce XXX dBm of power. Layout of the design was restricted to a 60 by 60 mil die. Both drain and gate bias were designed to accept the same voltage, simplifying product integration by allowing the use of the same power regulation circuitry. Small signal simulation predicts 21.5 dB of gain, meeting the 20 dB requirement. Both input and output match are better than the -14 dB requirement.

It was decided to use the same periphery for the driver stage as the final stage. This was done because of concern over the accuracy of the fet model at the extreme edges physical size. To reduce power consumption of the first stage, it was biased at a lower gate voltage. The result was a device that had a peak drain current 1/3 of the 2nd stage, thereby reducing power consumption.

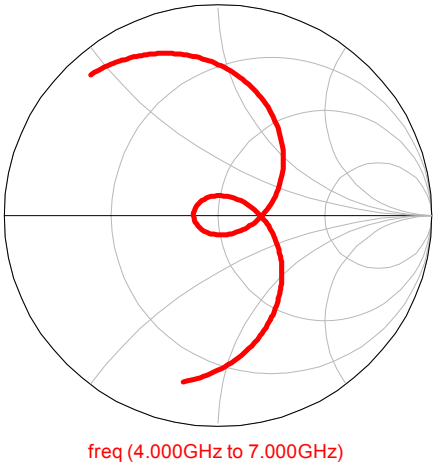


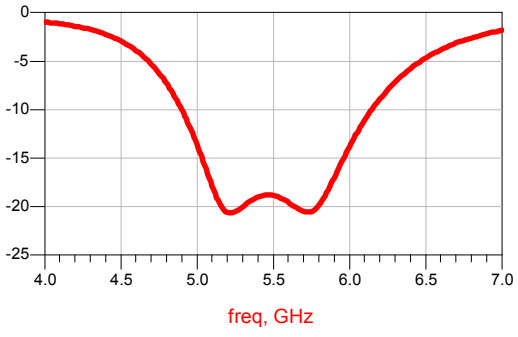

The first pass of the design employed 2 element matching networks for the output, input and interstage networks. Initial simulations showed that while the design met the requirements at the center of the band, performance quickly deteriorated toward band edges. Since the initial layout showed sufficient space to handle extra components, more elements were added to the different matching networks.

To improve PAE the output matching network (OMN) was modified. . As indicated in the figure below, a Parallel combination of inductor and capacitor was added in series and shunt. The addition of these elements created a looping of the impedance locus, thereby enhancing the bandwidth of the output Cripps match.

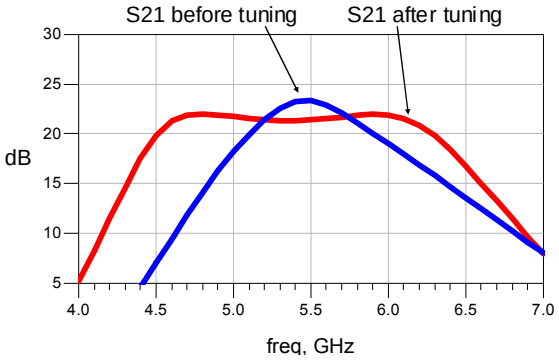


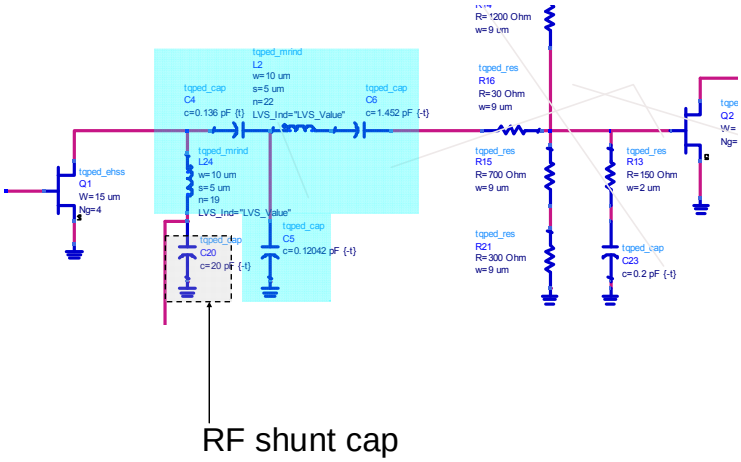

The figures below show the return loss looking of the OMN looking into the lumped element Cripps equivalent circuit of the fet's output.



Although gain was better than 20 dB, the +/- 1 dB gain ripple requirement was exceeded. ADS's filter synthesis tool was employed to create a more complicated interstage matching network. Additional tuning improved the gain ripple to less than +/- 0.3 dB, as indicated in the graph below.

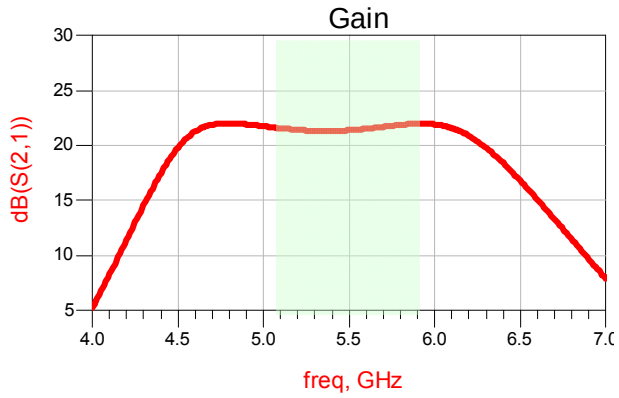


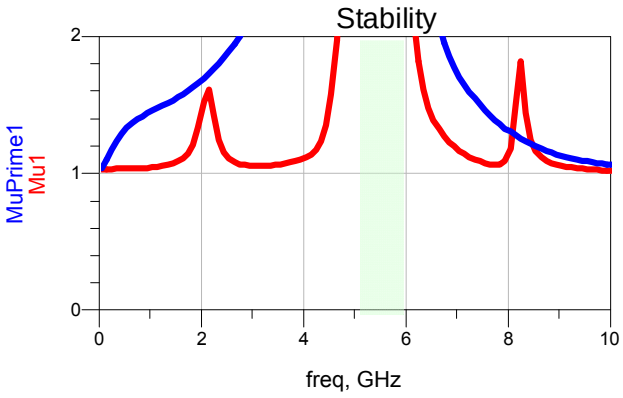



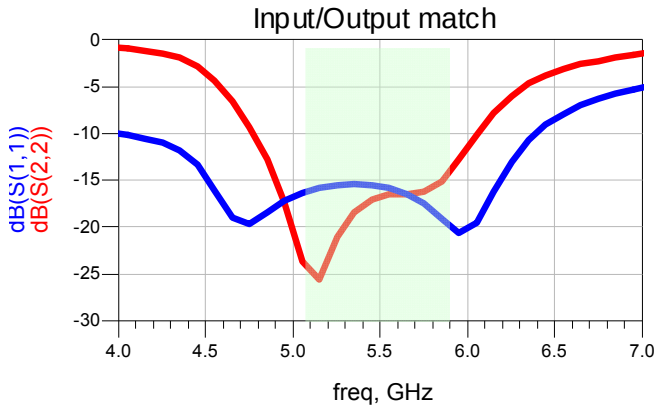

The filter synthesis tool was also used on the input matching network (IMN). Tuning of the IMN enabled the design to meet the input match requirement for the entire band.

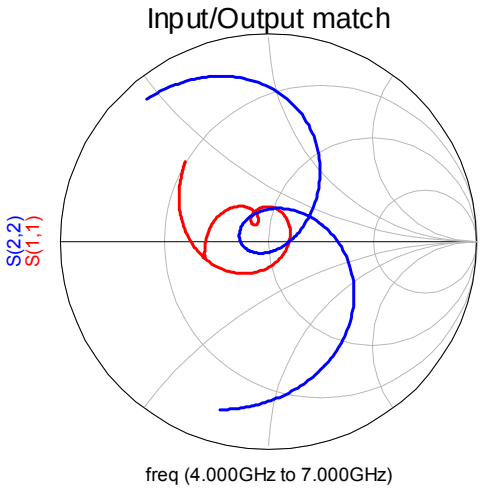
# Simulation

The following graphs depict small signal performance.

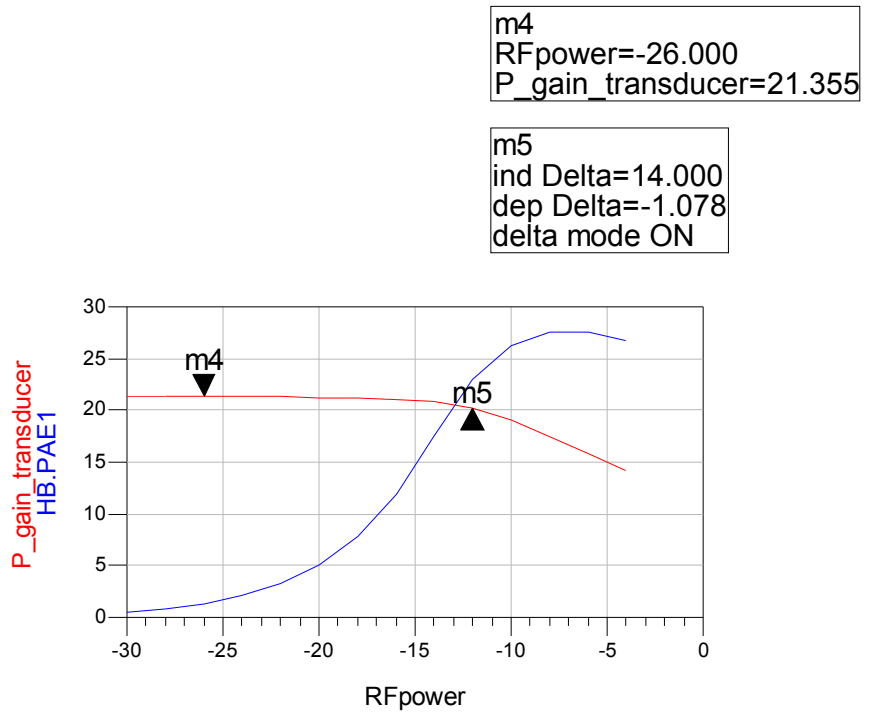


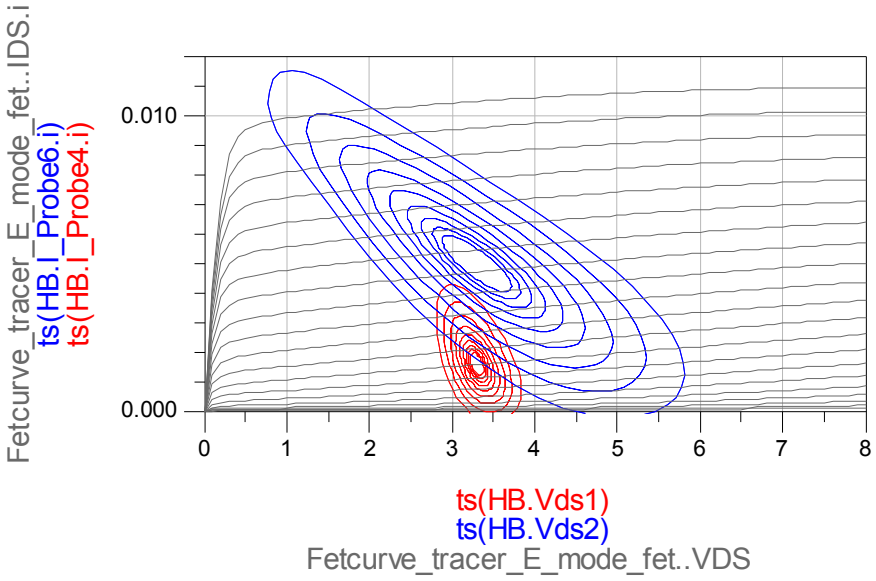



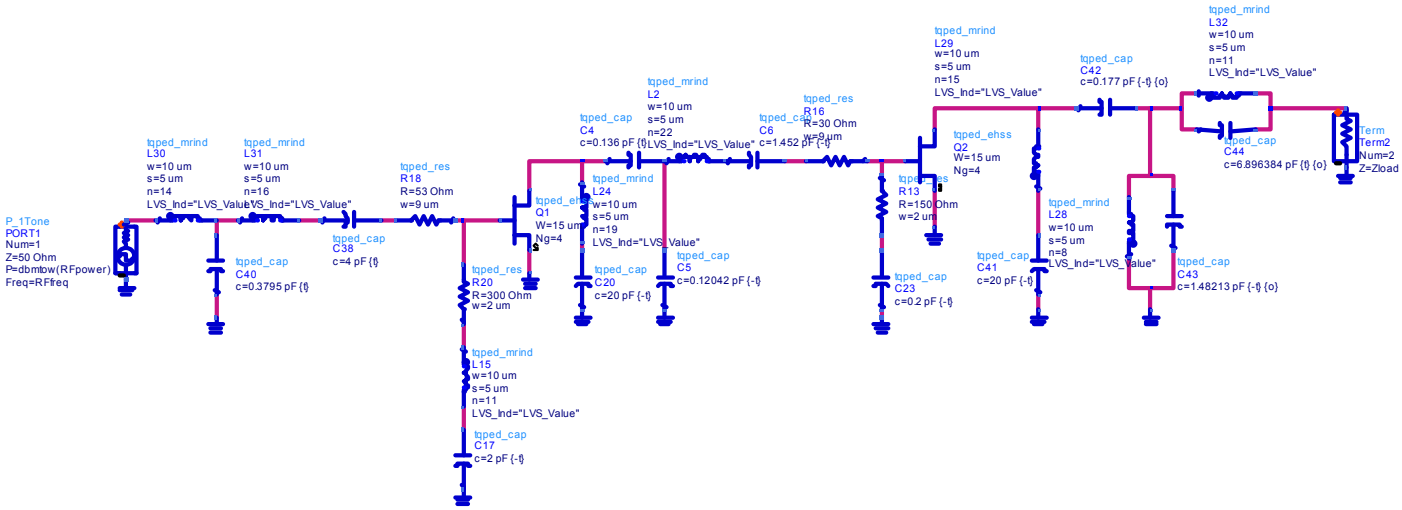
The following graphs depict large signal performance.



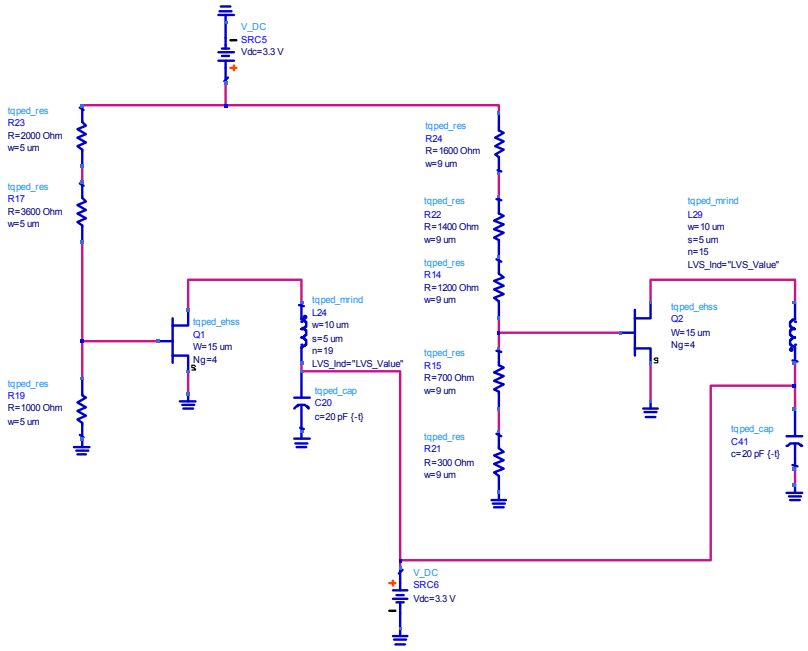



# Schematics

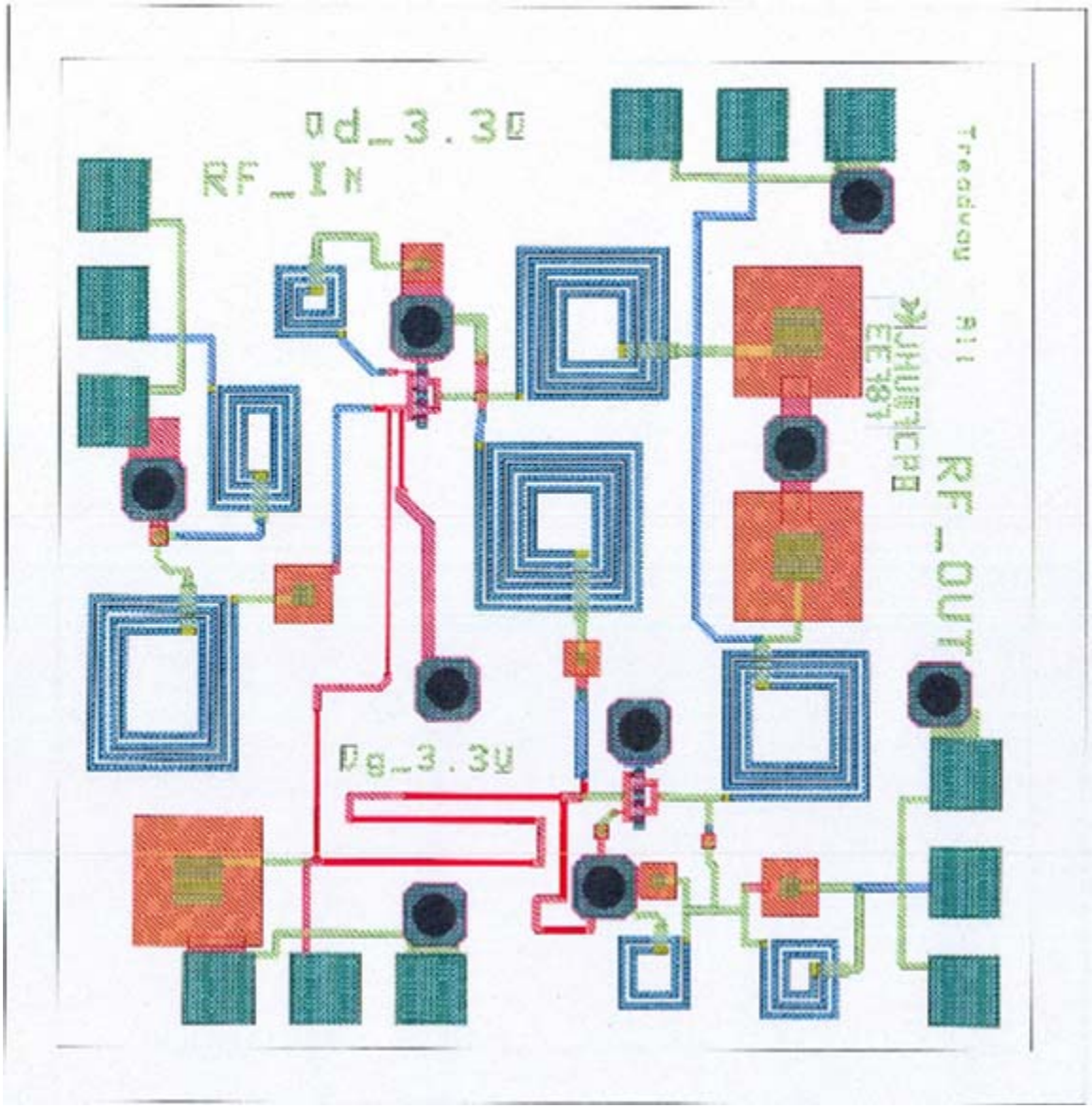
## RF schematic




## DC schematic



## Layout



# Test Plan.

Small signal performance

1. Measure s-parameters on a VNA. Reduce VNA output power to -20dBm. Attach fixture to VNA. Adjust Vg bias supply to 0 V and slowly raise Vd bias to 3.3 V. Verify devices are pinched off. Slowly raise Vg supply to 3.3 V. Verify Vd bias current does not exceed 10 mA.
2. Measure s-parameters from 4 to 7 GHz

Large signal performance.

1. Perform Pin/Pout test. Be sure to drive part into 1 dB compression.
2. Perform test at 5.15 GHz, 5.5 GHz, and 5.875 GHz.

# Broadband Small Signal Amplifier MMIC

**Jeremy Stampfly**

**MMIC Design EE525.787**
**Fall 2007**
**Prof. John Penn**

**Abstract**

This report describes the design, simulations and layout for a five stage GaAs MMIC distributed amplifier. The amplifier is designed to be operated from 2.305 to 5.875 GHz while limiting the gain ripple to less than ±0.5 dB. The broadband small signal amplifier design is a project for the MMIC Design (EE525.787) Fall 2007 class. The TriQuint process is utilized for this design. Each stage of the amplifier utilizes an enhanced pHEMT device.

# Introduction

Broadband performance for amplifiers is desired for small signal amplifiers (SSA), low noise amplifiers (LNA) and power amplifiers (PA). The goal in each case is to produce the desired performance over the greatest bandwidth possible. This report presents a broadband SSA design approach. Two different designs were investigated; the first is a five stage distributed amplifier and the second is a two stage feedback amplifier. Only the distributed amplifier will be presented in this report.

The SSA described here is to operate over a bandwidth of 3.575 GHz while meeting the performance specifications listed in table 1 (page 3). The greatest challenge in this design is to obtain the desired performance while limiting the device power per pHEMT to 10 mW or less. The design is also limited to a single power supply. Later in this report it will be shown that amplifier size, device power and small signal gain were compromised to meet the bandwidth and gain ripple specifications.

Agilent Technologies, Advanced Design System (ADS) 2006A software was used to design, perform simulations and produce a layout for the distributed amplifier. The TriQuint Semiconductor TQPED pHEMT process was utilized for this design.

# Design Approach

The design specifications for the broadband SSA are listed in table 1 (page 3). Two possible designs were considered for this project. The first was to use a cascaded feedback amplifier design. This design limits the number pHEMT devices in order to limit the power consumption of the amplifier while meeting the gain and bandwidth requirements. The other design is a distributed amplifier; distributed amplifiers have good gain-bandwidth performance. Distributed amplifiers don't have the high gain or low noise performance of other designs. However, this type of amplifier can produce similar gains over a wider bandwidth. The distributed design was chosen for this project.

Initially 60 um (4x15) Emode pHEMT devices were used. These devices were biased at 3.3 VDS, 0.5 VGS and 3 mA IDS. In order to meet the small signal gain requirement a cascaded four stage design (8 total pHEMT devices) was used. While limiting each device to 10 mW per device the designer was unable to meet the bandwidth and gain ripple requirements. However, when the device size was increased to 300 um

(5x20) devices it was trivial to meet all of the specifications except for device power. Specification relief was given in order to move forward on the design. The output power, small signal gain and device power requirements were lowered to best effort. Authorization was given by the instructor to use up to 60 x 90 mil ANACHIP layout.

| Parameter | Specification | Goal |
|---|---|---|
| Frequency (MHz) | 2305 – 5875 | - |
| Bandwidth | > 3575 | - |
| Gain small signal (dB) | > 18 | 22 |
| Gain Ripple (dB) | ±0.5 | - |
| VSWR,50 Ohm | <1.5:1 input & Output | - |
| Supply Voltage (VDC) | 3-3.6 | 3.3 |
| Size | 60 x 60 mil ANACHIP | - |
| Power (mW) | < 10 per device | - |

**Table 1** – Broadband small signal amplifier design specifications. The first column on the left lists the design parameter and the units of the parameter. The middle column lists minimum design specifications. The right column lists the design goals that exceed the specifications.

When designing the amplifier first ideal inductors were utilized. TQPED resistors and capacitors were utilized during the entire design process. A voltage divider network is used to provide both the drain and gate voltages from a single power supply. A large inductor is used in all of the simulations to represent a long wire from the supply to the circuit. The RF is blocked from the DC power supply by large 20 pF capacitors.

The amplifier circuit consists of six inductors on the gate line. One inductor is placed before the first pHEMT and one after the final pHEMT. An additional inductor is placed between each device. Both the drain and gate lines have the same number of inductors. The inductors on the drain line are distributed similarly to the gate line. There is an additional inductor that matches the voltage divider to the drain line of the circuit. These inductors along with the device size of each pHEMT were adjusted independently to compromise between small signal gain, bandwidth and gain ripple. Each of these components can be seen in figure 8 (page 8). Additionally, terminating resistors are used on both the gate and drain lines to minimize disruptive reflections in the circuit.

Simulation using ideal inductors produced a small signal gain performance in access of 17 dB across the target band. Next, the TQPED inductors were substituted in the circuit for the ideal components. The Induct_fndy1.exe program was utilized to compute the number of segments and dimensions of the inductor to produce the target inductance. After the replacement of the ideal components with the TQPED comments the circuit was optimized for best performance.

The last step in the design process was to place the amplifier components into the layout. The traces of the appropriate lengths were then placed into the schematic and re-simulated. This process took several iterations to produce the final design. After adjusting the inductor dimensions the trace length were updated.

## Simulations

Each of the simulation in figures 1 – 5 (pages 4-6) were performed using the amplifier design with TQPED components. Figure 1 (page 4) is a plot of the gain (S21), input match (S11) and output match (S22) verses frequency. Five markers were used to examine the gain ripple. The markers were placed at 2.3, 3, 4.8 and 5.9 GHz. The greatest difference in gain is 0.91 dB. Therefore the gain ripple is less than ±0.5 dB. Notice also that the output match is optimized for 4.1 GHz with a match of greater than 35 dB. The input match is greater than 15 dB for the entire bandwidth of interest. Also, the amplifier has a gain and ripple that is consistent down to approximately 1 GHz. A bandwidth of over 4.5 GHz has been achieved. However, the minimum small signal gain specification was missed by almost 3 dB at 5.875 GHz and 2 dB at 4 GHz.

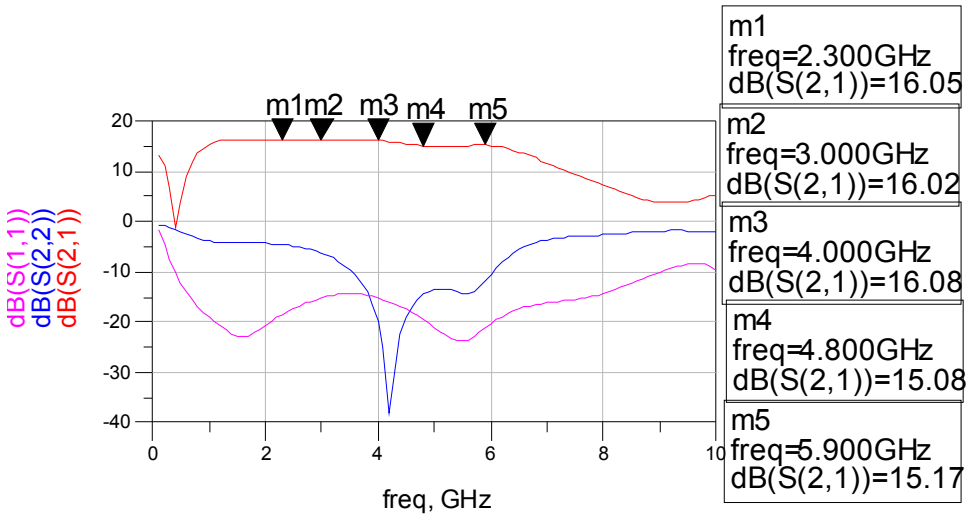



**Figure 1** – Small signal gain plot. The Gain (S21), and input match (S11) and output match (S22) plotted verses frequency. The simulation was performed from 100 MHz to 10 GHz.

Figure 2 (page 5) contains plots of the noise figure (top left), input and output matches and stability (top right), VSWR (bottom left) and stability verses frequency. The simulation was performed from 100 MHz to 10 GHz. The noise figure at each band edge is approximately 3.5 dB. The minimum noise figure is found at 4 GHz to be approximately 1.6 dB. The VSWR between 4 and 5 GHz exceeds the design specifications. Both the input and output VSWR are less than 1.5. The VSWR performance below 4 GHz and above 5 GHz are both outside of the specified levels.

Each gradually increases to levels approaching 5 at the band edges. Both stability plots indicate that the circuit will be stable between 100 MHz and 10 GHz.

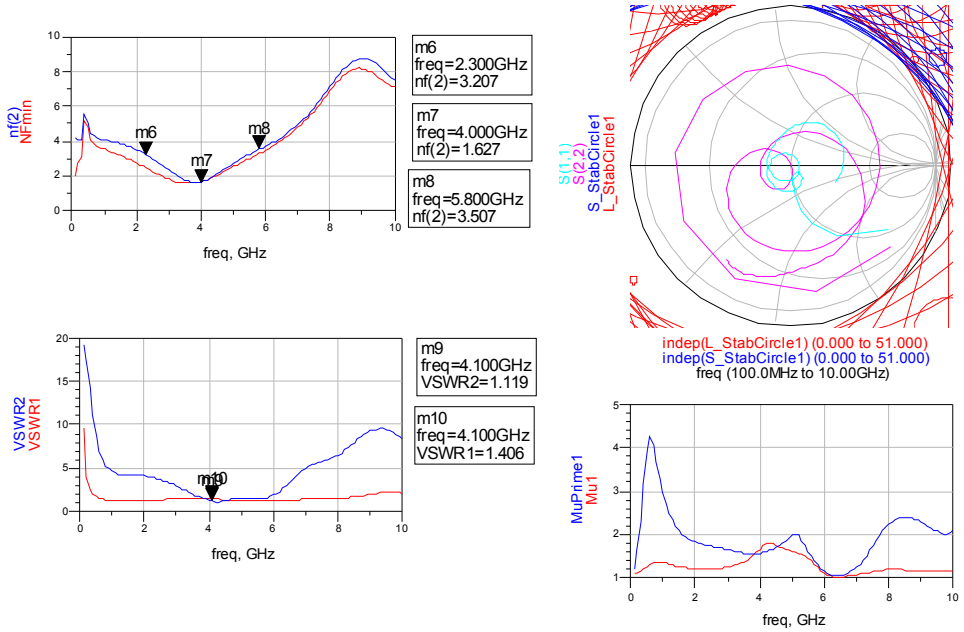



**Figure 2** – Noise figure verses frequency (top left), input and output match and stability (top right), VSWR verses frequency (bottom left) and input and output stability verses frequency (bottom right). Each of these simulations were performed from 100 MHz to 10 GHz.

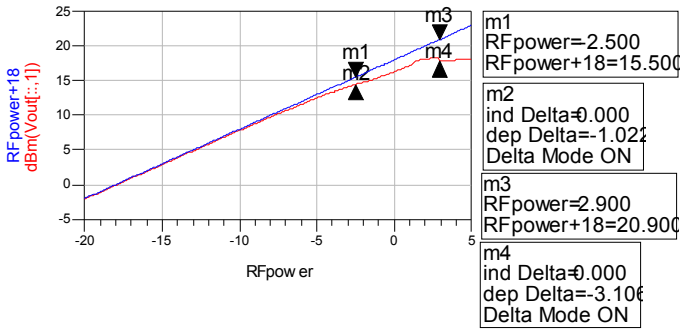



**Figure 3** – Plot of input power (dBm) verses output power at 2305 MHz. The 1 dB compression point is at markers 1 and 2. The 3 dB compression points are at markers 3 and 4.

Figures 3-5 (pages 5, 6) are plots of the input output power verses input power at 2.305, 4.09 and 5.875 GHz. In each of the three plots the 1 dB and 3 dB compression points are marked. In figure 4 the 1 dB compression point is at –2.5 dBm of input power. The 3 dB compression point is at 2.9 dBm of input power. In figure 4 the 1 and 3 dB compression points are at 0.9 and 4.8 dBm of input power respectively. In figure 5 the 1 and 3 dB compression points are at –3.9 and 3.7 dBm of input power respectively. The data indicates that the greatest input power at the 1 and 3 dB compression point is achieved at the center frequency. In both figures 3 and 4 the simulations appears to break down at approximately 2 dB of input power. In figure 5 the simulation appears to behave as anticipated.

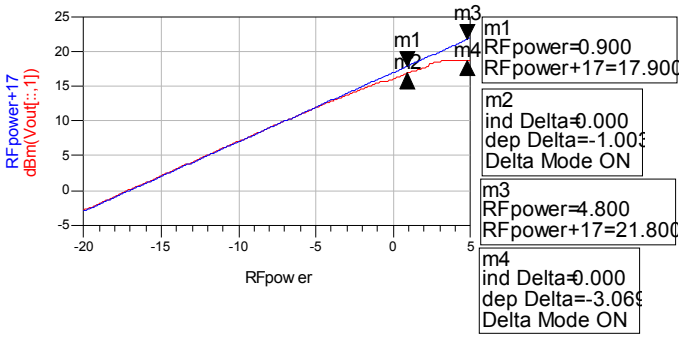



**Figure 4** – Plot of input power (dBm) verses output power at 4090 MHz. The 1 dB compression point is at markers 1 and 2. The 3 dB compression points are at markers 3 and 4.

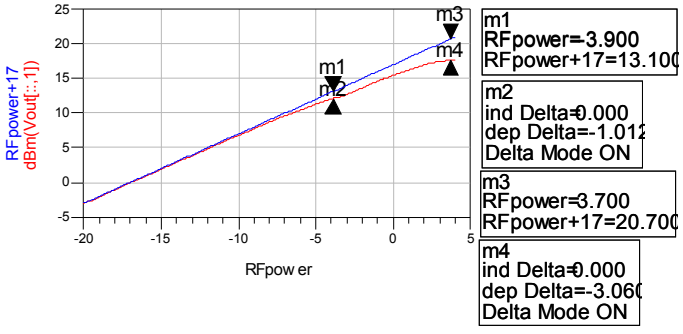



**Figure 5** – Plot of input power (dBm) verses output power at 5875 MHz. The 1 dB compression point is at markers 1 and 2. The 3 dB compression points are at markers 3 and 4.

# DC Analysis

The amplifier is supplied with a single 3.3 VDC external power supply. A voltage divider is used to reduce the input voltage to 0.6 VDC. This voltage is used to bias the gates of the enhanced devices. The first device has 3.27 VDC applied to the drain of the device. The voltage is reduced with each device. At the fifth device the drain voltage is 3.21 VDC. Bitmaps of the drain (left) and gate (right) voltages are in figure 6 (page 7).

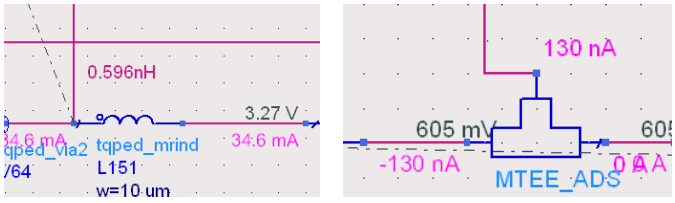



**Figure 6** - Drain Input (left), Gate Input (right)

Figure 7 (page 7) displays the DC analysis of the five devices that are used in the amplifier. The devices are displayed in the order that they are used in the circuit. The device that is closest to the input is located on the left in the figure. The device that is closest to the output is on the right of the figure. The drain voltage and current for the five devices are tabulated in table 2 (page 7) along with the device power consumption. The total power consumption for the entire amplifier is 115.2 mW.

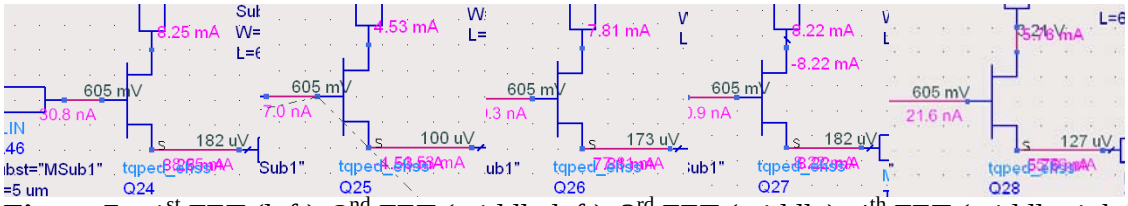



**Figure 7** – 1st FET (left), 2nd FET (middle left), 3rd FET (middle), 4th FET (middle right) and 5th FET (right).

| Device Number | Drain Voltage (VDC) | Drain Current (mA) | Device Power Consumption (mW) |
|---|---|---|---|
| 1 | 3.27 | 8.25 | 27 |
| 2 | 3.24 | 4.53 | 14.7 |
| 3 | 3.22 | 7.81 | 25.1 |
| 4 | 3.21 | 8.22 | 26.4 |
| 5 | 3.21 | 5.76 | 18.5 |

**Table 2** – Drain voltage (VDC), drain current (mA) and device power consumption (mW) for the five enhanced devices.

# Schematic

This section contains schematic of the entire distributed amplifier (figure 8, page 8), RF input and voltage divider (figure 9, page 8), pHEMT devices (figures 10-12, pages 9-10) and RF output (figure 12, page 10). The DC bias voltages and current are supplied in the upper left corner of figure 8 (page 8). The RF input is supplied in the lower left corner and RF output is in the lower left corner of figure 8 (page 8).

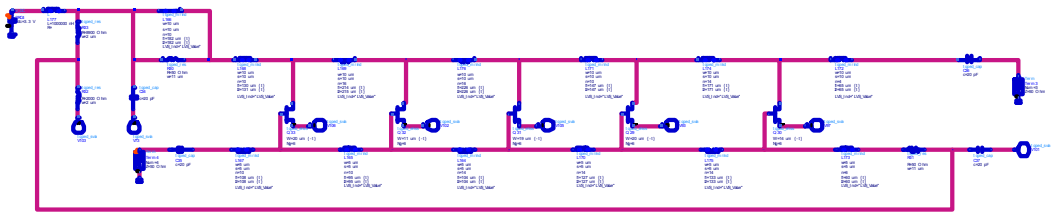


**Figure 8** – Schematic for a five stage distributed amplifier. Included are voltage divider and RF input and output.

Figure 9 (page) is an expanded view of the DC distribution and RF input. The gate voltage is developed using a voltage divider. The drain voltage is supplied through the inductor L166 and terminating resistor R30.

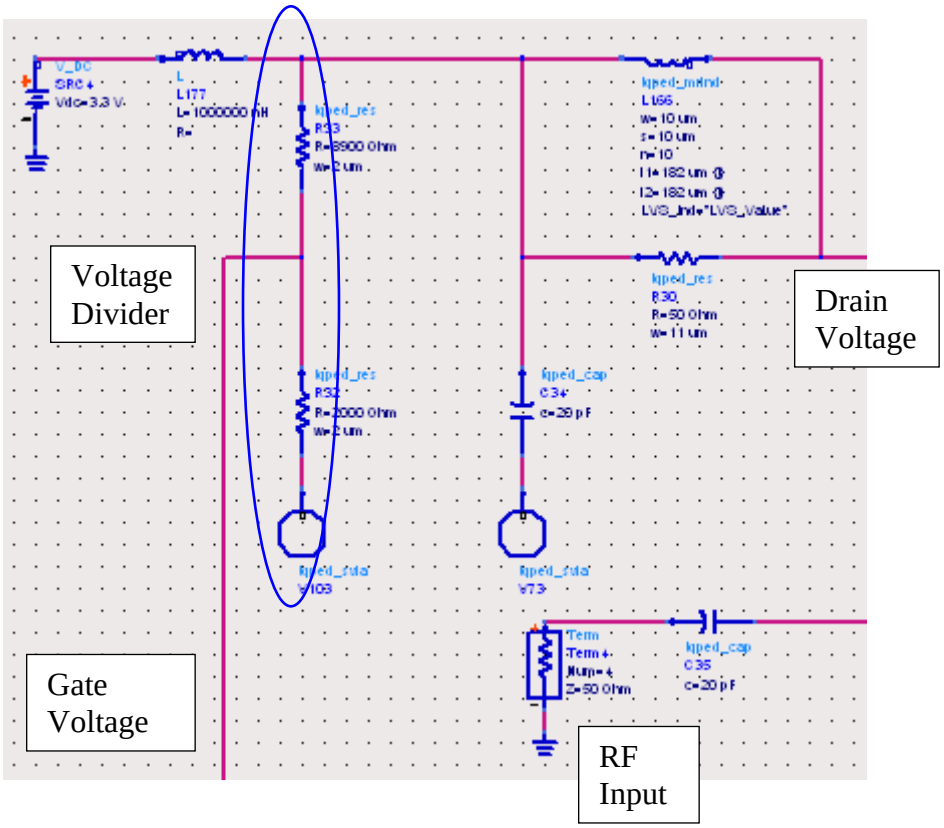



**Figure 9** – DC supply and RF Input for the distributed amplifier. A voltage divider is utilized to enable single source operation.

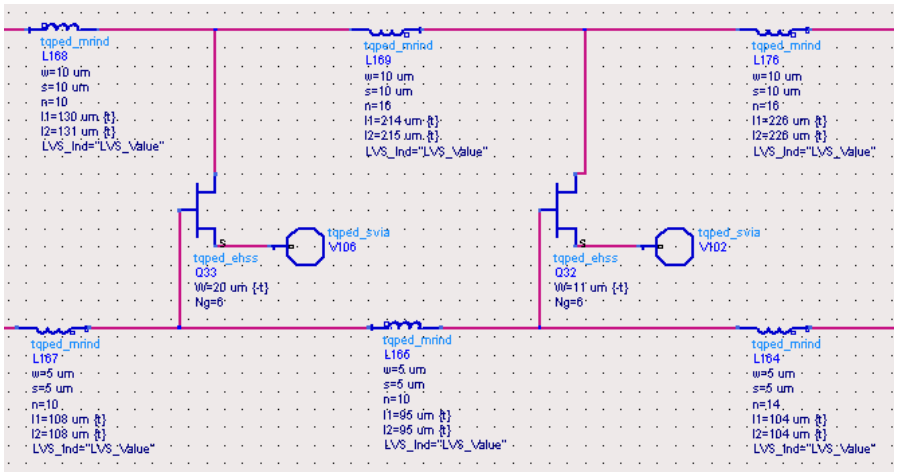



**Figure 10** – First to pHEMT devices from the input.

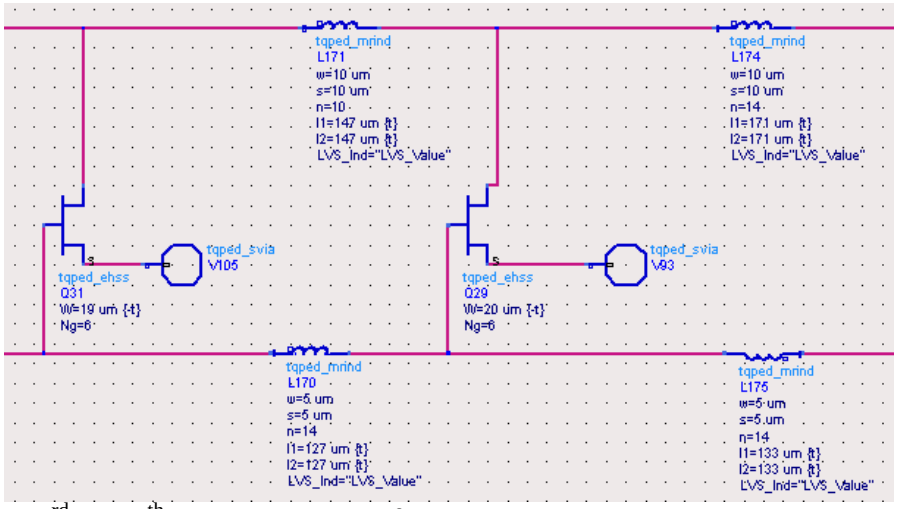



**Figure 11** – 3rd and 4th pHEMT devices from the input.

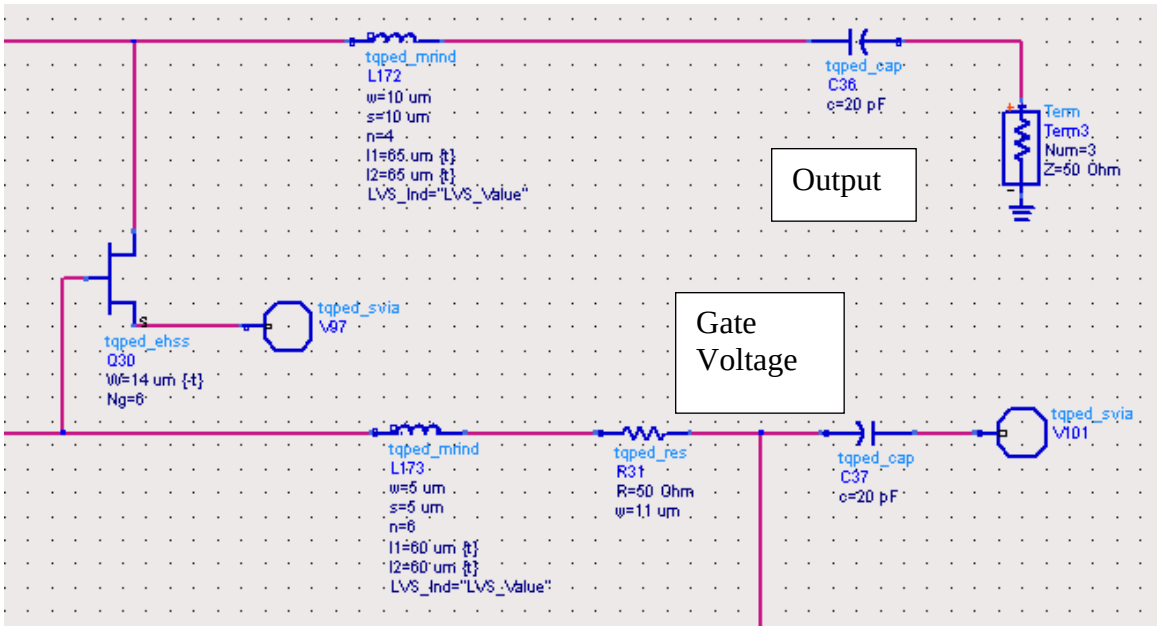



**Figure 12** – Last pHEMT device with RF output and gate voltage input.

## Layout

Figure 13 (page 11) is an illustration of the distributed amplifier layout. The layout occupies a 60 x 90 mil area. The RF input is located in the upper left corner of the circuit. The DC input is in the upper right corner and the RF output is in the lower right corner of the circuit. The pHEMT devices and associated inductors are placed in the layout in order from the input to the output. The voltage divider is placed across the top of the circuit.

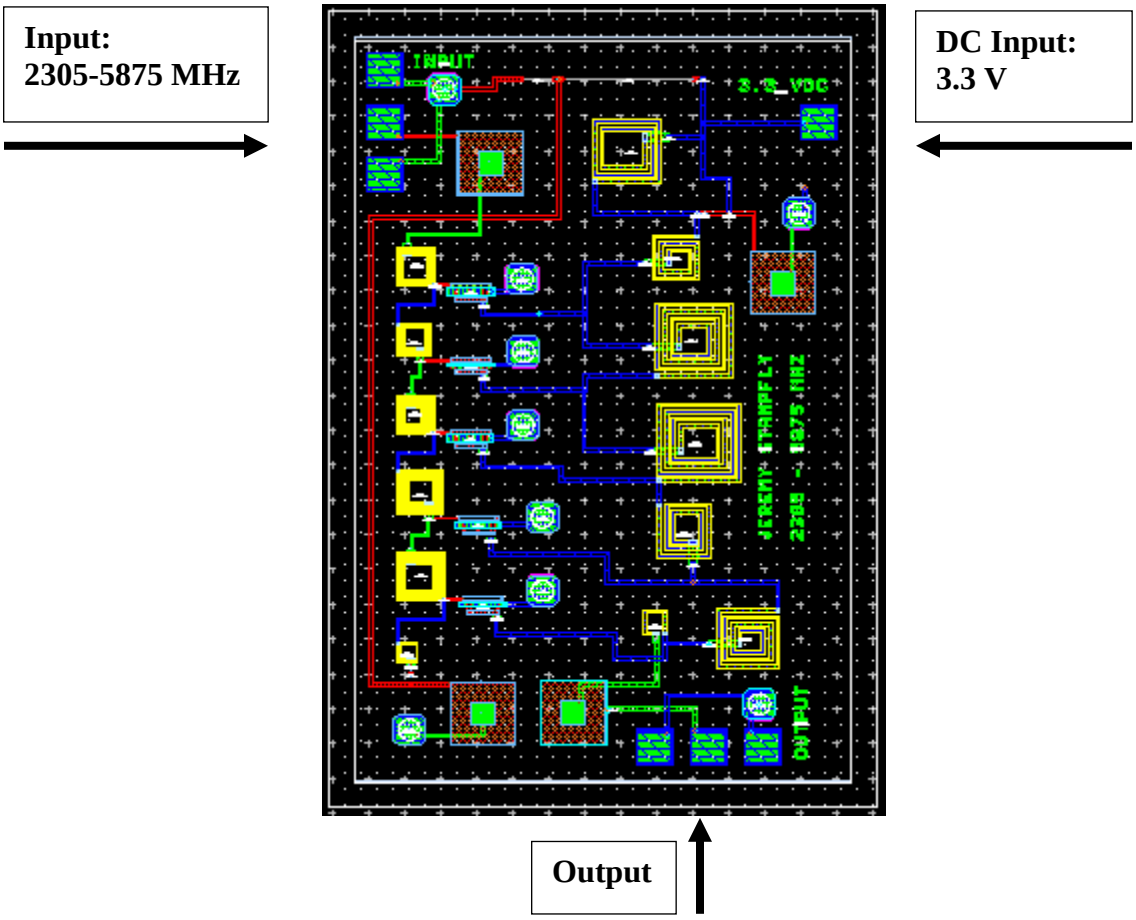



**Figure 13** – Layout of the distributed amplifier. The RF input is in the upper left corner of the circuit. DC input is in the upper right corner of the circuit. RF output is lower right corner of the circuit. The circuit is designed to operate from 2.305 – 5.875 GHz.

## Test Plan

1. Power up test equipment.
2. Calibrate network analyzer from 100 MHz to 10 GHz.
    a. Calibrate using open, short, thru and load test fixtures.
    b. Power levels are not anticipated to approach the measurement equipment limits.
3. Place circuit into the test fixture and connect RF input and output probes as shown in figure 13 (page 11).
4. Set DC supply to 3.3 V, 0 A.
5. Increase current until the circuit is drawing 34.6 mA.
6. Perform s-parameter measurements from 100 MHz to 10 GHz.
7. Connect frequency synthesizer to the input port.
8. Connect a spectrum analyzer to the output port.
9. Set frequency to 2.305 GHz and sweep the power from –20 to 5 dBm.
10. Repeat step 9 at 4.09 GHz.
11. Repeat step 9 at 5.875 GHz.

# Conclusion

Distributed amplifiers have good gain-bandwidth performance. This type of amplifier is a good choice for applications where noise figure and power consumption are not critical. In this design a bandwidth of 4.5 GHz was achieved with the worst gain in that band being approximately 15.2 dB. Distributed amplifiers can be cascaded to improve the gain performance of the design. For battery operated system the distributed amplifier is not recommended.

# A 3.3V, 2.4GHz 0.5μm GaAs Common-Source, Two-Stage Low-Noise Amplifier

by

Erica Simcoe

A Design Project submitted in fulfillment
of the requirements for

EE787 MMIC Design Course

JOHNS HOPKINS UNIVERSITY

December 11, 2007

## ABSTRACT

*Abstract* — This paper presents a 3.3V battery operated, 0.5µm Gallium Arsenide (GaAs) low-noise amplifier (LNA) operating at 2.4GHz. Using a common-source configuration with two stages and EMODE pHEMT transistors, the designed amplifier provides a noise figure of less than 2.2dB in conjunction with a power gain of greater than 26dB. Focusing on a low power consumption design, this LNA operates using a 3.3V battery and draws less than 20mW. A shunt resistor on the drain along with a feedback resistor between the drain and gate were utilized to eliminate potential stability problems. The ideal elements are replaced with the foundry library elements and a layout is generated in preparation for fabrication. A test plan is discussed for evaluating the fabricated device and allowing for a comparison of the measured results to the simulated performance.



*Keywords* — MMIC, 0.5µm Gallium Arsenide (GaAs), Low-Noise Amplifier, Common-Source


## 1. INTRODUCTION

The overall theme of the design project for the Johns Hopkins University EE787 Microwave Monolithic Integrated Circuit (MMIC) Design course is a configurable S-band or C-band duplex transceiver. This paper will focus on the S-band frequency regime of the project, particularly the design and development of a low-noise amplifier (LNA). The S-band frequency range of interest is from 2.305 to 2.497 GHz, covering the wireless communications services (IEEE 802.11, Bluetooth, Wireless LANs) and the Industrial, Scientific, and Medical (ISM) radio bands. One key aspect of this project is that it will concentrate on small, lightweight, and low power designs that will be intended for battery powered operation, from 3.0 V to 3.6 V.

In a RF transceiver, the LNA is the first component in the receiver subsystem. Designed for low noise figure, the LNA is used to bound the receiving systems' overall noise figure. A low noise figure allows weak received signals to be amplified with minimal additive noise and distortion, thus increasing the dynamic range of the receiver. Large gain in the first stage of the receiving chain also factors into setting the overall noise figure of the receiver; however, a high gain and low noise figure amplifier is difficult to obtain using a single-stage design. Therefore, multi-stage designs are utilized to incorporate both of these desired traits.

This paper details the design of a 2.4GHz, 0.5µm GaAs common-source, two-stage LNA powered by a single 3.3V battery. Two 4 X 15um (60um) EMODE pHEMTs are used in the design due to their high gain and low noise characteristics with low bias power. Several aspects of the design affect the amplifiers performance. First, the output and intermediate matching networks are used to obtain maximum gain as well as to maintain a good impedance match. Second, the input matching network sets the noise figure for the design. Lastly, a feedback circuit in addition to a shunt impedance is used on each of the amplifier stages to stabilize the amplifier and reduce power consumption.

## 2. LNA TOPOLOGY

Various topologies exist for LNA circuits, but the common-source topology was chosen for this design. A common-source design has the RF input signal applied to the gate of the transistor while the amplifier RF output signal is extracted from the drain. Any stabilizing resistors must be implemented on the output of the transistor so the thermal noise introduced is post-amplification. The input and output matching networks perform impedance transformations to provide noise and power matching, respectively. Ideally, an LNA would have low noise and high gain characteristics. However achieving power matching and noise matching require two different approaches that often result in two different solutions. Maximum output power occurs when the input impedance equals the conjugate match of the source impedance, resulting in $\Gamma_{in} = \Gamma_s^*$. The condition for minimal noise is met when $\Gamma_s = \Gamma_{opt}$. An input matching network (IMN) is designed to impedance match $\Gamma_{opt}$ of the transistor to 50Ω, where $\Gamma_{opt}$ is the optimum reflection coefficient for the lowest noise figure at a particular frequency. Figure 1 illustrates a common-source low noise amplifier circuit with stabilizing resistor, IMN, and OMN.

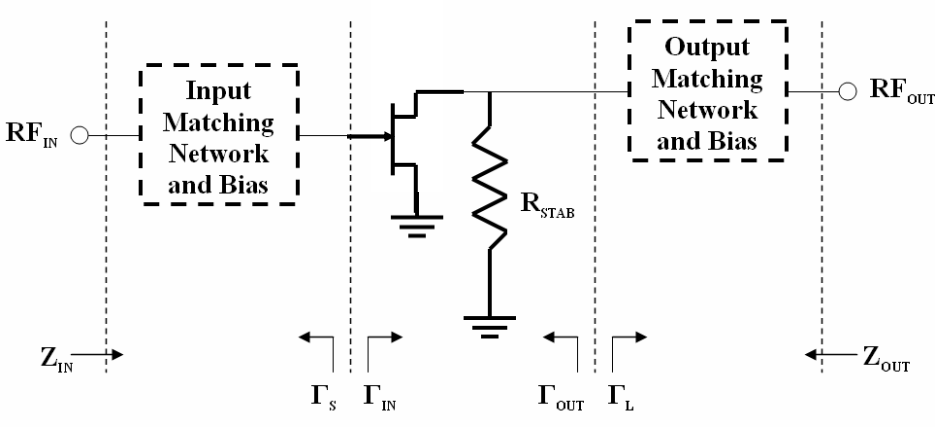



Figure 1. Common-Source LNA Topology

To achieve a high gain LNA, a two-stage design is employed. This architecture allows for the first stage to be designed with an extremely low noise figure, hence setting the overall noise figure of the LNA. Then the second stage provides the necessary amplification to achieve an overall high gain.

## 3. SIMULATION SOFTWARE PACKAGE AND FOUNDRY

### 3.1 SIMULATION SOFTWARE PACKAGE

Agilent Technologies Advanced Design System (ADS), version 2006A, was used as the simulation software package for this project. Linear and nonlinear circuit simulations were used to analyze the performance of the LNA, while the tuning and optimization capabilities were exploited to finalize the design. Elements in the TQPED process library from TriQuint Semiconductor were used to create a final design that accounts for parasitics in these non-ideal components.

### 3.2 FOUNDRY

TriQuint Semiconductor provides custom foundry services with capabilities including Gallium Arsenide (GaAs) wafer processing. Using proprietary libraries developed by TriQuint Semiconductor that are compatible with Agilent Technologies ADS simulation software package, more realistic simulations were performed and analyzed in the development of the LNA. The TQPED library, version 2.2, was used for the simulations provided in this paper.

## 4. DESIGN APPROACH

### 4.1 BIASING

The first step in the design process is to determine the DC operating point. This is accomplished by sweeping the drain voltage (VDS) and the gain voltage (VGS) of the transistor. The EMODE pHEMT is used in calculating the DC IV curves, shown in Figure 2. It is determined that an appropriate bias for the LNA is:

VDS = 2.4 V
IDS = 3 mA
VGS = 0.58 V

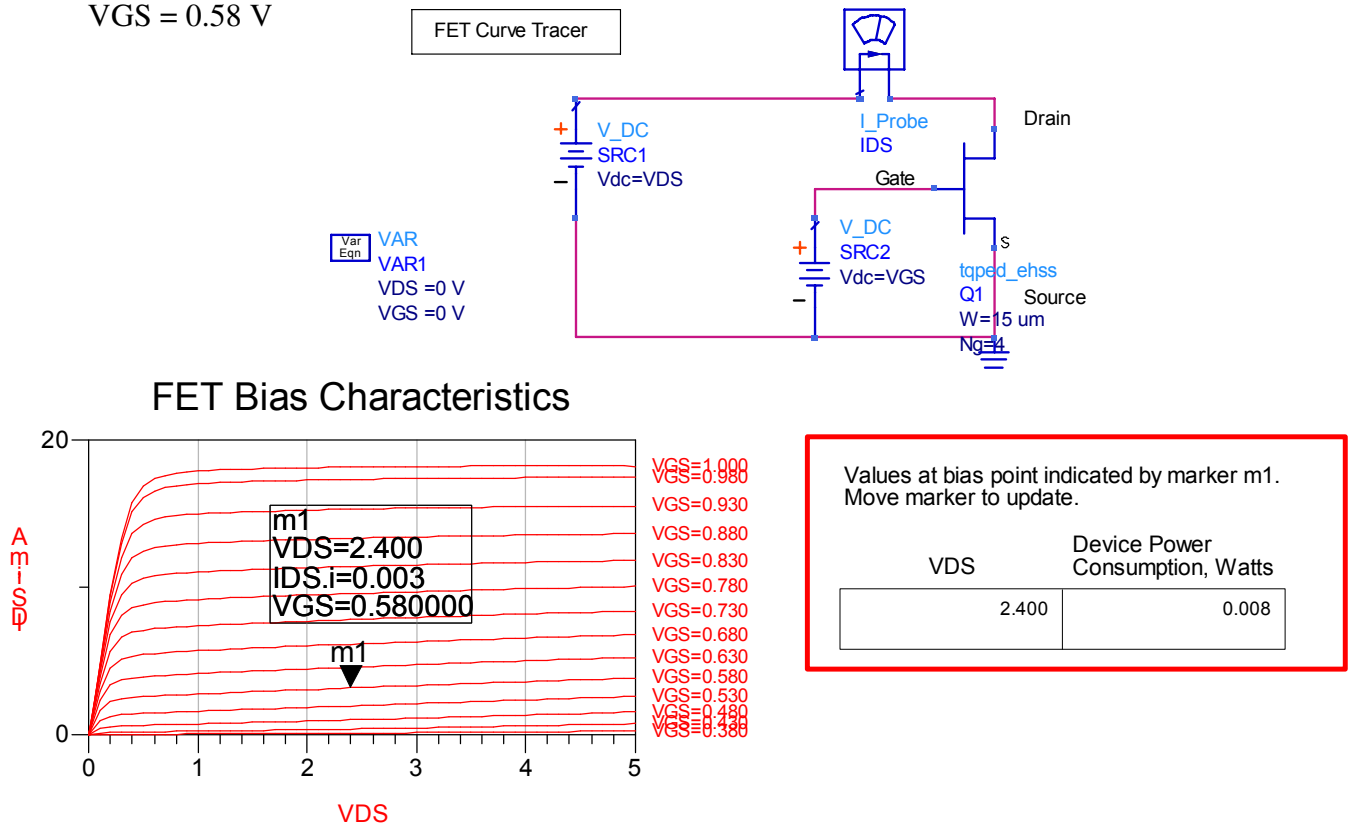



Figure 2. Determining an Appropriate DC Bias

Note that the biasing gate voltage is positive because the pHEMT is an EMODE. With this bias point the DC power for a single stage is 8 mW. The above bias voltages are less than the battery operating limits of 3.0V – 3.6V. Therefore, a resistor divider network will be used to drop voltage when the biasing network is designed. Initially ideal bias components are used when designing the LNA, and these will be replaced with nonideal components once the amplifier is completely designed.

## 4.2 STABILITY

The next step in the design process is to stabilize the transistor. Because the LNA is being designed for a minimum NF, the stabilizing network should be placed on the output side of the LNA. Two methods of stabilizing the transistor were studied, (1) a feed back resistor between the drain and gate, and (2) a shunt resistor on the drain. Both of these options were attempted separately, but neither provided unconditional stability. However, when used in conjunction with one another, the LNA became unconditionally stable from 100 MHz to 10 GHz.

Since the LNA is being designed to operate via a battery, it is essential to minimize wasted power loss in any portion of the stabilizing network. Therefore, DC blocking capacitors were used in series with the stabilizing resistors to minimize the amount of power dissipated by the resistors. DC blocking capacitors are also utilized to isolate the inter-stages of the amplifier in addition to the external RF ports on the amplifier from the various bias voltages.

## 4.3 INPUT AND OUTPUT MATCHING NETWORK

Subsequently the input matching network was designed for the best possible noise figure and the output matching network was designed for maximum gain as well as the best input and output match. Both networks are comprised of series capacitors and shunt inductors. It should be noted that all components are ideal in this initial design phase, including the components used in the previously discussed stabilizing network.

## 4.4 IDEAL SINGLE-STAGE DESIGN

After designing the input and output matching networks, a single-stage design is complete. Favorable results were obtained after simulating the design:

Gain = 13.6 dB
NF = 1.5 dB
Match (input) = –10 dB.
Match (output) = –46 dB

## 4.5 IDEAL TWO-STAGE DESIGN

After the ideal single stage design yielded promising results, two identical single stages were cascaded together. The ideal cascaded system provided the following performance:

Gain = 27.9 dB
NF = 1.5 dB
Match (input) = –7.5 dB
Match (output) = –32dB

### 4.6 NON-IDEAL TWO-STAGE DESIGN

Next, the ideal components were replaced with TriQuint components and the design was tuned and optimized. As expected, the performance of the system was degraded due to the parasitic losses modeled in the TriQuint components. The non-ideal cascaded system provided the following performance:

Gain = 26.2 dB
NF = 2.1 dB
Match (input) = –5.0 dB
Match (output) = –40.9 dB.

The last step in the design was to design the DC bias network. To reduce complexity in the layout of the design it is of interest to bring in only one battery to supply the drain and gate voltages for both pHEMTs. Because this LNA is designed for a VDS value less than 3.0 V to 3.6 V a resistor divider network is implemented. One leg of the divider drops the voltage down to approximately 2.4 V to supply the drain voltage and another leg of the divider drops the voltage down to 0.58 V to supply the gate voltages. One single resistor divider network is used to provide power to both pHEMTs.

## 5. SPECIFICATIONS VS GOALS

Table 1 compares the initial design goals to anticipated performance based on the non-ideal design simulations.

Table 1. Design Goals vs. Simulated Performance

| Parameter | Design Goal | Simulated Performance |
|---|---|---|
| Center Frequency [$f_c$] | 2.305-2.497 GHz | 2.4 GHz |
| Bandwidth | > 200 MHz | 200 MHz |
| Gain [$S_{21}$] | > 24 dB | 26.9 dB (nom) |
| Gain Ripple | ±0.5 dB | ±1.0 dB |
| Noise Figure [NF] | < 3 dB | 2.06 dB (nom) |
| Input IP3 | > 0 dBm | -12 dBm |
| Input VSWR | < 1.5:1 | 4.1:1 (nom) |
| Output VSWR | < 1.5:1 | 1.07:1 (nom) |
| Supply Voltage | 3.0 – 3.6 V | 3.3 V |
| Size | 60 x 60 mil ANACHIP | 60 x 60 mil ANACHIP |

## 6. TRADEOFFS

The first tradeoff in this design was encountered near the beginning of the design process. It involved stabilizing the circuit. There was no easy way to stabilize the system without using a feedback network. Initially it was a concern that this topology would feed noise back into the system. However, after running simulations, the noise fed back into the system was not enough to compromise the system. It was still well below the 3dB NF goal.

Another tradeoff encountered was trying to optimize gain and output match as well as noise figure and input match. A nominal gain of 26.1 dB was achieved across the band, while at the same time a 1.4:1 output VSWR was maintained. The gain ripple was not bad, at a value of ± 1 dB, but did not meet the ±0.5 dB goal. Also, a nominal NF of 2.2 dB was achieved. However, the input VSWR was not desirable, at a nominal value of 4.7:1. No way was found to meet the goals for all these parameters simultaneously; such is the nature of a tradeoff.

## 7. FINAL DESIGN

The final design of the two-stage, common-source LNA design using TriQuint library components is presented. Figure 3 illustrates the overall schematic of the final design with the complete bias circuit included.

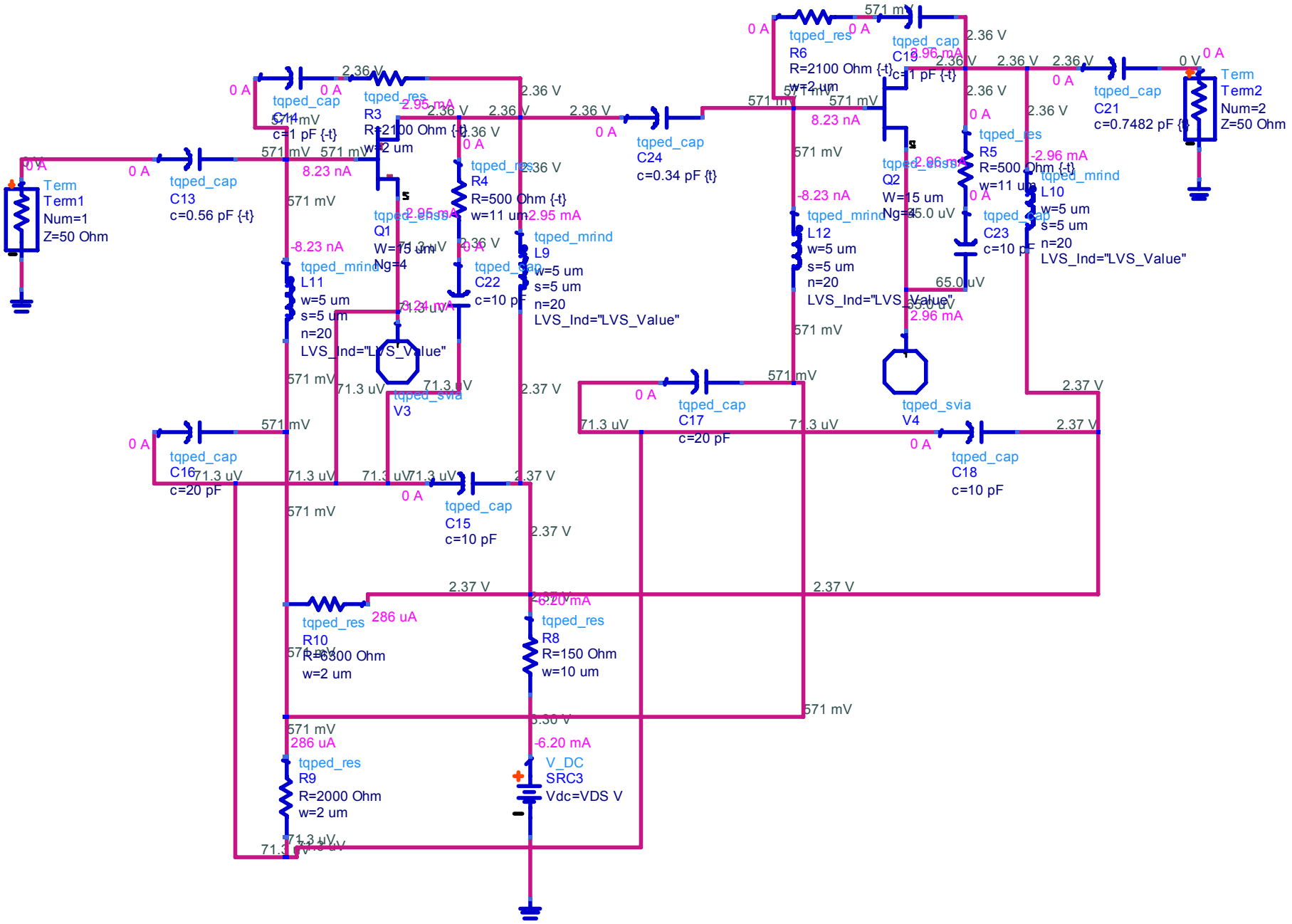



Figure 3. Final Design Schematic with DC Bias

Figures 4a-4d illustrate the simulated S-parameters of the final design. Both a broadband and narrowband view of the response is shown. The markers indicate the performance at the designed center frequency.

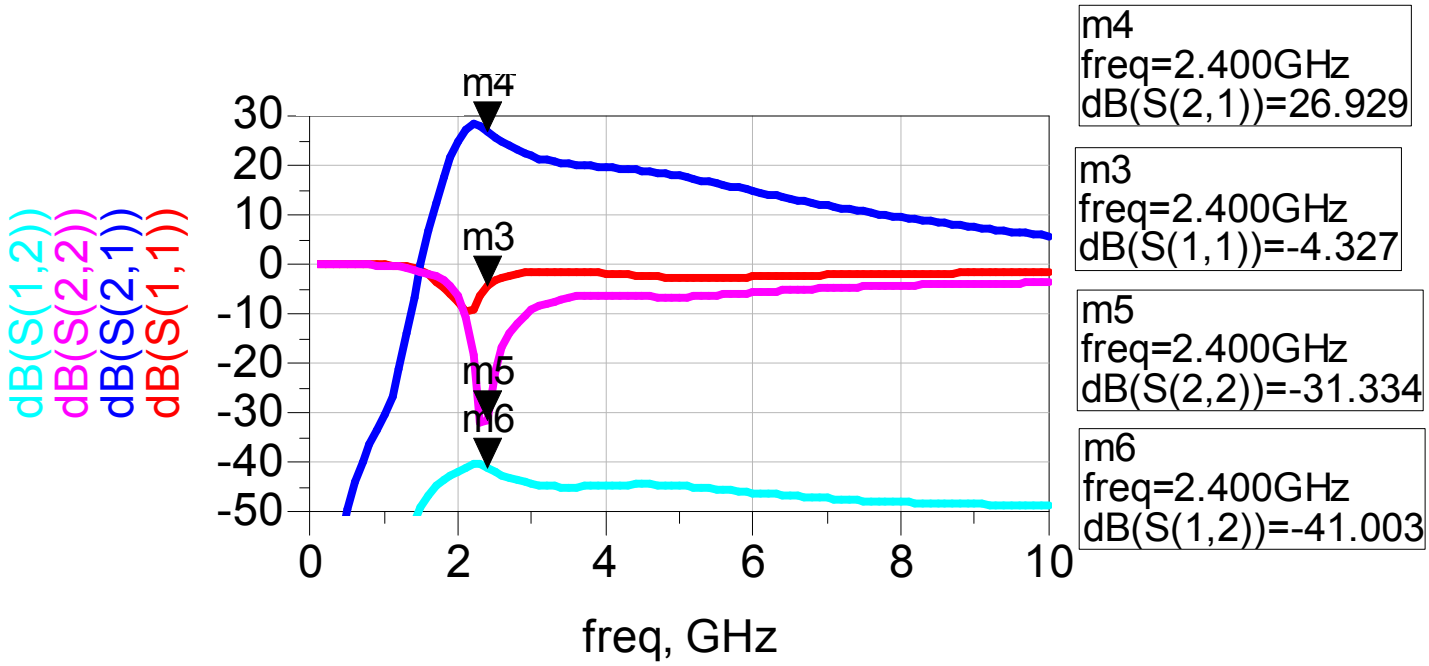



Figure 4a. S-Parameters (Broadband) of Final Design

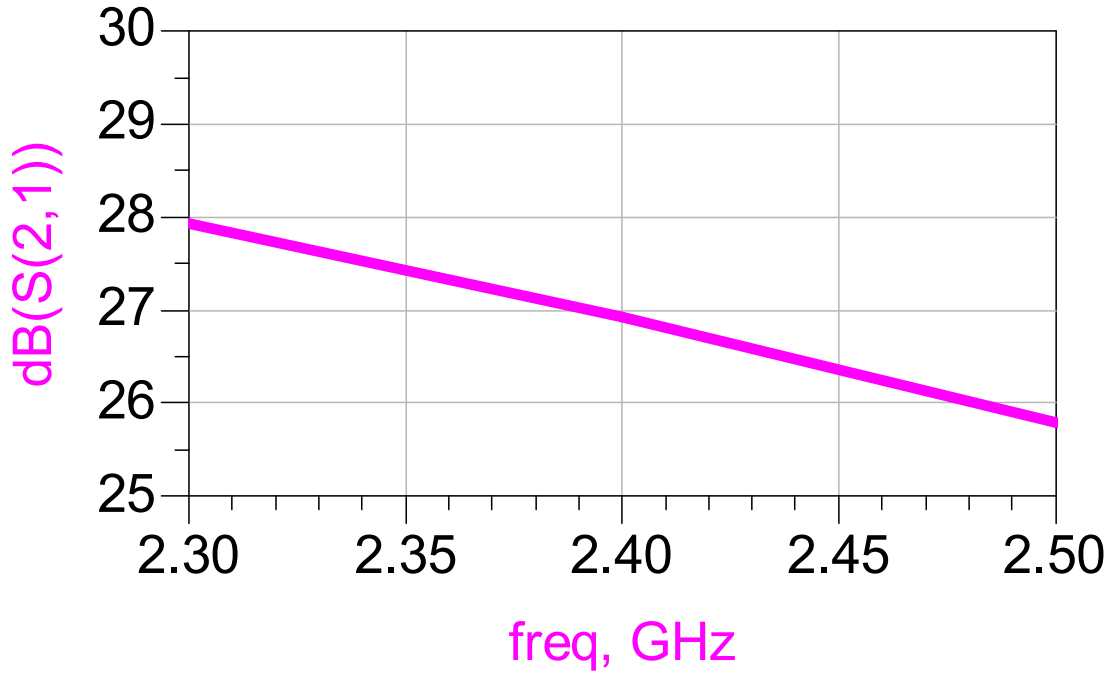



Figure 4b. Gain ($S_{21}$) of Final Design

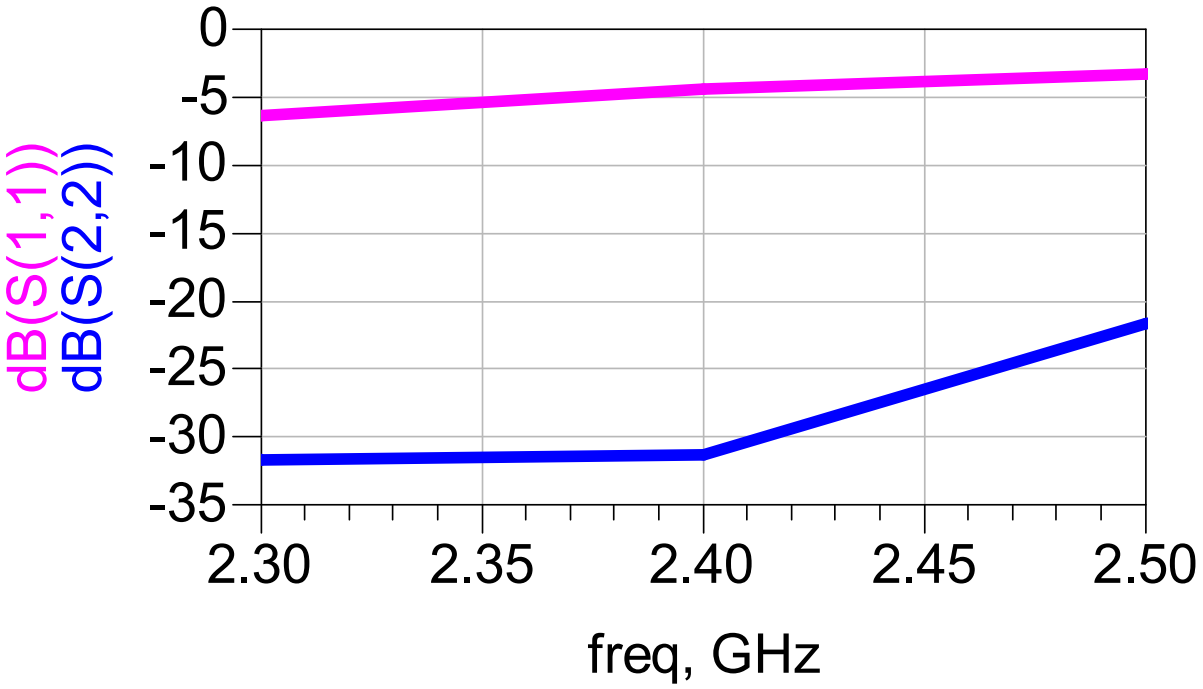



Figure 4c. Input/Output Matching ($S_{11}$/$S_{22}$) of Final Design

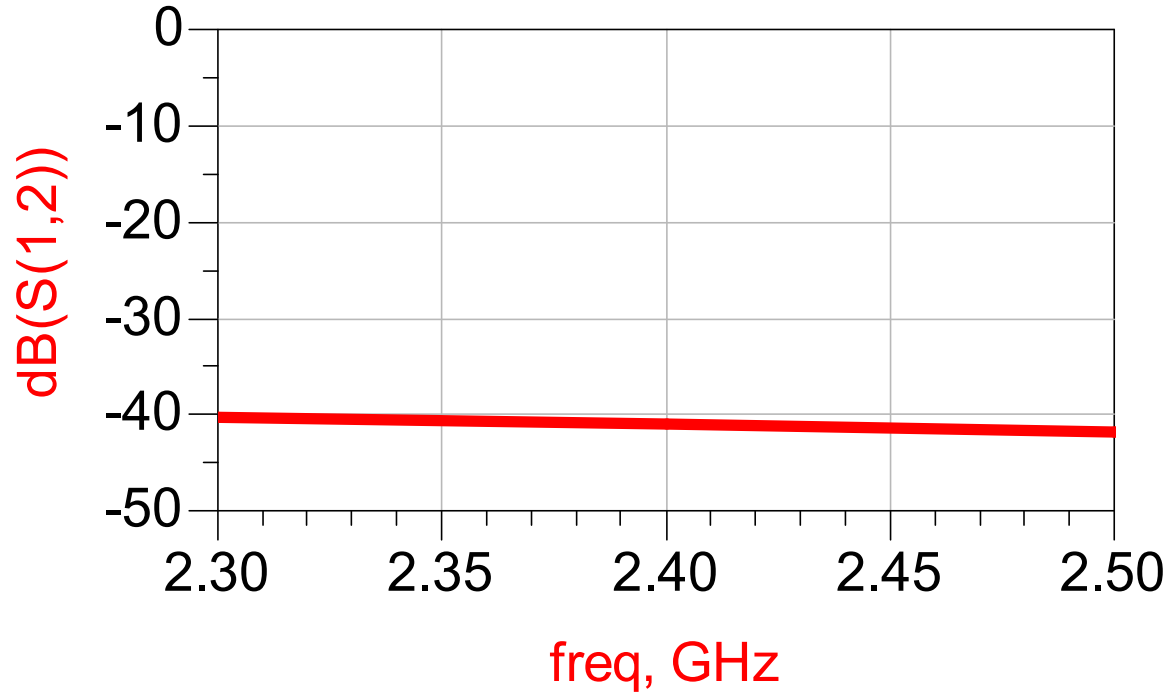



Figure 4d. Reverse Isolation ($S_{21}$) of Final Design

Figure 5a displays the simulated broadband noise figure of the final design and the theoretical achievable minimum noise figure. The markers indicate the performance at the designed center frequency. A narrowband view of the response is shown in Figure 5b.

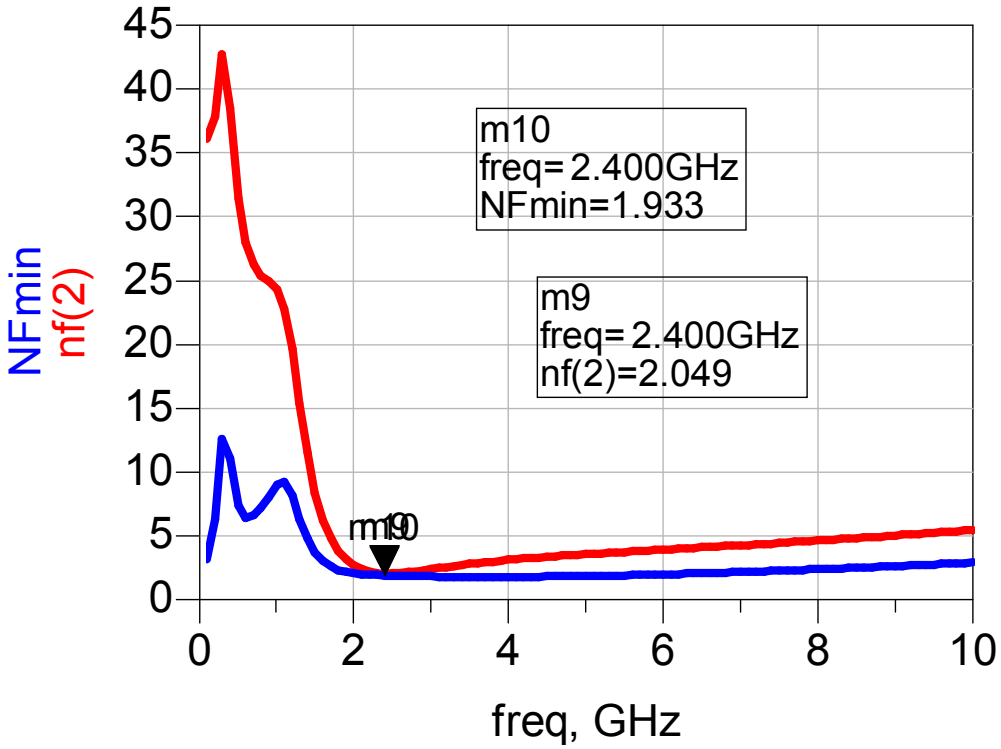



Figure 5a. Noise Figure (Broadband) of Final Design

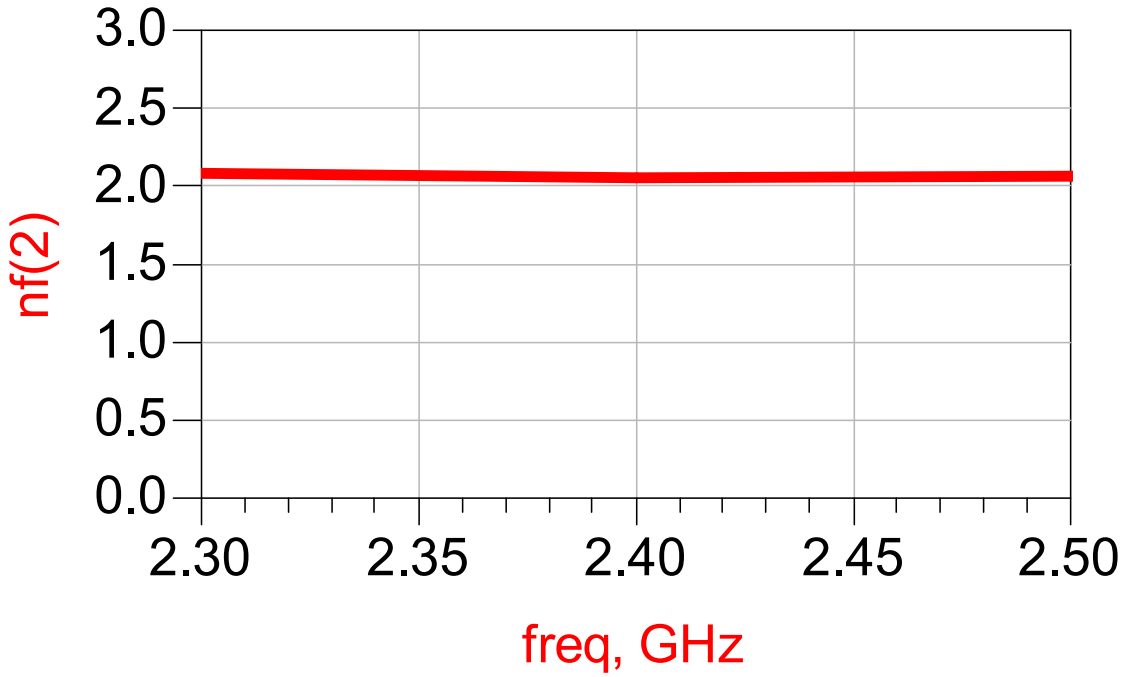



Figure 5b. Noise Figure (Narrowband) of Final Design

Figure 6 displays the simulated stability of the final design. Note that all μ (Mu) values are greater than 1 across the broad frequency range.

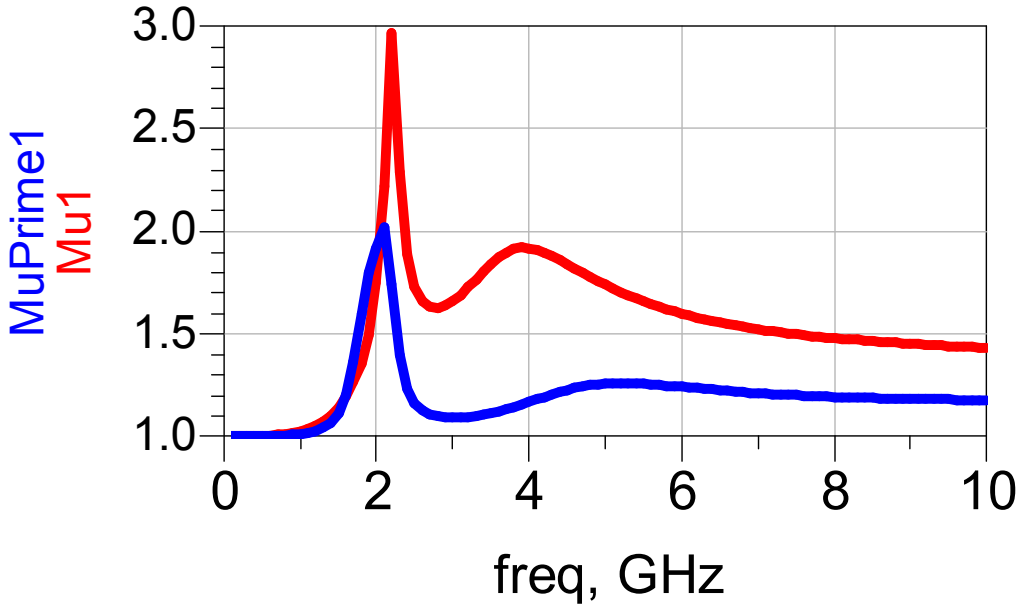



Figure 6. Stability of Final Design

Figure 7 illustrates the simulated third order intercepts (IP3) of the final design. The red curve is the first-order response while the blue curve is the third-order response. The theoretical intersection point of these two curves (displayed by the dashed lines stemming from the linear region of the amplifier) designates the IP3 point, which is approximately -12dBm relative to the input RF power.

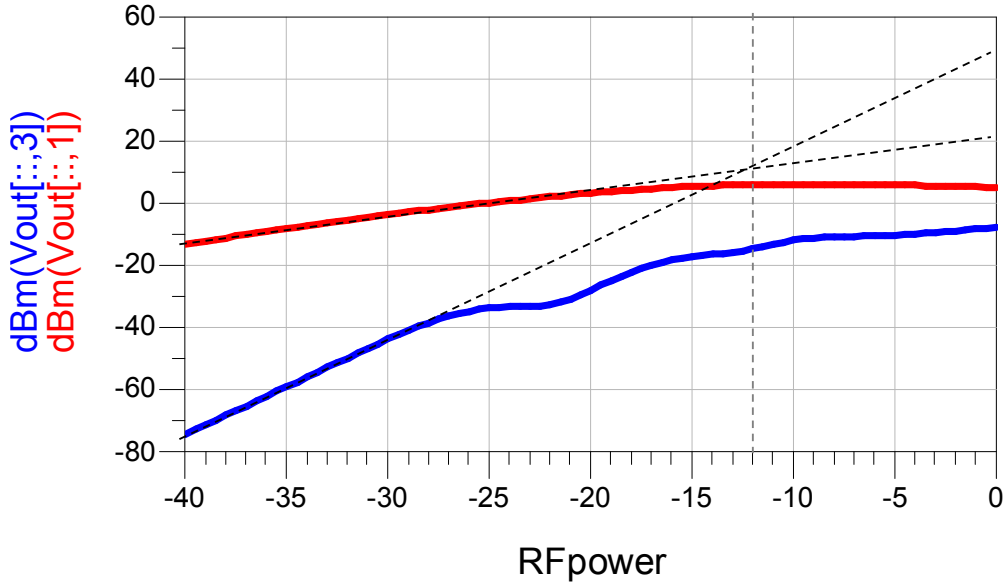



Figure 7. Third-Order Intercept of the Final Design

Several attempts were made before successfully placing all of the components in the layout. Precaution was taken to ensure there was enough space between inductors and other components so as not to introduce coupling into the system. Also, care was taken to place the ground vias as close as possible to the ground-signal-ground (GSG) pads. Lastly, it was important to ensure that the traces, as well as resistors, were large enough to handle the amount of current that the simulation predicted would run through them. Figure 8 illustrates the final design layout.

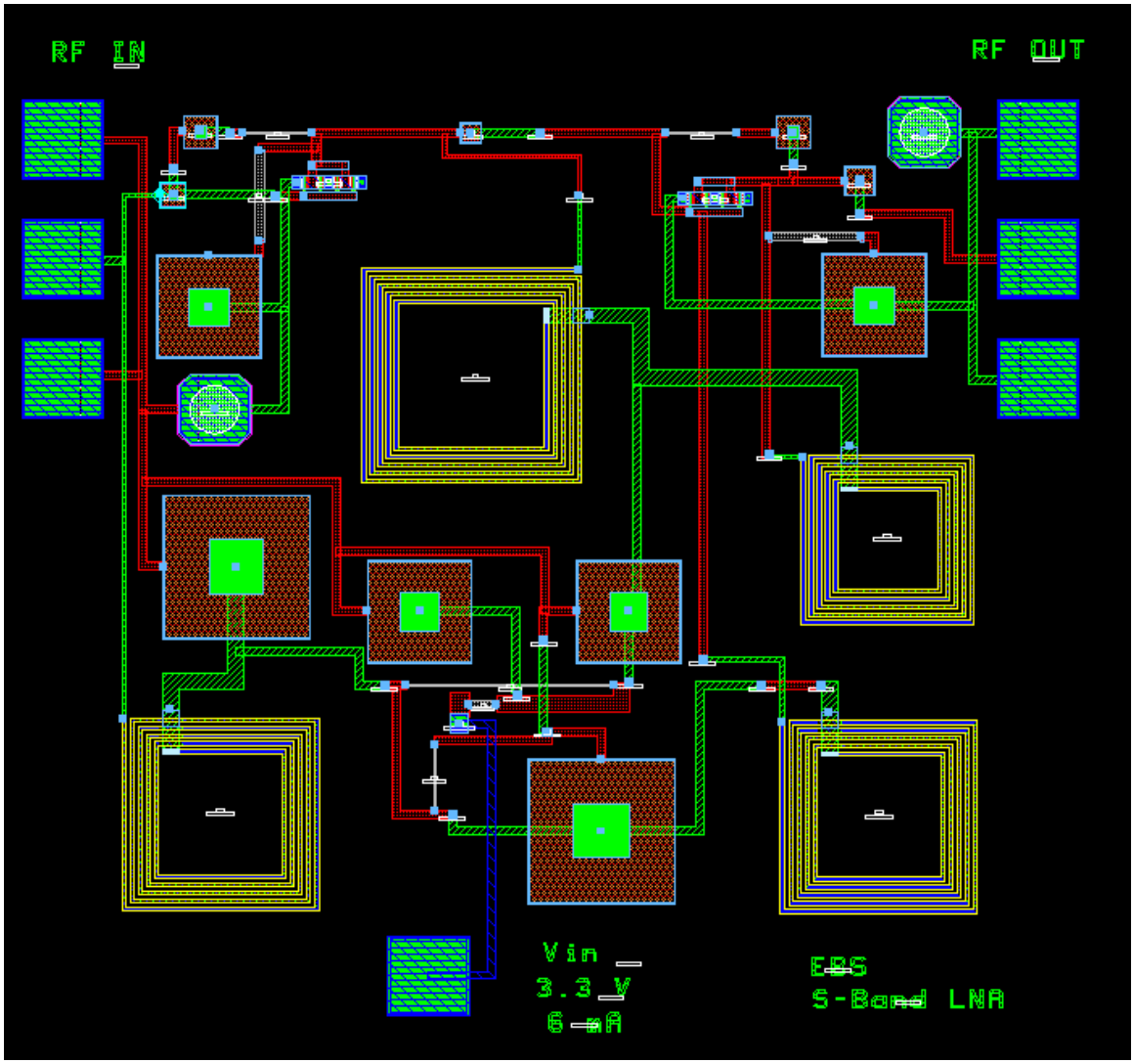



Figure 8. Final Design Layout

## 8. TEST PLAN

There are three measurements of interest for the LNA: (1) S-parameter measurements, (2) noise figure measurements, and (3) compression measurements.

First, power must be applied to the chip. To do this, apply a needle probe to the Vin pad on the chip. Slowly, increase the voltage to 3.3 V and verify that the power supply is drawing approximately 6.2 mA of current.

For the s-parameter measurements, first calibrate the network analyzer. Then, connect the GSG probes to the RF IN pad and the RF OUT pad on the chip. Finally measure the s-parameters on the network analyzer and save the data to a disk.

A similar setup is employed when taking the noise figure measurements. First calibrate the noise figure meter. Apply a noise source at the RF IN side of the chip. Take a measurement at the RF OUT side of the chip and save the data.

A signal generator in conjunction with a spectrum analyzer is used to make the compression measurements. Connect the signal generator to the RF IN side of the chip. Connect the spectrum analyzer to the RF OUT side of the chip. Set the signal generator to 2.4 GHz. Start at -40 dBm, and sweep the input power in 1dBm increments until compression is reached. Save the data to a disk.

## 9. SUMMARY

Overall, the designed LNA exhibits low noise figure, high gain, high reverse isolation, and low DC power consumption all encompassed in a compact layout. The gain ripple is slightly larger than the design goal, but still is comparable with COTS LNAs. In addition, the design goal for input VSWR was not achieved, but a tradeoff could be made to sacrifice some noise figure and/or gain to attain a better input match. The main focus of designing a compact, low power consumption device operable via a single battery cell was successfully accomplished. A comparison of measured results to the simulated performance will allow for validation of the models used in the design.

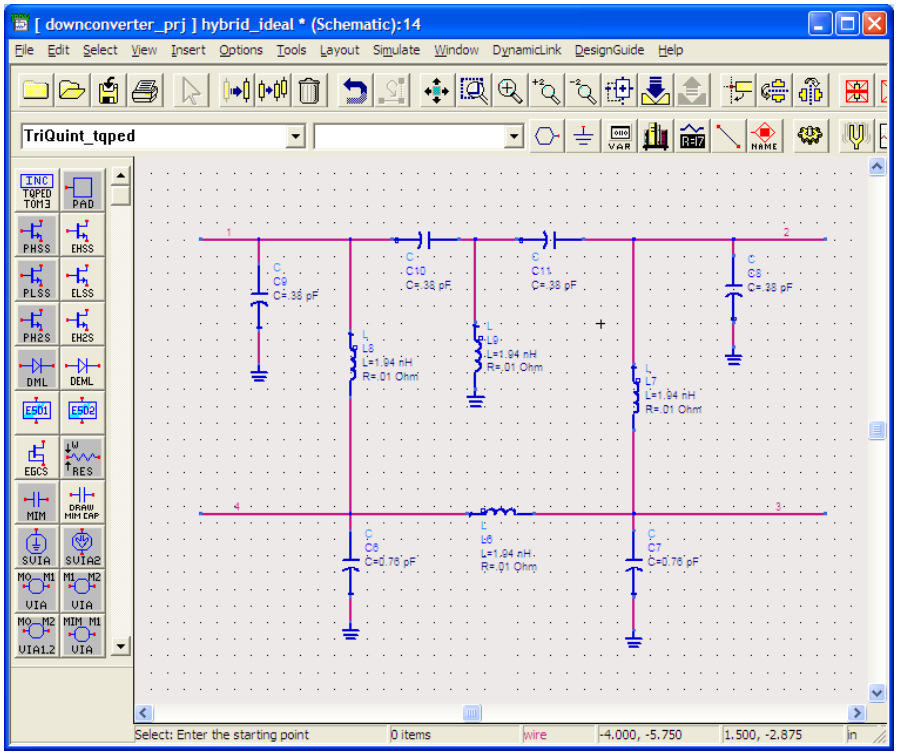
# 525.787
# MMIC Design
# C Band Mixer

Alexander Mendes
Dec.8th, 2007

Abstract:
The purpose of this design was to create a up/downconverting mixer that operates using a 2.8GHz LO. Various designs were considered, and a lumped element equivalent retrace mixer, using depletion-mode FETs as diodes was decided upon. Performance for 5.7GHz RF input, and 100 MHz IF input, are shown.

Discussion of Design.

The mixer used is based on a lumped-element implementation of a racrace mixer, a form of 180 degree hybrid coupler. This design was chosen because of it's relative ease to implement, and because these mixers usually have low conversion losses. The limitations of the TriQuint library was also a factor in this – most double-balanced or active mixers require balun transformers, which the TriQuint library does not provide. The figure below shows the ratrace hybrid using ideal lumped elements, tuned to 5.8GHz.




Port 2, in this model, will be the LO input, while port 4 will be the RF input/output. Because of it's relatively low frequencies, the IF Input/output can theoretically be at any point in the hybrid, however, it was found that port 1 offered slightly better performance. In order to improve isolation and conversion loss, simple highpass filters (3dB point 2.5GHz) were added to the LO and RF ports, and a lowpass filter (same 3dB point) to the IF port.

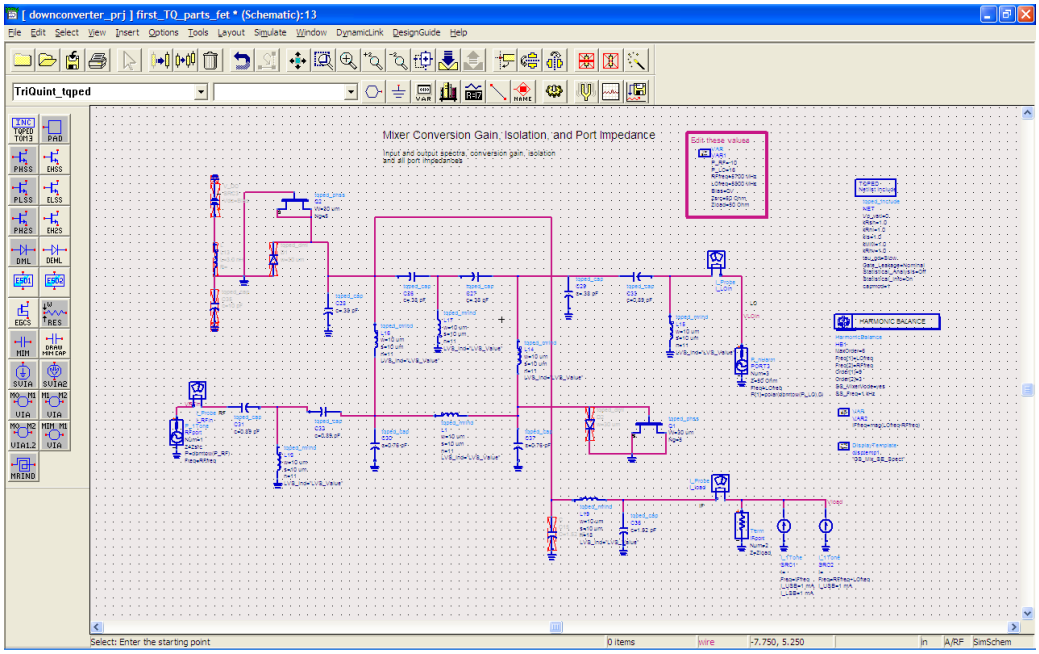
In order to complete the mixer, two nonlinear components must be added to the design – one to port 1 above, and one, in an opposite orientation, to port 3. The initial design used two overlap diodes, which are included in the TriQuint set. However, these devices require a very well controlled bias voltage – it was found that, depending on the diodes' physical characteristics, a 1.3-1.4 input was ideal, and deviations of as little a s0.1 volts had a large effect on conversion loss. An effective design, therefore, would require not only an additional input pad, but also a resistor network to minimize deviation. Furthermore, even when the diode widths were tuned, the maximum predicted conversion loss was 18 dB, which is far below the 6-9 dB goal for this design.

A second approach is to use two FETS, with source and drain tied together, to act as a type of diode. In this design, two depletion-mode FETs, each with gate width of 30 um and 5 fingers, are used. This was found to give optimal conversion loss. It was also found no input voltage was needed – the circuit gives best performance at 0 volt input. However, to compensate for this, a high LO drive is needed for the circuit to function – a table of downconversion performance vs. LO drive is given below.

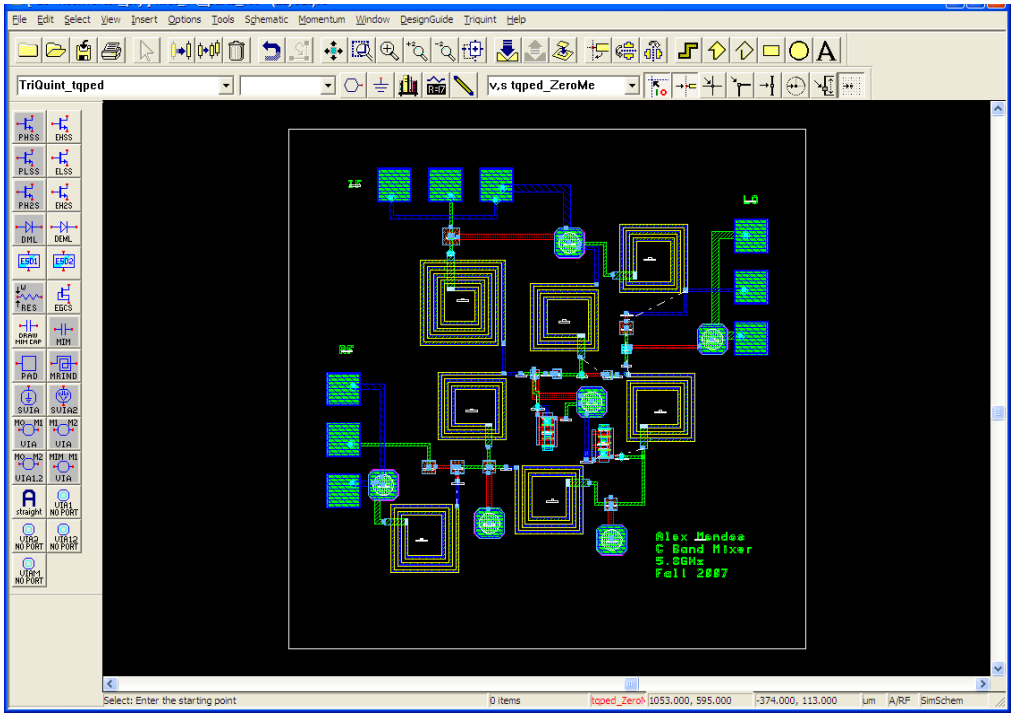
| **RF Power (dBm)** | **Downconversion Loss (dB)** |
|---|---|
| +10 | 17.4 |
| +11 | 10.4 |
| +12 | 7.1 |
| +13 | 6.1 |
| +14 | 5.8 |
| +15 | 5.6 |
| +16 | 5.5 |

Table of downconversion loss (5.8GHz LO, 5,7GHz -10dBm RF)

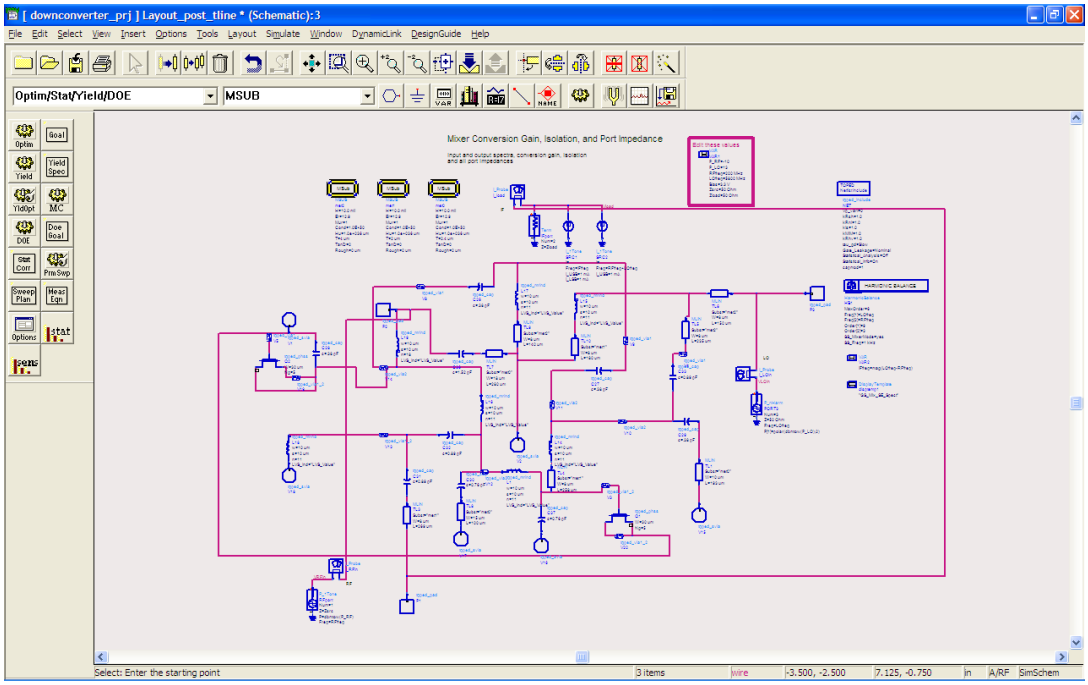
From this, it appears that a +13dBm drive LO is needed for best performance, while roughly +11dBm of LO power is needed to meet the design goals.



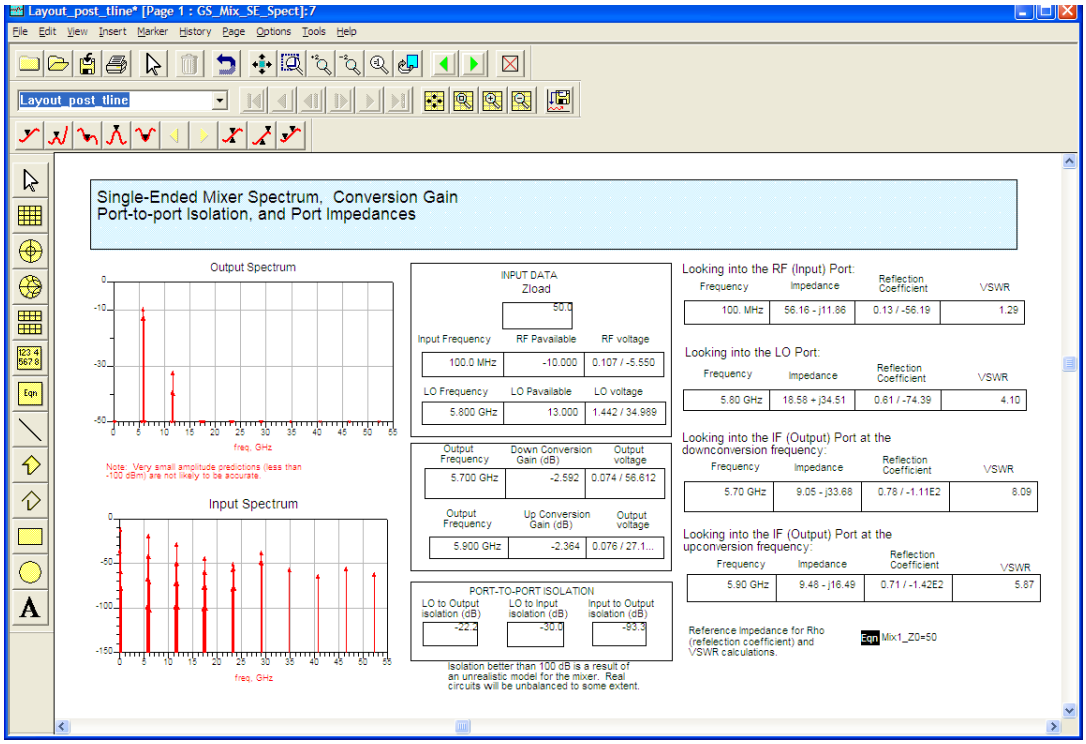

An ideal schematic of the ratrace mixer. This layout includes filtering on each input and output, as discussed above.



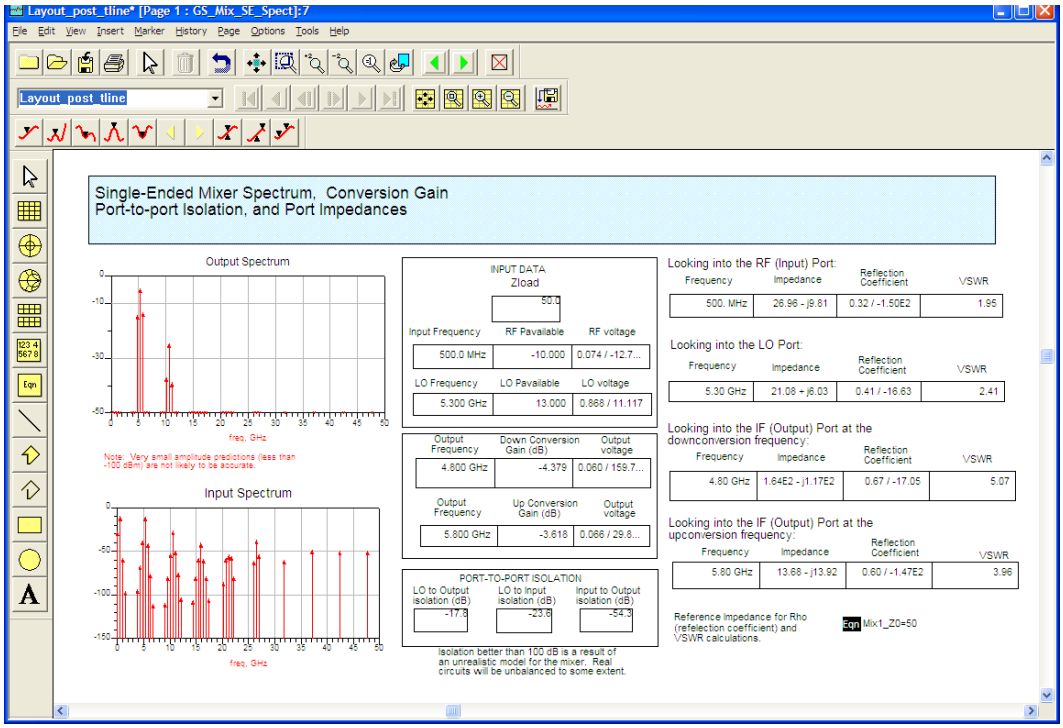

Layout of the mixer. While most components are connected using short traces, note that The RF input, as well as a few traces to ground vias show long traces. These are included in simulation results, however, these lengths were found to have little effect on the design performance



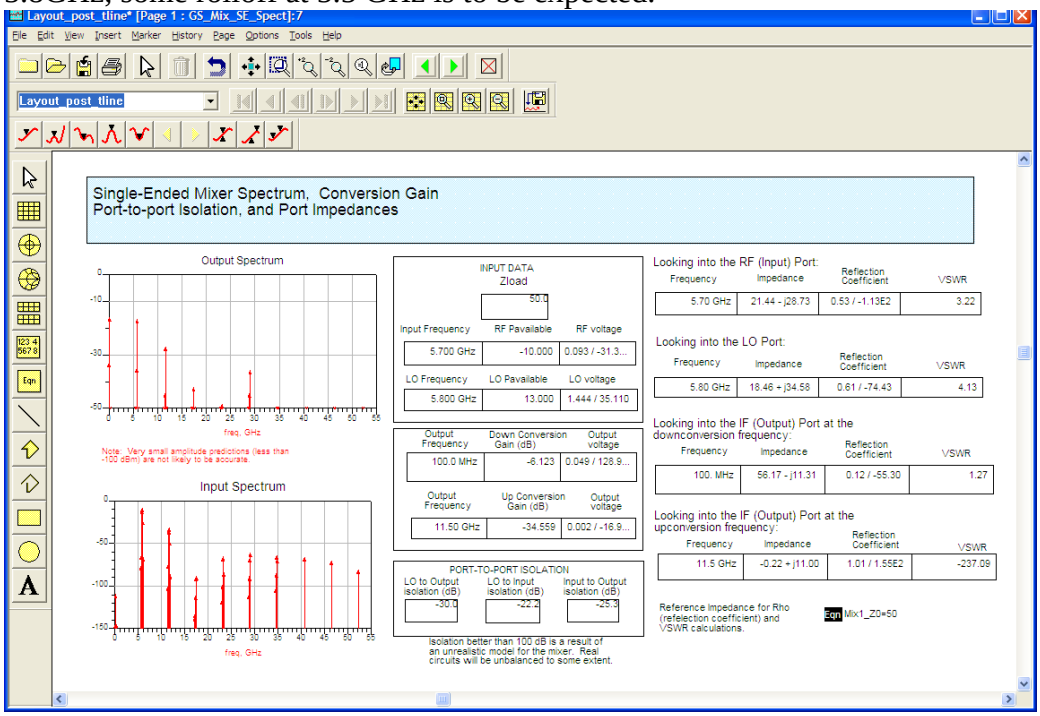

Schematic used for final simulation. Longer traces were added into the schematic, but short traces are ignored. Unlike the previous picture, this shows the schematic configured for upconversion simulation.




Upconversion results. IF = 100MHz, -10dBm, LO = 5.7GHz, 13dBm. The conversion loss here is better than expected at -2.6dB, however, the relatively high LO leakage may make this design impractical.




Upconversion, IF = 300MHz, LO = 5.5GHz. Note that the conversion loss is now 4.4dB. Because the filters added to the various inputs should not have an effect, this must be due to the nature of the circuit itself. Since the Ratrace was optimized for 5.8GHz, some rolloff at 5.5 GHz is to be expected.




Downconversion, 5.7GHz RF, 5.8GHz LO. Despite including basic filters, the LO and RF frequencies are still present on the IF output – however, as these are far from the IF frequency, they can be easily filtered out externally.

Test plans:

Test Equipment:

2 Frequency Generators, 0.1-6 GHz minimum.
1 Spectrum Analyzer, 0.1-6 GHz minimum frequency
3 test probes

Test 1: Downconversion

Equipment setup:
Calibrate all necessary equipment, measure and record cable losses, etc.
Set LO Generator to 5.8 GHz, +13 dBm (or maximum) output power
Set RF Generator to 5.7 GHz, -10 dBm output power
Turn off generator power outputs and connect all devices to the correct inputs
Turn on LO, followed by RF.

Measurements

RF Frequency sweep:
Vary RF input from 5.7 GHz to 6.2 GHz, record IF power and frequency.

RF Power Sweep

Set RF input to 5.7 GHZ
Vary RF Power from -10 to +10 dBm. Record output power and conversion loss

LO Power Sweep

Set RF Power to -10dBm, 5.7GHz
Vary LO input power and record output power and conversion loss

Test 2: Upconversion

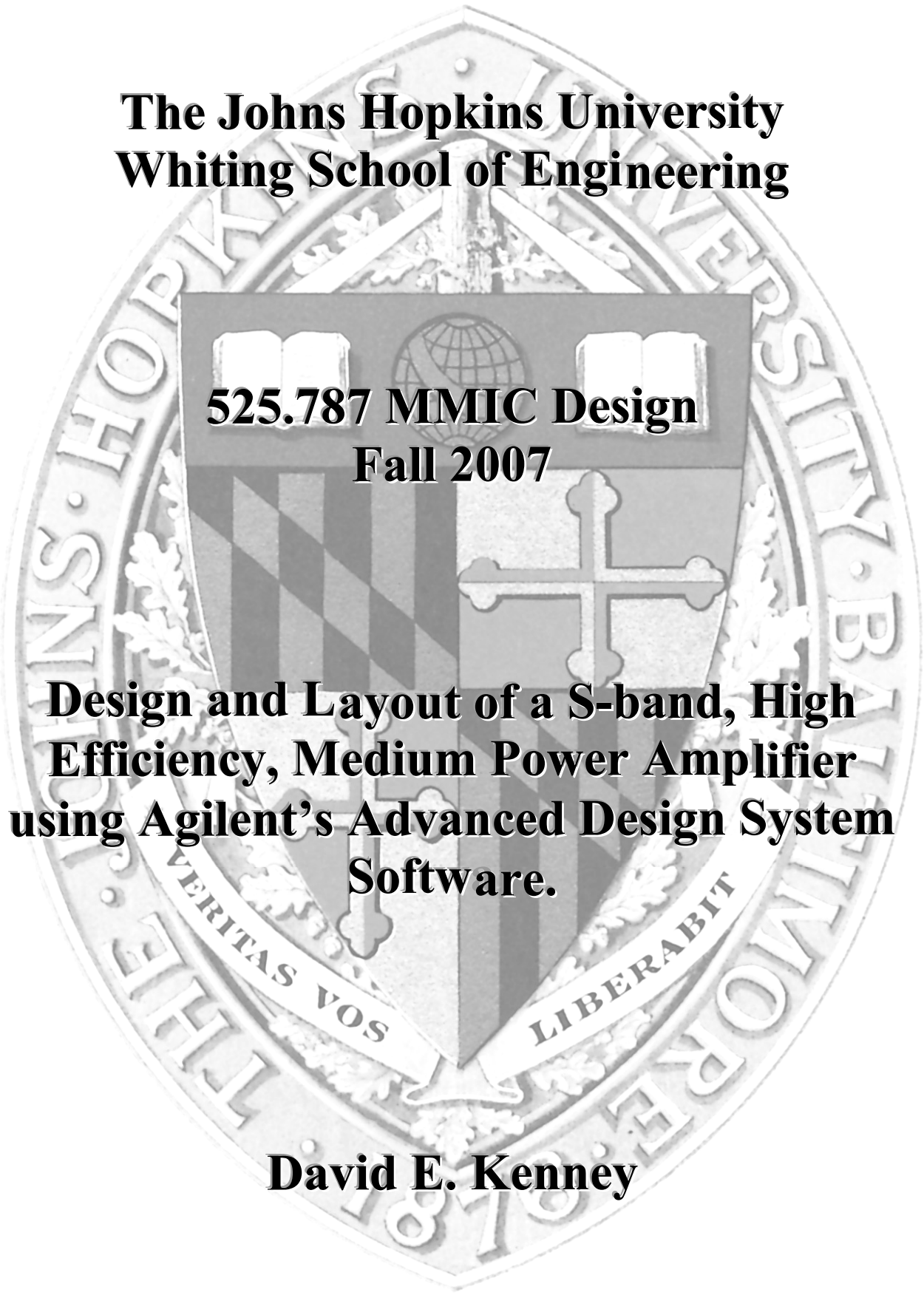
Measurements
RF Frequency sweep:
Vary RF input from 0.1GHz to 0.5 GHz, record IF power and frequency.

RF Power Sweep

Set RF input to 0.3 GHZ
Vary RF Power from -10 to +10 dBm. Record output power and conversion loss

LO Power Sweep

Set RF Power to -10dBm, 5.7GHz
Vary LO input power and record output power and conversion loss



# The Johns Hopkins University
# Whiting School of Engineering

## 525.787 MMIC Design
## Fall 2007

# Design and Layout of a S-band, High Efficiency, Medium Power Amplifier using Agilent's Advanced Design System Software.

**David E. Kenney**

# Table of Contents



## Figures and Tables

## 1. Abstract

This paper describes the design, simulation and layout of a two-stage GaAs MMIC power amplifier operating at S-band frequency from 2.3 to 2.5 GHz. The power amplifier was designed using Agilent's Advanced Design System Software which included the TriQuint elements library. The critical design parameter for this High Efficiency Power Amplifier design is Power Added Efficiency (PAE). Simulations show that my design should achieve a PAE greater than 22% over a 100 MHz bandwidth centered at 2.4 GHz.

## 2. Introduction

Modern RF and microwave transmitter designs utilize integrated circuit power amplifiers that directly interface with the radiating element in order to maximize RF power output and efficiency. The primary goal for this design is to get the most RF output power for a given DC power consumption in order to extend battery life. My design will utilize a single supply voltage in the range of 3.0 to 3.6 VDC so that a small battery will be able to power the device. Additionally, I chose to build a two stage design that uses two 60 μm (4x15) Emode PHEMTs. The Emode FET was selected over the Dmode FET due to it's higher gain for a given DC power consumption.

My S-band Power Amplifier design is based on the following criteria:

| | |
|---|---|
| FREQUENCY: | 2305 to 2497 MHz |
| BANDWIDTH: | > 193 MHz |
| GAIN, small signal: | > 24 dB with a goal of 26 dB |
| GAIN RIPPLE: | $\pm$ 1 dB |
| OUTPUT POWER: | TBD @ 20-25% PAE |
| SUPPLY VOLTAGE: | + 3.3 Volts only, goal (3 to 3.6V range) |
| VSWR, 50 Ohm: | < 1.5:1 input & output |
| SIZE: | Layout must fit on a 60 x 60 mil ANACHIP |

## 3. Design Approach

My design strategy will be to use two stages in order to get sufficient gain and power output over the 200 MHz bandwidth. I found during some initial simulations that a single amplifier would not allow me to meet the gain ripple requirements and hence a two stage design is required. One of the goals for this design is to minimize power consumption to less than 40 mW. Also, keep in mind that the two stages will be self biased through a voltage divider network so there will be additional power consumed by biasing resistors. So, the first step will be to design the output stage using the Cripps method to determine the output

network with a bias goal of $I_{max}/2 \approx 15$ mA. The next step will be to design the driver amplifier stage biased to approximately 15 to 20% of $I_{dss}$. Finally I will combine the two stages using a matching network and simplify the inter-stage topology while tuning the remaining elements to obtain the specifications listed in the introduction.

## 3.1. Power Amp

### 3.1.1. Determine Initial Bias Point, PAE, and RCripps

Setting Vds to 3.5 VDC we see in Figure 3.1.1 that Vgs is equal to 0.679 VDC which is a reasonable bias point for an Emode FET. This bias value will allow for a simple design of the associated resistor bias network.

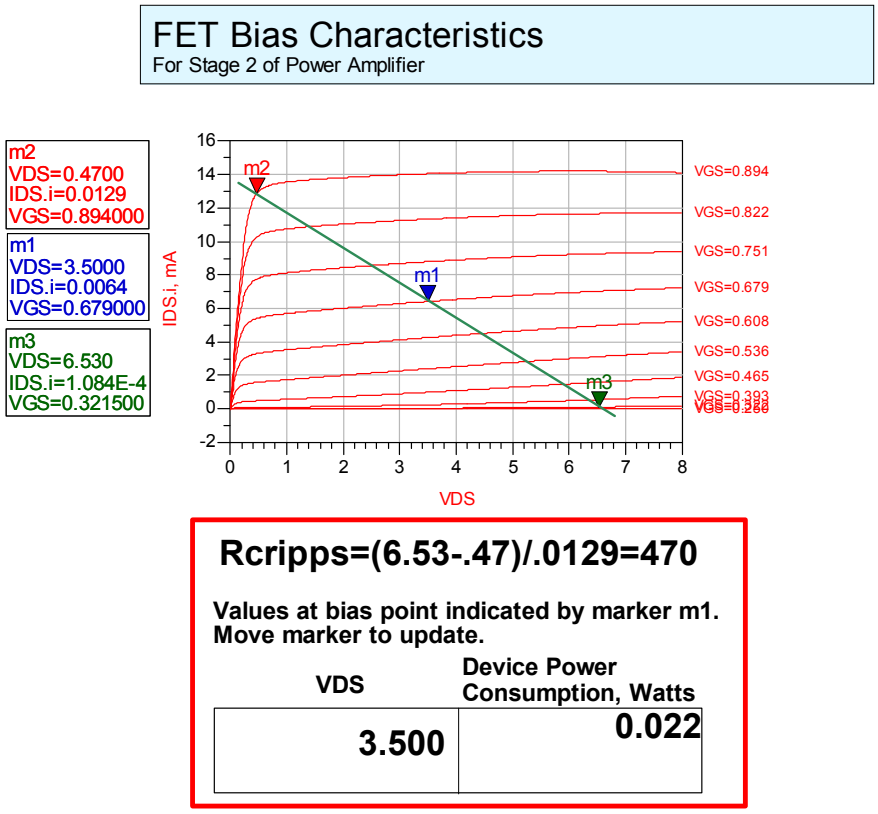



**Figure 3.1.1, Emode FET Bias Characteristics for a 60 µm (4x15) TriQuint FET**

Using the load line in Figure 3.1.1 I determine that ΔVDS is equal to 2x(3.5 – 0.47)V = 6.06 V and that Δ IDS is about 12.9 mA. Therefore, RF output power should be approximately equal to (ΔVDS x Δ IDS)/8 ≈ 9.8 mW. With the device power consumption at 22 mW my Power Added Efficiency (PAE) should be approximately 44 %. However, I expect the actual PAE to be lower due to the additional power that will be consumed by biasing resistors. My Rcripps value can be calculated with the formula ΔVDS / Δ IDS which equals 470 Ω.

### 3.1.2. Add Bias Circuitry and Stabilize

My main goal for the design of my bias circuit is to achieve a single DC feed for the Gate and Drain of my Emode FET's. I discover during simulations that the stability of the circuit is greatly affected by the value of the bias resistors. The higher the resistance the more unstable the circuit becomes. I utilized a series resistor "R5" to stabilize my circuit with higher value bias resistors. Higher value bias resistors are preferred in order to lower the power consumed by the bias circuit and improve the gain. My stabilized bias circuit is illustrated in Figure 3.1.2 below.

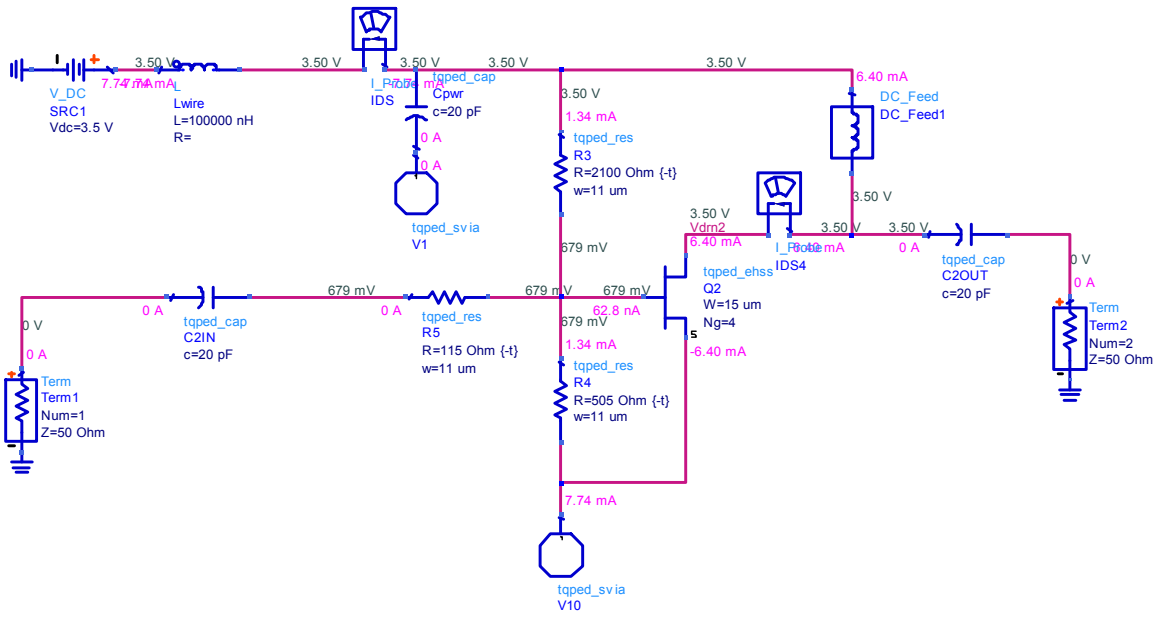



**Figure 3.1.2, Power Amp output stage with bias and stability circuit.**

### 3.1.3. Matching Network

Now using the "Cripps Method" I design the output matching circuit. The impedance looking into the output (S22) of the amplifier is equivalent to a 59.6 fF shunt capacitor in parallel with a 1457 Ω shunt resistor (Rds), which gives a S22 value of 536.7 - *j*703.4 Ω. I want to resonate out the reactance and replace Rds with the resistance of Rcripps = 470 Ω. This results in a S22 value of 398.8 - *j*168.5 Ω. Now I take the conjugate value of S22 and use the Smith chart to determine the circuit element values that correspond to the path going from 398.8 + *j*168.5 Ω to 50 Ω. This results in a 9.4 nH shunt inductor followed by a 0.46 pF series capacitor which provide a match to 50 Ω for the Cripps output matching circuit. I place the components in the ADS schematic and then determine the value of S11. To do this I take the conjugate value of S11 (200.5 + *j*185.9 Ω) and design an input matching circuit to map S11 to 50 Ω. Doing this yields a 7.31 nH shunt inductor followed by a 0.524 pF series capacitor. Figure 3.1.3a illustrates the schematic for an ideal output stage of my power amplifier design.

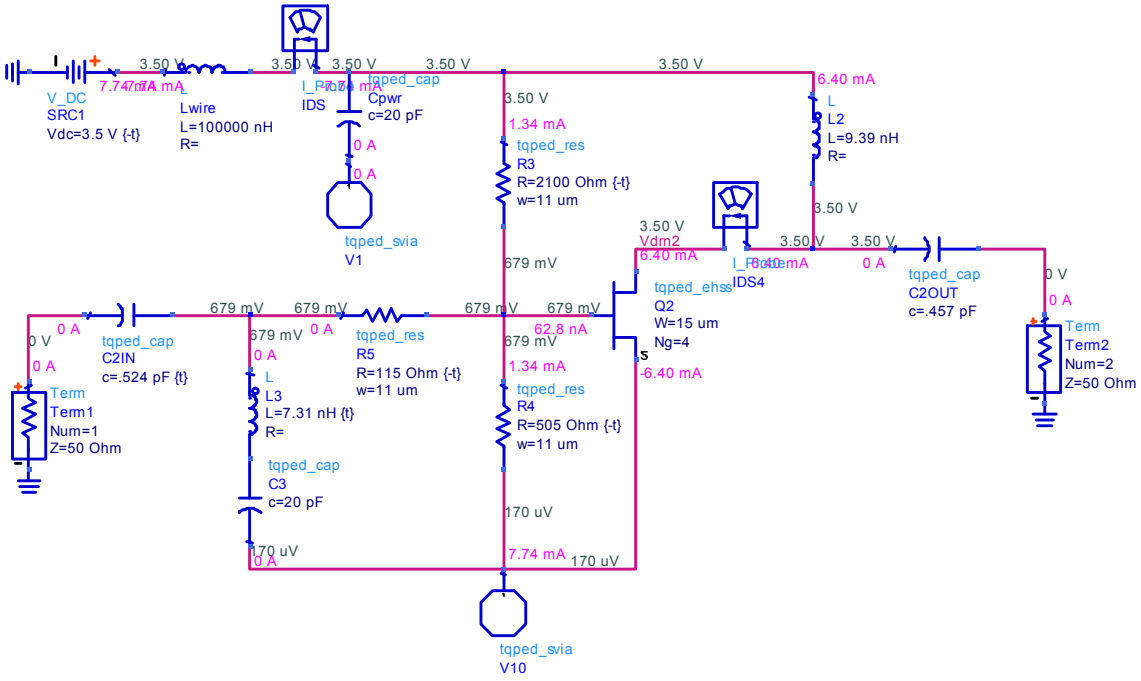



**Figure 3.1.3a, Power Amp ideal output stage with matching circuit using $R_{Cripps}$ method**

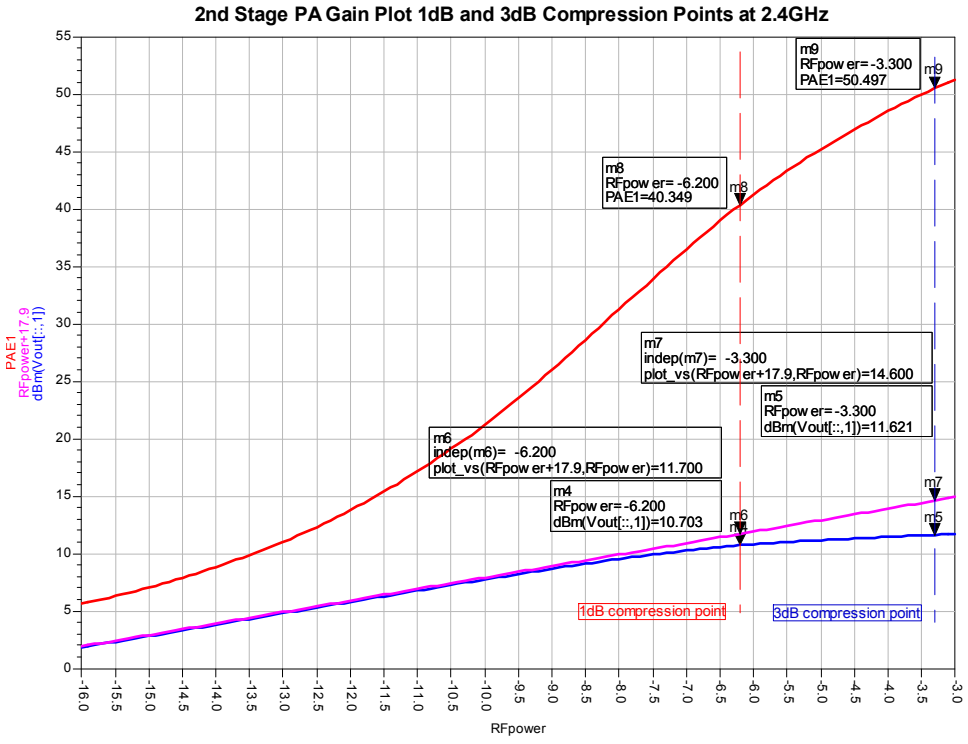



**Figure 3.1.3b, Gain, Power Out, and PAE for the ideal Power Amp output stage.**

Note from Figure 3.1.3b it can be seen that 1 dB of compression occurs at approximately -6.4 dBm of RF power in. This is a key piece of information required for the design of the Driver Amplifier stage. The driver amplifier will be designed to be linear past -6 dBm RF Power in to prevent compression before the output stage of the power amp.

## 3.2. Driver Amp

### 3.2.1. Determine Bias Point

For the driver amp design it is important to achieve gain with minimal DC power. This may be accomplished with the load line shown in Figure 3.2.1a below. The bias point is based on taking approximately 20% of IDSS of the output stage, refer to Figure 3.1.1.

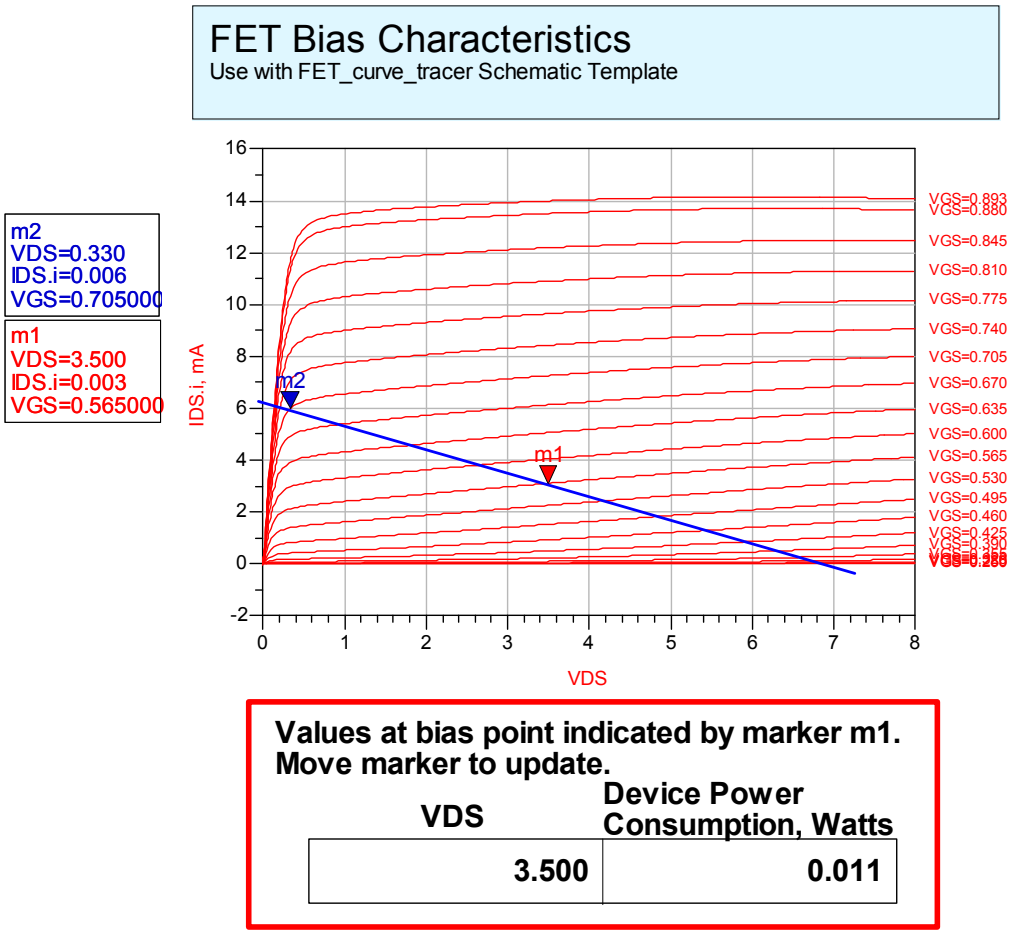



**Figure 3.2.1a, Emode FET Bias Characteristics for a 60 µm (4x15) TriQuint FET**

Using the load line in figure 3.2.1a I determine the RF output power for my driver stage should be approximately (ΔVDS x Δ IDS)/8 ≈ (2(3.5-.33)VDC x 6mA)/8 ≈ 4.8 mW. With the device power consumption at 11 mW my Power Added Efficiency (PAE) should be

approximately 43 %. However, I expect the actual PAE to be lower due to the additional power that will be consumed by biasing resistors. Now I generate my circuit using the same steps and criteria used in section 3.1.2 through 3.1.3 to come up with my circuit shown in figure 3.2.1b below.

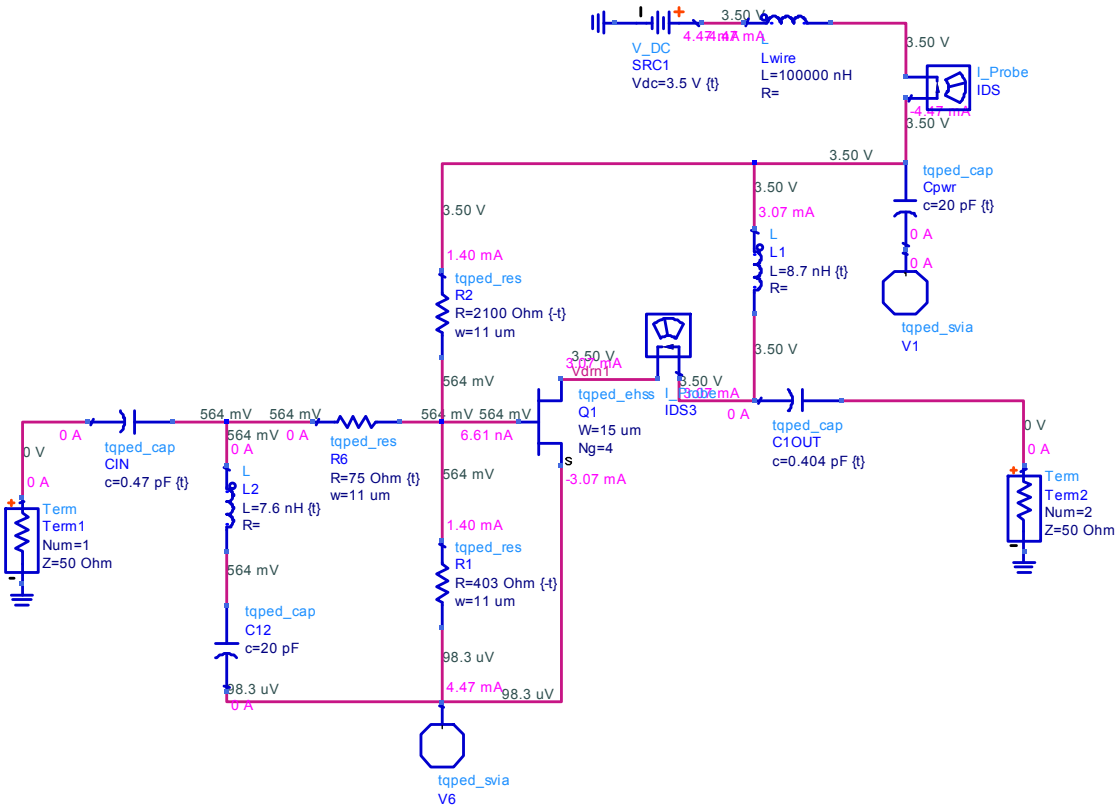



**Figure 3.2.1b, Power Amp ideal driver amp stage with matching circuits.**

### 3.2.2. Matching interface network

Now that I have my driver amp stage I need to match the output of the driver amp to the input of the power amp output stage. I use the smith chart to determine the component values of my intermediate matching circuit and connect the two circuits and tune. Figure 3.2.3 shows the entire two stage high efficiency power amp circuit. Note that I tune the two stages to obtain a flat gain response across the entire bandwidth as illustrated in Figure 3.2.4. Also, I met the specification for VSWR across the entire bandwidth for the input but I was only able to achieve the output VSWR specification for about 140 MHz of bandwidth. This would be one of the areas of concentration for future improvements of my circuit.

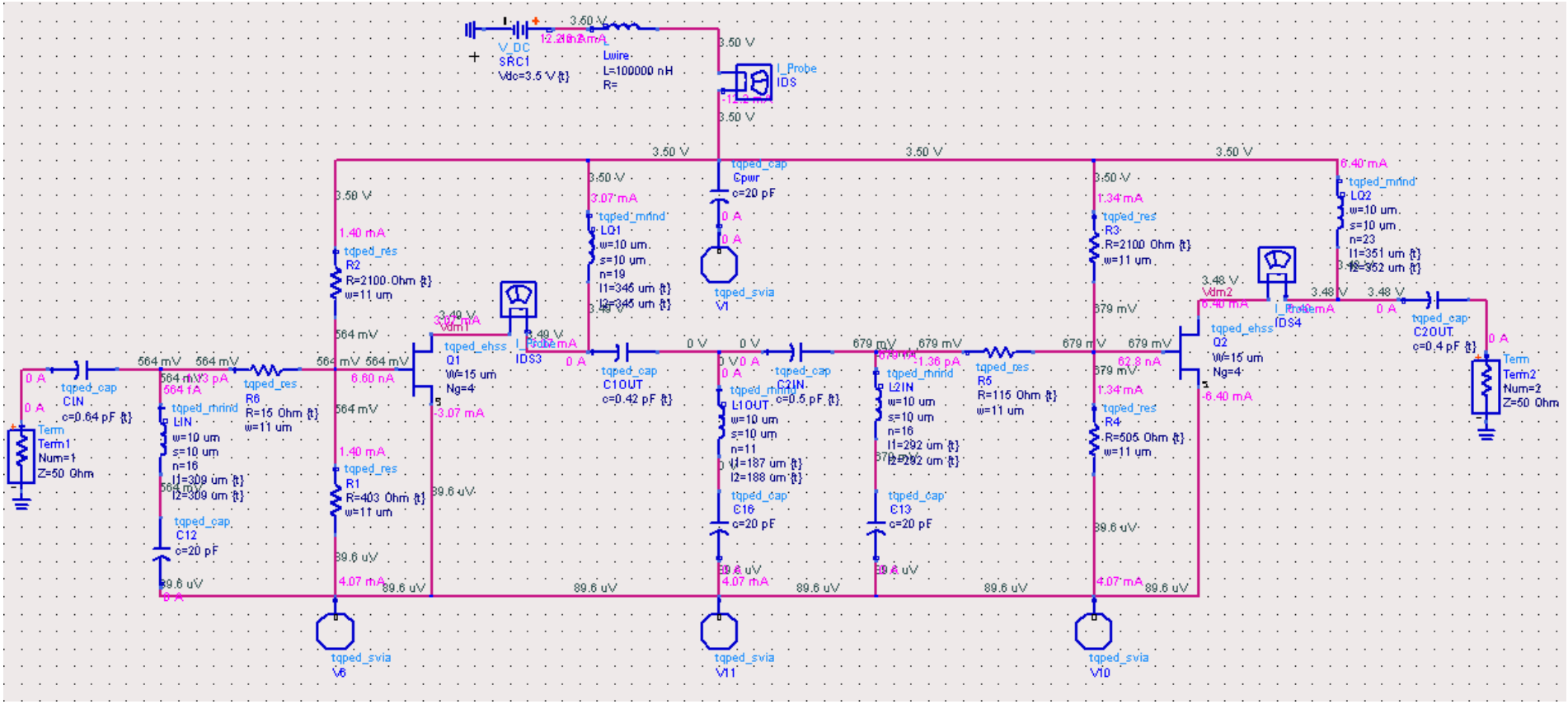



**Figure 3.2.3, Two Stage, High Efficiency, Medium Power Amplifier with single DC power feed.**

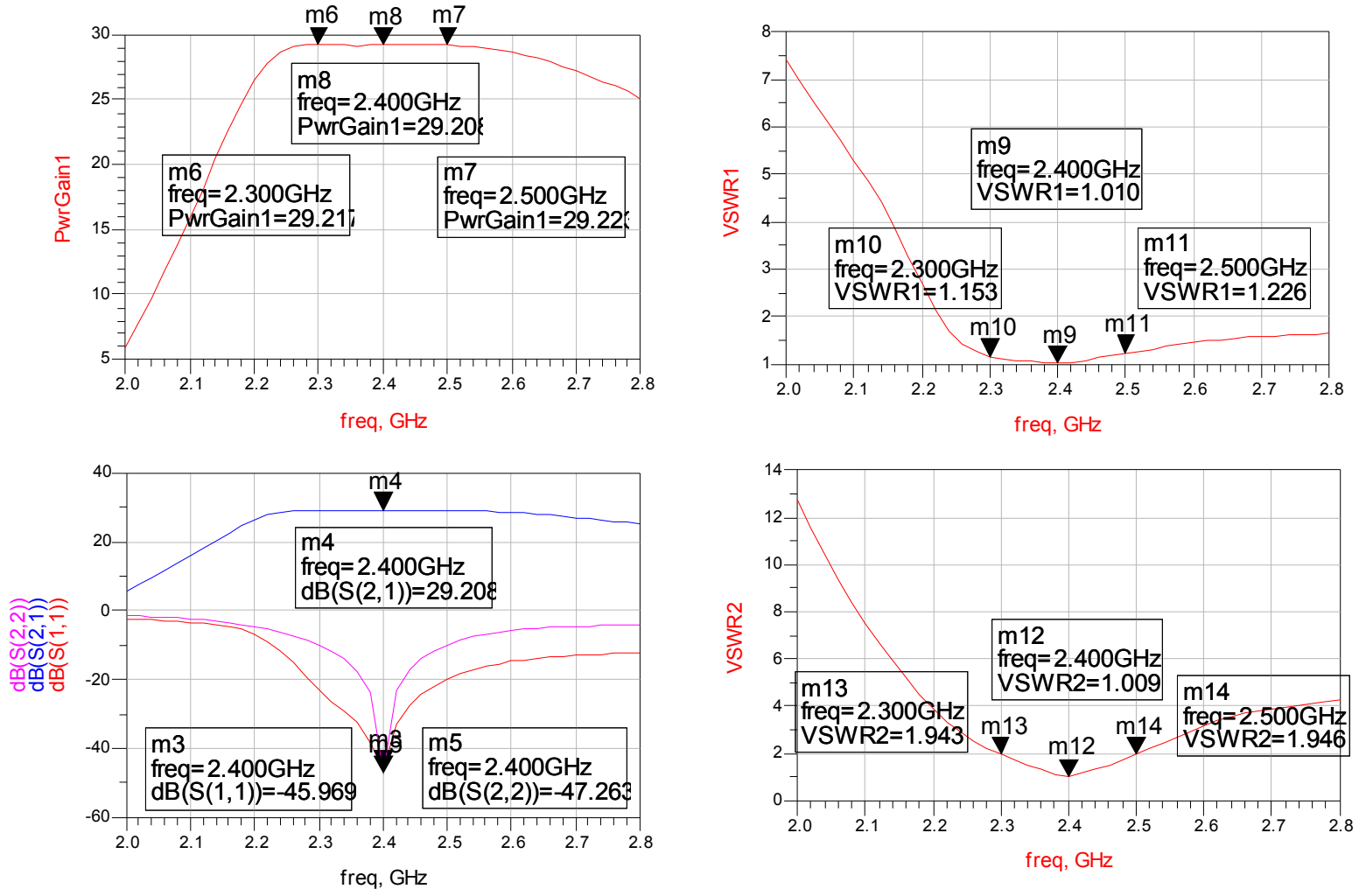



**Figure 3.2.4, Linear Simulation results from my High Efficiency, Medium Power Amplifier.**

### 3.3 Specification versus goals

Table 3.3.1 summarizes the design specification and the simulated results of both the simplified schematic and final layout schematic.

| | Specification Goal | Simplified Schematic | Final Layout |
|---|---|---|---|
| **Bandwidth** | **> 193 MHz** | **200 MHz** | **200 MHz** |
| **Gain** | **26 dB** | **29 dB** | **28 dB** |
| **Gain Ripple** | **± 1 dB** | **± 0.02 dB** | **± 0.2 dB** |
| **Output Power** | **TBD** | **10.1 dB** | **10.2 dB** |
| **Power Added Efficiency** | **20-25%** | **24%** | **23.3%** |
| **VSWR** | **< 1.5:1 input & output** | **1.01:1 input 1.01:1 output** | **1.01:1 input 1.01:1 output** |
| **DC Supply Voltage** | **3.0 – 3.6 VDC** | **3.5 VDC** | **3.5 VDC** |

**Table 3.3.1, Specification Compliance Matrix for a Two Stage, S-band Power Amp.**

### 3.4 Tradeoffs

The only major tradeoff I recognized in designing this circuit was Gain versus Stability. As I mentioned earlier there was a clear tradeoff when determining the size of the biasing resistors and the amount of power consumed by the bias circuit. Larger value biasing resistors meant lower power consumption by the bias circuit and higher power added efficiency. However, the tradeoff came in the form of instability to the circuit and therefore the need for larger series stabilizing resistors resulting in higher noise. However, noise was not a factor of consideration in the design of this circuit. Ultimately, an iterative process was used to determine the size of the biasing resistors and series stabilizing resistors.

## 4 Additional Simulations

Figure 4.1 illustrates the results of a nonlinear simulation detailing the dynamic load line response for my 1st and 2nd stages of the Power Amplifier. Figure 4.2 further illustrates the nonlinear simulation results showing Power Added Efficiency, Power Output, and Gain of my final circuit layout. Figure 4.3 and 4.4 show the linear simulation results of my final circuit.

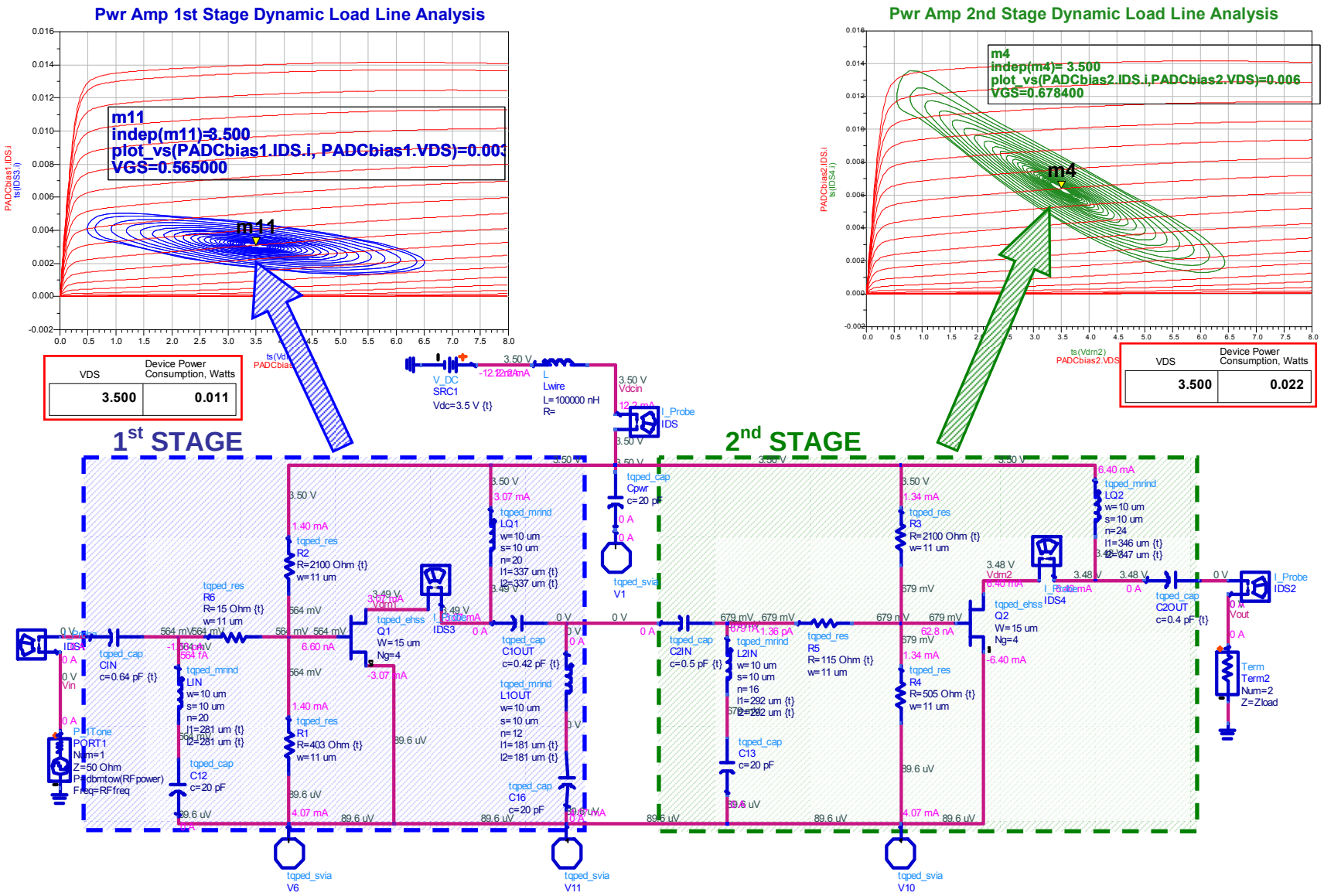



**Figure 4.1, Non-Linear simulation of my 2 stage High Efficiency, Medium Power Amplifier.**

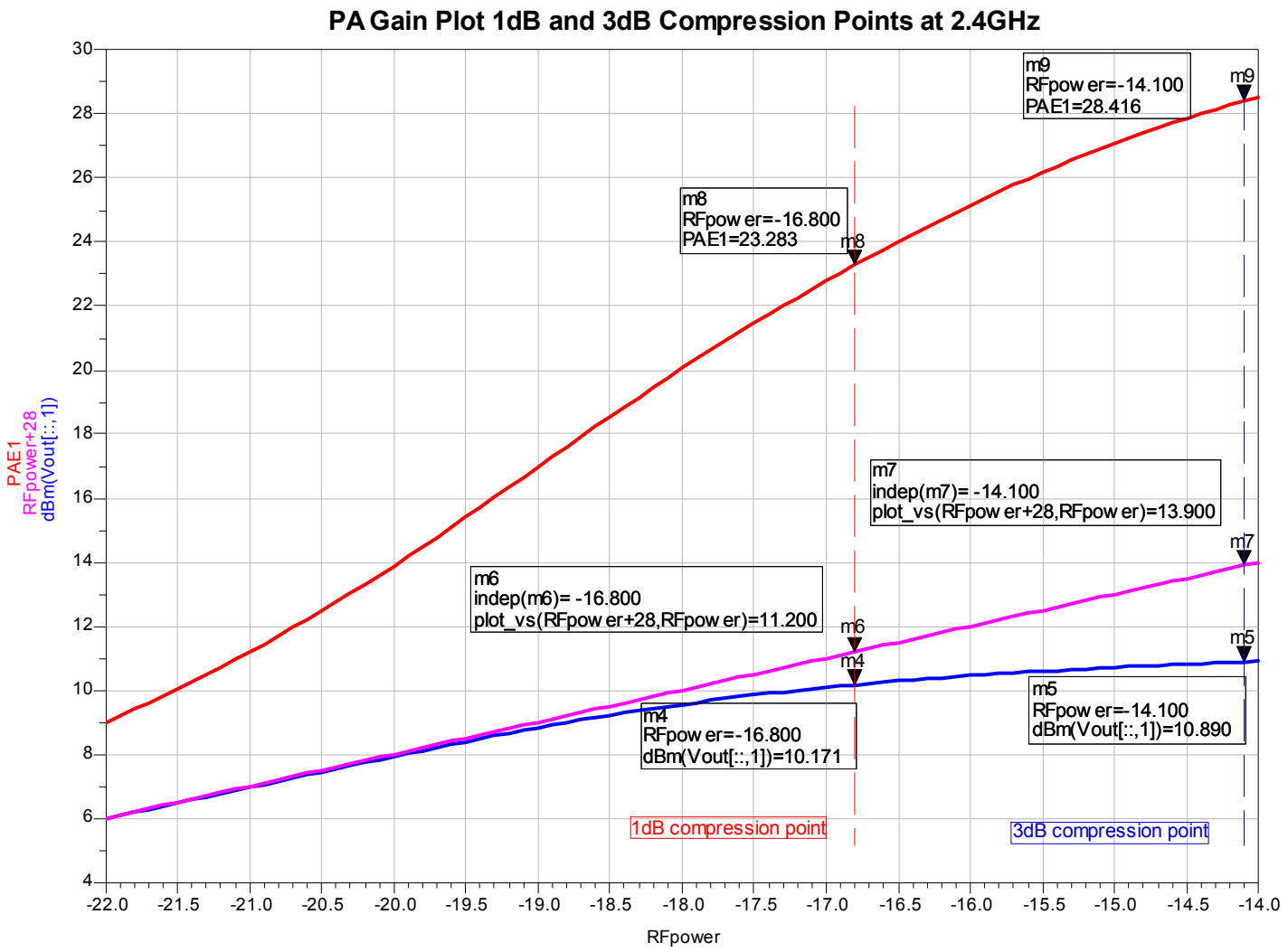



**Figure 4.2, Non-Linear simulation showing PAE, Gain, and Power Output at 1dB and 3dB compression points.**

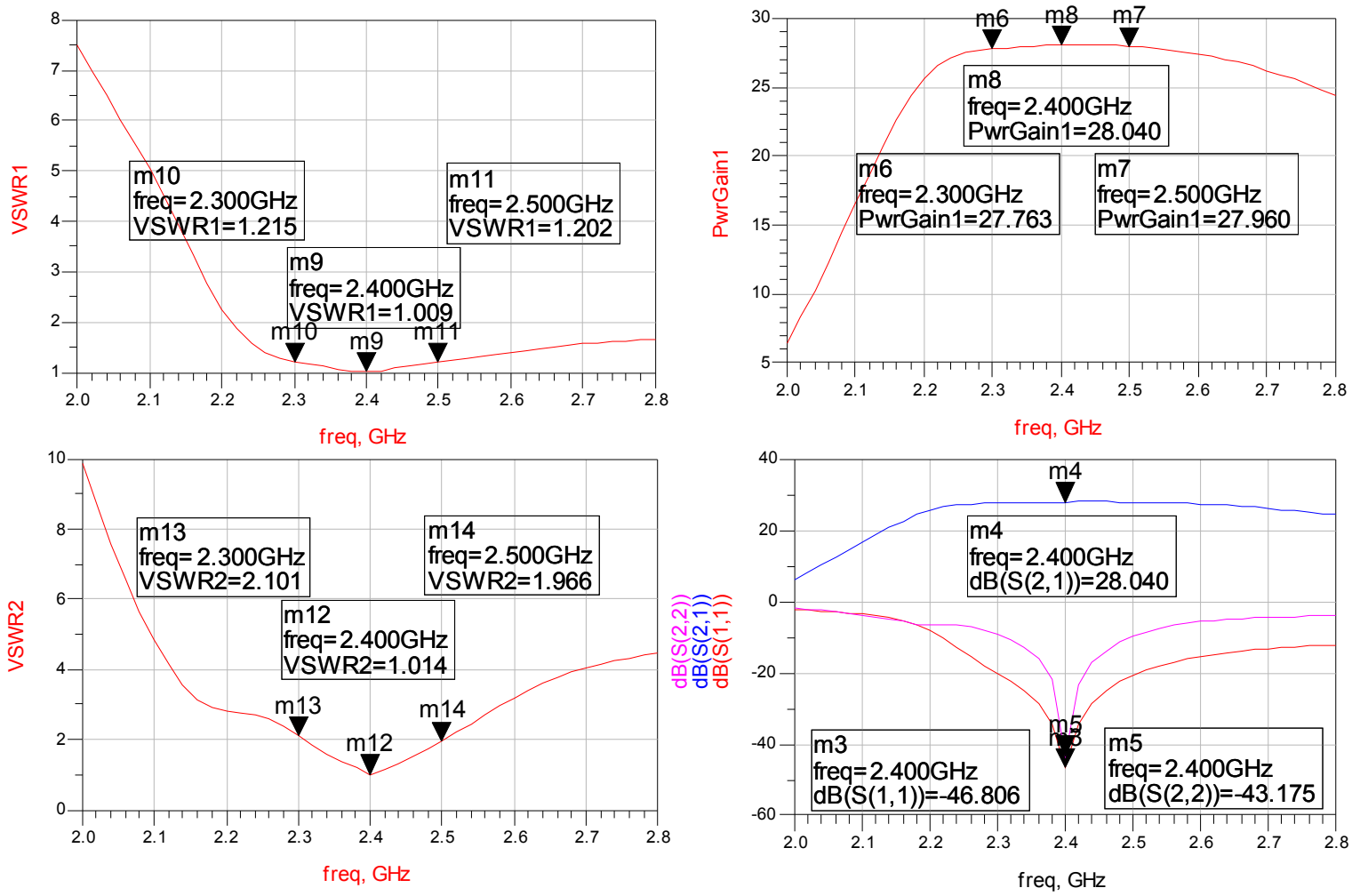



**Figure 4.3, Linear Simulation showing Gain, Gain ripple, and VSWR (Final Circuit).**

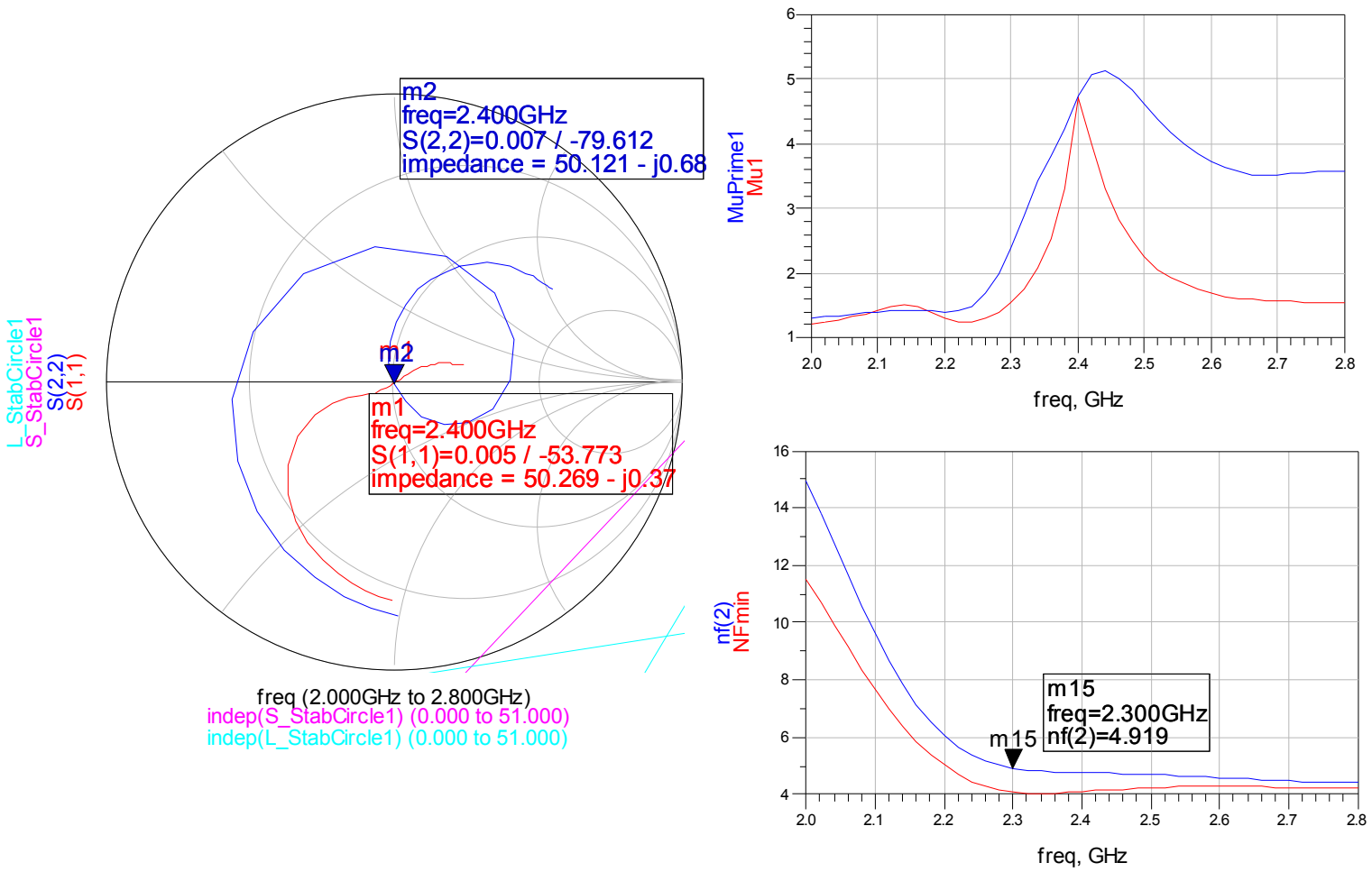



**Figure 4.4, Linear Simulation showing Stability and Noise (Final Circuit).**

## 5. Layout

The final circuit layout is illustrated in Figure 5 below.

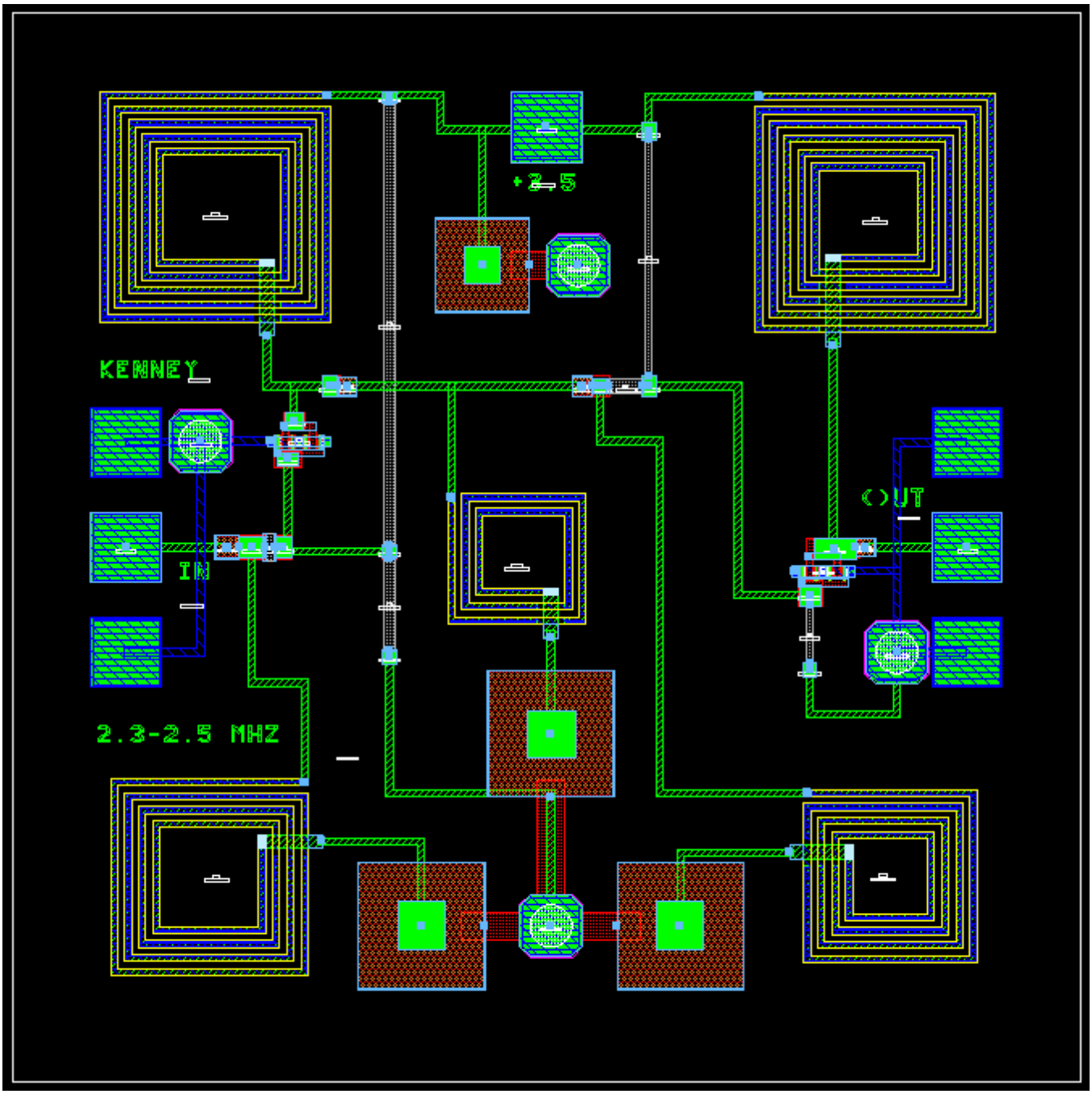



**Figure 5, S-band, High Efficiency, Medium Power Amplifier Layout generated in ADS.**

## 6. Test Plans

The following test procedures are recommended to test the 2 stage S band power amplifier.

### 6.1 Linear Parameters

Use an Agilent network analyzer to obtain the s parameters of the amplifier.

1. Calibrate the analyzer from 1GHz to 10GHz.
2. Place the DC bias power probe on the pad of the chip labeled "+3.5V".
3. Place probe tips on the designated pads. The input port is labeled "IN" and the output port is labeled "OUT".
4. Turn on the power supply and slowly adjust to +3.5V.
5. Record data.

### 6.2 Power measurements

For power measurements it is recommended that a signal generator and spectrum analyzer be used.

1. Connect the signal generator probe to the input pad of the amplifier chip, which is the port marked "IN".
2. Connect the spectrum analyzer probe to the output pad of the amplifier chip, which is the port marked "OUT".
3. Place the bias probe on the pad of the chip labeled "+3.5V".
4. Turn on the power supply and slowly adjust to +3.5V.
5. For Pin vs. Pout set the generator to the frequency of interest and sweep the power up to, but not exceeding, 0 dBm and recording measurements from spectrum analyzer after each interval.
6. For Pout vs. Frequency set the Generator to -16.8 dBm. Sweep the frequency and record measurements from the spectrum analyzer after each interval.

## 7. Conclusion & Recommendations

The S band 2 stage, high efficiency medium power amplifier design was a success and met and exceeded all of the specification goals in it's simulations. Future recommendations on this design would include improving the output match to achieve < 1.5 to 1 VSWR over the entire bandwidth. Table 7 illustrates the achieved results from the simulations performed using ADS.

| | Specification Goal | Simplified Schematic | Final Layout |
|---|---|---|---|
| **Bandwidth** | **> 193 MHz** | **200 MHz** | **200 MHz** |
| **Gain** | **26 dB** | **29 dB** | **28 dB** |
| **Gain Ripple** | **± 1 dB** | **± 0.02 dB** | **± 0.2 dB** |
| **Output Power** | **TBD** | **10.1 dB** | **10.2 dB** |
| **Power Added Efficiency** | **20-25%** | **24%** | **23.3%** |
| **VSWR** | **< 1.5:1 input & output** | **1.01:1 input 1.01:1 output** | **1.01:1 input 1.01:1 output** |
| **DC Supply Voltage** | **3.0 – 3.6 VDC** | **3.5 VDC** | **3.5 VDC** |

**Table 7, Specification Compliance Matrix for a Two Stage, S-band Power Amp.**

# 1.0) ABSTRACT

A vector modulator was developed for use within the Wireless Local Area Network (WLAN) frequency band. The amplitude and phase of the I (in-phase) and Q (quadrature) components are set via reflective attenuators, thus creating a flexible architecture that can generate quadrature phase shift keying (QPSK) while still supporting binary phase shift keying (BPSK). Optimal performance occurs at 5500 GHz, but with a -15 dB input impedance bandwidth from 5150 to 5875 MHz the modulator can operate over all frequencies in the WLAN band. Utilization of TriQuint's 0.5 um PHEMT GaAs process enabled the design to fit onto a 120 X 60 mil GaAs chip.

# 2.0) INTRODUCTION

A vector modulator allows the transmission of data across a wireless medium. The advantage of utilizing QPSK over BPSK is that for a given symbol rate within a system, the effective bit rate doubles since two bits can be sent simultaneously on the I and Q channels. This results in the bandwidth of the modulated signal being reduced by a factor of two.

A QPSK modulated waveform takes on one of four phase states; +45º, +135º, -135º, and 45º. The modulated signal that creates these phase states can be represented by the following equation:

$$S(t) = A_I \cos(wt) + A_Q \sin(wt)$$

The relative amplitudes of the I component ($A_I$) and Q component ($A_Q$) determine the phase state of the modulated signal based off the use of the trigonometric identity: $a\cos(wt) + b\sin(wt) = C\cos(wt + \theta)$ . The values of $A_I$ and $A_Q$ required to create a QPSK waveform are as follows:

| θ | $A_I$ | $A_Q$ |
|---|---|---|
| 45 | 1 | 1 |
| 135 | -1 | 1 |
| -135 | -1 | -1 |
| -45 | 1 | -1 |

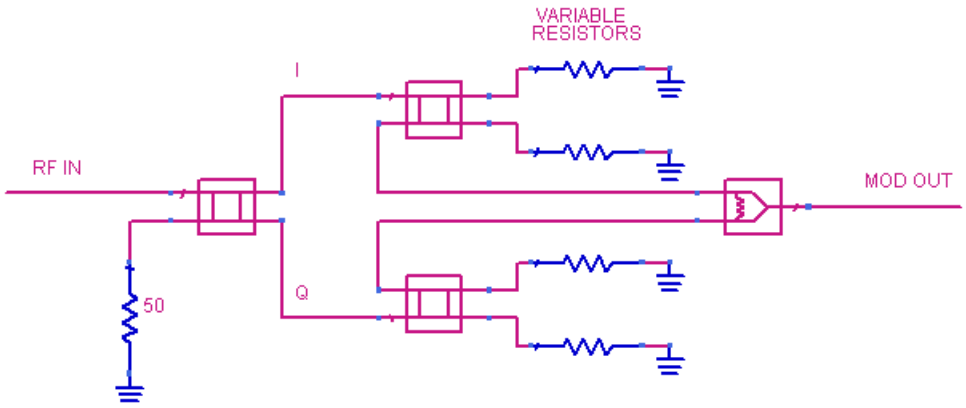
The vector modulator I designed inputs an RF tone with the generic form Acos(wt), and outputs a QPSK modulated waveform. This requires three sections within the modulator; a branch-line hybrid coupler to create the I and Q components, two reflective attenuators to vary $A_I$ and $A_Q$, and a Wilkinson power divider to then combine the I and Q components. The adjustment of $A_I$ and $A_Q$ are controlled via the application of a unique DC voltage to each I and Q channel.

My vector modulator design also enables the transmission of BPSK data. A BPSK modulated waveform can also be represented by the same equation above, but the signal only takes on two phase states: 0º and 180º. Therefore $A_Q$ is always set to 0 and the relative amplitude $A_I$ of is toggled between +1 and 1.

The design, simulation, and layout of my design were all performed in Advanced Design System (ADS) using TriQuint components. Due to the operating frequency of my design (5150 – 5875 MHz), all sections of the modulator were built with lumped elements.

# 3.0) DESIGN APPROACH

A block diagram of my I-Q vector modulator is shown below:




The following sections will provide a detailed description of each segment of the modulator.

## 3.1) Branch-line Hybrid Design

The individual 50 and 35 Ω sections of the branch-line hybrid coupler were created with lumped elements using low-pass π networks designed for operation at 5500 MHz. For the 50 Ω sections, the ideal values for the inductor and capacitors were 1.45 nH and 0.58 pF respectively. For the 35 Ω sections, they were 1.02 nH and 0.82 pF.

Ideally, a branch-line hybrid will output two signals that are equal in power (-3 dB in relation to the input) and 90º out of phase. I therefore utilized a branch-line hybrid on the input of my design to establish the I and Q components.

The key characteristics of a branch-line hybrid are output signals having equal amplitude and 90º phase difference, and an input impedance of 50 Ω on all four ports. It is possible to design a 90º branch-line hybrid that has an input impedance of approximately 50 Ω across the WLAN frequency band, but it is possible only to have a 90º phase difference at one frequency. As a result, I chose to design my 90º branch-line hybrid such that the two outputs had a 90º phase difference at 5500 MHz.

When substituting TriQuint components for the ideal inductor and capacitor values calculated for the low-pass π networks, I was able to obtain results that closely mirrored an ideal 90º branch-line hybrid. In particular, the phase difference of the two output ports was 89.64º. Also, the loss of the I component was -3.59 dB as opposed to -3.62 dB for the Q component. The additional loss in relation to the -3 dB ideal case is due to the inherent loss in the TriQuint inductors. The input match to all four ports on my 90º branch-line hybrid design was better than -15 dB across the WLAN band.

## 3.2) Reflective Attenuator Design

A reflective attenuator is designed by taking a 90º branch-line hybrid and intentionally mismatching the through and coupled ports, thereby creating reflected power that can be captured on the isolated port. When an ideal 90º branch-line hybrid is loaded with 50 Ω terminations on its through and coupled ports, no power is delivered to the isolated port. The greater the mismatch on the through and coupled ports, the more power that will be delivered to the isolated port.

The goal of the reflective attenuators used in my design is to produce outputs that have relative amplitudes of either 0, +1, or -1. In other words the reflective attenuator will output signals that have a power level of either 0 Watts, or some other non-zero power level with 180º phase separation for the ± 1 case. As mentioned above, the 0 case occurs when the through and coupled ports are loaded with 50 Ω. The ± 1 cases can be obtained from many different resistance values, but the resistances must be paired up such that they create a reflection coefficient with equal magnitude and opposite phase based off the following equation:

$$\Gamma = \frac{R_{OUT} - 50}{R_{OUT} + 50}$$

The greater the magnitude of Γ, the more power that will be delivered to the isolated port. It is desirable that the reflective attenuator design supply as much power as possible to the isolated port as this translates into less insertion loss in the in the I-Q vector modulator as a whole. The maximum magnitude of Γ is 1, and this occurs when Rout is either a short or open circuit. A short would create a relative amplitude of -1, and the open +1.

For my reflective attenuator design, I am using the drain of a TriQuint 0.5 um PHEMT as the variable attenuator on the through and coupled ports. The drain of this PHEMT consists of a parallel RC circuit, where the resistance is adjustable via the voltage supplied to the gate. When the PHEMT is biased near its $I_{DSS}$ level a very low resistance is provided. When the PHEMT is biased near pinch-off, a large resistance is presented. Even when the PHEMT is fully turned 'ON' however, a resistance of 0 Ω can not be obtained. The larger the physical size of the PHEMT, the lower the resistance value that can be achieved. On the contrary, a larger PHEMT also results in a greater parallel capacitance. This is undesirable because an ideal reflective attenuator requires a purely resistive load. In the 'ON' state, the effects of the parallel capacitance are negligible because the low resistance value dominates. In the 'OFF' state however the effects of this capacitance is much more pronounced. Therefore a compromise must be made in choosing a PHEMT size that provides adequate 'ON' resistance while keeping parallel capacitance at a minimum.

For my design a I chose a 200 um PHEMT, which provided an 'ON' resistance of 10 Ω. I was able to resonate out the parallel capacitance of this PHEMT by placing an ideal

8.45 nH inductor across its drain-to-source leads, but since this inductor would be physically large to implement via a TriQuint spiral inductor I chose not to include it in my final design as the effects of the parallel capacitance using a 200 um PHEMT was not too severe.

A reflective attenuator is required for both the I and Q channels to set the relative amplitudes of $A_I$ and $A_Q$. To set the value of either $A_I$ or $A_Q$ to +1, the PHEMT devices on both the through and coupled ports of the branch-line hybrid are biased in the 'ON' state thus setting the load on these ports to 10 Ω. Conversely, to set the value of $A_I$ or $A_Q$ to -1 the PHEMT devices are biased in the 'OFF' state thus setting the load on these ports to 250 Ω. To set the value of $A_Q$ to 0 for BPSK modulation, the PHEMT devices are biased to present 50 Ω to the ports. The following gate voltages are used to bias the 200 um PHEMT devices in the reflective attenuator:

| Vgs (V) | R (Ω) |
|---|---|
| -0.66 | 250 |
| -0.52 | 50 |
| 0.05 | 10 |

## 3.3) Wilkinson Power Divider Design

The 70 Ω sections of the Wilkinson power divider were created with lumped elements using low-pass π networks designed for operation at 5500 MHz. The ideal values for the inductor and capacitors were therefore 2.05 nH and 0.41 pF respectively.

Ideally, when used as a splitter a Wilkinson power divider will output two signals that are equal in power (-3 dB in relation to the input) and phase. When used as a combiner, it will equally sum two inputs that are 90º out of phase. I therefore utilized a Wilkinson power divider on the output of my design to sum the I and Q components.

For simplicity I chose to analyze my Wilkinson power divider as a splitter, recognizing that if I designed it correctly in this regard its use as a combiner would be transparent. The key characteristics of a Wilkinson power divider used as a splitter then are output signals the have equal amplitude and phase, and an input impedance of 50 Ω on all three ports. I designed my Wilkinson power divider to meet all of these specifications across the WLAN band. Additionally, my design was based off the two outputs having an absolute phase lag of 90º at 5500 MHz.

When substituting TriQuint components for the ideal inductor and capacitor values calculated for the low-pass π networks, I was able to obtain results that closely mirrored an ideal Wilkinson power divider. In particular, the phase and amplitude differences between the two output ports was indistinguishable, with the loss on both output ports measuring at -3.27 dB. The additional loss in relation to the -3 dB ideal case is again due to the inherent loss in the TriQuint inductors. The input match to all three ports on my Wilkinson power divider was also better than -15 dB.

### 3.4) Design Specifications

The following chart shows the specifications for my vector modulator design. As the attached plots in the Simulated Data section will show, all specifications were met except for input compression point when the phase state is set to -135º.

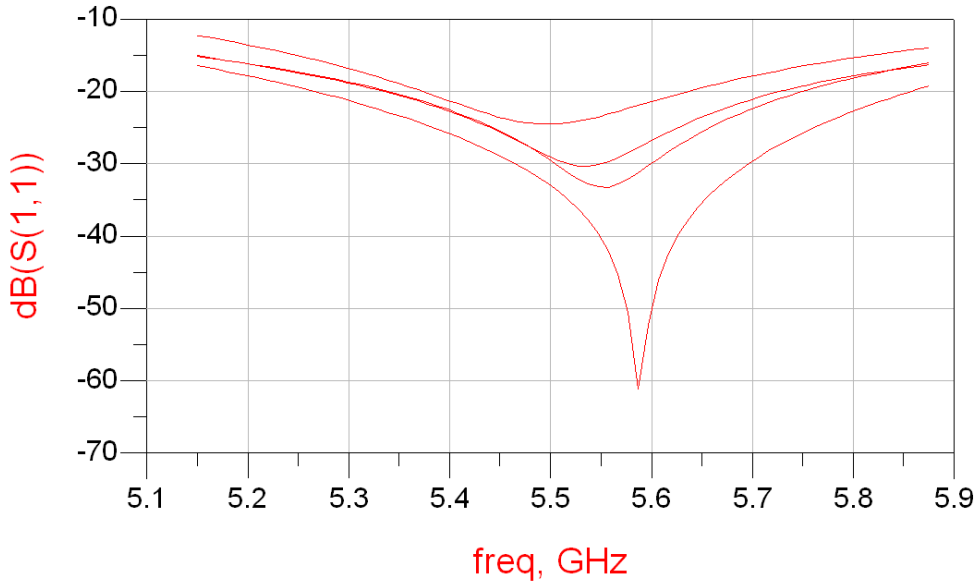
| Specifications | | | |
|---|---|---|---|
| | MIN | TYP | MAX |
| RF Frequency Range (MHz) | | 5150 - 5875 | |
| I/Q Frequency Range (MHz) | | DC – 50 | |
| I/Q to RF Isolation (dB) | 10 | 16 | |
| Conversion Loss (dB) | | 7 | 10 |
| Input Compression Point (dBm) | 0 | 7 | |
| VSWR | | 1.5:1 | 2.5:1 |

# 4.0) Simulated Data

The following data is taken from simulations in ADS.

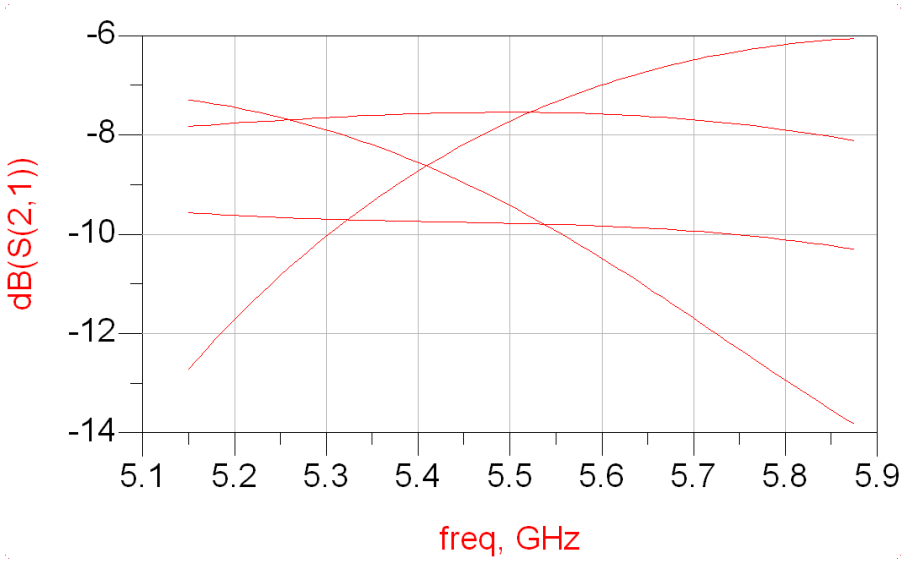
### 4.1) Input Match

The input matching plot is swept across the 5150 – 5850 frequency band, with one plot being taken for each of the four nominal phase states of a QPSK modulated waveform. The nominal phase states constitute the PHEMT's in the reflective attenuator being biased to either 10 or 250 Ω.



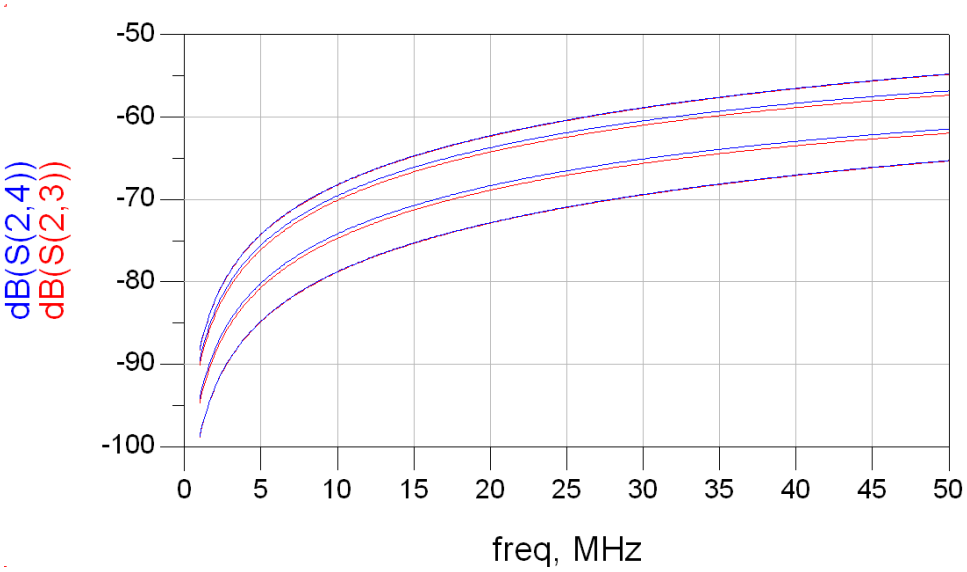
## 4.2) Gain

The gain plot is swept across the 5150 – 5850 frequency band, with one plot being taken for each of the four nominal phase states of a QPSK modulated waveform. As can be observed, the gain varies with each phase state as a result of the reflective attenuators not being ideal. In any case though, at the design center frequency of 5500 MHz insertion loss is less that 10 dB.



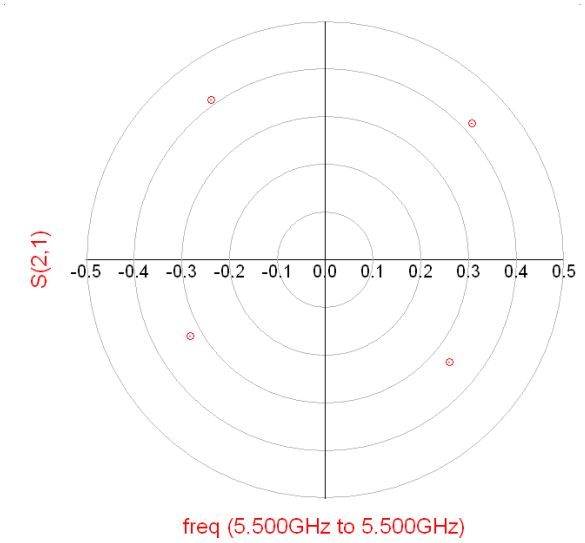

## 4.3) I/Q to RF Isolation

The isolation plot is swept across DC – 50 MHz with one plot being taken for each of the four nominal phase states of a QPSK modulated waveform.



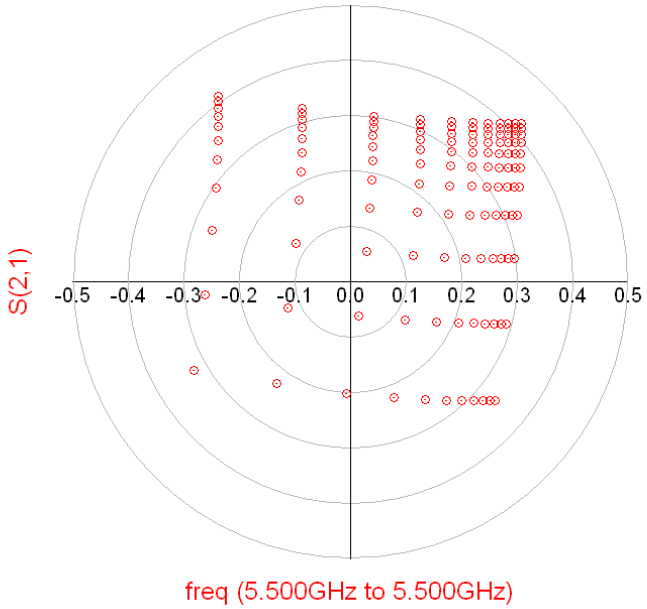
## 4.4) Constellation Diagram @ 5500 MHz

The following constellation diagram was taken with the load resistances set to 10 and 250 Ω on the reflective attenuators.



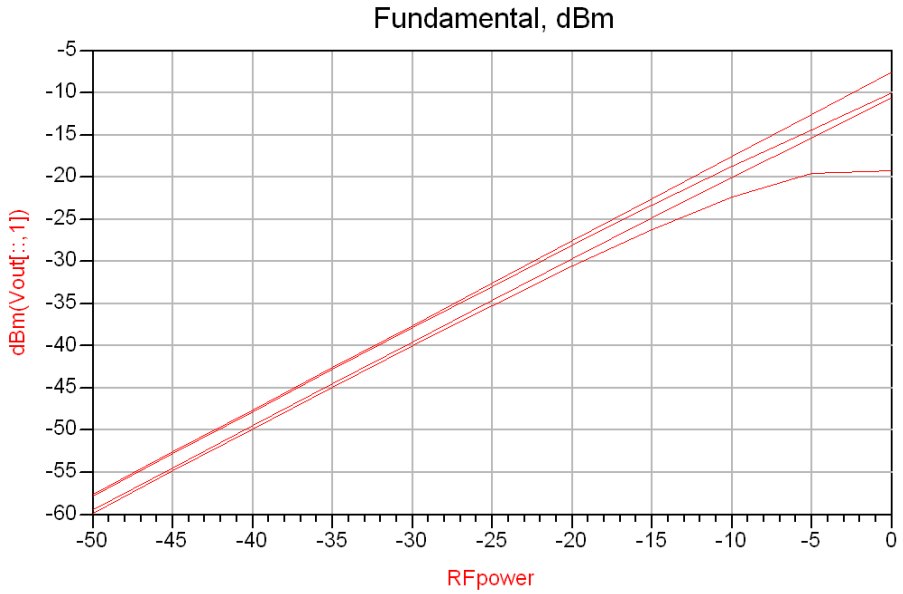

## 4.5) Constellation Diagram @ 5500 MHz Across Multiple Attenuator Settings

The following constellation diagram was taken with the load resistances set to multiple values in-between 10 and 250 Ω on the reflective attenuators. As can be observed, a square is formed by varying these resistance with any point inside the square being realizable.



## 4.6) Input Compression Point

The following plot shows input vs. output power at 5500 MHz across all four nominal phase states of a QPSK modulated waveform. As can be observed, the input compresses rapidly when the phase state is set to -135º. At this phase state both the I and Q reflective attenuators are biased to 250 Ω meaning the PHEMT's are biased are near pinch-off.

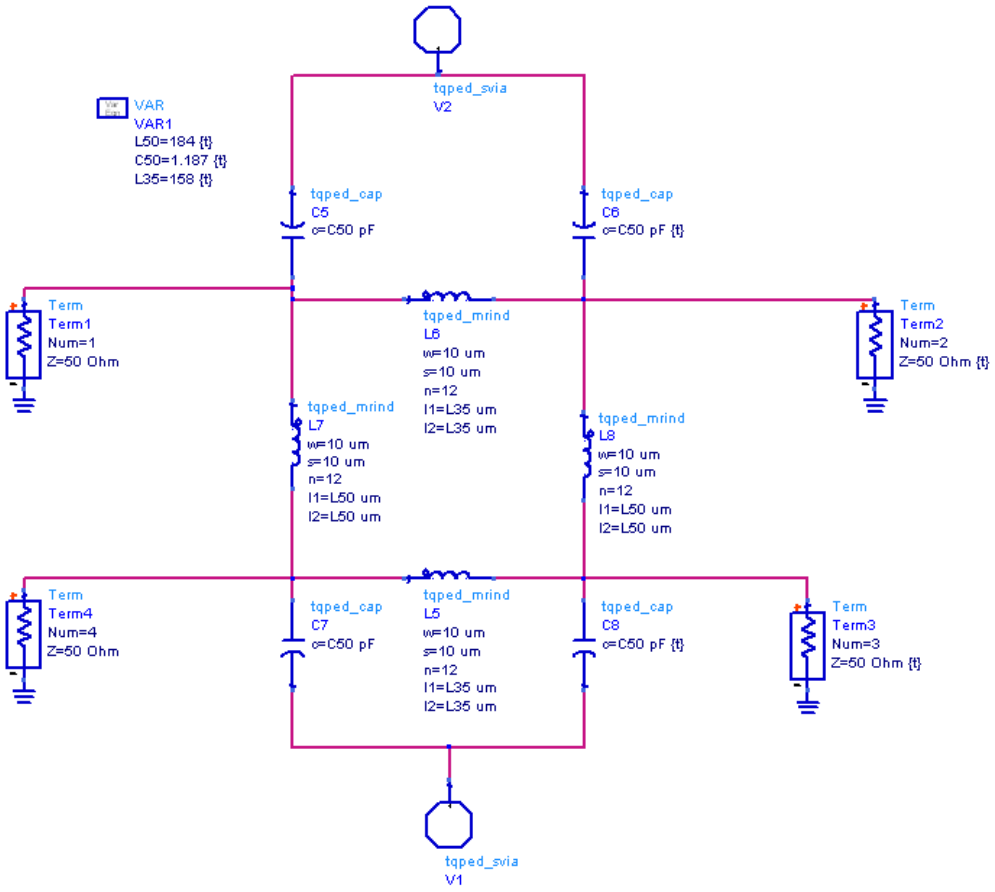



→ I = -0.66 V, Q = -0.66 V

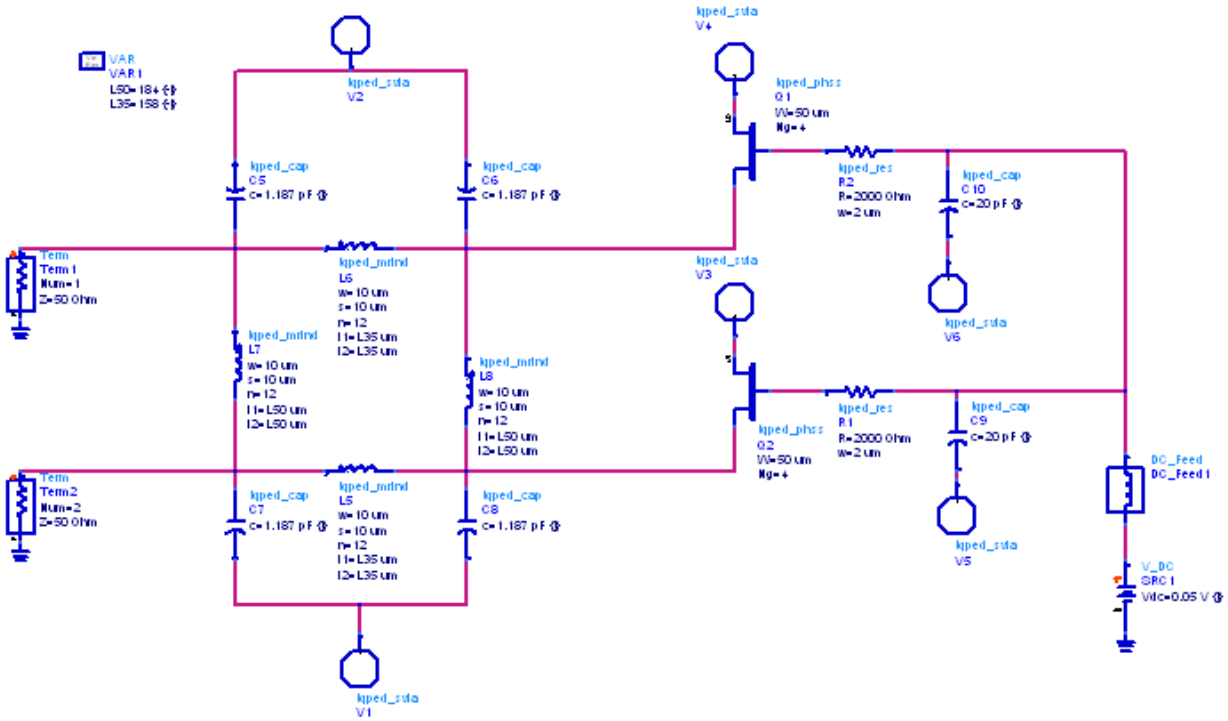
# 5.0) Schematic

The following sections show the three individual segments of my I-Q vector modulator design along with overall schematic.

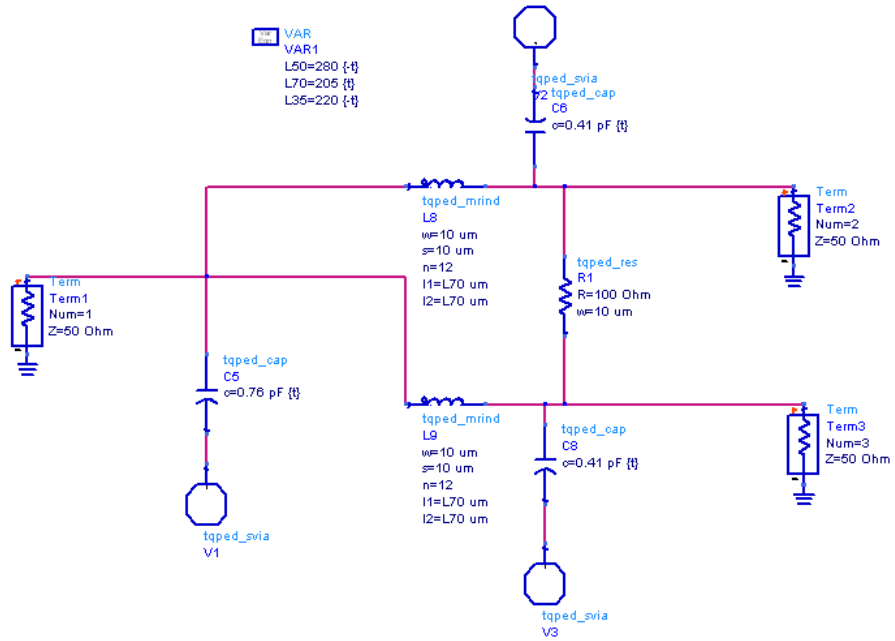
## 5.1) Branch-line Hybrid



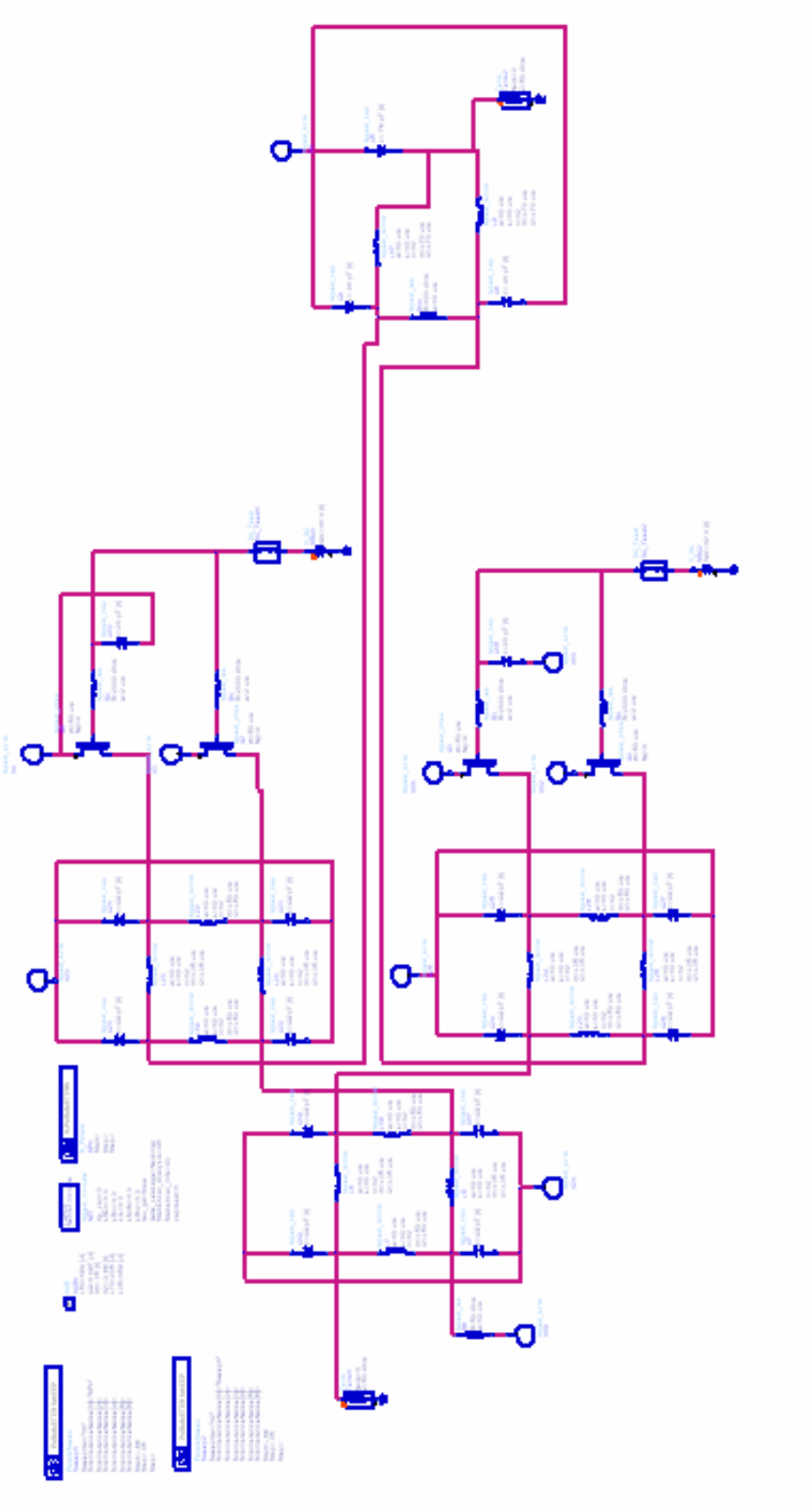
## 5.2) Reflective Attenuator



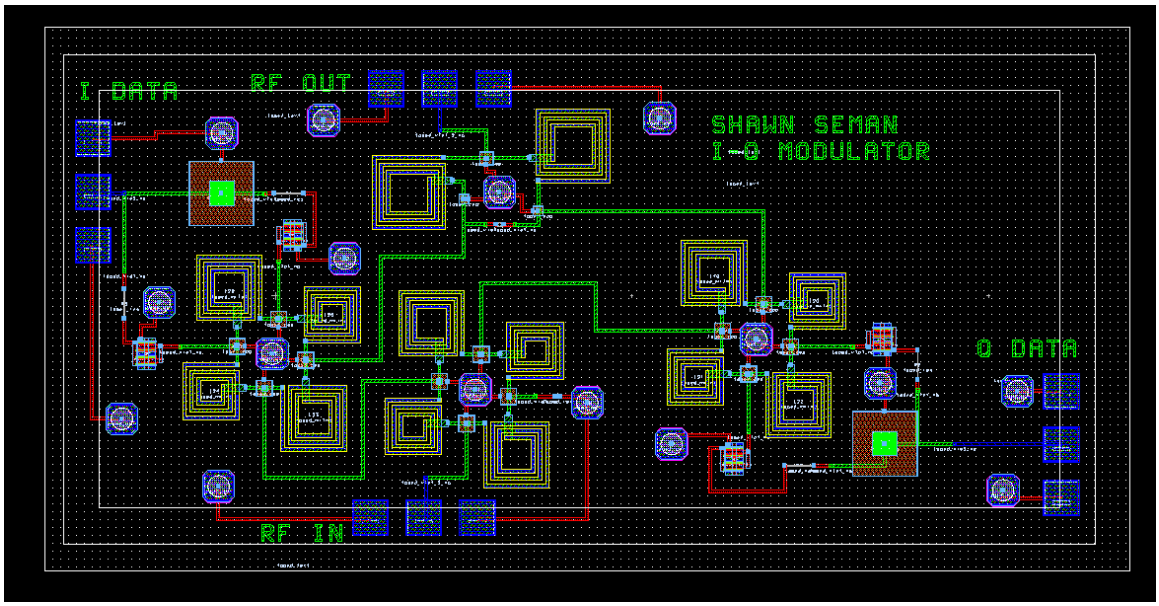

## 5.3) Wilkinson Power Divider



## 5.4) I-Q Vector Modulator



# 6.0) Layout




# 7.0) Test Plan

To test my I-Q vector modulator I will need a vector network analyzer (VNA) and two DC power supplies to bias the I and Q channels.

My plan is to test my design in three phases:

1) I will measure input match and gain across frequency for all four nominal QPSK phase states. The following table shows the DC voltages needed for these phase states:

| θ | I | Q |
|---|---|---|
| 45 | 0.05 | 0.05 |
| 135 | -0.66 | 0.05 |
| -135 | -0.66 | -0.66 |
| -45 | 0.05 | -0.66 |

2) I will measure input compression point and generate a constellation diagram at 5500 MHz for all four nominal phases states listed in Step 1.

3) I will tune the I and Q bias voltages to create a constellation diagram that places the phase states at exactly +45º, +135º, -135º, and -45º with equal magnitudes. This will involve setting the I and Q voltages somewhere between 0.05 and -0.66 V.

# 8.0) Summary and Conclusion

The use of TriQuint's 0.5 um PHEMT GaAs process in conjunction with ADS enabled the development of a MMIC I-Q vector modulator in the WLAN frequency band. Expectations from simulated data are that this modulator will operate over a wide bandwidth with low insertion loss. The flexible architecture of the design will enable the design to be tuned to an optimal performance level via the biasing of the I and Q channels. The design also has the additional appeal of being compatible with both QPSK and BPSK systems.

The one area of concern with this design is that simulated data shows the input compresses at a much lower power level when the phase state is set to -135º. In this phase state the PHEMT's in the reflective attenuators are biased near pinch-off, so it will be interesting to see if the simulations are accurate.

The hardest challenge posed during the design process was developing the reflective attenuators. As discussed in the Design Approach section, usually the difficult aspect of this particular design is the parallel capacitance present in the drain of the PHEMT. However even using pure resistances to load the through and coupled ports of the branch-line hybrid, I could not create an ideal reflective attenuator with TriQuint inductors and capacitors. Therefore for this design to perform more optimally without requiring tweaks on the I and Q channel bias voltages, I would recommend doing the design with distributed elements if at all possible.

# 9.0) References

Penn, John E. "A Balanced Ka-Band Vector Modulator MMIC." Microwave Journal, June 2005

Egan, Jonathan. "Vector Modulator." MMIC Design Final Report, Fall 2006

Pozar, David M. "Microwave and RF Design of Wireless Systems." Jon Wiley & Sons, Inc. 2001

http://en.wikipedia.org/wiki/Phase-shift_keying