

**Fall 2008 JHU EE787 MMIC Design Student Projects
Supported by TriQuint, and Applied Wave Research
Professors John Penn and Dr. Michel Reece**

Medium Power Amplifier—Matt Crowne
Phase Shifter C-band – Mitesh Patel
Mixer S-Band – Brendan McElrone
Power Amplifier C-band – Ben Brawley

Low Noise Amplifier – Minhaj Raza
Small Signal Amplifier – Tom Pierce
Power Amplifier C-band – D. Durachka
Volt. Cont. Osc. C-band – Kang Yuan



Matthew Crowne
525.787 MMIC Design
Fall 2008
Instructor: John Penn
C-Band Low Power PA

Abstract

A C-Band power amplifier for lower power applications was designed using the Triquint GaAs MMIC library and Applied Wave Research's Microwave Office design environment. The amplifier consists of two cascaded stages and is intended to maximize efficiency over other design parameters. The amplifier is centered at 5.5 GHz and achieves 38% power added efficiency and 20 dB of Gain across a +/- 200 MHz bandwidth with 9 dBm output power.

Introduction

A single ended C-Band power amplifier was designed for maximum efficiency on a Triquint MMIC process. The amplifier consists of two stages utilizing enhancement mode GaAs PHEMTs with on-chip matching networks. The driver stage has a gate periphery of 16um and is biased class AB. The final stage has 72um of gate periphery and is biased deep class B. The design is intended to run off a single 3.3V supply and has internal bias circuitry to produce the gate voltage. In Addition, separate gate pads are provided that can both check the bias points of the PHEMTs or, if necessary supply gate bias. This design allows maximum flexibility for prototype development.

A simplified schematic is shown in Figure 1. The output matching network was designed to maximize efficiency. The interstate match also had to be designed for gain and efficiency, while the input match could focus on increasing gain.

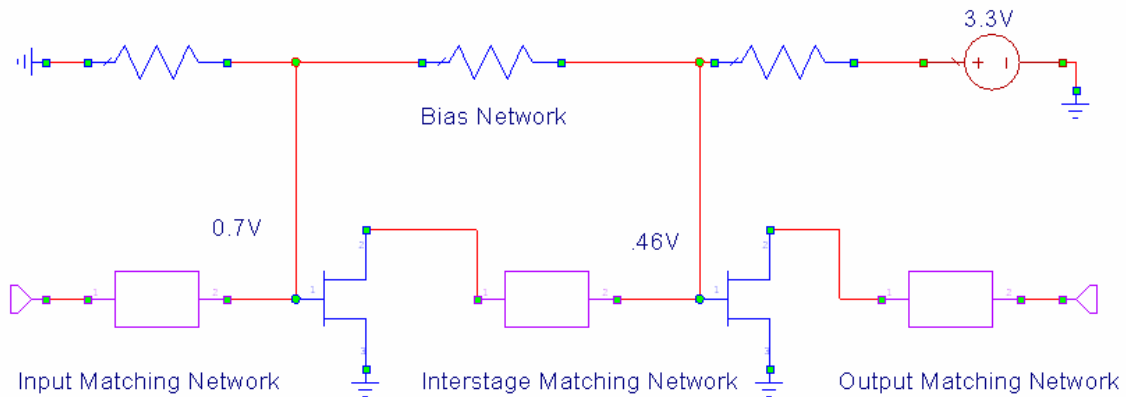


Figure 1. – Simplified Schematic

Table 1 summarizes key performance parameters across the operating bandwidth.

Frequency	Pout	Gain	PAE
GHz	dBm	dB	%
5.3	9.58	20.39	38
5.5	9.89	20.74	43.25
5.7	9.26	20.15	40.27

Table 1. - Key Performance Parameters

Design Approach

The amplifier was designed to maximize efficiency for a low power application. The metrics used to design this amplifier are summarized in Table 2

	Spec	Goal
BW:	5.3 Ghz-5.7GHz	
Pout:	9 dBm	10 dBm
PAE:	>40%at fc	40% across the bandwidth
Gain Ripple:	+/- 0.5	+/- 0.5

Table 2. – Specifications and Goals

Several approaches were investigated for meeting these specifications. Approaches that seemed promising early in the design phase utilized class-F or some other high efficiency technique. However, such an approach requires more components than a traditional matching network. Ideal simulations that appeared promising quickly lost their appeal when the low quality inductors inherent with Triquint and other GaAs MMIC processes. When the results reduced to efficiencies that are achievable with a deep class B approach the simpler matching networks they offered became more attractive. The DCIV plots are shown in Figure 2. For the driver stage $V_{gs} = 0.7V$ and for the final stage $V_{gs} = 0.5V$. These values were tuned in the final design

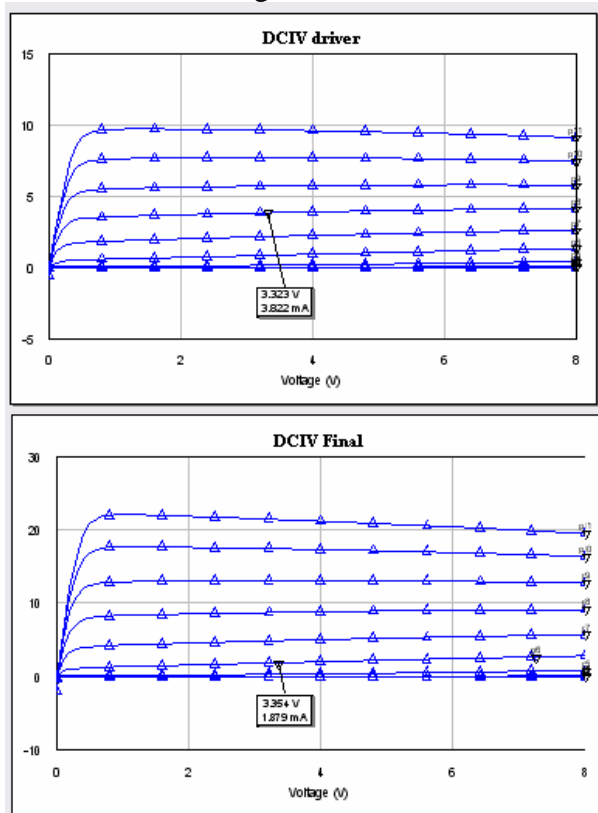


Figure 2 – DCIV curves

As a deep class B bias excluded a Cripps method approach to determining optimum output load, a load-pull simulation was performed on the output FET model. The load pull contours are shown in figure 3 for 5.5 GHz. The simulated ideal output matching network is indicated with the red “x” and the maroon “x” is the output match from the finalized layout.

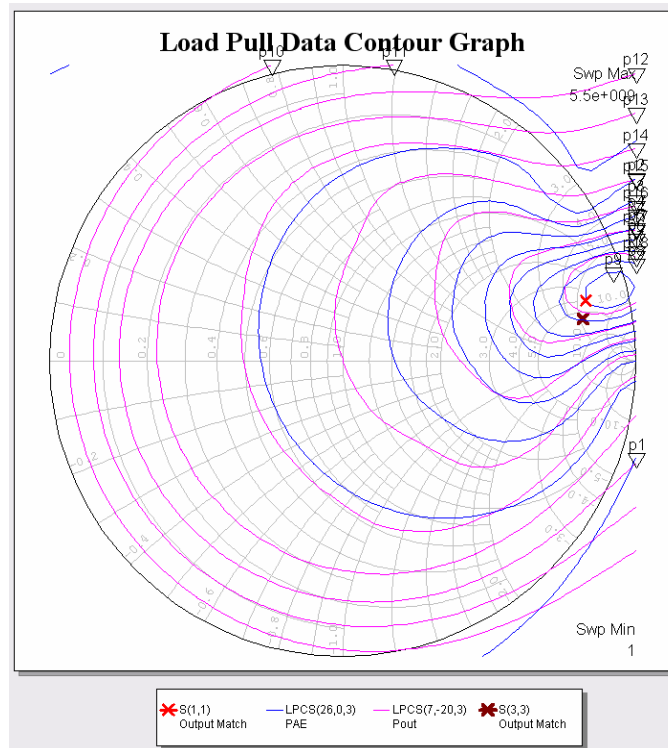


Figure 3 – Load Pull and Matching Networks

The best match for both the PAE and Pout are located on the edge of the smith chart, this is a product of the deep class B bias on the devices means that the match that will be limited in bandwidth. As the design is meant to maximize PAE at the center frequency (with a goal of extending that over +/- 200 MHz) this will still be suitable for our design. The match was achieved with a shunt inductor-series cap combination that also provides a drain voltage insertion and a DC block on the output of the MMIC.

Next, the input matching network for the first stage was designed for the driver stage. The IMN was designed to provide the maximum gain available. Figure 4 shows the available gain circles and the results of the IMN simulation. The design would be revisited for final tuning after the layout was near completion.

The interstate matching network was the final component to be designed. In an interstate matching network, the output of the driver stage is matched to the input of the final stage without having an intermediate 50 ohm match in between. A shunt inductor series capacitor pi pad topology was chosen to achieve this match and allow convenient bias insertion for the drain of the driver and the gate of the final stage.

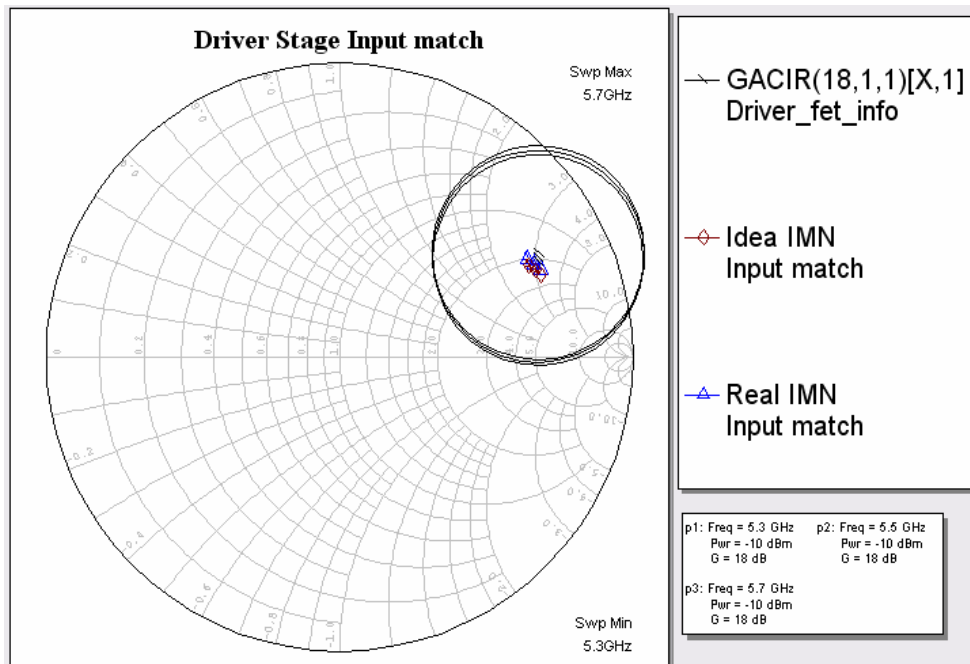


Figure 4. – Available gain circles and input match for the driver stage

The design is stabilized with a shunt resistor on the power device with a large cap to ground. In this location the resistor will not dissipate significant RF power and the DC blocking cap to ground ensures no DC power dissipates in the resistor. It was decided not to put a stabilizing resistor onto the driver stage as a significant amount of gain was lost with the addition of the 200 ohm resistor on the final. The combined amplifier has an input and output mu value greater than 1 and with 50 ohm terminations the amplifier should not oscillate. Figure 5 shows the stability factor over frequency.

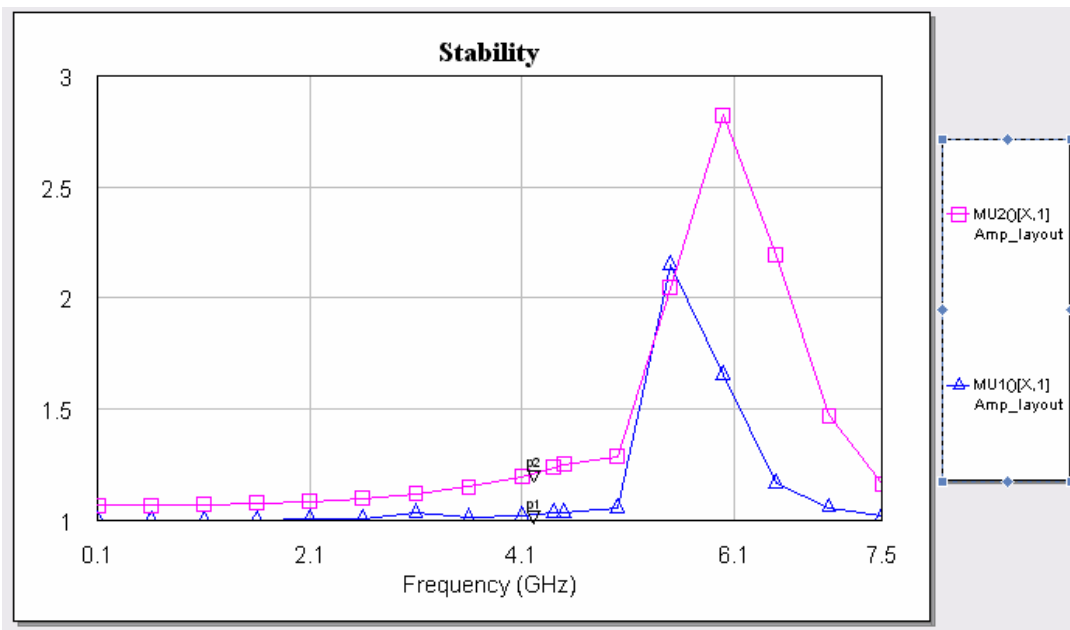


Figure 5.-Stability factor for the final design

Figures 6 and 7 shows the combined amplifiers performance after the layout was finalized. Figure 6 shows the amplifiers power output, PAE and power gain as the input power is increased at the center frequency of 5.5 GHz.

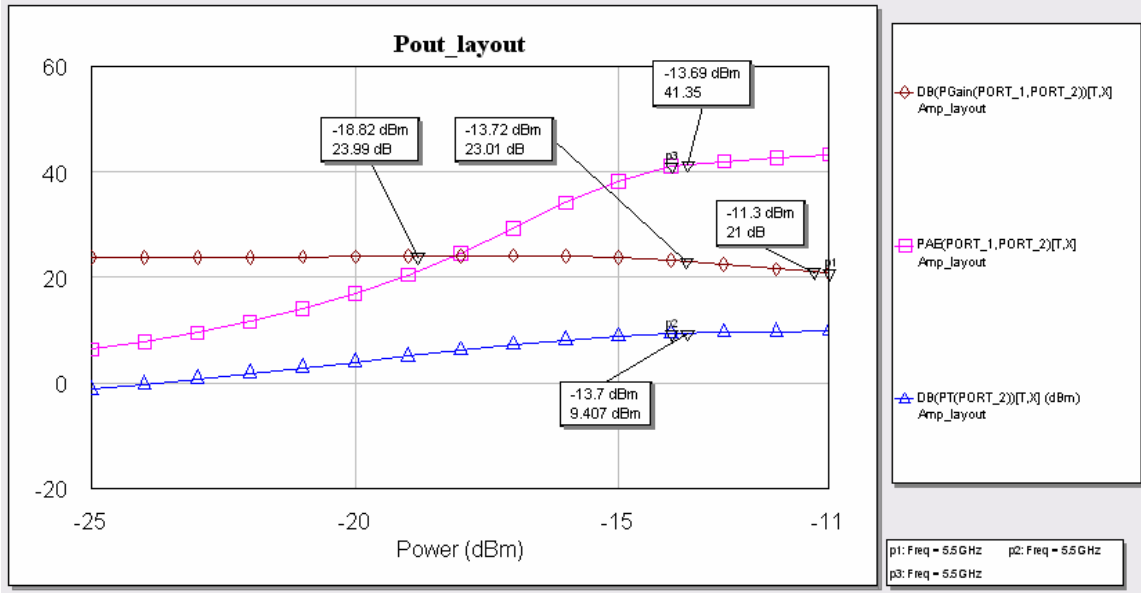


Figure 6 – Pout, PAE and Gain vs. Pin

Figure 7 shows a power sweep with a fixed Pin. When driven properly 38% PAE is achieved as is a Pout greater then 9 dBm with 20 dB of gain from 5.3 GHz to 5.7 GHz.

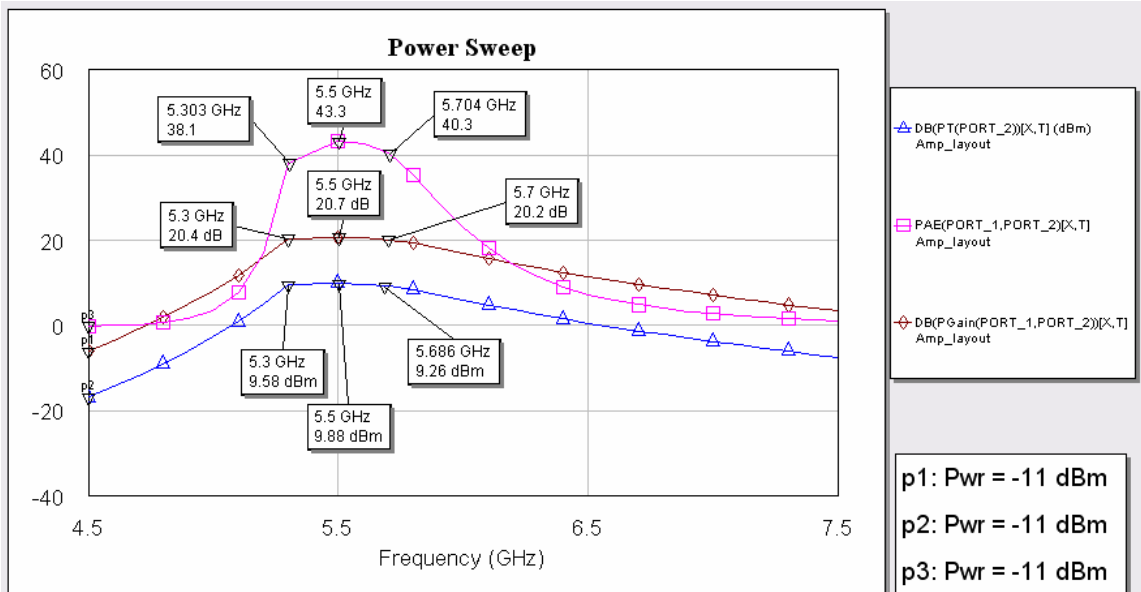


Figure 7 – Pout vs. Frequency

The simplified schematic is presented below in figure 8. The simulated data presented here used AWR's transmission line models on the Triquint substrate that have been removed for clarity, see Appendix A for the full schematic. From left to right are the amplifier's input matching network, driver stage, interstage matching network, final stage, and the output matching network. The bias network runs along the bottom of the amplifier.

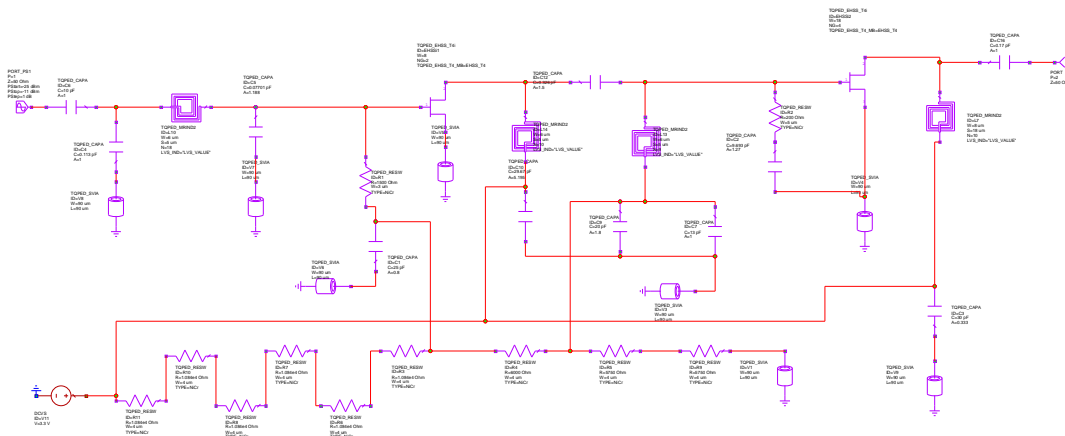


Figure 8 – Amplifier Schematic

The layout is shown in figure 9. The input is at the bottom of the chip and the output is at the top. The RF ports use ground-signal-ground ports for maximum RF performance. To the left are the supplementary gate bias ports. On the right hand side is the main power pin and a supplemental ground pin as well. Layout successfully passed ICED design rule check before submission to Triquint.

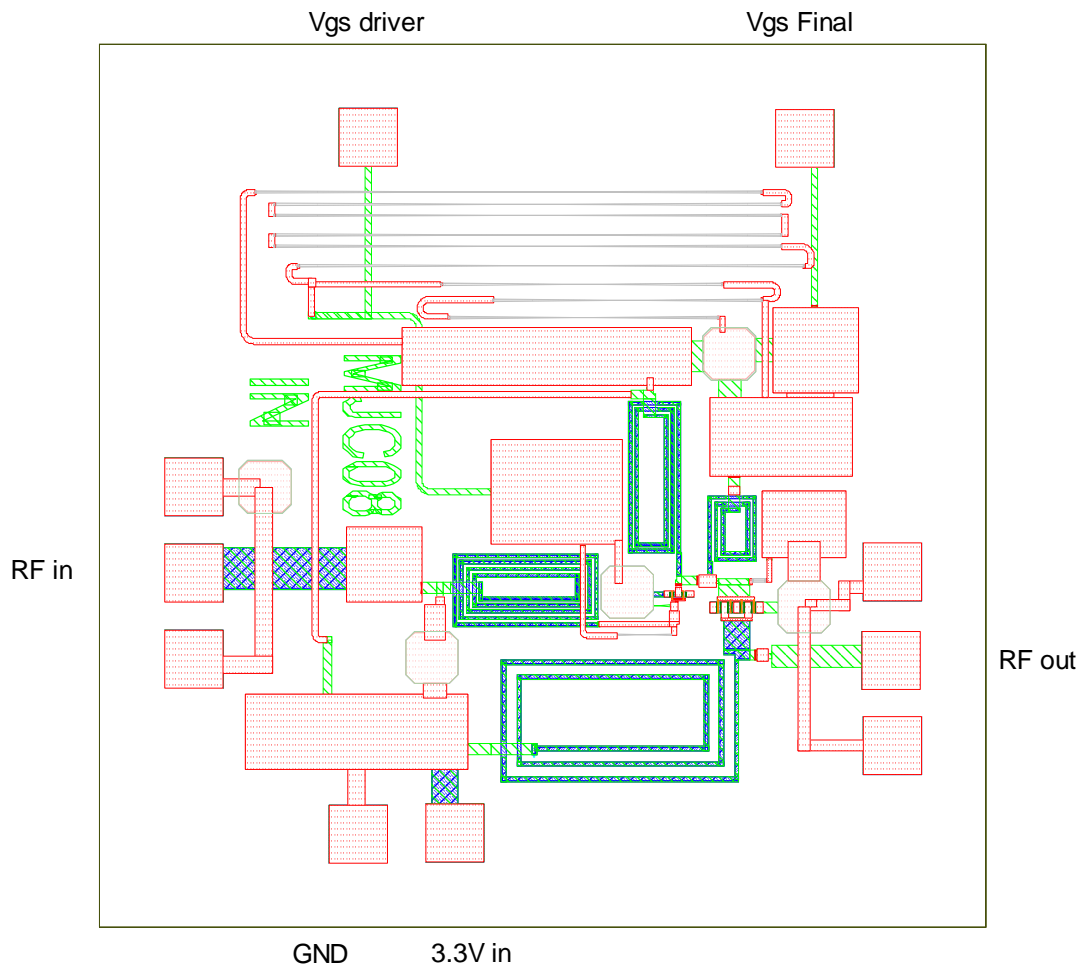


Figure 9 – Amplifier MMIC Layout

Test Plan

Test equipment needed:

1. Agilent 8510 Network Analyzer (or equivalent)
2. Agilent E3632A power supply (or equivalent)
3. Agilent 34410A DMM (or equivalent)
4. Agilent 8683B signal generator (or equivalent)
5. Agilent E4416A power meter (or equivalent)
6. Agilent 8480 Power sensor (or equivalent)

The Amplifier should be connected to a 3.3 V power supply which has been current limited to 20 mA. As the design consists of PHEMTs and contains internal bias circuitry there is not the concern of damaging the devices if there is not gate bias applied before the drain bias.

Test procedure:

1. With no RF source applied, power on DUT power pin with 3.3V and record quiescent current:
 _____ mA (approximately 3 mA)
2. Set logic analyzer so that Pout < -20 dBm and frequency from 2.5 GHz to 7.5 GHz. Record the small signal gain and the small signal S11 and S22.
 _____ S11
 _____ S22
 _____ S21

This will verify the general health of the amplifier as well as check that the design is centered at 5.5 GHz

3. Set the signal generator for -20 and 5.3 GHz and perform the following measurements (Grayed cells are calculated parameters.)

Pin = -20 dBm			
Frequency	Pout	Gain	Current
GHz	dBm	dB	mA
5.3			
5.5			
5.7			

1 dB compression Measurements						
Frequency	Pin at P1dB	P1dB	Gain @ P1	Current	Pconsumption	PAE
GHz	dBm	dBm	dB	mA	mW	%
5.3						
5.5						
5.7						

3 dB compression Measurements						
Frequency	Pin at P3dB	P3dB	Gain @ P3	Current	Pconsumption	PAE
GHz	dBm	dBm	dB	mA	mW	%
5.3						
5.5						
5.7						

Table 3. - Tabulated Data

Conclusions

A C-Band power amplifier was designed that achieves greater than 38% efficiency and 9 dBm out with 20 dB of gain across 400 MHz of bandwidth. All design specifications were achieved. Due to the design tradeoffs to maximize efficiency not all of the design goals were achieved, a summary of the simulated performance is given in table 4.

	Spec	Goal	Simulated	Measured
BW:	5.3 Ghz- 5.7GHz			
Pout:	9 dBm	10 dBm		
PAE:	>40%at fc	40% across the bandwidth		
Gain Ripple:	+/- 0.5	+/- 0.5		

Table 4. - Specs, goals, and worst case measured parameters

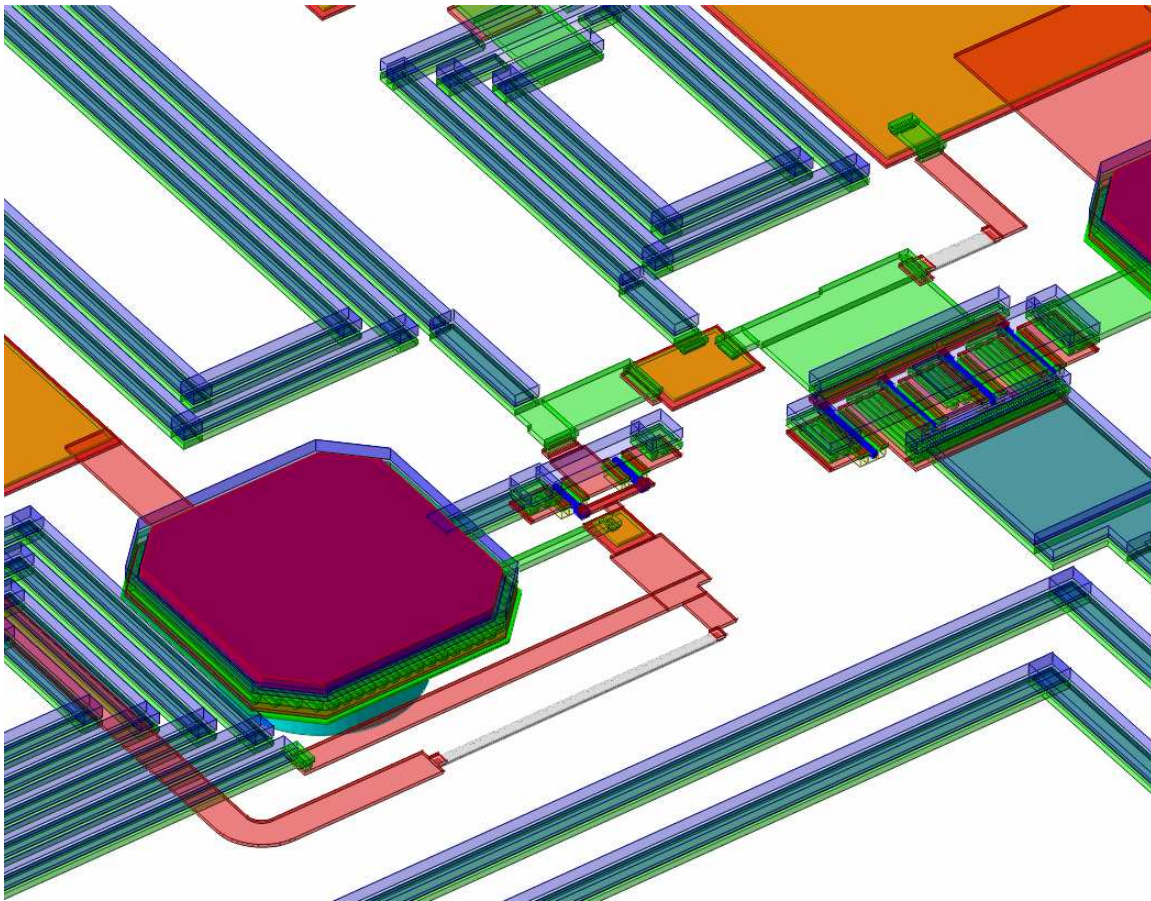
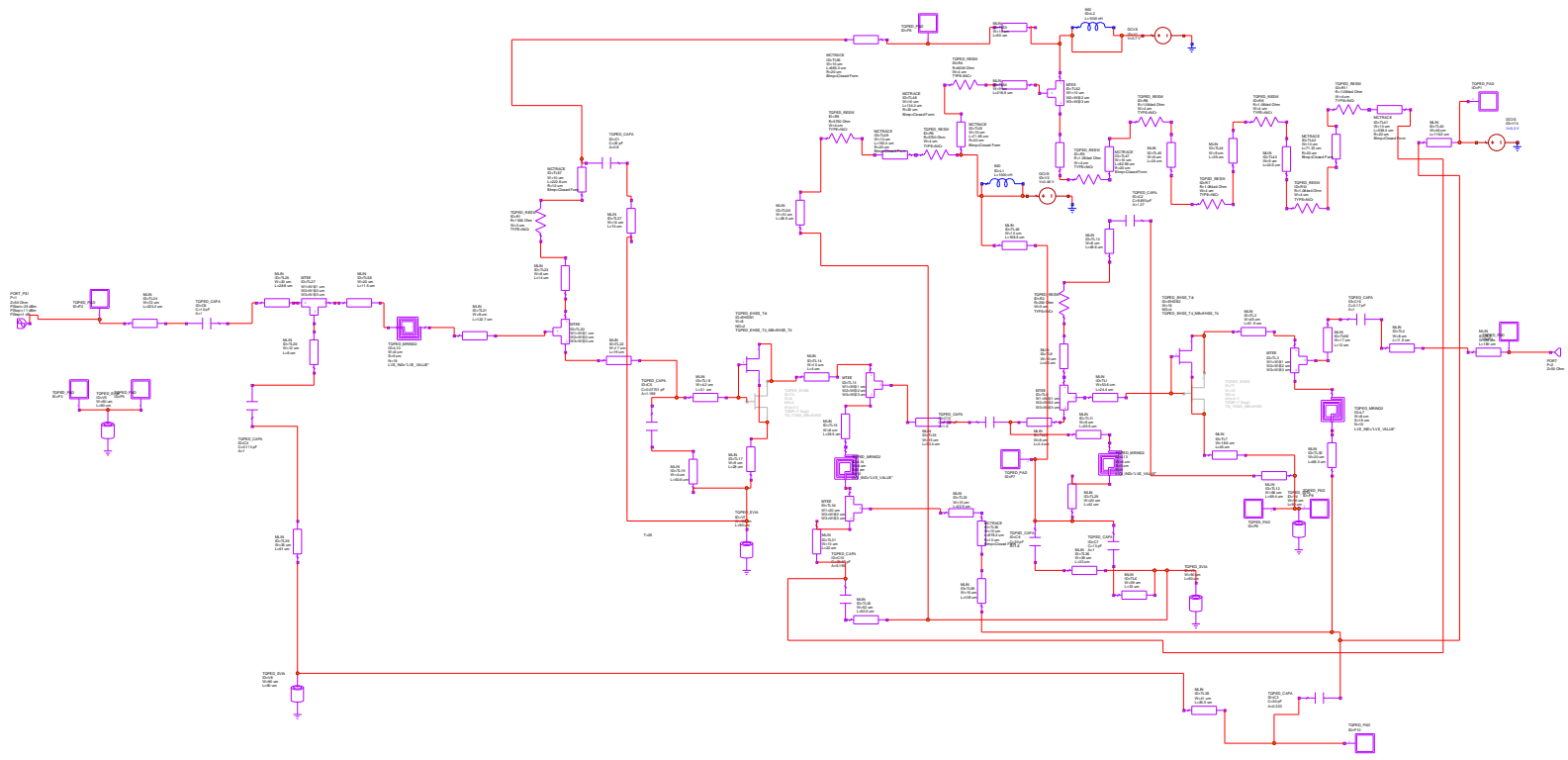


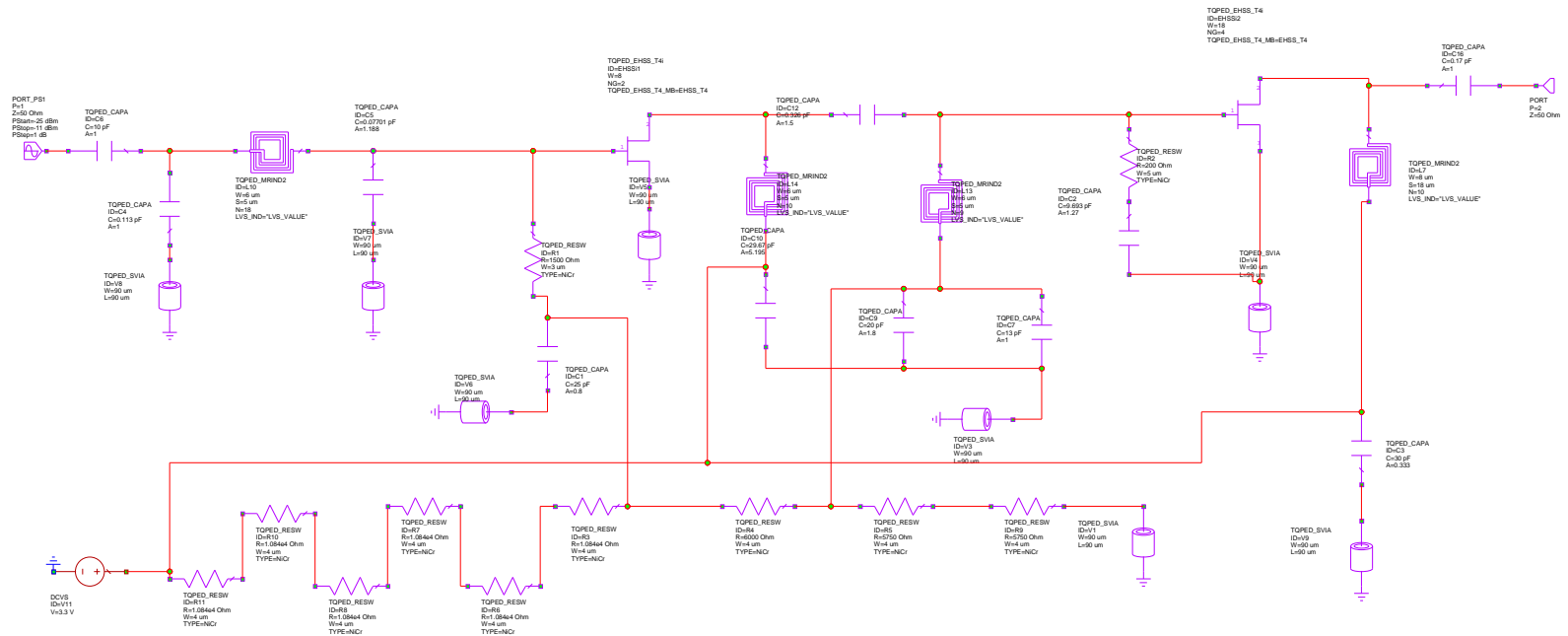
Figure 10. – close up of the transistors

APENDIX A – Schematic Views

Full Schematic



Simplified Schematic



“Swami Shreeji”

**MMIC EE787 Final Report
C-Band 3Bit Phase Shifter
Fall 2008**

By: Mitesh Patel

Table of Content

<u>1.Abstract.....</u>	<u>3</u>
<u>2.Introduction.....</u>	<u>3</u>
<u>3.Design Approach.....</u>	<u>3</u>
<u>a.Specification vs. Goals.....</u>	<u>4</u>
<u>b.Tradeoffs.....</u>	<u>4</u>
<u>4.Simulations</u>	<u>5</u>
<u>5.Schematic.....</u>	<u>7</u>
<u>a.Switch Schematic.....</u>	<u>7</u>
<u>b.RF Schematic</u>	<u>7</u>
<u>c.DC Schematic</u>	<u>8</u>
<u>6.Layout Plot</u>	<u>8</u>
<u>7.Test Plan</u>	<u>9</u>
<u>8.Summary & Conclusions.....</u>	<u>9</u>
<u>Appendix A.....</u>	<u>10</u>

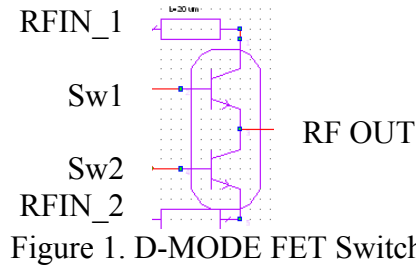
1. Abstract

This report talks about C- Band 3bit phase shifter designed using Microwave Office from AWR inc. and Triquent's TQPED library for a MMIC design. Each bit is switched between +/- 22.5, +/- 45, and +/- 90 giving relative phase shift from 0 to 360deg in 45deg increment at center frequency of 5.5Ghz. The design was layout on 60mil x 60mil AnaChip.

2. Introduction

A 3-bit phase shifter is a circuit element used in many applications, especially in Radar. A phase shifter takes RF signal in and output same RF signal but at different phase. In radar application, by changing the phase of signal, you can steer the beam of antenna in different angle without physically moving the antenna. Hence, you can scan a wide region without even moving the antenna. By changing the phase rapidly, one can change the direction of beam digitally at very fast rate. Here, Phase shifter plays a key roll.

3. Design Approach



As shown above, each bit of phase shifter has two FET switches, which switches either of two inputs (RFIIN1 or RFIN2) to RF Output and vice versa. Another word, depending on voltage applies to Sw1 and Sw2, RF1 is connected to RF OUT or RF2 is connected to RF Out.

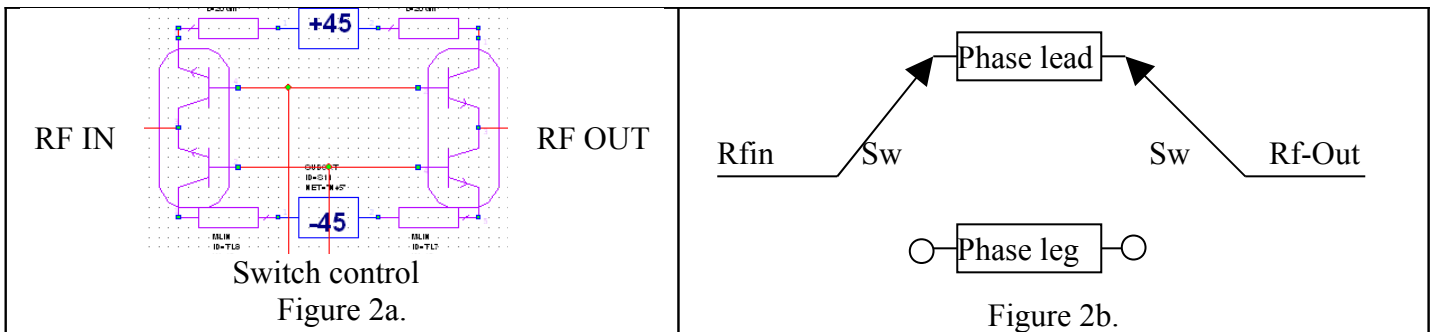


Figure 2. Single Bit circuit.

When we combine two switches with circuit which lead or leg phase by certain amount, we get 1bit phase shifter, as shown above. In figure 2a, when switches are connected to top circuit (hence bottom switch off) we get Phase lead by certain amount. When both bottom switch on (top switch off), we get phase leg by certain amount. Right side and left side, top and bottom switch are tie together so they switched simultaneous and act like one switch, as shown in figure 2b. Switching is controller by applying 0v to turn it on, and -2V to turn it off and it is done digitally.

Once we connect the circuit for all the 3-bit, the final circuits looks like what's shown in figure 3 below. Each switch for each bit (lead or leg) is control by switch box, which switch it on (0V) or off (-2V). At any given time, there either phase Lead or leg part of the circuit is on but not both. That gives either +/- X amount of phase from each bit. When we combine three such phase bit, we get following 3-bit phase shifter circuit.

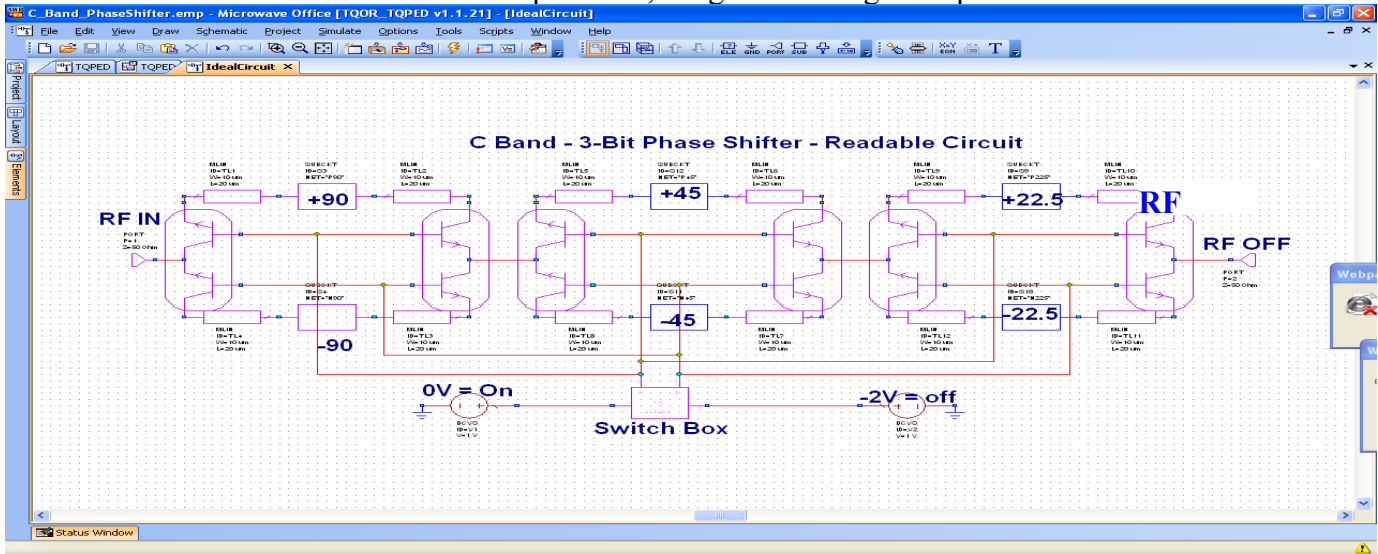


Figure 3. 3-bit Phase shifter switching circuit

Each of the phase bit are made of capacitor and/or inductor. Inductor leads the phase from capacitor. We have used pi network (series cap, shunt inductor and series cap) to get the lead part of the phase and another pi network (shunt cap, series inductor and shunt cap) to get the lag part the phase. Then each element are tuned until we got the desire phase of +/- 22.5, +/ 45, and +/- 90deg.

a. Specification vs. Goals

Criteria	Goal	Simulation Results
Frequency	5150 to 5875 MHz	5150 to 5875 MHz
Bandwidth	> 725 MHz	> 725 MHz
Insertion Loss	<6 dB min IL	< 11dB
Phase shift	Step 45, 90 and 180	Step 45, 90 and 180
VSWR, 50Ohm	<1.5:1 input & Output	<2:1 input & Output
Supply Voltage	0 to +3.3volts switch input	0v and -2V
Size	60 x60mil ANACHIP	60 x60mil ANACHIP

b. Tradeoffs

In designing 3-bit phase shifter, there are two main tradeoffs. One is number of fingers in D-FET (3 vs. 6). 3 finger FET gives you better isolation (-20dB) and less space, however, less current carrying capability. 6 fingers gives you more current carrying capability but worst isolation (-10dB) and requires more space. We use 3finger for our design approach. 2nd trade was in size of inductor. If we make inductor bigger, the separation between turn increase and give better insertion loss. However it requires more space, we have many inductors in our circuits. In our design, we kept size of inductor small to fit every thing in 60mil by 60mil circuits at cost of few more dB of

insertion loss. After fitting everything on layout, we notice that we had space to increase the size of inductor, but due to lack of time, were not able to do it

4. Simulations

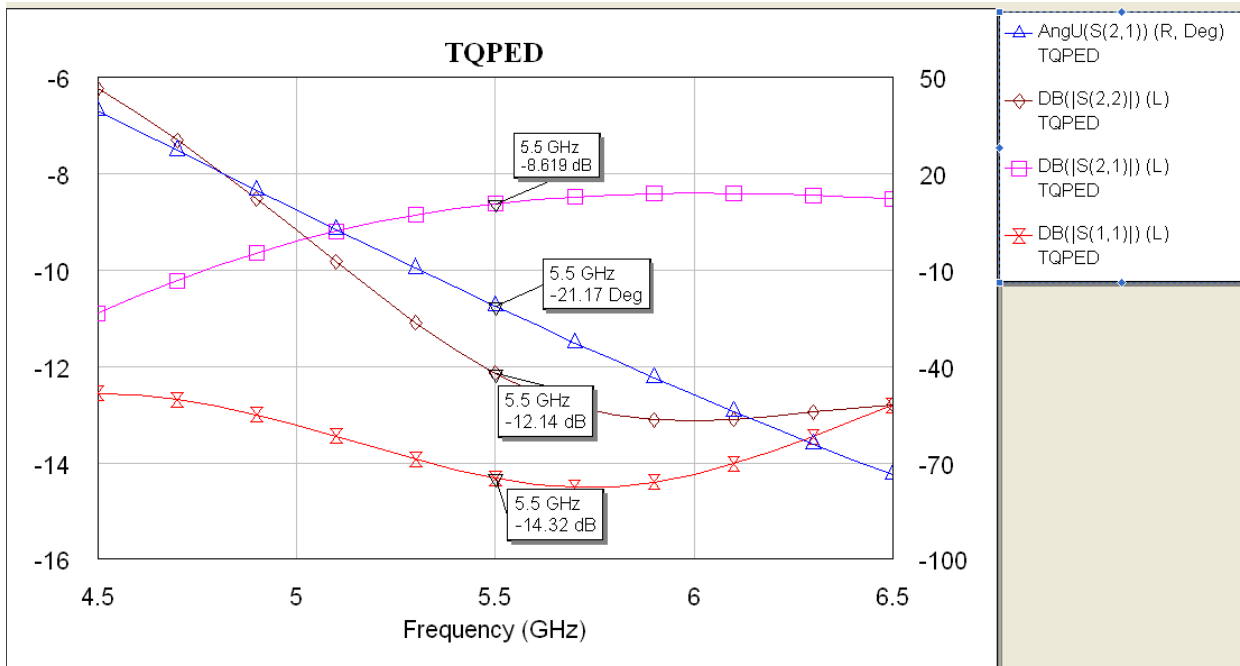


Figure 4: S-Parameter for -22.5deg Phase shifter

Figure 4 shows, S-parameter of -22.5deg when first bit is set to -90, second bit to +45 and last bit to +22.5, hence -22.5deg simulation results were obtained. Insertion loss of -8.6dB is expected since capacitor and inductor are lossy element.

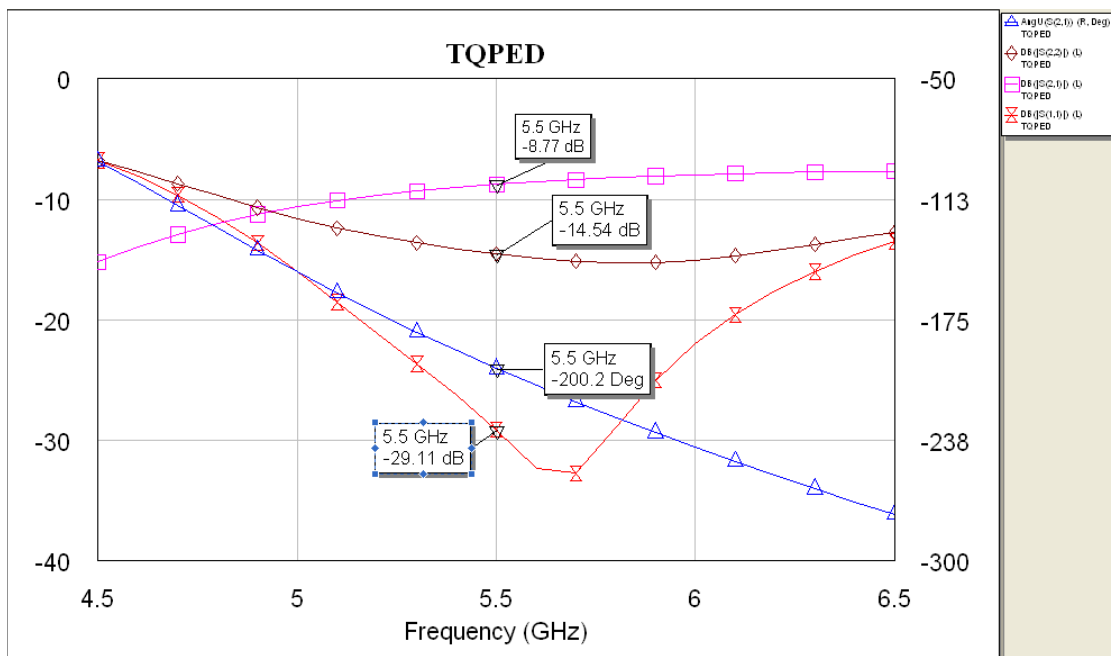


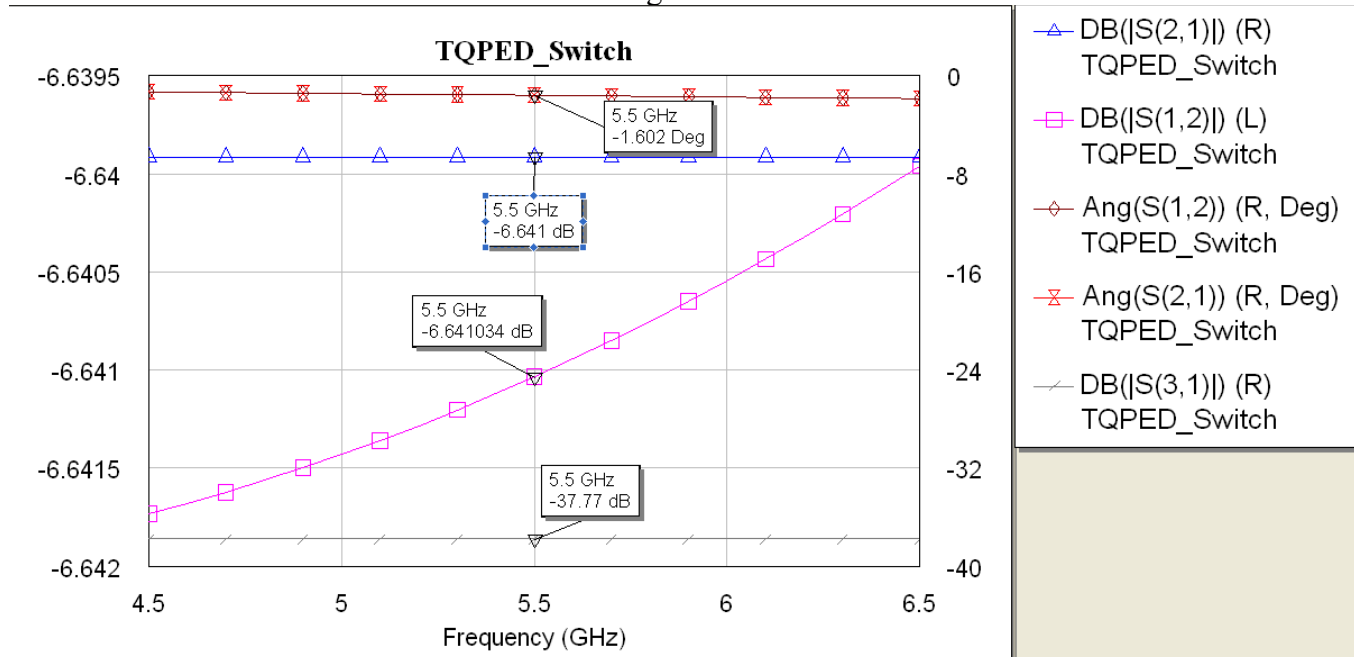
Figure 5: S-Parameter for 157.5deg Phase shifter

Figure 5 shows, the S-Parameter for 157.5 (-202.5+360 = 157.5) deg phase shift. This is achieved by setting 1st bit to +90, second bit to +45 and last bit to +22.5deg. Insertion loss of 8.77dB is expected out all three bit.

Similar to 157.5 and -22.5 deg simulation above, rest of the results were obtain and recorded below for all the combination of the 3-bit phase shifter (lead and leg)

Simulated Phase Results							
Each 3 bit individual Phase			Calculated Results		Simulated Results		
90	45	22.5	Absolute Phase(deg)	Relative phase(deg)	S21 Phase(deg)	S21(dB)	Delta Phase (deg)
1	1	1	157.5	315	159.8	-8.7775	2.3
1	1	-1	112.5	270	107	-9.57	5.5
1	-1	1	67.5	225	61.79	-11.23	5.71
1	-1	-1	22.5	180	22.61	-11.328	0.11
-1	1	1	-22.5	135	-21.17	-8.62	1.33
-1	1	-1	-67.5	90	-70.64	-9.07	3.14
-1	-1	1	-112.5	45	-116.5	-9.63	4
-1	-1	-1	-157.5	0	-158.4	-10.1	0.9
90deg bit equal 1 corresponds to +90 (0v Vgs), while -1 corresponds to -90 (-2vs Vgs)							
Absolute Phase Example --> $157.5 = 90*1 + 45*1 + 22.5*1$							
Relative Phase = Absolute Phase + 157.5							

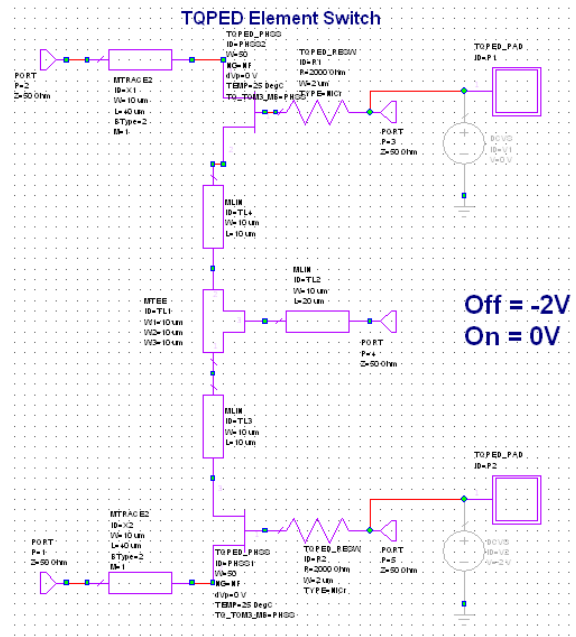
Similar to whole phase shifter circuit above, following figure shows S-Paramater for just single switch shown in figure 1.



For just single switch, insertion loss between RFIN 1 and RFOUT is -6.6dB, and phase offset of 1.6deg. Isolation between RFIN2 and Output is -37dB.

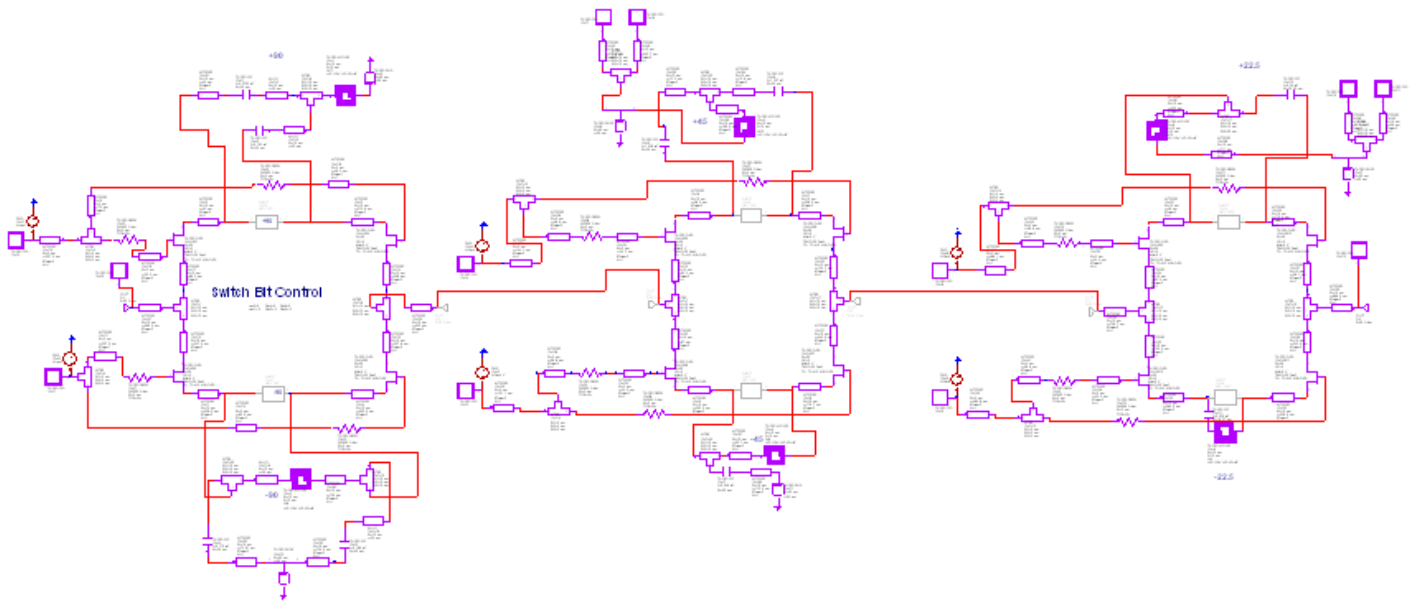
5. Schematic

a. Switch Schematic



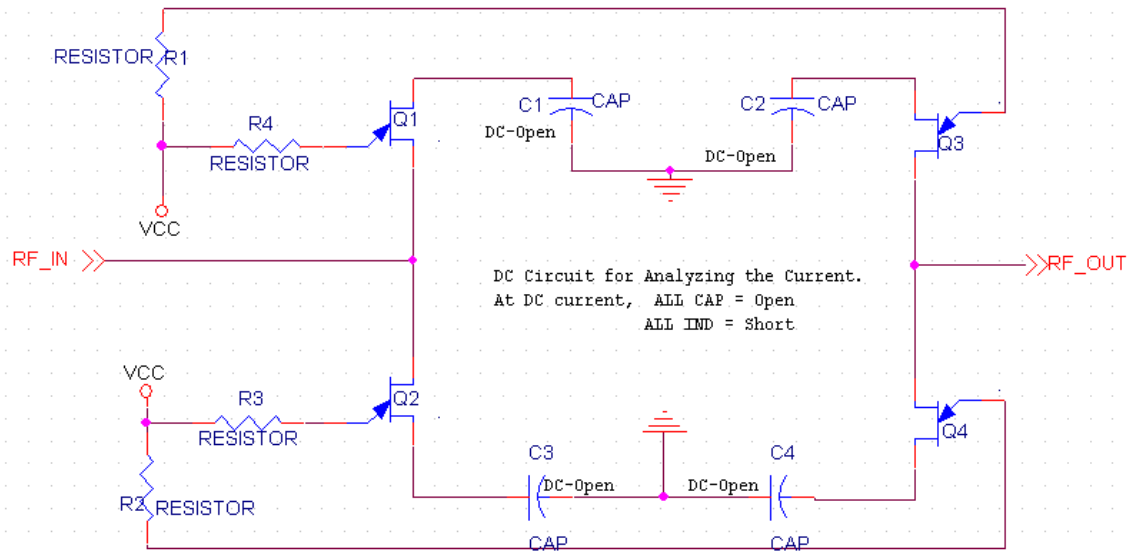
Schematic for the single switch

b. RF Schematic



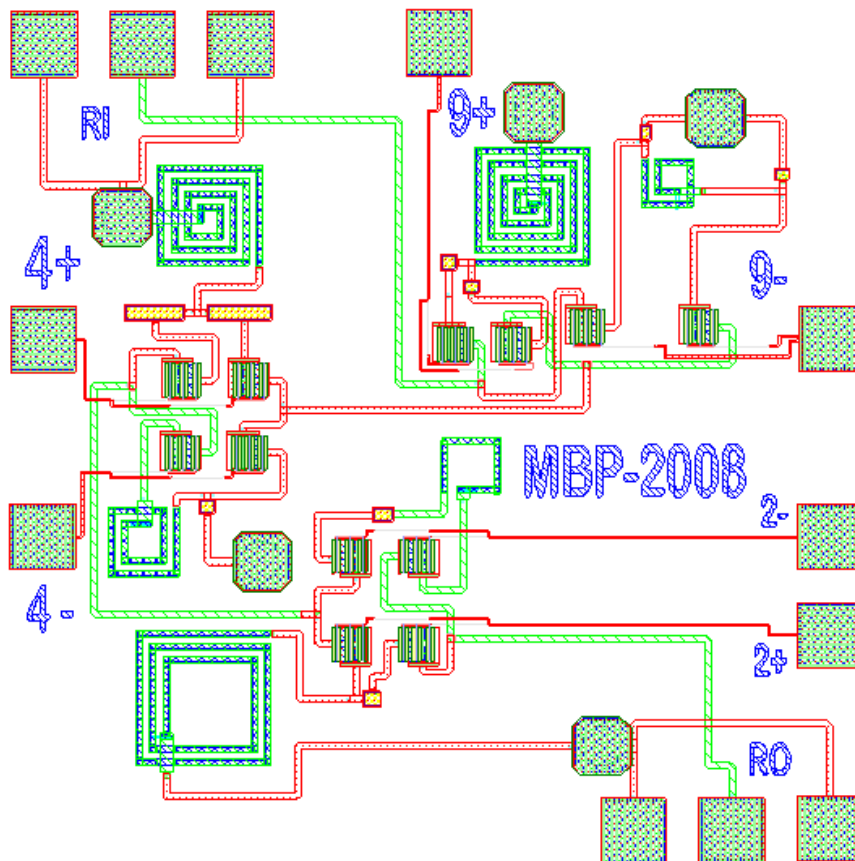
Above is final RF schedule for 3bit Phase shifter, which has all the switches and phase shift bit. Left circuit is 90deg bit, middle is 45deg bit, and at the end is 22.5deg bit. All the top part is for positive phase shift (lead), all the bottom corresponds to negative phase shifts (leg). To see detail of any phase shift bit, please refer to schematic in appendix.

c. DC Schematic



Above circuit shows DC current simulation of single bit. All Capacitor acts as open in DC, and all inductor (not shown) act as DC short.

6. Layout Plot



Above is layout for the final 3-bit phase shifter circuit. RF input is located at (RI) top-left handside with Ground-Signal-Ground pas. RF output (RO) is located in the bottom right hand side with Ground-Signal-Ground pads.

Rests of pads are for the switch, where we can apply, 0v or -2v to switch on/off. 0V turn on it, and -2V turn it off. 4+ reference to 45deg phase shifter bit. 9- reference to 90deg phase shifter bit, and 2+ reference to 22.5deg phase shifter bit.

7. Test Plan

- Calibrate the network work analyzer for 4.5 to 6.5GHz in 10Mhz step. Place marker at 5.15 GHz, 5.5 GHz and 5.875 GHz.
- Apply 0V or -2V to all pads labeled (4+, 4-, 9-, 9+, 2-, or 2+)
- Connected GSG probe from Network analyzer port 1 to RF input pads label 'RI'.
- Connect GSG probe from Network analyzer port 2 to RF Output pads label 'RO'.
- Measured Phase and magnitude of S21 and record it on table above
- Switch the voltage to next configuration on table below and re-measured the phase and magnitude
- When done measuring, disconnect, turn off all the equipment.
- Finally compare measured results verse simulation.

Measured vs. Simulated Results Comparison							
Each 3 bit voltage			Measured results		Simulated Results		
90 (9+/-)	45 (4+/-)	22.5 (2+/-)	Absolute Phase(deg)	Absolute Magnitude(dB)	S21 Phase(deg)	S21(dB)	Delta Phase (deg)
0V	0V	0V			159.8	-8.7775	
0V	0V	-2V			107	-9.57	
0V	-2V	0V			61.79	-11.23	
0V	-2V	-2V			22.61	-11.328	
-2V	0V	0V			-21.17	-8.62	
-2V	0V	-2V			-70.64	-9.07	
-2V	-2V	0V			-116.5	-9.63	
-2V	-2V	-2V			-158.4	-10.1	

8. Summary & Conclusions

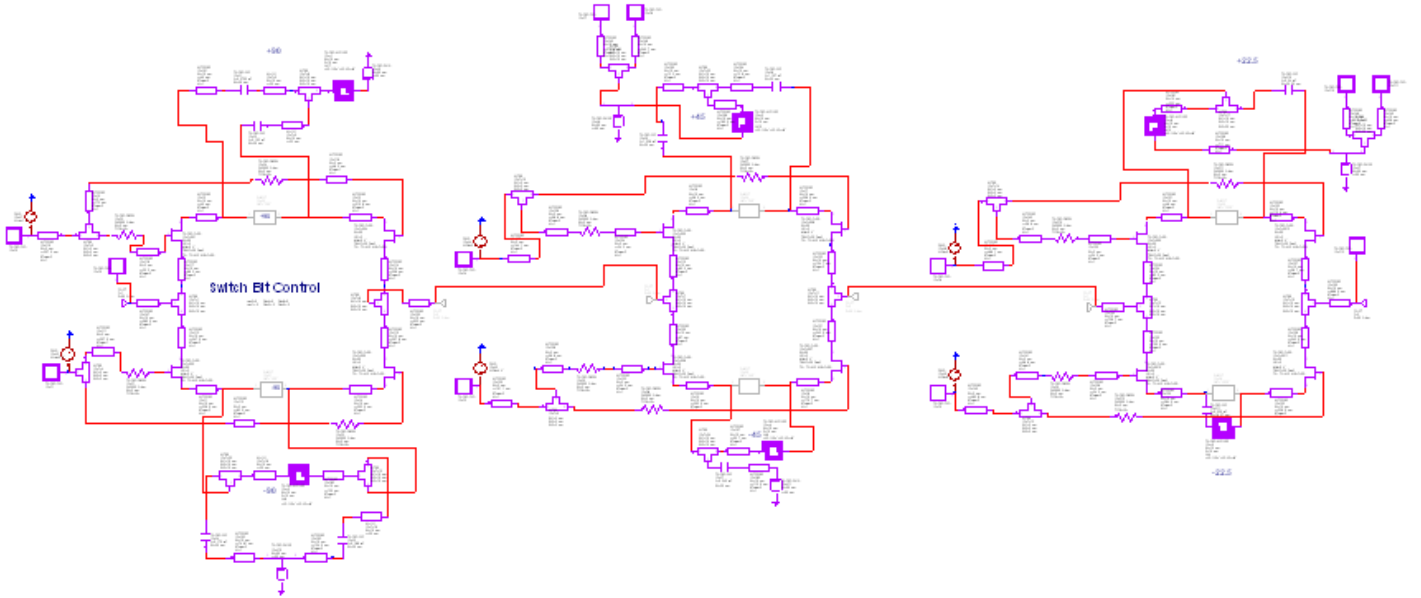
The C-band phase shifter was designed very close to specification. As seen in table 1, phase shift accuracy exceeded specification requirement (worst case of 5deg off from target). All three bits were fitted in 60mil by 60mil layout. Insertion loss in this design was exceeding the requirement value because of smaller inductor size use and too many transmission lines instead of using single line with routing tool.

With more time, following can be improve in this design

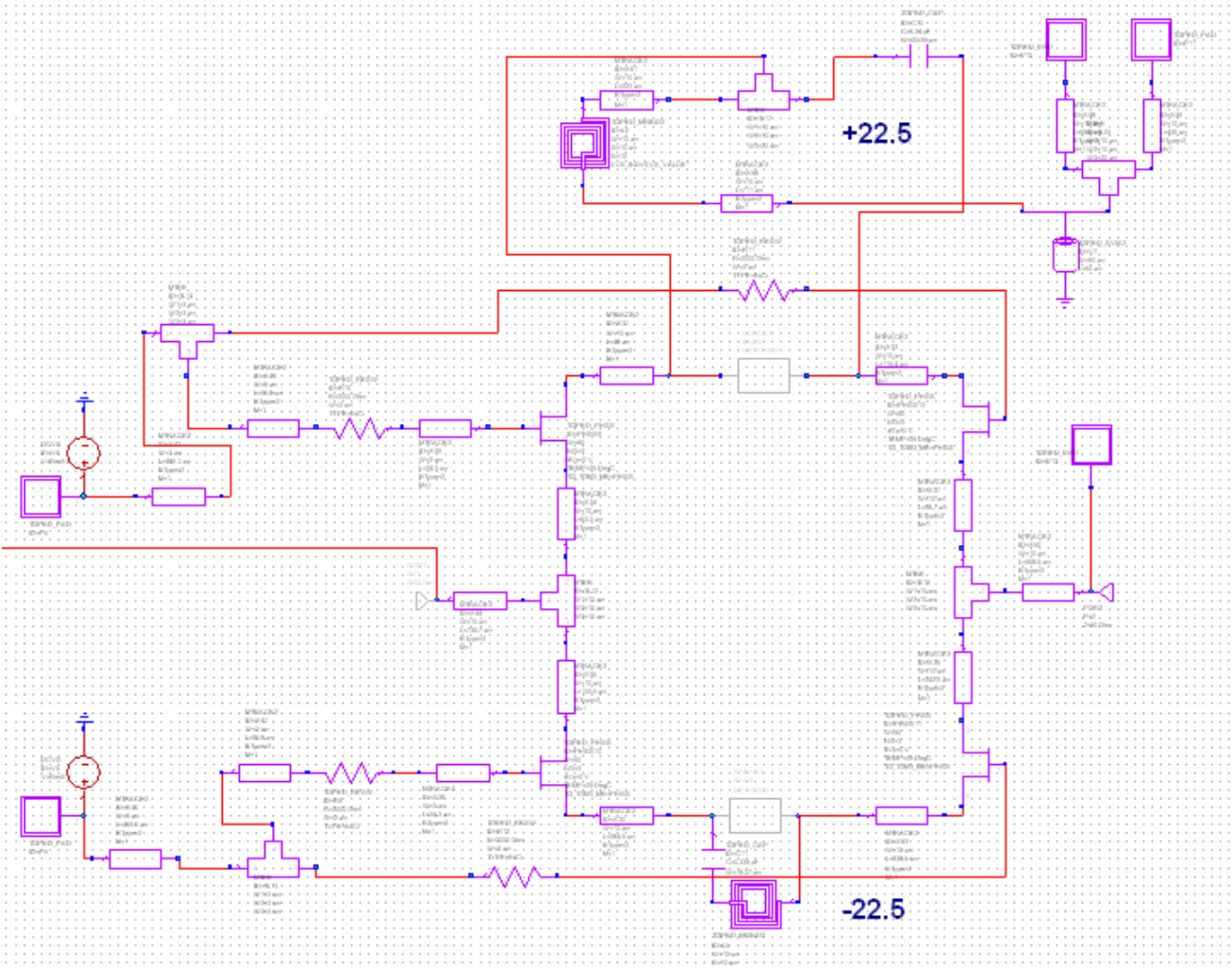
- Add circuit to use +3.3 and 0v for source switching control
- Try to reduce the insertion loss by
 - Make all the inductor little bigger and retune each
 - Avoid series component as much as possible
- Look into the possibility of using E-mode transistor for any improvement
- Simulate RF structures in a EM simulator to find out unwanted coupling or interaction between parts.

Appendix A

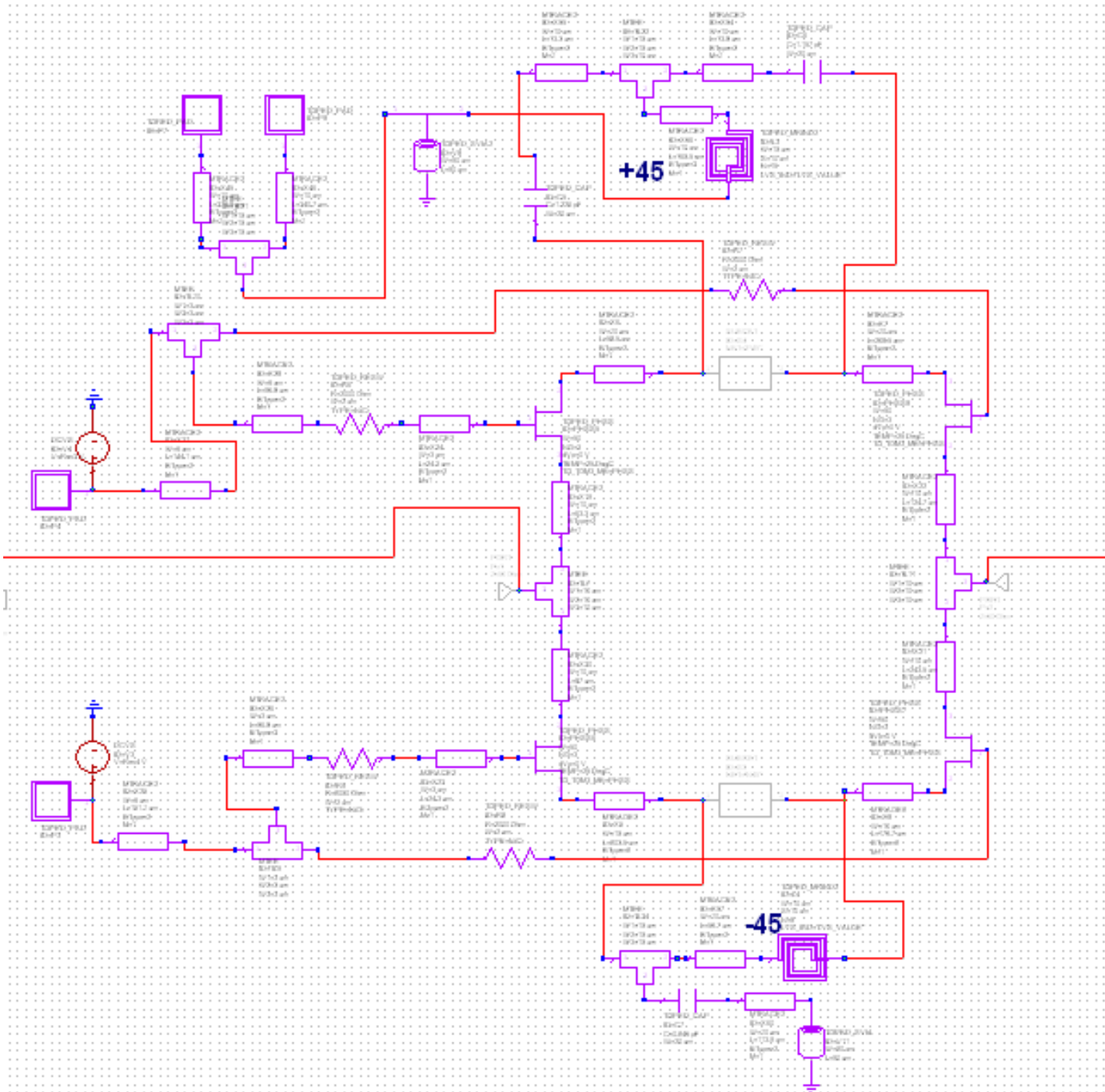
a. Final RF Schematic & Results



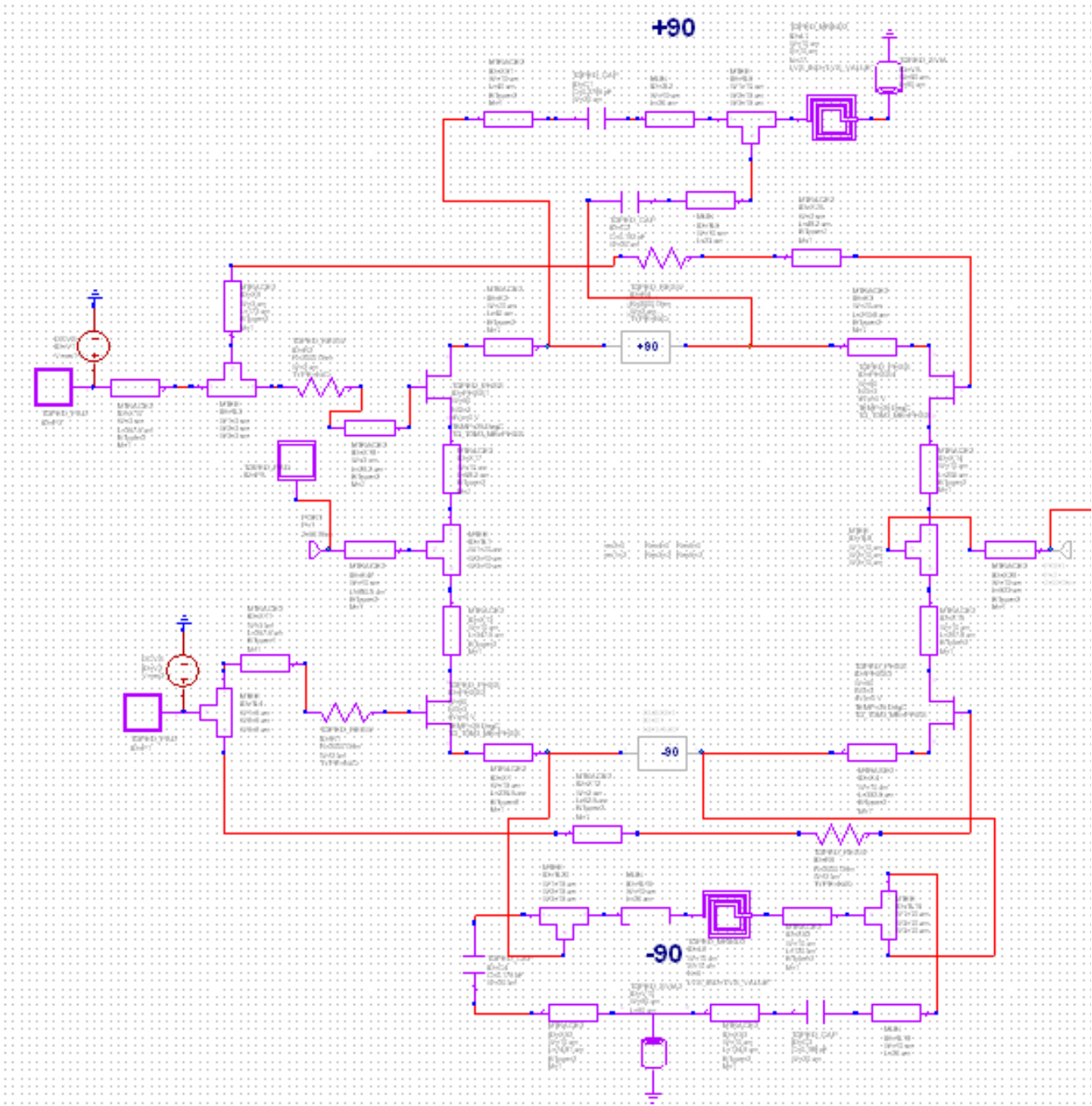
Above is final RF schedule for 3bit Phase shifter. Left circuit is 90deg bit, middle is 45deg bit, and at the end is 22.5deg bit. All the top part is for positive phase shift, all the bottom corresponds to negative phase shifts. Detail of each 3 bits circuit is given below.



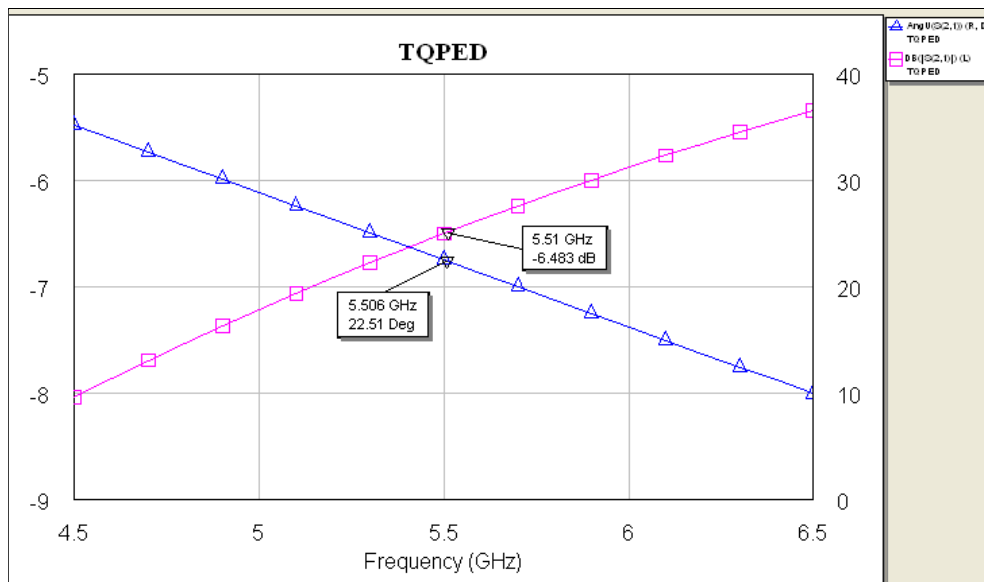
Circuit for 22.5deg phase shift. Top loop corresponds to Positive phase shift, while bottom loop corresponds to negative phase shift.



Circuit for 45deg phase shift. Top loop corresponds to Positive phase shift, while bottom loop corresponds to negative phase shift.

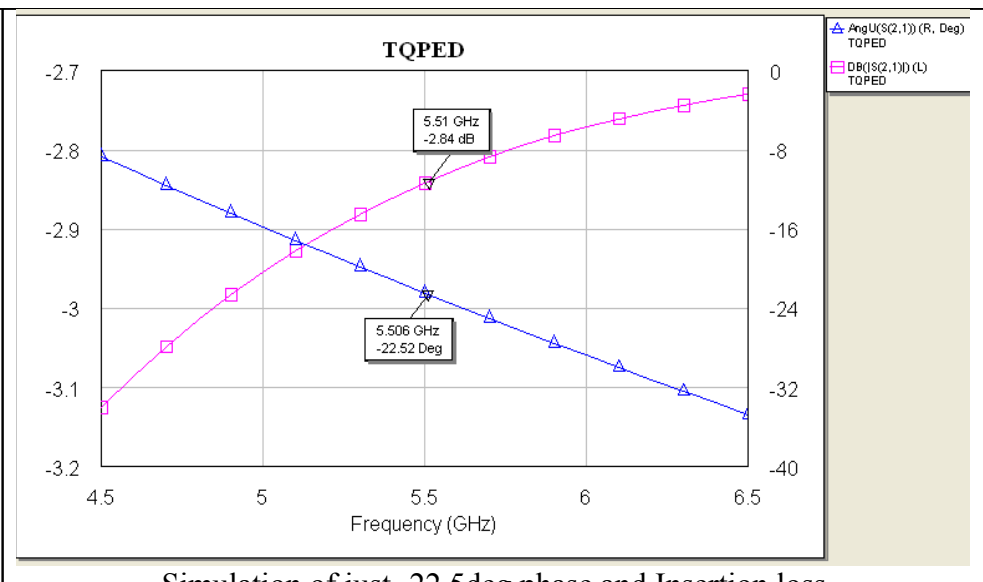


Circuit for 90deg phase shifter. Top loop corresponds to Positive phase shift, while bottom loop corresponds to negative phase shift.

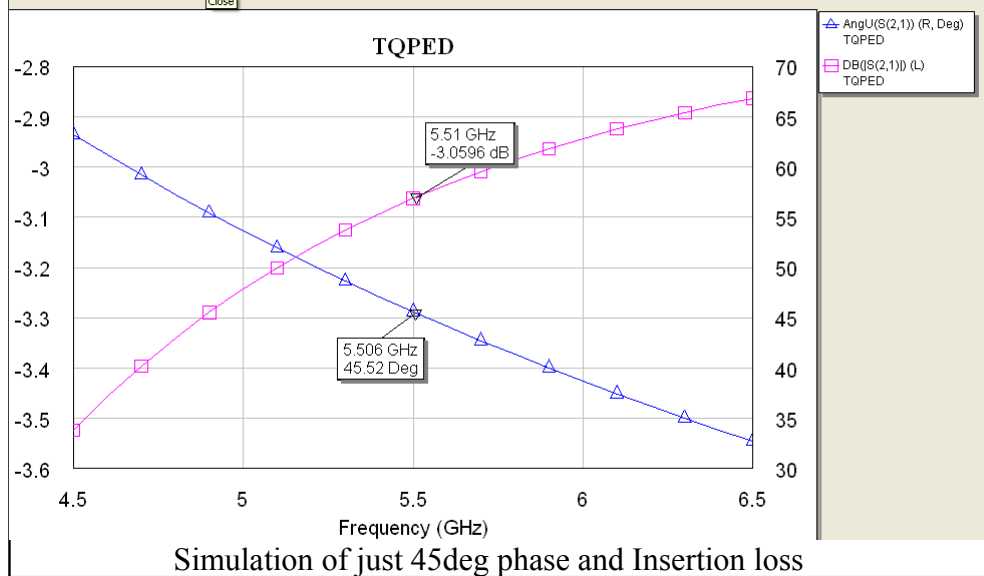


Simulation of just 22.5deg phase and Insertion loss

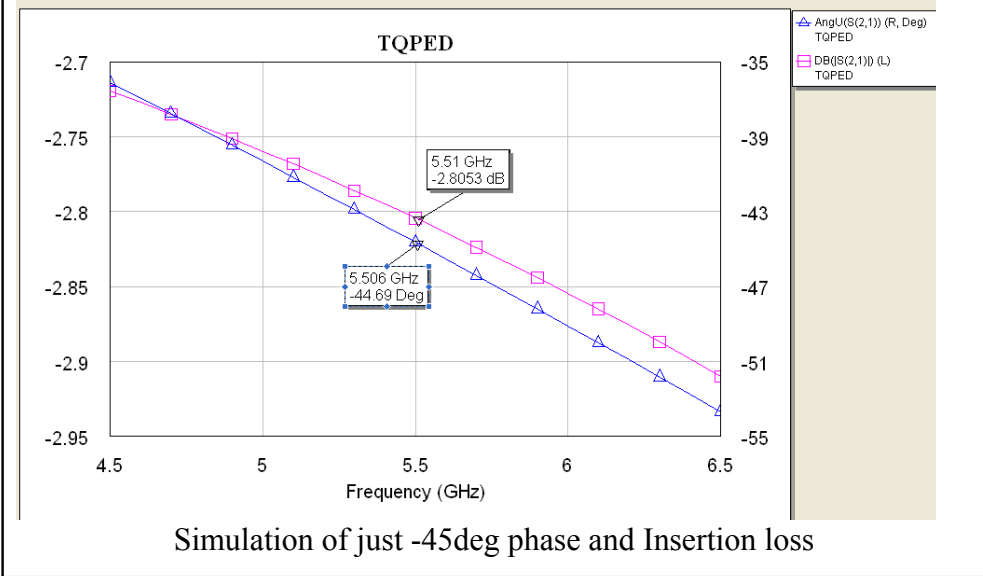
+45deg



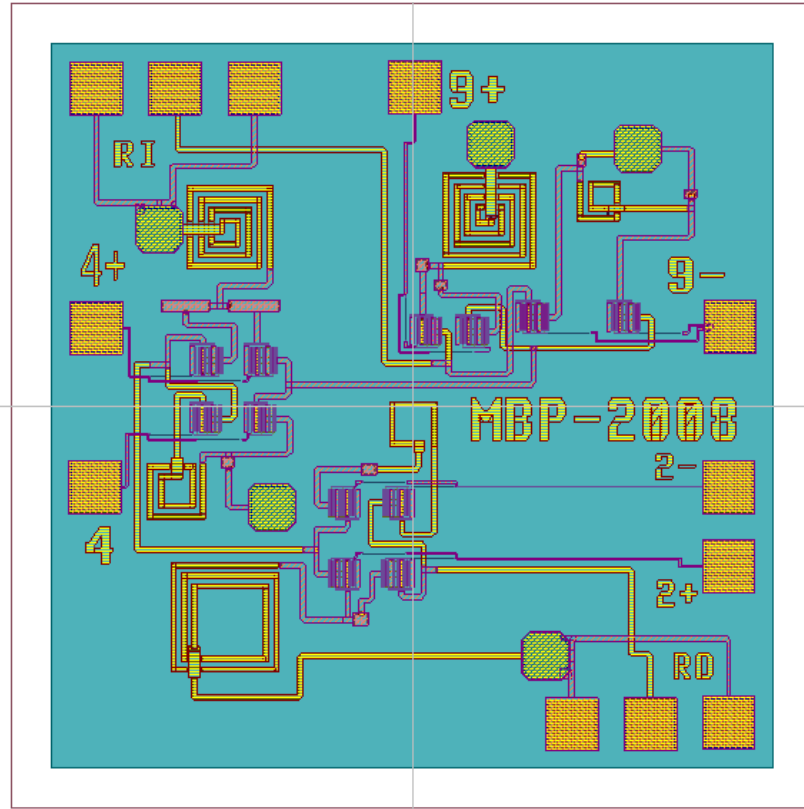
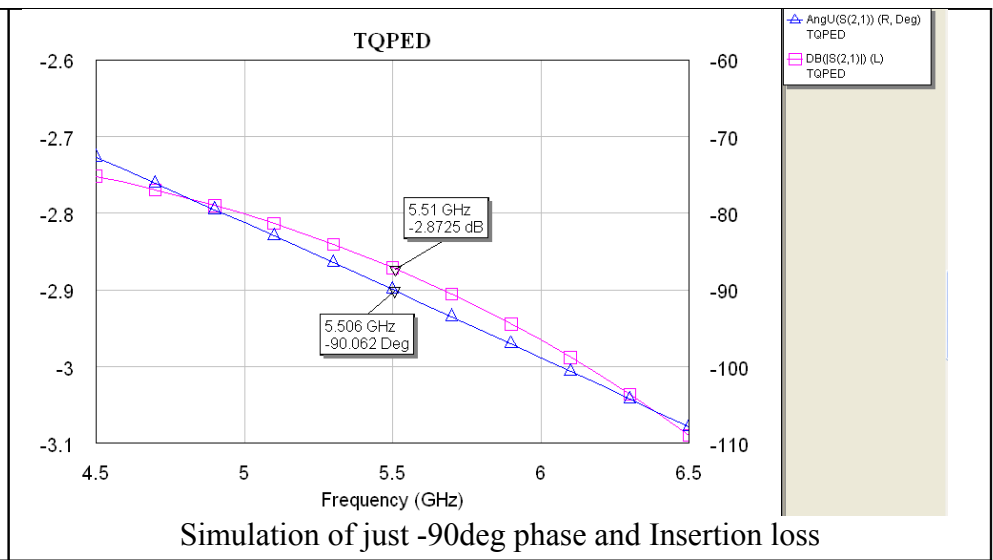
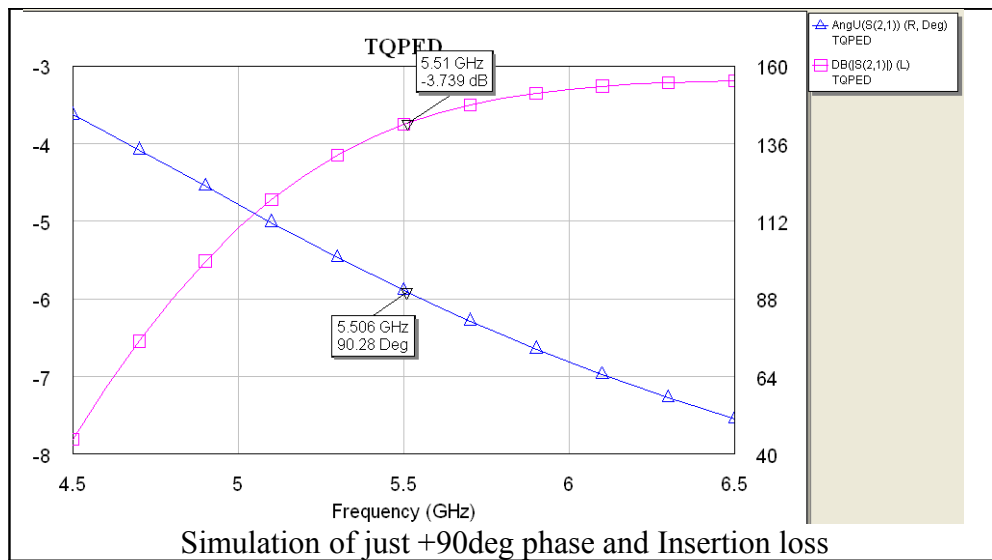
Simulation of just -22.5deg phase and Insertion loss



Simulation of just 45deg phase and Insertion loss



Simulation of just -45deg phase and Insertion loss



Different view of the layout Chip
Page 15 of 15

S-Band Up/Down Mixer

EE 525.787 – MMIC Design

Fall 2008

Prepared by: Brendan McElrone

Abstract

The following report details a monolithic microwave integrated circuit (MMIC) S-Band up/down mixer design. The mixer was designed for a radio frequency (RF) input range of 2.3 – 2.5 GHz. The local oscillator (LO) design frequencies range from 2.2 – 2.6 GHz with an up/down-converted intermediate frequency (IF) of 100 MHz. Based off a rat-race coupler design, the s-band mixer incorporates TriQuint modeled PHEMT transistors as switching diodes. Design simulations verified acceptable results: conversion loss less than 9 dB, RF/LO isolation greater than 20 dB, voltage standing wave ratio (VSWR) better than 2.5:1. The mixer meets all design requirements at an LO power of +4dBm with optimal performance at +7dBm.

1 Introduction

With intentions of creating a configurable S-band duplex transceiver, an up/down mixer was designed to cover the wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies. The up/down mixer incorporates a 180° lumped element rat-race coupler with diode configured transistors. An ideal lumped element model of the design is shown in Figure 1.

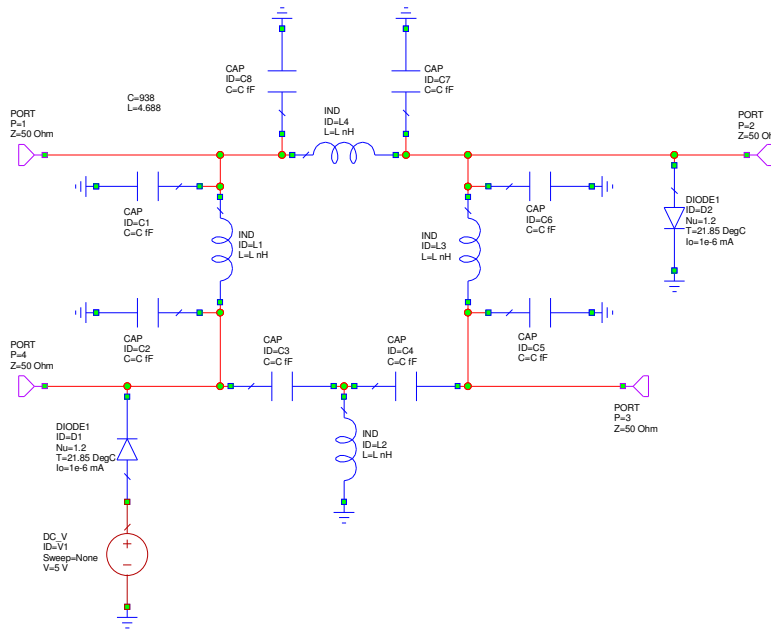


Figure 1: Ideal lumped element S-band up/down mixer

The mixer RF frequencies range from 2.3 – 2.5 GHz and the LO frequencies range from 2.2 – 2.6 GHz. The design targeted a maximum LO power of +7dBm with simulations showing a functional design at +4dBm. Simulations demonstrate conversion loss approximately 8dB, RF/LO isolation approximately 25dB, and a VSWR ranging from

1.2:1 – 2.3:1. A layout file was designed around a 60x60mil TriQuint anachip. Tradeoffs were made between layout size and circuit design for optimal performance characteristics.

2 Design Approach

As a subsystem of a configurable duplex transceiver, requirements must be specified prior to design implementation. Table 1 outlines these requirements.

Table 1: S-band up/down mixer design requirements

Mixer Property	Minimum Requirement	Design Goal
RF frequency	2.305 – 2.497 GHz	2.3 – 2.5 GHz
LO frequency	2.205 – 2.397 GHz	2.2 – 2.6 GHz
IF frequency	100 MHz	100 MHz
Isolation (RF/LO)	10 dB	16 dB
LO power	+7 dBm	0 dBm
VSWR	2.5:1	1.5:1
Conversion Loss	10 dB	7 dB

Several design steps were taken in order to effectively design a mixer meeting all of the predefined requirements. An ideal model of the rat-race coupler was designed followed by a TriQuint element based design. Upon optimizing the coupler, the diode configured PHEMT devices were incorporated into both the ideal and non-ideal models.

Optimization was performed on the switching diode mixer designs. A layout file was then created and a final optimization was performed through layout property extraction. These steps are detailed in the following sections.

2.1 Rat-race Coupler Design

The 180° rat-race coupler was designed with both ideal and non-ideal components. In order to optimize the coupler, an equivalent power split between the coupling ports is desired. Additionally, theoretical phase requirements are desired. Figure 2 shows the non-ideal model with optimized coupled power. The non-ideal phase measurements were within the desired range.

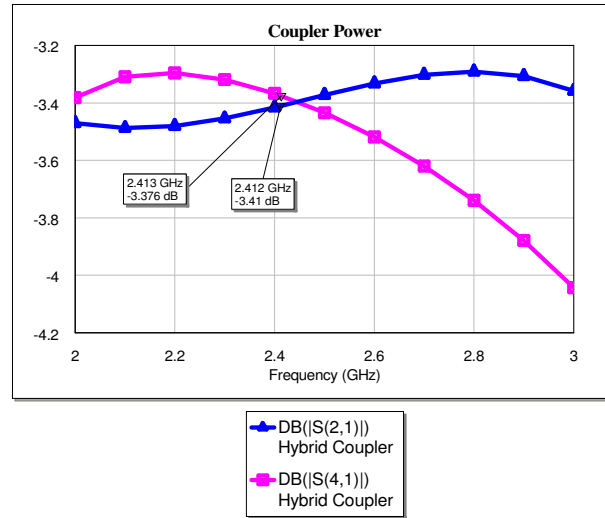
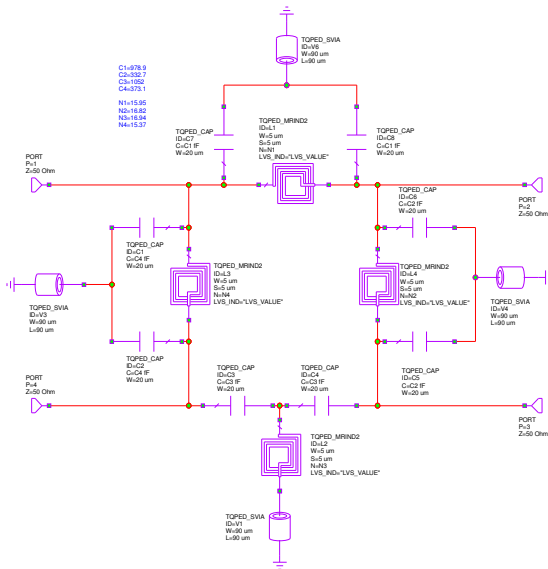


Figure 2: Non-ideal rat-race coupler (left), non-ideal coupled power (right)

2.2 PHEMT Diode Configuration

The TriQuint PHEMT devices were optimized to reduce the effect on the rat-race coupler when incorporated into the design. In order to function as a diode, the PHEMT drain and source terminals were connected and acted as the diode cathode. The gate terminal was used as the anode. Ideally, the diode should look like a 50 ohm terminal when introduced into the coupler. In order to simplify the design, PHEMT width dimensions and finger count of 50 μm and 2 respectively were used. Without implementing a diode matching network, these dimensions control optimization of the diode match. A direct current (DC) bias voltage source was used to reduce the overall LO drive power needed to turn the diodes on and off. The 0.7V bias was optimized in the final design.

2.3 Mixer Design

The diode configured PHEMT devices were incorporated into the coupler design to create the up/down mixer configuration. One diode was placed from coupler port 4 (anode) to ground (cathode). The other diode was configured from DC bias (anode) to coupler port 2 (cathode).

The initial mixer design approach was geared toward isolation optimization. S-parameters of the mixer were optimized during this process. Final design configurations were tuned to meet all requirements. Figure 3 shows the optimized S-parameters.

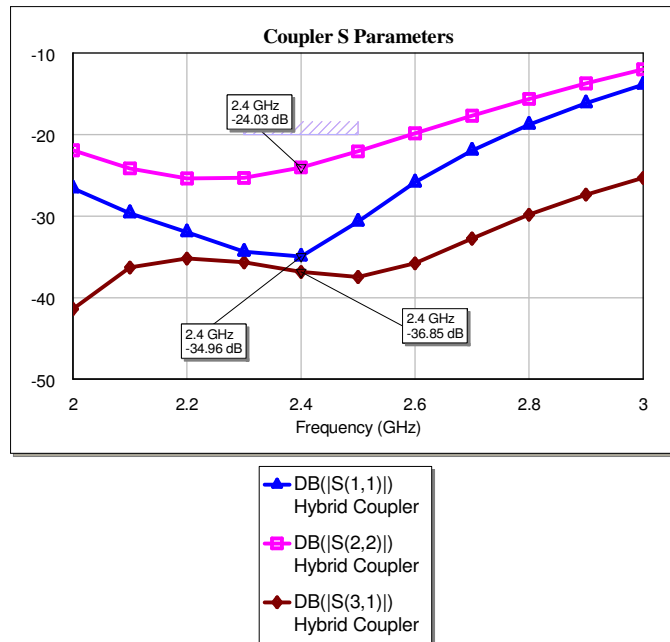


Figure 3: Optimized S-band mixer s-parameters.

2.3.1 RF/LO/IF Isolation

With an ideal coupler based mixer design, the IF port can be inserted into the design in several configurations yet have no effect on performance. In order to do this, a large series inductor was used between the IF port and the other mixer circuitry.

In order to isolate the DC bias from the RF and LO ports, large series blocking capacitors were inserted between the RF/LO ports and the other circuitry.

2.4 Trade-offs

Many of the design trade-offs were a result of the 60x60mil area constraint. The RF/LO blocking capacitors were optimized for performance yet limited to reduce area consumption. Similarly, the inductor dimensions were limited.

Another trade-off involved the PHEMT diode circuitry. Introducing diode matching networks would enhance the performance of the mixer. Due to area constraints, the matching circuitry was left out of the design and the transistor dimension optimization was used to best match the device.

3 Simulations

A summary of the simulated results are shown in Table 2.

Table 2: Simulated results summary

Mixer Property	Simulated Results	Minimum Requirement
Isolation (RF/LO)	> 25 dB	10 dB
LO power	+4 dBm	+7 dBm
VSWR	1.2:1 – 2.3:1	2.5:1
Conversion Loss	~ 8 dB	10 dB

3.1 Conversion Loss

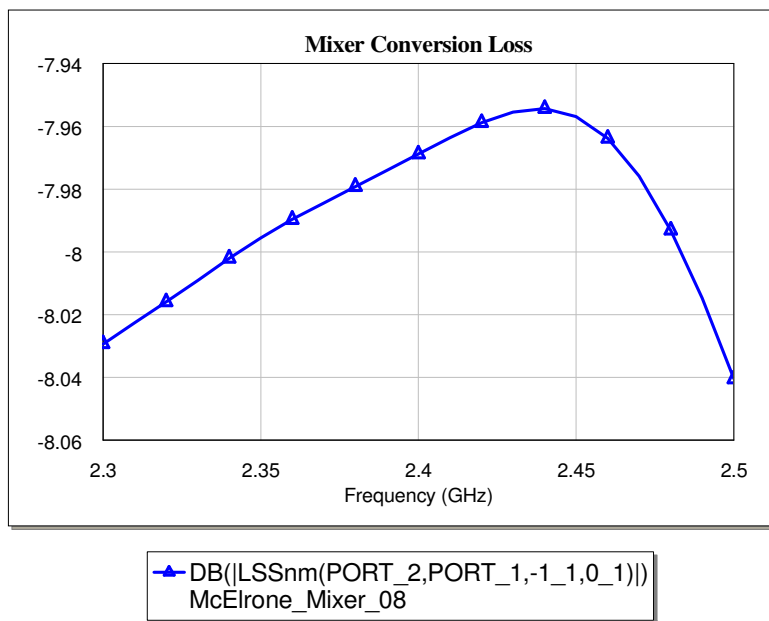


Figure 4: S-band up/down mixer conversion loss

3.2 RF/LO Isolation

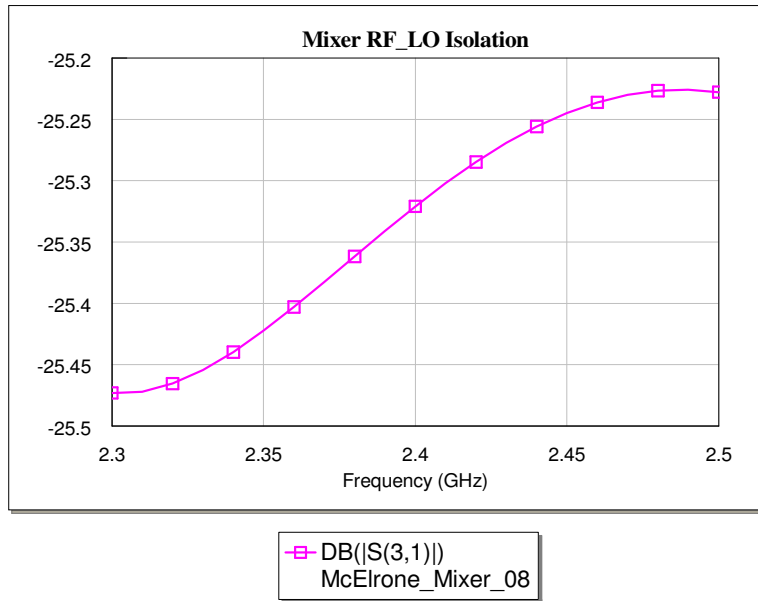


Figure 5: S-band up/down mixer RF/LO isolation

3.3 VSWR

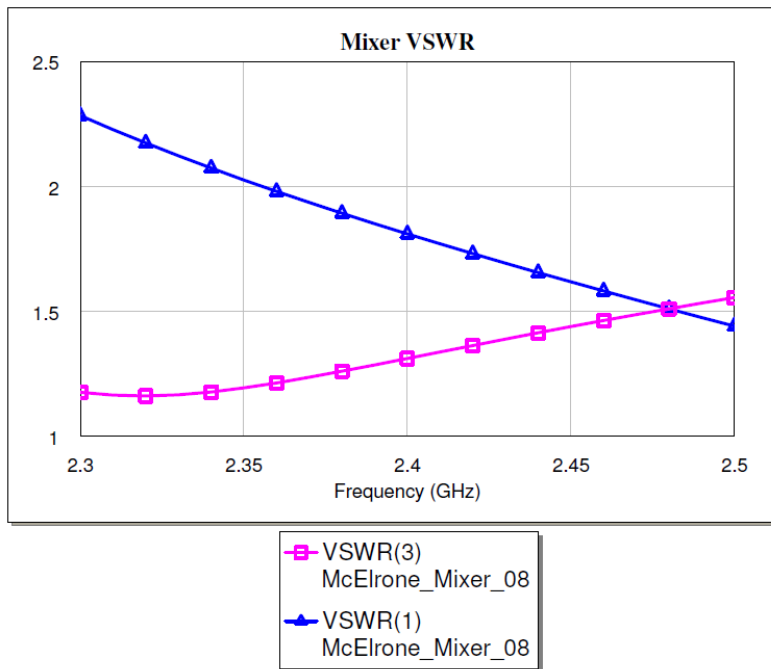


Figure 6: S-band up/down mixer VSWR

3.4 IF Spectral Analysis

3.4.1 Up Mixer

3.4.1.1 High Band

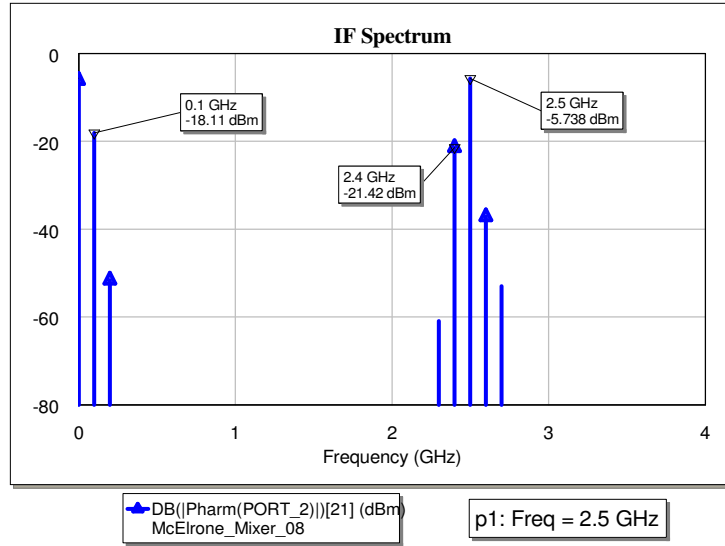


Figure 7: IF spectrum, mixer in high band of up mixer mode

3.4.1.2 Low Band

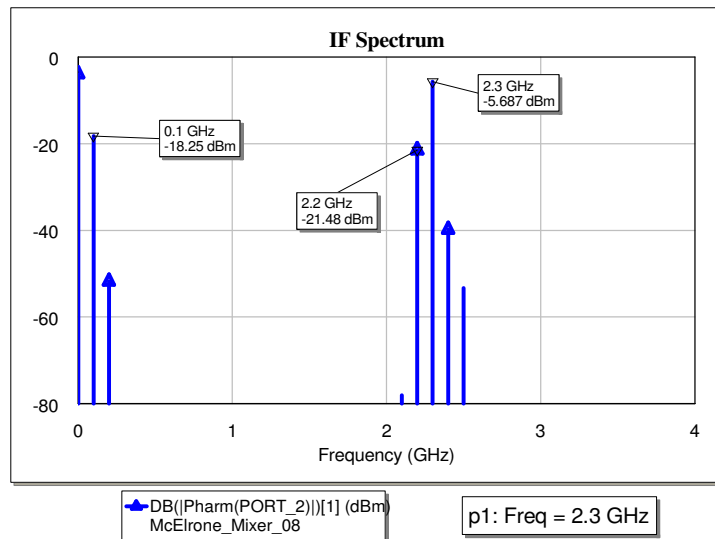


Figure 8: IF spectrum, mixer in low band of up mixer mode

3.4.2 Down Mixer

3.4.2.1 High Band

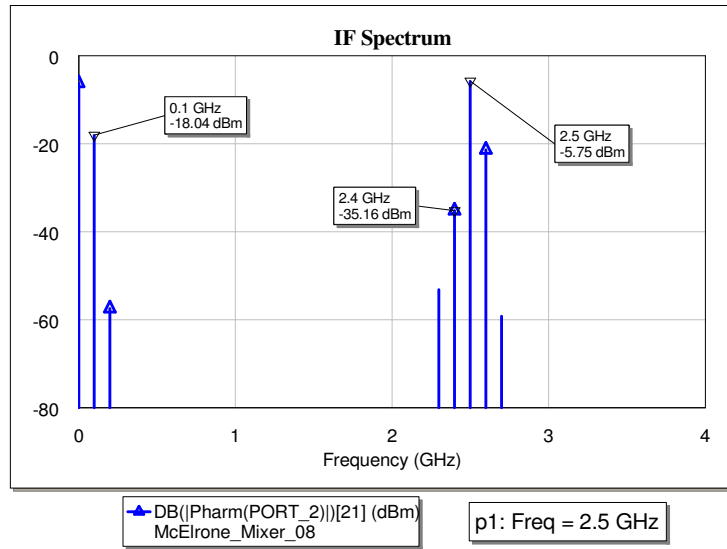


Figure 9: IF spectrum, mixer in high band of down mixer mode

3.4.2.2 Low Band

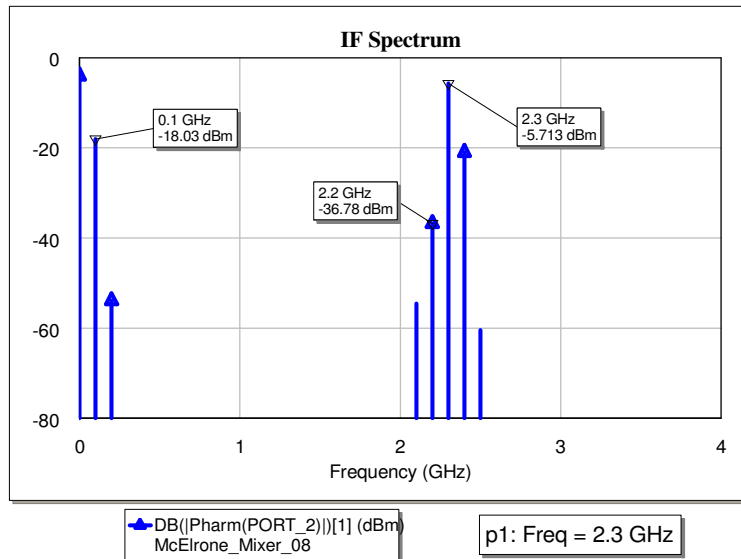


Figure 10: IF spectrum, mixer in low band of down mixer mode

5 Layout

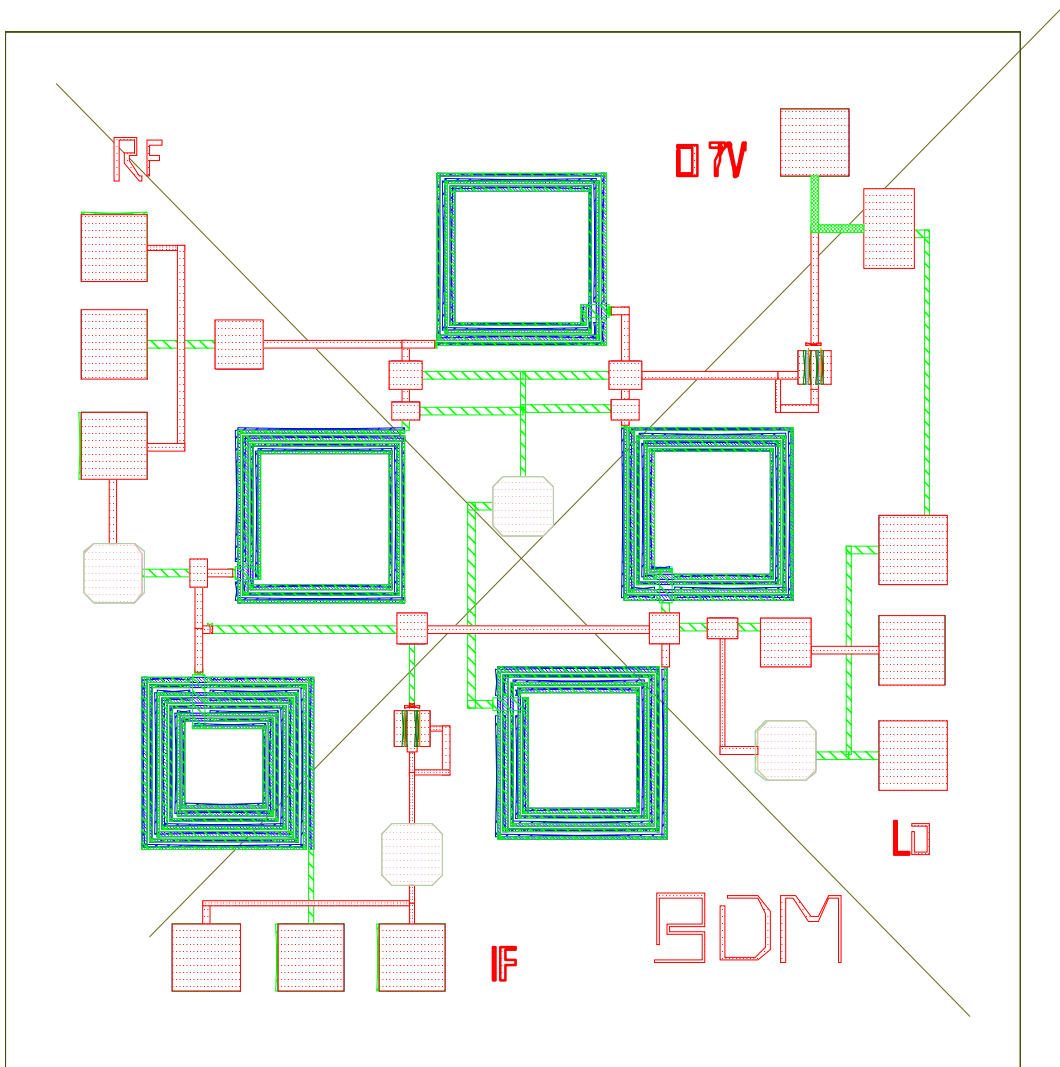


Figure 12: S-band up/down mixer layout

6 Test Plan

6.1 S-parameter Testing

1. Connect network analyzer to the appropriate ports. Use RF as port 1 and LO as port 2. Setup to sweep from 2.3 – 2.5GHz.
2. Terminate IF port into a 50 ohm load
3. Apply 0.7Vdc to the DC bias terminal
4. Measure the s-parameters

6.2 Up Mixer Testing

1. Connect a signal generator to the LO port. Setup to sweep from 2.2 – 2.4 GHz in 0.05GHz increments. Set power output to +7dBm.
2. Connect a signal generator to the IF port. Set the frequency to 100MHz. Set power output to -10dBm.
3. Connect a spectrum analyzer to the RF port
4. Apply 0.7Vdc to the DC bias terminal
5. Measure RF output power at each LO frequency

6.3 Down Mixer Testing

1. Connect a signal generator to the LO port. Setup to sweep from 2.2 – 2.6 GHz in 0.05GHz increments. Set power output to +7dBm.
2. Connect a signal generator to the RF port. Setup to sweep from 2.3 – 2.5 GHz in 0.05GHz increments. Set power output to -10dBm.
3. Note: Keep the RF and LO signals consistent with a 100MHz IF output signal
4. Connect a spectrum analyzer to the IF port
5. Apply 0.7Vdc to the DC bias terminal
6. Measure the 100MHz IF output power at each frequency interval

7 Summary and Conclusions

As detailed in the document, the S-band up/down mixer met all design requirements. Optimizing the rat-race coupler circuitry was beneficial to the overall performance of the mixer. The design was successfully optimized for the area constraint. With the addition of diode matching networks, the mixer performance could be further optimized. The DC bias source effectively reduced the LO input power requirement.

A 3.3V, C-Band GaAs MMIC Two-Stage Single-Ended Power Amplifier

by

Benjamin Brawley

A Design Project submitted in fulfillment
of the requirements for

EE 787 MMIC Design

JOHNS HOPKINS UNIVERSITY

December 8, 2008

ABSTRACT

Abstract — This paper presents a 3.3V, 0.5 μ m pHEMT on 100 μ m gallium arsenide (GaAs) power amplifier operating across the 5150-5875MHz frequency range. Using a two-stage single-ended configuration with on-chip input/output matching networks, the designed amplifier provides a power gain of 20dB in conjunction with a 1dB compression level of -9dBm. A reverse isolation of greater than 30dB and DC power consumption of less than 43mW were achieved. A feedback resistor is utilized to eliminate potential stability problems in addition to a large capacitor on the bias voltages. The ideal elements are replaced with the foundry library elements and a layout is generated in preparation for fabrication. A test plan is detailed for measuring the design for comparison to the simulated performance.

Keywords — MMIC, Power Amplifier, Single-Ended

1. INTRODUCTION

Modern RF and microwave transmitter designs utilize integrated circuit (IC) power amplifiers (PA) that directly interface to the radiating element of an antenna to provide maximum RF power output and efficiency. The goal of this PA design is efficiency – to get the most RF output power for a given DC power consumption. Utilization of a single voltage supply, such as a 3.3V coin cell battery, is required. The specifications for the PA design are as follows:

- (i) On chip drain and gate bias network
- (ii) On chip input and output matching networks
- (iii) FET size tuned for efficient power operation with good input & output VSWR
- (iv) Frequency: 5150 to 5875 MHz
- (v) Bandwidth: > 800MHz
- (vi) Gain, small signal: > 20dB
- (vii) Gain ripple: ± 1 dB goal
- (viii) Output power: TBD @ 20-25% PAE (Power Added Efficiency)
- (ix) Supply voltage: +3.3V only, goal (3.0 to 3.6V range)
- (x) VSWR, 50 Ω : < 1.5:1 input & output
- (xi) Size: 60 x 60 mil ANACHIP

This paper details the design of a C-band, two-stage singled-ended configuration PA fabricated in TriQuint TQPED GaAs process centered at 5.5GHz. This design exhibits a gain of 20dB, an input and output VSWR of less than 1.25:1, a reverse isolation greater than 30dB, a 1dB compression (P_{1dB}) of -9dBm, and requires less than 43mW of DC power, all packaged within less than a 60mil x 60mil footprint.

2. DESIGN APPROACH

Several topologies exist for PA circuits, with the single-ended topology being one of them. In a single-ended design, the RF input signal is applied to the gate while the amplifier RF output signal is extracted from the drain. Any stabilizing resistors must be implemented on the input of the transistor so the power loss across the resistors does not decrease the amount of output power. An ideal PA would have a high compression point, high efficiency, and high gain. Maximum output power occurs when the input impedance of the output matching network equals the conjugate match of the drain impedance for a specified Cripps impedance value.

To increase the gain of a single-stage amplifier, a second transistor can be configured in cascade. With the addition of another active component, comes additional gain and power consumption. It is important to optimize the driver amplifier stage for high efficiency so the overall PA efficiency remains high.

3. SIMULATION SOFTWARE PACKAGE AND FOUNDRY

3.1 SIMULATION SOFTWARE PACKAGE

Applied Wave Research, Inc (AWR) Design Environment Version 8.02 was used as the simulation software package for this project. The AWR Design Environment (AWRDE) suite is comprised of several software packages, including Analog Office (AO), which was utilized for the MMIC design of the PA. Linear and nonlinear circuit simulations were used to analyze the performance of the PA, while the tuning and optimization capabilities were exploited to finalize the design. Elements in the TQPED process library from TriQuint Semiconductor were used to create a final design that accounts for parasitics in the non-ideal components.

3.2 FOUNDRY

TriQuint Semiconductor is an independent semiconductor wafer foundry with capabilities of MMIC wafer processing. The TriQuint TQPED 0.5 μ m pHEMT process is ideal for switches, low-noise amplifiers, power amplifiers, and integrated transceivers. This particular process has D-mode and E-mode transistors, metal-insulator-metal (MIM) capacitors, spiral inductors, thin film resistors, and three metal interconnect layers. Using proprietary libraries developed by TriQuint Semiconductor that model the TQPED process and are compatible with AWRDE, more realistic simulations were performed and analyzed in the development of the PA.

4. DESIGN AND CIRCUIT SIMULATIONS

This section details the design of the PA, starting with the transistor model supplied by TriQuint based on the TQPED process, followed by the stabilization circuitry, transistor biasing, and matching network (input and output) designs.

4.1 TRANSISTOR DEVICE – BIAS POINT AND CRIPPS ANALYSIS

The active element used in this amplifier design is an E-mode pHEMT transistor. This particular transistor is a commercially available GaAs process from TriQuint Semiconductor. The exact transistor model used in the TQPED 1.1.21 library was the TQPED_EHSS_T3, which is an adjustable-length 0.5 μm transistor. A width of 15 μm and a gate finger value of four were chosen for this design. Table 1 lists the parameters of the utilized transistor.

Table 1. pHEMT E-Mode Transistor Properties

Description	Properties
pHEMT Model Type	TQPED_EHSS_T3
Gate Width (W)	15 μm
Number of Gate Fingers (NG)	4

Prior to selecting the E-mode device, a comparison between the D-mode and E-mode was performed. The E-mode transistor has a higher gain for a given DC power consumption compared to the D-mode, as shown in Figure 1.

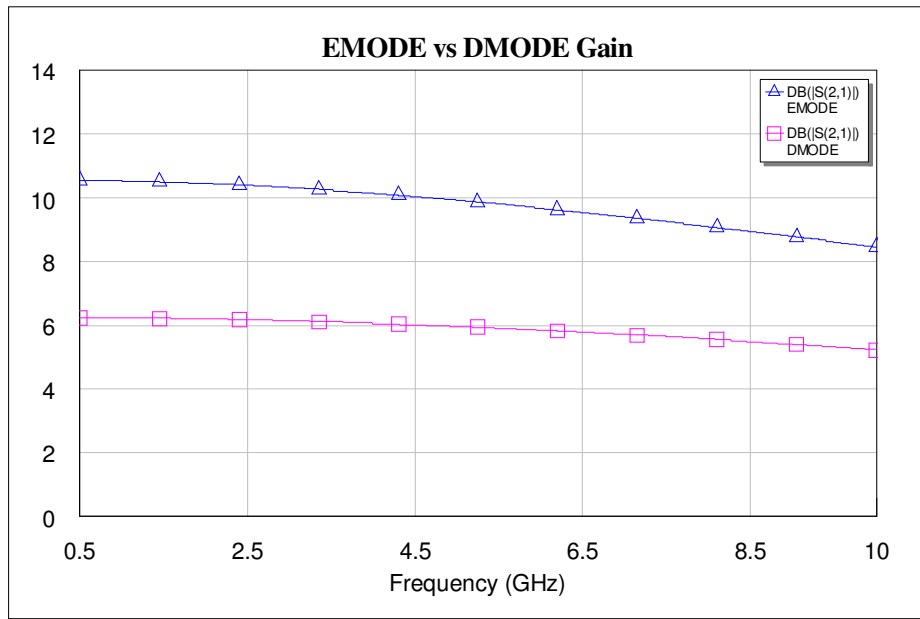


Figure 1. D-mode vs E-mode Achievable Gain

Using a swept voltage generator on the gate and drain, the IV curves for E-mode transistor is generated and illustrated in Figure 2.

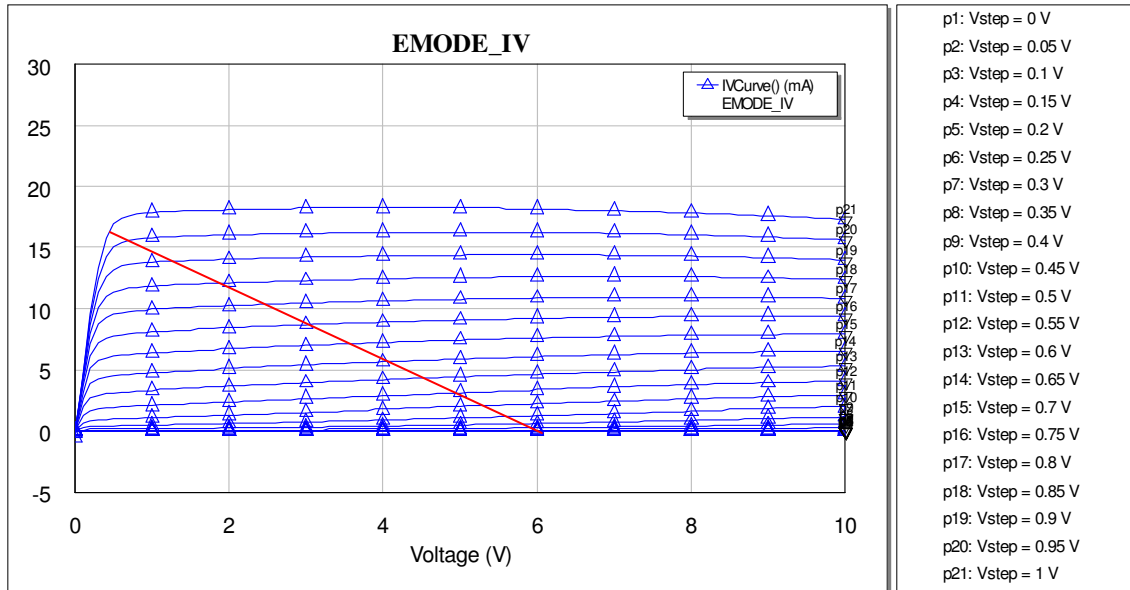


Figure 2. IV Curves for the E-mode (4x15um) pHEMT

From the IV curves, it was determined that the optimum bias point voltage for a V_{DS} of 3.3V is V_{GS} equal to 0.75V. This bias value can be obtained with a resistive divider network using the single 3.3V supply.

A Cripps Method load-line analysis is a technique that can be used to determine the optimum output impedance needed to be present at the output stage of the PA. Using the load-line shown in Figure 2, the usable region of both the drain current and drain-to-source voltage is used to derive the performance of the PA as:

$$\begin{aligned}
 V_{GS} &= 0.75V \\
 V_{DS} &= 3.3V \\
 V_{DSmin} &= 0.6V \\
 V_{DSmax} &= V_{DS} + (V_{DS} - V_{DSmin}) = 3.3V + (3.3V - 0.6V) = 6.0V \\
 IDSS &= 8.7mA \\
 I_{DSmax} &= 17.4mA
 \end{aligned}$$

The RF output power of the PA should be approximately equal to $(\Delta V_{DS} \times \Delta I_{DS})/8 \approx 11.7mW$. With the device consumption at approximately 29mW, the Power Added Efficiency (PAE) should be approximately 40%. However, the final PA design will have a lower PAE value since the design will be a dual-stage configuration and the power loss in the resistive biasing networks.

The Cripps resistance is calculated from the load-line analysis as $\Delta V_{DS} / \Delta I_{DS}$ resulting in a value of 310 Ω .

4.2 BIAS CIRCUITRY AND STABILITY

Stability is one of the most critical properties of an amplifier circuit. An unstable circuit will oscillate and hence not perform as a controlled amplifier. Likewise, a main goal of the design is to use a single supply voltage, such as a coin cell battery. Therefore, a resistive divider network is necessary to achieve the gate bias (0.75V) while the coin cell battery voltage of 3.3V will directly supply the drain bias. It was determined early in the modeling phase that the resistor values of the gate bias network directly affect the stability of the design. To combat this effect, two separate stability circuits were studied and compared. A series gate resistor, shown in Figure 3, was compared against a feedback resistor, shown in Figure 4. Since a main goal of the PA design is to minimize power consumption and maximize PAE, a DC blocking capacitor was added in series with the feedback resistor to eliminate power loss in this stability circuit.

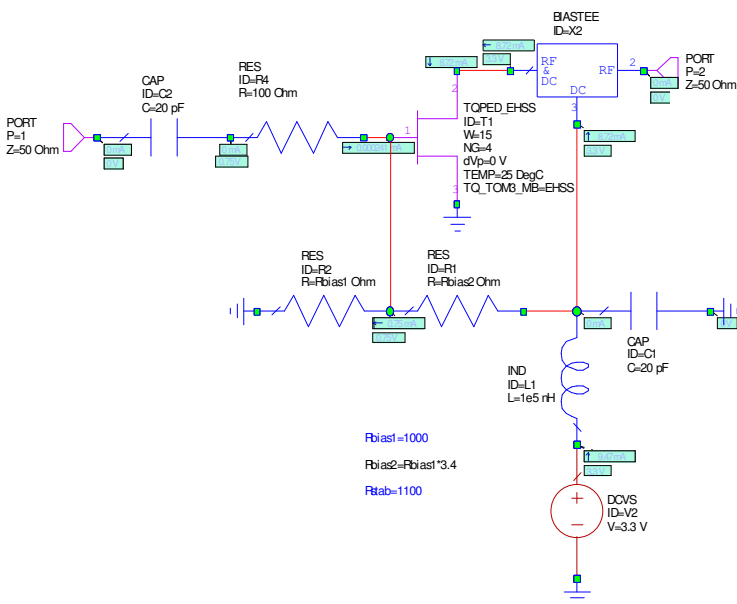


Figure 3. Gate Resistor Stability Circuit

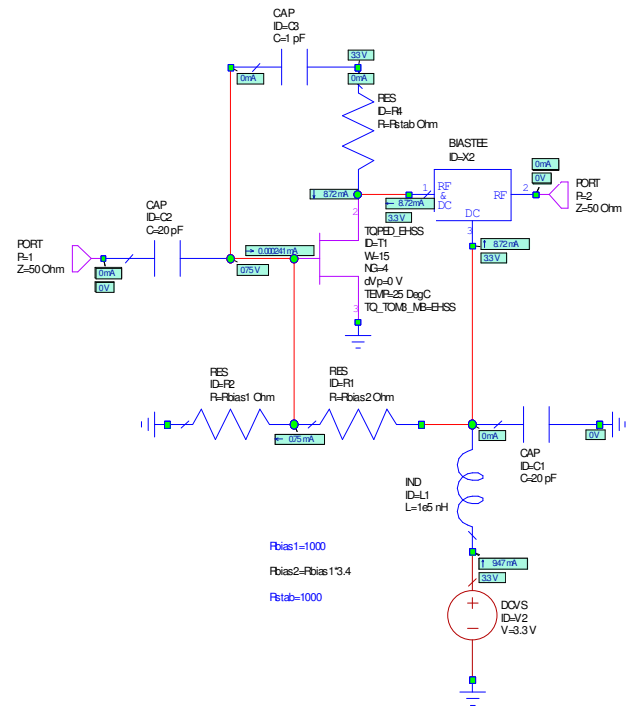


Figure 4. Feedback Stability Circuit

The performances of both circuits are shown in Figures 5 and 6. The stability, Figure 5, is slightly better across the 0.5-10GHz frequency range for the feedback resistor circuit (pink and blue curves). However the real advantage of the feedback stability circuit is noticed in comparing the gain, shown in Figure 6. The achievable gain rolls off much faster using the gate series stability circuits (pink curve) compared to the feedback stability circuits (blue curve). Thus the feedback stability circuit was chosen for the PA design.

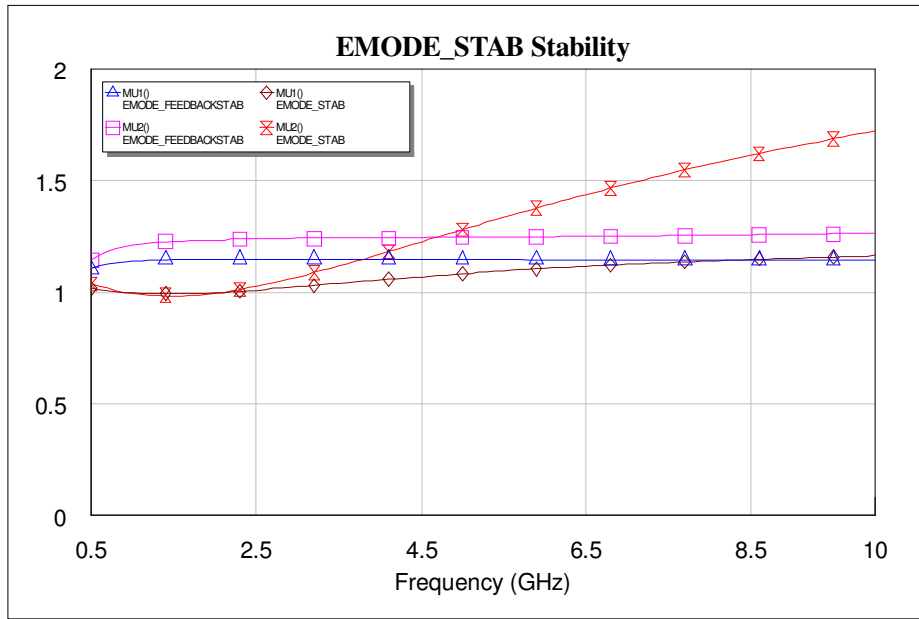


Figure 5. Stability for the Series Gate Resistor Circuit and the Feedback Resistor Circuit

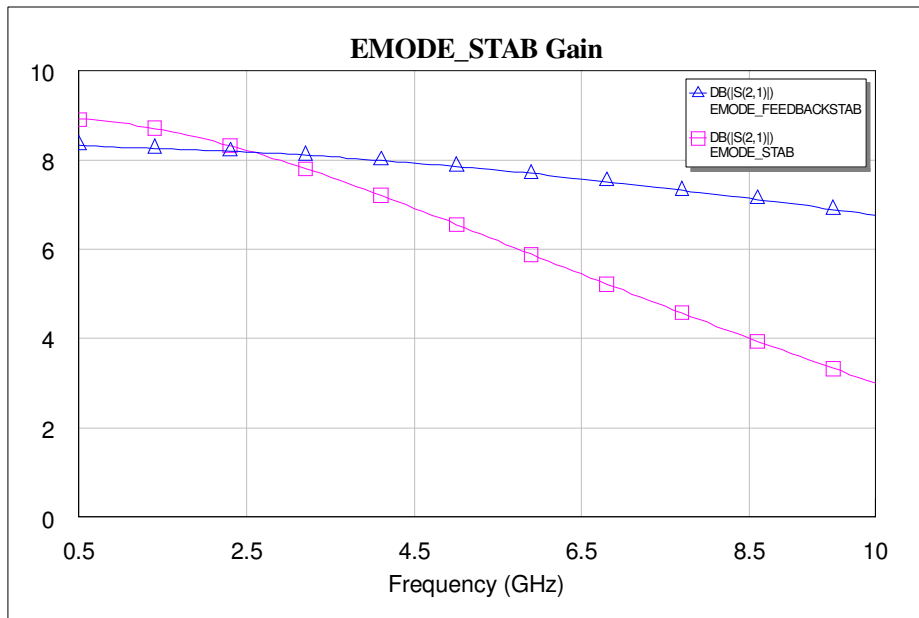


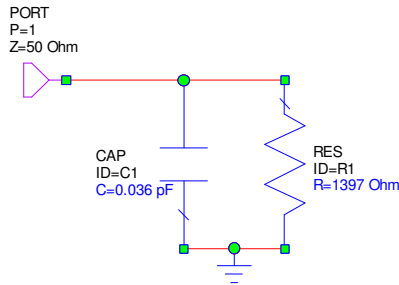
Figure 6. Gain for the Series Gate Resistor Circuit and the Feedback Resistor Circuit

4.3 INPUT AND OUTPUT MATCHING NETWORKS

The output impedance of the E-mode transistor at the center frequency of the design is shown on the smith chart in Figure 7. Using a simple circuit to model the drain impedance of the E-mode, the shunt capacitance and resistance were chosen so the impedance of the circuit was

equal to the output impedance of the transistor. Once the capacitance and resistance values are known, the resistance is changed to the R_{cripps} value, and this new impedance is used to design the PA. For maximum power transfer, the output matching network (OMN) of the PA is designed to supply the complex conjugate of the R_{cripps} model. Figure 8 illustrates the OMN design, which consists of shunt inductance of 3.4nH and a series capacitance of 251.5pF.

Simple Circuit Model of the Transistor Drain



Simple Circuit Model of the Transistor Drain with Rcripps

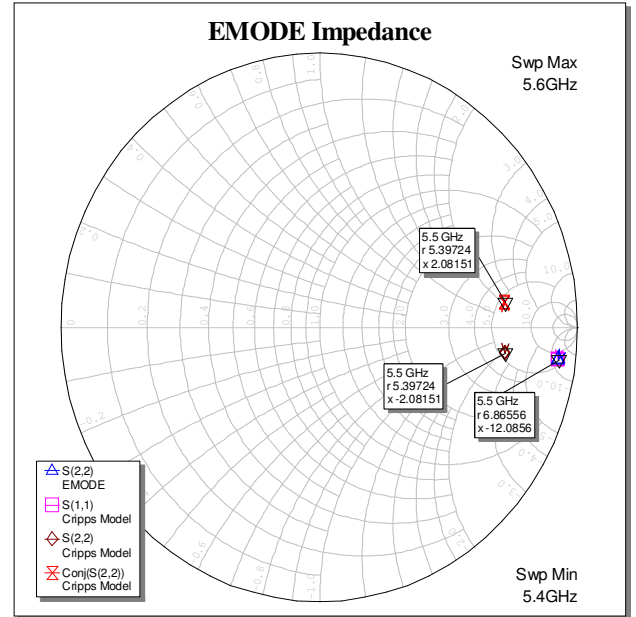
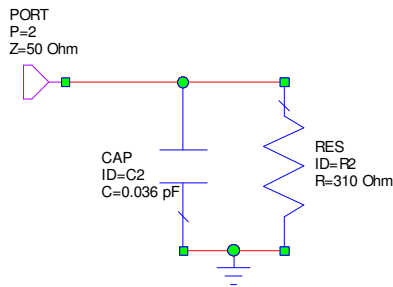


Figure 7. Transistor Library Model and Rcripps Circuit Model Output Impedance

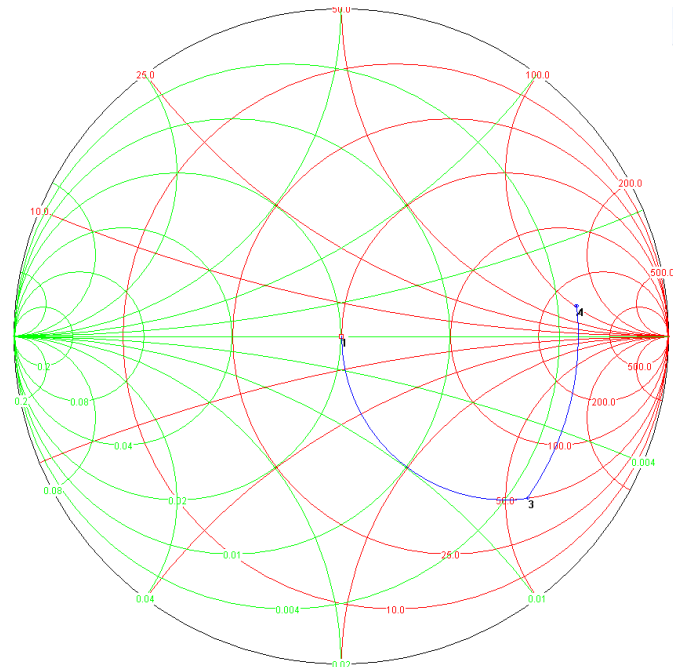
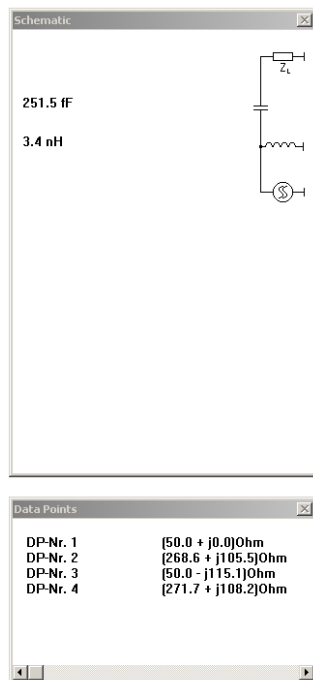


Figure 8. Output Matching Network Design

The input matching network (IMN) is designed to match input impedance of the transistor to 50Ω . A series inductance of 1.52nH comprises the IMN. A large capacitor is included in series to act as a DC blocking capacitor while minimizing its affect on the impedance matching. Figure 9 illustrates the single-stage PA design using ideal components. The linear S-parameter performance of the ideal single-stage PA design is shown in Figure 10 and the overall stability is shown in Figure 11.

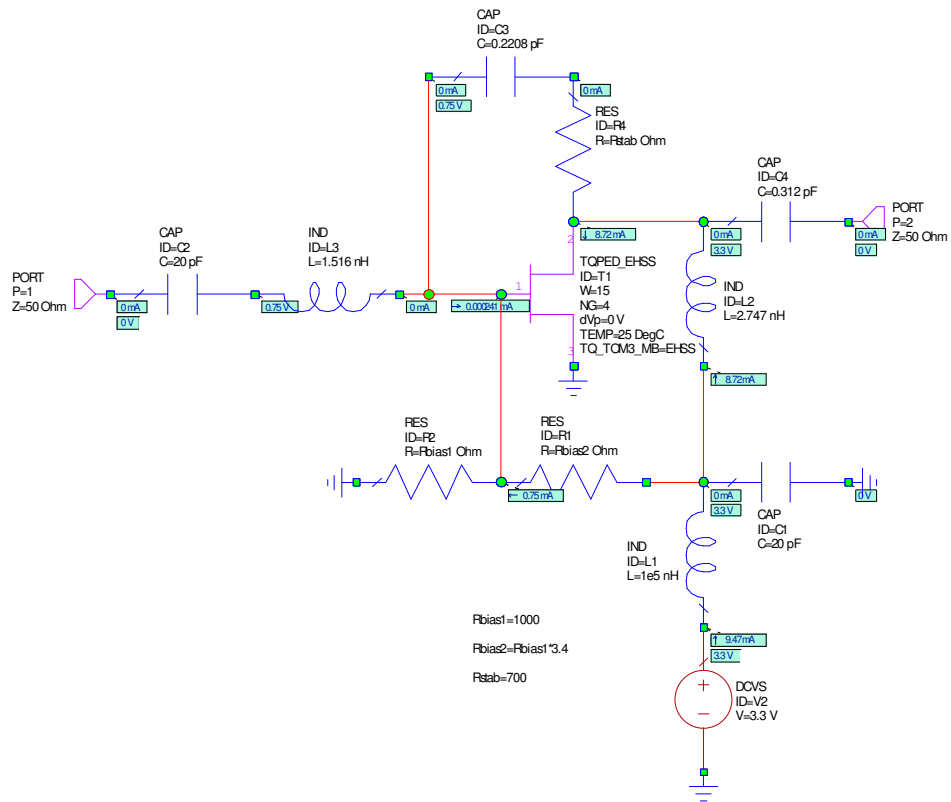


Figure 9. Ideal Single-Stage PA Design

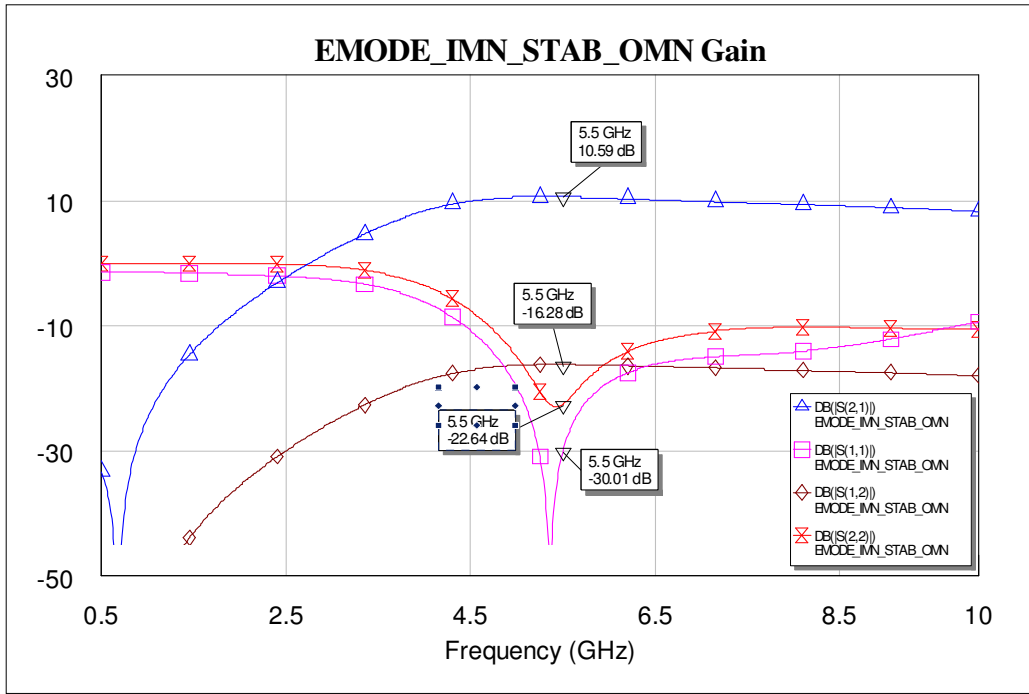


Figure 10. S-Parameter Performance of Ideal Single-Stage PA Design

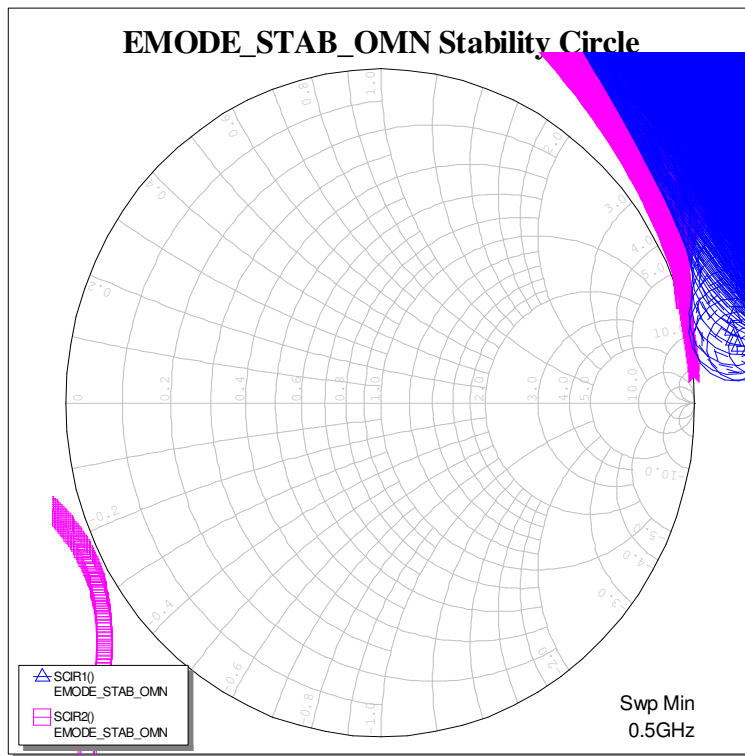


Figure 11. Stability Performance of Ideal Single-Stage PA Design

4.4 DRIVER AMPLIFIER

The driver amplifier is used to provide additional gain but with minimal DC power consumption. In addition, the driver amplifier must still be linear in the region where the output-stage amplifier design is in compression. The bias point of the driver amplifier is based on taking approximately 20% of I_{DSS} of the output-stage (reference Figure 2).

Using the load line shown in Figure 12, the RF output power of the driver stage amplifier is approximately $(\Delta V_{DS} \times \Delta I_{DS})/8 \approx (2(3.3V - 0.33V) \times 5mA)/8 \approx 3.7mW$. With the device consumption at approximately 8.25mW, the Power Added Efficiency (PAE) should be approximately 45%. However it is expected that the actual PAE will be lower due to the additional power loss in the biasing network.

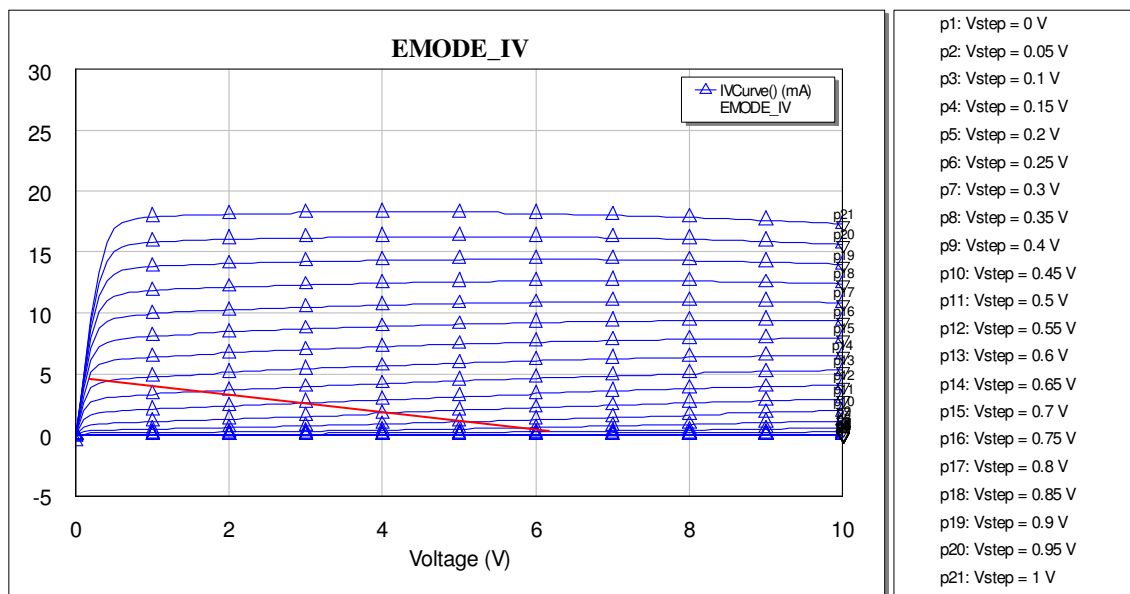


Figure 12. IV Curves for E-mode Driver Amplifier

The driver amplifier stage is designed using the same steps described in sections 4.2 and 4.3. The final ideal driver amplifier stage design is shown in Figure 13 with its linear S-parameter performance and stability shown in Figures 14 and 15, respectively.

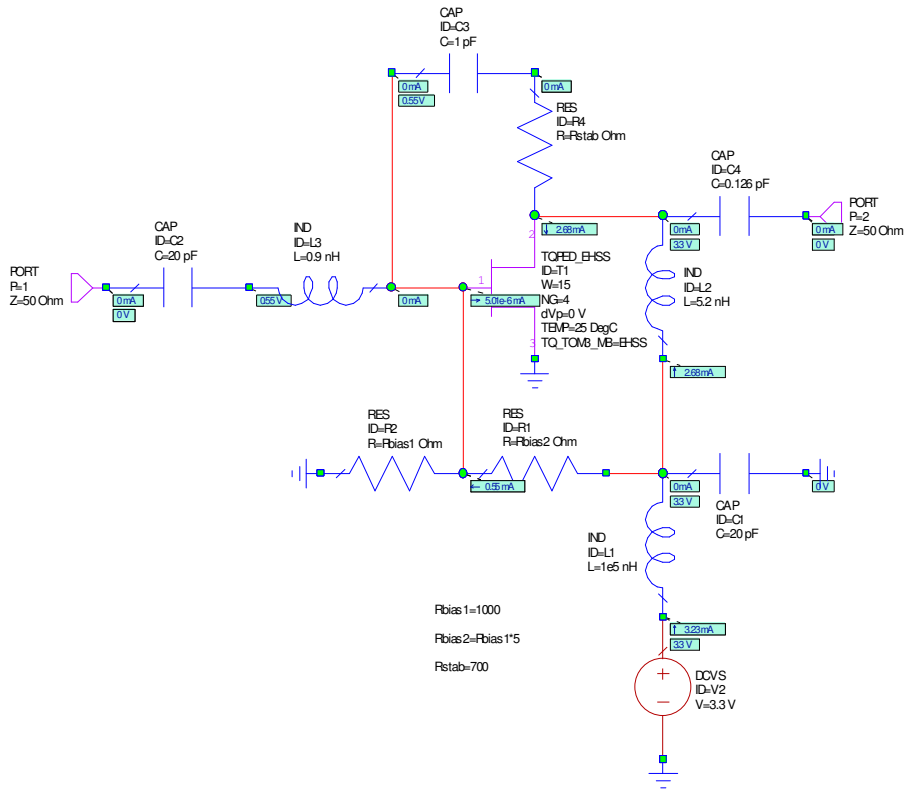


Figure 13. Ideal Driver Amplifier Design

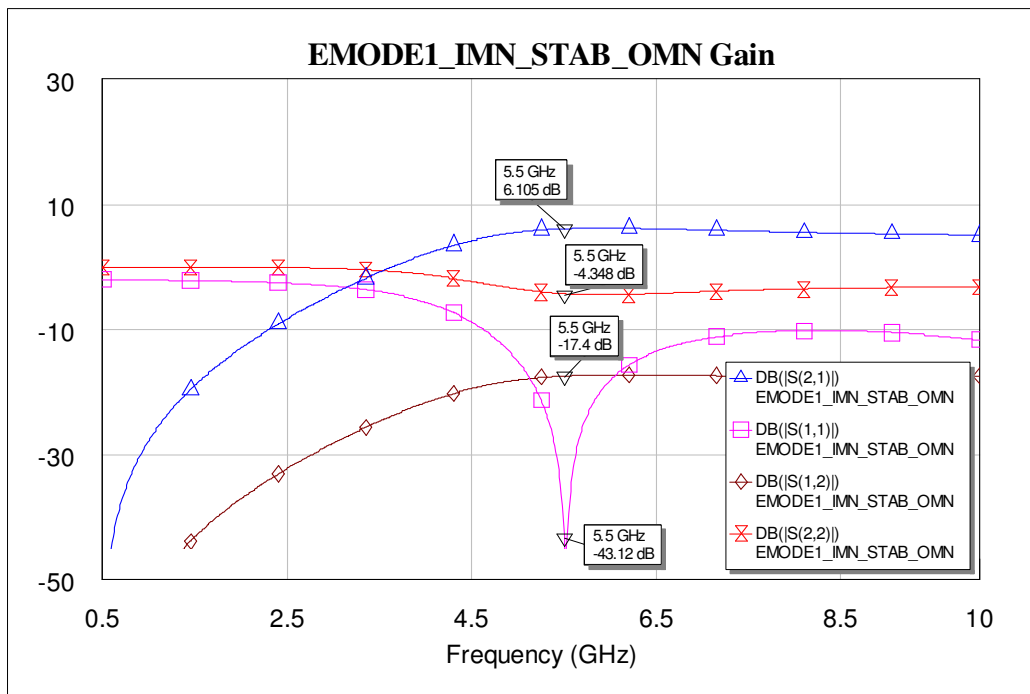


Figure 14. S-Parameter Performance of Ideal Driver Amplifier Design

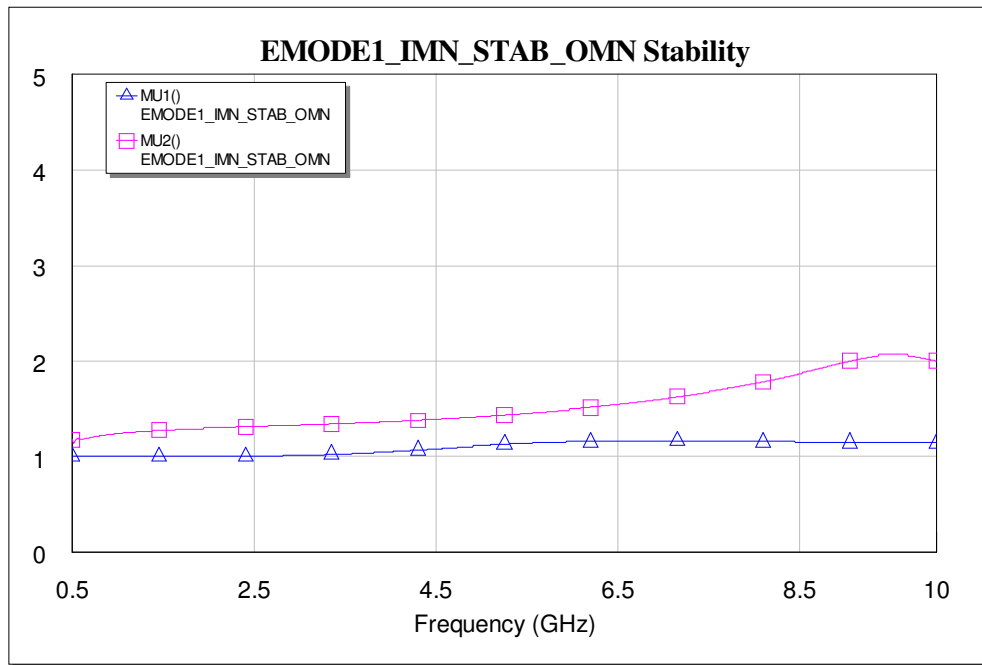


Figure 15. Stability Performance of Ideal Driver Amplifier Design

4.5 TWO-STAGE SINGLE-ENDED PA DESIGN

The final PA design consists of an input driver amplifier stage followed by an output power amplifier stage. The output of the driver amplifier stage needs to be matched to the input of the power amplifier stage. Figure 16 shows the final PA design using ideal components, with Figure 17 illustrating the linear S-parameter performance and Figure 18 illustrating the overall stability.

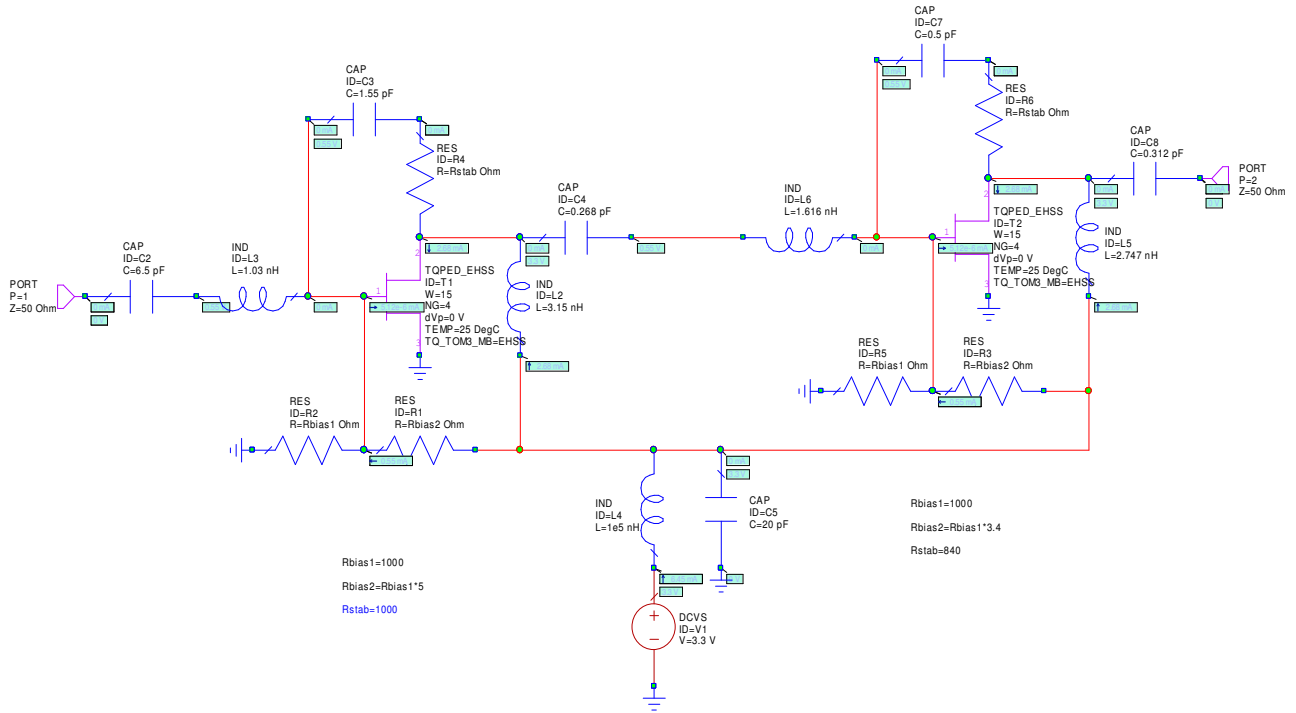


Figure 16. Ideal Two-Stage Single-Ended PA Design

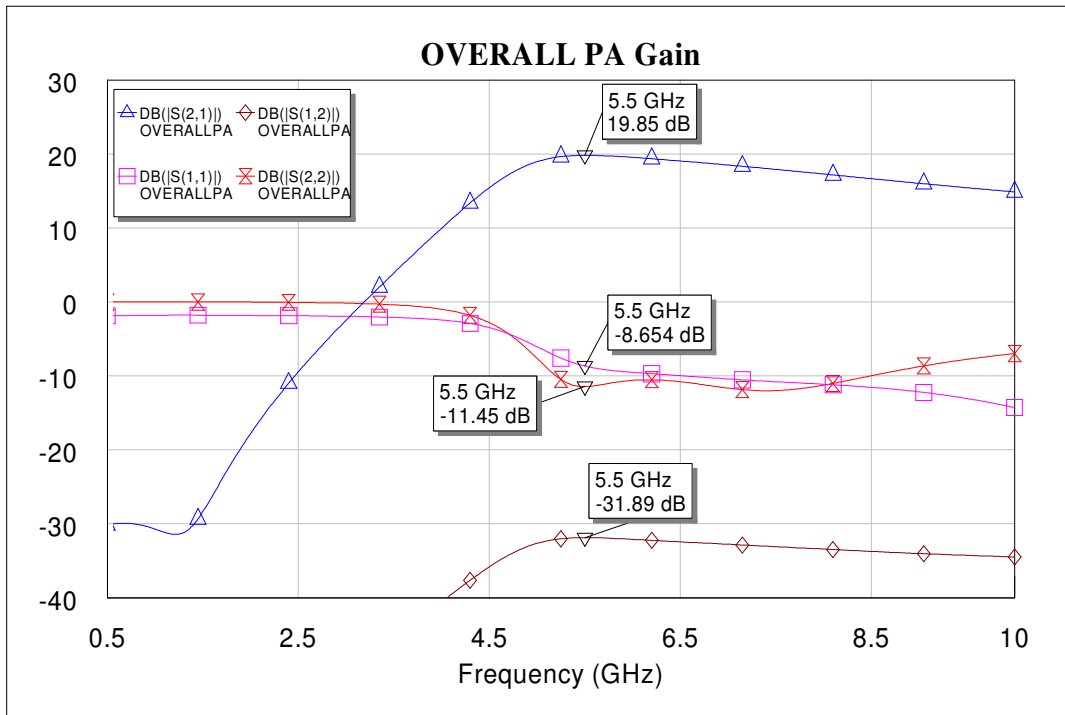


Figure 17. S-Parameters Performance of Ideal Two-Stage Single-Ended PA Design

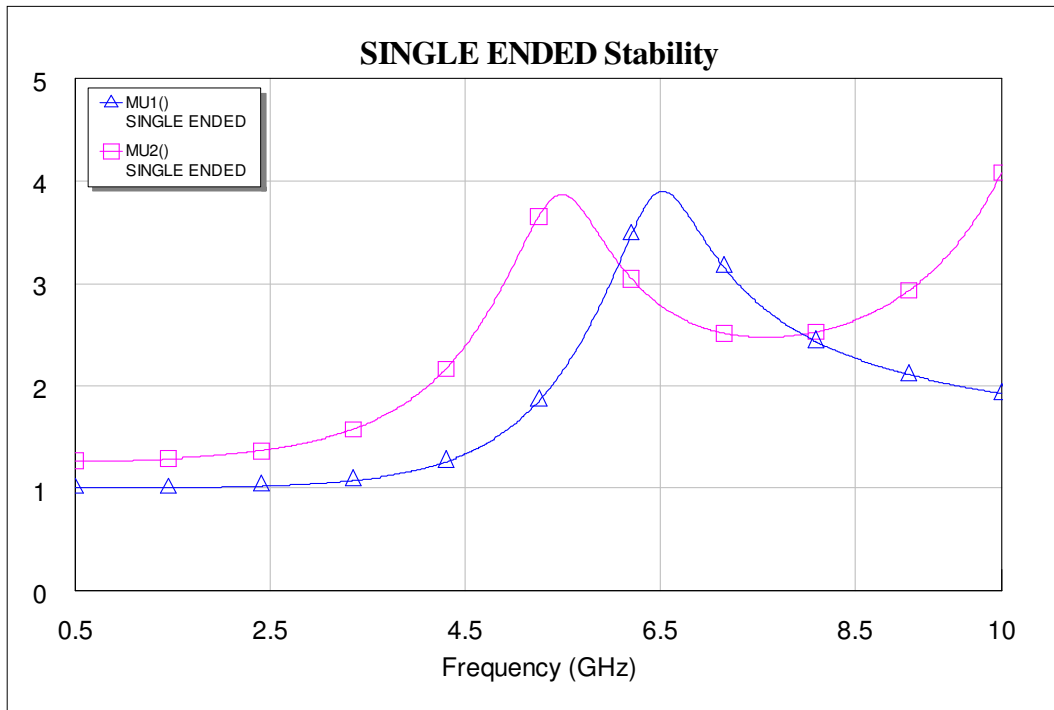


Figure 18. Stability Performance of Ideal Two-Stage Single-Ended PA Design

5. LAYOUT AND FINAL SIMULATED PERFORMANCE

5.1 IDEAL VERSUS NON-IDEAL COMPONENTS

Like the transistors, all the ideal components can be replaced with TriQuint TQPED Library components. These components model the non-ideal parasitics that arise in all real components. Replacing these components one at a time, while tuning and optimizing the circuit in discrete stages allows for a better design. In addition, since the components on the output of the transistor stages will have small resistance values associated with them, the output power will be reduced. Also, on-chip inductors and capacitors have lower quality factors (Q) resulting in less optimum performance. Figure 19 illustrates the non-ideal PA design with all ideal components replaced with TQPED Library components, including RF and Bias pads. Figures 20 and 21, respectively, show the S-parameter and stability performance with these non-ideal components, while Figure 22 shows the 1dB compression for the design frequency. Figure 23 shows the PAE of the final non-ideal design.

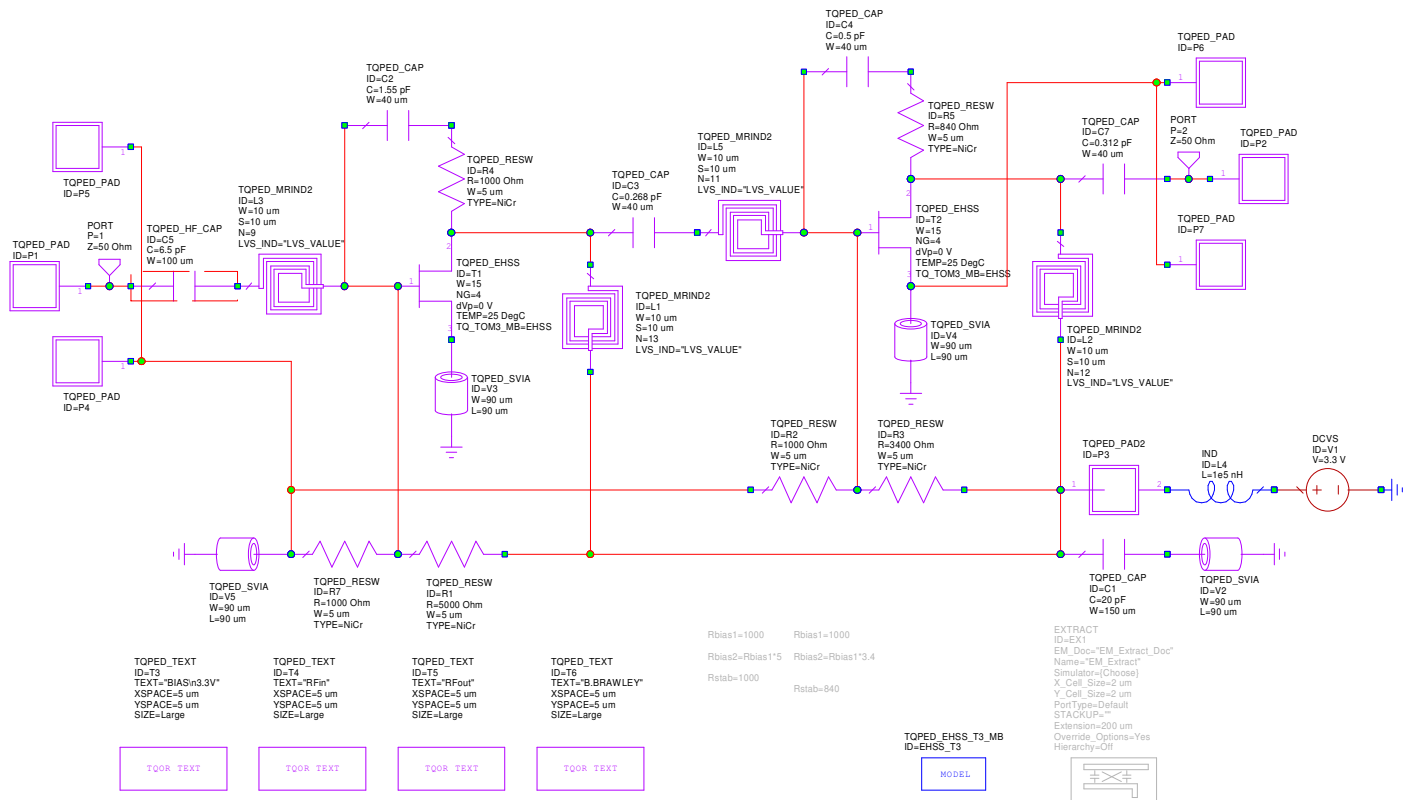


Figure 19. PA Design with Non-Ideal Components

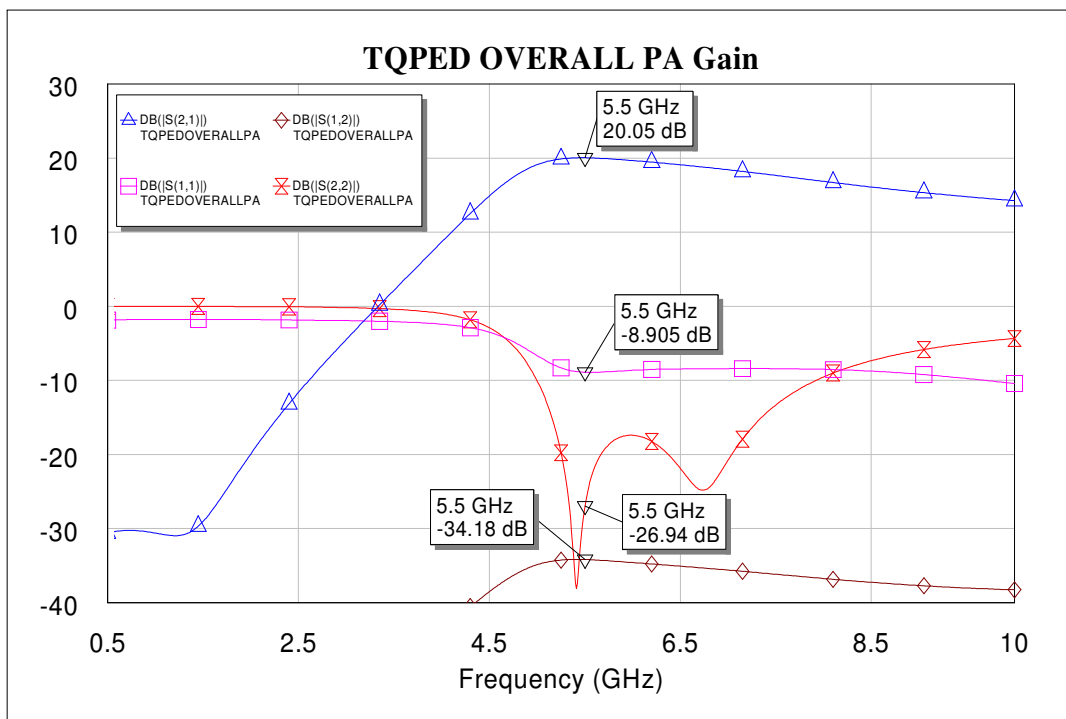


Figure 20. S-parameter Performance of PA Design with Non-Ideal Components

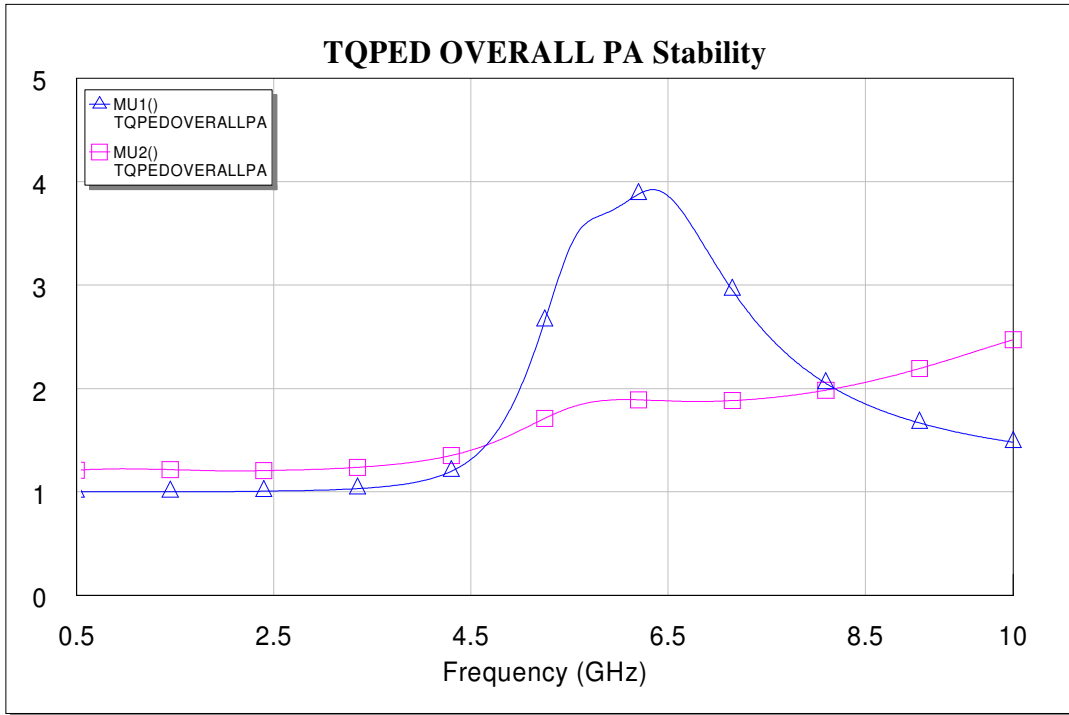


Figure 21. Stability Performance for PA Design with Non-Ideal Components

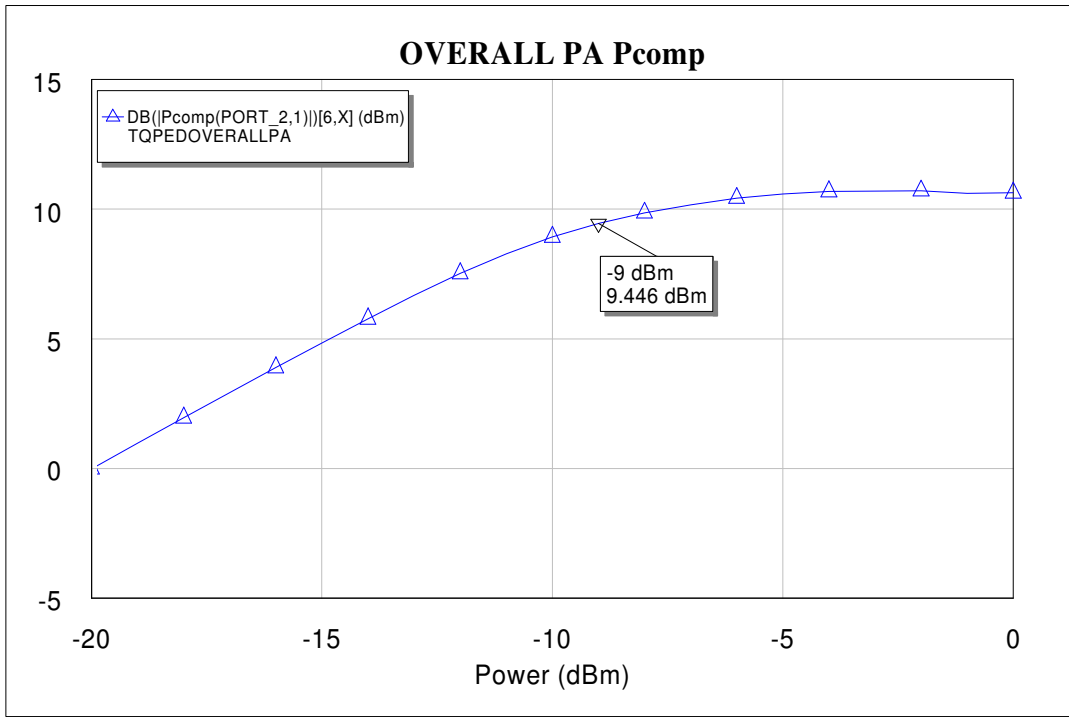


Figure 22. Power 1dB Compression for PA Design with Non-Ideal Components

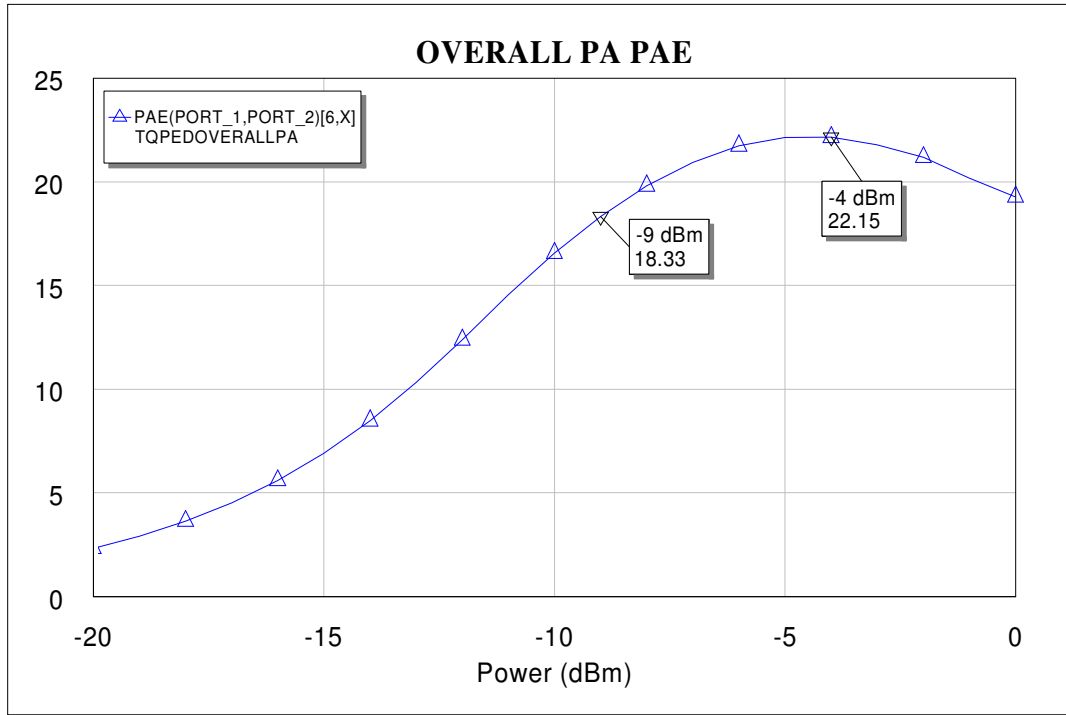


Figure 23. PAE for PA Design with Non-Ideal Components

Table 2 lists a comparison between the PA performance with the ideal and non-ideal components. Notice the slight degradation in performance due to the added resistance and lower Q factors of the components.

Table 2. Comparison Between Ideal and Non-Ideal Components Performance

Parameter	Ideal Circuit Performance	Non-Ideal Circuit Performance
Frequency [f]	5.5GHz	5.5GHz
Gain [S_{21}]	19.9	20.0
Input Match [S_{11}]	-8.7	-8.9
Output Match [S_{22}]	-11.5	-26.9
Reverse Isolation [S_{12}]	-31.9	-34.2
DC Power	42.3mW	42.7mW

5.2 LAYOUT

Once the ideal components are replaced with the non-ideal components, a layout can be generated. The TriQuint TQPED process has 3 metal layers with different thickness values. In preparation for bench testing of the fabricated PA, a ground-signal-ground pad configuration is incorporated, with the pads on a 120 μ m pitch. Figure 24 illustrates the generated layout in 2D, while figure 25 depicts the layout in 3D.

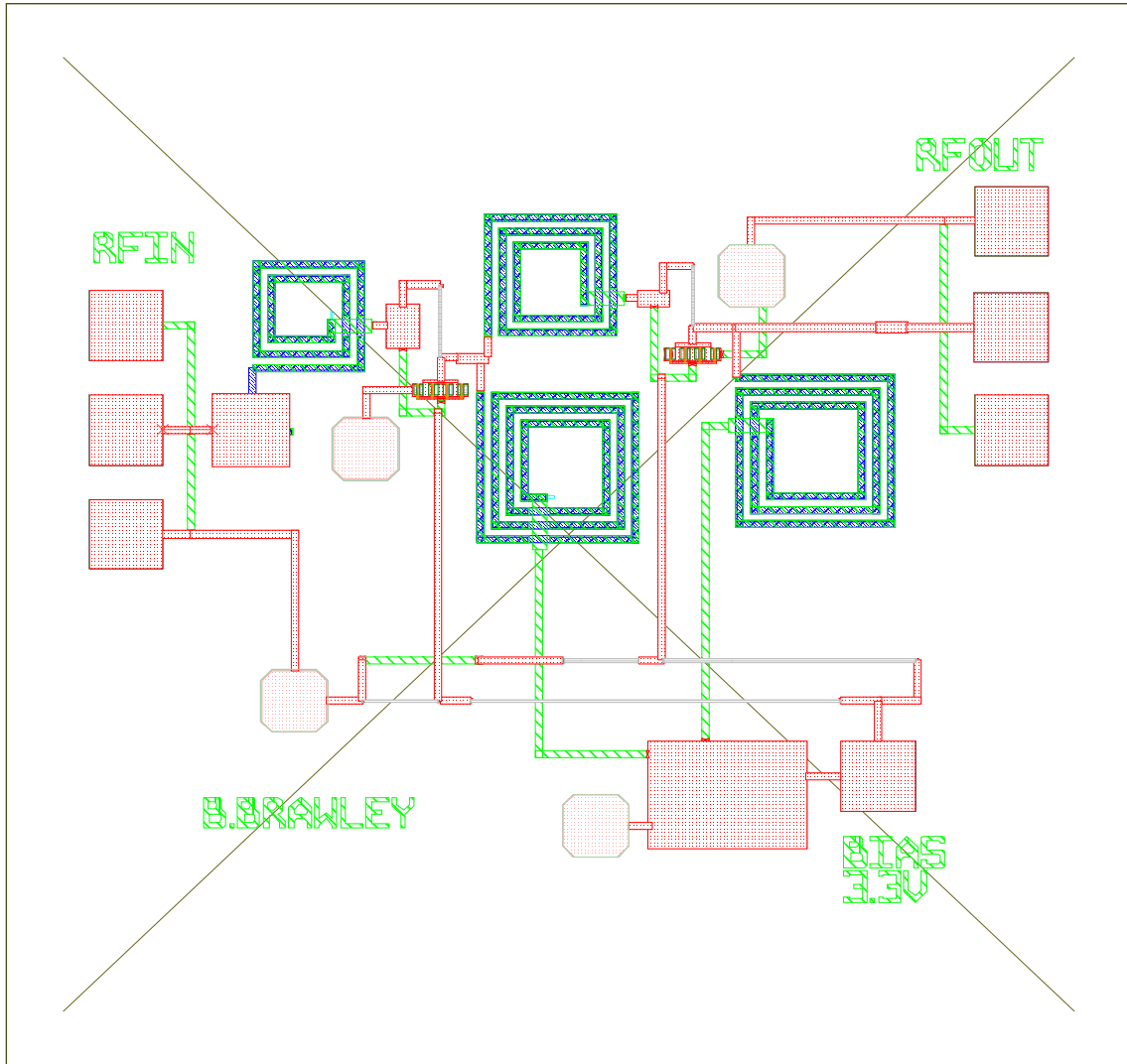


Figure 24. Final PA Design Layout

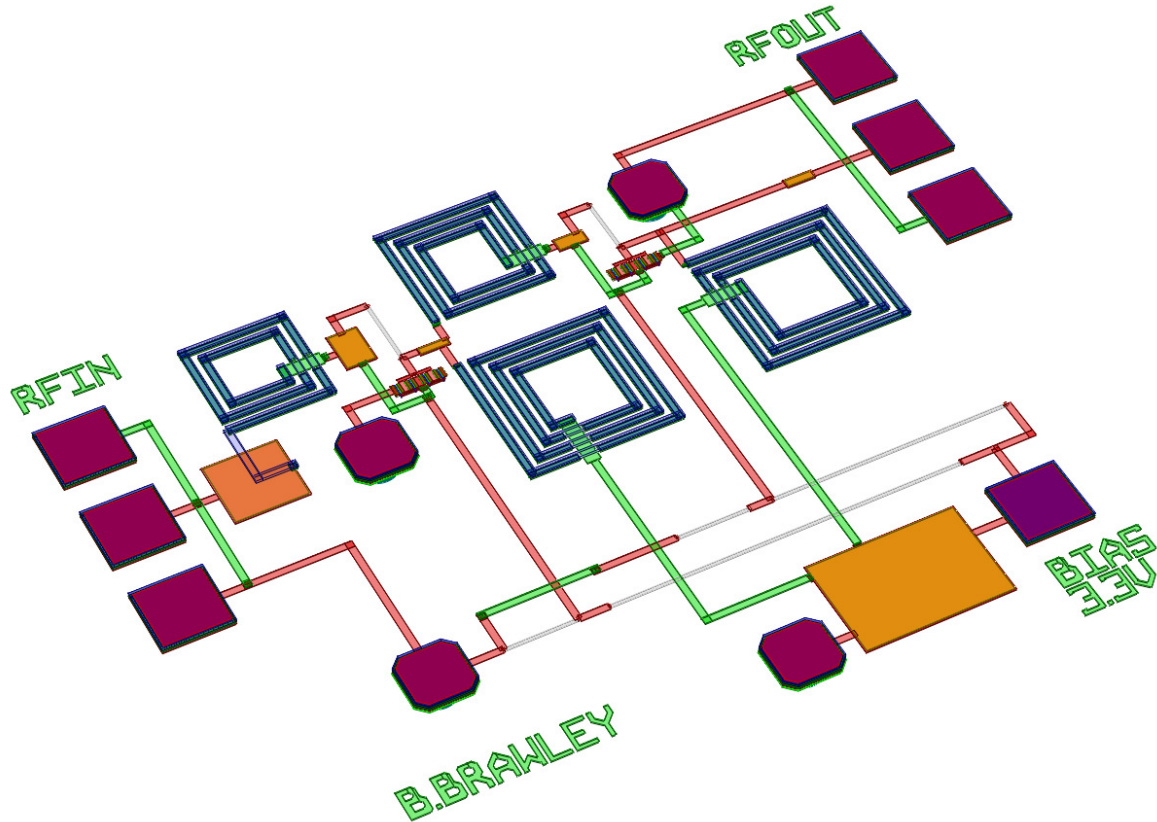


Figure 25. 3D Image of Final PA Design Layout

5.3 EXTRACTION OF LAYOUT MODEL

Once the layout is generated and signal, power, and ground paths are included, the trace runs can be extracted and included in the non-ideal simulation. Additional degradation in performance is incurred with the addition of these extracted traces.

5.4 FINAL DESIGN PERFORMANCE

Overall, the designed PA exhibits moderate output power, moderate efficiency, high gain, high reverse isolation, and low DC power consumption all encompassed in a compact layout. Table 3 lists the properties and performance of the designed PA.

Table 3. Simulated Performance of the Designed PA

Parameter	Simulated Performance
Center Frequency [f]	5.5GHz
Bandwidth	13%
Gain [S_{21}]	20dB
Gain Ripple	± 0.5 dB
Input Match [S_{11}]	-9dB
Output Match [S_{22}]	-27dB
Reverse Isolation [S_{12}]	-34dB
1dB Compression	-9dBm
DC Power	12mW
PAE	20%
Layout Footprint	60mil x 60mil

6. DISCUSSION AND FUTURE WORK

6.1 DISCUSSION

Overall, the PA design has moderate performance and all simulations indicate that the design will perform close to the design specifications. However there are some areas for improvement. First, the driver amplifier stage could be designed to operate with less power consumption, either by using a lower bias voltage or by using a smaller sized transistor. In addition, the inter-stage matching network should be designed for a power match instead of a 50Ω match. This would have increased efficiency while still maintaining the necessary gain requirements.

6.2 FUTURE WORK

In order to verify the performance of the designed PA presented, the circuit must be fabricated and measured. A comparison of measured performance to the simulated performance allows for validation of the models used in the design. The following test plan will be utilized to test the PA upon the completion of its fabrication.

6.2.1 Test Plan

Test Equipment

The following is a list of the required test equipment to measure both the linear parameters and the power performance of the PA:

Power Supply	Network Analyzer	Wafer Probe Station
Signal Generator	Spectrum Analyzer	Low-loss RF cables

Linear Parameter Measurements

The following steps are used to measure the linear (S) parameters of the PA:

- (1) Calibrate the network analyzer across the 0.5GHz to 10GHz frequency range using proper calibration standards (short, open, load, thru – SOLT). Include all RF cables necessary to connect the network analyzer to the probe station in the calibration.
- (2) Turn on DC power supply and set voltage to 0V.
- (3) Turn off DC power supply.
- (4) Place the DC bias probe on the pad of the chip labeled “+3.3V”.
- (5) Place the input RF probe (ground, signal, ground) on the pad of the chip labeled “RFin”.
- (6) Place the output RF probe (ground, signal, ground) on the pad of the chip labeled “RFout”.
- (7) Turn on the DC power supply and slowly adjust the voltage to +3.3V while watching the current draw (simulated current consumption is < ?mA)
- (8) Record the S-parameter data (S11, S21, S12, and S22).

Power Measurements

The following steps are used to measure the power performance of the PA:

- (1) Calibrate the insertion loss in the RF cable used to connect the signal generator to the probe station and the RF cable used to connect the spectrum analyzer to probe station.
- (2) Turn on the DC power supply and set the voltage to 0V.
- (3) Turn off the DC power supply.
- (4) Place the DC bias probe on the pad of the chip labeled “+3.3V”.
- (5) Place the signal generator probe (ground, signal, ground) on the pad of the chip labeled “RFin”.
- (6) Place the spectrum analyzer probe (ground, signal, ground) on the pad of the chip labeled “RFout”.
- (7) Turn on the DC power supply and slowly adjust the voltage to +3.3V while watching the current draw (simulated current consumption is < ?mA)
- (8) For Pin vs Pout measurement, set the signal generator to the frequency of interest (?) and sweep the power up to but not exceeding 0dBm and record the output power values from the spectrum analyzer.
- (9) For harmonics analysis measurements, set the signal generator to a center frequency of 5.5GHz and sweep the spectrum analyzer across a broad frequency range and record harmonic content power levels.

ACKNOWLEDGMENT

The author is indebted to Applied Wave Research, Inc (AWR) for the use of Analog Office design software package and Triquint Semiconductor for the use of their design libraries and for the future fabrication of the designed circuit.

Minhaj Raza
EE 787
WIDE BAND LOW NOISE AMPLIFIER
1.2-3GHz
Dec 9th 2008

Abstract:

The design of a Monolithic Microwave Integrated Circuit (MMIC) low power low noise amplifier (LNA) circuit will be described in this paper. The use of LNA Design is applicable in the industrial fields of GPS, Medical, and Cellular technologies. The amplifier operates with 3 VDC supply voltage at VDD and a 0.75 VDC at VGG and total current draw of 76 mA. The amplifier has a 1 dB bandwidth of more than 1.8 GHz (1.2 GHz-3 GHz). The amplifier has the NF of less 1.7 db throughout its working frequency. The amplifier achieves a power gain of 29 dB with the input 1 dB compression point of -14.5 dBm. The amplifier has the input port match (S11) of -14dB or better, and in addition the output port match (S22) is also -13 dB or better. The unconditional stability of the LNA is also observed for the entire working frequency.

Introduction:

This report will focus on the design, simulation, layout, optimization and test plan for the low power low noise amplifier. The normal use of a LNA is at the front end of the RF receiver system providing the first stage of amplification after the receive antenna and adding as little noise as possible with providing the maximum gain. Large gain in the first stage of the receiving chain also factors into setting the overall noise figure of the receiver; however, a high gain and low noise figure amplifier is difficult to obtain using a single-stage design. Therefore, multi-stage designs are utilized to incorporate both of these desired traits.

Design Approach:

The design consists of a two-stage amplifier design powered by a positive 3VDC source for drain ports of the PHEMT and another 0.75 VDC source for the gate ports of the PHEMT. Two 6 X 50um EMODE FET's are used in the amplifier due to their higher gain and lower noise figure. A feedback resistor in series with a capacitor was used to flatten the output response of the LNA as shown in Figure 1.

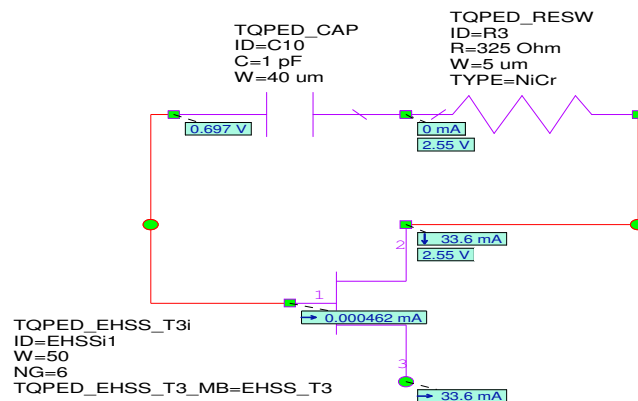


Figure 1. PHEMT with feedback Resistor

The simplest form of the design (common-source) was used to approach the design goals. In it, the RF input signal is applied to the gate of the PHEMT while amplifier RF output signal is extracted from the drain port. The input and output matching networks perform impedance transformations to provide noise and power matching, respectively. The goal is to have low noise and high gain characteristics at the same time. Maximum output power occurs when the input impedance equals the conjugate match of the source impedance, resulting in $\Gamma_{in} = \Gamma_s^*$. The condition for minimal noise is met when $\Gamma_s = \Gamma_{opt}$. An input matching network (IMN) is designed to impedance match Γ_{opt} of the transistor to 50Ω , Γ_{opt} is the the optimum reflection coefficient or the lowest noise figure at a designed frequency (2GHz). This information was obtained from the .s2p data file of the measured data provided in the class. Figure 2 shows a generalize input and output matching circuit of an amplifier except for a series resistor added prior to the output matching network.

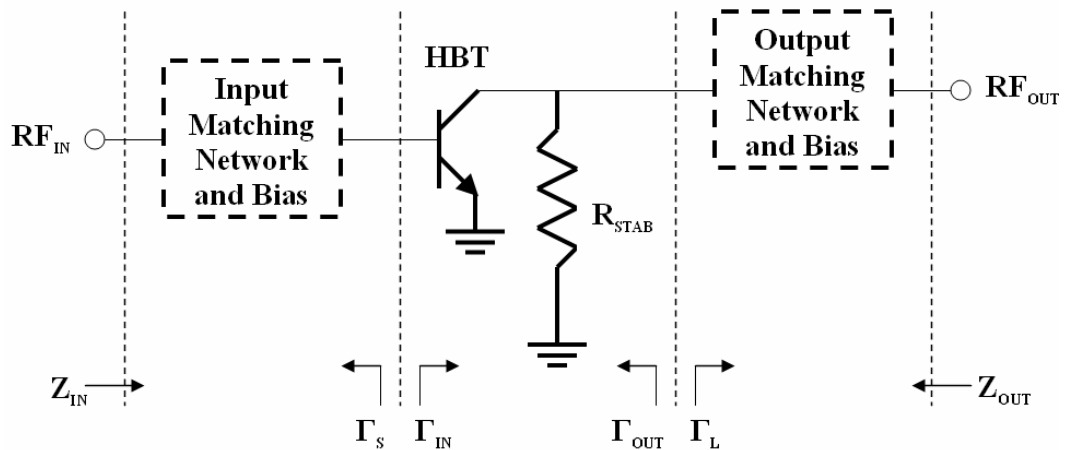


Figure 2. Input and Output Matching

The stability of the circuit was observed at this point, and it was noticed that a stabilizing circuit network was required to add stability resistors to stabilize the the LNA for the entire working frequency. Figure 3 shows a output stability circuit.

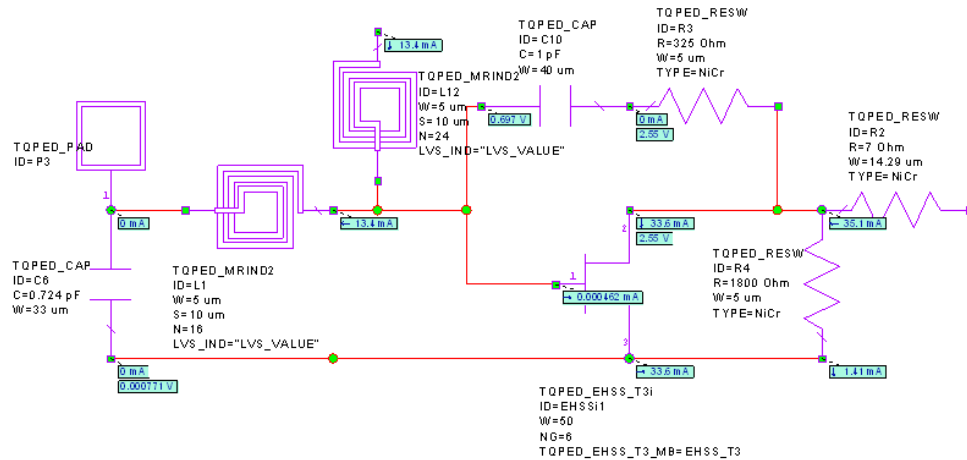


Figure 3. Output Stability Resistor Network

To achieve a high gain LNA, a two-stage design is employed. This architecture allows for the first stage to be designed with an extremely low noise figure, hence setting the overall noise figure of the LNA. Then the second stage provides the necessary amplification to achieve an overall high gain.

SIMULATION SOFTWARE

Applied Wave Research (AWR) Microwave Office provided by the Applied Wave Research version 9.01 Build 4229 rev1 (58736), was used as the simulation software package for this project. Linear and nonlinear circuit simulations were used to analyze the performance of the LNA. Elements in the TQPED process library TQOR_TQPED v1.1.21 from TriQuint Semiconductor were used to create a final design that accounts for parasitics in these non-ideal components. The initial design was generated using the lumped elements and gradually these lumped elements were replaced by TriQuint parts.

BIASING

The first step in the design process is to determine the DC operating point. This is accomplished by sweeping the drain voltage (VDS) and the gain voltage (VGS) of the transistor. The EMODE pHEMT is used in calculating the DC IV curves, shown in Figure 4. It is determined that an appropriate bias for the LNA is:

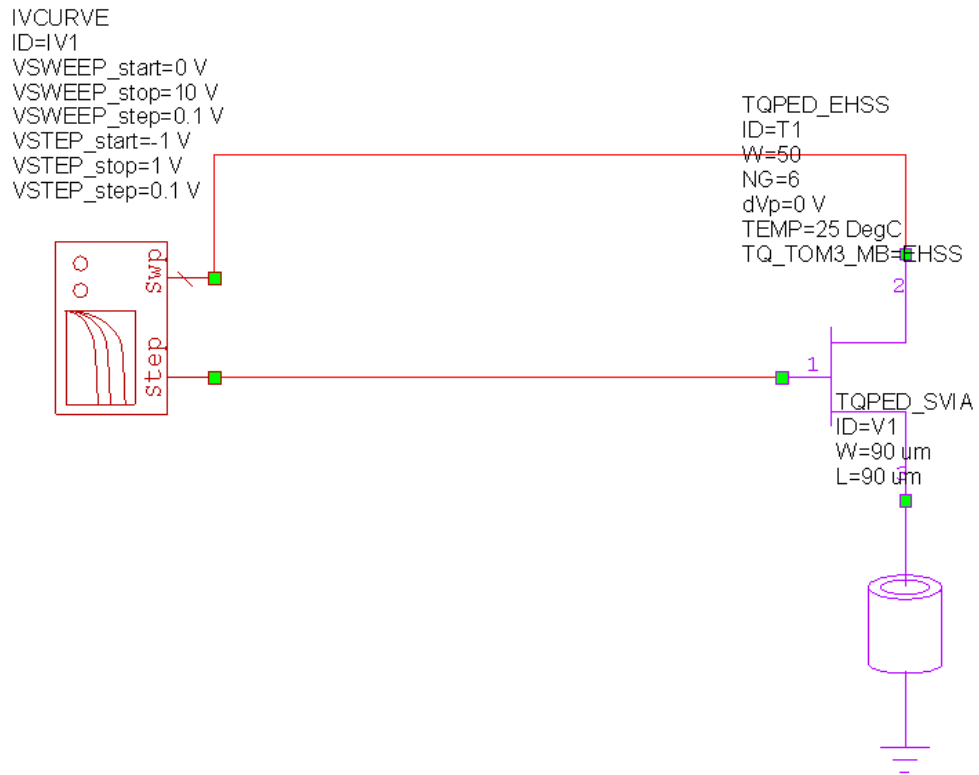


Figure 4. IV Curve Circuit

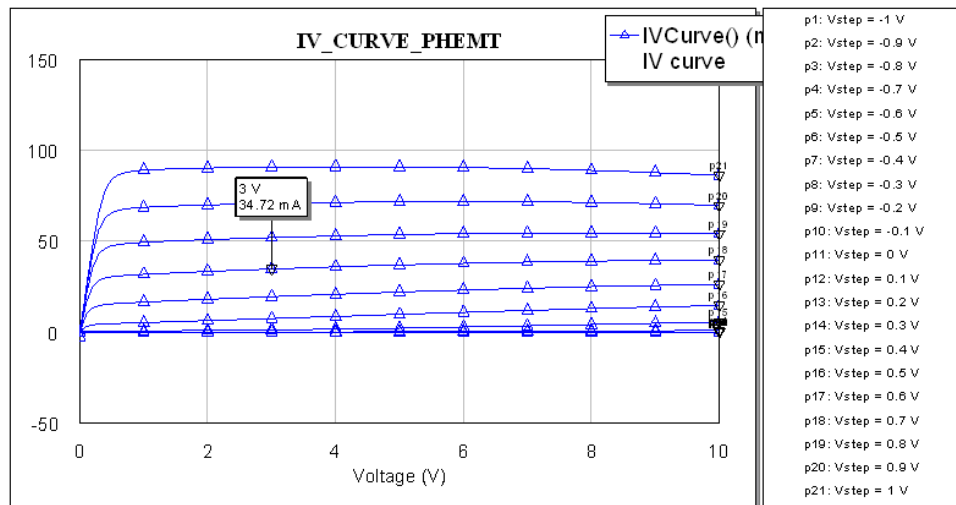


Figure 5. IV Curve for the PHEMT

Note that the biasing gate voltage is positive because the pHEMT is an EMODE.

STABILITY

The next step in the design process is to stabilize the transistor. Because the LNA is being designed for a minimum NF, the stabilizing network should be placed on the output side of the LNA. Two methods of stabilizing the transistor were studied, (1) a feed back resistor between the drain and gate, and (2) a shunt resistor and a series resistor on the drain. Both of these options were attempted separately, but neither provided unconditional stability. However, when used in conjunction with one another, the LNA became unconditionally stable from 1 GHz to 3.2 GHz.

Since the LNA is being designed to operate via a battery, it is essential to minimize wasted power loss in any portion of the stabilizing network. Therefore, DC blocking capacitors were used in series with the stabilizing resistors to minimize the amount of power dissipated by the resistors. DC blocking capacitors are also utilized to isolate the inter-stages of the amplifier in addition to the external RF ports on the amplifier from the various bias voltages.

INPUT AND OUTPUT MATCHING NETWORK

Subsequently the input matching network was designed for the best possible noise figure and the output matching network was designed for maximum gain as well as the best input and output match. Both networks are comprised of series capacitors and shunt inductors. It should be noted that all components are ideal in this initial design phase, including the components used in the previously discussed stabilizing network.

IDEAL SINGLE-STAGE DESIGN

After designing the input and output matching networks, a single-stage design is complete. Favorable results were obtained after simulating the design:

Gain = 15 dB

NF = 1.5 dB

Match (input) = -15 dB.

Match (output) = -20 dB

IDEAL TWO-STAGE DESIGN

After the ideal single stage design yielded promising results, two identical single stages were cascaded together. The ideal cascaded system provided the following performance:

Gain = 29.2 dB

NF = 1.65 dB

Match (input) = -13 dB

Match (output) = -22dB

Final Design:

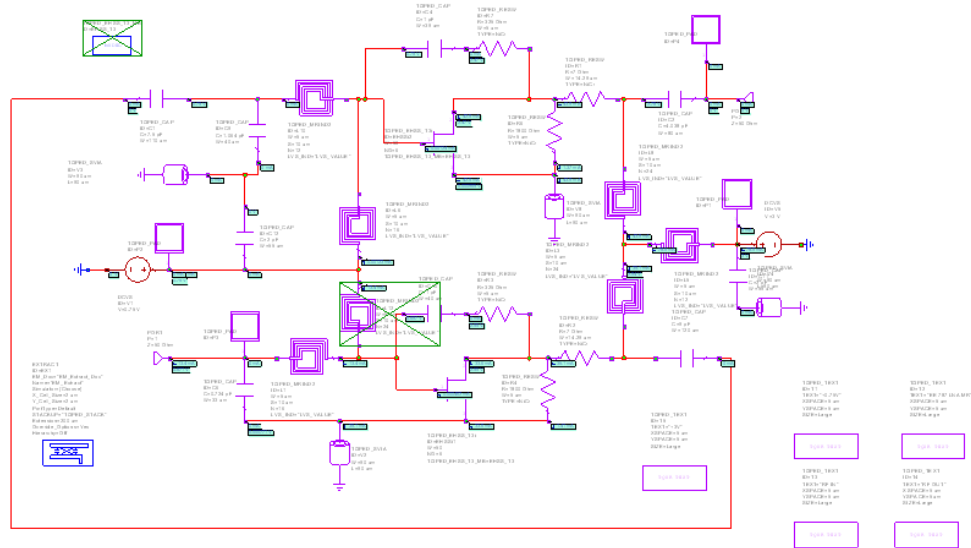


Figure 6. Complete Circuit Design of the LNA with TriQuint Parts

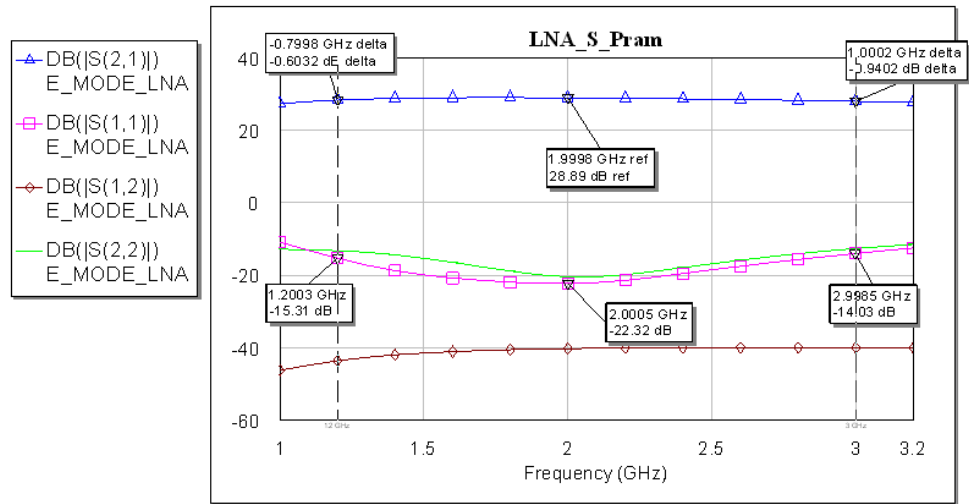


Figure 7. Linear / S-Parameters of LNA

It was observed that by comparison the E-mode PHEMT has better gain response with a low Noise Figure than the D-mode.

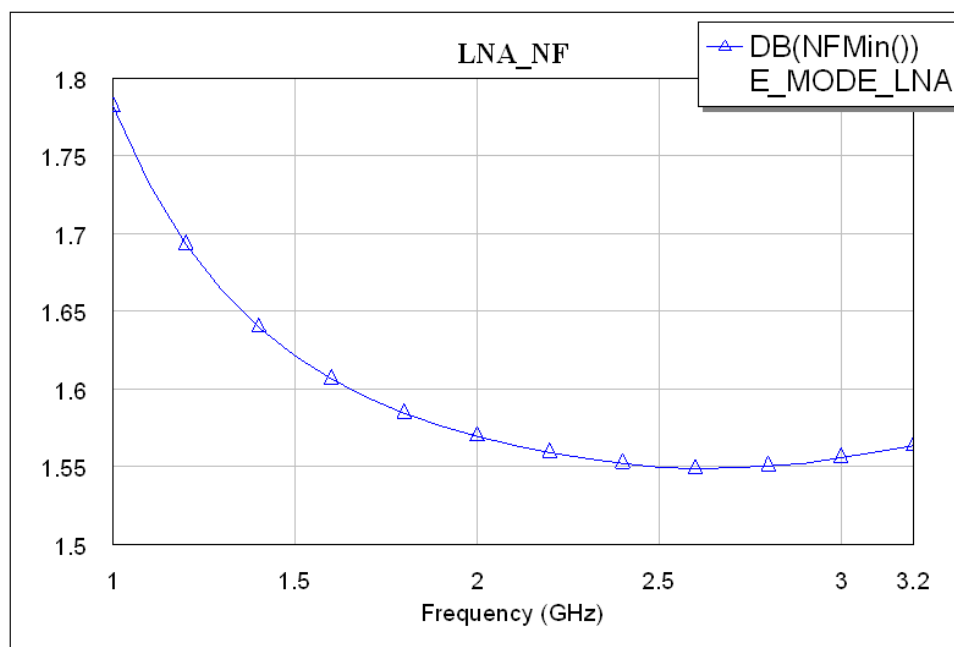


Figure 8. Noise Figure Response of the PHEMT

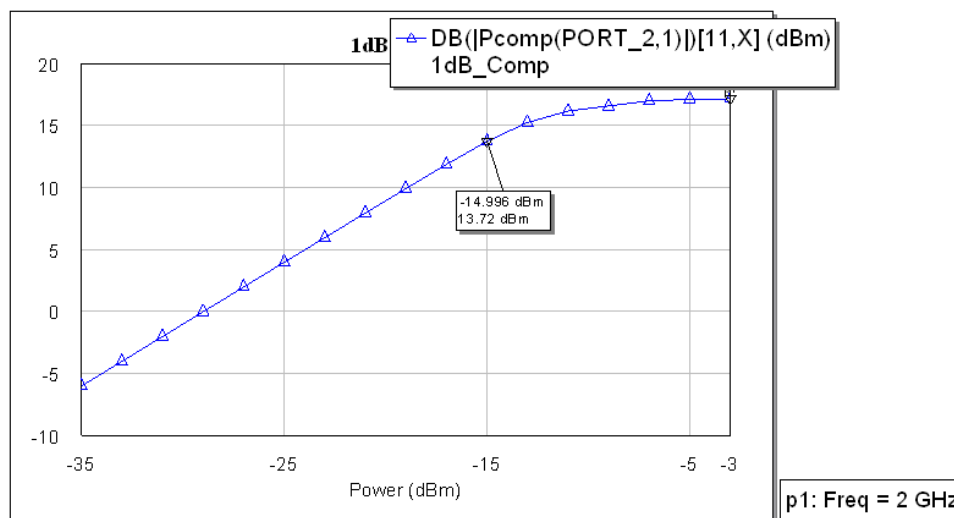


Figure 9. 1 dB compression point for the LNA

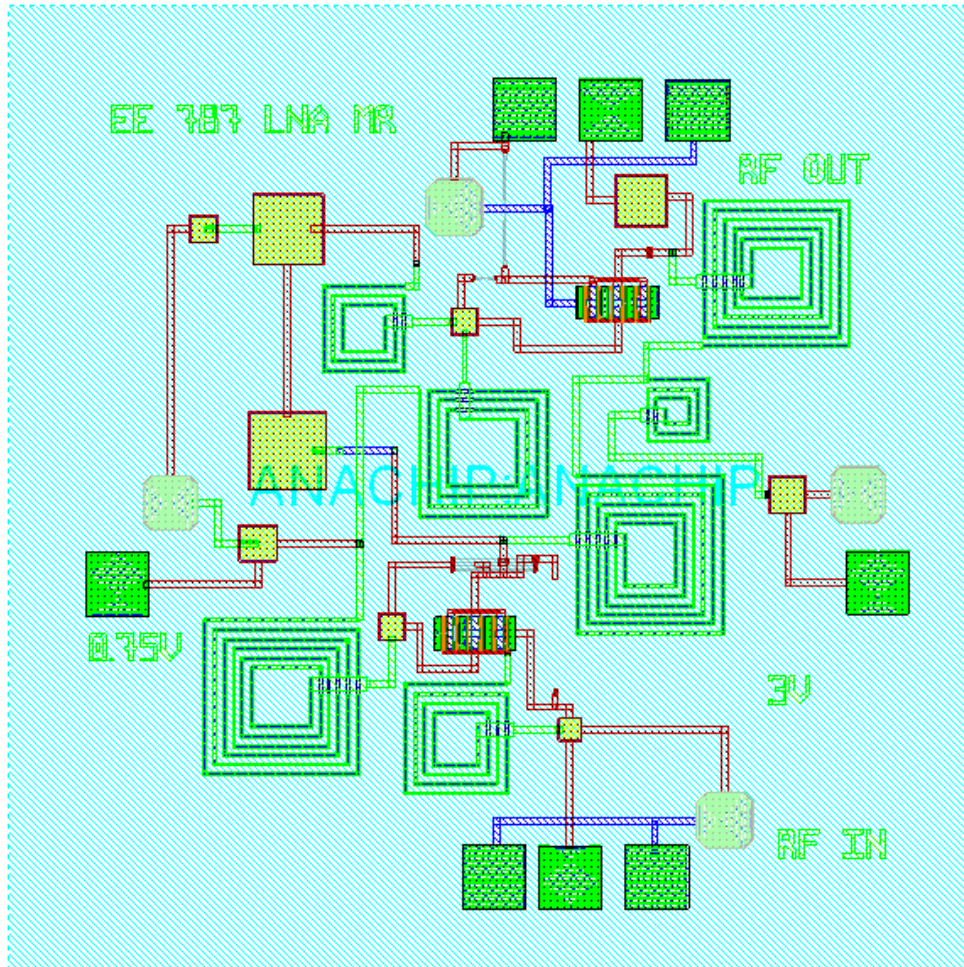


Figure 10. Final Layout of the LNA

TEST PLAN

There are three measurements of interest for the LNA: (1) S-parameter measurements, (2) noise figure measurements, and (3) compression measurements.

First, power must be applied to the chip. To do this, apply a needle probe to the voltage supply to 0.75 and 3 volts pads on the chip. Slowly, increase the voltage to 3 VDC with also providing 0.75 VGS and verify that the power supply is drawing approximately 36 and 45 mA of current for both stages.

For the s-parameter measurements, first calibrate the network analyzer. Then, connect the GSG probes to the RF IN pad and the RF OUT pad on the chip.

Finally measure the parameters on the network analyzer and save the data to a disk. A similar setup is employed when taking the noise figure measurements. First calibrate the noise figure meter. Apply a noise source at the RF IN side of the chip. Take a measurement at the RF OUT side of the chip and save the data.

A signal generator in conjunction with a spectrum analyzer is used to make the compression measurements. Connect the signal generator to the RF IN side of the chip. Connect the spectrum analyzer to the RF OUT side of the chip. Set the signal generator to 2.4 GHz. Start at -40 dBm, and sweep the input power in 1dBm increments until compression is reached. Save the data to a disk.

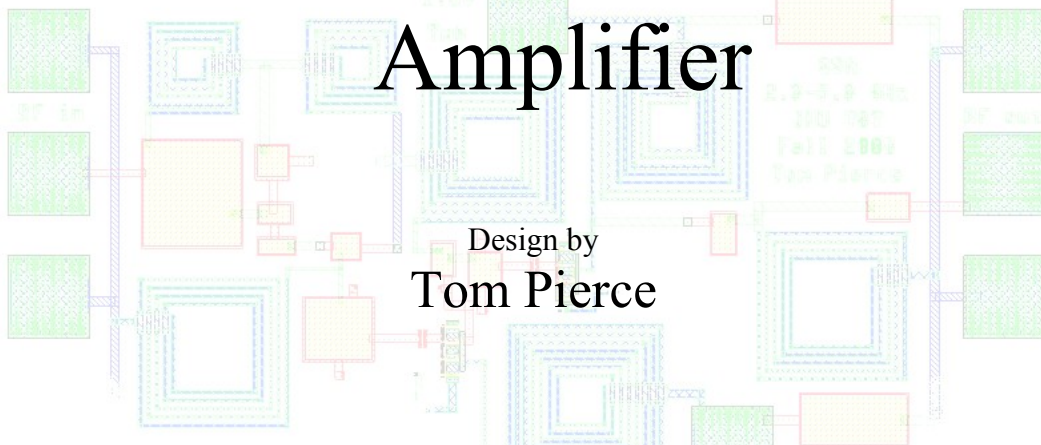
SUMMARY

Overall, the designed LNA exhibits low noise figure, high gain, high reverse isolation, and nominal DC power consumption all encompassed in a compact layout. A comparison of measured results to the simulated performance will allow for validation of the models used in the design.

Broadband Small Signal Amplifier

Design by
Tom Pierce

JHU 525.787 MMIC Design
Fall 2008



Abstract

This paper describes the design and simulation of a two stage broadband small signal amplifier using the TriQuint process for MMIC fabrication. The design uses two E-Mode pHEMT devices with feedback to achieve a gain of 23 ± 1 dB from 2.305 GHz to 5.785 GHz. The total DC power consumption is 19.68 mW from two 1.5 V supplies. All simulations were performed in Microwave Office version 8.01r build 4229 from Applied Wave Research, Inc. (AWR) with the TriQuint process library version 1.1.21.

Introduction

This broadband small signal amplifier is designed for low power and small size. It can be operated off of two 1.5 volt batteries drawing 6.56 mA each. It fits within a 30 x 60 mil area including scribe lines. Each stage is identical with the same size FET and voltage divider bias network. The frequency of operation is from 2305 MHz to 5875 MHz.

The front end of the amplifier consists of a low pass filter with a cutoff frequency of about 5.8 GHz. Next is the input matching network followed by the first stage FET. An interstage matching network sits between the two stages and at the end is the output matching network (Figure 1).

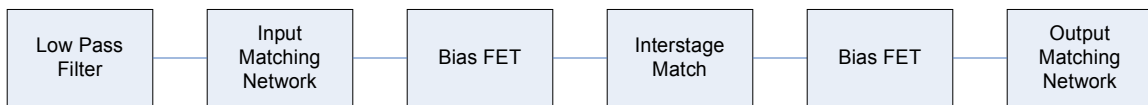


Figure 1 Block diagram of 2-stage broadband amplifier

Design Approach

The specifications and achieved goals for this design are shown below (Table 1). All but one of the specifications have been achieved and the power and size have been cut in half. The output IP3 was not meet due to an oversight in the requirements that went unnoticed until the design had been completed.

Parameter	Specification	Goals
Frequency	2305 to 5875 MHz	2305 to 5875 MHz
Bandwidth	>3575 MHz	>3575 MHz
Gain (small signal)	≥ 20 dB	22 dB
Gain Ripple	± 1 dB	± 1 dB
Output IP3	> +20 dBm	+6.9 dBm
VSWR, 50 Ω	< 1.5:1 input & output	< 1.5:1 input & output
Supply voltage	+ 3.3 V	+ 1.5 V
Size	60 x 60 mil ANACHIP	30 x 60 mil
FET size	4x15	4x15

Table 1 Design specifications and achieved goals.

The first step of this design is to determine the type of FET to use. The Emode PHEMPT provides higher gain than the Dmode at the same power with less noise. The Emode is also biased with a positive gate voltage, which will make the bias network design simpler. With the type and size of the device known, an IV curve trace is generated to determine the bias voltage (Figure 2).

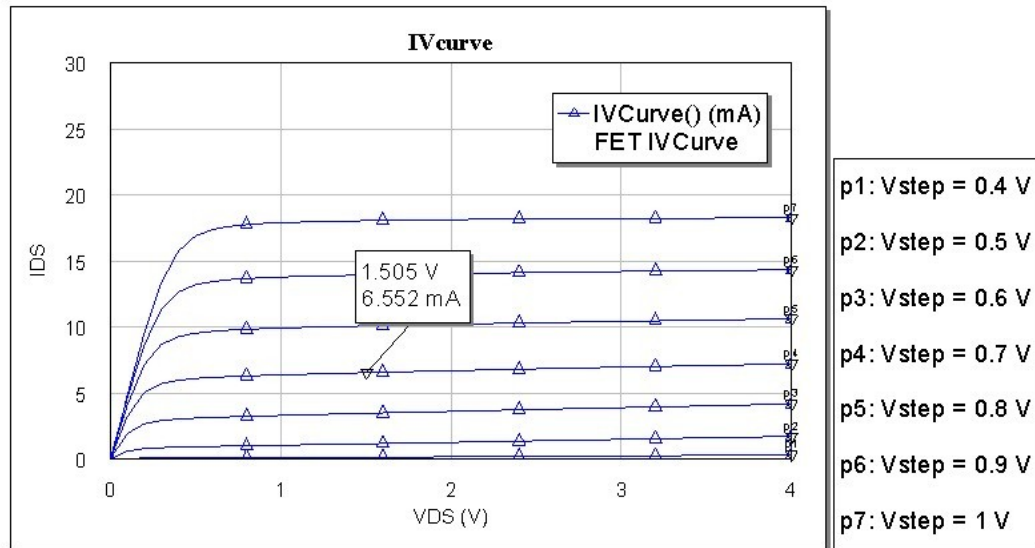


Figure 2 IV curve for 4x15 Emode PHEMPT

Keeping low power in mind, we would like to be less than 10 mW DC power for each stage. With a 1.5 V supply, we have a budget of 6.67 mA. This translates to $V_{GS} = 0.7V$.

The bias network is a simple voltage divider with 2000 Ω and 1750 Ω resistors (Figure 3). An 8 Ω gate resistor was added for stability. A large inductor is used to isolate the rf signal from the DC source, and a capacitor to ground is also used to short out any rf that makes it past the inductor. The voltage divider network also provides a shunt feedback path on each stage. The feedback path helps increase bandwidth and stability. Another design approach to increase bandwidth is a distributed design, but that would require more components and more power. Since this design focuses on low power and small size, the feedback amplifier design is used.

The input, interstage, and output matching networks all use a tee network layout with two capacitors and one inductor (Figure 4). Early simulations looked promising, but the gain did not fall off at high frequencies. A 5-element low pass Pi network filter (Figure 5) was added at the input to cut off the high frequency gain. If a larger bandwidth is desired, the low pass network elements can be adjusted, but the gain will still slowly decrease as the frequency increases.

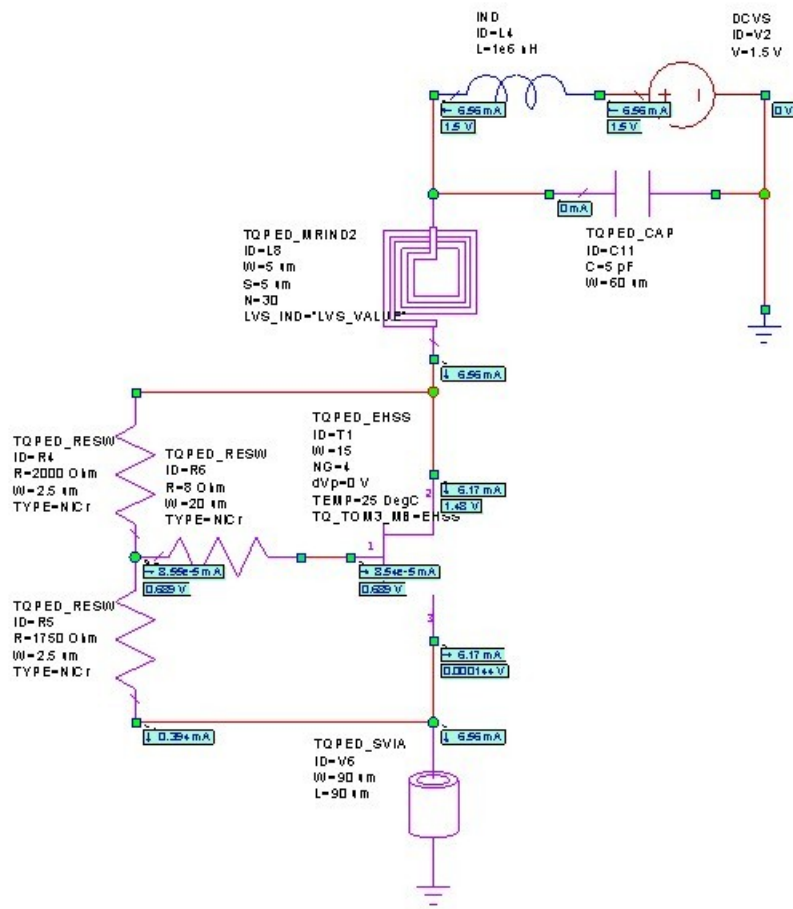


Figure 3 DC bias network with FET.

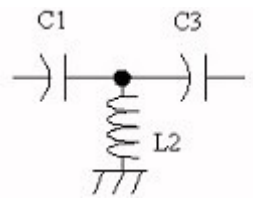


Figure 4 Matching network layout.

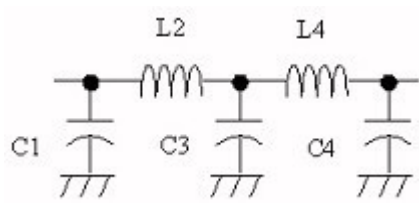


Figure 5 Low pass filter layout.

Simulations

The following results were simulated in Microwave Office version 8.01r build 4229 from Applied Wave Research, Inc. (AWR) with the TriQuint process library version 1.1.21. The FETs use the TOM3 model.

The gain and match are shown in figure 6. The median of the gain is 23.1 dB with a ripple of ± 1 dB over the targeted frequency range. The minimum gain of 22.12 dB is at 2.305 GHz and the maximum gain of 24.09 dB at 4 GHz. The match could be better, but at the cost of gain flatness. The VSWR is shown in figure 7 and meets the specification of $< 1.5:1$ for the entire bandwidth except for a small range around 3 GHz. This was noticed after the design had been frozen and went unnoticed because of not rechecking the VSWR after rerouting some traces in the layout.

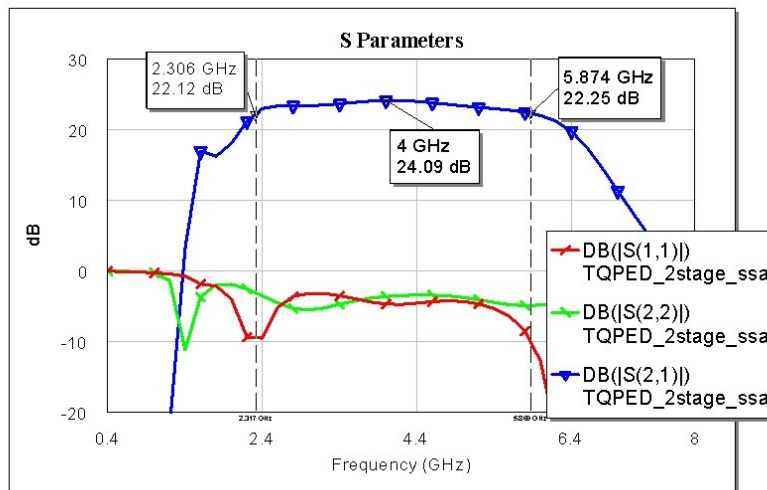


Figure 6 Gain and match.

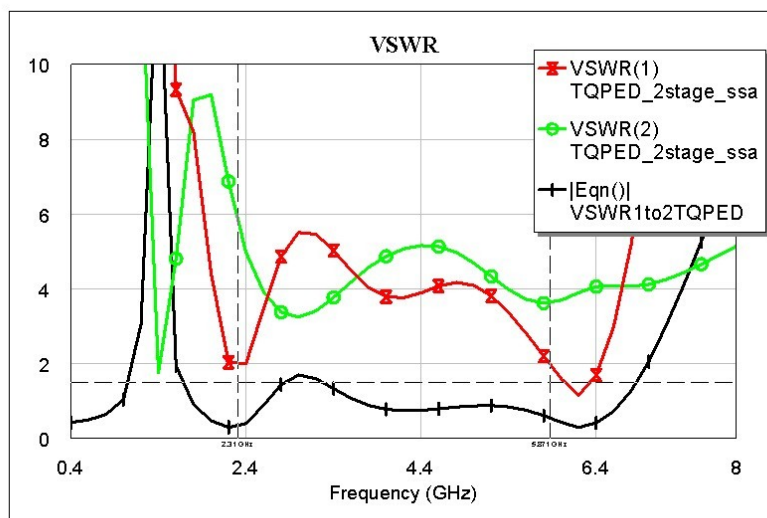


Figure 7 VSWR.

The output power at the 3dB compression point is 6.9 dBm (Figure 8). The output IP3 specification is $> +20$ dBm, but during the design, the power gain was mistakenly used as the check for this parameter. Increasing the DC power will increase the rf output power, but at the cost of efficiency, and this design may burn out at high DC power.

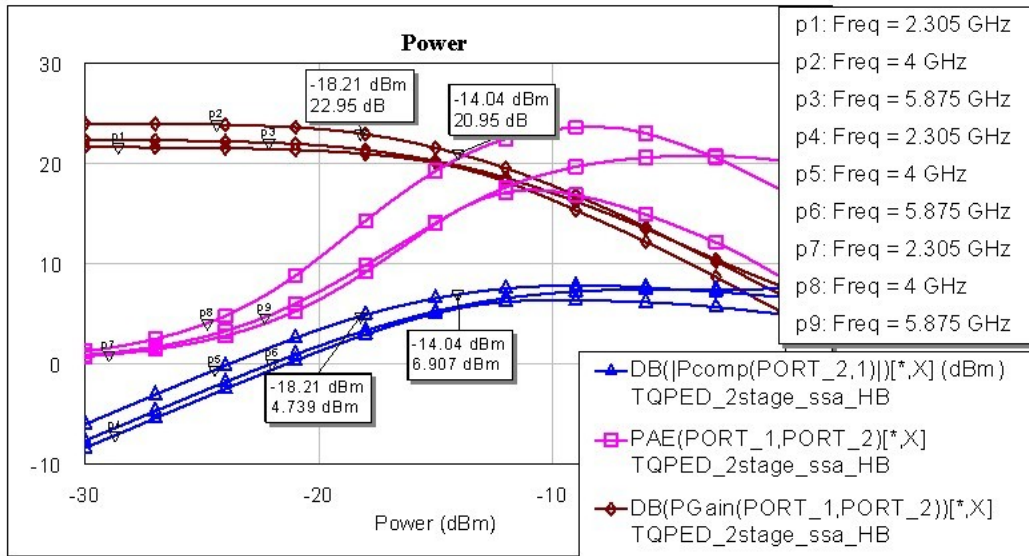


Figure 8 3dB power compression.

Figure 9 shows that the design is unconditionally stable for all frequencies.

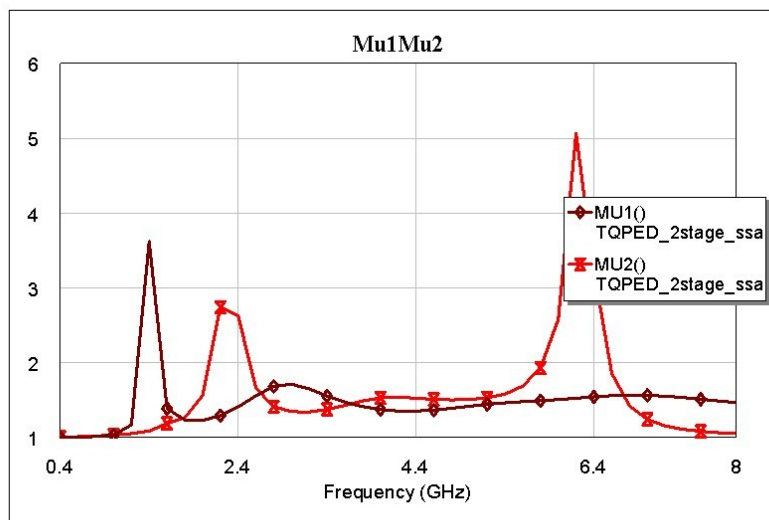


Figure 9 Stability.

Schematics

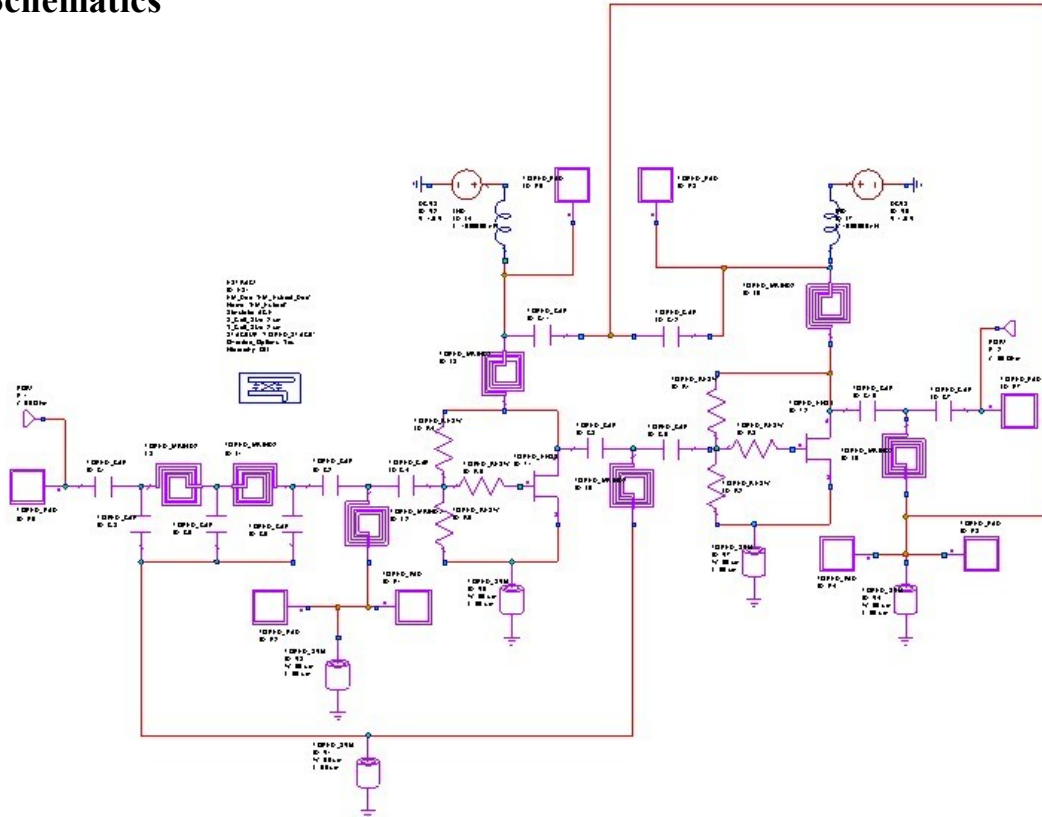


Figure 10 RF schematic.

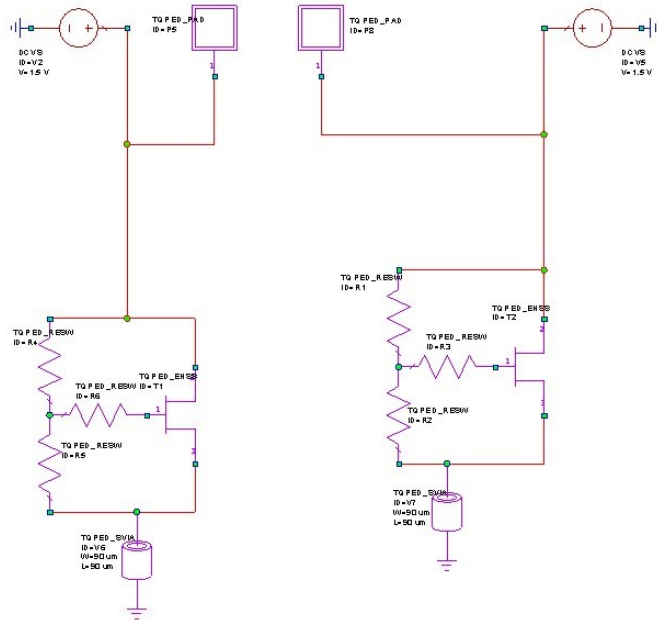
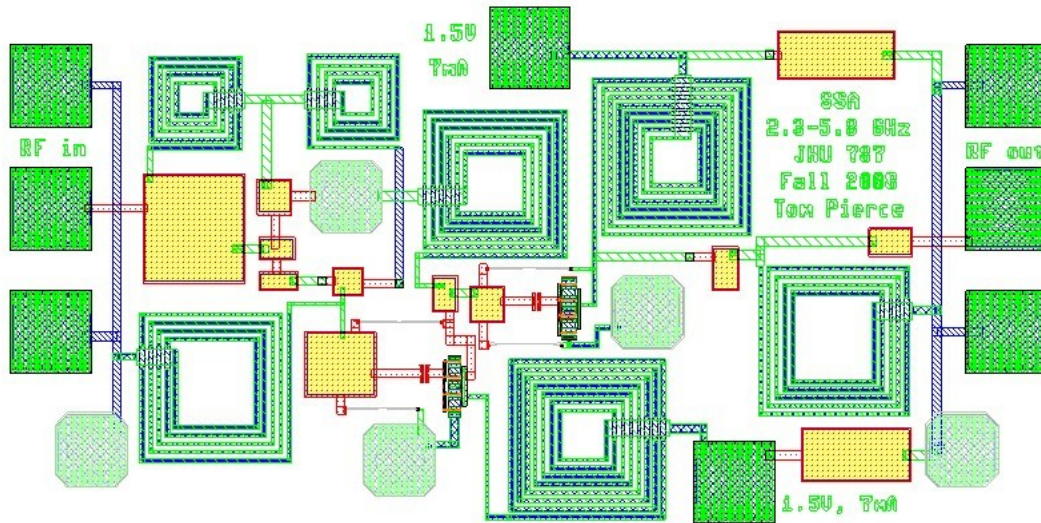


Figure 11 DC schematic.

Layout



Test Plan

After fabrication, the amplifier will be tested in lab and compared to the simulated results. The test equipment available includes the Agilent 8510 vector network analyzer, Cascade Model 43 wafer probe station with up to 4 RF probes and 4 DC needle probes, signal generators, and a spectrum analyzer. The steps to complete testing are the following:

S-Parameter Measurements

1. Power up the equipment.
2. Calibrate the network analyzer using open, short, thru, and load test fixtures.
3. Mount circuit on probe station and connect probes RF in, RF out, and both DC sources.
4. Set each DC supply to 1.5 volts and limit each current to 10mA.
5. Measure the s-parameters from 100 MHz to 8 GHz and note S21 at 2.305 GHz, 4 GHz and 5.875 GHz (see table below).
6. Save the s2p file.

IP3 Measurements

1. Note the power losses in the cables.
2. Connect the signal generator to the input of the device.
3. Connect the spectrum analyzer to the output of the device.
4. Connect and set the DC bias as above.
5. Set the frequency to 2.305 GHz and sweep the input power from -30 dBm to -10 dBm noting the output power at 2 dB intervals (see table below).
6. Repeat step 5 at 4 GHz.
7. Repeat step 5 at 5.875 GHz.

Gain		
Frequency (GHz)	Simulated (dB)	Measured (dB)
2.305	22.12	
4	24.09	
5.875	22.25	

Cable loss at input

Cable loss at output

Power			
Pin (dBm)	Pout (2.305 GHz)	Pout (4 GHz)	Pout (5.875 GHz)
-30			
-28			
-26			
-24			
-22			
-20			
-18			
-16			
-14			
-12			
-10			

Summary and Conclusions

This design of a broadband small signal amplifier is both low power and very small. Some minor modifications can be made to better the match and VSWR while being careful not to affect the gain ripple. There were no noise data in the TOM3 model of this device, but noise parameters should be looked into if this design is used for low noise applications. If noise is an issue, then the low pass filter can be moved to the output of the circuit to lessen its affect.

The only specification that clearly fails simulation is the output power at the 3dB compression point. This is the fault of the designer by mistakenly reading the wrong parameter throughout the design process. Other than that, the amplifier design shows effective use of the simulation tools and design techniques learned during the rf and microwave courses taught at JHU

Appendix

This page should be printed and brought to the lab during testing.

S-Parameter Measurements

1. Power up the equipment.
2. Calibrate the network analyzer using open, short, thru, and load test fixtures.
3. Mount circuit on probe station and connect probes RF in, RF out, and both DC sources.
4. Set each DC supply to 1.5 volts and limit each current to 10mA.
5. Measure the s-parameters from 100 MHz to 8 GHz and note S21 at 2.305 GHz, 4 GHz and 5.875 GHz (see table below).
6. Save the s2p file.

IP3 Measurements

1. Note the power losses in the cables.
2. Connect the signal generator to the input of the device.
3. Connect the spectrum analyzer to the output of the device.
4. Connect and set the DC bias as above.
5. Set the frequency to 2.305 GHz and sweep the input power from -30 dBm to -10 dBm noting the output power at 2 dB intervals (see table below).
6. Repeat step 5 at 4 GHz.
7. Repeat step 5 at 5.875 GHz.

Gain		
Frequency (GHz)	Simulated (dB)	Measured (dB)
2.305	22.12	
4	24.09	
5.875	22.25	

Cable loss at input

Cable loss at output

Power			
Pin (dBm)	Pout (2.305 GHz)	Pout (4 GHz)	Pout (5.875 GHz)
-30			
-28			
-26			
-24			
-22			
-20			
-18			
-16			
-14			
-12			
-10			

Design Description: C-Band, Class A, Power Amplifier

This document will describe the design from its initial concept to the final product, which will be a two stage power amplifier designed towards the following specifications:

<p>Power Source: 3.6 V Lithium Battery, it along with its specifications are shown to the right.</p>		<p>Soft LS 14250 3.6 Volt 1/2 AA Lithium Battery</p> <p>Specifications:</p> <table border="0"> <tr> <td>BM Part #:</td> <td>BAT-TL5101-S</td> </tr> <tr> <td>Voltage:</td> <td>3.6 Volt</td> </tr> <tr> <td>Capacity:</td> <td>1.1 Ah</td> </tr> <tr> <td>Type:</td> <td>Lithium</td> </tr> <tr> <td>Shipping Weight:</td> <td>0.03 Pounds</td> </tr> </table>	BM Part #:	BAT-TL5101-S	Voltage:	3.6 Volt	Capacity:	1.1 Ah	Type:	Lithium	Shipping Weight:	0.03 Pounds
BM Part #:	BAT-TL5101-S											
Voltage:	3.6 Volt											
Capacity:	1.1 Ah											
Type:	Lithium											
Shipping Weight:	0.03 Pounds											
<p>Frequency Band of Operation: 5.7 - 6.1GHz</p> <p>1-dB Compression Point: ≥ 0dB, relative to the input</p> <p>Power Gain at 1-dB Comp: 20dBm (100mW)</p> <p>Fundamental isolation: ≥ 10dBm</p>												

Given the gain requirements of the amplifier explained above, it will most likely be necessary to include two amplifier stages. The first stage will employ a PHEMT sized appropriately to drive the second stage which will be providing the bulk of the gain required. The simulations that will be needed to characterize the amplifier are detailed in Table 1 below:

Simulation Plan	
Stability:	MU1 and MU2 curves
	Stability Circles (Smith Chart Plot)
Non-Linear:	Harmonic Power Historesis Plots
	Output Power of the Fundamental Frequency examined over a range of input power levels
	Transient Output Voltage Waveforms at 1-dB and 3-dB Compression Points
	Power Added Efficiency
Linear:	S-Parameters (Rectangular and Smith Chart Plots)

Table 1

One of the issues that every power amplifier design has to deal with is supplying the amount of desired power to the load while keeping the current draw as low as possible. Because being able to supply 100mW to the load doesn't get you very much if

you have to change the supply batteries every twenty minutes. This issue can be mitigated by designing for the best possible power efficiency.

As this is a power amplifier design, I will start the design work on the 2nd stage which I will refer to as the power stage of the device. Once this stage is complete, I will concentrate my efforts on designing the 1st stage, which will be referred to as the driver stage. The gain of this stage should at the very least satisfy the following equation to meet the minimum design requirements:

$$G_{DriverStage,(dB)} = 20dB - G_{PowerStage,(dB)} \quad \text{Equation 1}$$

The 1-dB compression point should either be equal to or exceed that of the power stage. I've already mentioned that the power draw of the circuit is an important consideration, during the layout of the amplifier careful attention needs to be given to the metal trace widths and what their ratings are for the maximum current density. Table 2 below describes these ratings for this technology.

Layer Number	Layer Designation	Maximum Current Density (mA/um)
3	NiCr	1.0
51	HVR	0.15
5	Ohmic	NA
7	D-Mode Gate	1.0*
50	E-Mode Gate	1.0*
9	Metal0	1.5
15	Metal 1	9.0
17	Metal 2	18.0
23	MIM	NA

Table 2

Section I: The Power Stage

The first thing that needs to be done is to appropriately size a device to achieve the requirements. Being that the compression point and power gain called for in this requirements aren't that trivial, the device will have to made large enough to accommodate these parameters.¹ The amount of RF power capable of being generated from a transistor can be estimated from the device's IV-Curves. Equation 2 below describes the relationship.

$$P_{RMS} = \left(\frac{\Delta V}{2\sqrt{2}} \right) \left(\frac{\Delta I}{2\sqrt{2}} \right) = \frac{\Delta V \Delta I}{8} (watts)_{rms} \quad \text{Equation 2}$$

¹ The device sizes of the power and driver stages went through several iterations before the final dimensions were chosen. This document will only present the devices present in the final design.

Figure 1 below describes the schematic used to generate the IV-Curves for the device used in the Power Stage of the amplifier. The dimensions of the device shown are described in Table 3 to the left of the figure. The actual curves are shown in Figure 2 at the bottom of the page.

Power Stage PHEMT Parameters	
Device Type	D-Mode PHEMT
Fingers	12
Width of each finger	50 microns
Total Width	600 microns
Device Length	0.5 microns

Table 3

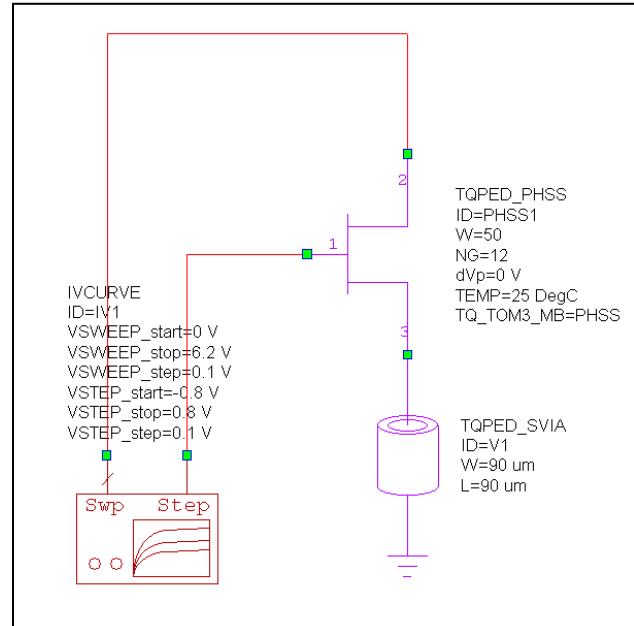


Figure 1

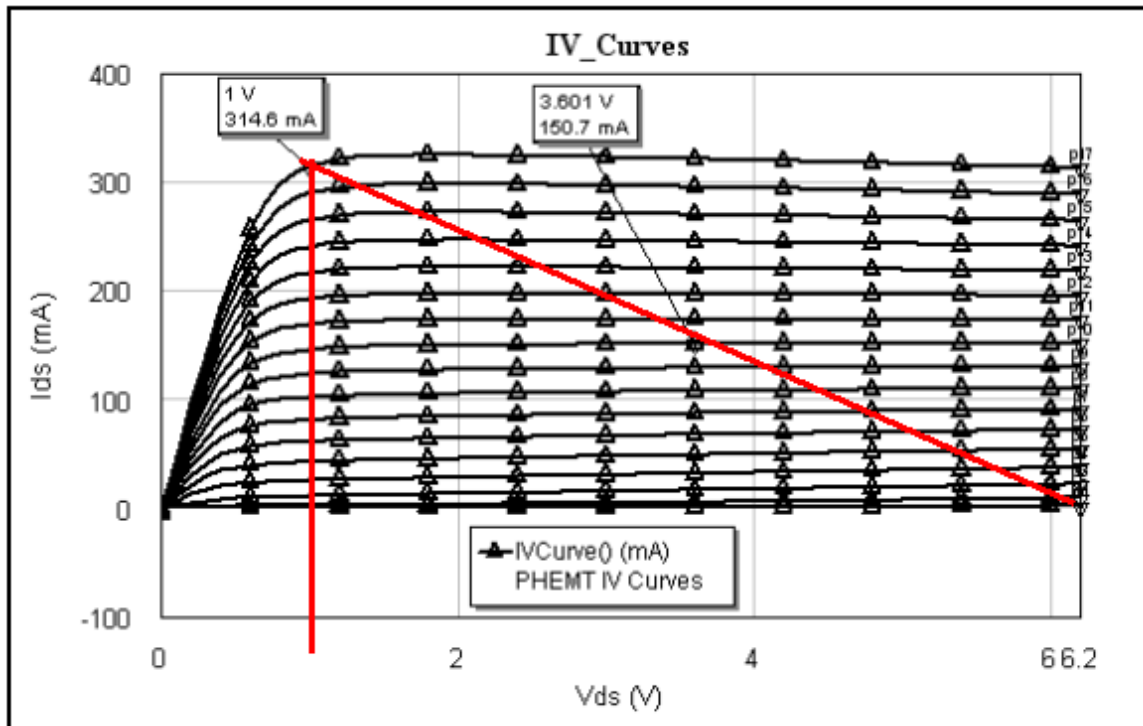


Figure 2

Referring to Equation 2 the values of ΔV and ΔI for this device are approximately 5.2 Volts and 320mA respectively. After substituting these values into Equation 2 and solving, we see that this device is capable of supplying 208mW, or 23.2dBm. The appropriate gate and drain voltages are 0 and 3.6-Volts respectively.

Since this is the power stage of the amplifier, it is appropriate to use the method developed by Steve Cripps in matching a 50- Ω port to the drain of this device. In the Cripp's method, we are conjugately matching to eliminate the C_{DS} while maintaining the R_{DS} value. Figure 3 below illustrates a circuit diagram of these components.

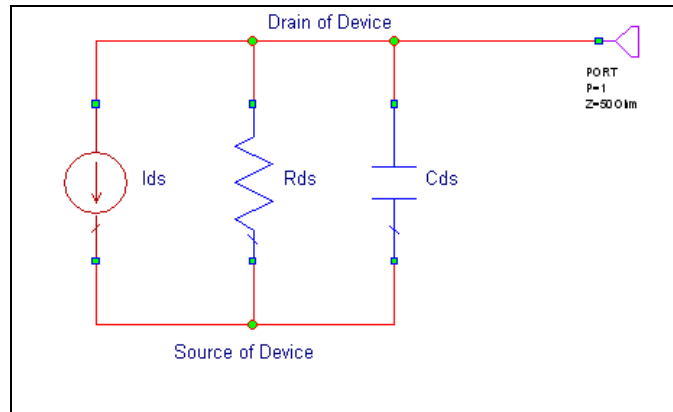


Figure 3

Since size and bias points of the device determine these values, we can approximate the R_{DS} value from the IV-Curves shown on the previous page.

$$R_{DS} = \left(\frac{5.2V}{0.32A} \right) = 16.25\Omega$$

C_{DS} can be approximated by inspecting the S_{11} Smith Chart plot for the device.

$$S_{11} = (3.15 - 15.5j)\Omega$$

Extrapolating from this value we can approximate C_{DS} to be 1.75pF. As this is a fairly large device, this value is pretty reasonable. The very first measurement that I've chosen to look at is the stability of the device. While it's true you can address the stability of a circuit at any point in the design cycle, it is best to address it up front. This will reduce the possibility of needing to put in additional circuitry after you've spent time matching to the ports. Figure 4 on the next page describes the preliminary schematic and simulation of the stability.

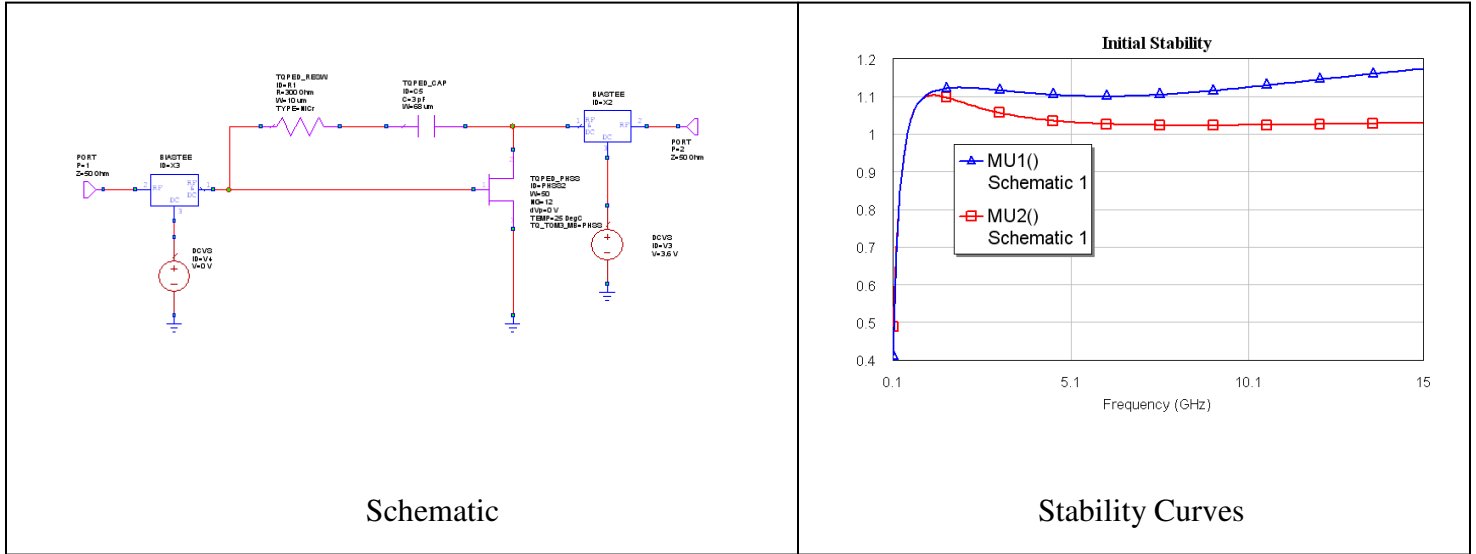


Figure 4

Although the stability is conditionally unstable from 100MHz to 500MHz, it may become unconditionally stable after the matching circuitry is added. I will re-visit this at the end of this section. The feedback capacitor's purpose is to serve as a DC blocker to prevent any unnecessary current at the gate.

The next step is to begin matching to the output of the device using the Cripp's Method. The table below describes the simulated S_{22} value at 5.9GHz, and the Z_{Cripps} value superimposed on this value. In this case, the Z_{Cripps} and S_{22} values are not coincident. It is the Cripp's resistance value that I will match the output of this circuit to.

$S_{22} = (46.2 + 5.3j)\Omega$
$Z_{Cripps} = (16.25 + 5.3j)\Omega$

The output matching circuit has been designed with a Smith Chart program. Figure 5 below describes this matching circuit.

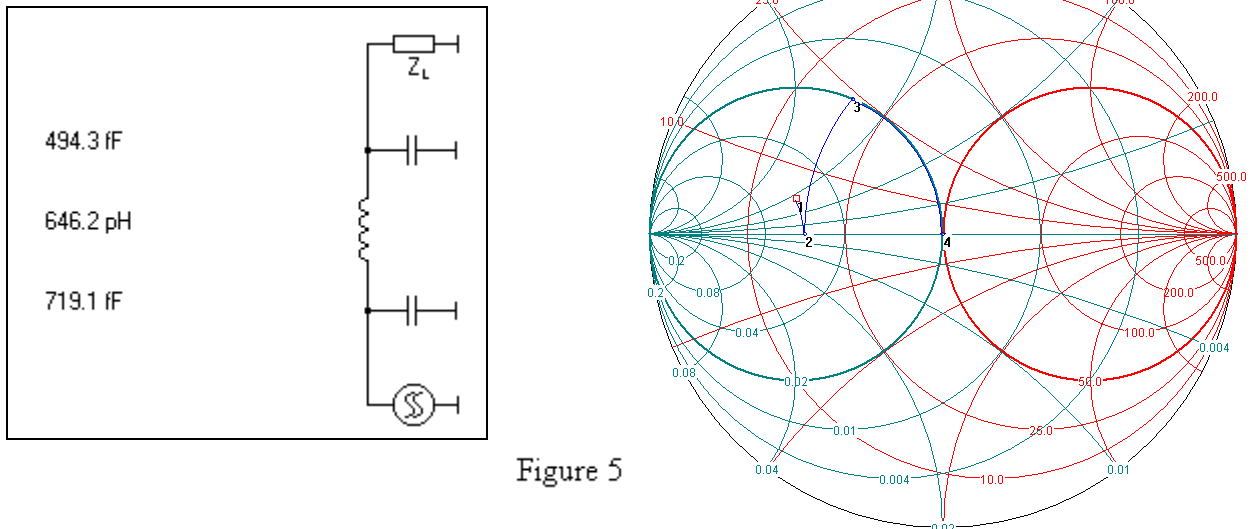


Figure 5

The input port has to be matched as close to 50Ω as possible, S_{11} was simulated to the following value at 5.9GHz.

$$S_{11} = (7.85 - 18.2j)\Omega$$

As luck would have it, the only component needed to supply a match to 50Ω is a single shunt inductor. Figure 6 below describes this.

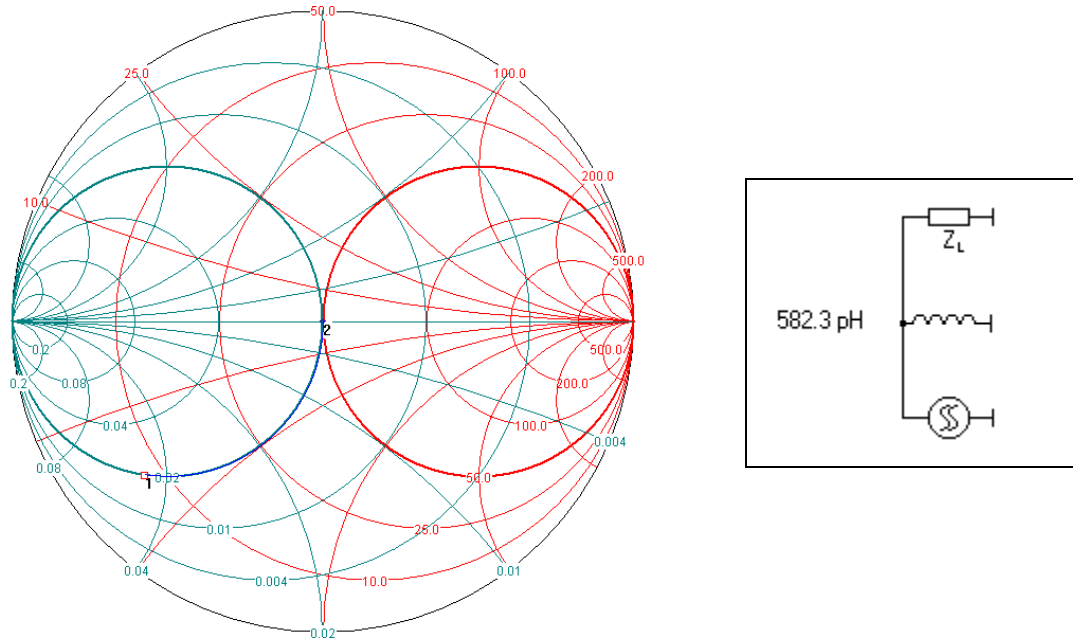


Figure 6

The finalized ideal schematic can be found in Figure 7 at the bottom of this page.

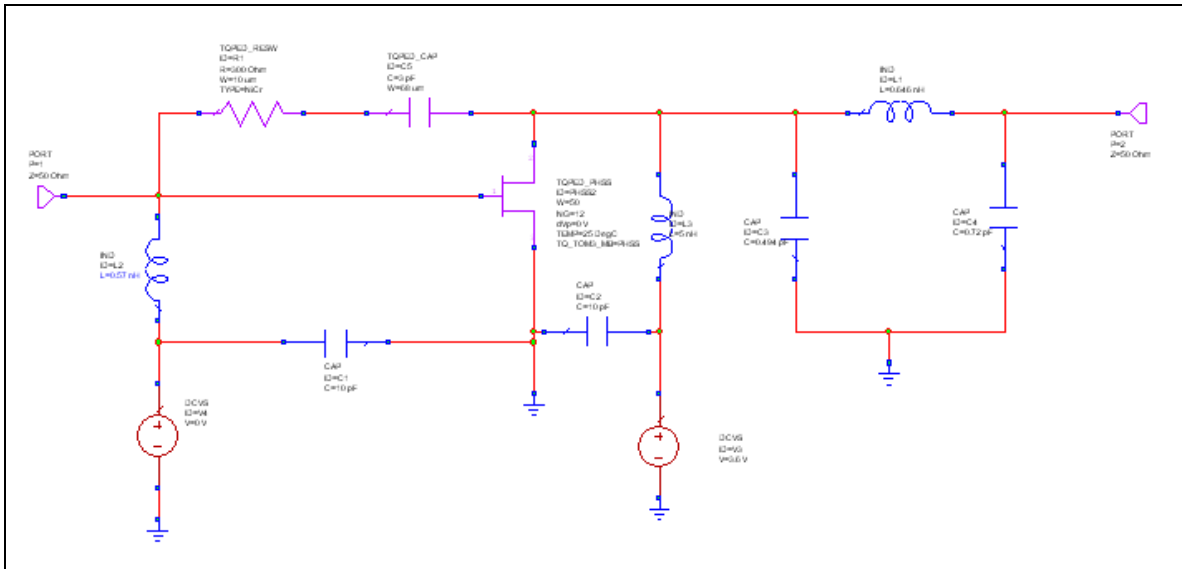


Figure 7

The following follow the simulation plan laid out in Table 1 found on the first page of this document.

Non-Linear Simulation Results:

Fundamental, 2nd, and 3rd harmonic power levels at 5.9GHz with an input power level of 0dBm.

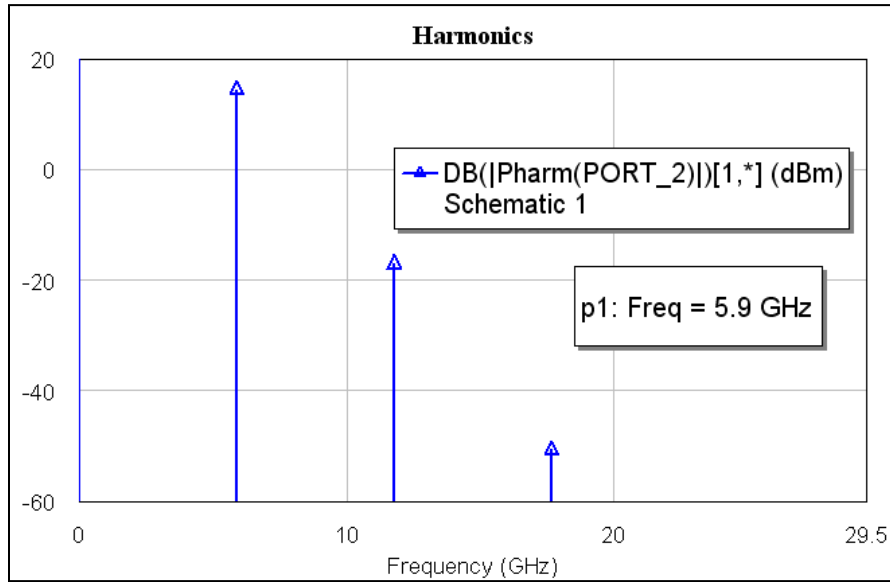


Figure 8

Clever analog design tricks might make it possible to boost the gain up to 20dB, but this would introduce more passive components which might destabilize the device. Since the real estate is available on the die, so rather than go this route I've decided to simply add an additional stage. Figure 9 below describes the 1- and 3-dB compression points. Power Added Efficiency and the output voltage waveforms are presented on the next page in Figures 10 and 11.

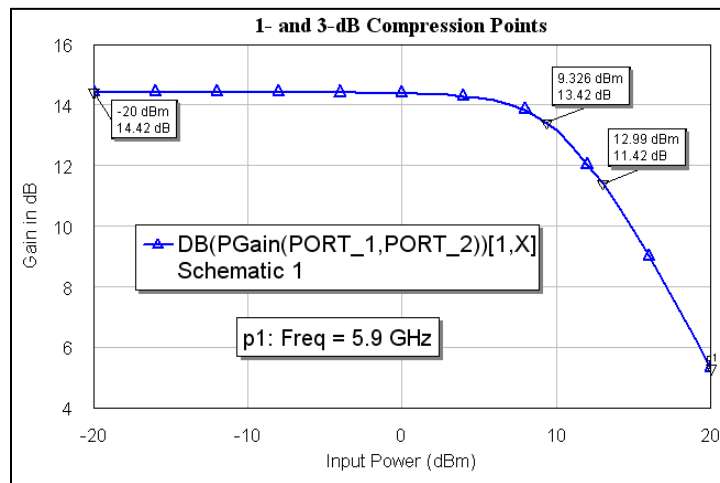


Figure 9

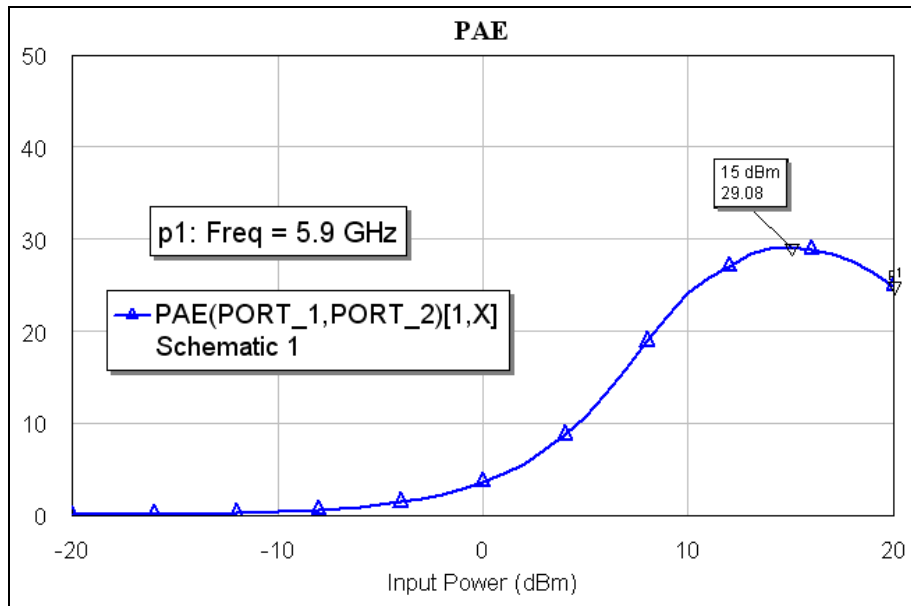


Figure 10

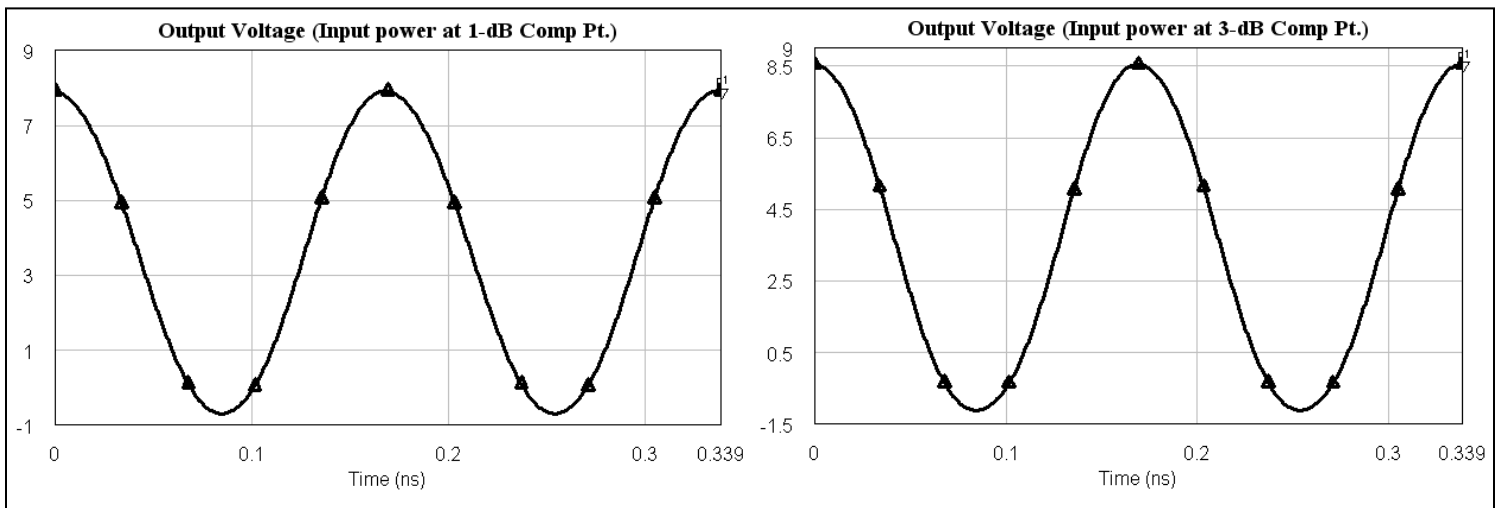


Figure 11

Although the waveform at the 3-dB compression point looks extremely well behaved, recall that this is for an ideal circuit. Upon closer inspection, there is a very small amount of ripple in the waveform, but not much. I expect these graphs to look much more realistic after the non-ideal elements are inserted and the two stages are put together.

Linear Analysis of the Power Stage:

The S-Parameters of the circuit shown in Figure 7 are presented on the next page. The specific points that have been called out are characterizing the target bandwidth of the system from 5.6GHz to 6.1GHz.

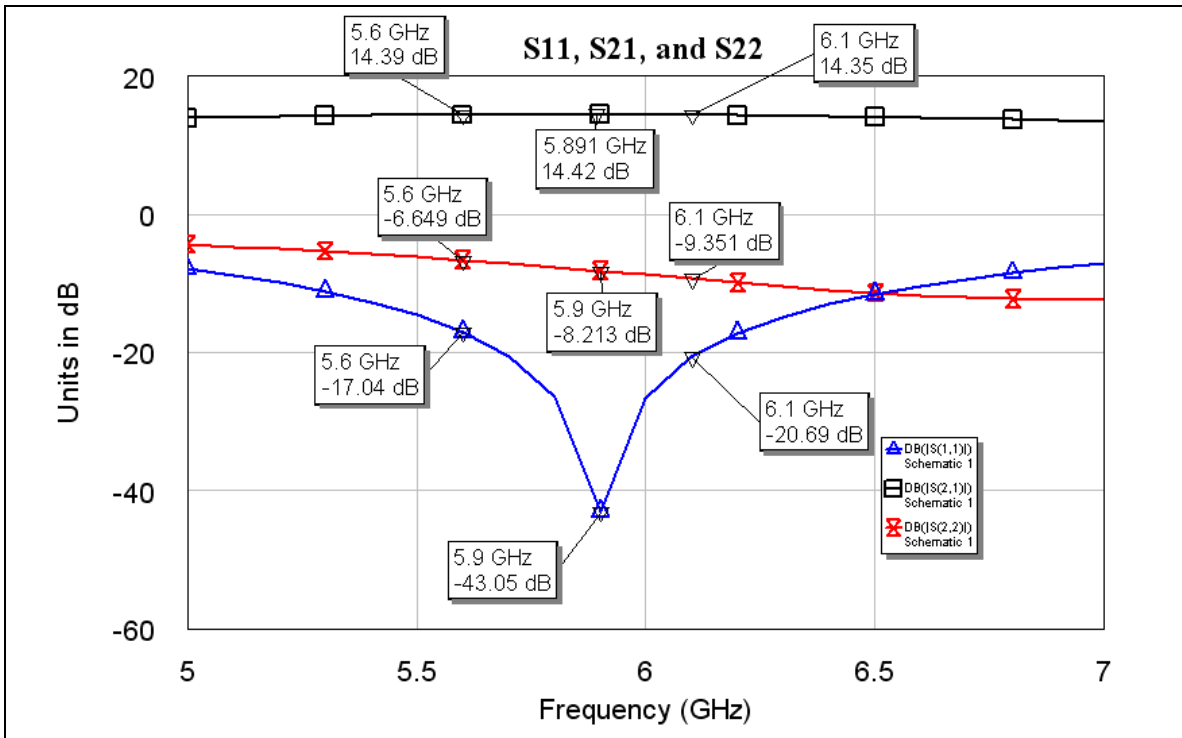


Figure 12

As suspected, the instability problems corrected themselves after the matching circuitry was added. Figure 13 below describes the MU curves again.

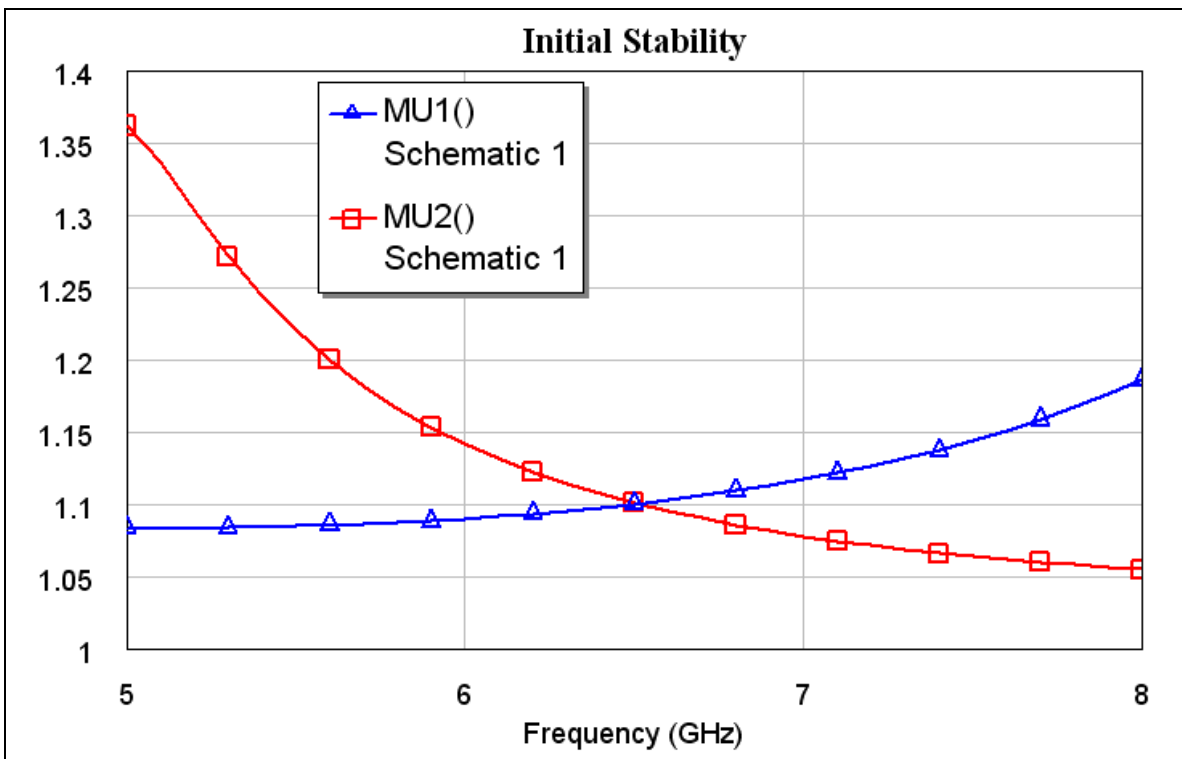


Figure 13

In order to reduce the size of this document, all of the non-ideal elements and back annotated simulations will be presented in Section III of this document, which describes the final circuit.

Section II: The Driver Stage

The method to design the driver stage is different from that of the power stage as its purpose is altered. Both ports of this stage will be matched to 50Ω , this is similar to the method one would use in designing an SSA. I will match the input of this device first, as the critical matching element here will be the output of this stage. I want there to be as little reflection as possible between the input of the power stage and the output of the driver stage.

The device dimensions chosen for this stage are shown below in Figure 14.

Driver Stage PHEMT Parameters	
Device Type	D-Mode
Fingers	2
Width of Each Finger	130 microns
Total Width	260 microns
Device Length	0.5 microns

Table 4

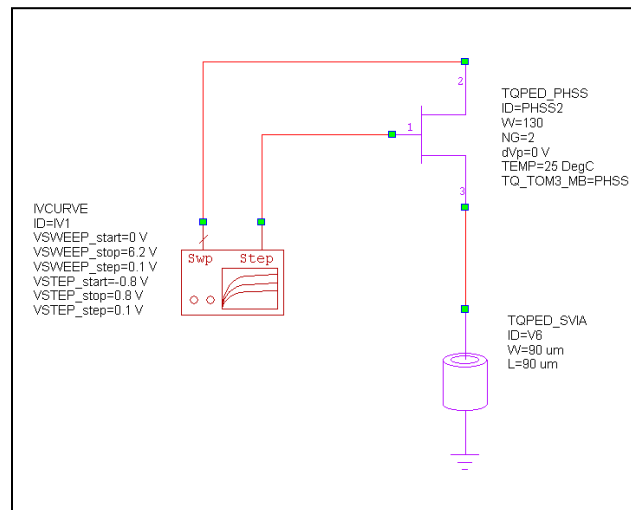


Figure 14

The IV-Curves for this device are shown on the following page. The bias point will again be chosen to ensure the largest current and voltage swings possible. As can be seen in Figure 15 the approximation for ΔV and ΔI are 5.2 Volts and 140mA. Therefore the approximate maximum output RF power can be found using Equation 2 again.

$$RF_{Power} = \left(\frac{\Delta V}{2\sqrt{2}} \right) \left(\frac{\Delta I}{2\sqrt{2}} \right) = 91mW$$

$$RF_{Power,dBm} = 10\log(91mW) = 19.6dBm$$

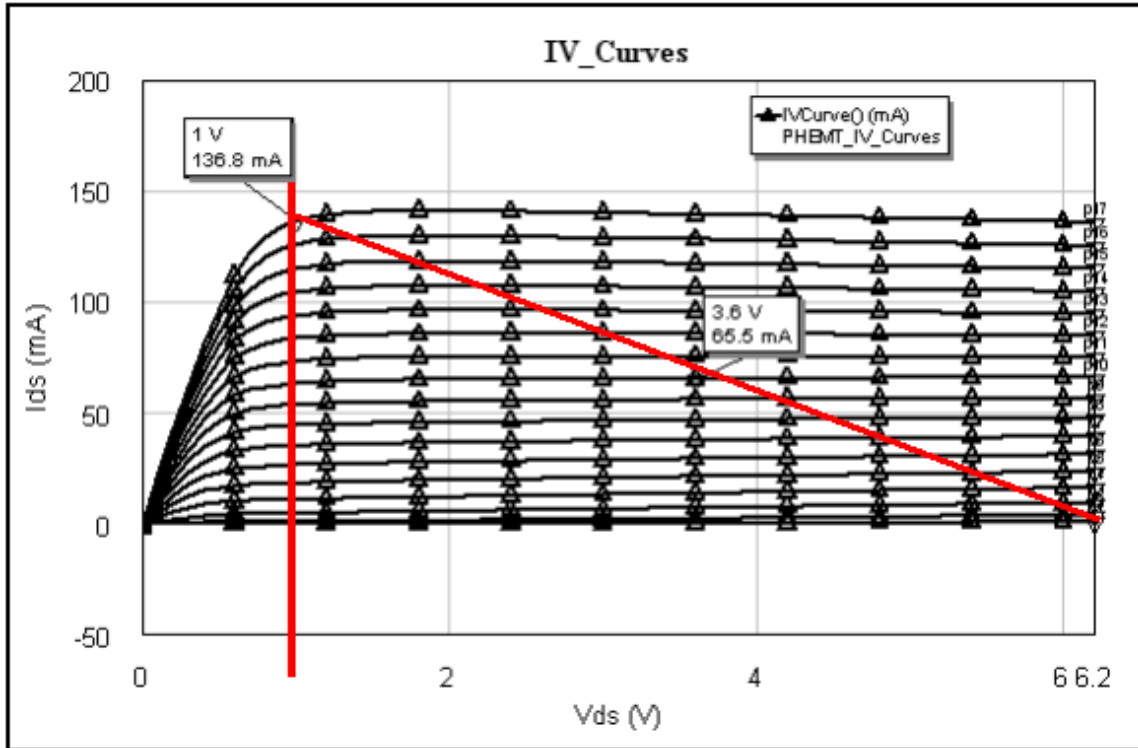


Figure 15

I'm using the same feedback technique for this stage as I employed for the power stage, and as before I will check the stability after I've added the matching components to ensure I am unconditionally stable. Figure 16 below describes the final ideal schematic designed for this stage.

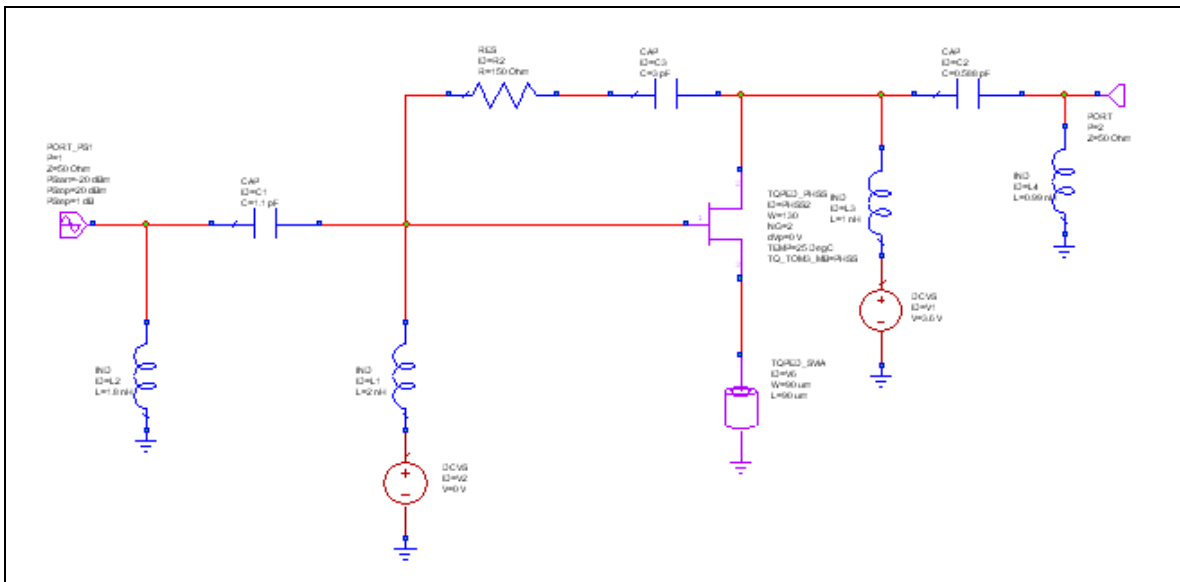


Figure 16

Non-Linear Simulations:

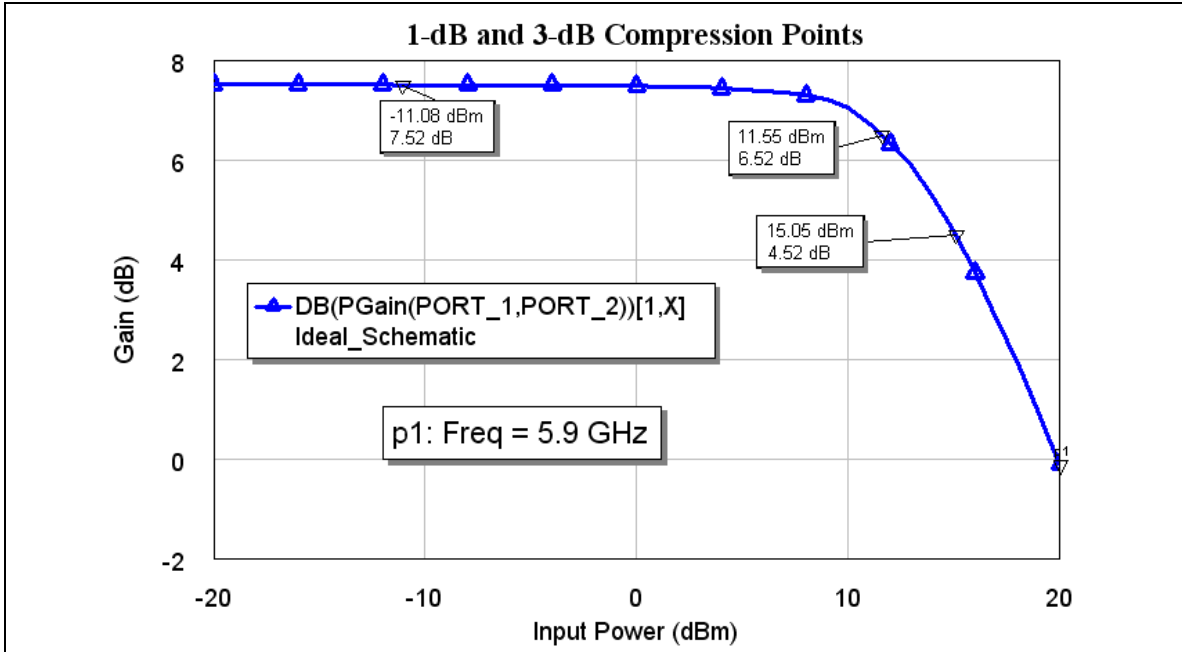


Figure 17

Comparing this graph to Figure 9, we can see that this stage compresses at a higher input power than the power stage does. Figure 18 below describes the harmonics for this stage.

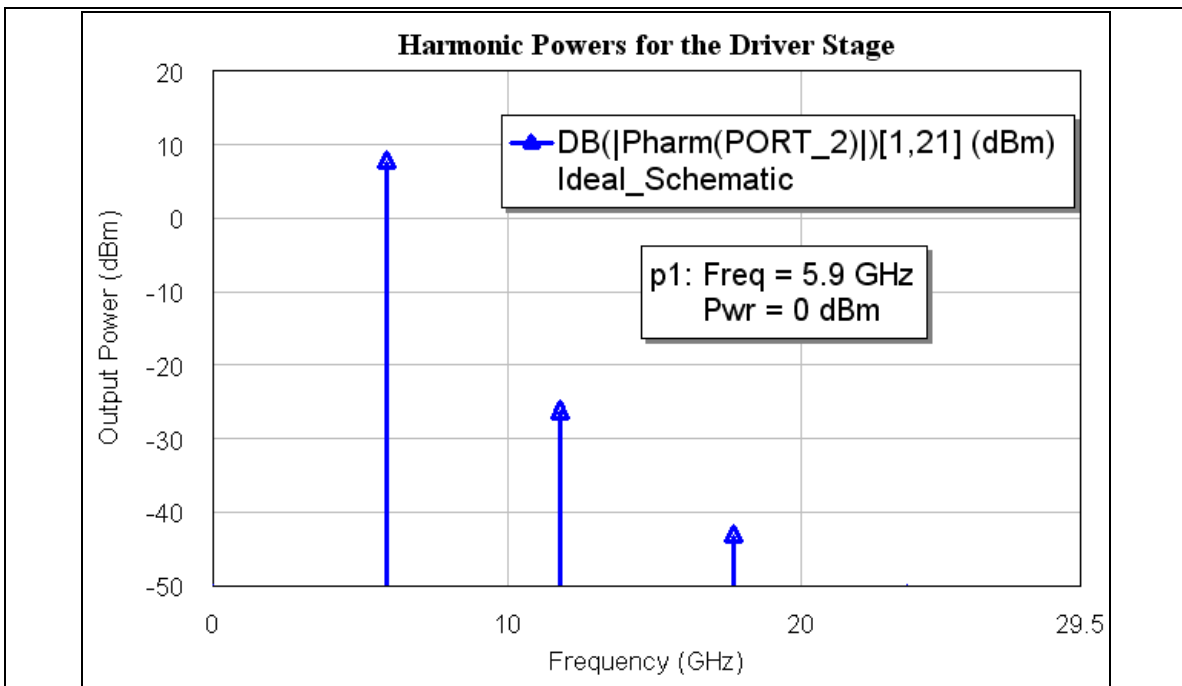


Figure 18

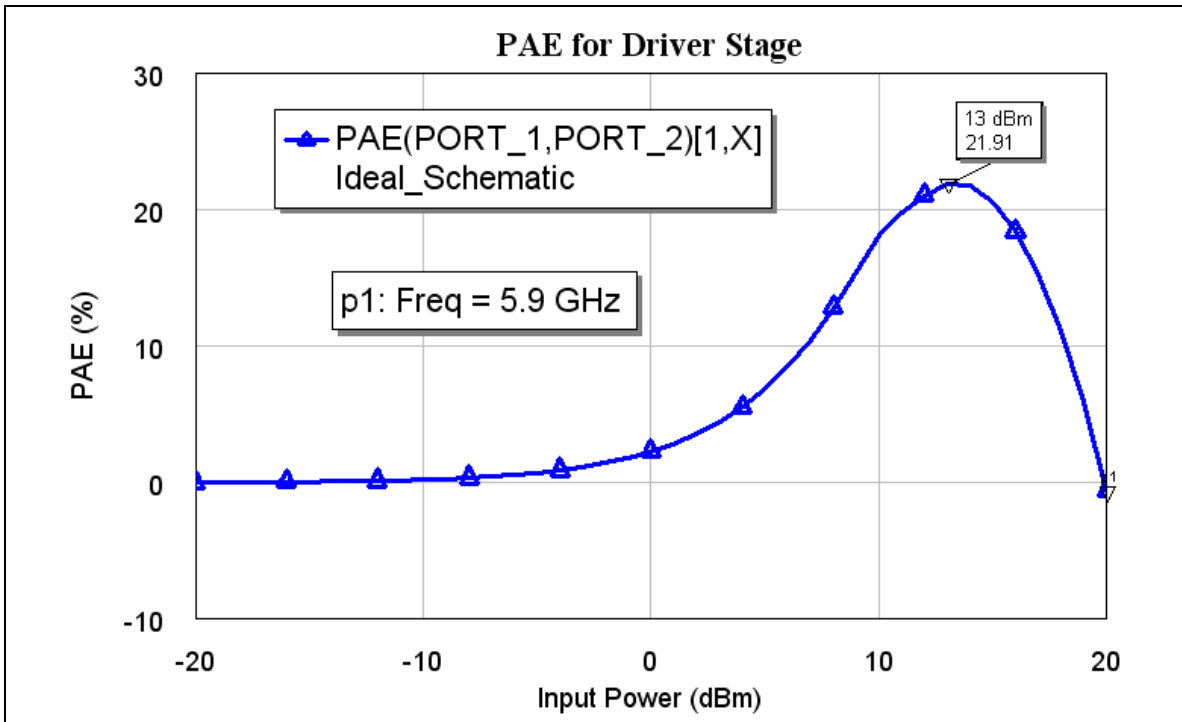


Figure 19

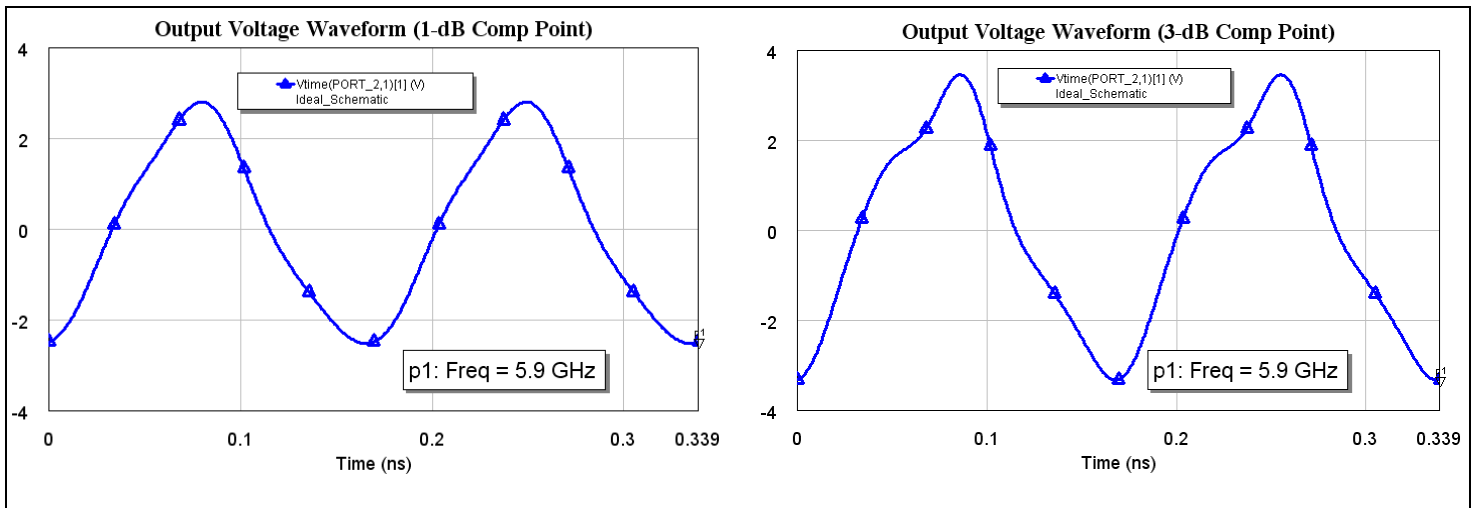
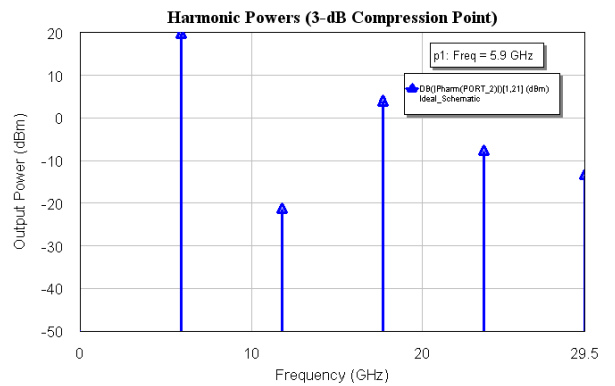


Figure 20

The harmonic distortion is much more prevalent in this stage than it was in the power stage. The figure to the right describes the harmonic powers associated with the first 5 harmonics. There is only about 15dB of isolation between the fundamental and the 3rd harmonic, which would cause this type of behavior.



Linear Simulations:

Figure 21 below describes the S-Parameters for this stage.

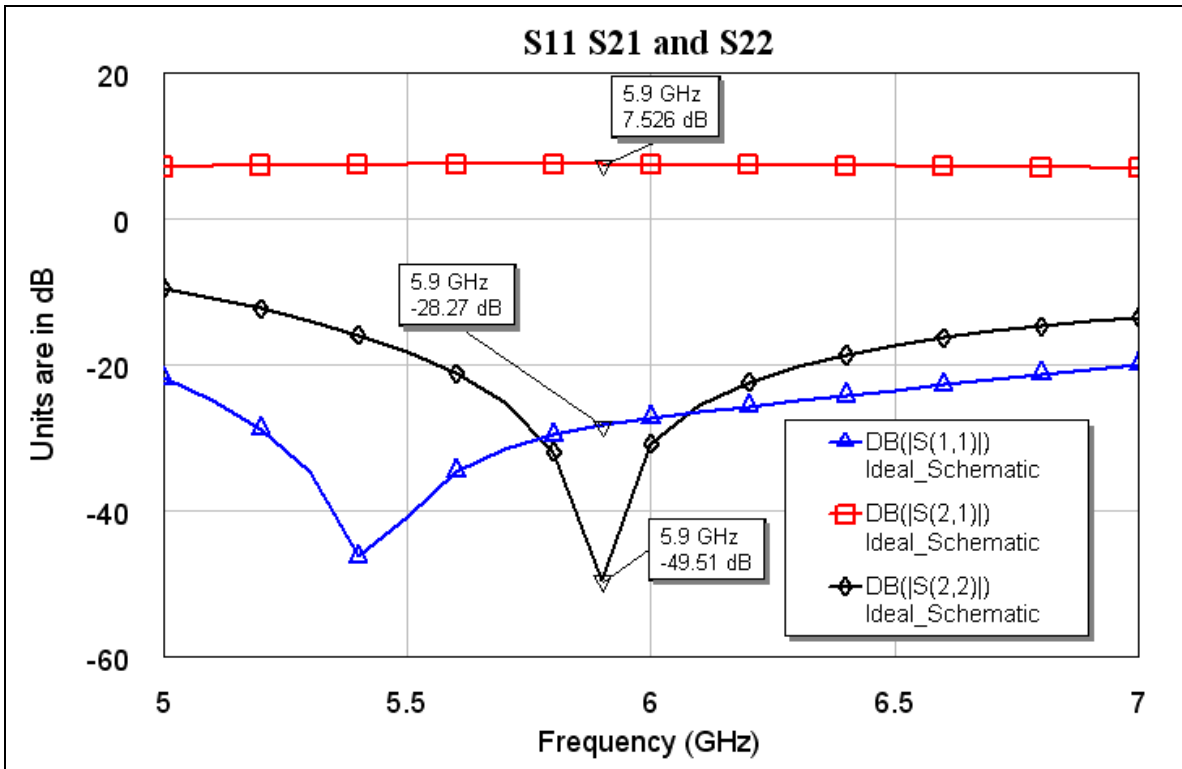


Figure 21

And finally, the stability shows that this stage is unconditionally stable.

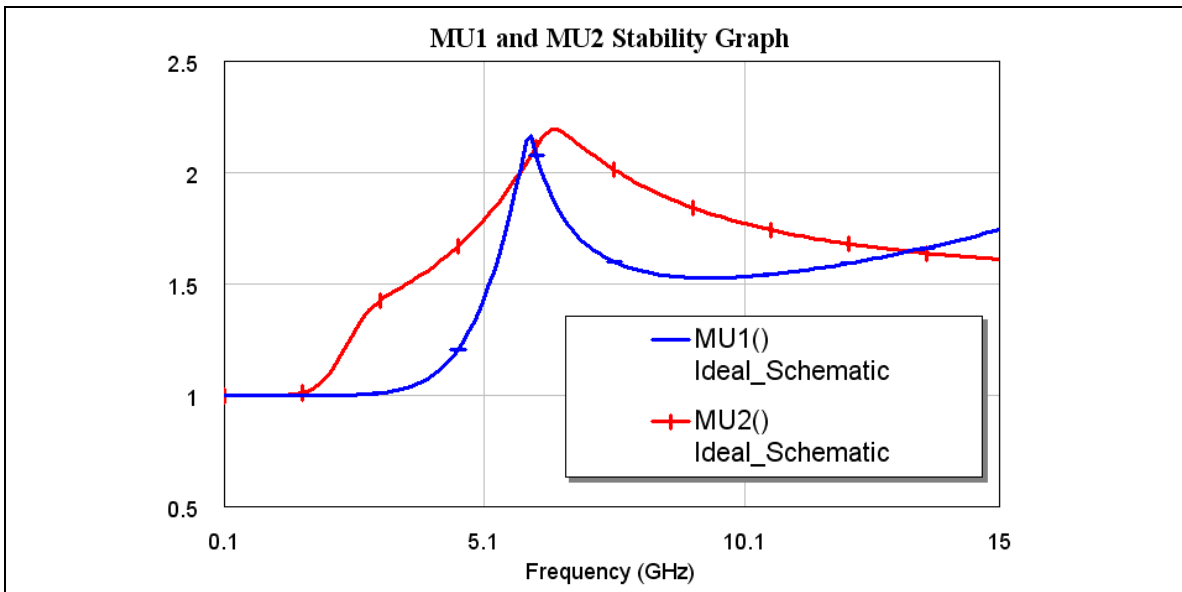


Figure 22

Section III: Putting it all together

Figure 23 below describes the final schematic of the C-Band amplifier. After examining the currents present at the gates of the transistors, I decided it would be prudent to go back and design in DC-Blocking capacitors in the feedback chains present in each stage.

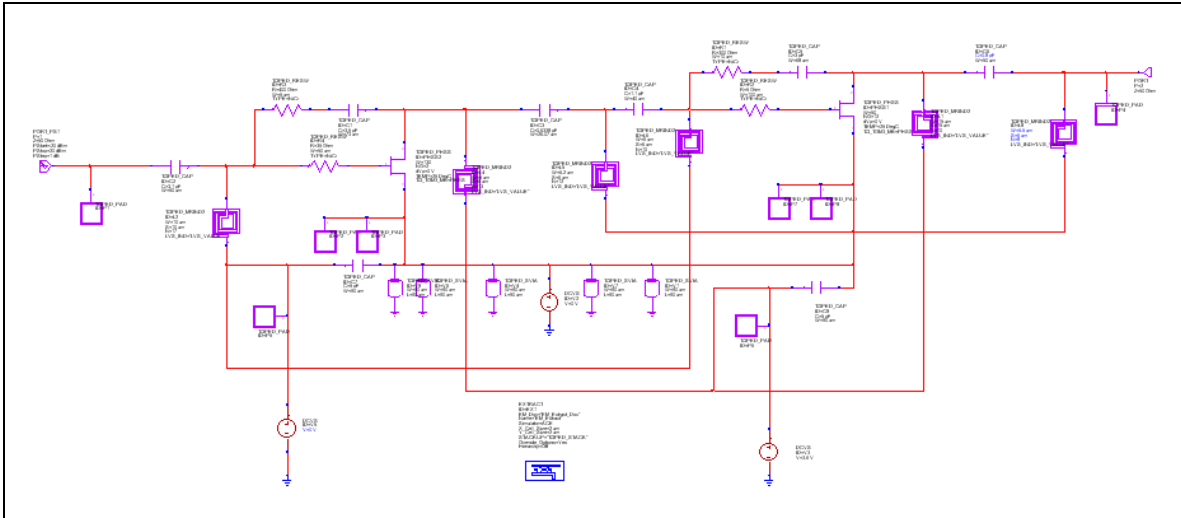


Figure 23

The final layout is presented in Figure 24 below.

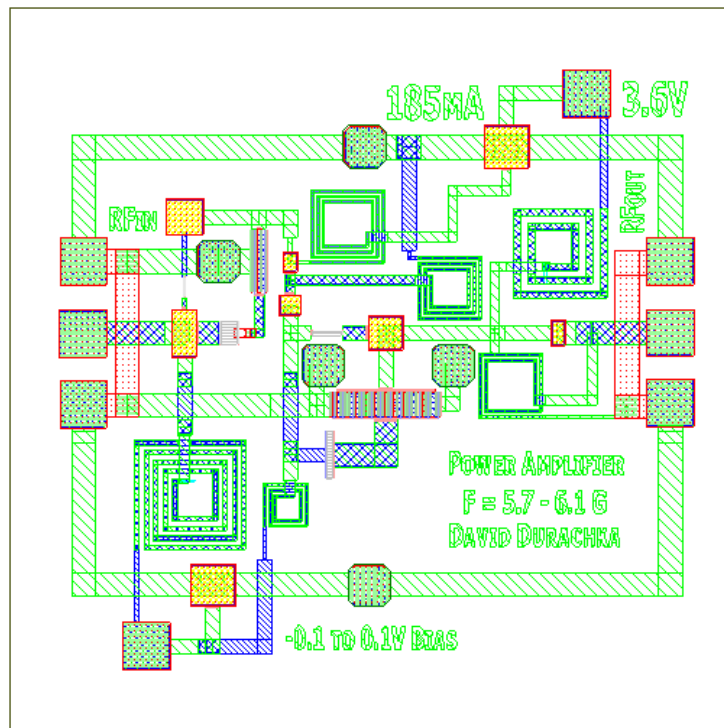


Figure 24

As can be seen in Figure 23 on the previous page, some changes were made to the 1st and 2nd stages. The most notable are the addition of the isolation capacitors at the input, inter-stage coupling, and at the output. Since I am biasing the PHEMT devices internally, these capacitors serve as DC-Blockers to ensure the bias points don't change. Also, some of the inductors were made larger to handle the current densities.

Table 5 below describes the physical and electrical characteristics of the amplifier.

Amplifier Physical Characteristics	
Layout Size	1330um x 1270um
Number of Pads	8 pads
Number of Substrate Vias	5 vias
Amplifier Electrical Characteristics	
Power Consumption	0.67W
Power Gain @ 0dBm Input	20.8dB
Max PAE	32.22%
1-dB Comp Point (Input)	0.2dBm
3-dB Comp Point (Input)	4.1dBm

Table 5

The following figures describe the back-annotated simulations run on the final version of the amplifier. Again, I am using the simulation plan that I laid out in Table 1 of this document.

Stability:

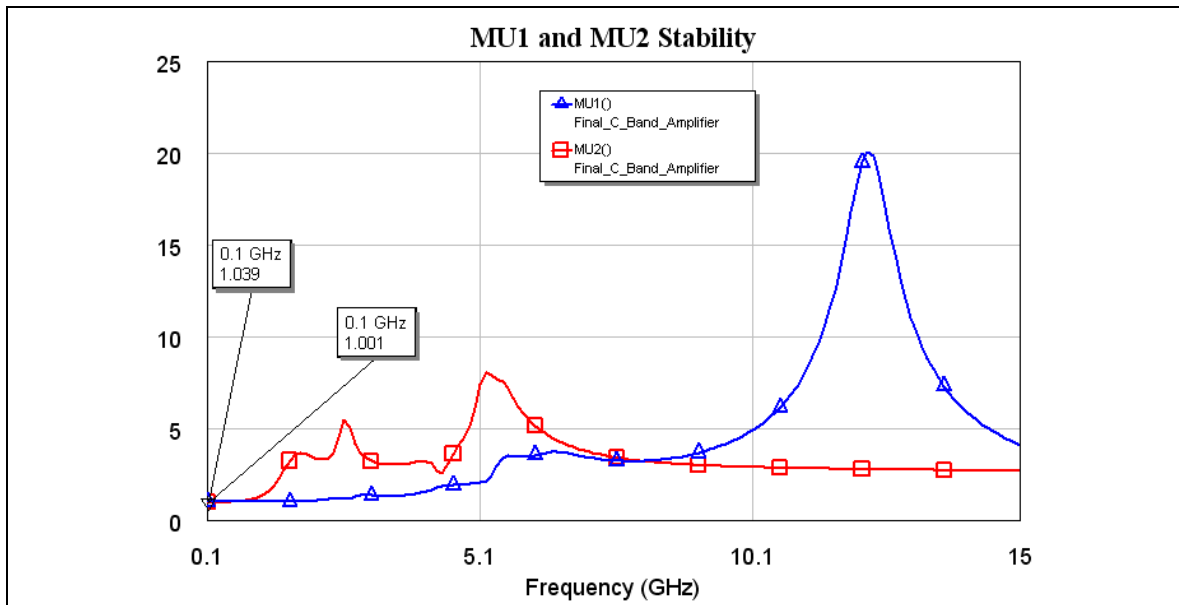


Figure 25

Non-Linear Simulations:

The following graphs show the non-linear behavior of the amplifier across the frequency band of interest. Measurements were taken at 5.7GHz, 5.9GHz, and 6.1GHz. Figure 26 below describes the 1-dB and 3-dB compression points of the system.

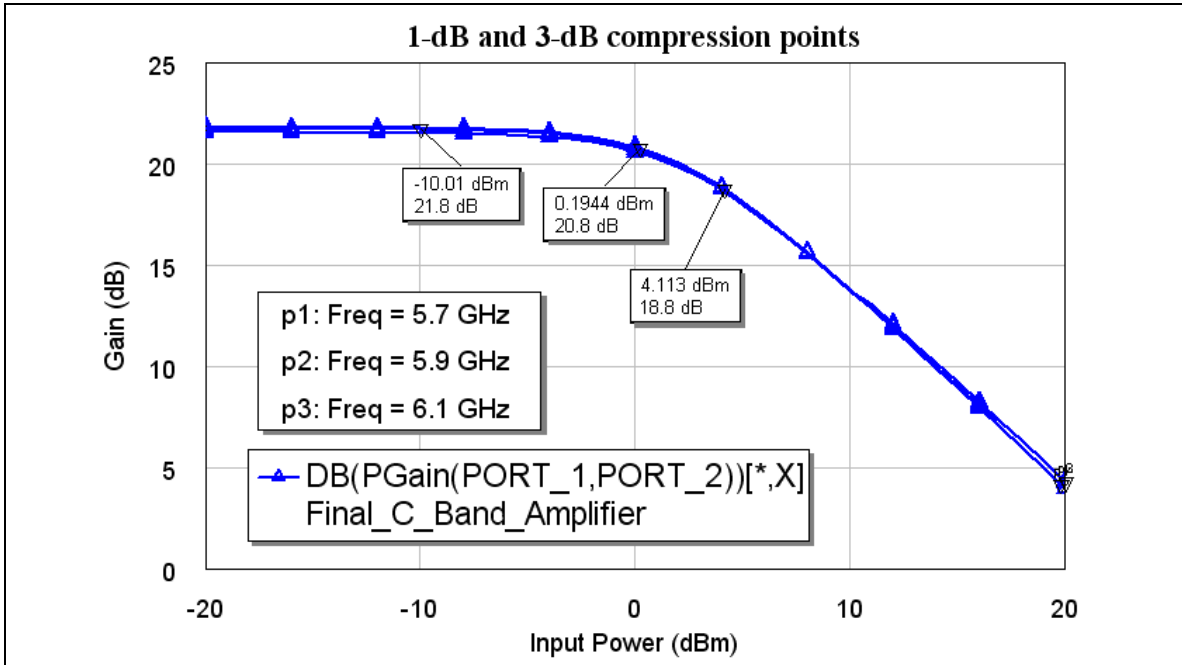


Figure 26

The next series of graphs show the behavior of the Harmonics at the same frequencies. Figures 28 – 30 were included as it is useful to see the behavior of the harmonics over a broad power range. The histogram below describes the behavior with in input of 0dBm.

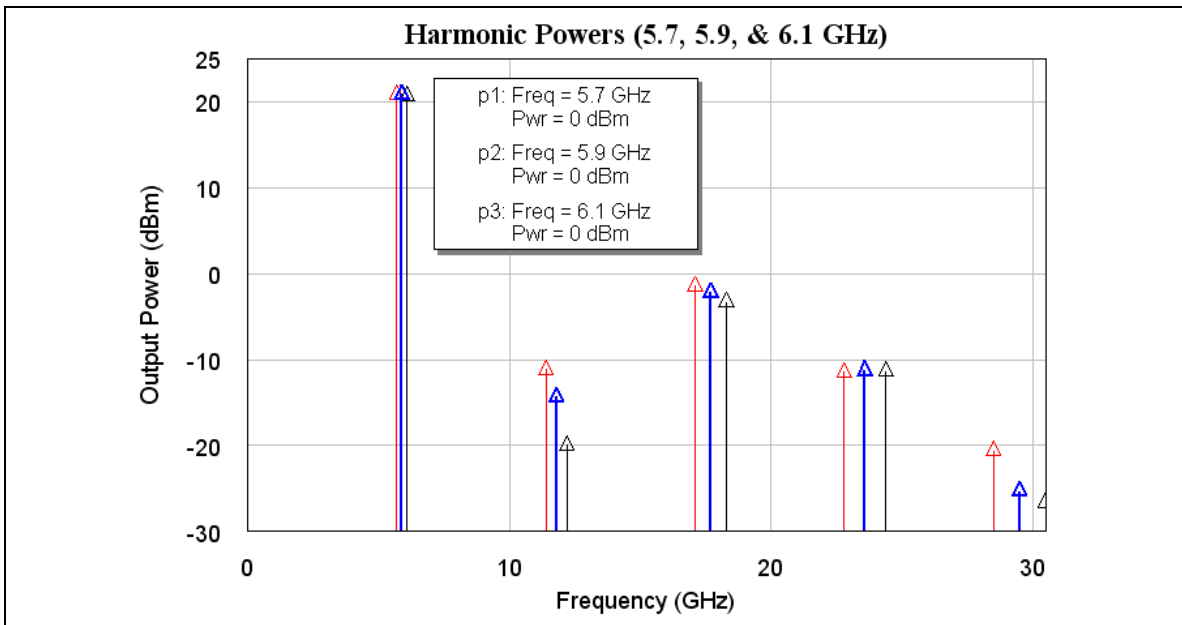


Figure 27

Fundamental = 5.7 GHz

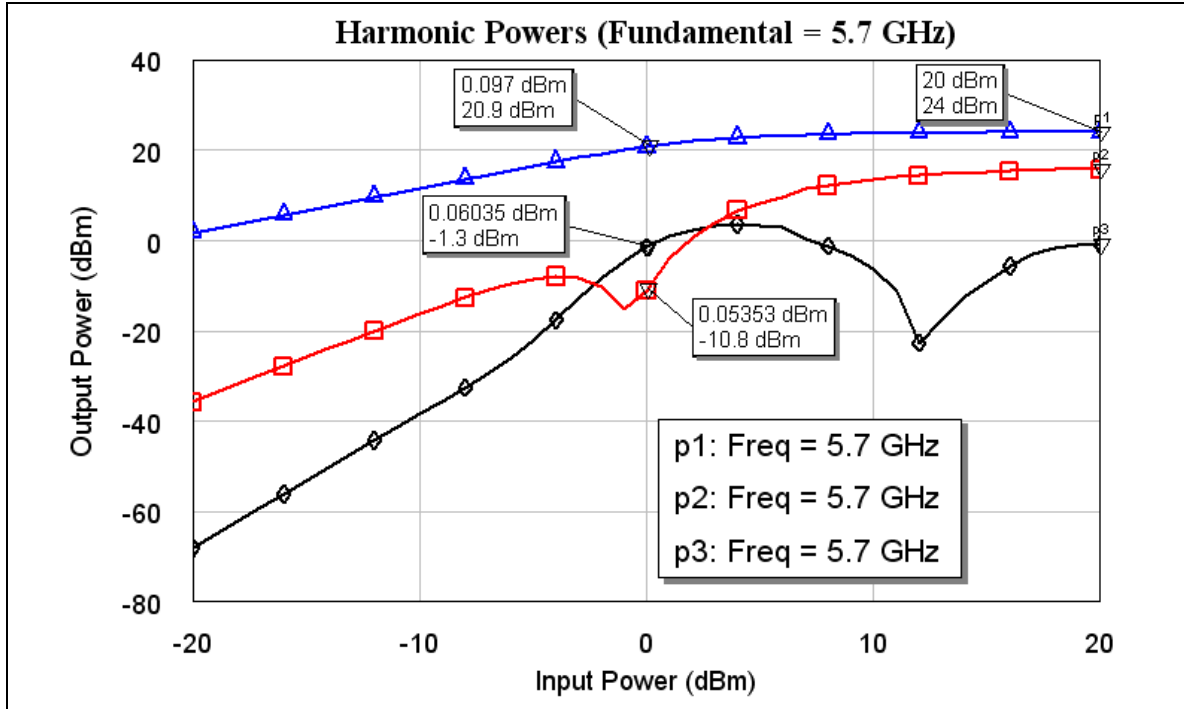


Figure 28

Fundamental = 5.9 GHz

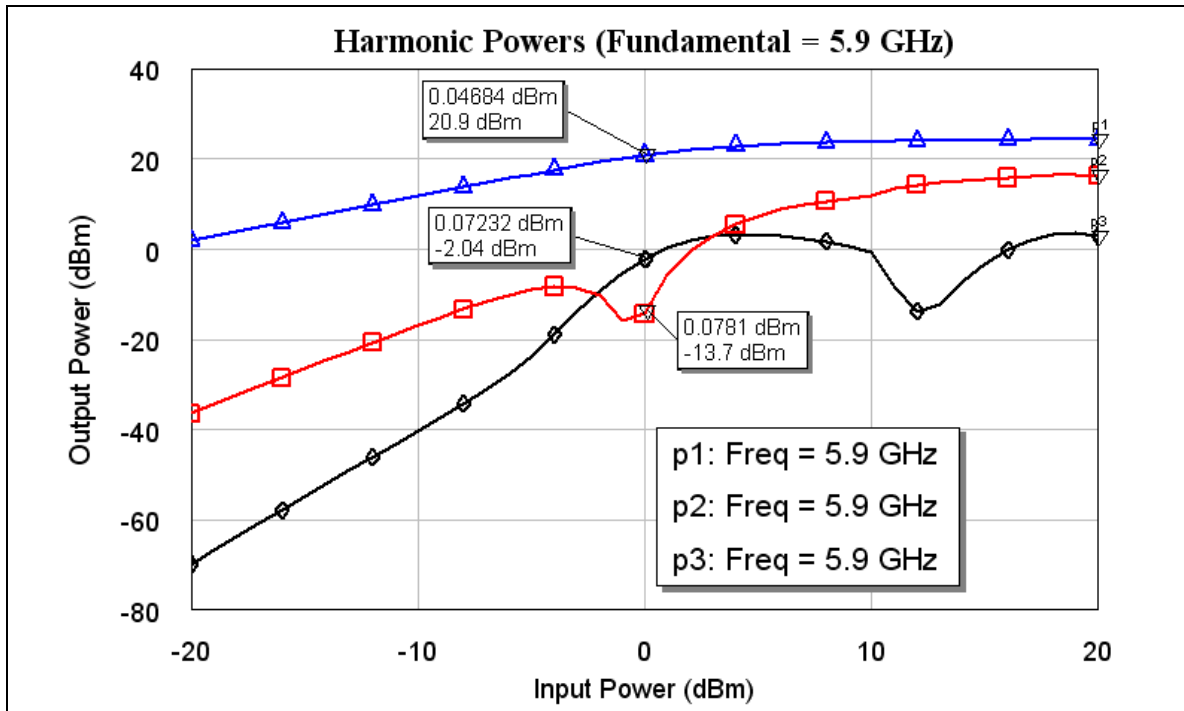


Figure 29

Fundamental = 6.1 GHz

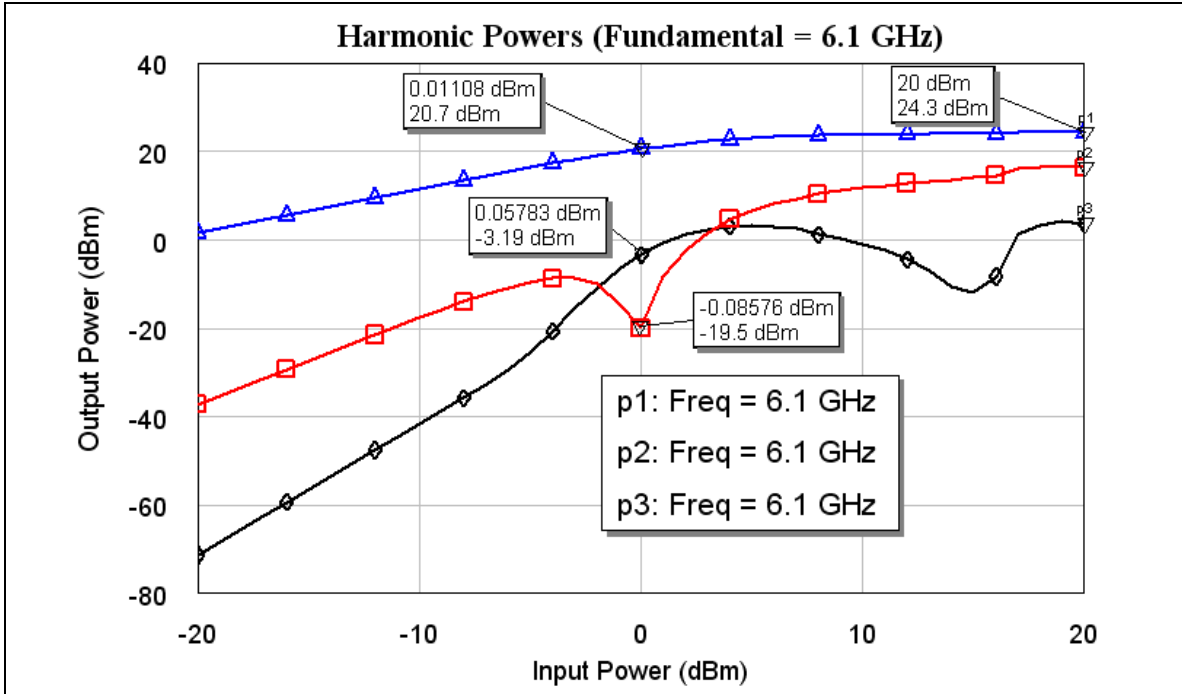


Figure 30

Figure 31 below describes the PAE at these same frequencies.

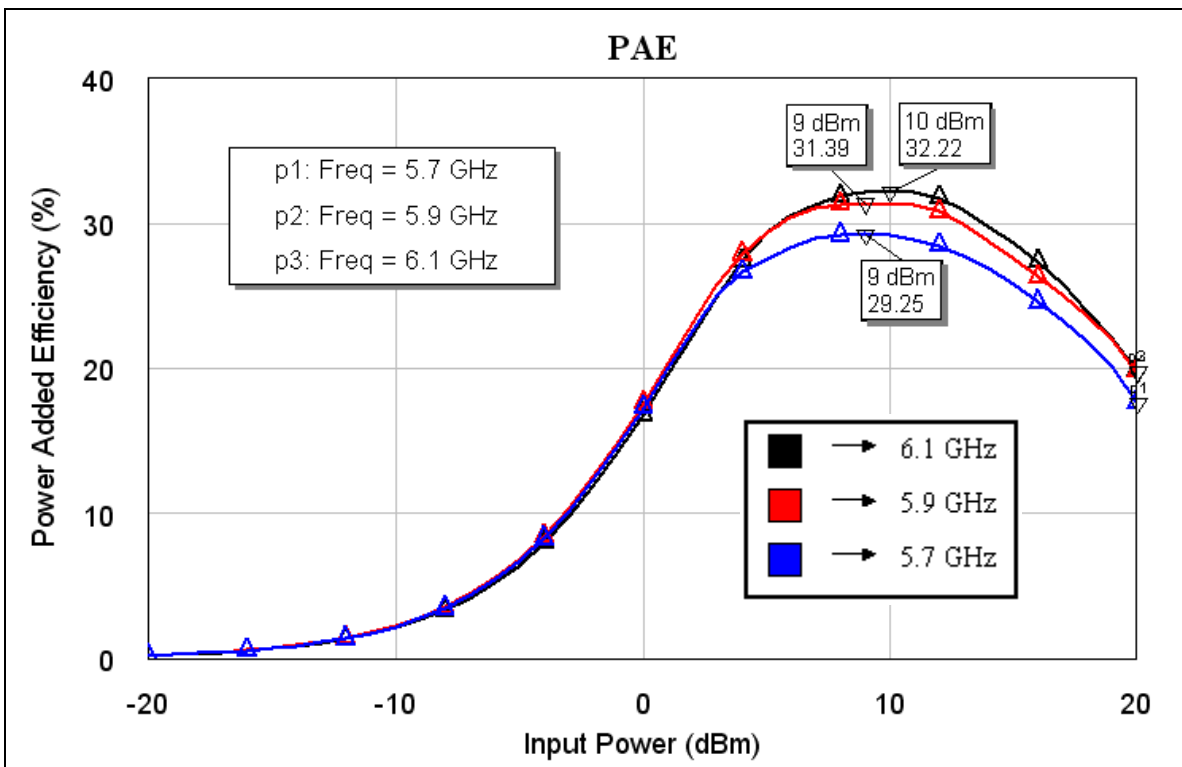


Figure 31

Finally, Figure 32 below describes the output voltage waveforms at the 1-dB and 3-dB compression points at 5.9GHz. These waveforms are centered about 0-volts due to the DC-Blocking capacitors used.

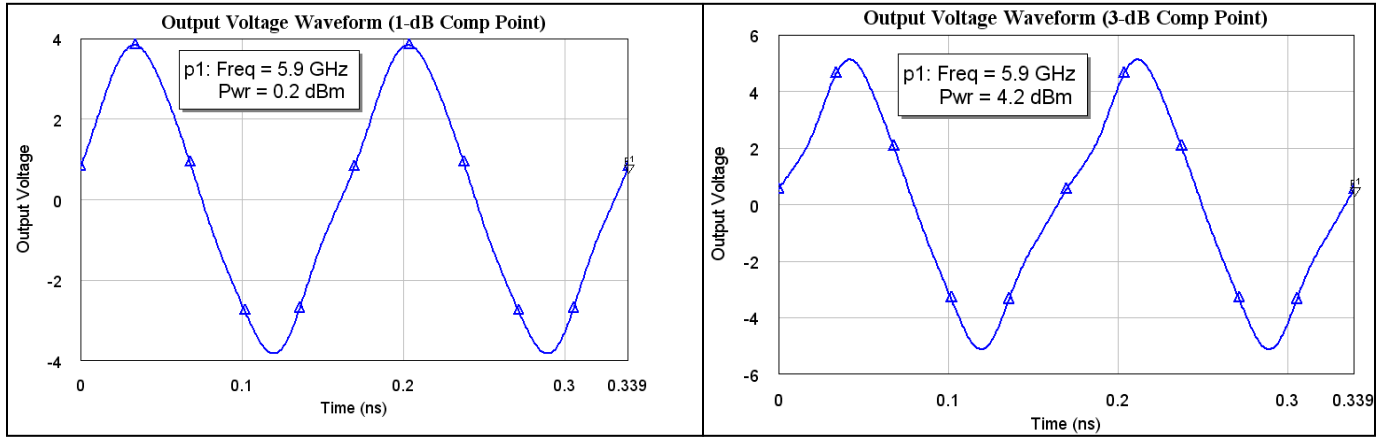


Figure 32

Linear Simulations:

Figure 33 below describes the S-Parameters of the amplifier.

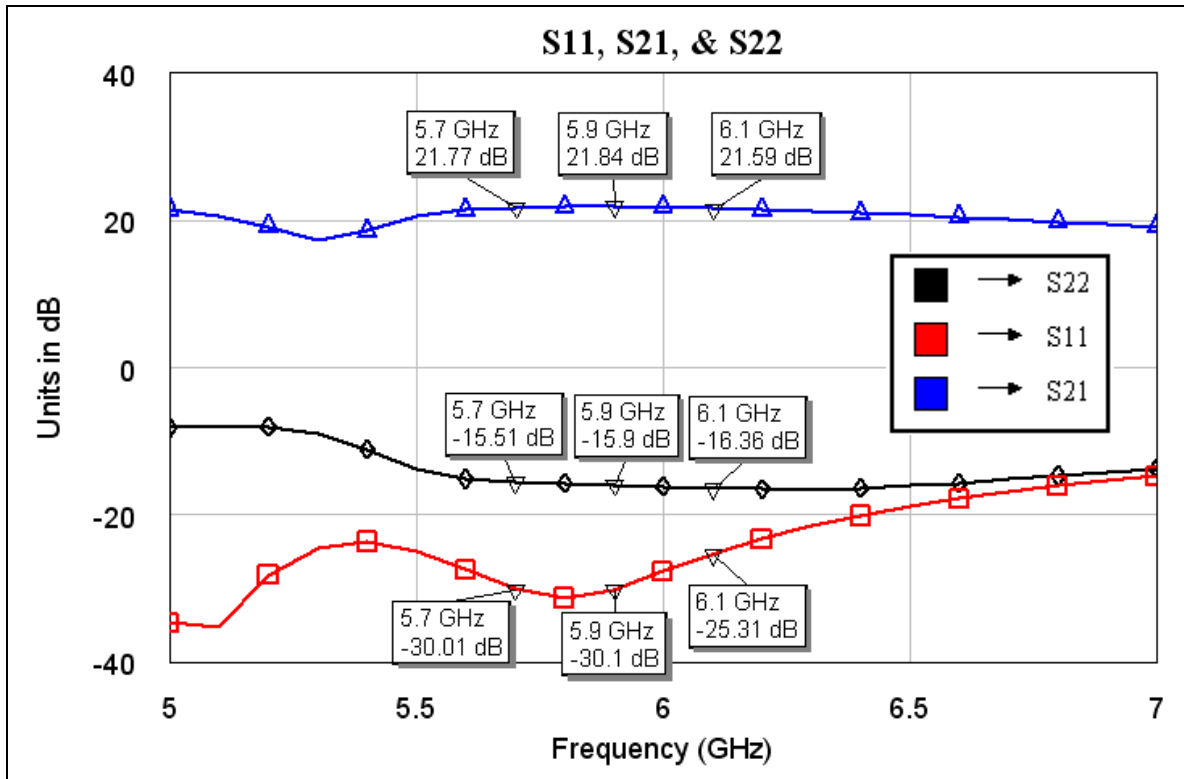


Figure 33

Section IV: Summary

This document describes a C-Band Power Amplifier operating in the frequency range of 5.7 – 6.1 GHz. Table 6 below describes the initial requirements and the back annotated simulation results used to reach these design goals.

Initial Design Requirements		Back Annotated Simulation Results	
1-dB Comp Pt.	0dBm	1-dB Comp Pt.	0.2dBm
Power Gain @ Comp Pt.	20dB	Power Gain @ Comp Pt.	20.9dB
Fundamental Isolation from 2nd and 3rd harmonics at 1-dB Comp Point	10dBm	Fundamental Isolation from 2nd and 3rd harmonics	Isolation from 2nd = 34.6dBm Isolation from 3rd = 22.9dBm
Power Consumption	< 750mW	Power Consumption	670mW

Table 6

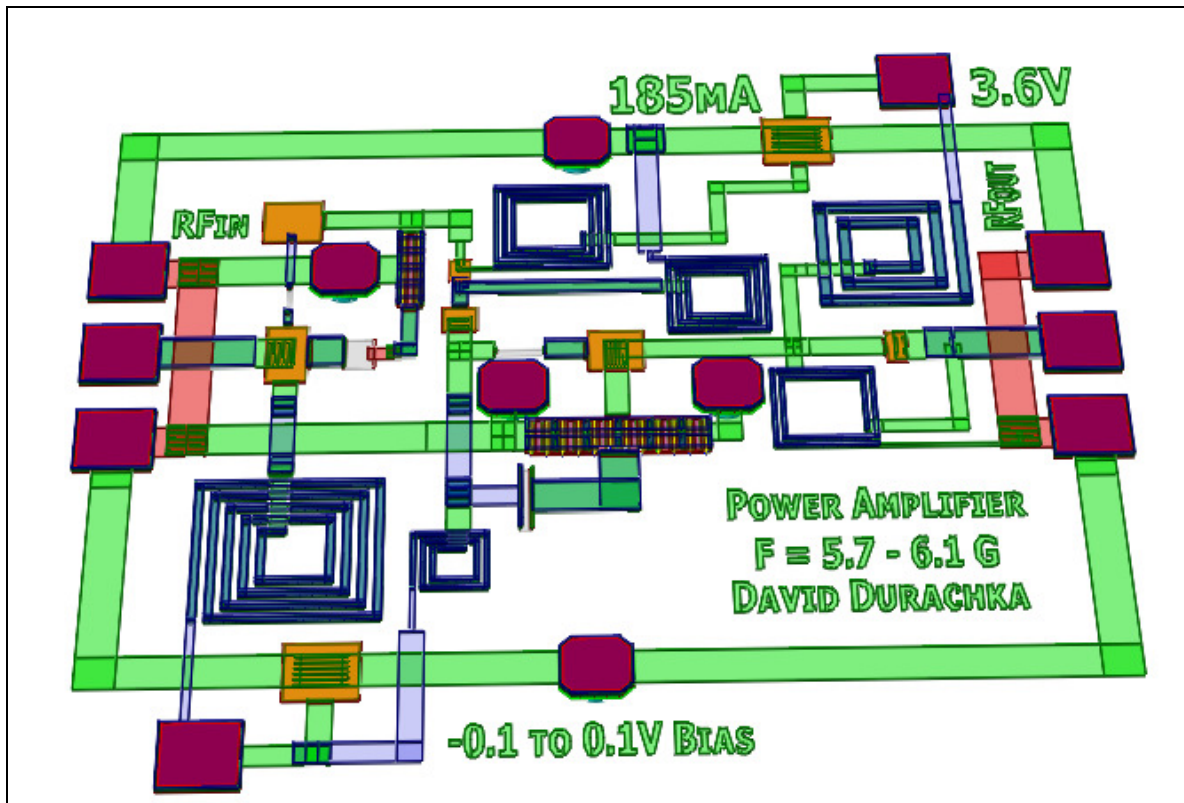


Figure 34

According to the design tool that I have, this layout is DRC clean.

Appendix A: Test Plan

Test I: DC Measurements

Make sure the substrate of the die is properly grounded, then apply 3.6-Volts to the appropriate pad. Labels have been laid out on the Metal 1 Layer to call out what each pad connection is. Table A.1 below describes the expected current draw of the amplifier.

DC Measurements	
Power Rail	3.6-V
Current Draw	185mA

Table A.1

Test II: RF Measurements

RF Measurement I: Power Gain

Once the DC parameters have been successfully tested, apply a bias of 0 Volts to the bias pad at the lower left-hand corner of the die. Then, using 150um pitch GSG probes apply a sinusoidal signal from the network analyzer with a power level of -20dBm, or 10uW. Table A.2 describes what should be produced at the output of the amplifier.

RF Measurements	
Input	-20dBm Signal
Bias	0-Volts
Power Rail	3.6-Volts
Output	0-dBm Signal

Table A.2

RF Measurement II: Compression Point

Once the gain has been verified at a low power level, gradually increase the input power to just above 1mW, or 0dBm. The amplifier should start to compress at this power level. The output power of the amplifier at this point should be 100mW at this input. Table A.3 describes these values.

RF Measurements	
Input	0-dBm Signal
Bias	0-Volts
Power Rail	3.6-Volts
Output	20-dBm Signal
Input Comp. Pt.	0.2dBm, 1.05mW

Table A.3

C-Band Voltage Controlled Oscillator (VCO)

**525.787.91 MMIC Design
December 5, 2008
Yong Kang Yuan**

TABLE OF CONTENTS

1.0	OVERVIEW	4
2.0	Oscillation Background and Theory	4
3.0	Electrical Specifications.....	5
4.0	Electrical Simulations	5
4.1	Bias-Tee Circuit	5
4.2	E-Mode PHEMT IV Characteristic	7
4.3	Varactor.....	8
4.4	Destabilizing the Active Device	11
4.5	Integration: Active Device and Varactor	16
4.6	Load Matching Network	22
4.7	THE VCO	25
5.0	PAD LAYOUT DESCRIPTION	28
6.0	TEST PLAN.....	29
6.1	Short Check.....	29
6.2	Bias Current and Voltages	30
6.3	Frequency Range	30
6.4	Out-of-Band Oscillation.....	30
7.0	Summary and Conclusions	30

LIST OF FIGURES

Figure 1: Bias-Tee Circuit Schematic.....	6
Figure 2: Input Reflection Coefficient S11 Simulation of Bias-Tee Circuit	7
Figure 3: E-PHEMT IV Schematic.....	8
Figure 4: E-PHEMT IV Characteristics.....	8
Figure 5: Variable Capacitor (Varactor) Schematic	9
Figure 6: Varactor Capacitance vs. Tuning Voltages	10
Figure 7: Varactor Capacitance vs. Tune Voltage from 0V to +0.4V	11
Figure 8: De-stabilize Active Circuit Schematic	12
Figure 9: Mapping Circle of De-stable Circuit	13
Figure 10: Load Stability of the De-stable Active Circuit.....	14
Figure 11: Mapping Circle with Optimal De-stabilizing Resistor.....	15
Figure 12: Load Stability Factor with Optimal De-stabilizing Resistor	15
Figure 13: De-stabilize Active Circuit Biasing.....	16
Figure 14: De-stable Active Circuit and Varactor Combined Schematic.....	17
Figure 15: “Vara-FET” Biasing Currents	17
Figure 16: Smith Chart-Gate Tuning Part 1.....	18
Figure 17: Smith Chart-Gate Tuning Part 2.....	19
Figure 18: Smith Chart-Drain Tuning Part 1	19
Figure 19: Mapping Circle, S11, and Load Stability of Vara-FET over Frequency and Tune Voltages	21
Figure 20: Z11 of Vara_FET over Frequency and Tune Voltages	22
Figure 21: Load Matching Network Schematic.....	23
Figure 22: Smith Chart: Z11 of Load Matching Network	24

Figure 23: C-Band VCO Complete Schematic.....	25
Figure 24: S11 Simulation of the Complete VCO.....	26
Figure 25: Extended Frequency S11 Simulation of VCO	27
Figure 26: Bias Current of VCO (active circuit and varactor).....	27
Figure 27: 2-D Layout View of the Complete VCO.....	28

LIST OF TABLES

Table 1: S11 of Vara_FET over Frequency and Tune Voltage.....	20
Table 2: Imaginary Part of S11 of Vara_FET over Frequency and Tune Voltage.....	20
Table 3: Real Part of Z11 of Vara_FET over Frequency and Tune Voltage.....	21
Table 4: Reactive Part of Z11 of Vara_FET over Frequency and Tune Voltage	21
Table 5: Z11 of Load Matching Network.....	24

1.0 OVERVIEW

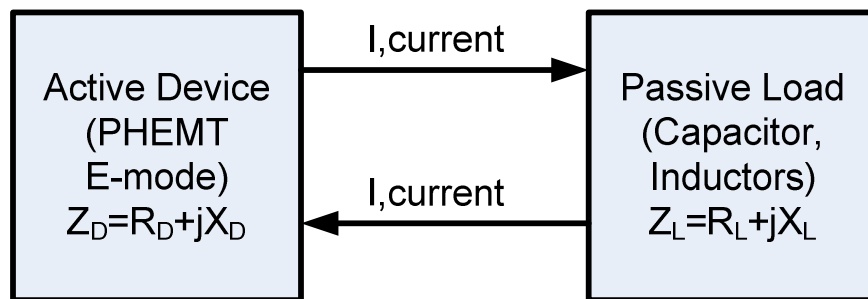
This document provides details of designing a C-band voltage controlled oscillator (VCO) under an electrical simulation environment such as AWR's Microsoft Office. The design of the VCO is based on using a pHEMT device with the concept of negative impedance matching, in which the circuit is matched for instability to achieve steady-state oscillation at the required frequencies. The details of the oscillation condition and the concept of negative impedance with instability are illustrated in sections that follow. The VCO is tuned by the use of a varactor, a reverse biased diode that varies capacitance with DC voltages.

In addition, the details of each individual sections of the VCO will be explained sequentially in this document. The VCO contains the following sections:

- Active Device Selection
- Bias Circuit
- Tunable Varactor
- Instability of Active Device
- Integration: Active Device and Varactor
- Passive Load
- Integration: Complete VCO

Finally, the components of the VCO are placed and routed on layout to be forwarded for manufacture fabrication. The layout considerations of the VCO are discussed.

2.0 Oscillation Background and Theory



According to the Kirchoff's law, the total loop voltage across the network shown in Figure 1 must be zero, $V = I * (Z_D + Z_L) = 0$, assuming that a steady state oscillation is occurring between the two networks and a non-zero loop current I that flows through the network. Therefore, if current is not 0, then $Z_D + Z_L = 0$ or $Z_D = -Z_L$; hence, negative impedance is achieved.

As illustrated in the Figure 1, the device and load impedance (Z_D and Z_L) both have a resistive and reactive components, R and X respectively. In the negative impedance condition, the $R_D = -R_L$ and $X_D = -X_L$. Assuming passive load are positive ($R_L > 0$), R_D must be negative. This negative resistance R_D condition could be achieved by destabilizing the active device with an appropriate resonance circuit. For simplicity, the design of the reactive part for both the device and the load networks are set to be equal; hence, $X_D = X_L = 0$.

The VCO shall use the series resonance type oscillator start-up conditions. A series resonance oscillator designs for a resistive component of the active network to be greater than three times the load resistive component and again, the reactive components of both parts to be equal; hence, $|R_D| > 3 R_L$ and $X_D = -X_L$.

3.0 Electrical Specifications

- Tuning Frequency: C-Band 5.2GHz to 5.9GHz
- VCC: +2.0V +/-5% , 18mA +/-5%
- Tune Voltage: 0V to +0.5V; +/-5%

4.0 Electrical Simulations

As mentioned, the C-Band voltage controlled oscillator shall be designed using AWR's Microsoft Office. In addition, the VCO shall be designed using components (active, passive, etc) from the TRIQUINT library. For the VCO design, passive components include resistors, capacitors, spiral inductors, microstrip lines, Tee-junctions, and substrate vias. The active components of the VCO include a D-mode and an E-mode PHEMT.

4.1 Bias-Tee Circuit

The bias-tee circuit is shown in Figure 1:

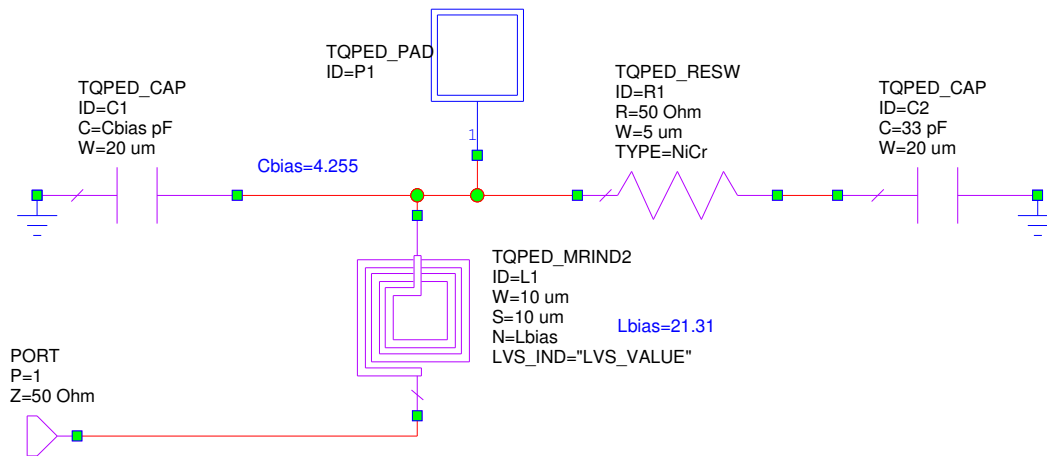


Figure 1: Bias-Tee Circuit Schematic

The bias-tee circuitry will be used to interface between the applied DC voltage and the drain (output) port of the active circuit. The input port (Port1) of the bias-tee shall exhibit high input impedance at the center operating frequency to avoid the coupling of microwave signals to the DC bias source/circuitry. Therefore, a spiral TQRIQUIN inductor (L1) is used as a RF choke.

By sequentially tuning the length of the spiral trace inductor, the input reflection coefficient can be made to achieve zero impedance. A capacitor to ground (C1), which could be thought as similar to an open stub, can be tuned to achieve high impedance at the input of the bias-tee circuit.

In addition, the bias-tee circuit shall also serve to suppress out of band oscillations; therefore, lumped element components are used for frequencies further away from the operating frequencies, especially for lower frequencies where higher transistor gains increase the threat of oscillation. A 50 Ω resistor (R1) placed at the end of the RF choke is an effective element at suppressing oscillation. Since we would like the resistor to not dissipate DC power a capacitor (C2) is added between the resistor and ground.

The S11 of the bias-tee circuit is plotted in Figure 2.

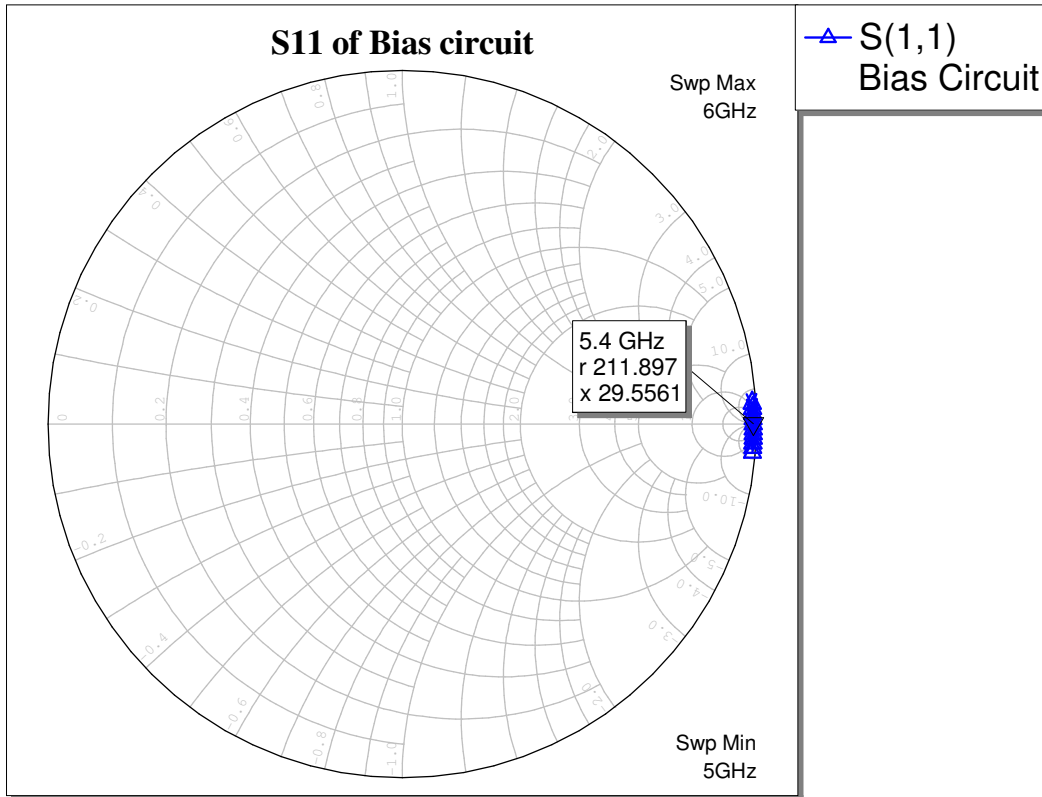


Figure 2: Input Reflection Coefficient S11 Simulation of Bias-Tee Circuit

Simulation of the bias tee input port S11 shown in Figure 2 confirms that the input is high impedance (open circuit) at the frequencies of interest (5GHz to 6GHz).

4.2 E-Mode PHEMT IV Characteristic

The main component of the active circuit is the TRIQUINT E-mode PHEMT. For the accuracy of the PHEMT model and to minimize resistive losses, the product of the width of the gate figure (W) and the number of gate figures (N) are set to 300um; i.e. W = 50um, N = 6. The I-V characteristic of the PHEMT is explored with different drain (Vds) and gate (Vgs) voltages. The 300um TRIQUINT PHEMT IV schematic and the simulation are shown in Figure 3 and Figure 4, respectively.

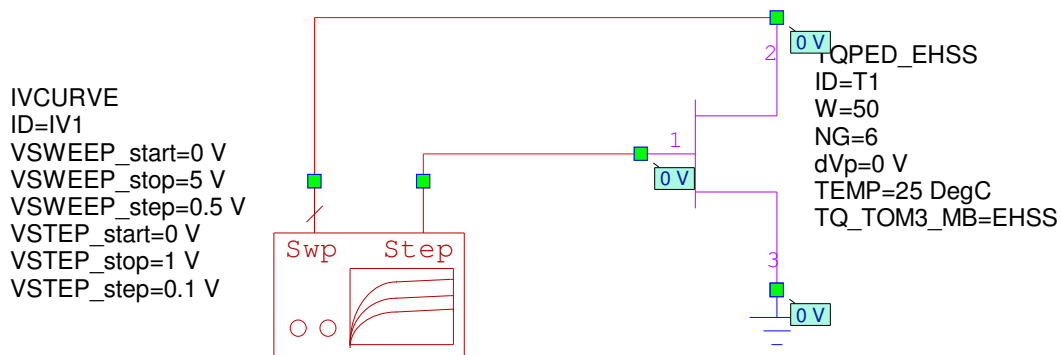


Figure 3: E-PHEMT IV Schematic

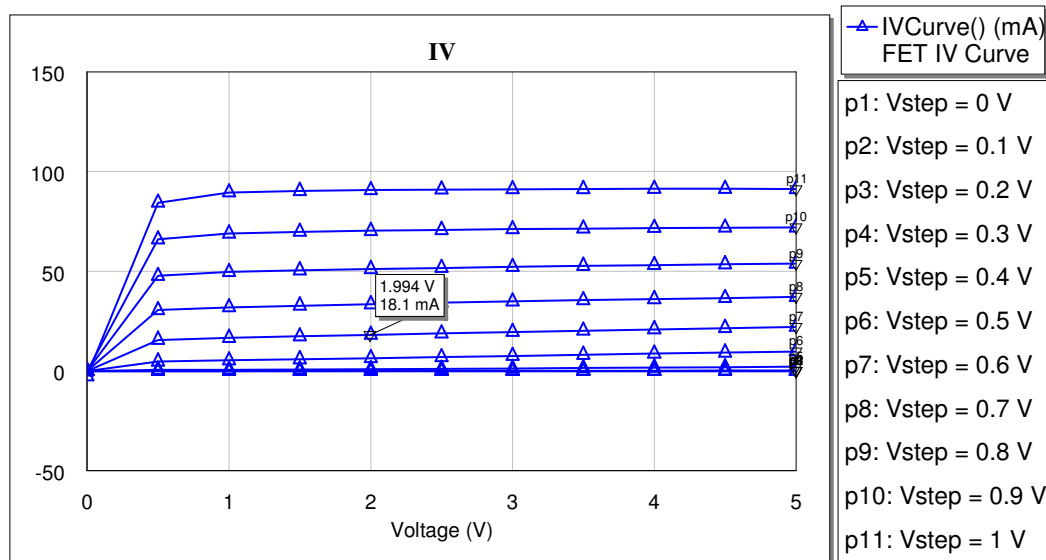


Figure 4: E-PHEMT IV Characteristics

The simulation shown in Figure 4 suggests that the PHEMT drain (V_{ds}) can be biased with +2.0V and the gate (V_{gs}) with +0.6V. The resultant current drawn is approximately 18mA. Since the gate port of the FET draws minimum current, the active circuit shall consume approximately 36mW of power (i.e. $2V * 18mA$). In addition, according to the simulation, it is possible to bias the drain port with lower voltage (i.e. 1V), since the I-V curve showed that the current is constant over V_{ds} . It would be explained in later sections how +2V bias on the drain port was selected.

4.3 Varactor

As mentioned, the VCO shall be tuned across the required oscillation frequency by using a variable capacitor. A variable capacitor shall be combined with an inductor to form the VCO resonant tank circuit (i.e. $f_0 = 1/(2*\pi*\sqrt{L*C})$). The variable capacitor (varactor) is designed by reverse biasing a diode. By applying DC voltages to the

negative port of a diode, it provides varying capacitance. The varactor can be created with a D-mode PHEMT by shorting the drain and source port, since diode junction exists between the gate and the source port of a FET. For similar reasons of selecting the proper size of the E-mode PHEMT, the D-mode PHEMT will also have six fingers with the finger width of 50um. The schematic of the varactor is shown in Figure 5.

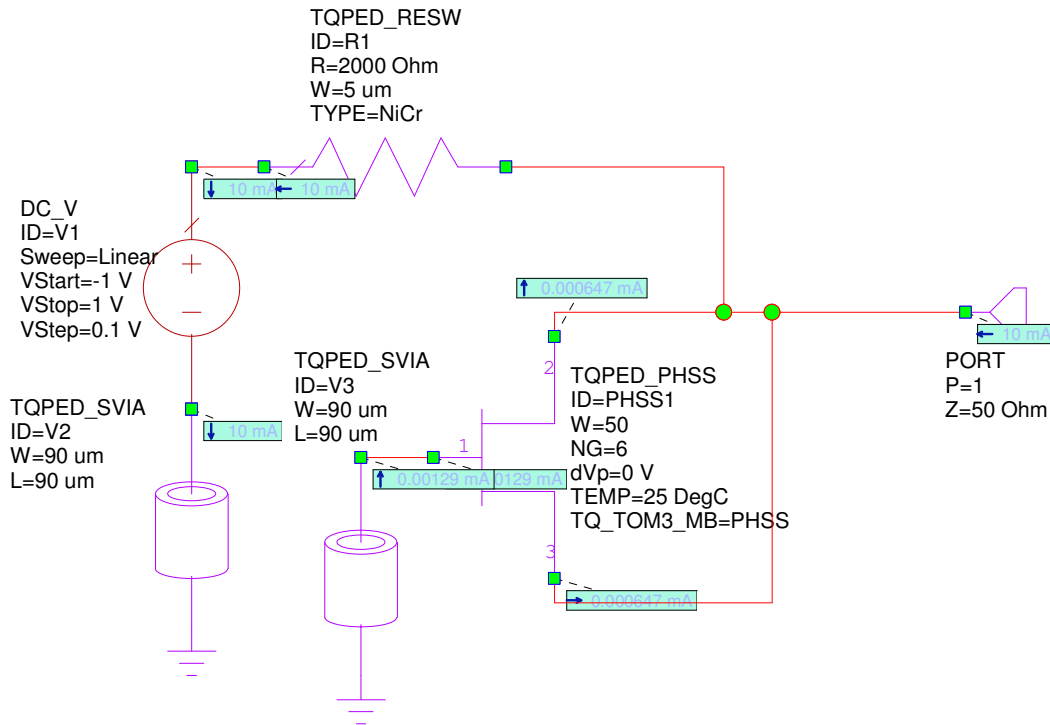


Figure 5: Variable Capacitor (Varactor) Schematic

As shown in the varactor schematic, DC bias is applied to the drain and source port through a 2kohm resistor. Since the current drawn is minimal, a 2kohm resistor is used to isolate the coupling of the RF signal of the active circuit, in which the varactor circuit shall be combined in later sections.

In addition, a D-mode PHEMT was selected for the varactor because it is possible to have negative tuning voltages at V_{tune} (V1); therefore, a wider range of capacitance becomes possible. The simulated capacitance with tuning voltages ranging from -1.0V to +1.0V (0.1V steps) are shown in Figure 6:

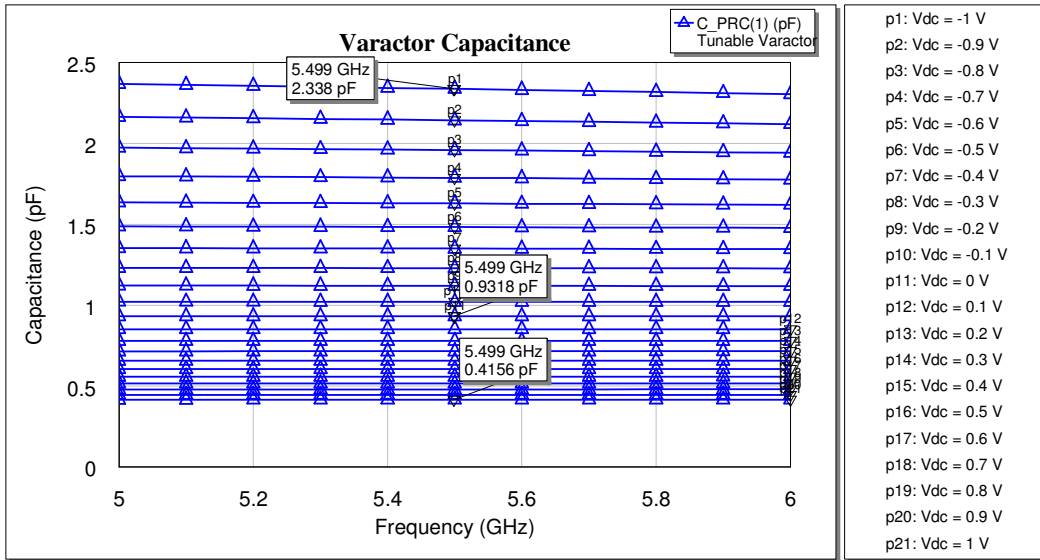


Figure 6: Varactor Capacitance vs. Tuning Voltages

According to the simulation, the varactor can tune from 2.338pF to 0.4156pF at tuning voltage of -1V to +1V. Though, the tuning curve is not linear, which is expected for a varactor. Therefore, to determine the potential oscillation frequency, the capacitance at the mid-tuning point is used: 0V with 0.9318pF. Assuming a 0.932nH inductor, the tank circuit can tune from 3.4GHz to 8GHz (-1V to +1V) with center frequency of 5.4GHz (0V); using the equation of $f_0 = 1/(2*\pi*\sqrt{L*C})$. Though, since the required oscillation frequency ranges from 5.2GHz to 5.9GHz, the tuning voltage of 0V to +0.4V shall be used for the convenience of positive voltages. Hence, the varactor capacitance shall range from 0.65669pF to 0.93176pF with inductor of 1.05nH to achieve the oscillation frequency range of 5.09 GHz to 6.06 GHz.

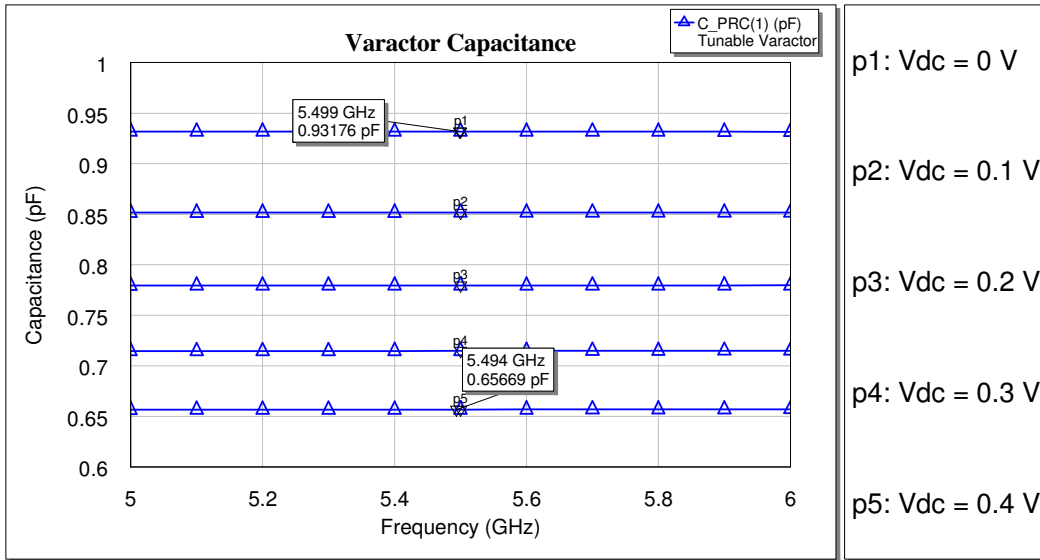


Figure 7: Varactor Capacitance vs. Tune Voltage from 0V to +0.4V

4.4 Destabilizing the Active Device

The de-stabilization of the E-mode PHEMT active circuit shall result in frequency oscillation. De-stabilization would be a process of creating a reflection coefficient ($|r|$) of the active circuit to be greater than one; in which more power are reflected back to the incident port. As mentioned in earlier sections, to compromise between oscillation growth and final oscillation frequency predictability, the series resonance oscillation condition shall have $|R_D| > 3R_L$ and $X_D = -X_L$. To de-stabilize the FET, the source port is connected to a series resistor to ground, in which to provide a feedback path from drain current to gate voltage to increase the magnitude of the S12. As S12 is greater than one, then the active device becomes unstable and the output impedance would be negative, hence, the oscillation condition is achieved.

The schematic of the De-stable circuit is shown below:

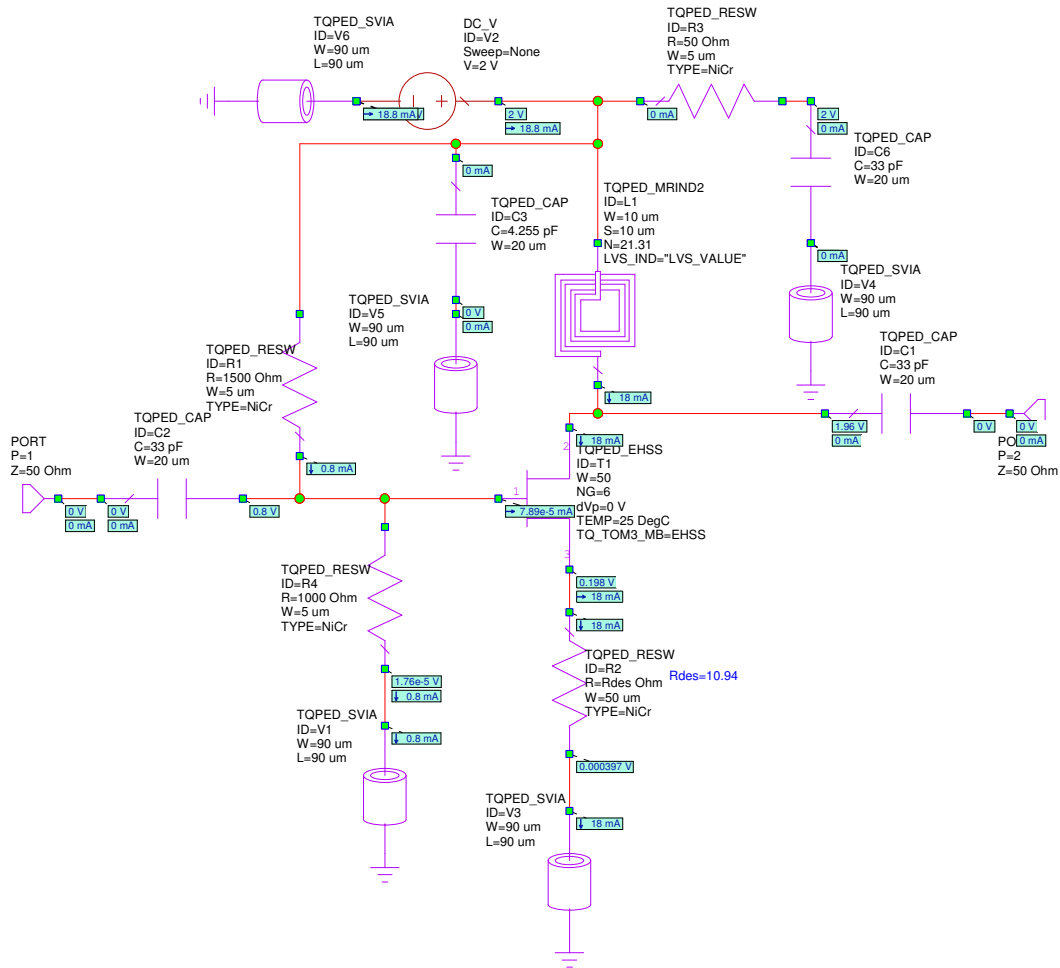


Figure 8: De-stabilize Active Circuit Schematic

The two port circuit consists the E-mode PHEMT, de-stabilizing resistor on the source port, and bias-tee of the drain and gate ports. The bias-tee interfaces the DC source to the drain (output) of the PHEMT, while the gate is biased using a voltage divider (R4 & R1) to achieve the required V_{gs} with the series de-stabilizing resistor (R2). The voltage divider method of the gate biasing is preferred to minimize the real estate of the VCO in layout. The disadvantage of the voltage divider method is that it depends on the V_{ds} ; therefore, less flexibility in adjustment of the V_{gs} . The input and output port is added with a capacitor to avoid DC coupling and dissipation of power on the 50Ω ports.

To simulate the de-stabilized active circuit, the ‘SMAP’ (Mapping Circles) function helps to plots the distance from the center of the Smith Chart to the farthest away point on the output mapping circle. Hence, the SMAP function is equivalent to plotting the inverse of the absolute value of the load stability factor, which is the required to meet the oscillation conditions. Therefore, by plotting the mapping circles and the load stability factor, one

can tell how destabilized the transistor has become. The simulation of the Mapping Circles and load stability factor are shown below:

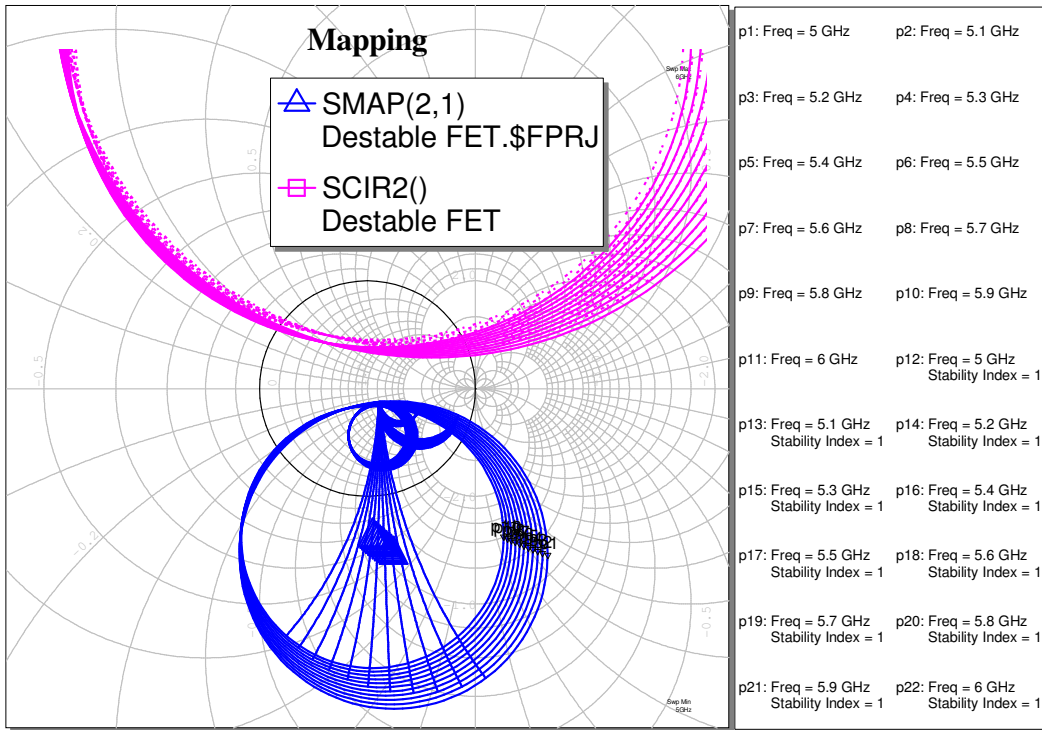


Figure 9: Mapping Circle of De-stable Circuit

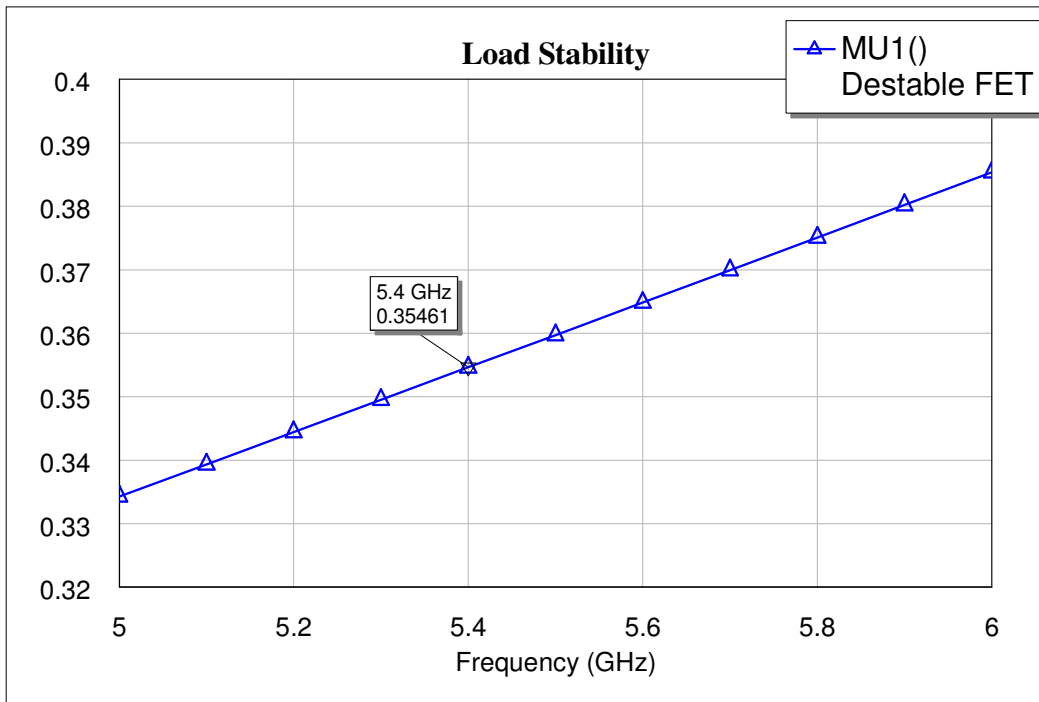


Figure 10: Load Stability of the De-stable Active Circuit

The de-stabilizing resistor was tuned at the frequency of interest to achieve a load stability factor of 0.35461 or the inverse of 2.82, which is close to the oscillation condition goal of 3. In addition, from 5GHz to 6GHz, the simulation showed that the inverse of the load stability ranges from 2.985 to 2.6. Furthermore, it can be observed that by tuning the destabilizing resistor to increase the inverse of the load stability factor, the mapping circle also increases in sizes; hence, the distance from the center of the Smith Chart to the farthest away point of the circle increase, which is expected. The finalized destabilizing resistor is tuned at 10.94Ω. To further explore the possible values of the destabilizing resistor to achieve a higher inverse of the load stability factor, the resistor was tuned to 7.84Ω and below is the mapping circles and load stability simulation:

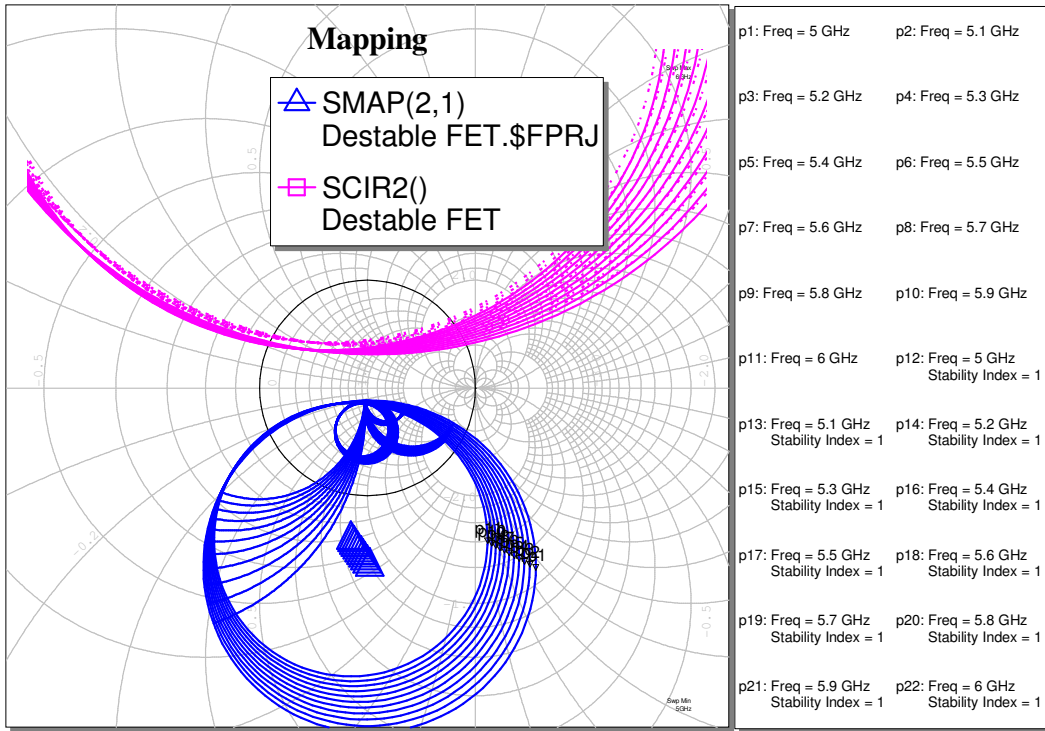


Figure 11: Mapping Circle with Optimal De-stabilizing Resistor

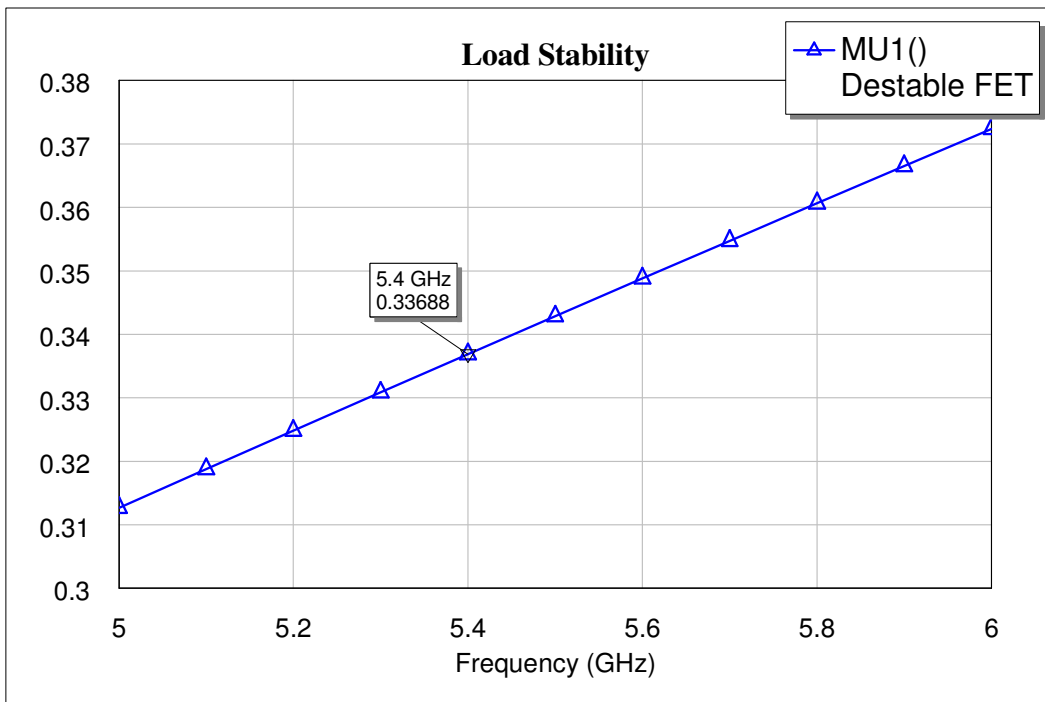


Figure 12: Load Stability Factor with Optimal De-stabilizing Resistor

As shown in Figure 11 and Figure 12, the inverse of the load stability factor achieves 3.19 to 2.67 from 5GHz to 6GHz. Due to more optimal biasing and layout of the VCO, 10.97Ω is used. The biasing and the current simulation of the active circuit are shown below:

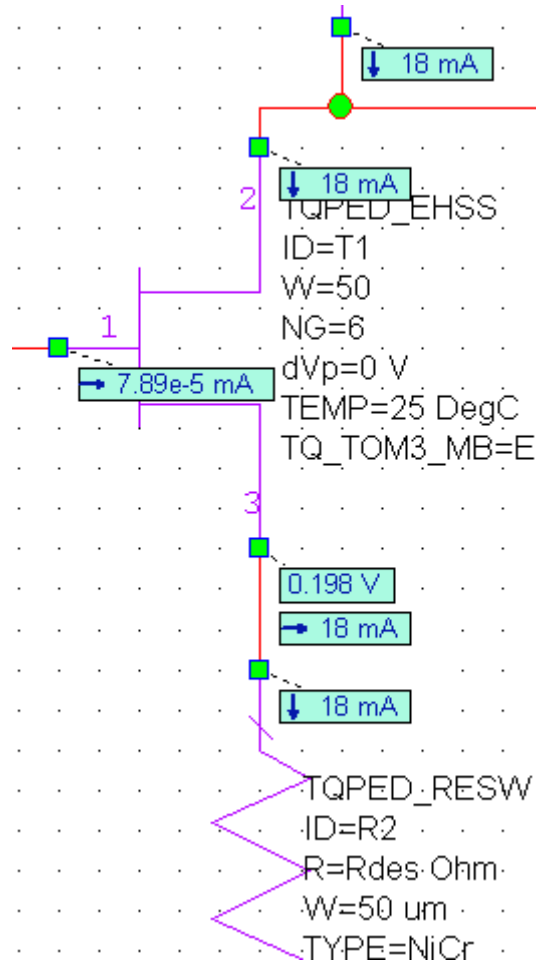


Figure 13: De-stabilize Active Circuit Biasing

As shown in Figure 13, minimal current are drawn on the gate port; therefore, resistors R1 and R4 width are set to 5um (maximum of 5mA of current). In addition, the finalized de-stabilizing resistor results in 18mA of current drawn on the source port, therefore, the width is set to 50um.

4.5 Integration: Active Device and Varactor

The active device (Figure 8) and varactor (Figure 5) are integrated to form the 'Vara_FET' circuit shown in Figure 14.

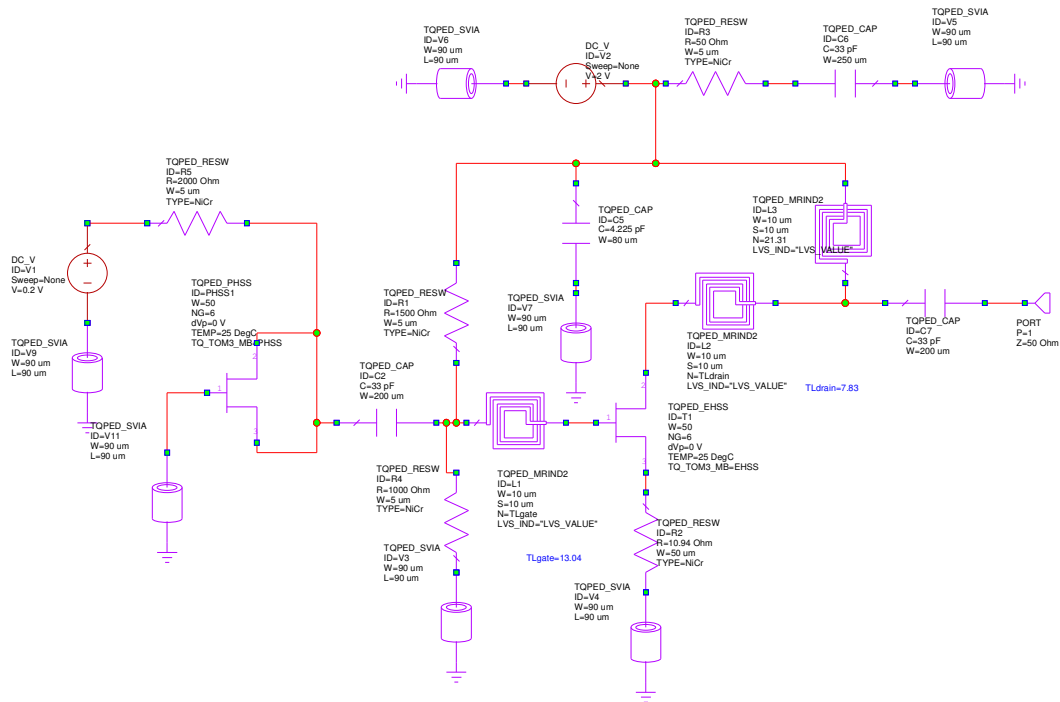


Figure 14: De-stable Active Circuit and Varactor Combined Schematic

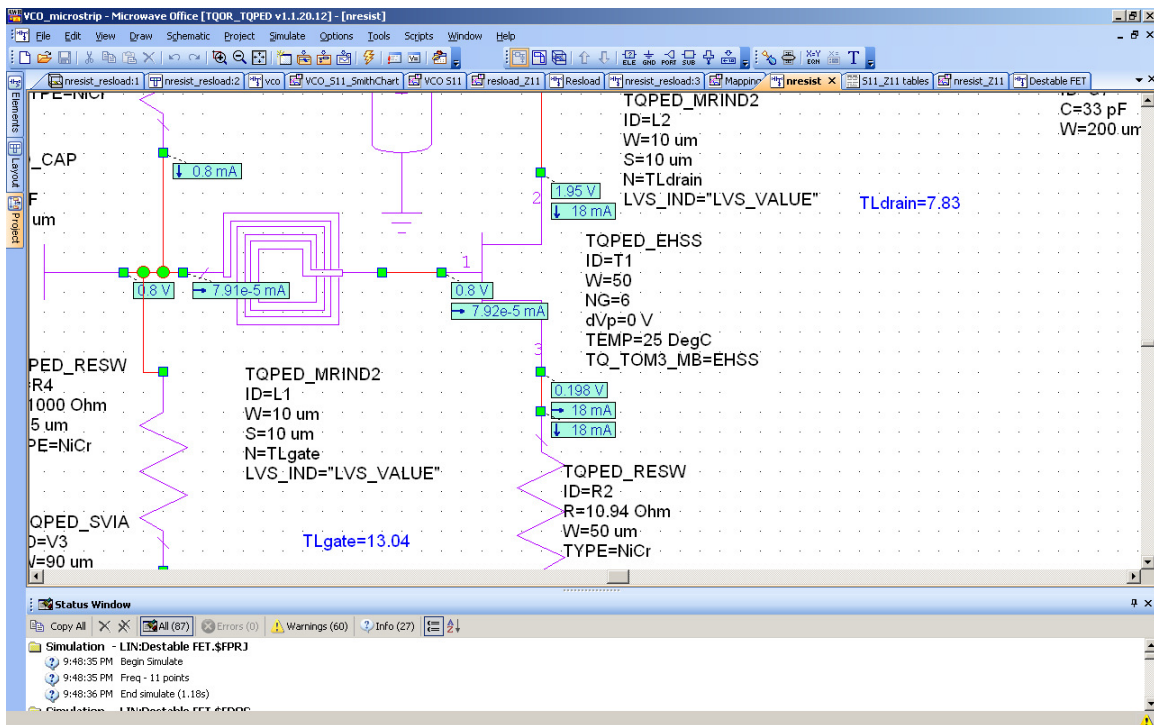


Figure 15: “Vara-FET” Biasing Currents

The simulation above showed that the bias at the drain port is 1.95V instead of 2V; therefore, there is 0.5V of loss through the spiral inductors. In addition, the V_{gs} is maintained at 0.6V (0.8V-0.198V), which is expected.

In addition, the schematic of the “Vara-FET” consists the tuned gate and drain spiral inductor to achieve the required S11 (real + imaginary) of approximately 2.82 and the reactive part to become 0° (-180°). The steps below shall illustrate the procedures of arriving to the required oscillation conditions and the schematic in Figure 14:

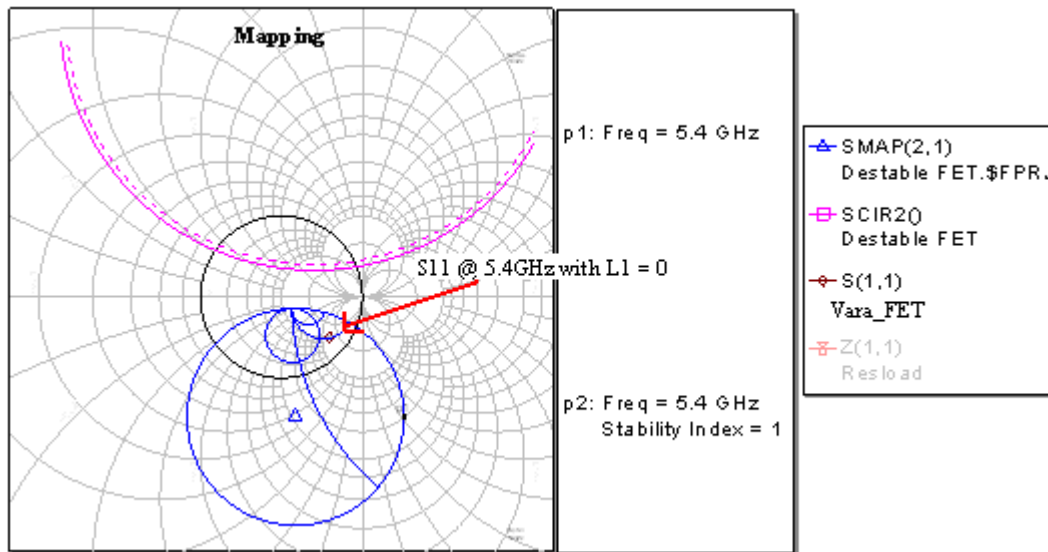


Figure 16: Smith Chart-Gate Tuning Part 1

The simulation of the Smith Chart in the figure above consists of the mapping circle of the De-stable Active Circuit, load stability of the De-stable Active Circuit, and the S11 of the Vara-FET at 5.4 GHz. To achieve the real part of S11 of 2.82, a spiral inductor (L1, act as a transmission line) is added to the gate of the E-mode PHEMT. Figure 16 represents the S11 of the Vara_FET with the length of L1 set to zero. The length of L1 is increased until the magnitude of S11 reaches maximum as shown in Figure 17, which shall be approximately 2.82.

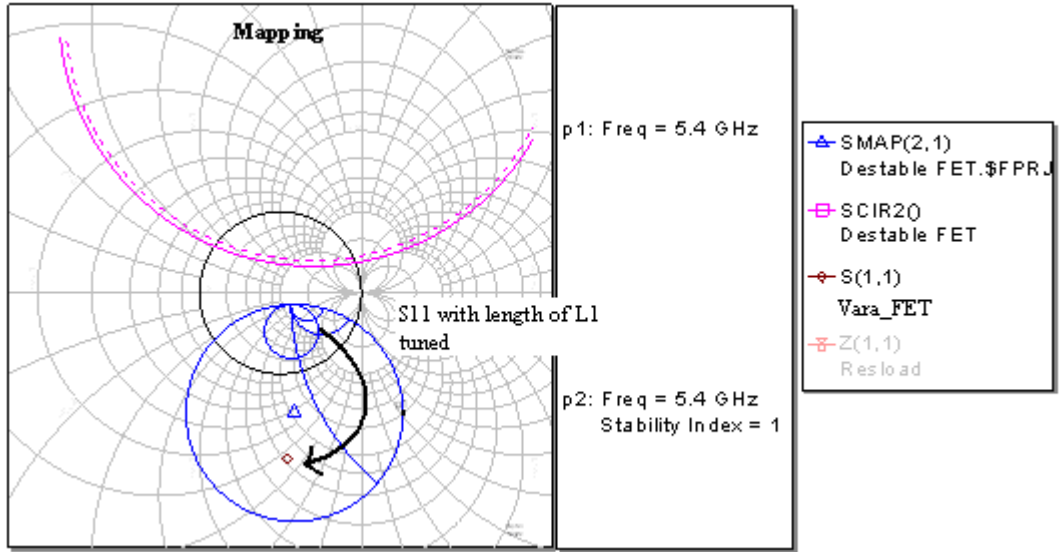


Figure 17: Smith Chart-Gate Tuning Part 2

After L1 is tuned (shown in Figure 17), the magnitude of S11 is measured to be 2.05. The simulation showed that the maximum magnitude of S11 that could be achieved is 2.05, which could be explained by the tuning element, the gate spiral inductor. The gate spiral inductor has sensitive impact to the circuitry; hence, a small amount of change in value could results in bigger effect in performance. Since there is limits of fine tuning the spiral inductor and the fact it's a non-ideal elements, the S11 of 2.05 is the best tuned value. Finally, at this point, the Vara_FET shall exhibit negative resistance and a certain reactance.

Next, the reactive part of Vara_FET's input impedance is tuned to achieve zero, or pure resistive. A spiral inductor (L2, act as a transmission line) is added to the drain port of the E-mode PHEMT. The Smith Chart simulation is shown in Figure 18:

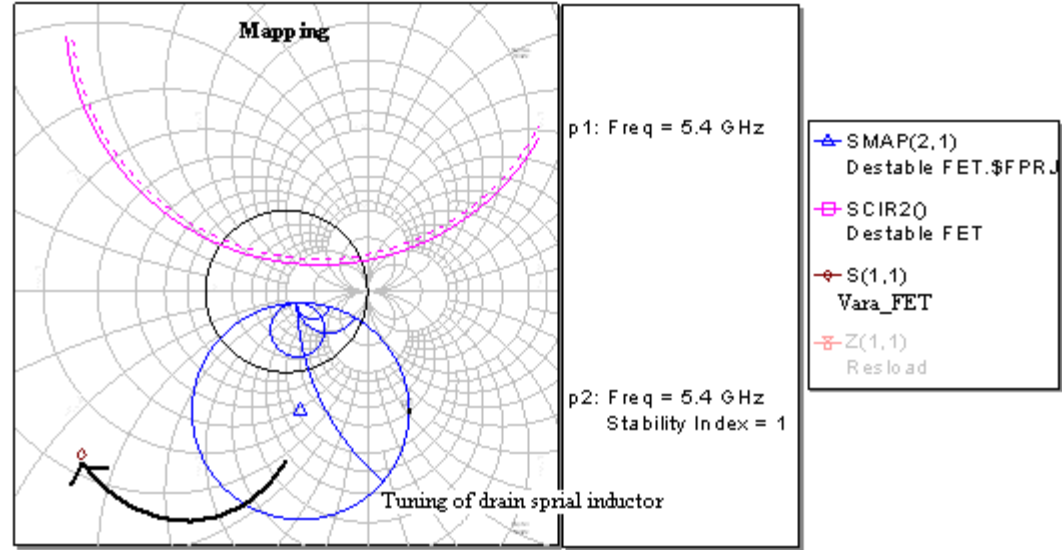


Figure 18: Smith Chart-Drain Tuning Part 1

The length of L2 is tuned until the reactive part becomes zero. As the length of L2 is increased, the S11 rotates clockwise until it reaches the zero or -180° . Below are plots and tables of the magnitude and phase of S11 after both the gate and drain spiral inductors are fine tuned; hence, the requirement of zero reactive component and magnitude of approximately 2.8 are achieved. The plots and tables are simulated from 5 GHz to 6 GHz (0.1GHz steps) with tuning voltages from 0V to +0.5V (0.1V steps).

Table 1: |S11| of Vara_FET over Frequency and Tune Voltage

Frequency (GHz)	Magnitude of S11					
	Vdc = 0 V	Vdc = 0.1 V	Vdc = 0.2 V	Vdc = 0.3 V	Vdc = 0.4 V	Vdc = 0.5 V
5	4.3281	4.3466	3.0897	2.1443	1.5915	1.2558
5.1	3.3951	4.1976	3.5571	2.4733	1.7819	1.3712
5.2	2.6532	3.5317	3.7718	2.844	2.0146	1.5109
5.3	2.124	2.8221	3.5167	3.1592	2.2869	1.6792
5.4	1.7463	2.2625	2.9722	3.2345	2.5674	1.8773
5.5	1.4693	1.8505	2.4264	2.9838	2.7697	2.0958
5.6	1.2602	1.5467	1.9866	2.5561	2.776	2.3005
5.7	1.098	1.318	1.6522	2.1297	2.5594	2.4235
5.8	0.96936	1.1418	1.3987	1.7754	2.2257	2.3944
5.9	0.86536	1.003	1.2038	1.4974	1.8892	2.2119
6	0.77995	0.89159	1.0511	1.2813	1.6004	1.9494

Table 2: Imaginary Part of S11 of Vara_FET over Frequency and Tune Voltage

Frequency (GHz)	IM (S11) (deg)					
	Vdc = 0 V	Vdc = 0.1 V	Vdc = 0.2 V	Vdc = 0.3 V	Vdc = 0.4 V	Vdc = 0.5 V
5	-1.3077	-3.6589	-3.0858	-2.0926	-1.4832	-1.1211
5.1	0.097473	-2.1804	-3.321	-2.472	-1.7293	-1.2788
5.2	0.67728	-0.55205	-2.7337	-2.7797	-2.007	-1.4619
5.3	0.87288	0.35775	-1.3856	-2.7288	-2.2733	-1.667
5.4	0.91534	0.73611	-0.19454	-2.0211	-2.4051	-1.8756
5.5	0.89817	0.86392	0.45889	-0.91498	-2.1849	-2.0334
5.6	0.85864	0.88548	0.74101	-0.014024	-1.4975	-2.028
5.7	0.81204	0.8633	0.83853	0.49273	-0.61103	-1.7191
5.8	0.76473	0.8241	0.85257	0.7229	0.090463	-1.0966
5.9	0.71933	0.77946	0.83027	0.80622	0.50002	-0.3864
6	0.67681	0.73445	0.79311	0.81872	0.6963	0.16738

By analyzing Table 1, under the “Vdc=0V” column, the |S11| is maximum at 5GHz. In addition, Table 2 shows that the reactive component is closest to zero at 5.1GHz; hence, it is possible to predict that the VCO should tune at approximately 5GHz to 5.1GHz with 0V of tuning voltage. Therefore, the tables above shall help in the prediction of the oscillation frequency at a particular tuning voltage.

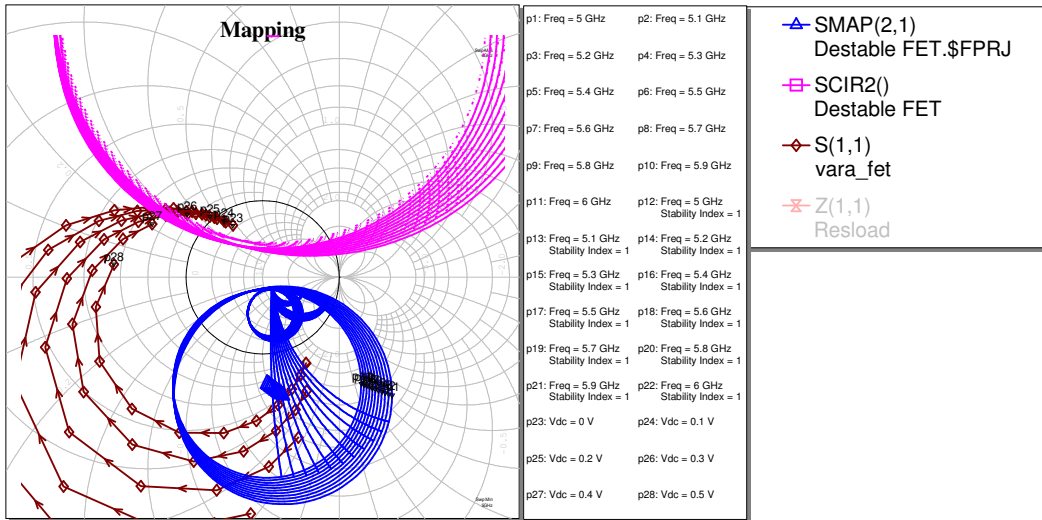


Figure 19: Mapping Circle, S11, and Load Stability of Vara-FET over Frequency and Tune Voltages

As mentioned, as the $|S_{11}|$ is tuned to ~ 2.05 , the input port of the circuit exhibits certain negative impedance. The negative impedance over frequency and tuning voltages are plotted and listed into tables below:

Table 3: Real Part of Z11 of Vara_FET over Frequency and Tune Voltage

Frequency (GHz)	Real part of Z11 (ohms)					
	Vdc = 0 V	Vdc = 0.1 V	Vdc = 0.2 V	Vdc = 0.3 V	Vdc = 0.4 V	Vdc = 0.5 V
5	-31.683	-36.389	-39.352	-38.588	-32.223	-19.957
5.1	-27.252	-32.217	-35.963	-36.77	-32.796	-23.276
5.2	-22.928	-28.052	-32.38	-34.437	-32.483	-25.457
5.3	-18.709	-23.911	-28.659	-31.701	-31.435	-26.634
5.4	-14.589	-19.807	-24.845	-28.651	-29.779	-26.933
5.5	-10.565	-15.748	-20.972	-25.357	-27.623	-26.471
5.6	-6.6332	-11.742	-17.066	-21.879	-25.059	-25.355
5.7	-2.791	-7.7947	-13.15	-18.264	-22.164	-23.681
5.8	0.96359	-3.9104	-9.2421	-14.551	-19.006	-21.534
5.9	4.6323	-0.09304	-5.3558	-10.773	-15.64	-18.991
6	8.2165	3.6543	-1.5036	-6.9566	-12.116	-16.122

Table 4: Reactive Part of Z11 of Vara_FET over Frequency and Tune Voltage

Frequency (GHz)	IM (Z11) (deg)					
	Vdc = 0 V	Vdc = 0.1 V	Vdc = 0.2 V	Vdc = 0.3 V	Vdc = 0.4 V	Vdc = 0.5 V
5	-4.6728	-14.882	-28.417	-44.886	-62.356	-77.557
5.1	0.50466	-8.4533	-20.499	-35.526	-52.151	-67.637
5.2	5.1427	-2.6995	-13.384	-27.008	-42.629	-58.023
5.3	9.3017	2.4566	-6.987	-19.266	-33.789	-48.799

5.4	13.032	7.0796	-1.234	-12.239	-25.618	-40.023
5.5	16.376	11.224	3.938	-5.8717	-18.094	-31.735
5.6	19.37	14.936	8.5833	-0.1109	-11.191	-23.959
5.7	22.044	18.255	12.749	5.0904	-4.8799	-16.706
5.8	24.424	21.215	16.478	9.775	0.8697	-9.978
5.9	26.535	23.847	19.805	13.982	6.0884	-3.7703
6	28.395	26.176	22.763	17.747	10.807	1.9273

As shown in Table 3 and Table 4, using the similar method to determine the frequency of oscillation with each tune voltages, one can observe that each tune frequency exhibits negative impedance that ranges approximately -35Ω to -18Ω and their corresponding phase is close to zero deg. The negative impedances over frequencies imply that oscillation is possible as long as the start-up oscillation condition is satisfied.

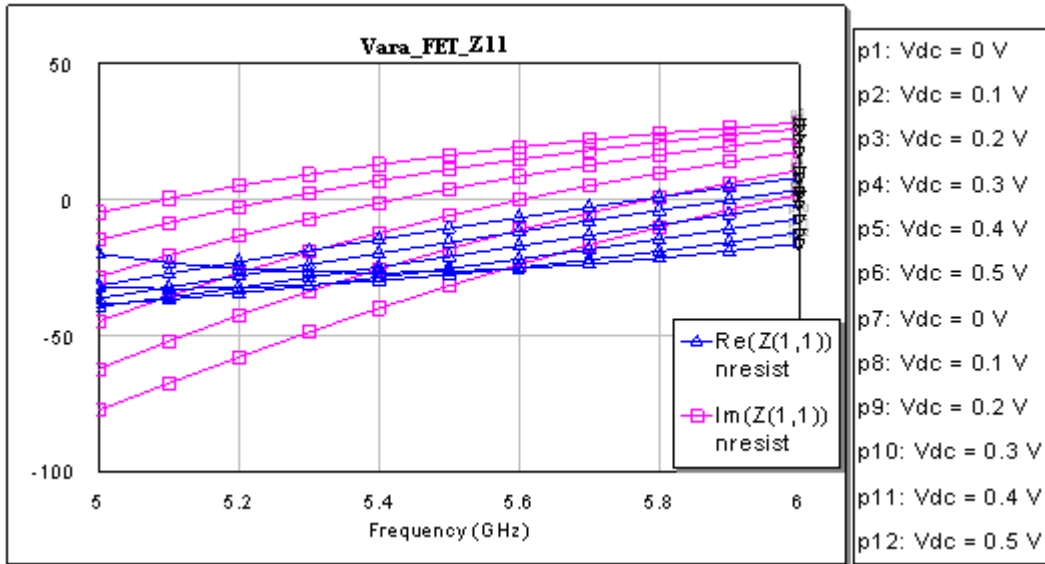


Figure 20: Z11 of Vara_FET over Frequency and Tune Voltages

Figure 20 plots the Vara_FET's real and imaginary component of the Z11 over frequency and tune voltages. As observed from the plot, the $IM(Z11)$ crosses the '0' line at the simulated frequency range with the tune voltage range; though, the more important characteristics is that each for all tune voltages, the $IM(Z11)$ crosses the '0' line transiting from negative phase to the positive phase. Therefore, it is determined that the Vara_FET exhibits a series resonance type VCO circuits and the oscillation condition of $|RD| > 3 RL$ and $XD = -XL$ should be considered.

4.6 Load Matching Network

As stated, the start-up condition of $|RD| > 3 RL$ is required; hence, the negative impedance (RD) range of -35Ω to -18Ω needs to be matched by the load matching network. The load matching network requires impedance that is three times less of the RD range, i.e. 11.7Ω to 6Ω , to interface with the impedance of the active network. This load is designed

using lumped elements (capacitors and spiral inductors). The schematic of the load matching network is shown below:

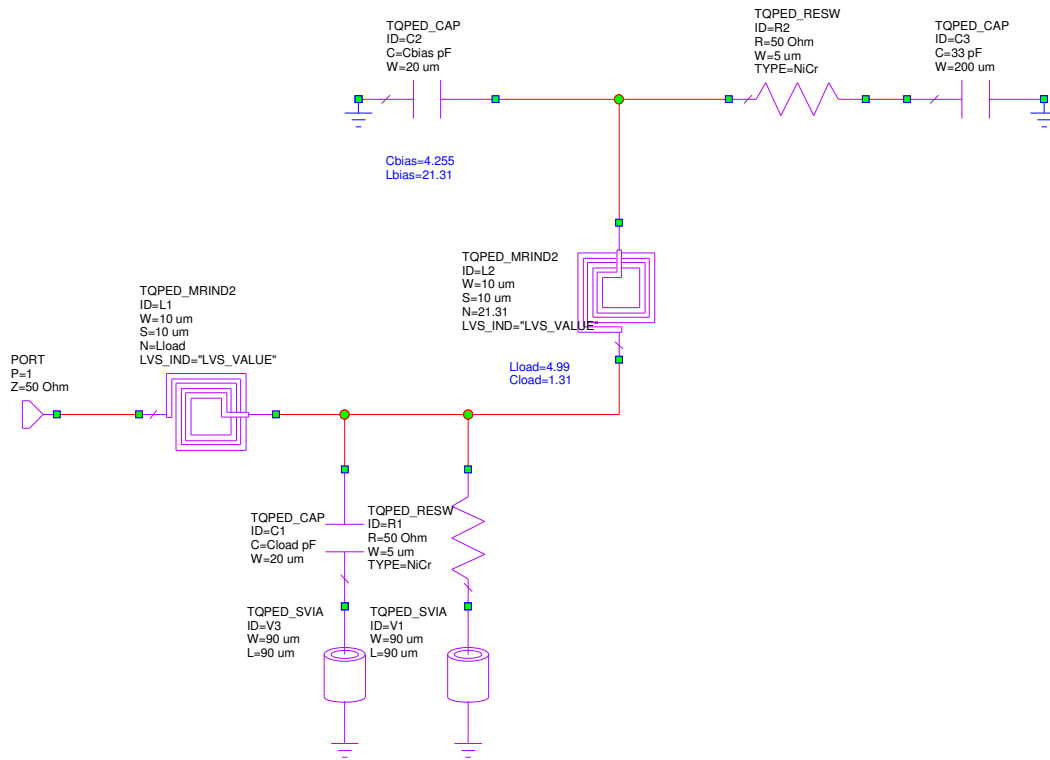


Figure 21: Load Matching Network Schematic

As shown, the Load Matching Network schematic consists of the bias-tee network, a 50-ohm input port, a 50-ohm load, and the lumped elements. The output side is connected to 50 ohms; therefore, the S11 measurement reflects the actual impedance seen by the active circuit. In addition, the bias-tee circuit is added to include any effect it might have on the load matching network.

The Smith Chart is used with the simulation tool to tune the load matching network to achieve the required impedances. The series spiral inductor and shunt capacitor topology is used for the load network. The tuned network S11 and the Z11 is plotted below:

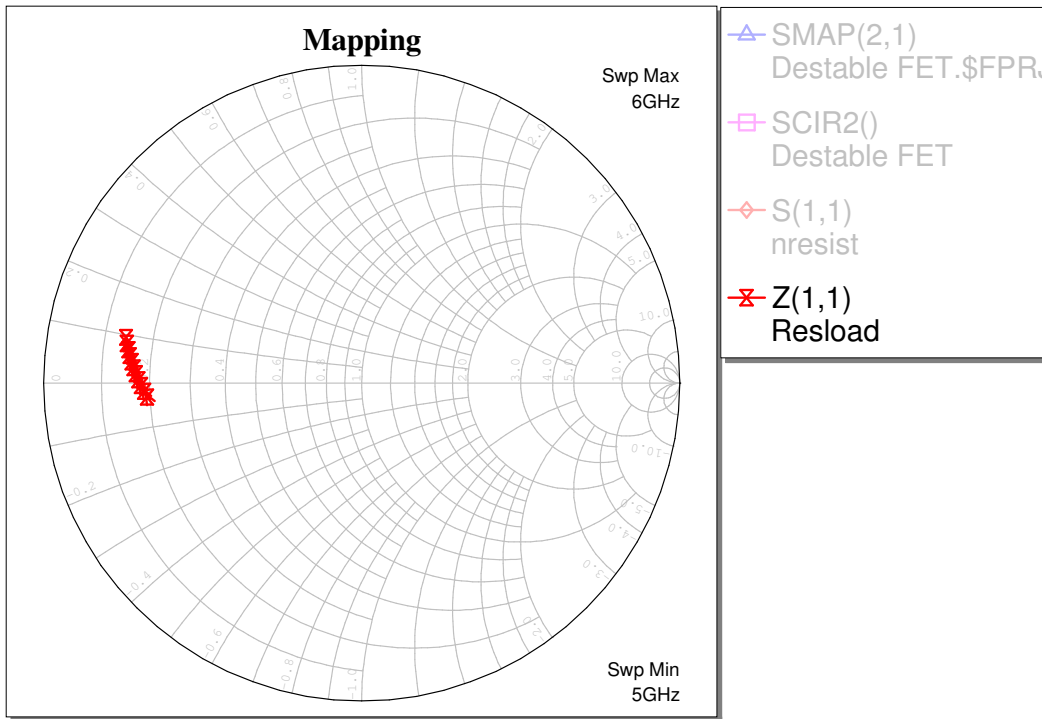


Figure 22: Smith Chart: Z11 of Load Matching Network

Table 5: Z11 of Load Matching Network

Frequency (GHz)	Input Impedance Z(1,1) of Resload	
	(Real)	(Imag)
5	9.6879	-1.5523
5.1	9.3538	-0.90226
5.2	9.0386	-0.25733
5.3	8.7407	0.3824
5.4	8.4591	1.0169
5.5	8.1926	1.6463
5.6	7.9401	2.2705
5.7	7.7008	2.8896
5.8	7.4737	3.5038
5.9	7.2581	4.1131
6	7.0532	4.7177

From both Figure 22 and Table 5, the simulation showed that the load matching network achieves approximately 10Ω to 7Ω from 5GHz to 6GHz, as compared to the required start-up oscillation condition of 11Ω to 6Ω . In addition, the phase component of the input impedance is nearly zero degree over frequency; therefore, the recommended start-

up conditions are achieved. Hence, the predicted tuning frequencies described in Section 4.5 are confirmed and shall be expected to oscillate since all conditions are satisfied.

4.7 THE VCO

The last step of the design is to combine the “Vara_FET” and the load matching network to form the C-Band VCO. The schematic of the complete VCO is shown below:

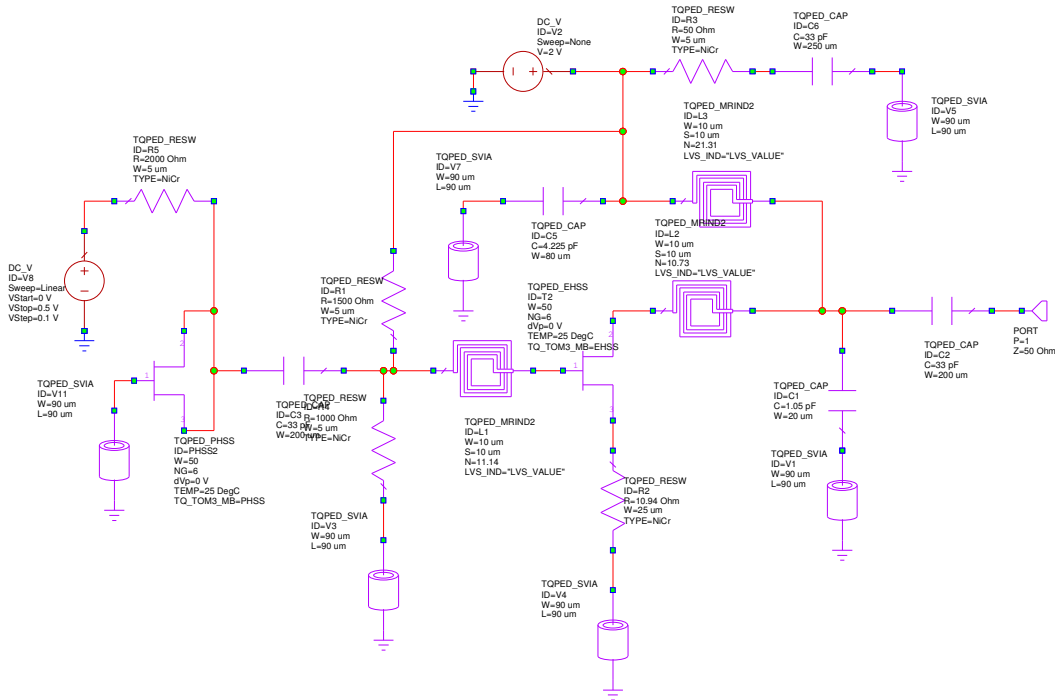


Figure 23: C-Band VCO Complete Schematic

Note: Due to the high density of components of the VCO, it would be difficult to view each component of the schematic; therefore, the reader is recommended to refer to the simulation file to examine the full schematic.

The VCO schematic consists of a direct connection between the “Vara_FET” and the load matching network. The 50Ω termination of the load matching network is removed and a 50Ω port is added to the output of the VCO. In addition, microstrip lines and interconnection microstrip-tees (not shown in Figure 23) are added to make the required connections between components in layout. By adding microstrip interconnection, the parasitics of these elements (inductance and capacitance) would affect the final simulation of the VCO; therefore, the VCO shall be fine tuned after the layout has been finalized. Furthermore, pads are added in the schematic to produce the recommended ground-signal-ground combination for the output port. Details on the creation of the layout shall be discussed in later sections.

The VCO was simulated with the tuning voltage from 0V to +0.5V (0.1V steps) and below is the plotted $|S_{11}|$ through frequency:

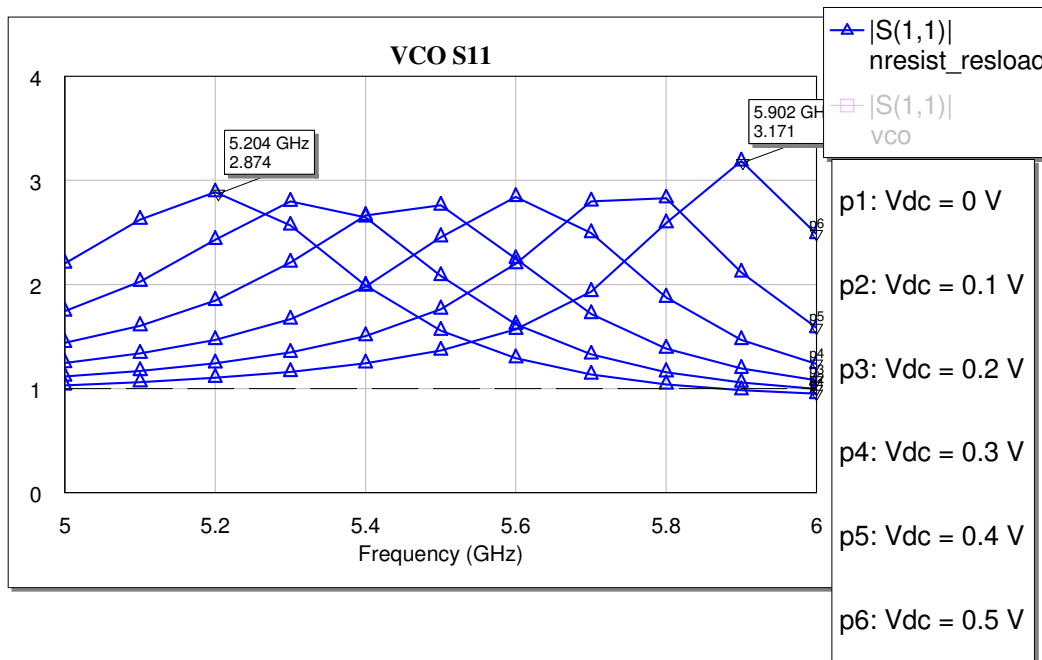


Figure 24: S11 Simulation of the Complete VCO

The $|S_{11}|$ plot suggests that the VCO is potentially unstable and therefore, oscillation shall occur. Though, with the start-up oscillation conditions being satisfied as discussed in prior sections, the VCO shall tune from 5.2GHz to 5.9GHz from 0V to 0.5V, respectively. In addition, it is possible to increase the range of frequency oscillation, simply by applying extended tuning voltage outside of 0V to 0.5V (i.e. -0.5V to +1V); though, as the tuning voltage is increased, the linearity of the varactor deteriorates since the package parasitic becomes the dominating capacitance.

Furthermore, despite the start-up oscillation conditions of the VCO are confirmed, it is necessary to verify if any there any out of band oscillation. The $|S_{11}|$ is plotted from 0.5GHz to 10GHz below:

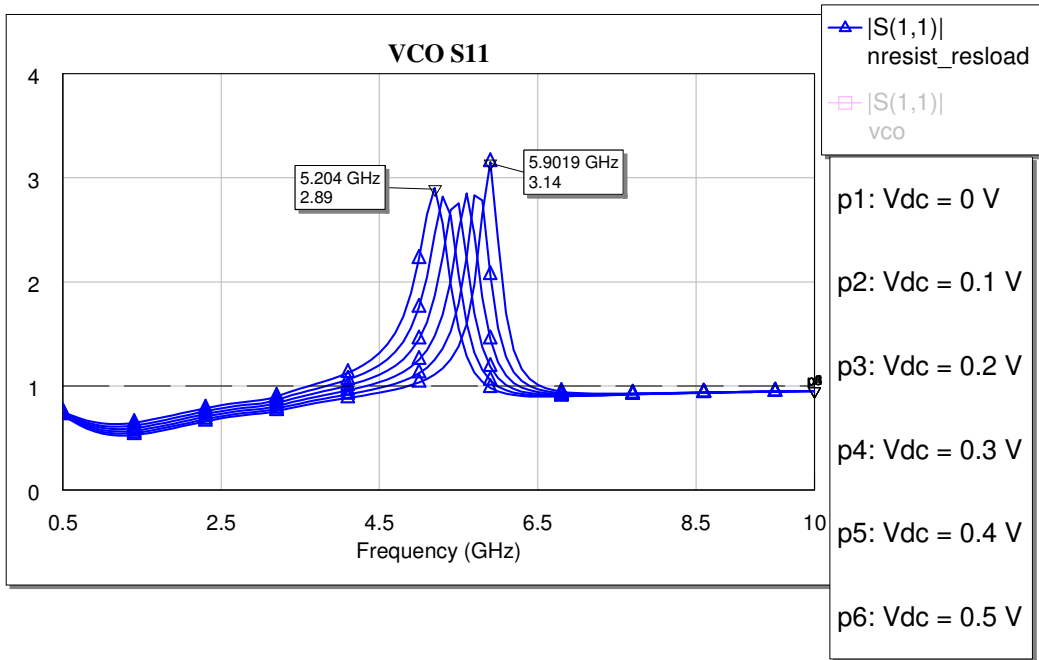


Figure 25: Extended Frequency S11 Simulation of VCO

As shown in the plot above, the $|S_{11}|$ is below one outside of the oscillation frequency band of interest; therefore, it is confirmed that the VCO do not have an out-of-band oscillation issue.

Finally, the bias currents of the VCO shall be checked. Below are plots of the simulated schematic that concentrate on the biasing voltages and currents:

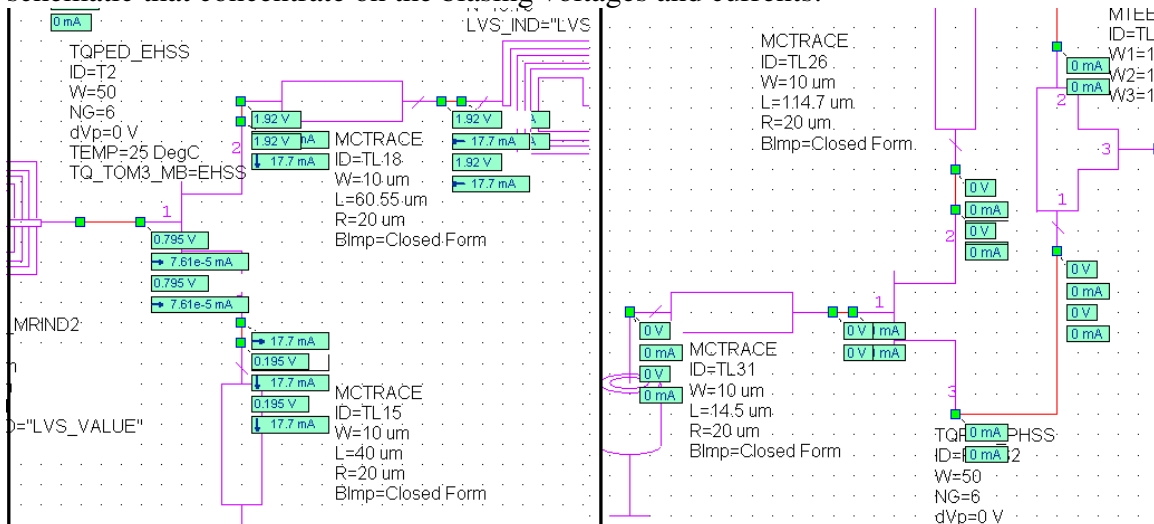


Figure 26: Bias Current of VCO (active circuit and varactor)

The DC source provided +2.0V to the bias-tee circuit of the active circuit and 0V to +0.5V on the bias of the varactor. As shown in the figure above, the drain bias of the

active FET is simulated to be 1.92V with 17.7mA, as compared to the expected of +2.0V and 18mA. Therefore, the simulation is very close to the expected values. In addition, as expected, the gate bias of the active circuit and the bias of the varactor show minimum current. Finally, the source with the de-stabilizing series resistor has 17.7mA of current flowing through, which is acceptable since the resistor is step to have width of 50um (i.e. handles up to 50mA). As a conclusion, the design of the C-Band VCO is completed and all requirements are satisfied.

5.0 PAD LAYOUT DESCRIPTION

The C-Band VCO is placed and layout within a 60um by 60um platform. The 2-D layout of the VCO is shown below:

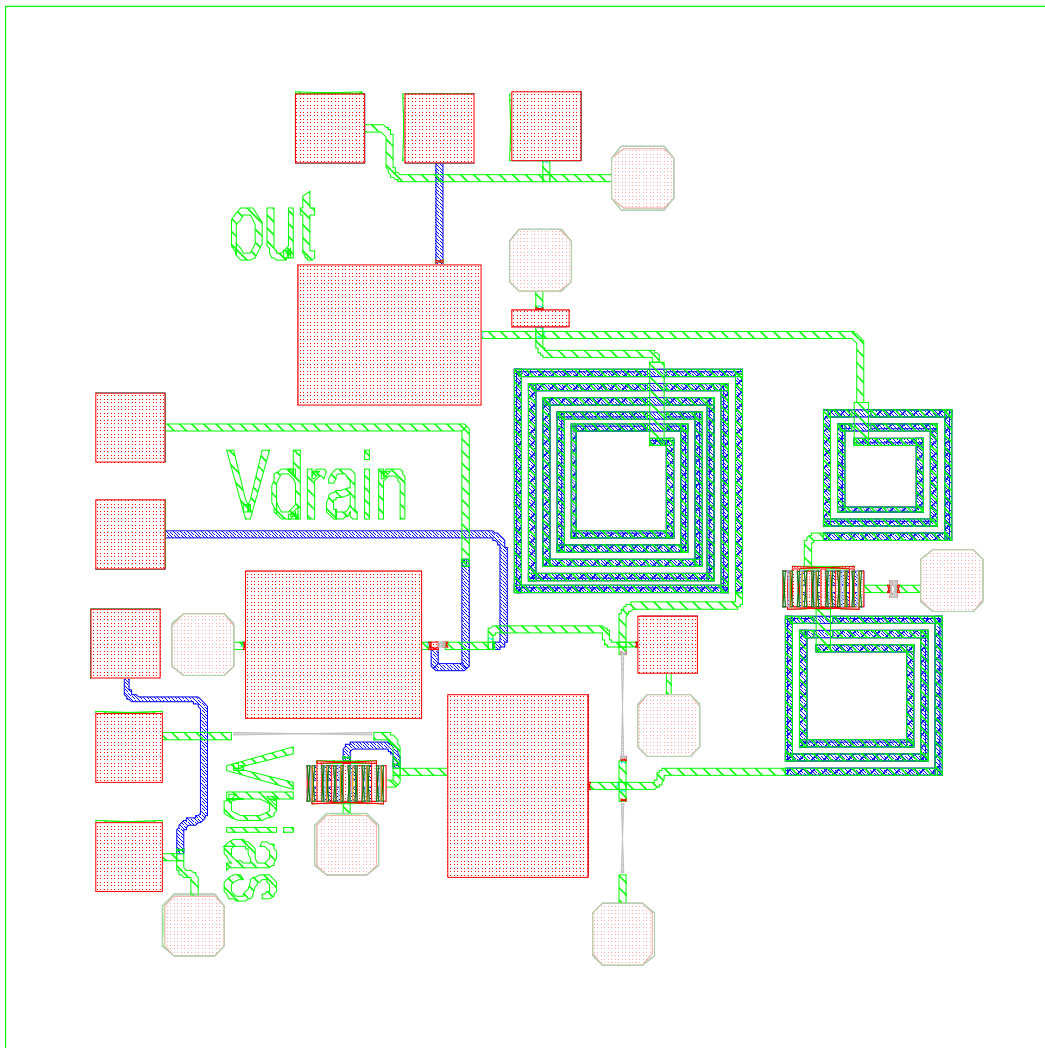


Figure 27: 2-D Layout View of the Complete VCO

The layout has three labeled ports: “Vbias”, “Vdrain”, and “Out”, which represents the varactor voltage bias, drain voltage bias, and VCO output port, respectively. Where appropriate and possible, a ground-signal-ground (GSG) pad configuration is used. The GSG is used for the convenience of testing purposes using the appropriate probes. The GSG is applied to both the “Vbias” and “Out” ports. The “Vdrain” port has only one pad where the DC source shall apply the required voltage level (+2.0V). An additional pad is placed above the “Vdrain” pad; this specific pad is used in case if additional decoupling on the bias-tee circuit is required.

The placement of the components are arranged to minimize the length of microstrip lines, since additional length affects the final performance of the VCO. In addition, the layout consists of three layers: Layer 1 (ground), Layer 2 (metal dielectric), and Layer 3 (metal dielectric). The routing of the microstrip lines utilizes two of the three layers (Layer 2 and Layer 3). The “green” routes represent Layer 2 and the “blue” routes represent Layer 3. It can be observed that by routing on both layers, real estate could be minimized.

Furthermore, ground vias are connected to Layer 1 (ground layer) by default. Though, since the vias connects to both Layer 2 and Layer 3, it is possible that parasitic inductance affects the performance of the final circuit. Therefore, the final layout was simulated to confirm the effects of the microstrip lines and vias have minimal effect on the final output.

Finally, the Design Rule Checker (DRC) was used to scan for any possible errors on the layout prior to sending out for manufacturing. For the VCO layout specifically, the DRC caught errors such as:

- Text Errors: text contains letters are creates sharp angles
- Ground vias: ground vias are placed too close to other components
- Inductors: spiral inductors were placed too close to the routing microstrips

All errors were resolved in layout prior to submitting for manufacturing of the VCO.

6.0 TEST PLAN

This section shall list the required test plan and procedures to compare the measured and the simulated performance of the C-Band VCO. In addition, the test plan shall confirm that all requirements of the VCO are satisfied.

6.1 Short Check

All non-ground pads (“Drain”, “Vbias”, and “Out” port) shall be checked for shorts. The “Out” pad shall be low impedance since it is the drain port of a FET; though, it shall be checked to ensure that it’s not shorted to ground.

Specification: No short shall occur

6.2 Bias Current and Voltages

The “Drain” pad shall be applied with +2.0V from a DC source. This is the power supply of the VCO. The DC source shall apply the positive output to the “Drain” pad and the negative (ground) output shall apply to the ground pad of the VCO. The DC source should be able to measure the current drawn from the VCO. The typical current drawn shall be 18mA.

Specification: +2.0V +/-5%; 18mA +/-5%

6.3 Frequency Range

This test shall confirm the specification of tuning frequency range. After the “short” test is completed and passed, apply the required power supply to the “Drain” pad and another DC source to the “Vbias” pad with 0V. Connect the “Out” pad to the spectrum analyzer. Measure and record the tuned frequency, power level of the carrier, and the second harmonic. Repeat the procedure by sweeping the “Vbias” voltage from +0.1V to +0.5V (0.1V steps)

Specification: Tune voltage of 0V to +0.5V (0.1V step)
Frequency range of 5.2GHz to 5.9GHz
Power Level (to be determined)
Second Harmonic (to be determined)

Note: One can extend the “Vbias” sweeping range (i.e. -0.5V to 1.0V) to explore the limitation of the varactor.

6.4 Out-of-Band Oscillation

This test shall confirm that out-of-band oscillation is not an issue. Particularly, this test shall scan if there is oscillation outside the frequency band of interest. Power up the VCO with the required supply voltage at the “Drain” pad. Connect the “Out” pad to the spectrum analyzer. Apply +0.3V to the “Vbias” pad. Scan from 0Hz to 4.5GHz and from 6.5GHz to 10GHz on the spectrum analyzer and observe for unexpected oscillation.

Specification: Out-of-band oscillation shall not occur.

7.0 Summary and Conclusions

The simulated VCO in the Microsoft Office meets all electrical requirements using TRIQUINT lumped and active elements. The design of the VCO is based on the negative impedance theory, which uses the start-up oscillation condition of a series resonance type oscillator. In addition, the layout of the VCO were placed and routed to fit into the 60um by 60um platform. Due to the effects of the interconnections and microstrip line connections of components, the VCO was simulated to confirm that all electrical requirements are still satisfied.

Furthermore, there are certain drawbacks of the finalized VCO. For example, to save real estate of the VCO layout, the gate bias of the active FET is designed to be dependent on

the power supply of the VCO (i.e. drain bias of the active FET). As a result, there is minimum flexibility of adjustment to the V_{gs} . In addition, the schematic and layout do not include extra pads on the gate and source port of the active FET.

Overall, this project to design a voltage controlled oscillator in AWR's Microsoft Office provided another power tool to simulate electrical circuit designs as compared to the likes of ADS and Eagleware. Though, it would be very interesting to compare the simulated results and the measured results after the VCO is manufactured.

More considerations of the layout would help to achieve better overall designs. For example, placement of components on layout could affect the overall performance. Though, it might be minor, but as frequency of interest becomes higher, the placement of component could be critical. In addition, the thought process of the design shall start from the theory and background stage up to the testing stage of the design itself. For example, on the testing stage of the VCO, it becomes critical to provide sufficient amount of test pads for verification of individual section of the circuit. Since it is a MMIC design, it is almost impossible for one to use test equipments to probe certain area of the design, therefore, sufficient test pads shall be implemented.

In addition, since the concept of the VCO design has been outlined in existing publications, the circuitry stage of the VCO was not as time consuming; though, using the software was more time consuming since this is the first time user. As more functionalities of the software are discovered and learned, it is apparent how powerful the simulation tool could become. For example, the tuning capability of component values; as the components values are tuned, the simulation provides live updates of the results; whereas, other simulation tools required an additional step to start the simulation after modifications to the values of components. In addition, the software's EM extraction capability allows users to route the design on layout in which it extracts all the routes to the schematic; this is a tremendous advantage of the software since it eliminates the addition of microstrip lines and interconnections to the schematic; which would result in a "crowded" schematic.