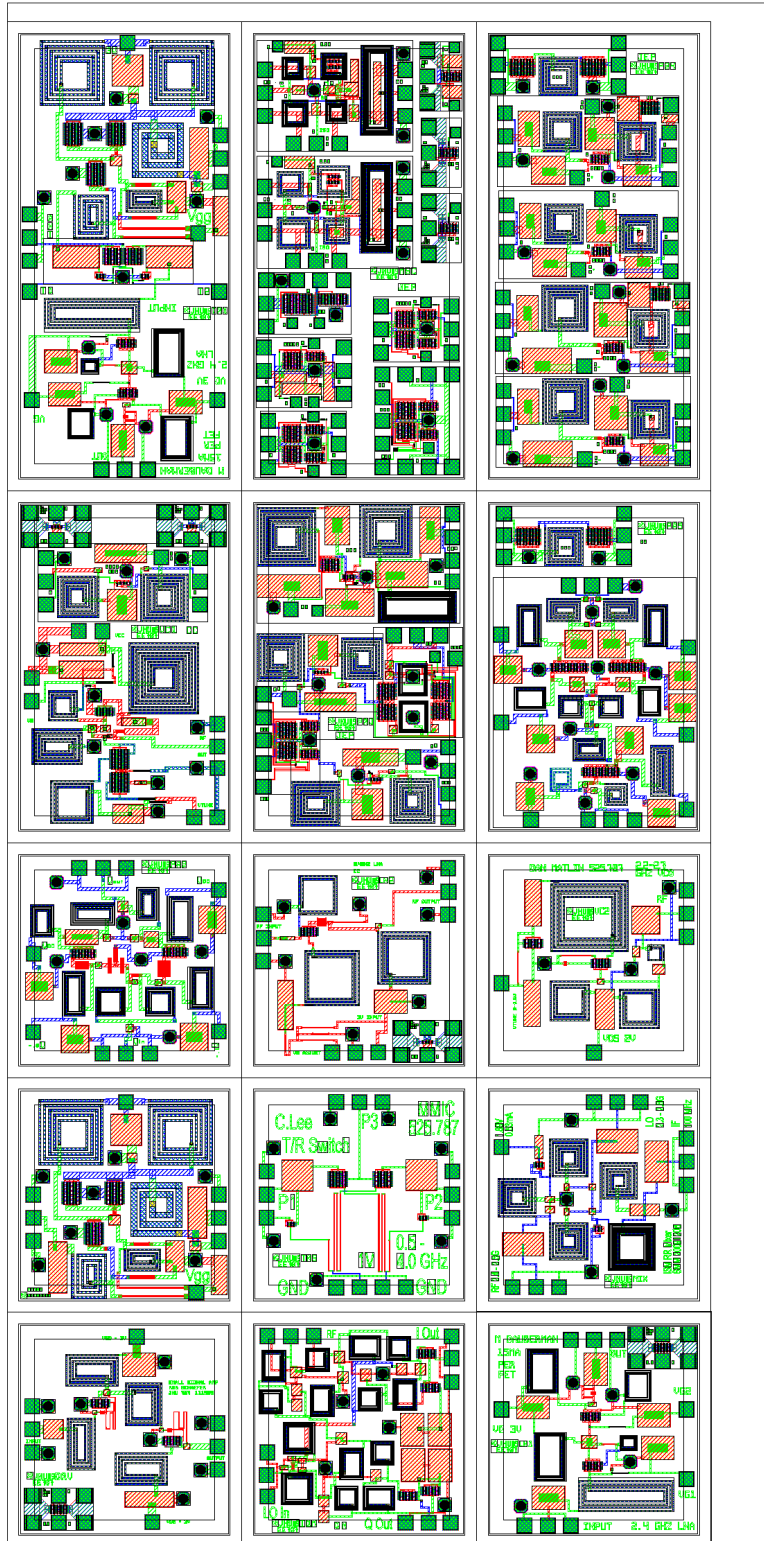


**Fall 2009 JHU EE787 MMIC Design Student Projects**  
**Supported by TriQuint, and Agilent Eesof**  
**Professors John Penn and Dr. Michel Reece**

Driver Amplifier— Robert Schaefer  
 Power Amplifier 1— Rowland Foster  
 Low Noise Amplifier 2— Clay Couey  
 Up/Down Mixer – Steve Moeglein  
 Volt. Cont. Osc. 1— Clay Couey

Low Noise Amplifier 1— Michael Dauberman  
 Power Amplifier 2— Ken McKnight  
 I/Q Mixer – David Nelson  
 T/R Switch – Chue Lee  
 Volt. Cont. Osc. 2— Dan Matlin



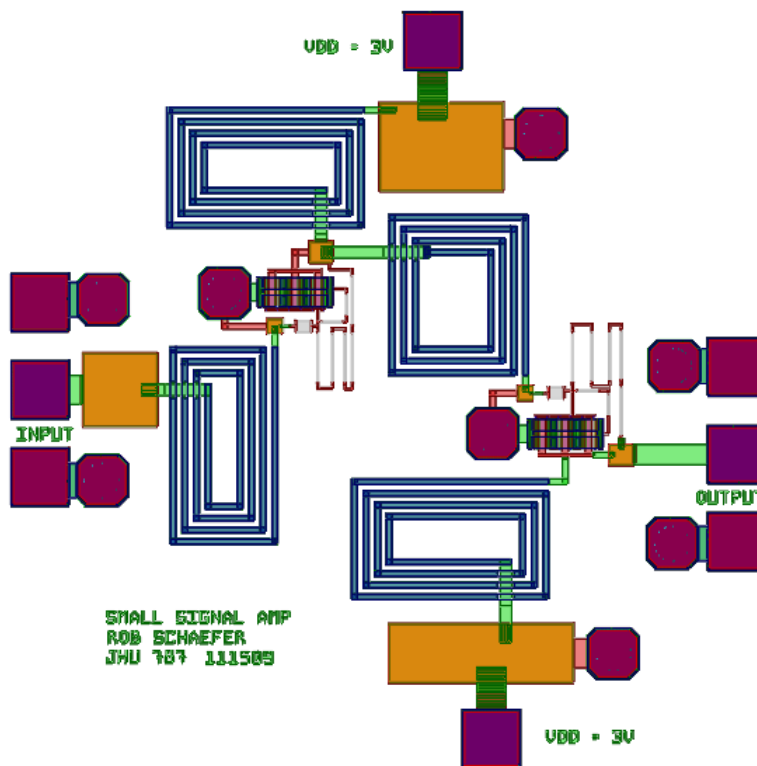


# Post Amplifier (Small Signal Amplifier)

Designer: Rob Schaefer

JHU 525.787 MMIC Design (Fall 09)

12/07/09



## Abstract

This paper documents the design of a two-stage post amplifier (small signal amplifier) for a frequency range from 2.4 to 2.5 GHz. Per the simulations, the amplifier has 23.5 to 24.3 dB of gain, input and output return losses less than -15.6 dB, and uses ~23mW of DC power. The transistors used for this design were both 300um Emode pHEMTs biased at  $V_{ds}=3V$ ,  $I_{DS}=3.5mA$ , and  $V_{gs}=0.45V$ . The design process used for this design is the Triquint TQPED 150mm, 0.5um pHEMT process. The design program used was AWR Corporation's Microwave Office (Version 9.01).

## Introduction

The two-stage post amplifier design started with the desire for an amplifier with ~22 dB of gain, good input and output return loss, low DC power consumption, moderate noise figure, and moderate power efficiency. This design achieves a gain of 23.5 to 24.3 dB, input return loss better than -15.6 dB, output return loss better than -16.7 dB, a noise figure better than 3.2 dB, a PAE of 45.5% at the P1dB point, and uses ~23mW of DC power. In the following sections of this paper I will present and discuss the requirements/goals, the design process, the simulated results, the module considerations, the layout and I/Os, and the test plan for this amplifier design.

## Block Diagrams

The post amplifier designed for this project was part in a larger system, show in Figure 1 below.

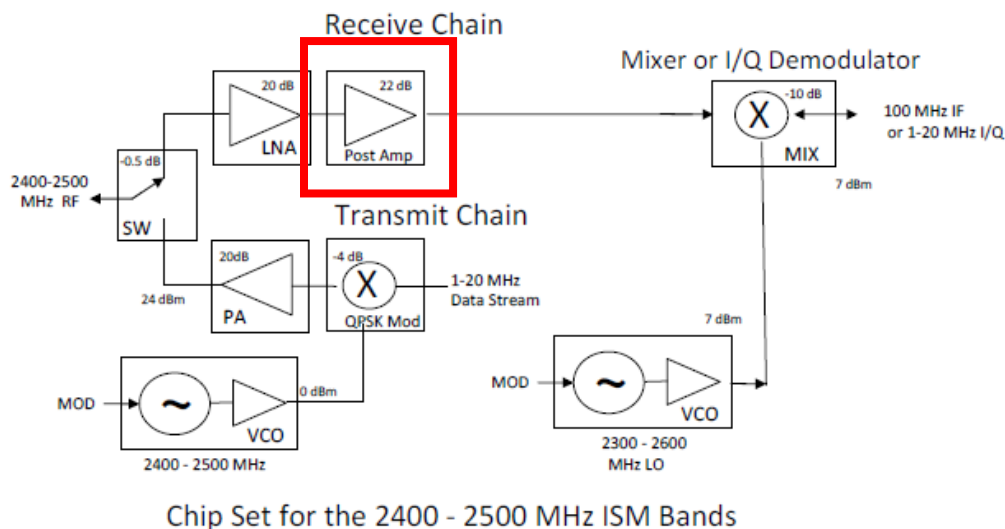
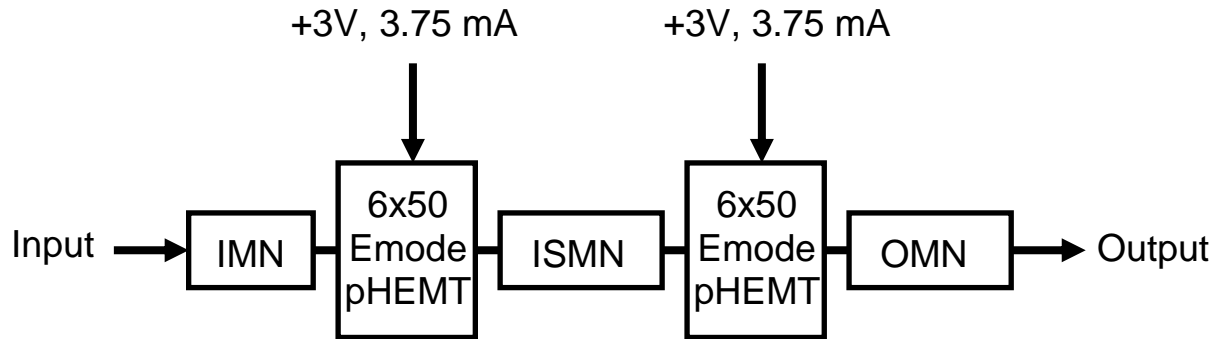


Figure 1

The post amplifier is part of the receive chain, following a Low Noise Amplifier and followed by a mixer or I/Q Demodulator. Module level requirements and other considerations that pertain to my design will be discussed in later sections of this paper.

A simple schematic for the Post Amplifier itself is provided in Figure 2. The amplifier is a two-stage design, with both the first and second stages using 6x50 (300um) E-mode pHEMTs. The design is biased at +3V and draws ~7.5mA of current (3.75mA per stage). Further design details will be discussed later in this paper.



**Figure 2**

### Requirements/Goals

The only true requirement placed on this design was to have at least 22 dB of gain over the frequency range of 2.4 to 2.5 GHz. Aside from this several goals were created for the design. As it is a small signal amplifier, it was desired to have a good input and output return loss. It was also thought practical to design the amplifier for unconditional stability, moderate DC power consumption, PAE, and noise figure (although not necessarily at the cost of the primary requirement). Using a voltage supply of 3V was also a preliminary goal. Table 1 below presents the requirements and goals for this design along with what I was able to achieve as far as simulated results.

**Table 1**

Parameter	Specification / Goal	Expected Performance (Triquint)
Frequency	2.4 to 2.5 GHz	2.4 to 2.5 GHz
Drain Voltage	+ 3.0 V	+ 3.0 V
DC Power	< 45 mW	22.65 mW
Gain	22 dB	23.5 to 24.3 dB
Gain Flatness	+/- 1 dB	+/- 0.4 dB
Noise Figure	< 3 dB	3.2 dB max
Input Return Loss	< -15 dB	< -15.6 dB
Output Return Loss	< -15 dB	< -16.7 dB
# of Stages	2	2
Size	60 x 60 mil	60 x 60 mil
PAE	TBD	45.5 % at P1dB
P1dB	TBD	15.0 dBm out
Stability	$\infty$	$\infty$

## Design

The design approach I took for this amplifier was to begin with a basic design by choosing an arbitrary bias point (but still using 3V for the  $V_{ds}$ ), conjugately matching a single stage, putting two stages together, and seeing where I stood as far as my 22dB of gain requirement. From there I created a second design where I was able to cut back on the gain in order to reach some of my other design goals. A more detailed description of my design process follows.

I initially looked at the DCIV curves for the E-mode pHEMT devices. For my first design I had chosen a bias point at  $V_{ds} = 3V$ ,  $I_{ds} = 7.5mA$ , and  $V_{gs} = 0.5V$ . To reduce the amount of DC power consumed by each stage, for my final design I changed the DC bias point at  $V_{ds} = 3V$ ,  $I_{ds} = 3.5mA$ , and  $V_{gs} = 0.45V$ . I figured this was far enough away from the pinchoff voltage (0.35V) to be safe. The DCIV curves for a single E-mode device are shown below in Figure 3.

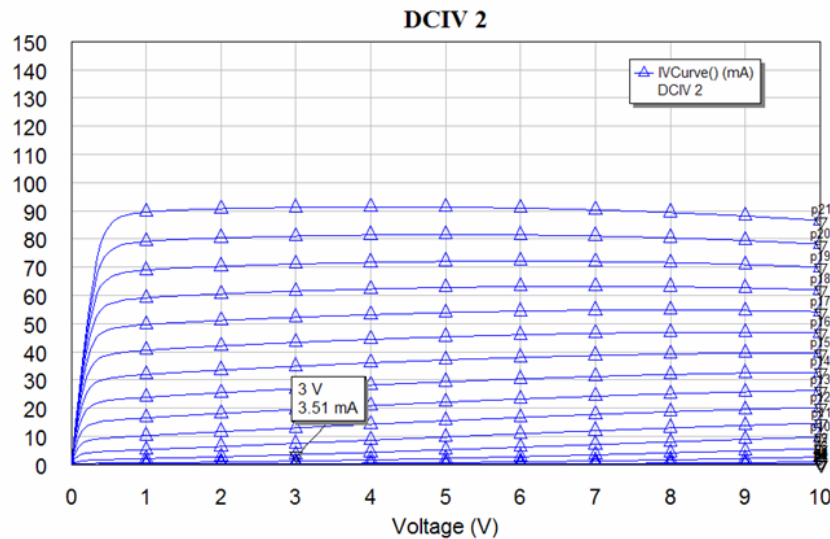


Figure 3

I then self-biased the pHEMTs using a voltage divider with the configuration shown in Figure 4. I used larger resistive values in the end to help with stabilizing the devices.

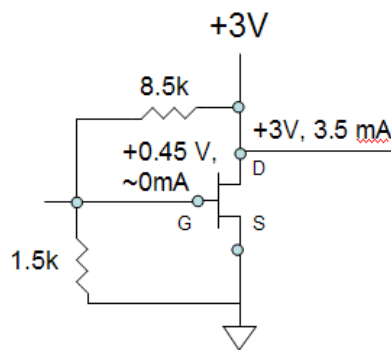
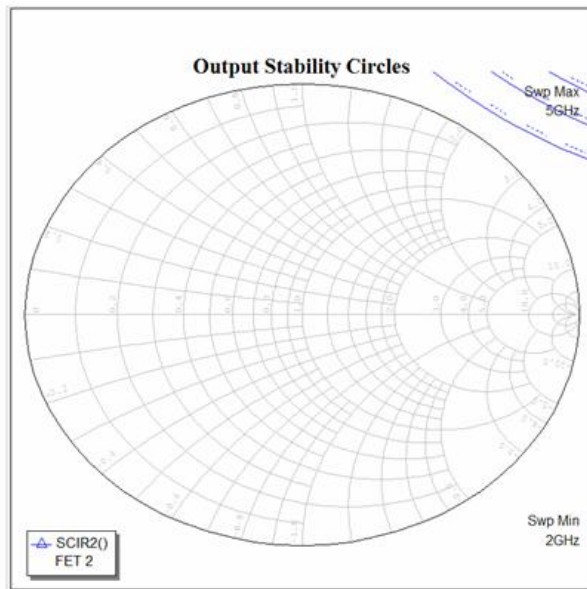
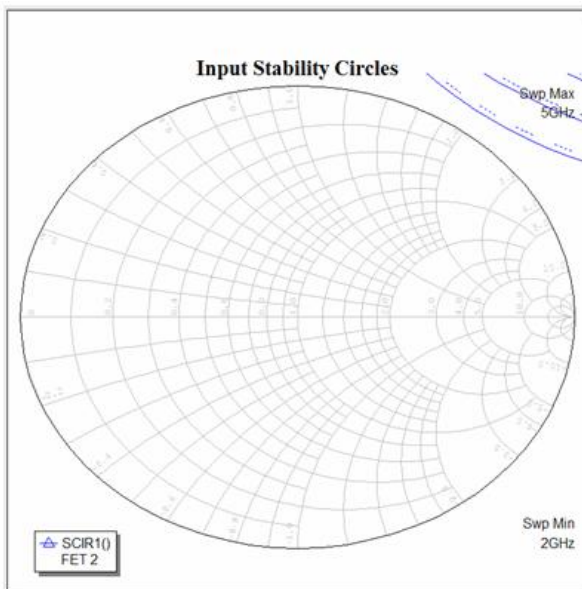
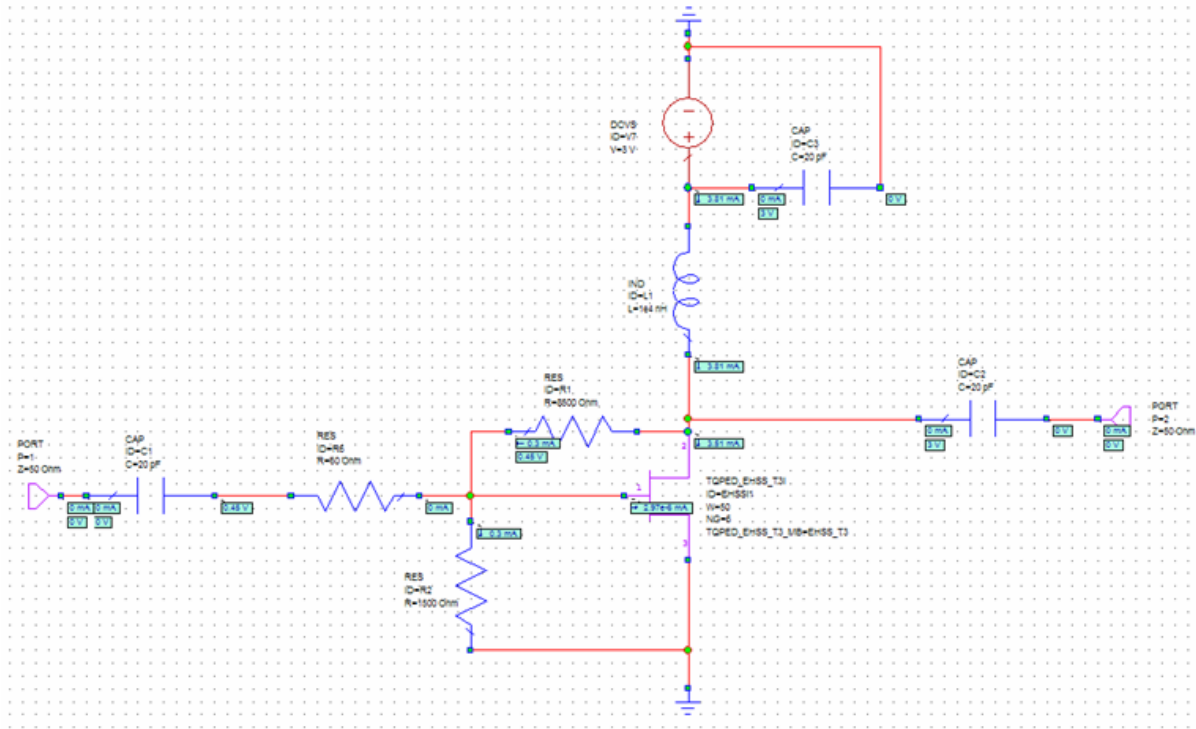
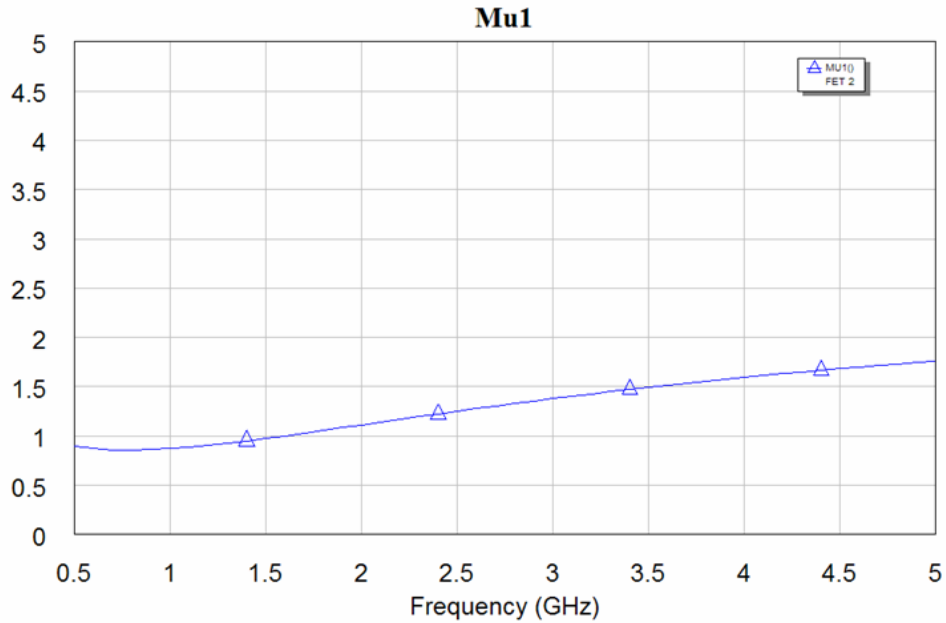


Figure 4

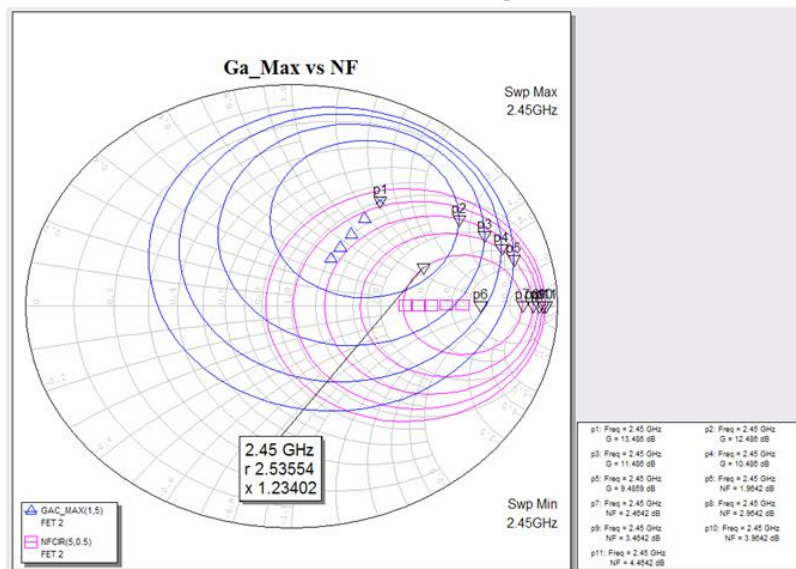
Next, I looked at stabilizing the transistor. I found it easiest to stabilize the design by adding a series 60 Ohm resistor to the gate, and as I mentioned above, I used larger values for my voltage divider to improve the stability as well. Although the design at this point was not unconditionally stable, as desired, adding real components helped to meet this goal. A schematic of the stabilized device as well as the resulting Mu1 plot and stability circles (from 2 to 5 GHz) are shown below in Figure 5.



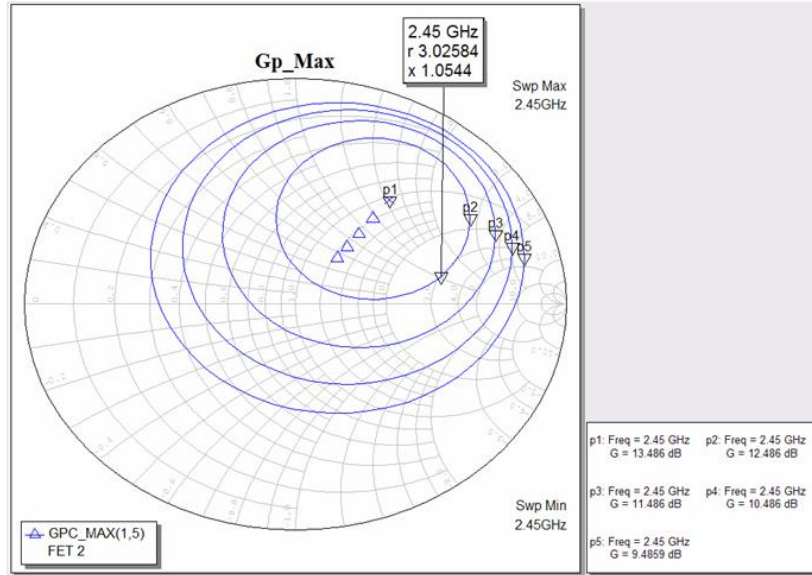


**Figure 5**

The next step in my design process was to find the appropriate input and output matches to achieve my goals. As this was a small signal amplifier design I began by matching to the simultaneous conjugate match. With this particular match I had great input and output return losses and a lot of small signal gain, but I additionally wanted to reduce my noise figure in case the design might be able to be used in another system (would be more of a selling point while also meeting the goals set forth for this project's system). So, I additionally looked at the noise figure circles and found a point where I wouldn't have to tradeoff too much gain but could reduce the noise figure and with some tuning was able to still achieve good input and output return losses. The gain and noise figure circles are shown below in Figure 6.



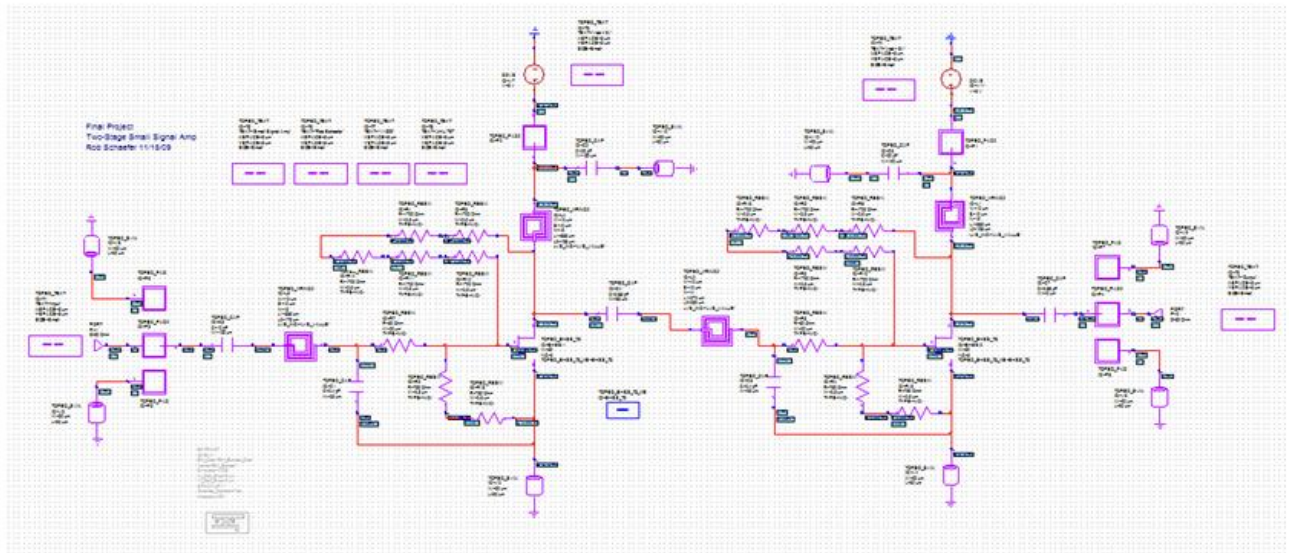




**Figure 6**

The Smith Chart Matching program was used to match to the chosen points. The single stage design was duplicated and cascaded to create the initial two-stage design. The interstage was then tuned to reach the desired performance goals.

The final steps of the design were the changing from ideal to real (Triquint supplied) elements, to which the design had to be further tuned to maintain its performance, and then the laying out of the elements and use of the extraction tool for the interconnecting traces. In the Simulations section that follows this section, the simulations for this final design (with extracted traces) are presented. Figure 7 below shows the final schematic for the two-stage post amplifier design.



**Figure 7**

## Simulations

The plots below correspond to the simulated final layout of the two-stage post-amplifier design. This includes the use of Triquint elements and extracted interconnect traces from the layout.

Looking at the DC analysis, the simulation in Figure 8 shows  $V_{ds} = 3V$ ,  $V_{gs} = 0.45V$ , and  $I_{ds} = 3.47\text{ mA}$  for the first stage and  $V_{ds} = 3V$ ,  $V_{gs}=0.45V$ , and  $I_{ds} = 3.78\text{ mA}$  for the second stage.

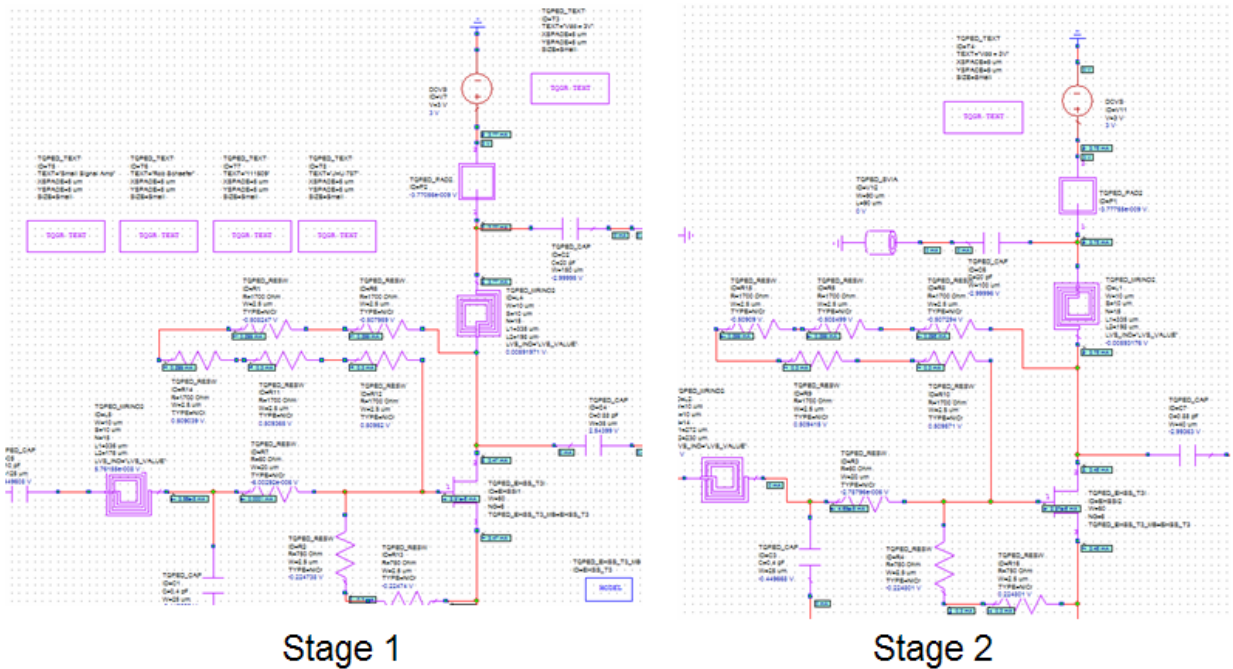


Figure 8

Looking at S21, the value for the gain ranges from 23.5 to 24.8 dB. This is relatively flat ( $\pm 0.4\text{ dB}$ ) across the band. A plot of S21 is shown in Figure 9.

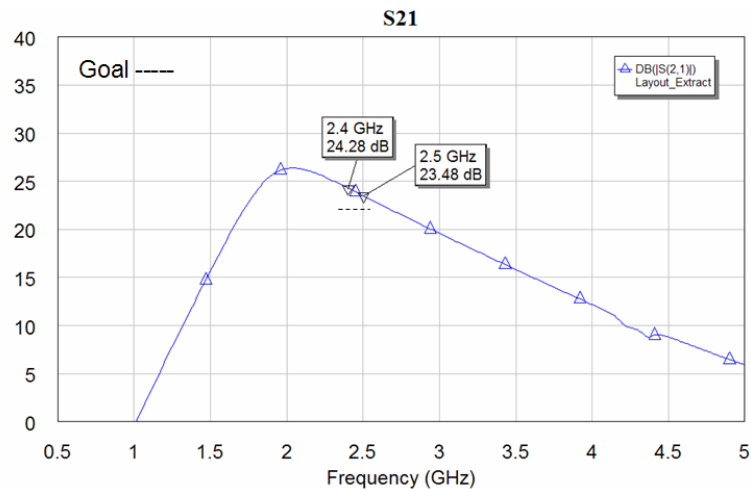


Figure 9

Looking at the input and output return losses, S11 values are better than -15.6 dB and S22 values are better than -16.7 dB. A plot of S11 and S22 is shown in Figure 10.

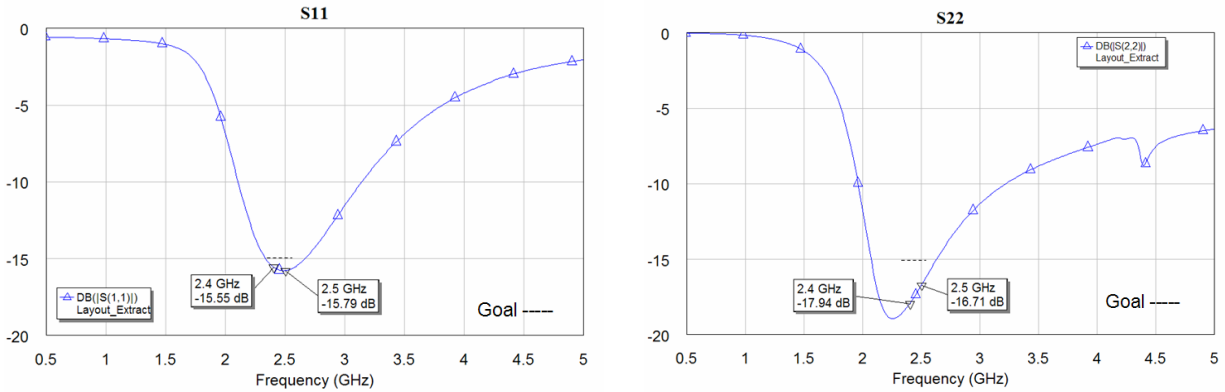


Figure 10

Looking at the stability (Mu1) plots the values are all above 1, from 0.1 to 10 GHz. Shown in Figure 11 below are the Mu1 plots for the individual stages as well as the amplifier as a whole.

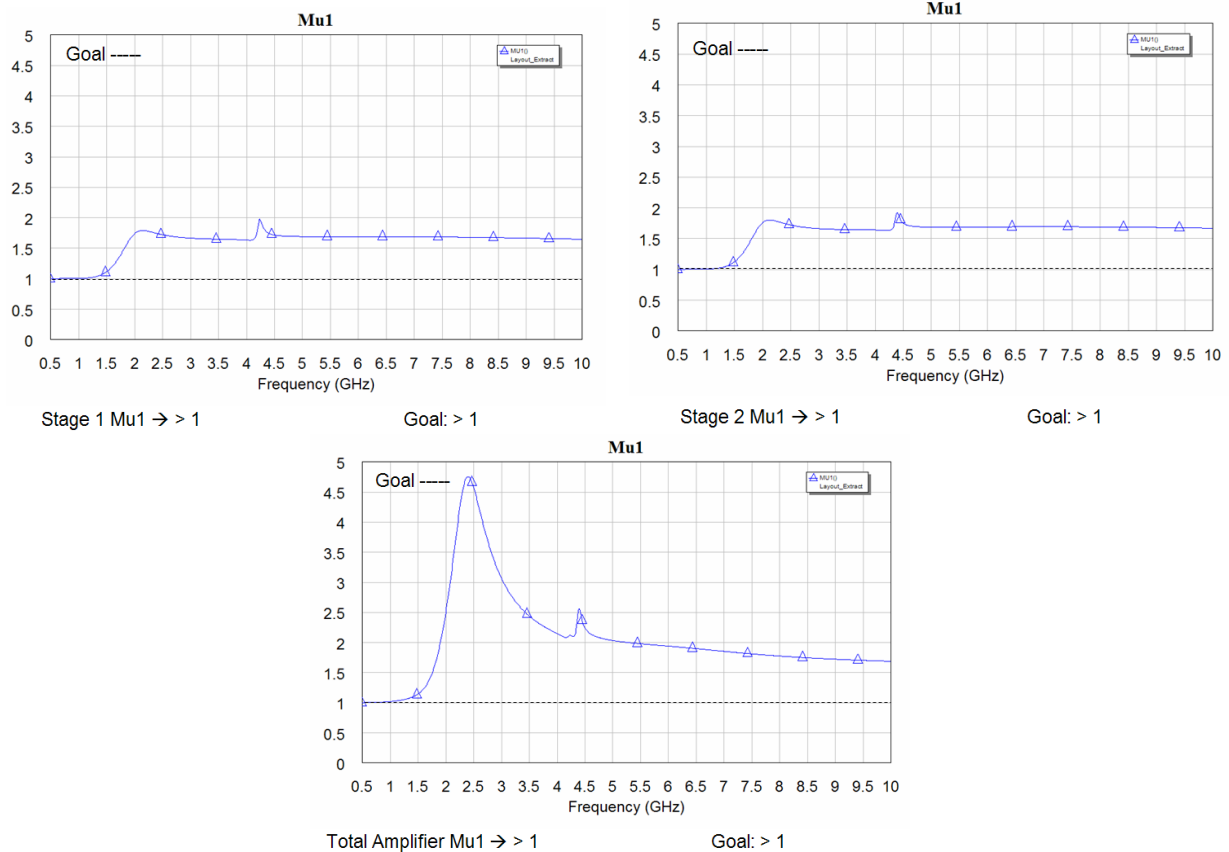


Figure 11

Looking at the noise figure plots, the value is ~ 3.2 dB across the band. I had set a goal of 3dB for noise figure and ended up 0.2 dB above this goal. Fortunately, since noise figure is not a primary goal for a small signal amplifier, this value was good enough. The noise figure plot is shown below in Figure 12.

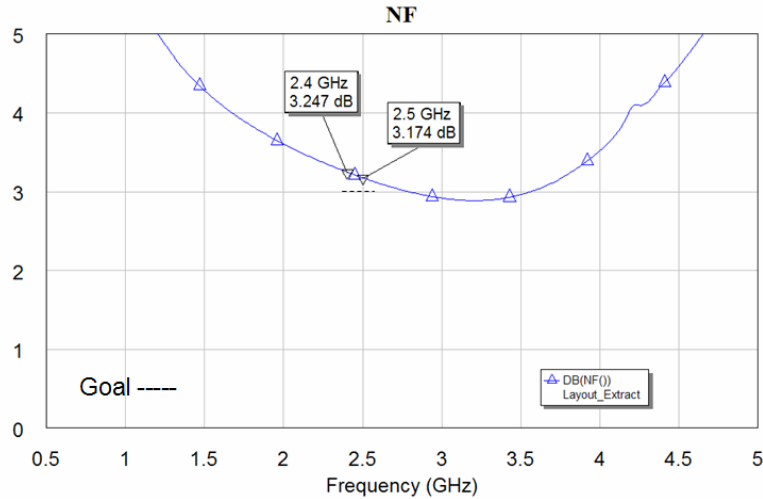


Figure 12

Finally, looking at the Input Power vs. Output Power and PAE, the amplifier has an output power of 15 dBm at its 1dB point (which is at -8 dBm in), and the PAE at this point is 45.5%. Plots are shown below in Figure 13.

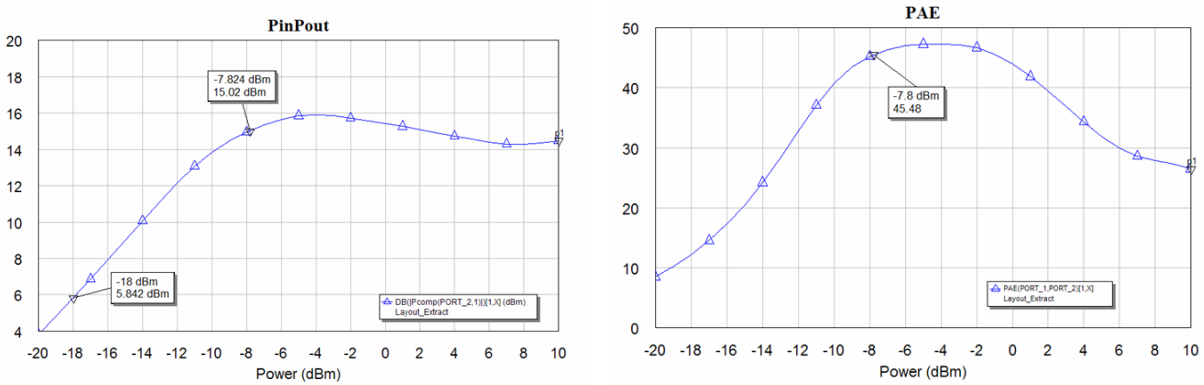


Figure 13

## Tolerancing

For this design I varied the biasing voltage and capacitor sizes to see the effects this would have on the simulated results. I also checked the current carrying capacities of the metal traces that I used to connect up the components in my layout.

The positive bias voltage is nominally +3V for this design. I simulated the design with bias voltages ranging from +2.6 to +3.4V in 0.2V steps. The largest concern I had with this was that I had biased relatively close to the pinch-off voltage of the pHEMT (450mV was the design  $V_{gs}$  and the Triquint manual gives a nominal pinch-off voltage of 350mV). With the voltage divider

I have in this design, +2.6V to 3.4V Vds relates to 0.39V to 0.51V Vgs. Looking at the plotted results at 2.45 GHz (center of band of interest), S21 changes from 15.4 to 26.9 dB, S11 changes from -11.4 to -17.4 dB, S22 changes from -12.8 to -21.9 dB, the noise figure changes from 3.2 to 3.5 dB, and the Mu1 values are all above 1, but increase in value as the voltage increased. Plots are presented below in Figure 14.

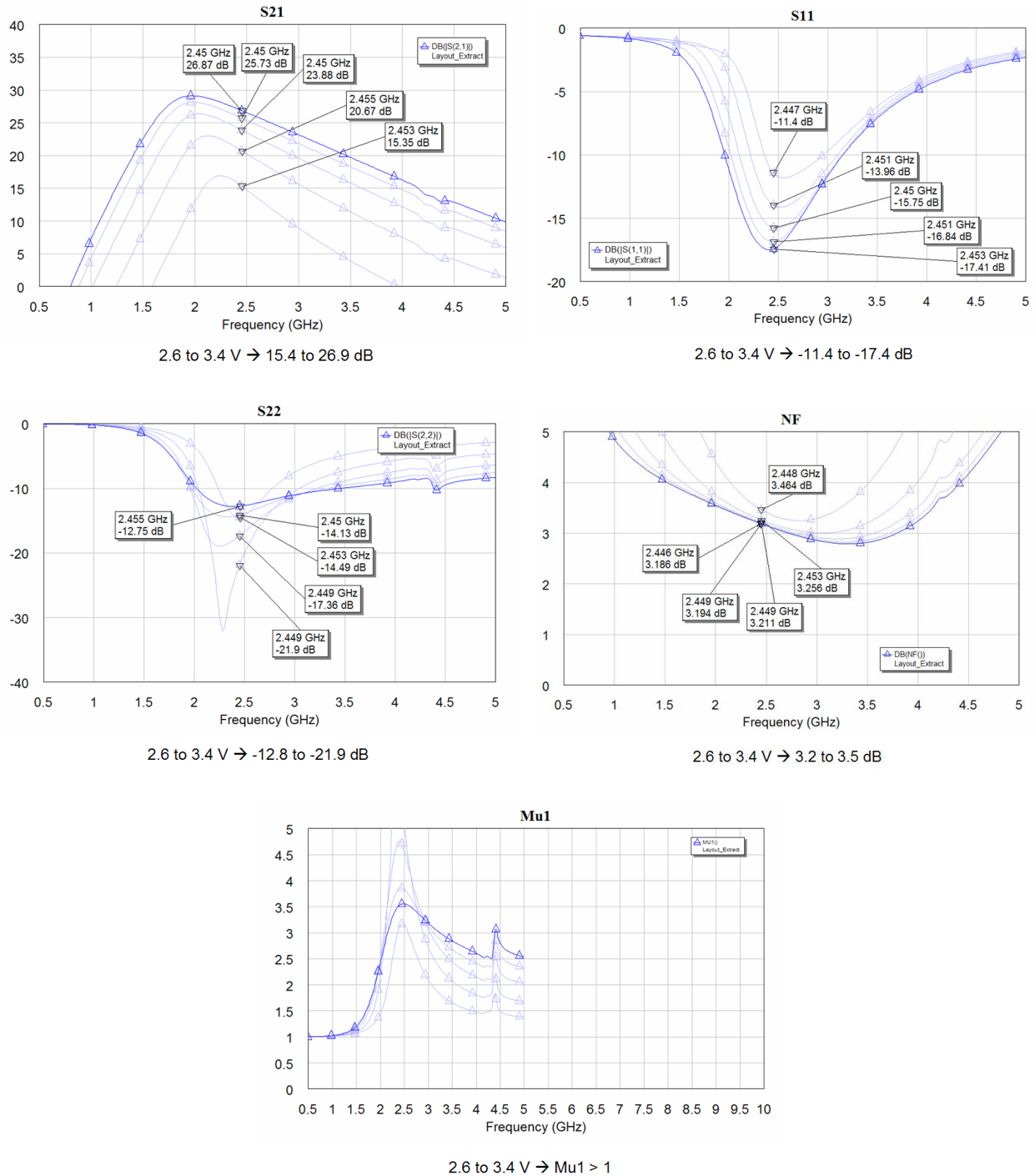
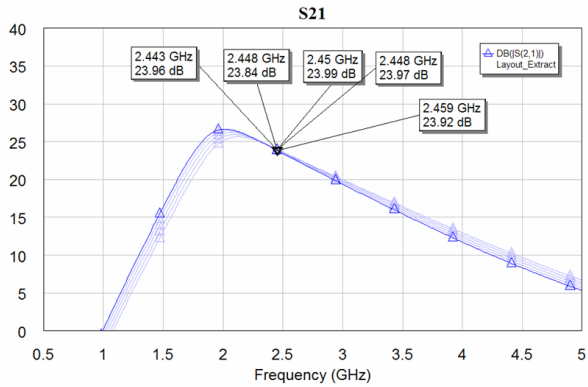
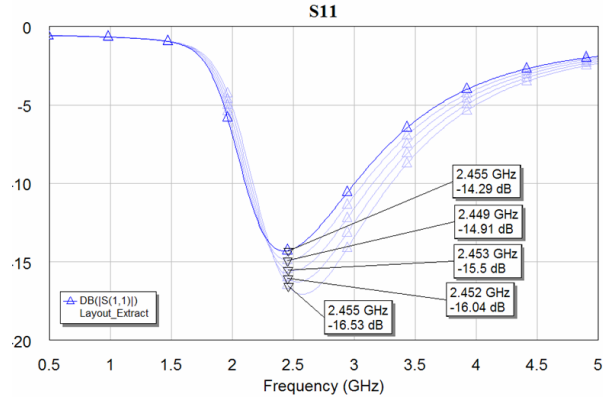


Figure 14

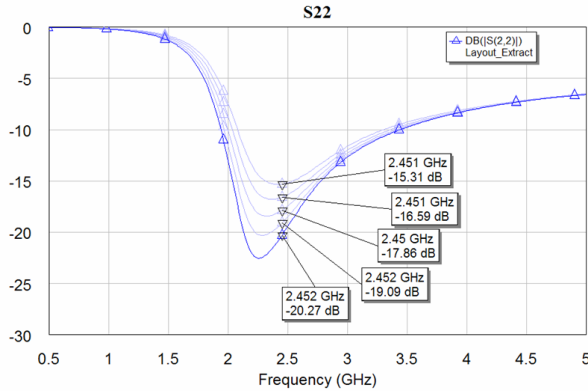
For checking the tolerance on the capacitors, I changed the capacitor values from -10% to +10% in 5% steps. S21 values were pretty consistent, changing only from 23.8 to 24 dB. S11 values changed from -14.3 to -16.5 dB. S22 values changed from -15.3 to -20.3 dB. Noise Figure values changed from 3.2 to 3.3 dB. Mu1 values were all above 1 and only around the band of interest did the Mu1 values seem to increase. The plots described above are shown below in Figure 15.



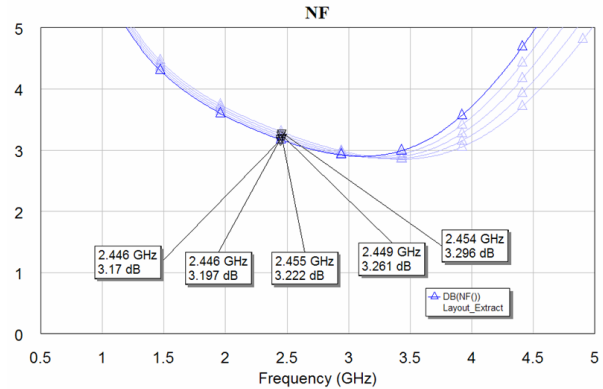
+/- 10% change in capacitance → ~24 dB



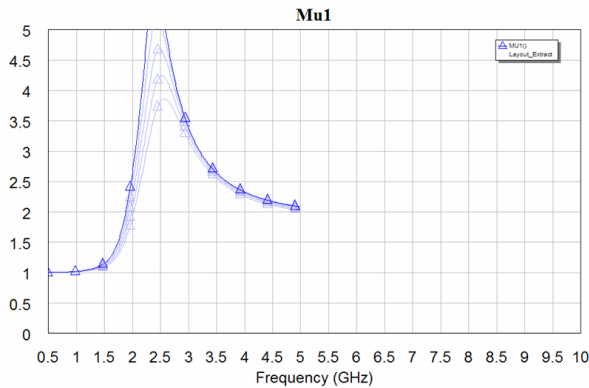
+/- 10% change in capacitance → -14.3 to -16.5 dB



+/- 10% change in capacitance → -15.3 to -20.3 dB



+/- 10% change in capacitance → 3.2 to 3.3 dB



+/- 10% change in capacitance → Mu1 > 1

**Figure 15**

Finally, I checked the line widths of the metal connections between components in my layout. Specifically, I was concerned with the current carrying capacities of the lines that would be experiencing a high current. I checked both the resistors in my biasing network as well as the lines from the DC pads to the pHEMTs. The Triquint design guide says that the NiCr resistors can handle 1 mA/um and the width of the resistors in my design are 2.5 um, therefore they can carry 2.5 mA. These resistors should see 0.3 mA of current, nominally, so they should be ok. The resistor location and analysis is shown below in Figure 16.

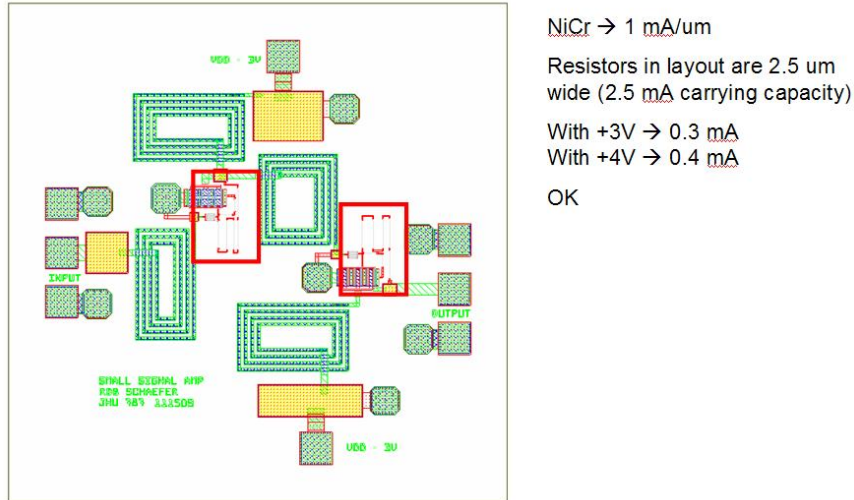


Figure 16

The Triquint design manual says that Metal 0 traces can handle 1.5 mA/um and Metal 1 can handle 9 mA/um. I actually had to increase some of my line widths to give myself some margin, so in the end the narrowest Metal 0 trace was 20 um wide and the narrowest Metal 1 trace was 10 um wide (amounting to being able to carry 30 mA of current on Metal 0 and 90 mA of current on Metal 1). From the DC analysis, with +3V, the max current these traces would see is 3.8 mA, however, with an increase in voltage (+4V for example), they could see up to 20.6 mA of current. The trace location and analysis is shown below in Figure 17.

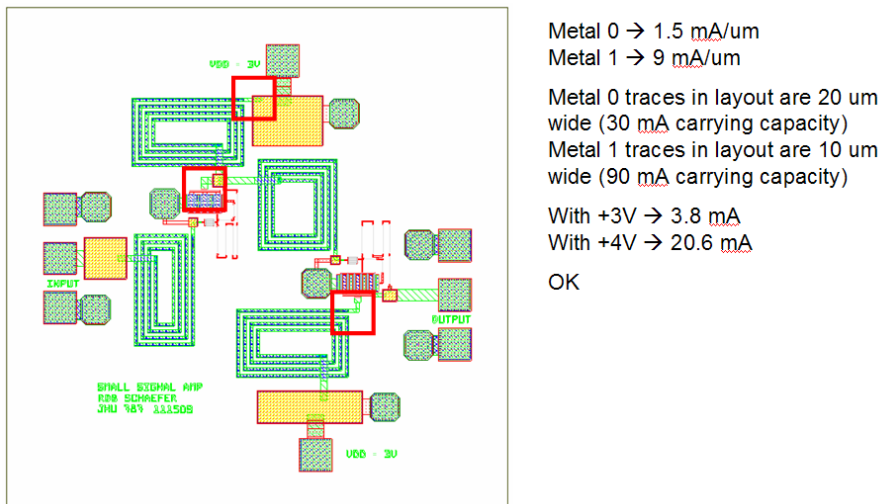


Figure 17

## Module Considerations

Part of the process for this design was to consider the effects my design would have on the chips on either side of my chip in the receive path and vice versa.

A low noise amplifier precedes my post amplifier. What I considered here was how good the match would stay if these two chips were placed in series. Both amplifiers were designed to 50 ohms, but putting the two designs together still might yield not as good a match as expected. Unfortunately, at the time of this report being written I did not have s2p data from the LNA design, but the simplest resolution seemed to be to design an attenuator to be placed between the two amps to ensure a good match. I designed a quick Tee attenuator shown below in Figure 18. My amplifier was not designed with the addition of an attenuator in mind, so adding this to my design would bring my gain below the 22dB spec, but I leave this as a future consideration with a redesign of the amplifier.

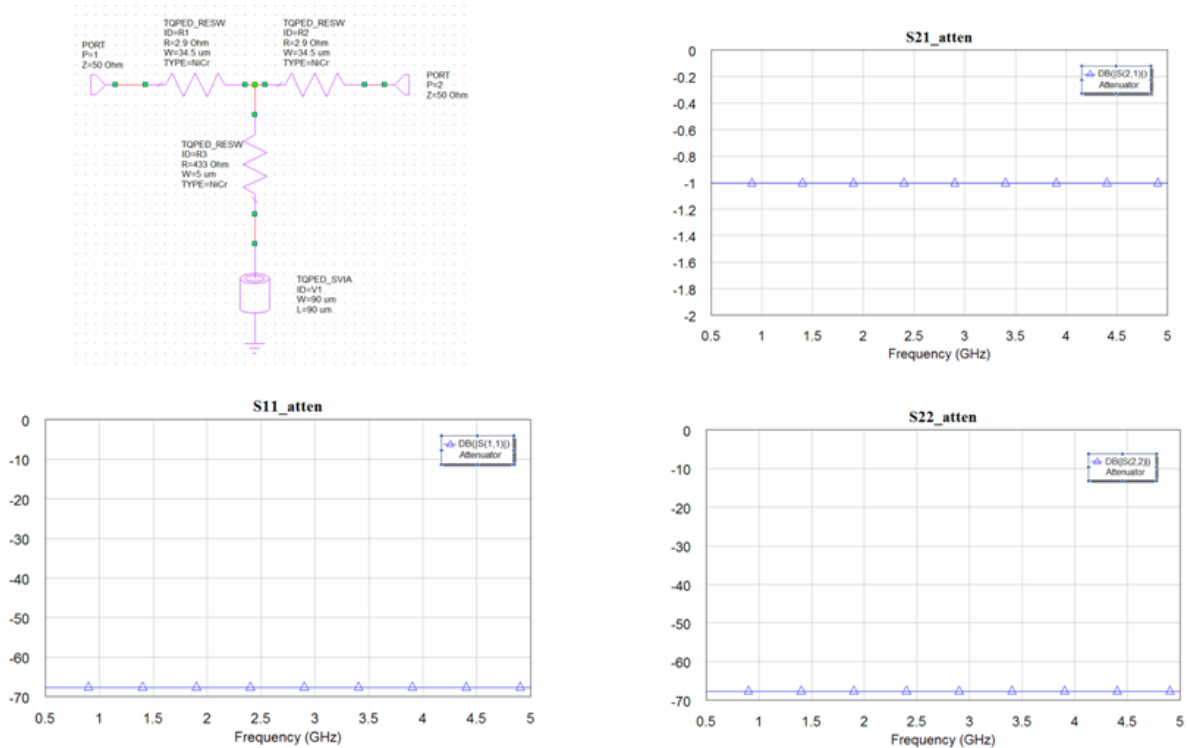


Figure 18

A mixer follows my amplifier in the receive chain. What I considered here was the filtering out of unwanted signals. In the top level block diagram there is not a filter anywhere along the receive chain meaning all sorts of unwanted signals and spurs could reach the mixer. To help resolve this I designed a band-pass filter that would probably be best placed closer to the receiver so that the unwanted spurs are not amplified, but I placed it between my amplifier and the mixer for this theoretical design. The BPF has a relatively low loss of -1.9 dB in the pass-band. The BPF has its -3dB points at 1.9 and 2.9 GHz, so it is not a terribly narrow filter. The return losses



do look good though as the input return loss is better than -15dB and the output return loss is better than -19.7 dB. Below in Figure 19 are the schematic and plots described above.

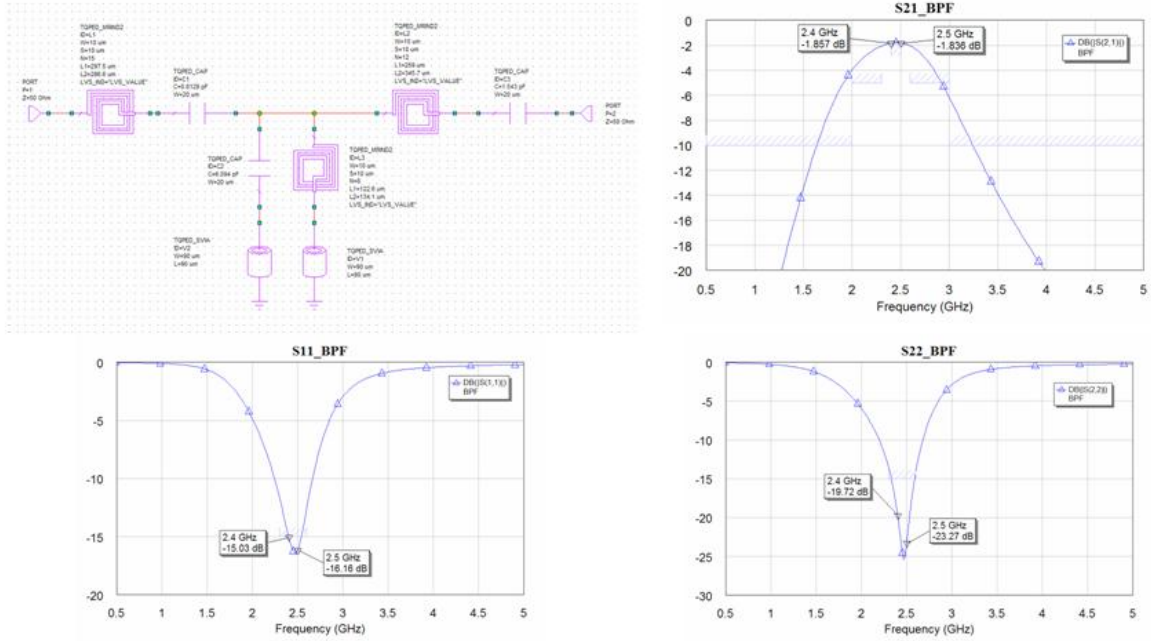


Figure 19

Placing my amplifier and this BPF in series I see the 1.9 dB of loss I expect from the filter and some degradation in the input return loss, but overall the return loss is still good. Plots follow in Figure 20.

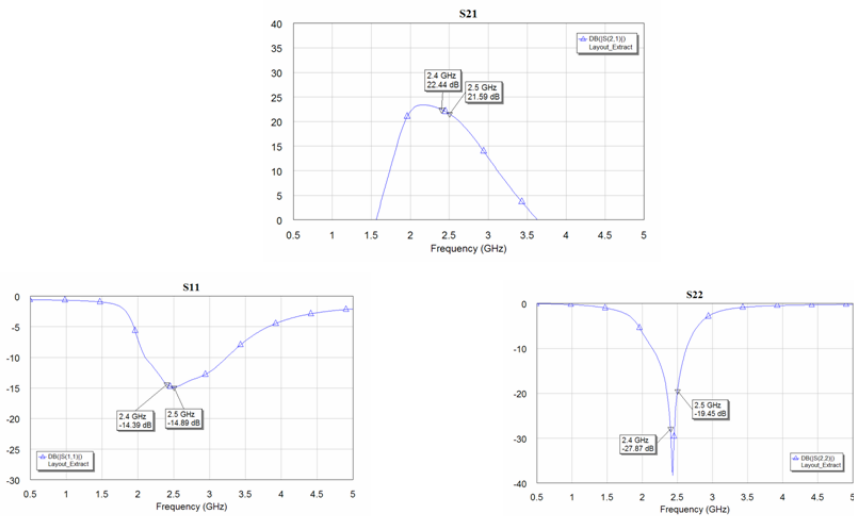


Figure 20

## Layout

Shown below in Figure 21 is the final layout for the post amplifier design. The west side of the MMIC is the input, which will be probed with a 150  $\mu\text{m}$  pitch ground-signal-ground probe. The east side of the MMIC is the output, which also will be probed by a 150  $\mu\text{m}$  pitch ground-signal-ground probe. The north and south side of the chip have the DC probe pads (3V, 3.75 mA each expected) and are designed for a single DC needle. The MMIC size is 60x60 mil.

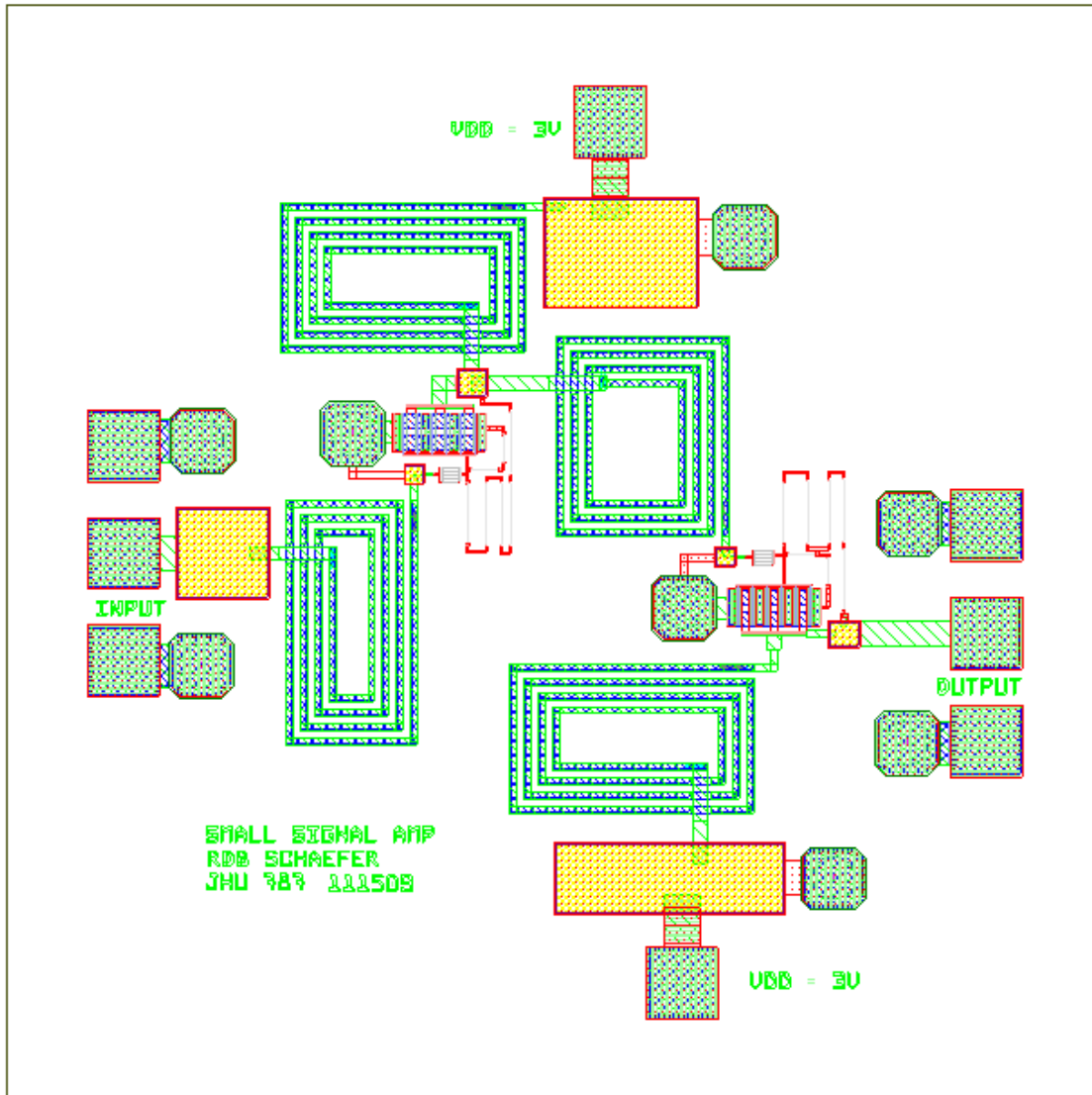
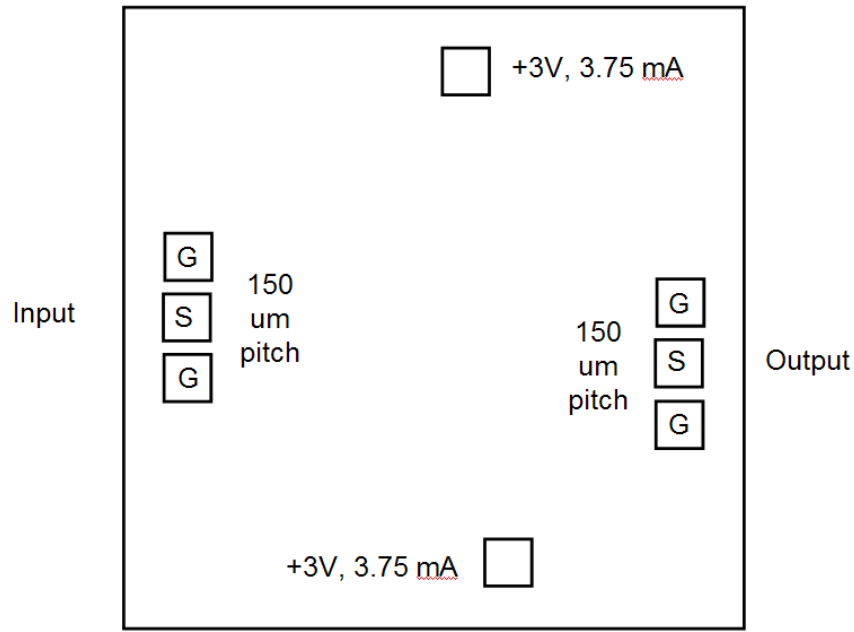


Figure 21

## MMIC I/Os

An outline for the MMIC is presented below in Figure 22. Shown are the input and output Ground-Signal-Ground pads (both are 150  $\mu\text{m}$  pitch) on the west and east sides of the MMIC, as well as the two DC pads (+3V, 3.75mA expected) on the north and south sides of the MMIC.



**Figure 22**

## Test Plan

The test plans included for this amplifier design are for small signal S-parameter testing. Equipment required for this test include a network analyzer and DC supplies. Probes required for this test include 150  $\mu\text{m}$  pitch ground-signal-ground probes on the west and east sides of the chip and single DC needles on the north and south sides of the chip. A step by step process follows:

- 1) Setup probe station with 150  $\mu\text{m}$  pitch ground-signal-ground probes on the west and east sides of the chip and single DC needles on the north and south sides of the chip.
- 2) Calibrate the test setup from 0.1 to 8 GHz using a 0.1 GHz step.
- 3) Place amplifier MMIC in test setup, bring probes down on probe pads, and turn on DC supplies (+3V). Note current draw from DC supplies (should be around 3.8 mA each or 7.6 mA total)
- 4) Take S-parameter data ( $S_{21}$ ,  $S_{12}$ ,  $S_{11}$ , and  $S_{22}$ ) from 0.1 to 8 GHz. Compare this to expected results (from 2.4 to 2.5 GHz:  $S_{21} \rightarrow 23.5$  to  $24.3$  dB;  $S_{11} \rightarrow < -15.5$  dB;  $S_{22} \rightarrow < -16.7$  dB)
- 5) Plot measured ( $s_{2p}$ ) data versus the modeled design for design verification.

## Conclusion

My goal for this project was to design a two-stage post amplifier with ~22 dB of gain, good input and output return loss, low DC power consumption, moderate noise figure, and moderate power efficiency. I wanted the amplifier to be able to be biased by a +3V supply and for the layout to be compact (fit within a 60x60 mil space). This design achieves a gain of 23.5 to 24.3 dB, input return loss better than -15.6 dB, output return loss better than -16.7 dB, a noise figure better than 3.2 dB, a PAE of 45.5% at the P1dB point, and ~23mW of DC power. The amplifier runs off of +3V and the layout fits in the standard 60x60 mil chip outline.

I do pull away from this design a few lessons learned which mostly revolve around considerations I should make earlier in the design process. Among these are the robustness of the design. I would like to have added some tunable biasing structure such that I could change the bias going to the pHEMT ( $V_{gs}$  for example) without changing my supply voltage (+3V). I figure I could have done this with some additional biasing pads with different resistances as part of the voltage divider. Another consideration I would like to have made earlier in the design was the inclusion of the attenuator and/or filter. I tried to design my amplifier efficiently such that I got just enough gain to have some margin, but if I wanted to add the attenuator to help with the match between the LNA and my amplifier, or if I wanted to add a filter to reduce the bandwidth the mixer sees, my gain would fall below the specification. So I could have designed for an additional 2 to 3 dB of gain to begin with which could have compensated for the loss of the attenuator and/or filter if I so desired to use them. An additional lesson learned would be being vigilant while learning to use new design software. I had a couple cases where the auto-routing of the traces shorted out a capacitor, so even though LVS might have caught this, I should have double-checked as I routed.

From my analysis and simulations I would conclude that my modeled design is a success. Of course I will not know if the design is a functional success until the MMIC is tested a few months from now.

# HPA MMIC Design—Final Project

---

## Table of Contents

- Abstract: 24dBm ..... 3
- Design Goals..... 3
- Design Steps..... 5
- Amplifier Topology and Bias Point..... 6
- Power Stage ..... 8
- Driver Stage..... 14
- Intermediate Matching..... 17
- The Complete Power Amplifier..... 17
- Predicted Performance of Two Stage Amplifier ..... 20
- Summary and Conclusions..... 22
- Test Plan..... 23
- Summary and Conclusions..... **Error! Bookmark not defined.**

# Table of Figures

---

Figure 1: IV curve for 6x140 $\mu$ m FET with Driver Stage Dynamic Load Line .....	8
Figure 2: IV Curve for Power Stage .....	9
Figure 3: Power Stage with Bias, and Stabilizing Resistors .....	9
Figure 4: Rds and Cds for the Parallel 6x140 $\mu$ m FETs.....	10
Figure 5: "Rcripps and Cds" with Vdd Bias Inductor Included .....	10
Figure 6: Output Matching Network: A LPF / Transform .....	11
Figure 7: Power Stage with OMN and Gate Stabilization .....	12
Figure 8: Stability Circles and Stability Parameters for Power Stage.....	12
Figure 9: Power Stage Predicted Performance .....	14
Figure 10: Driver Stage with Input Gate Stabilization.....	15
Figure 11: Rds and Cds for the Driver Stage .....	15
Figure 12: Stability Circles and Stability Parameters for the Driver Stage.....	16
Figure 13: Output Power and Gain for the Driver Stage.....	16
Figure 14: Intermediate Matching .....	17
Figure 15: Schematic for Complete Power Amplifier .....	18
Figure 16: Layout for Complete Power Amp.....	19
Figure 17: Predicted Power Out, Gain, Harmonics, and Efficiency.....	21
Figure 18: Stability of Complete Power Amp.....	21
Figure 19: IV Curves for the Two Stages in the Complete Power Amp.....	22
Figure 20: S Parameters .....	22

# Table of Tables

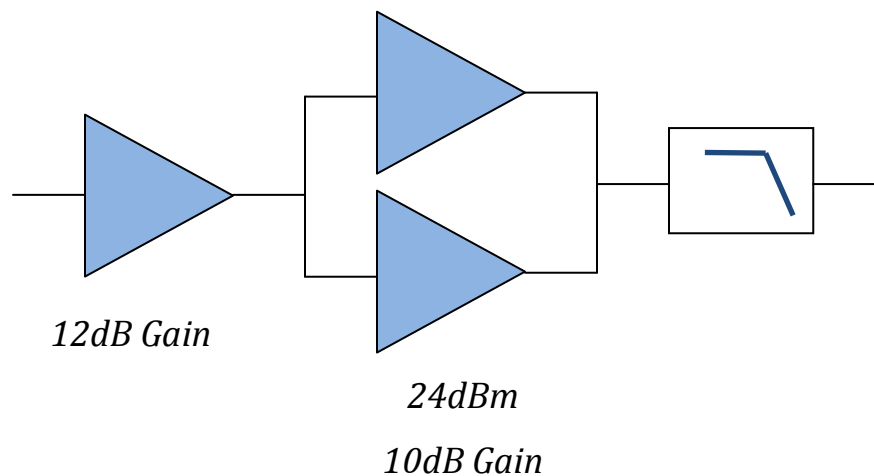
---

Table 1: Power Amplifier Design Goals.....	4
Table 2: Power Budget.....	6

## Abstract: 24dBm

This document describes a 24dBm power amplifier, with 20dB gain, designed for 2.40 to 2.50GHz. It consists of three 6 x 140 $\mu$ m depletion PHEMPTs, each biased at +3V drain voltage and -0.25V gate voltage. Each FET draws about 110mA. The driver stage operates linear. The output stage consists of two FETs connected in parallel. A lowpass filter on the output stage reduces the 2<sup>nd</sup> and 3<sup>rd</sup> Harmonic to less than -30dBc. The bandpass filter impedance was chosen so that it transforms 50 ohms to the desired load line impedance for the HPA stage.

The circuit was designed with Microwave Office software using Triquint MMIC component libraries.



## Design Goals

The design goals for the power amplifier are summarized in Table 1. The -30dBc harmonics requirement was self-imposed.

Operating Frequency	2.40 – 2.50 GHz
Compressed Output Power	24dBm
Small Signal Gain	22dB
Compressed Gain	20dB at 24dBm Output Power
Input Match	15dB
Output Match	10dB
2 <sup>nd</sup> and 3 <sup>rd</sup> Harmonics	-30dBc at 24dBm Output Power
Power Added Efficiency (PAE)	30%
Drain Voltage	+3V
Stability	Unconditionally Stable

**Table 1: Power Amplifier Design Goals**



## Design Steps

1. Determine number of stages and bias point for each amplifier to achieve desired output power and efficiency. (Limited to +3V supply.) Efficiency is maximized by using fewer stages.
2. Design compressed power stage.
  - a. Design DC bias circuit.
  - b. Select output matching network to achieve load line that maximizes output power.
  - c. Include lowpass filter as part of OMN to suppress harmonics.
  - d. Stabilize FET with series and shunt resistors at gate.
3. Design linear driver stage
  - a. Design DC bias circuit.
  - b. Stabilize FET with series and shunt resistors at gate.
  - c. Determine desired load line that maximizes output power.
4. Design intermediate matching network so the input to the power stage presents the ideal load line to the driver stage.
5. Design the input matching network for the driver stage.
6. Verify stability, power out, gain, input match and other requirements of complete power amplifier.

## Amplifier Topology and Bias Point

Efficiency is maximized by using fewer amplifier stages. Linear output power is maximized by only compressing the power stage. Two stages is an obvious choice, since 10dB gain per stage is typical and practical. A simple power budget helps determine the requirements for the two stages. The power stage is assumed to have 10dB power gain at 2dB compression. The driver stage is allotted 12dB gain.

If we want the driver amp to operate 2dB below compression, it will need to have a P1dB of at least  $16.3\text{dBm} + 2\text{dB} = 18.3\text{dBm}$ . If the driver stage consists of two FETs in parallel, each FET must have a minimum output power of  $24.3\text{dBm} - 3\text{dB} = 21.3\text{dBm}$ . Therefore, it is reasonable to use the same FET at the same bias point for both stages, but with the output stage having two FETs in parallel.

Achieving approximately 30% power added efficiency, will limit the drain current to each FET to a little less than 100mA. Efficiency could probably be improved slightly by reducing the drain bias current to the driver amp, but for simplicity, I chose to bias all three FET identically.

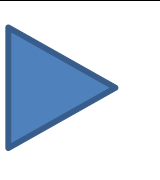
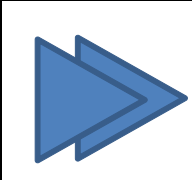

			
	<b>Driver</b>	<b>Power Amp</b>	<b>Low Pass Filter</b>
<b>Gain</b>	12.0 dB	10.0 dB	-0.3 dB
<b>Cum Gain</b>	12.0 dB	22.0 dB	21.7 dB
<b>Compression</b>	0.0 dB	2.0 dB	0.0 dB
<b>Pout</b> 4.3 dBm	16.3 dBm	24.3 dBm	24.0 dBm
<b>Pout</b> 0.0027 W		0.27 W	0.25 W
<b>Ibias</b>	100 mA	200 mA	
<b>Vbias</b>	3.00 V	3.00 V	
<b>Pdc</b>	0.30 W	0.60 W	
<b>Pout</b>	0.25 W		
<b>Pdc</b>	0.90 W		
<b>PAE</b>	27.6%		

Table 2: Power Budget



IV curves for a 6x140μm depletion PHEMPT show that  $V_{gs} = -0.25V$  achieves  $I_{ds}$  of approximately 100mA at  $V_{ds} = 3V$ . This FET (6x140 depletion PHEMPT) and this approximate bias point ( $V_{gs} = -0.25V$ ,  $V_{ds} = 3V$ ,  $I_{ds} = 100mA$ ) are used for all three FETs in the power amplifier.

The dynamic load line at 2.45GHz for the driver stage in the complete power amplifier (when the power stage is at 24dBm) is superimposed on the FET IV curve. The driver stage is operating linearly, as desired.

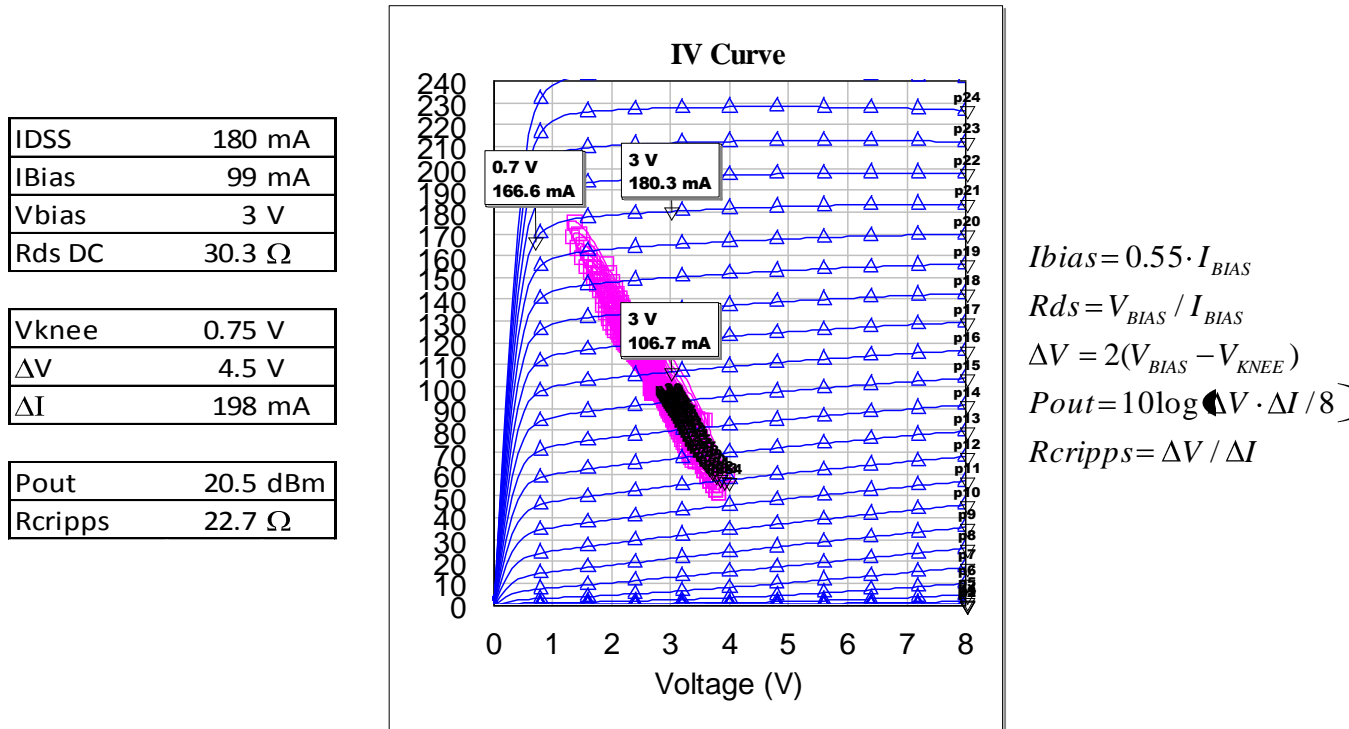


Figure 1: IV curve for 6x140μm FET with Driver Stage Dynamic Load Line

### Power Stage

The IV curve for two 6x140μm FETs in parallel is shown in Figure 2. The DC bias condition for the two parallel FETs is shown in the schematic of Figure 3: Power Stage with Bias, and Stabilizing Resistors. We should expect an output power of about 23.5dBm with this power stage. The FETs should be sized slightly larger, but I decided to stick with the 6x140μm FETs. The load line of the power stage in the complete power amplifier is superimposed on the IV curves of Figure 2. Driven deeper into compression, it does achieve an output power >24dBm

IDSS	360 mA
IBias	198 mA
Vbias	3 V
Rds DC	15.2 Ω

Vknee	0.75 V
$\Delta V$	4.5 V
$\Delta I$	396 mA

Pout	23.5 dBm
Rcripps	11.4 Ω

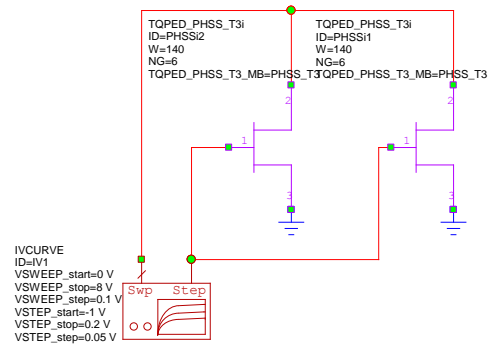
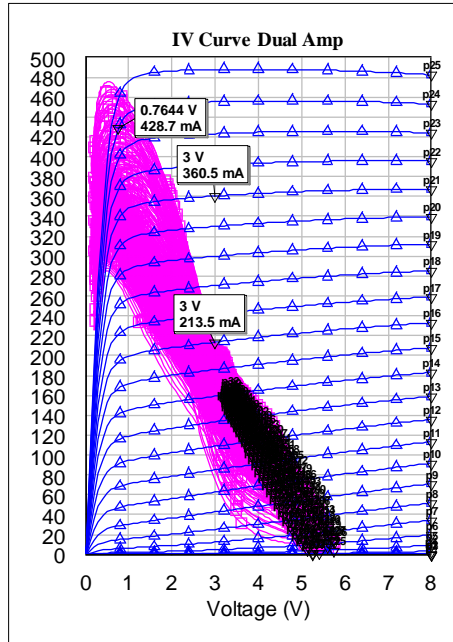


Figure 2: IV Curve for Power Stage

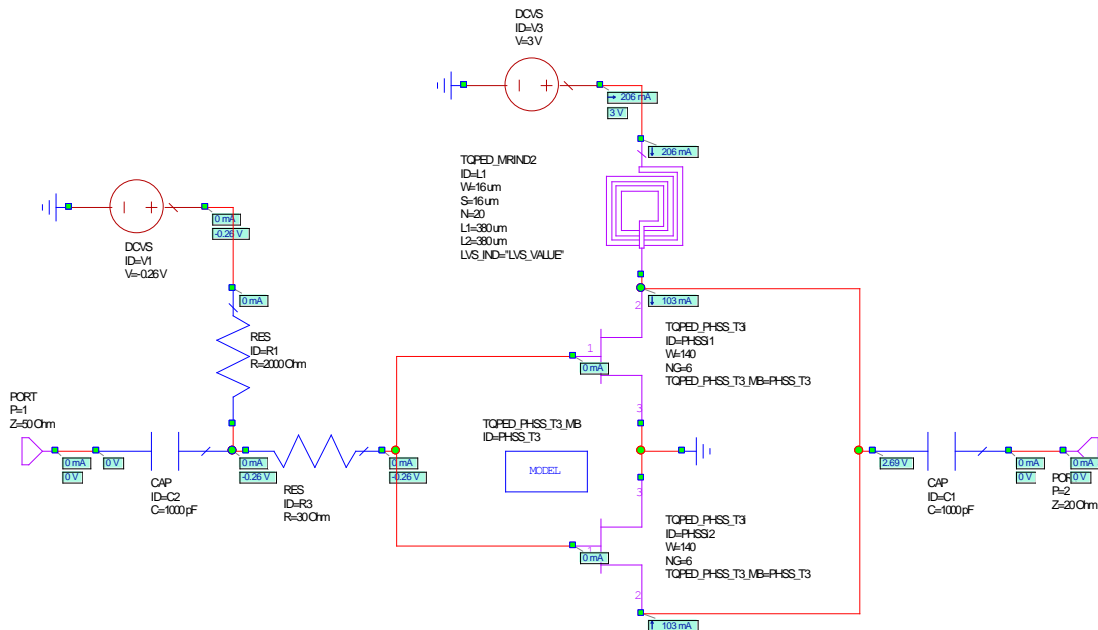


Figure 3: Power Stage with Bias, and Stabilizing Resistors

$R_{ds}$  and  $C_{ds}$  for the two FETs in parallel are approximately  $17.5\Omega$  and  $1.19\text{pF}$  as shown in Figure 4. To maximize output power, with  $V_{ds} = 3\text{V}$ , the power stage wants to see a load of  $R_{cripps} = 15\Omega$ .  $R_{cripps}$  and  $R_{ds}$  for the power stage are approximately equal, so we should expect a decent output match for the power amplifier. The output reactance is partly resonated out by the inductor in the  $V_{dd}$  bias circuit as is shown in Figure 5.

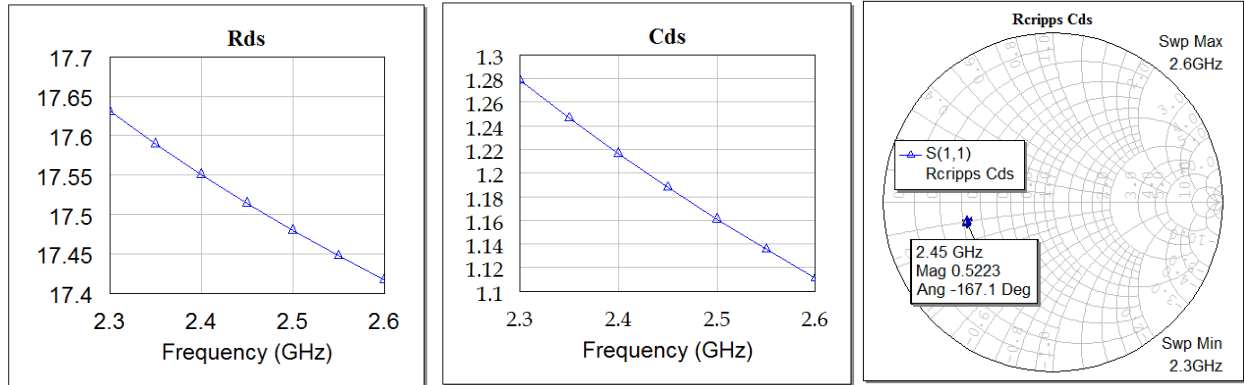


Figure 4: Rds and Cds for the Parallel 6x140µm FETs.

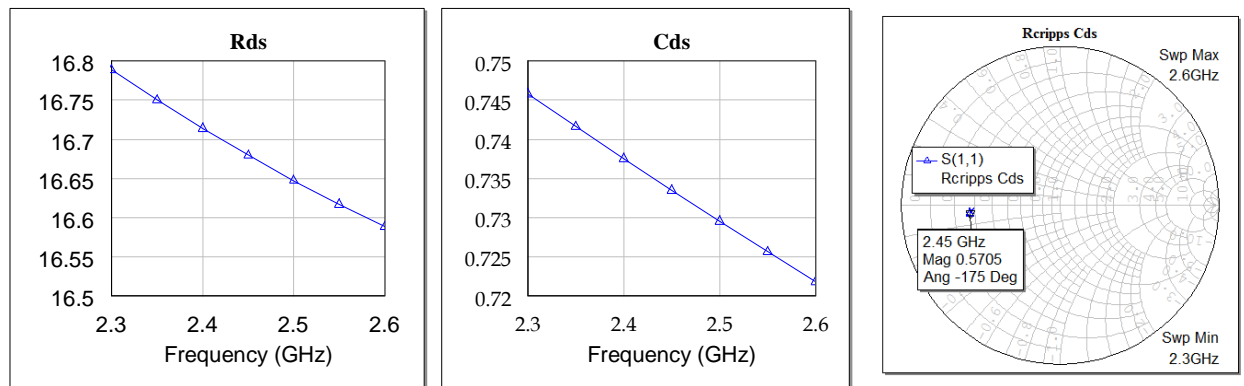
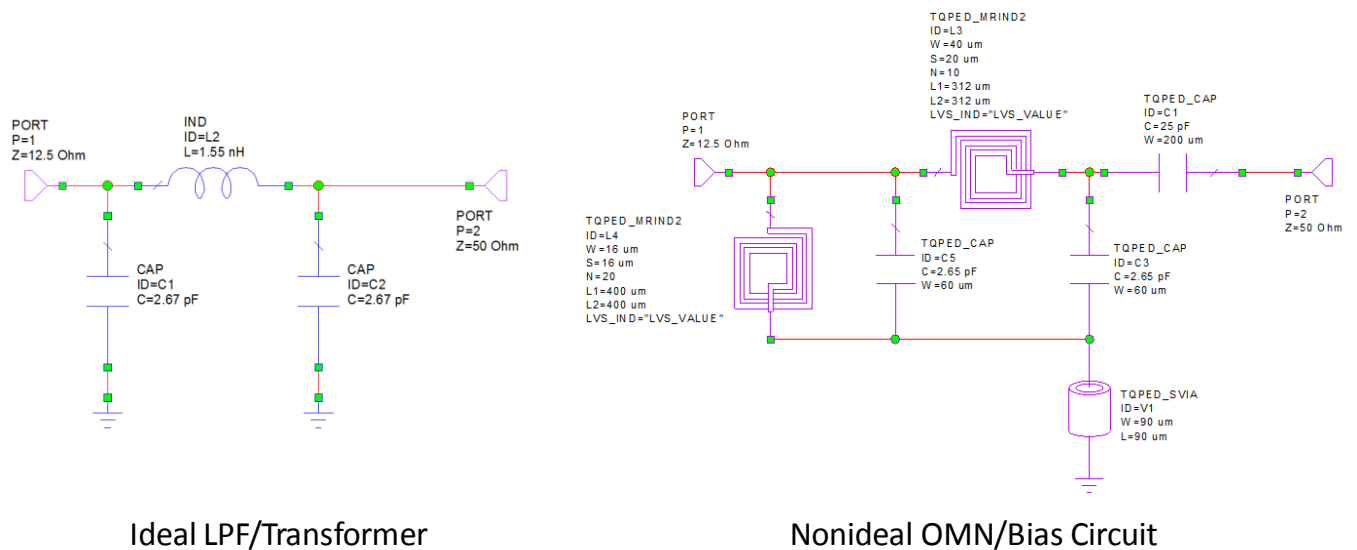


Figure 5: "Rcripps and Cds" with Vdd Bias Inductor Included

The power stage output matching network is a (maximally flat) lowpass filter whose impedance was selected to transform the  $50\Omega$  port to the desired load line. But, the lumped element low-pass filter is not simply a transmission line equivalent. For a lowpass T configuration transmission line equivalent, the inductors and capacitors have the same impedance  $g_1=g_2=g_3=1.0$ . For the lowpass filter, the inductors and capacitors have different impedances;  $g_2=2.0$  for the inductors and  $g_1=g_3=1.0$  for the capacitors.

Figure 12 shows the low pass filter / transformer with ideal lumped elements and the output matching network / bias circuit with Triquint MMIC elements. Performance is shown with the circuits driven by a  $12.5\Omega$  source. The output matching network / bias network has in-band return loss of approximately 20dB, in-band insertion loss of approximately 0.4dB, 10.3dB attenuation of the 2<sup>nd</sup> harmonic, and 18.6dB attenuation of the 3<sup>rd</sup> harmonic. Since  $R_{ds} = 17\Omega$ , not  $12\Omega$ , the OMN / Bias network should have been optimized for a  $17\Omega$  source. This is why the power stage has a 10dB match, instead of a 20dB match.



Ideal LPF/Transformer

Nonideal OMN/Bias Circuit

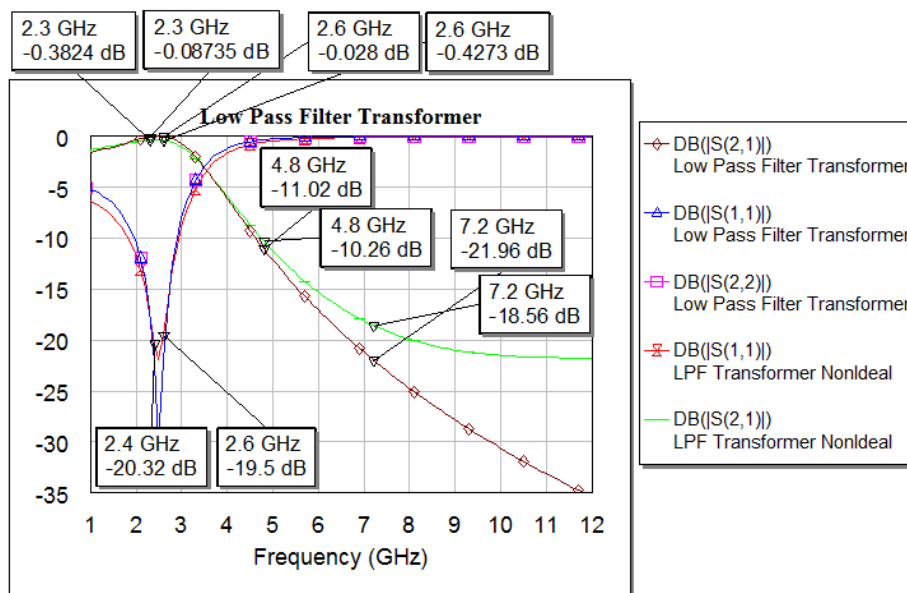


Figure 6: Output Matching Network: A LPF / Transform

The input matching network and gate stabilization resistors for the power stage are shown in Figure 7. Stability circles and mu stability parameters for the power stage are shown in Figure 8. Above 4.8 GHz, the input stability parameter is almost exactly 1, since the LPF is highly reflective outside the passband.

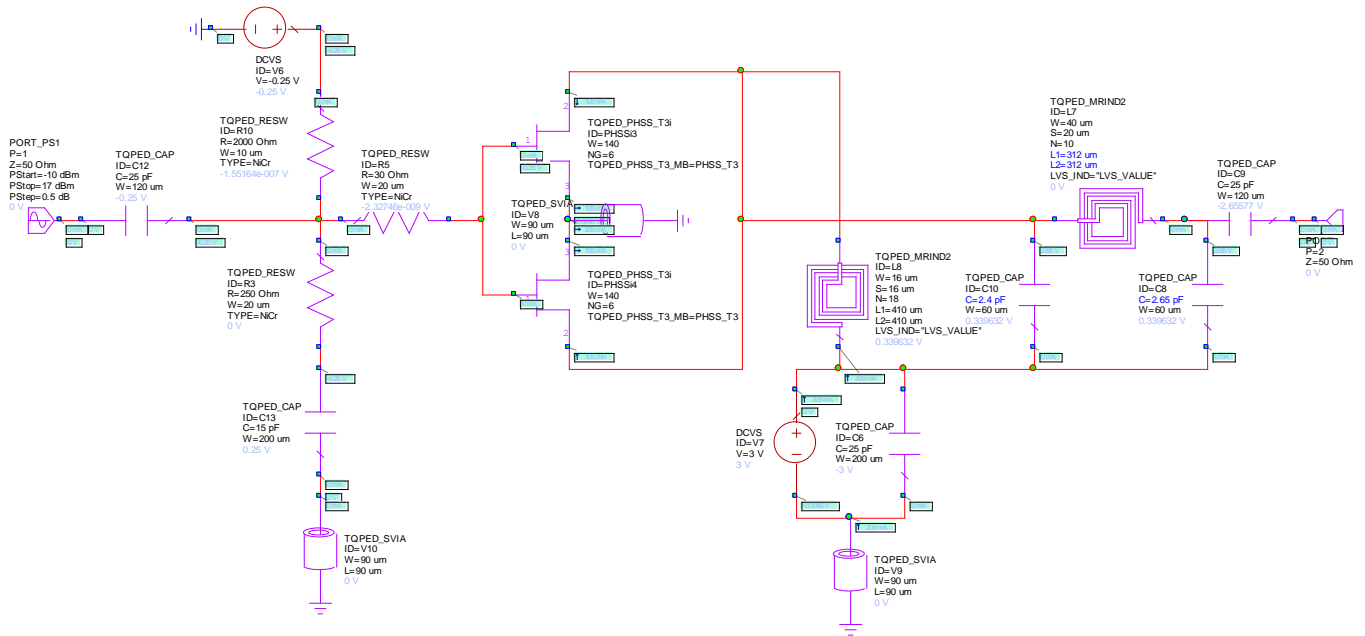


Figure 7: Power Stage with OMN and Gate Stabilization

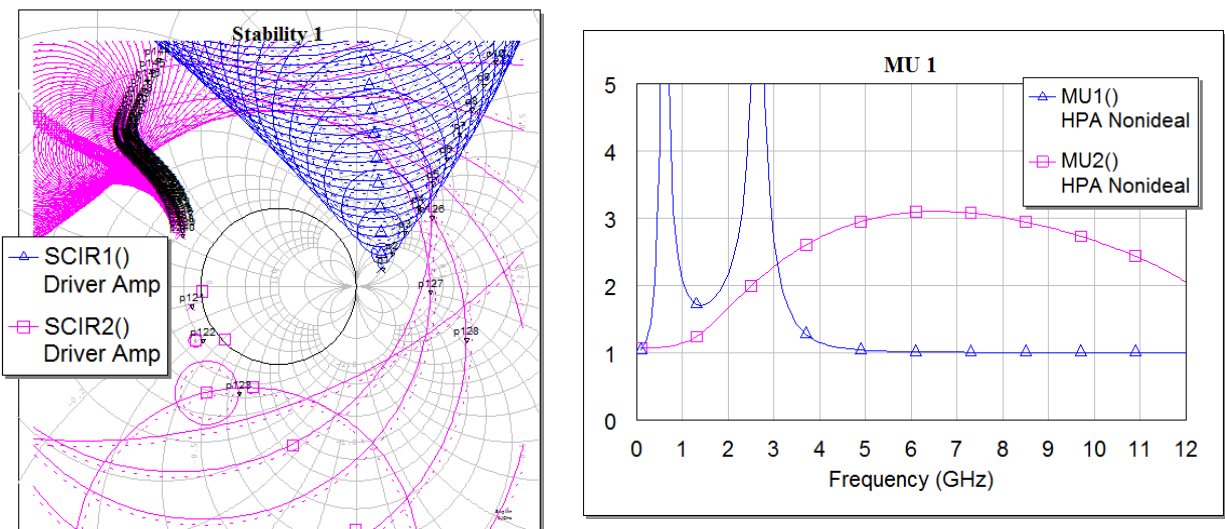
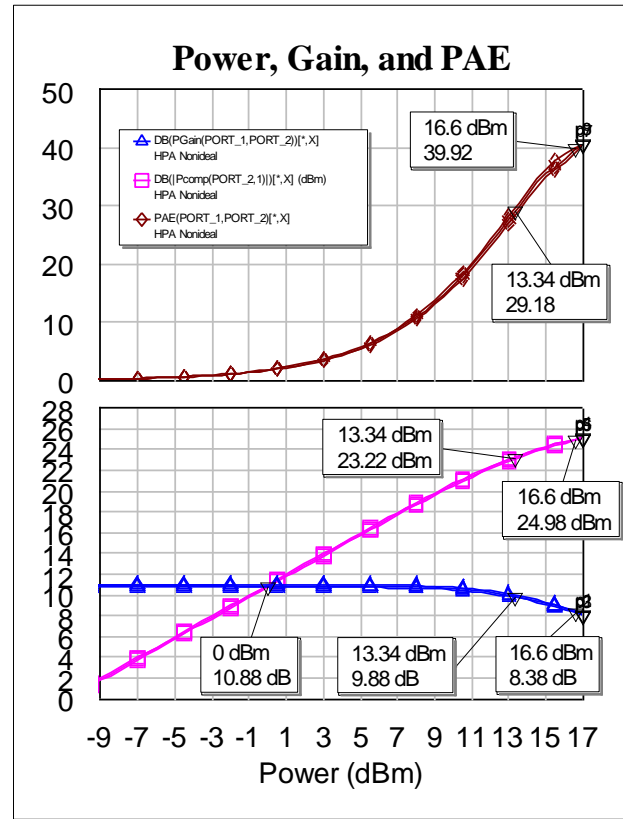
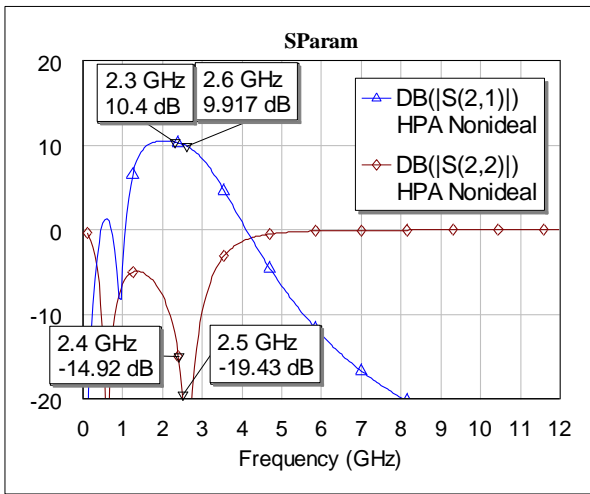


Figure 8: Stability Circles and Stability Parameters for Power Stage



The predicted output power of the power stage is approximately 25dBm and 8.4dB gain at 2.5dB compression, as shown in Figure 9. Power added efficiency approaches 40%. The 2<sup>nd</sup> and 3<sup>rd</sup> harmonics are -30dBc and -45dBc.



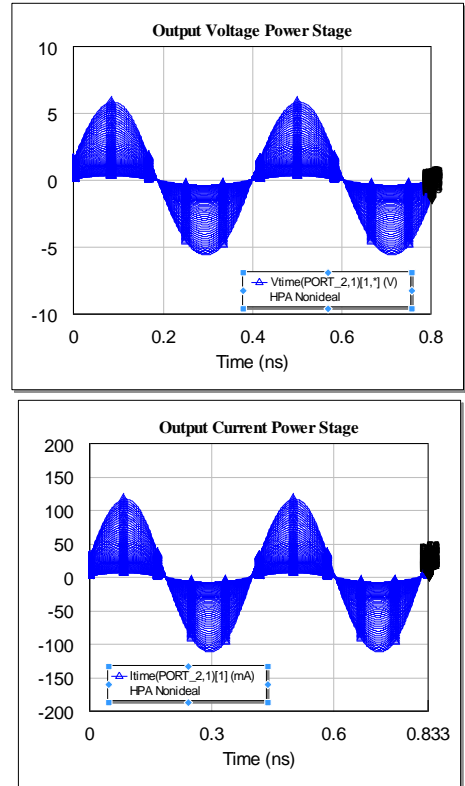
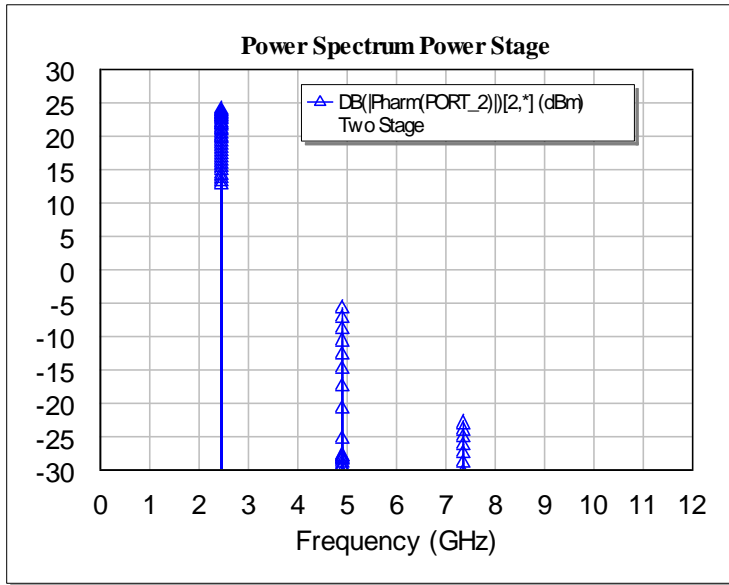


Figure 9: Power Stage Predicted Performance

## Driver Stage

The driver FET with gate stabilizing resistors is shown in Figure 10. The FET is unconditionally stable from 0.1 to 12 GHz. It outputs about 16dBm power with about 12dB of gain when it is 0.5dB compressed. So, it is adequate to drive the power stage.

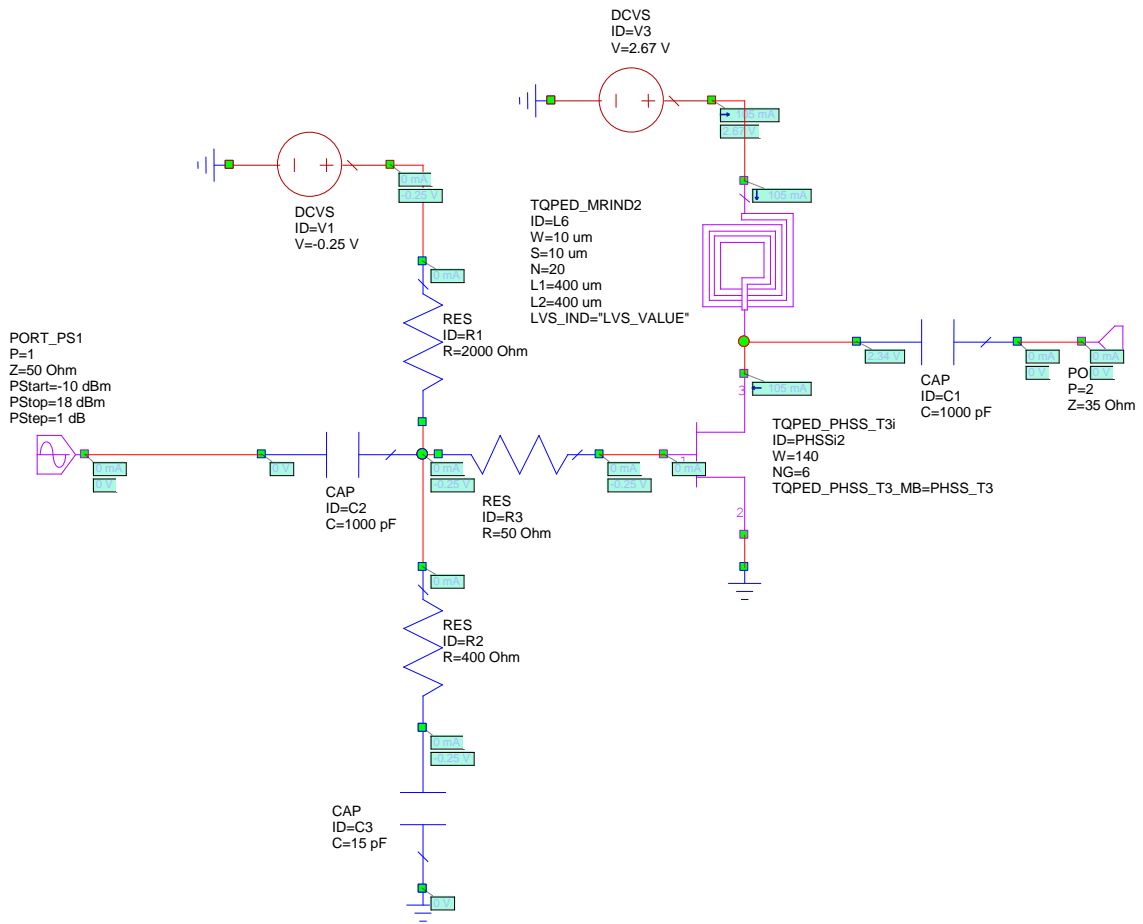


Figure 10: Driver Stage with Input Gate Stabilization

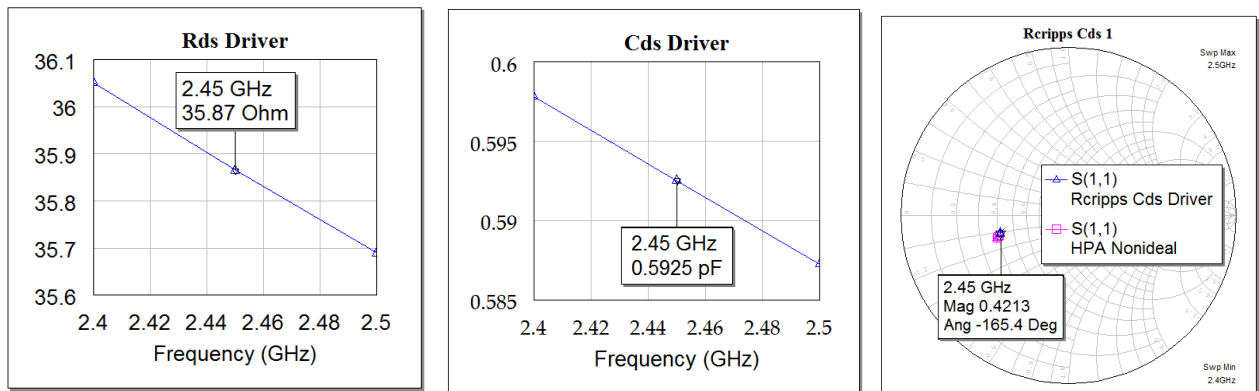


Figure 11: Rds and Cds for the Driver Stage

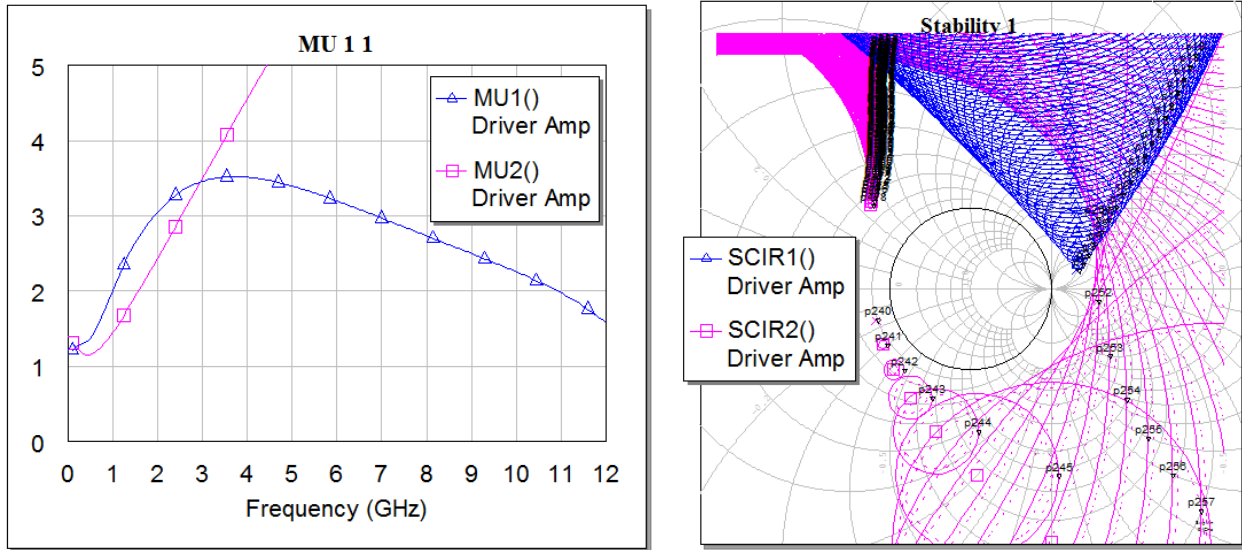


Figure 12: Stability Circles and Stability Parameters for the Driver Stage

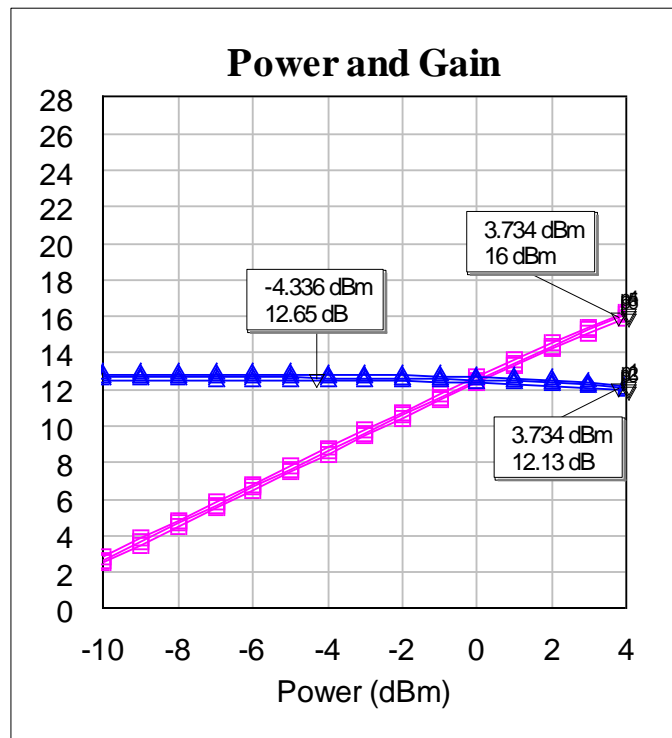


Figure 13: Output Power and Gain for the Driver Stage

## Intermediate Matching

The intermediate matching circuit makes the input of the driver stage look like the ideal load line for the driver stage.

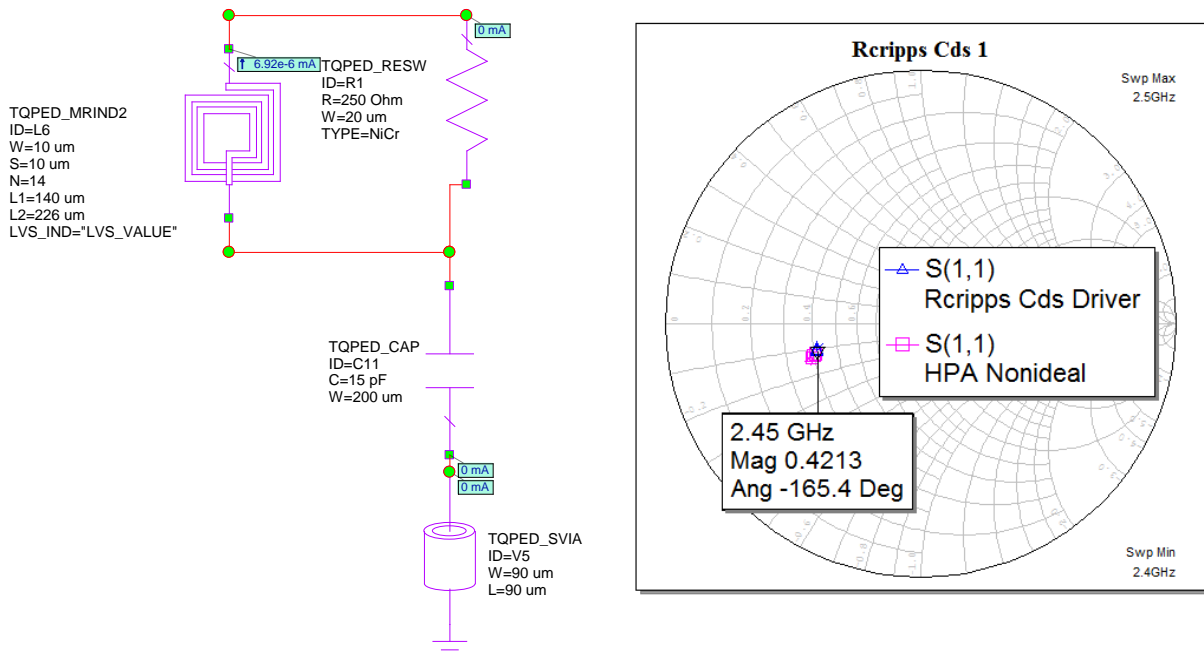


Figure 14: Intermediate Matching

## The Complete Power Amplifier

The schematic and layout for the complete two stage power amplifier are shown in Figures 15 and 16. Somehow I forgot a filtering capacitor on the V<sub>gg</sub> input. (Originally, I had one, but it was accidentally discarded during the layout process.) The inductor in the OMN / LPF consists of 40 $\mu$ m wide conductors to minimize loss.

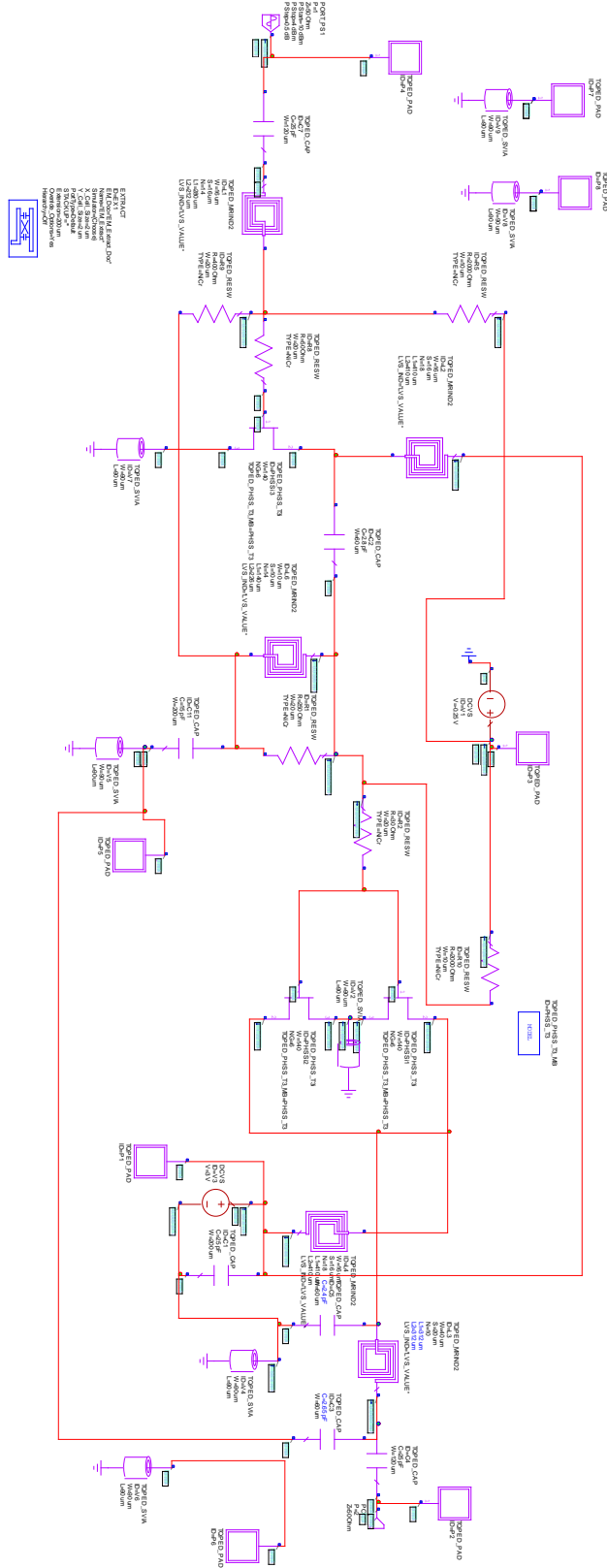


Figure 15: Schematic for Complete Power Amplifier

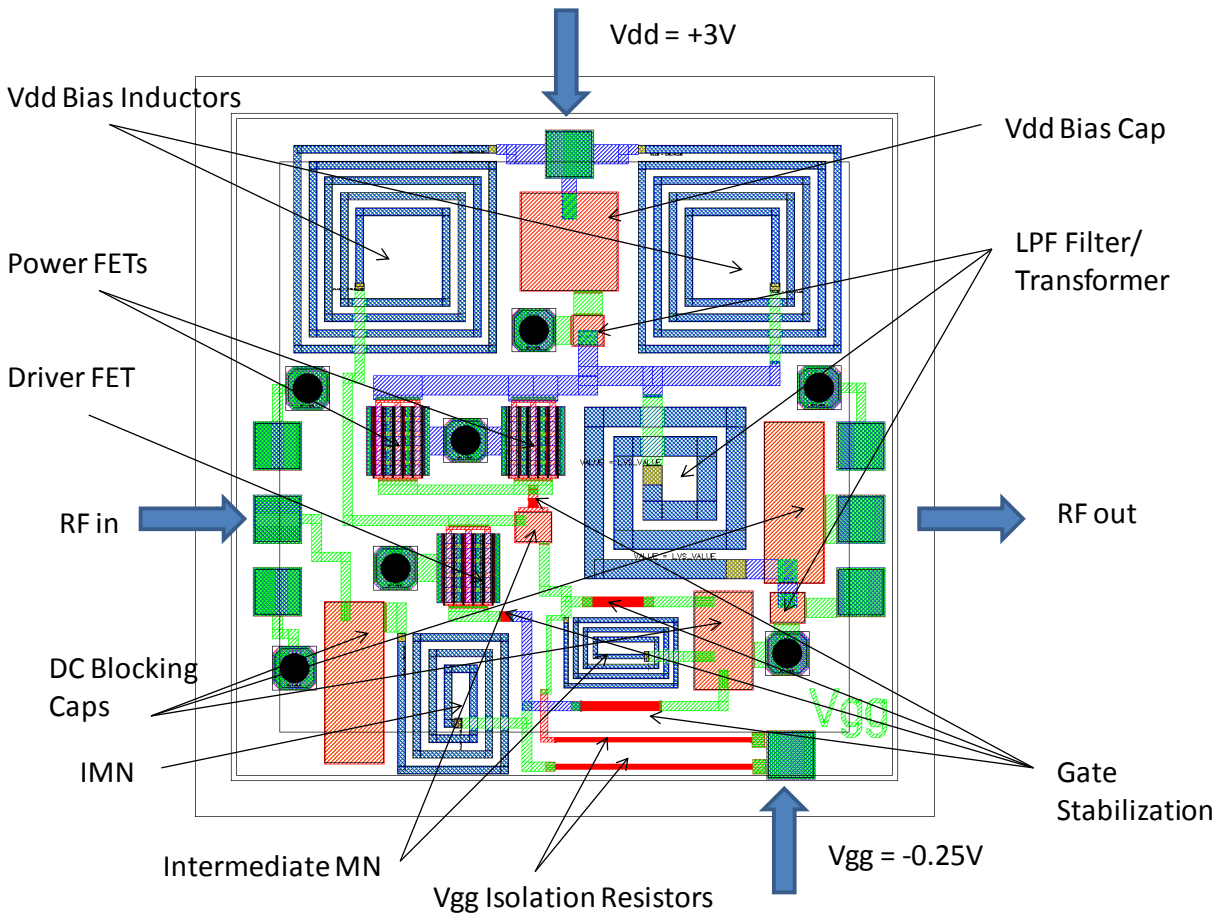


Figure 16: Layout for Complete Power Amp

## Predicted Performance of Two Stage Amplifier

Simulations predicted 25dBm output power with 20.4dB gain at 2.5dB compression. The 2<sup>nd</sup> and 3<sup>rd</sup> harmonics are approximately -30dBc and -45dBc. The amplifier is unconditionally stable.

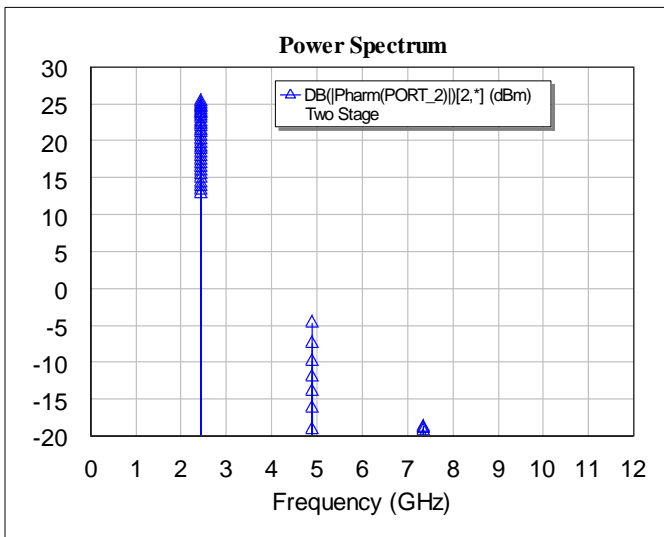
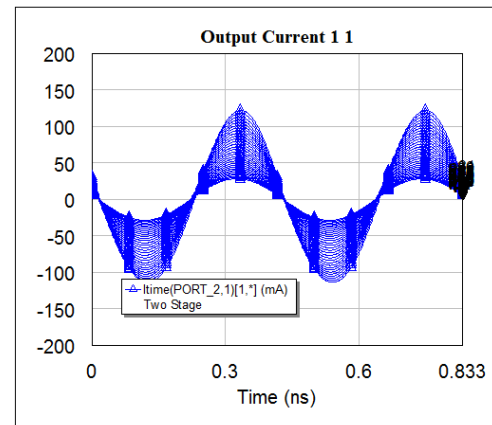
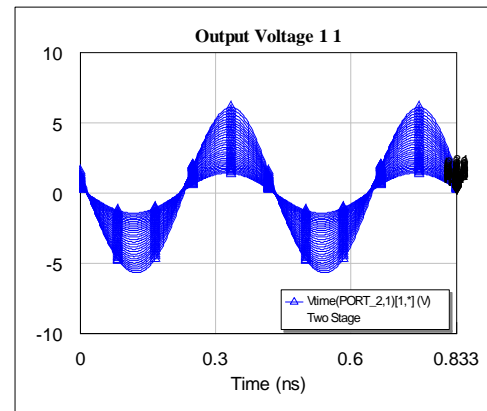
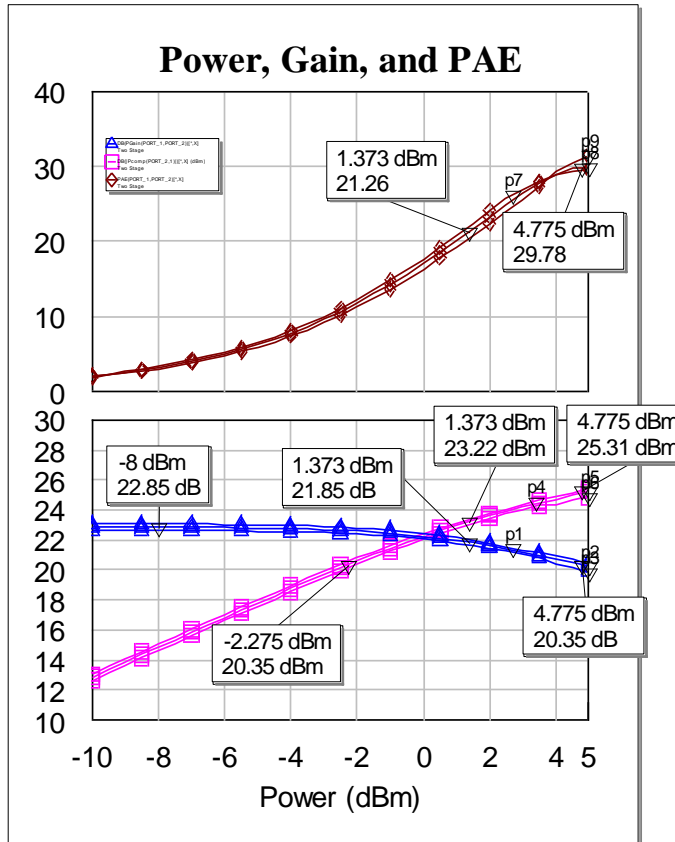




Figure 17: Predicted Power Out, Gain, Harmonics, and Efficiency

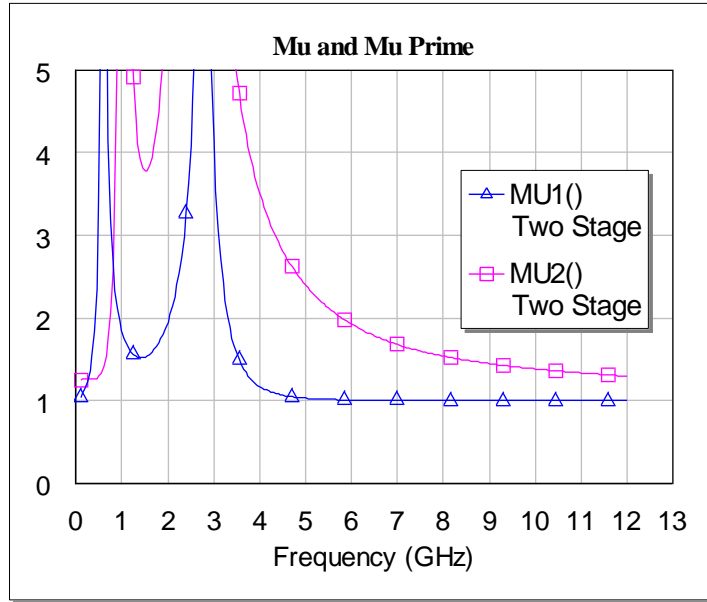


Figure 18: Stability of Complete Power Amp

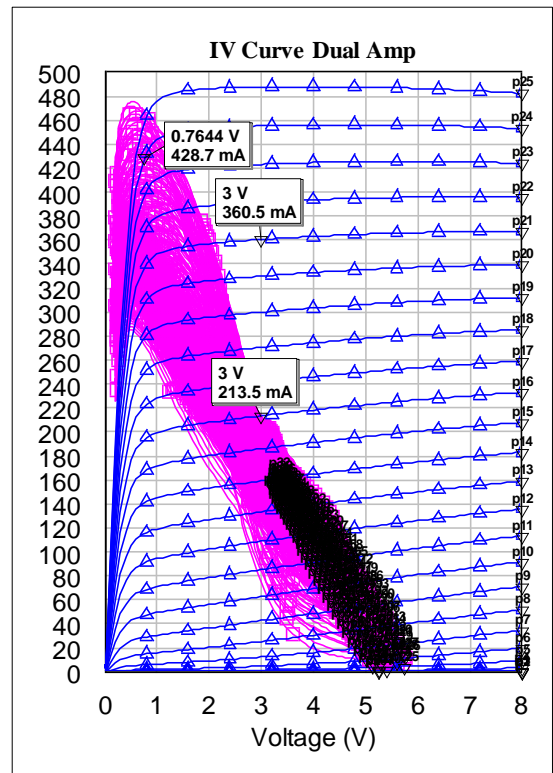
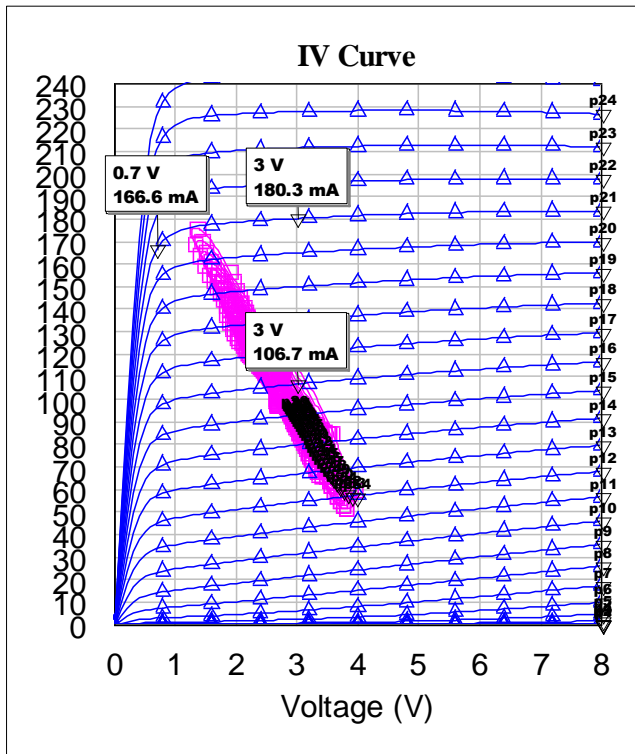


Figure 19: IV Curves for the Two Stages in the Complete Power Amp

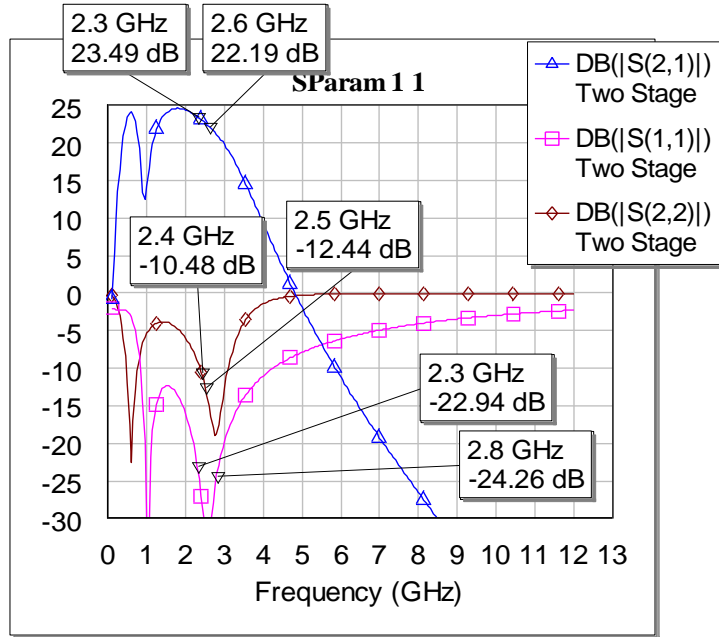


Figure 20: S Parameters

## Summary and Conclusions

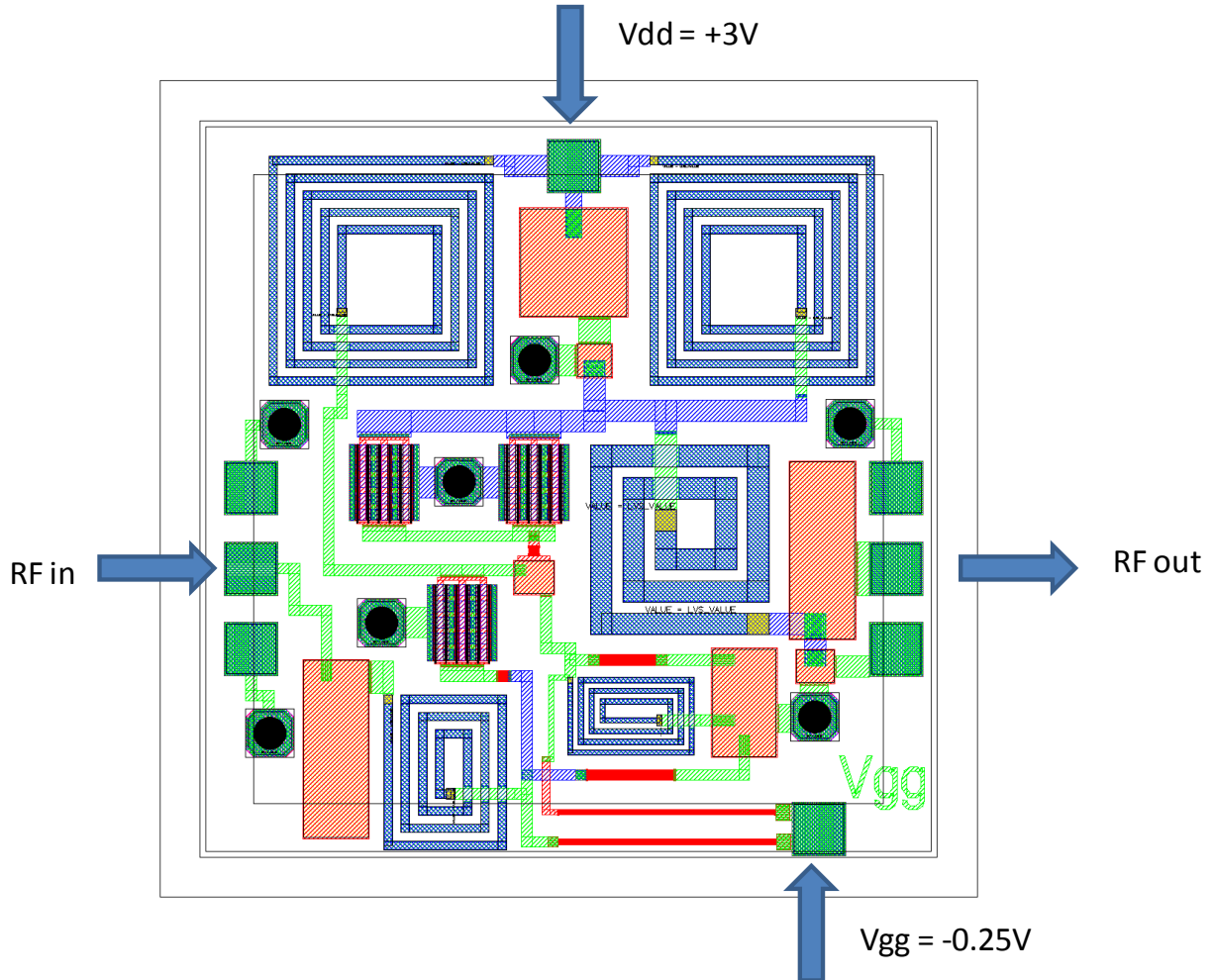
Simulations predict the power amplifier will meet its performance requires, except efficiency. It has about 29% PAE. If time permitted, I would redesign the amplifier with a little more margin, run tolerance studies and plot load pull contours.

Also, somehow the Vdd filter capacitor was omitted from the schematic and the layout, and a redesign would fix this omission.

	Requirement	Simulation
Operating Frequency	2.40 – 2.50 GHz	2.40 – 2.50 GHz
Compressed Output Power	22dBm	24.8dBm
Small Signal Gain	22dB	22.8dB
Compressed Gain	20dB at 24dBm Output Power	20.8dB
Input Match	15dB	22dB
Output Match	10dB	10.5dB
2 <sup>nd</sup> and 3 <sup>rd</sup> Harmonics	-30dBc at 24dBm Output Power	-30dBc 2 <sup>nd</sup> , -45dBc 3rd
Power Added Efficiency (PAE)	30%	29% at 24.8dBm
Drain Voltage	+3V	+3V
Stability	Unconditionally Stable	Unconditionally stable

## Test Plan

1. Connect  $50\Omega$  load to RF output port.
2. Connect  $-0.25\text{V}$  to  $V_{gg}$ .
3. Connect  $+3\text{V}$  to  $V_{dd}$ .
4. Connect  $-20\text{dBm}$  at  $2.45\text{ GHz}$  to RF input port. Measure gain, input match, and output match. Observe stability.
5. Increase RF input power to  $-10\text{dBm}$ . Measure gain and observe stability.
6. Increase RF input power to  $+6\text{dBm}$  in  $1\text{dB}$  increments. Measure output power. Calculate gain. Stop when the amplifier is  $3\text{dB}$  compressed.



**2.4 GHz LNA Project**  
**525.787 MMIC Design**

**Clay Couey**

## Abstract

This paper describes the design and simulated results of a low noise amplifier (LNA). The LNA is to operate at 2.4 GHz and will be fabricated on Triquint's TQPED pHEMT (pseudomorphic high electron mobility transistor) process. The main design goal was to design the amplifier to have a noise figure as close as possible to the optimum noise figure,  $NF_{opt}$ , given from the scattering parameters (S-Parameters) for the process from Triquint. The design utilized inductive source degeneration in order to allow simultaneous optimization of noise figure and input return loss. The design has 10 dB of gain with a NF of  $< 0.9$  dB with excellent match on input and output ( $S_{11}$  and  $S_{22}$  are approximately -20 dB). Input P-1 dB compression is approximately -4 dBm.

## Introduction

The design was targeted to be the first stage of gain in a receive chain, biased with a single (positive) power supply that would enable battery operation. Bias was chosen as +3V with current draw of 15 mA. Triquint's TQPED process allows enhancement mode and depletion mode pHEMTs, the design requirement of a single power supply is more easily met with an enhancement mode pHEMT. It was also convenient that  $NF_{opt}$  for the enhancement mode at 2.4 GHz occurred at a source impedance nearer to 50 ohms than for the depletion mode. A common-source, enhancement-mode pHEMT was therefore the chosen topology.

A gain of approximately 10 dB was chosen for two reasons. In order to properly "set" the noise figure of the chain, at least 10 dB of gain from a first-stage LNA is desired. But if this is to be the first stage of a two-stage LNA (total gain likely  $\sim 20$  dB), it is desirable for the gain of the first stage to be only moderately high in order to prevent the first stage from becoming the dynamic range limiting element – allowing the second stage to also be approximately 10 dB but with higher bias and compression point. The gain of the process is much higher than 10 dB at the design frequency of 2.4 GHz, so feedback was employed to reduce the gain. Resistive feedback would raise the noise figure, so reactive feedback, in the form of an inductor from source to ground, was employed.

The  $NF_{opt}$  of the process at a bias similar to the designed LNA was approximately 0.5 dB; the goal, therefore, was to degrade this as little as possible, with an expectation that a final NF of  $< 1.0$  dB would be attainable. In order to minimize noise figure degradation, efforts were made to minimize the need for components on the input side of the amplifier. All stabilization was done on the output of the LNA, and the input matching topology was chosen to allow the matching inductor to be the path for the gate bias. Ultimately, the finite quality factor (Q) of the input matching inductor was the single largest contributor to noise figure, with the source-to-ground feedback inductor being the only other contributor of significance.

## Design Approach

The design of the LNA began with the noise parameters included in the S-Parameter file for the TQPED process. The IDSS/4 file was biased at +3.0V/19mA, a similar bias to the design.

RAW	NOISE	DATA		
Freq	FMIN	GAMMA	OPT	Rn
GHz	dB	Mag	Ang	(NORMALIZED)
1	0.42	0.609	6.676	0.155
2	0.43	0.5298	28.683	0.129
*2.4	0.482	0.50572	35.3646	0.1278
3	0.56	0.4696	45.387	0.126
4	0.66	0.4258	60.019	0.125

\* 2.4 GHz row is interpolated

The table above set the design goal of the NF – specifically, to degrade this 0.48 dB number as little as possible. A realistic spec is that the noise figure will be < 1.0 dB once non-idealities are introduced, with a goal of < 0.8 dB.

The output match on an LNA should be excellent, as there is no NF penalty for matching into any arbitrary load and optimizing the output match simultaneously gives the maximum gain for a given input match. Correspondingly, a specification of a return loss of at least 15 dB is set, with a goal of 20 dB.

The input match on an LNA, however, does come with a tradeoff. Highest gain occurs when the input impedance of the amplifier matches the characteristic impedance of the system (typically 50 ohms), so the ideal input impedance for highest gain would be  $50+j0$  and the input matching network would be designed accordingly and would be from the perspective “looking into” the amplifier (S11). However, this matching network transforms the driving source impedance (assumed to be  $50 + j0$ ) into a load presented to the input of the transistor, and it is this input loading which determines the noise figure of the amplifier. It is only when the input matching network presents 50 ohms as the  $Z_{opt}$  for the transistor that  $NF_{opt}$  is attained.

It would be simply fortuitous if the matching network which optimizes S11 simultaneously presented a source impedance of 50 ohms to be the ideal source impedance for optimal noise figure. To an extent, there can be significant forgiveness for an imperfect S11; gain can always be increased with additional stages later, and passband ripple due to input reflections may not be an issue, especially in narrowband systems. A spec of  $S11 < -10$  dB is viewed as acceptable, and there is little effect on the overall gain at this point. However, with the use of source degeneration feedback, a goal of  $S11 < -15$  dB is pursued, again bounded by the governing goal of minimization of noise figure degradation.

Similarly, the stability of the transistor is a parameter which does come with a tradeoff, although the significance of the tradeoff ultimately depends on the design. If, for example, resistive stabilization was required on the input that could not be bypassed at the operational frequency, the noise figure will be strongly impacted by the need to stabilize the device. If, however, the

stabilization can occur at the output, only the gain and output intercept points are affected and, assuming there is still decent overall gain even with the stabilization resistor, the effect on the noise figure is small. This was the design goal for this LNA – that all stabilization occurs on the output.

The power supply requirement is single supply, +3V operation. It is likely that the design, if battery powered, might be exposed to +2.7V to +3.6V, so the design would ideally work well across this battery range. With a simple passive biasing scheme, the device current will vary with the power supply, but the overall specifications – especially gain and noise figure, should not vary significantly.

Input power compression is a specification driven by the gain of the device and the DC power budget. With approximately 45 mW of DC power consumption, even a 10% drain efficiency would produce an output power of 4.5 mW (+6.5 dBm). Referred to the input, with a gain of approximately 10 dB, an input P-1 dB of -3.5 dBm should be achievable, unless there is significant loss due to resistive stabilization (or unless the gain is actually higher than 10 dB).

The design should work from 2.3 to 2.5 GHz, and there is little tradeoff required to meet this specification. The matching networks are wideband enough to provide nearly identical performance across the entire band.

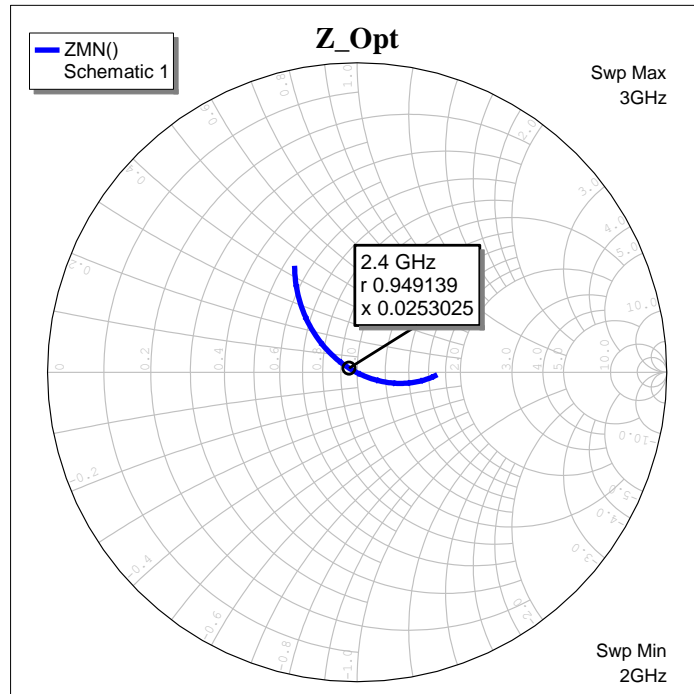
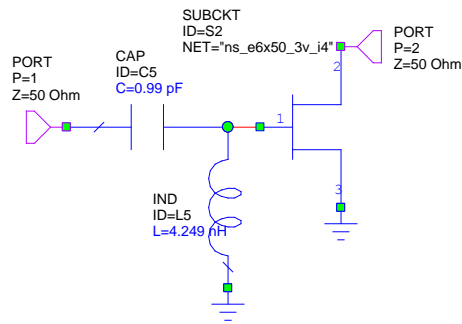
The sizing of the pHEMT would normally be a parameter available to the designer, but in this case, the 6x50 um device was chosen to match the device for which noise parameter data was given. This device size seemed to be well matched for the application and was not viewed as a significant tradeoff.

Given the analysis above, the following table reflects the specifications and goals of the design.

<b>Parameter</b>	<b>Specification</b>	<b>Goal</b>
Operating Frequency	2.3 to 2.5 GHz	2.3 to 2.5 GHz, same specs
Gain, S21	10 dB < Gain < 12 dB	Same
Gain Variation (Ripple)	< 1.0 dB	< 0.5 dB
NF	NF < 1.0 dB	NF < 0.8 dB
S11	< -10 dB	< -15 dB
S22	< -15 dB	< -20 dB
Power Supply Requirements	Single Supply, +3.0V	+3.0V to +3.6V operation
Power consumption	< 50 mW	Same
Input P-1 dB	-3.5 dBm	Same
Output P-1 dB	+6.5 dBm	Same
Stability	“Stable” – no obvious issues, especially near operating frequency	Unconditionally Stable, entire frequency range

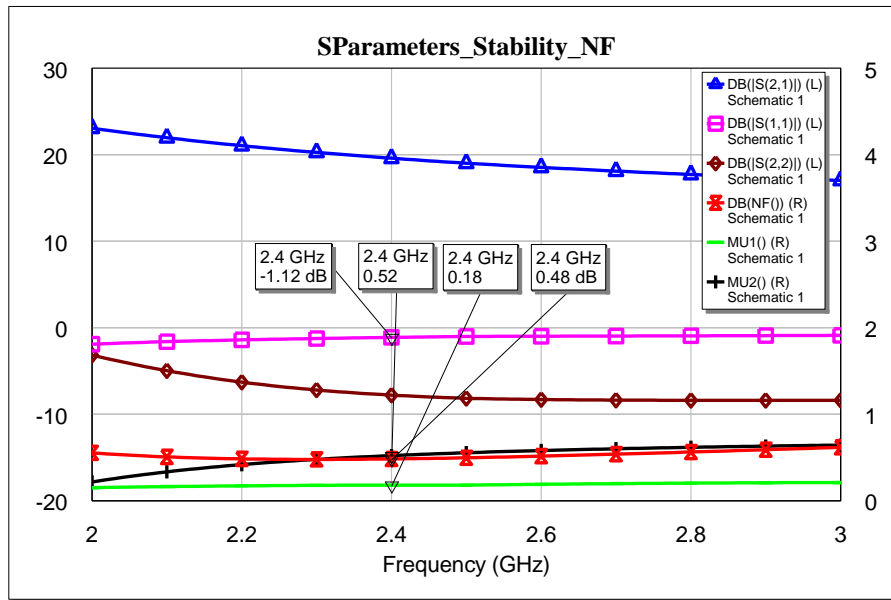
Because the stabilization of the device and the input match are the two specifications that do potentially come with a tradeoff, a quick analysis of these aspects of the design are included in more detail – specifically, how the source inductor helps the design.

Below is a simple two-element matching network which provides  $Z_{opt}$ , the source impedance which provides minimum noise figure. There are two such networks, but the one used is the highpass topology because it allows feeding in the bias through the shunt inductor. The simulated noise figure is 0.48 dB, which matches the  $NF_{opt}$  attained from the S-Parameter file, and is demonstrated with the plot of  $Z_{opt}$  showing that with the input matching network, optimal noise figure is achieved with a source impedance of 50 ohms.

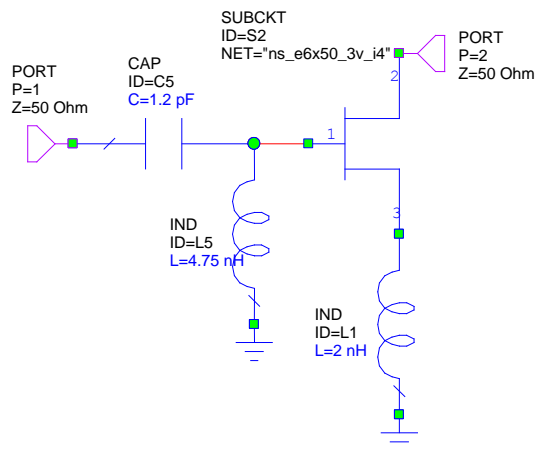


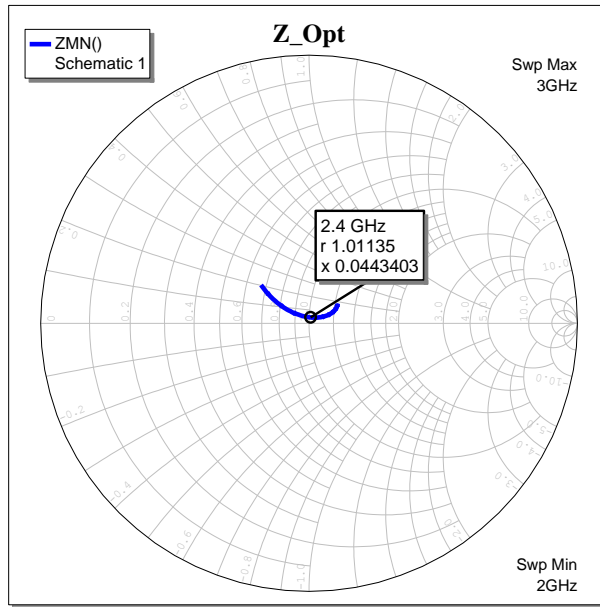


While noise figure is a priority, this input matching network is not a good starting point for the design. As shown in the following plot, the design is highly unstable, with MU1 and MU2 much less than 1.0, and S11 is an atrocious -1.1 dB. Even if the output could be stabilized with resistors, the input return loss will still be poor.



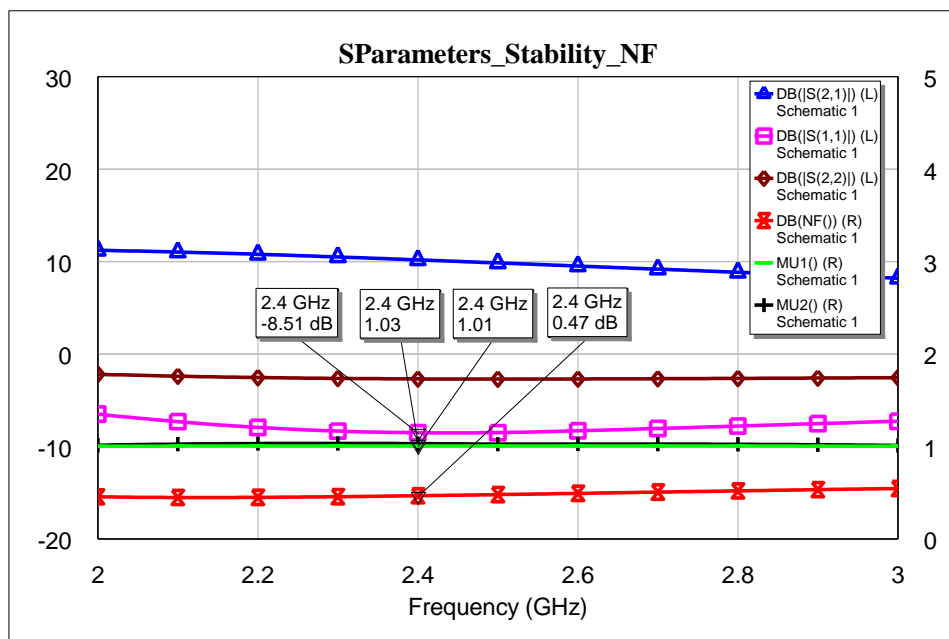
However, the addition of an (ideal) inductor from source to ground significantly improves the stability and input return loss of the amplifier without degradation to the noise figure. Below is the schematic with the addition of the source inductor. Note that the source inductor does slightly affect  $Z_{opt}$ , so the component values in the input matching network have been adjusted to re-center  $Z_{opt}$  at 50 ohms.





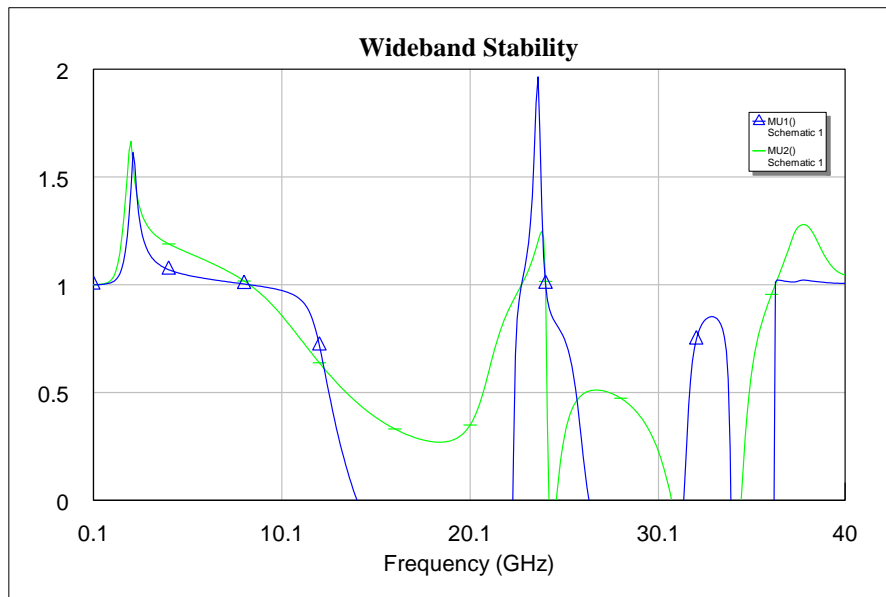
The 2 nH inductor has a significant effect on the overall design of the amplifier. MU1 and MU2 are now above 1.0 and the input return loss is greatly improved, with an S11 of -8.5 dB. As expected from the Zopt plot above, the noise figure remained at NF<sub>opt</sub> of ~ 0.48 dB. Note that the gain is significantly reduced, which would be expected from feedback, but it is likely that a total LNA gain of 20+ dB would have required two stages of gain so lower gain is not only acceptable but desirable.

This demonstrates the value of the source inductor as a starting point for the design. Since the (ideal) inductive feedback has no resistance, there is no degradation in the noise figure and it relocates Z<sub>opt</sub> to an S11-friendly portion of the Smith chart.

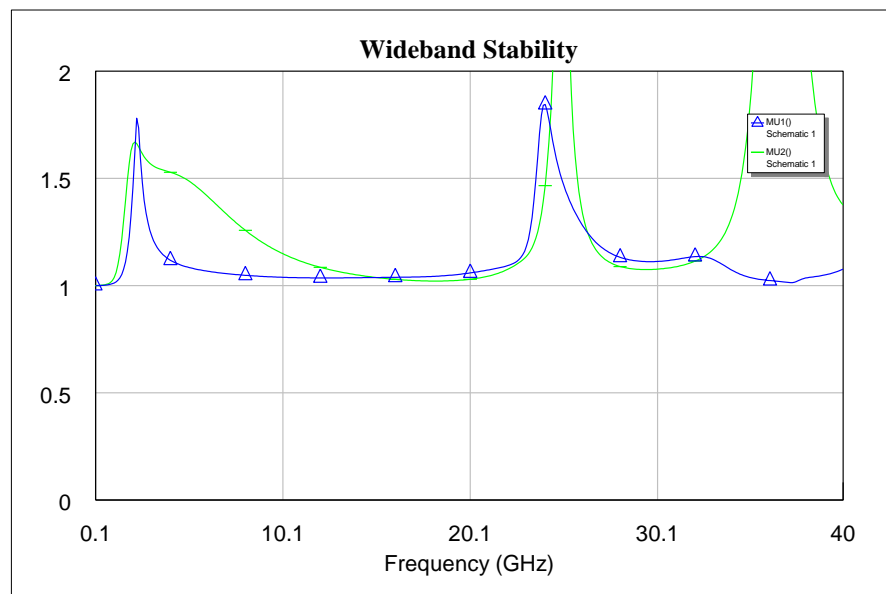


## Simulations

The source inductor and ideal matching network served as the starting point for the design. While the source inductor stabilized the amplifier in the operating frequency range, the actual design with layout had a strong potential instability at high frequency (above 10 GHz).



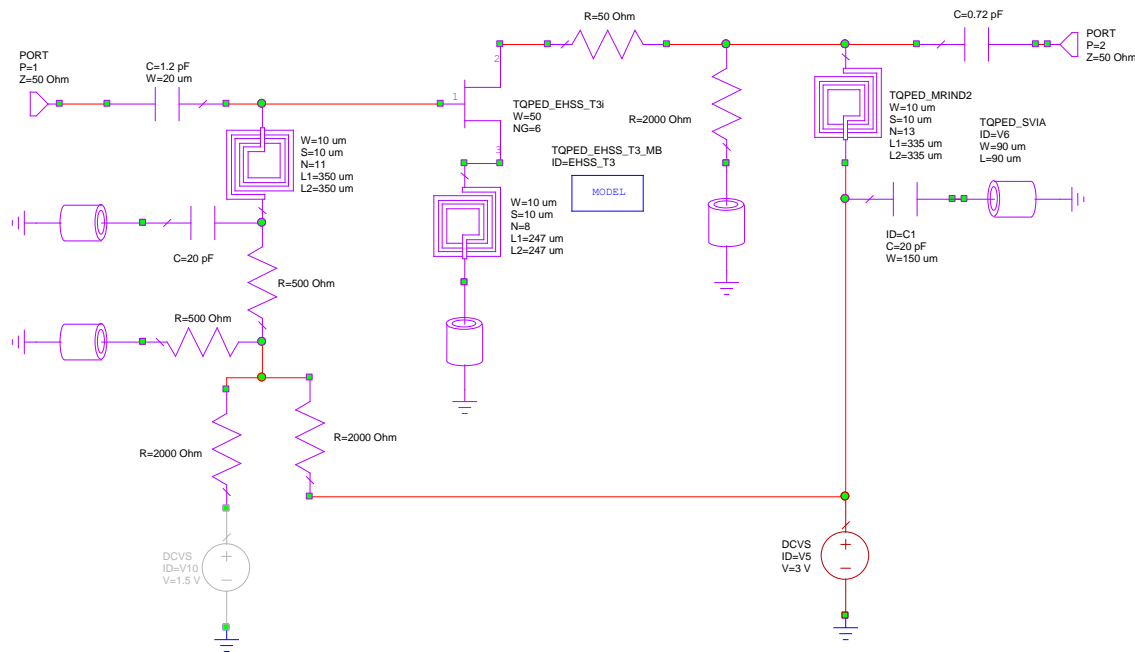
The addition of a series 50 ohm resistor followed by a shunt 2000 ohm resistor on the output solved this potential problem and achieved unconditional stability but did degrade the noise figure by approximately 0.07 dB (even though stabilization was all on the output).



Changing to actual Triquint TQPED spiral inductors degraded the noise figure, as expected. The source inductor was not a significant contributor (0.02 dB), and the input matching inductor was the dominant noise source, raising the noise figure by 0.2 dB. This brought the noise figure up to approximately  $0.48 + 0.07$  (stabilization)  $+ 0.02$  (actual source inductor)  $+ 0.2$  dB (actual input matching inductor) = 0.77 dB

This would have had an input return loss of approximately -10 dB, which would have likely been acceptable. However, subsequent tweaking found that at a relatively minor cost to noise figure, significantly better input return loss was achievable. Allowing another 0.05 dB of degradation allowed S11 to be  $< -17$  dB; this tradeoff for better input return loss was made in the final design.

Below is the final schematic. Note that the input and output matching networks are highpass topologies, allowing the shunt inductor to feed in the bias (with a large 20pF capacitor to RF ground the shunt inductors). No attempt was made at bypassing (either at DC or at 2.4 GHz) the resistors was used for high-frequency stabilization on the output. This does come at a cost.

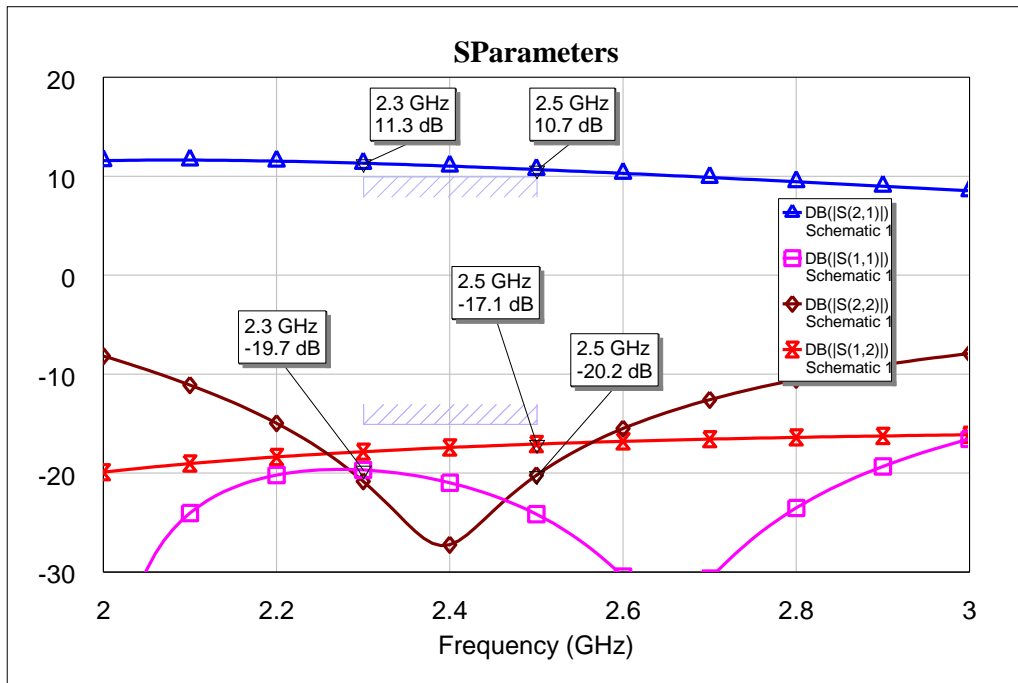


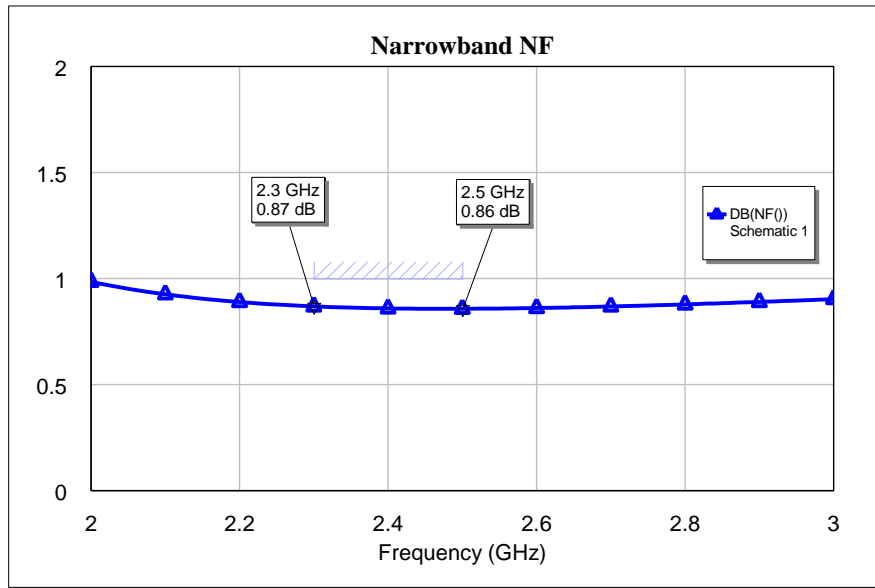
For DC power consumption, at 15 mA bias, the voltage drop across the 50 ohm resistor is 0.75V and the resistor consumes 11 mW. Similarly, the current draw through the 2000 ohm shunt resistor is 1.5 mA and the resistor consumes 4.5mW. This power consumption is unnecessary and could be eliminated. A capacitor in series with the 2000 ohm resistor would eliminate its power consumption, and an inductor in parallel with the 50 ohm resistor would eliminate its.

For RF, the 50 ohms is effectively in series with the output load. However, the output matching network presents the output 50 ohm load as approximately 200 ohms with impedance transformation, so the impact of the series 50 ohms is not as significant as it might initially appear, but simulation showed that there was a cost of approximately 1.5 dB of gain. This would also subtract from the output compression and intercept points of the device.

An attempt was made to bypass the 50 ohm resistor but the resonance of the bypass inductor adversely affected the high-frequency stability, defeating the original point of the 50 ohm resistor. So the inefficiency was accepted, and as an ancillary benefit, the 50 ohm resistor does serve to deliver a more constant current as a function of active device variation.

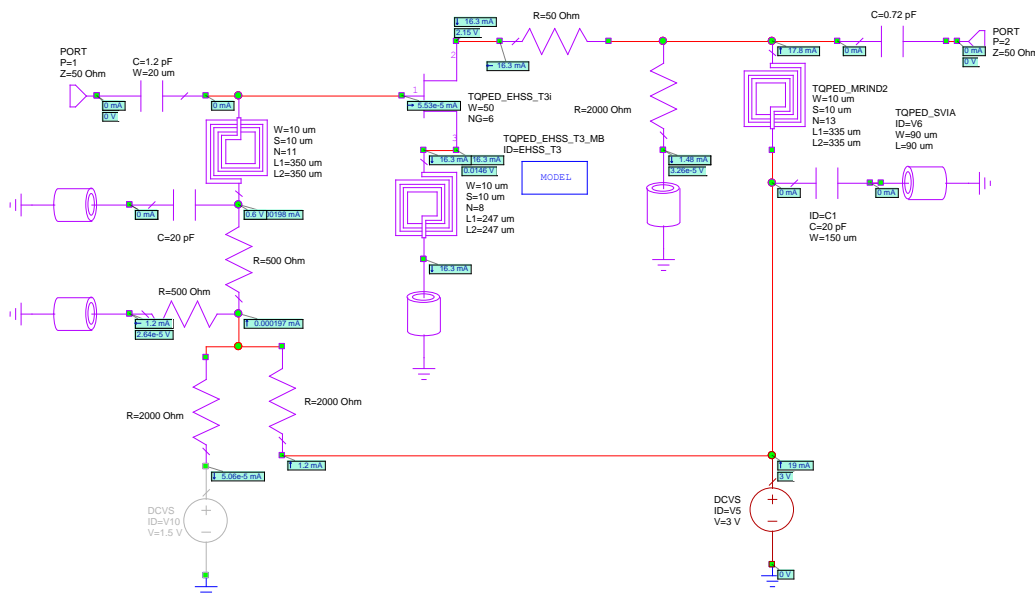
The final S-Parameters, after extracting the actual layout and tweaking the components to absorb the effects of the layout, are reflected in the following plot. Gain was 10.7 to 11.3 dB over the 2.3 to 2.5 GHz passband. Input and output return losses were ~ 20 dB and the reverse isolation was ~ 17 dB. Noise figure was 0.87 dB after all final tweaking – a degradation of approximately 0.4 dB from  $NF_{opt}$ .

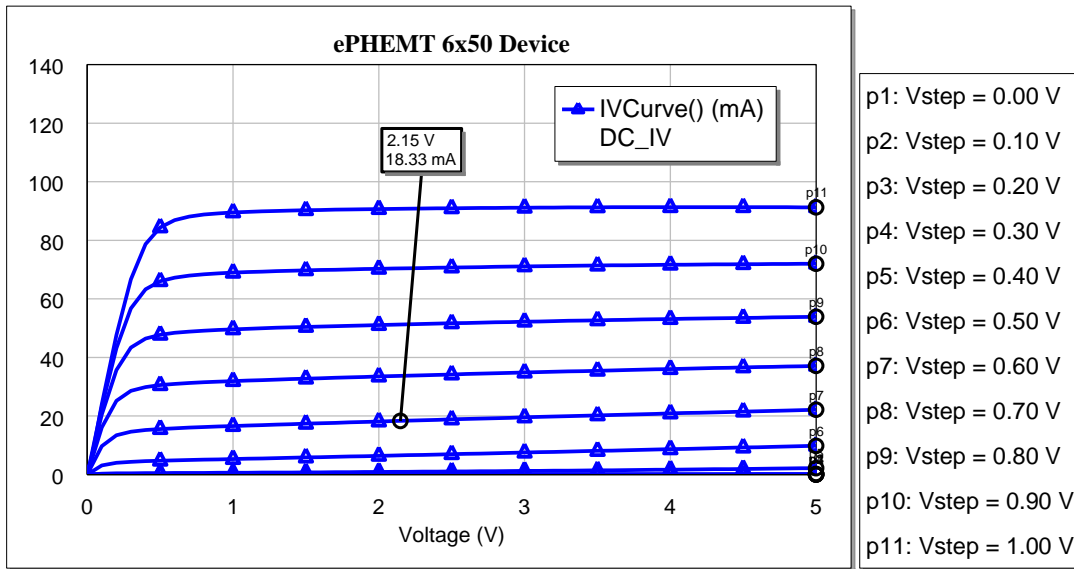




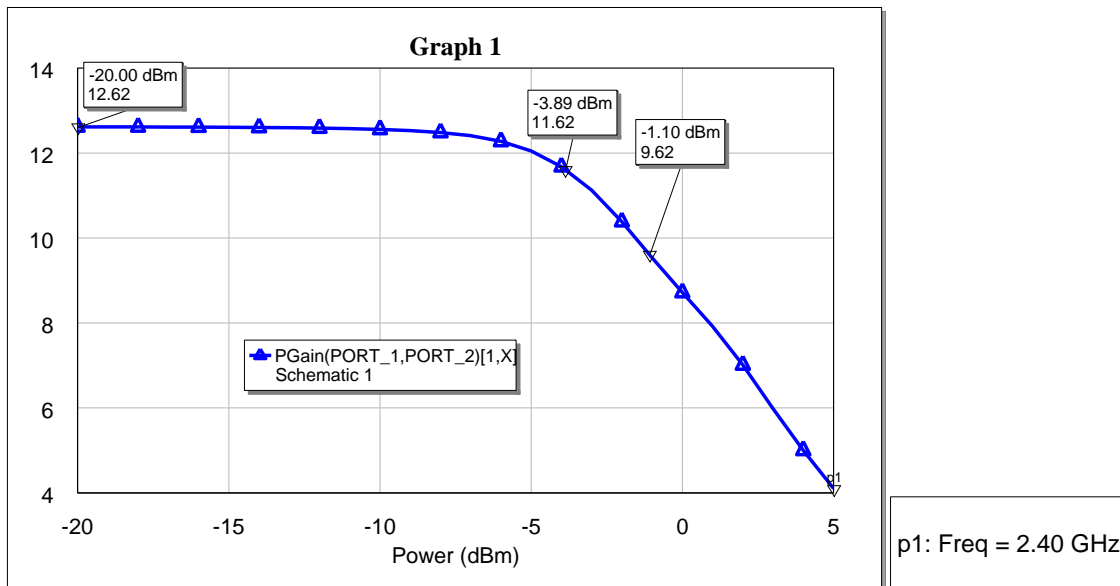
Bias was +3V / 19 mA, of which 16 mA was into the device. As already mentioned previously, 1.5 mA went into the output stabilization shunt resistor, and there was another 1.2 mA on the gate bias. A low frequency termination provided increased *low* frequency stabilization ( $f < 10$  MHz), so some extra current was consumed in providing that low frequency path.

$V_{ds}$ , with  $V_{cc}$  of +3V, is +2.15V and the gate is biased at 0.6V with a simple resistive voltage divider. An extra gate voltage was exposed in order to tweak the bias in order to account for the actual fabricated device which may draw more or less current at  $V_{gs} = 0.6V$ . An I-V curve is included showing the bias point is as expected ( $V_{gs}=0.6V$  and  $V_{ds}=2.15V$  predicted  $\sim 18mA$ ).



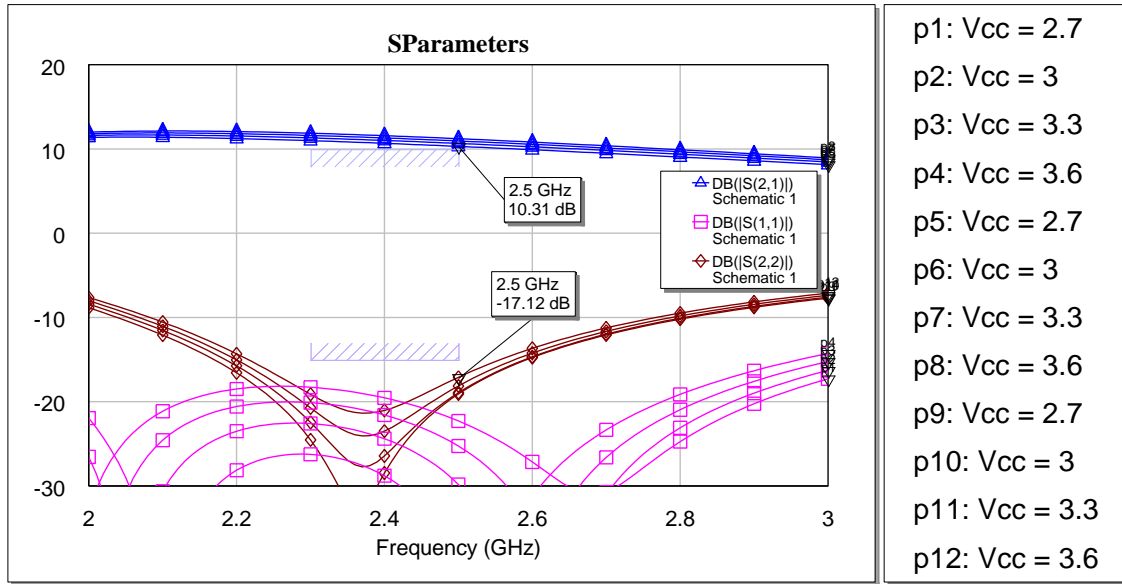


A power sweep was performed at 2.4 GHz to find P-1 dB. [Note: the small signal gain when driven from a power sweep source was 12.6 dB whereas the S-Parameter gain from a linear port was only 11 dB, and this discrepancy was never understood.] Using the 12.6 dB gain as the reference, P-1 dB occurred with an input of -3.9 dBm (output P-1 dB of +7.7 dBm). As a reference point, P-3 dB occurred at an input of -1.1 dBm (output of +8.5 dBm), showing that there is not much more output power to be had beyond P-1 dB (an extra 2 dB of drive only increased the output power by 0.8 dB).

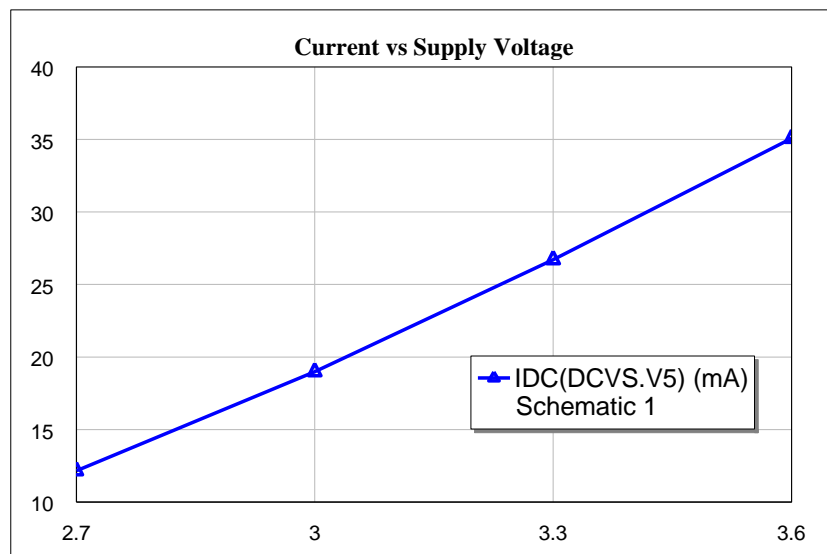


## Simulations vs. Variations

The design was tested against power supply variation from 2.7V to 3.6V. There was little variation in the S-Parameters, with the minimum gain only reducing to 10.3 dB and the worst return loss was 17 dB.

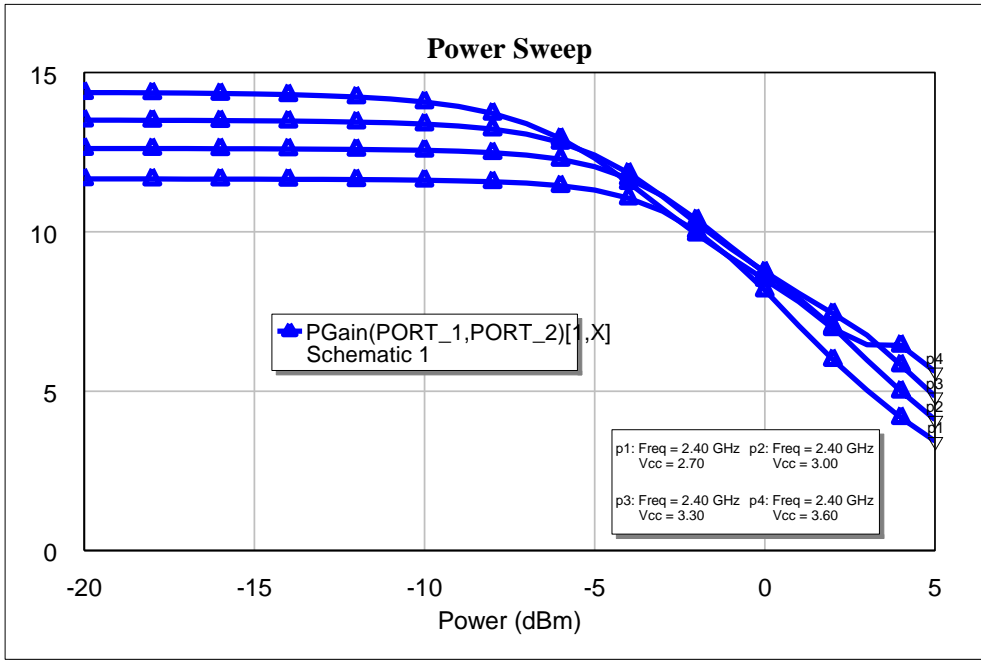


There was significant variation in the supply current as a function of supply voltage. This was expected, as the bias was a simple passive bias, a resistive divider of the supply voltage. The current varied from 12 mA to 35 mA for bias of +2.7V to 3.6V, respectively.



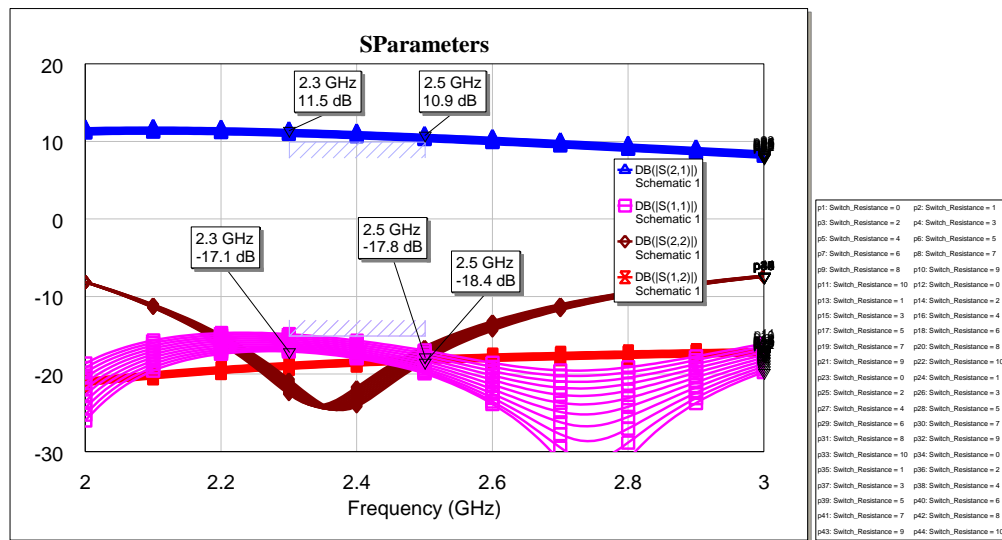


As mentioned earlier, there is a discrepancy between the gain when the source is a power sweep port instead of a linear sweep port, so the P-1 dB comparison as a function of power supply is not viewed as reliable. The power sweep showed the small-signal gain being as high as 14 dB, whereas the linear sweep gain was only as high as 11.8 dB.

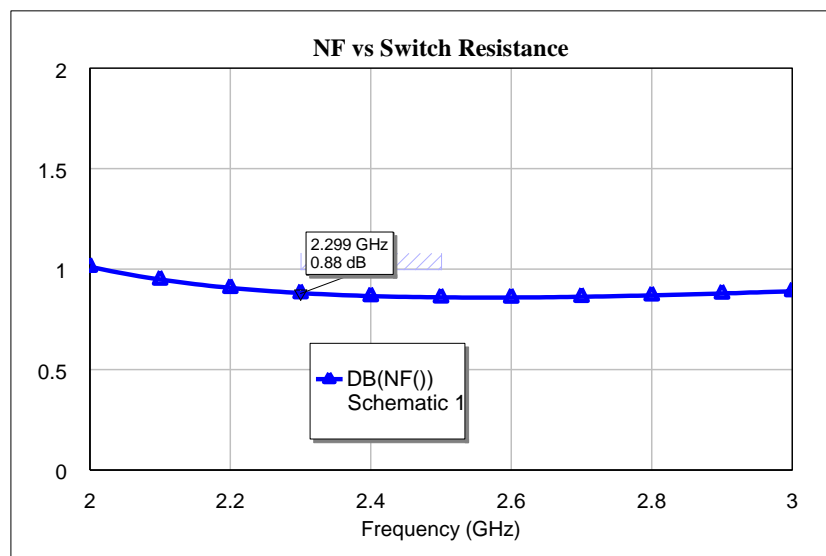


The design was simulated against variations in the source impedance. Specifically, it is likely that the LNA could be preceded by a transmit/receive FET switch with an ON resistance of a few ohms. A series resistance was swept from 0 to 10 ohms to model this effect.

Neither the S-Parameters nor the noise figure varied significantly. Gain stayed around 10 dB and the return losses were still > 15 dB each, so no redesign would be necessary to account for the increased source impedance presented by the preceding switch's ON resistance in series with the original source impedance of 50 ohms, although S11 could be improved slightly if desired.



Noise figure was virtually unaffected. While a series 10 ohm resistor certainly degrades the noise figure, the noise figure of the amplifier itself was not changed with the increased source impedance. Below is the LNA with a source impedance of 60 ohms; NF increased only 0.01 dB.

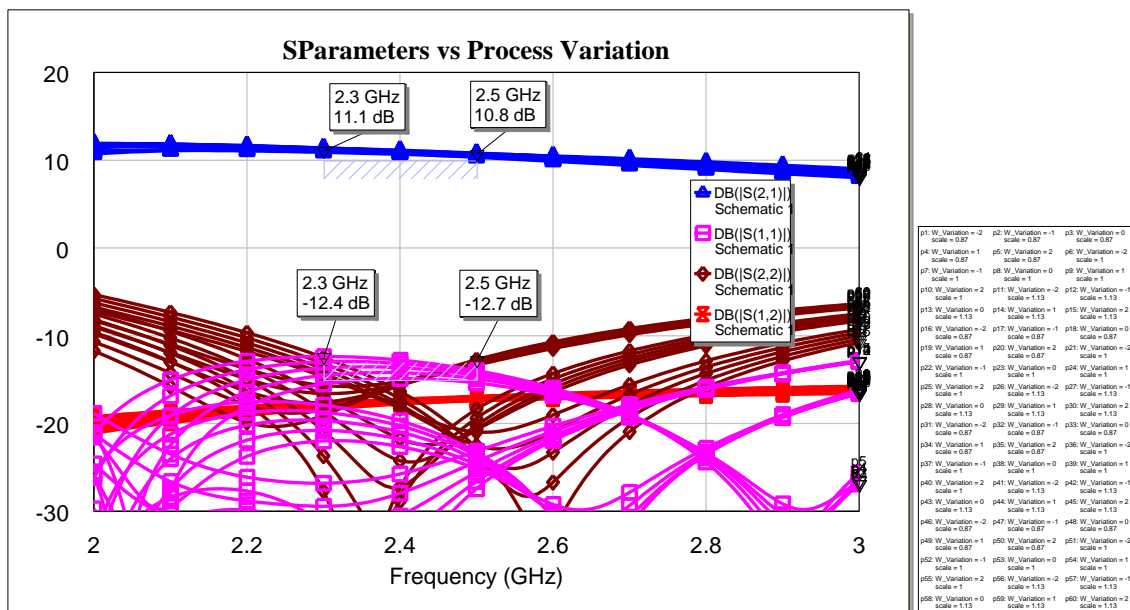


An attempt was made at simulating the process as a function of process variation. The width of the inductors and capacitors was set to be +/- 2 um from the nominal design and the S-Parameters were swept to reflect this variation.

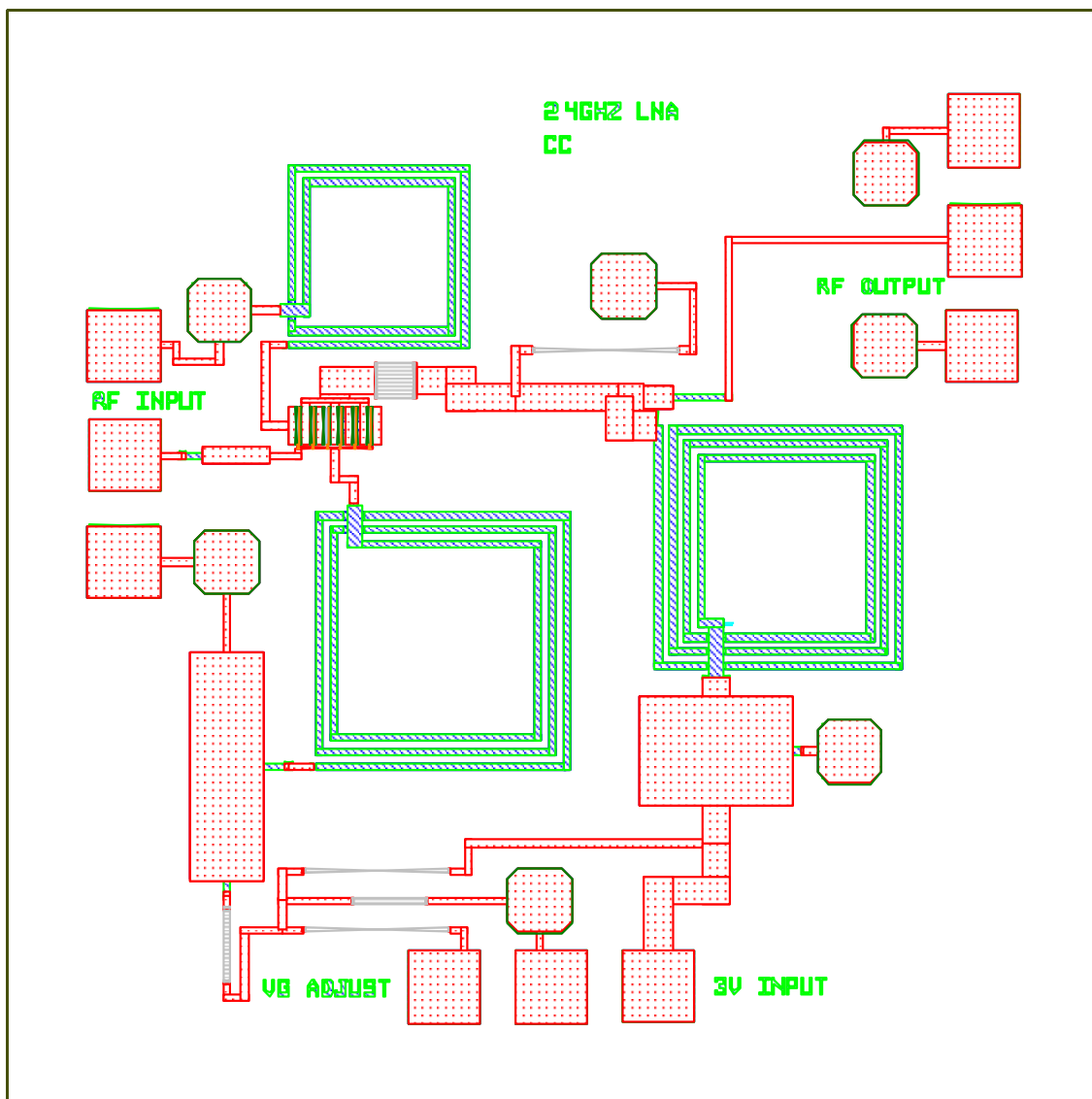
The choice of +/- 2 um was somewhat arbitrary, although it was based on the logic that if a feature size of 5 um was allowed, the tolerance could not be as bad as 5 um, and 2 um represented a significant variation as a percentage of an allowable feature size. The variations were assumed to be in the same direction for all components - either all increased or all increased by the same amount (and the validity of this assumption is not known). The resistors were not varied because there was little dependence on their actual values other than for bias (and the variation in bias due to resistor tolerance would be small compared to the significant variation which would occur for the +2.7V to +3.6V power supply variation, and the bias will be adjusted as necessary with the “Vg Adjust” pin).

Inductance values are mainly determined by the length. For example, an N=12 square spiral inductor with 300 mil length and width is 4.47 nH with 10 um width and 10 um spacing but only increases to 4.55 nH with 8 um width and 12 um spacing, a variation of < 2%.

The capacitance values are more strongly affected, as the capacitance is directly proportional to the area. A representative capacitor might have been 20 um X 50 um, so a variation of +/- 2 um represents a variation of almost 15% and this variation dominated the attempted Monte Carlo variation. However, the match was broadband enough to accommodate this variation and still achieve return losses of better than 12 dB – sufficient to only negligibly affect the gain.



The final layout is given below. The inductors provide a general reference for where the circuits are; the upper inductor is the source inductor, the lower-left inductor is the input matching inductor, and the right-most inductor is the output matching inductor. The layout was relatively straightforward, although the 50 ohm stabilization resistor (which became a 50 ohm bias resistor) was initially undersized. It was 10  $\mu\text{m}$  wide and the TQPED process specifies the NiCr resistors as being rated for 1.5 mA /  $\mu\text{m}$ , and there was simply no reason to design at the limit. The use of Metal0 (red) as the main routing layer would not normally be recommended, as the current handling is much reduced as compared to Metal1 and Metal2, but since the currents here are small, it is acceptable (and simplified routing, as capacitor connections always have one side connected to Metal0).



## Test Plan

### Test Equipment Required:

- Network Analyzer (S-Parameter Sweep)
  - Signal Generator / Spectrum Analyzer or Network Analyzer (Power Sweep)
  - Noise Diode / Spectrum Analyzer (Noise Figure Measurement)
  - ~ 20 dB of additional RF gain with characterized noise figure performance
  - Two RF Probes (RF Input and RF Output)
  - Two DC Probes ( $V_{cc}$  and  $V_g$  Adjust)
1. Starting at  $V_{cc}=0V$ , step up the supply voltage towards +3.0V, keeping track of the current draw. If the current approaches 19 mA (total, of which 16 mA will be into the device) before  $V_{cc} = +3.0V$  is achieved, utilize the “ $V_g$  Adjust” pin to override the passive on-chip gate bias and lower the gate voltage, ultimately allowing  $V_{cc}$  to be +3.0V with current of 19 mA. Similarly, if  $V_{cc} = +3.0V$  results in a current draw lower than 19 mA, utilize  $V_g$  Adjust to increase the gate voltage to achieve +3.0V / 19 mA operation. Note: while LNA was designed to be unconditionally stable, it would be recommended to terminate input and output into 50 ohms; an unexpected oscillation could affect the bias.
  2. Once properly biased, sweep the amplifier on a network analyzer with an input power of approximately -20 dBm (small signal relative to expected compression point). A sweep utilizing the full bandwidth of the network analyzer should be performed in order to verify out of band stability.
  3. A power sweep shall be performed, either using the network analyzer in single-frequency continuous wave (CW) mode or using a signal generator and a spectrum analyzer, to find P-1 dB. This should be verified at 2.3, 2.4, and 2.5 GHz.
  4. The noise figure of the device shall be characterized. With only ~ 10 dB of gain, additional amplification will be required to overcome the noise figure of the spectrum analyzer, with the amount of additional gain required dependent upon the spectrum analyzer’s performance (i.e. internal preamp or not).

## Summary and Conclusions

Revisiting the original specifications and goals:

Parameter	Specification	Goal	Design
Operating Frequency	2.3 to 2.5 GHz	2.3 to 2.5 GHz, same specs	
Gain, S21	10 dB < Gain < 12 dB	Same	10.7 – 11.3 dB
Gain Variation (Ripple)	< 1.0 dB	< 0.5 dB	0.6 dB
NF	NF < 1.0 dB	NF < 0.8 dB	0.87 dB
S11	< -10 dB	< -15 dB	< -19 dB
S22	< -15 dB	< -20 dB	< -20 dB
Power Supply Requirements	Single Supply, +3.0V	+3.0V to +3.6V operation	Little variation in S-Parameters
Power consumption	< 50 mW	Same	< 60 mW
Input P-1 dB	-3.5 dBm	Same	-3.9 dBm
Output P-1 dB	+6.5 dBm	Same	+7.7 dBm
Stability	“Stable” – no obvious issues, especially near operating frequency	Unconditionally Stable, entire frequency range	Unconditionally Stable, entire frequency range

The priority specifications of gain ~ 10 dB with a NF of < 1.0 dB were met. However, there is some room for improvement. Specifically, the resistive stabilization network consumes DC power (~ 9 mW) and the resistors are not bypassed at the operational frequency of 2.4 GHz, reducing gain, output power capability, and overall efficiency. Initial efforts of bypassing the resistor resulted in a high-frequency resonance so the resistors were not RF-bypassed.

Accepting an inferior input return loss would have allowed a slight improvement in noise figure (most likely < 0.1 dB improvement) and would also have allowed higher gain (less source inductor feedback).

The input P-1 dB specification was missed slightly, but the output P-1 dB was higher than spec. This was due to the unknown difference in simulated gain when driven from a power sweep source instead of a linear sweep.

The bias current variation as a function of power supply voltage, acceptable for now in a lab environment where it can be adjusted, would need to be reduced with active biasing techniques.

I would like to thank AWR / Microwave Office for the use of their IC design software and for the support from Gary Wray. I would also like to thank Triquint Semiconductor for allowing these circuits to be fabricated.

# **ISM Band Up/Down Mixer**

## Design Project Final Report

Design By:  
Steve Moeglein

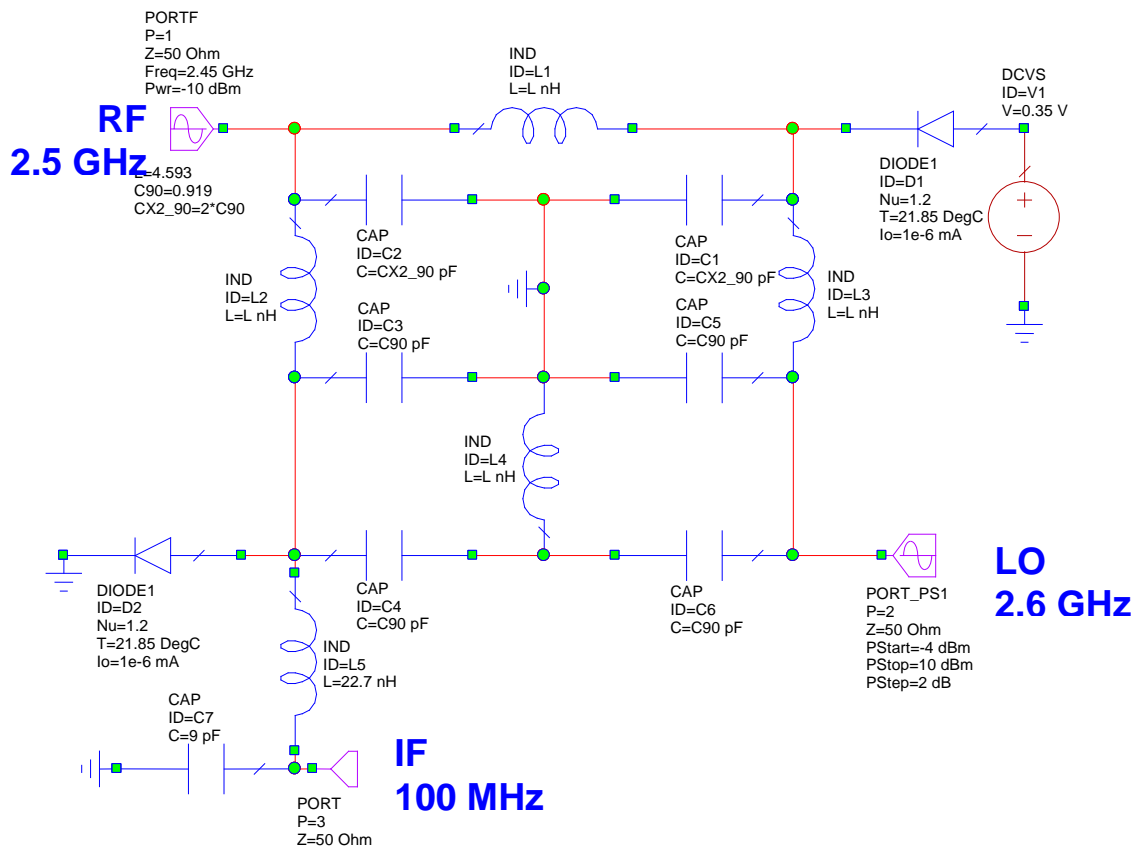
525.787.91 MMIC Design  
JHU Fall 2009

## Abstract

This paper describes the design and simulation of an Industrial, Scientific and Medical (ISM) band up/down mixer using the TriQuint Oregon process (TQOR TQPED) for monolithic microwave integrated circuit (MMIC) fabrication. The mixer was designed for a radio frequency (RF) input range of 2.4 – 2.5 GHz. The local oscillator (LO) design frequencies range from 2.3 – 2.6 GHz with an up/down-converted intermediate frequency (IF) of 100 MHz. The design uses two E-mode PHEMT devices, configured as diodes, and a rat race 180° hybrid coupler. Design simulations verified acceptable results: conversion loss less than 14 dB, RF/LO isolation greater than 20 dB, RF/LO input match of 10 dB return loss for a VSWR less than 2.0:1. The mixer did not meet all design requirements at the specified LO power of +7dBm. The design was not able to achieve the 10 dB conversion loss requirement at +7 dBm. The total DC power consumption is 0.988 mW from one 1.89 V supply. All simulations were performed in Microwave Office version 9.01b build 4856 Rev 1 from Applied Wave Research, Inc. (AWR) with the TriQuint process library v1.1.21.11.

## 1. Introduction

This ISM band up/down mixer design is intended to be part of the chip set for an ISM band transceiver. The up/down mixer utilizes a lumped element 180° hybrid rat race coupler with two diode configured E-mode PHEMT transistors to perform the mixing. An ideal lumped element model of this mixer is shown below in Figure 1.



**Figure 1: Ideal lumped element model of an ISM band up/down mixer**

The designed ISM band up/down mixer RF frequency range is 2.4 – 2.5 GHz and the LO frequency range is 2.3 – 2.6 GHz with an IF design frequency of 100 MHz. The design goal of the mixer was to provide 10 dB of conversion loss with a LO input drive of +7 dBm. While the design is functional the above goal was not achieved. Design simulations show conversion loss is approximately 13.3 dB with -10 dBm RF input



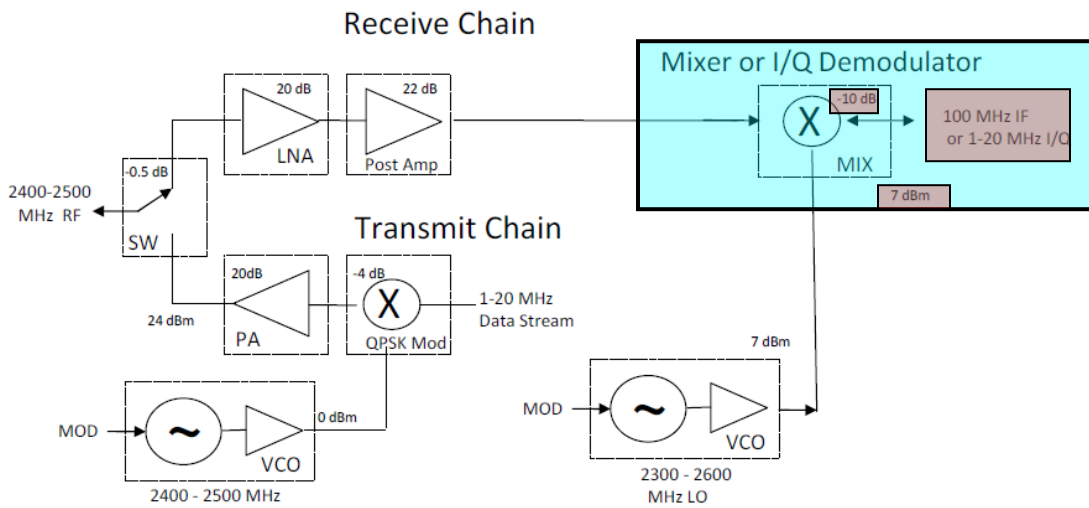
and +7 dBm LO input power. Optimal performance achieves 13 dB conversion loss with an LO input drive of + 12 dBm. The RF/LO input matches achieve 10 dB or greater return loss, with LO to RF isolation greater than 20 dB.

## 2. Design Approach

As part of the chip set for an ISM band transceiver, the up/down mixer must be designed to interface properly with the surrounding chips and packaging. This requires a block diagram with input/output (I/O) requirements defined for each MMIC chip. Often it is helpful to have a cascaded model of all the chips and packaging to identify any design aspects that need to be improved. However, due to time constraints, this was omitted and each MMIC chip designer was asked to consider this independently.

### 2.1. Block Diagram

Figure 2 below is the block diagram of the ISM band transceiver. This block diagram was used to define the basic I/O requirements for each MMIC chip design.



Chip Set for the 2400 - 2500 MHz ISM Bands

Figure 2: Block Diagram for ISM Band Transceiver Chip Set.

The ISM band up/down mixer and its basic requirements are highlighted in the block diagram in Figure 2 above. Other specific goals will be defined in the sections below.

### 2.2. Specific Goals

Using the requirements given in the block diagram in Figure 2 and basic RF performance knowledge, the following table of requirements and design goals were compiled to proceed with designing the ISM band up/down mixer.

Table 1: ISM band up/down mixer requirements and goals

Mixer Property	Minimum Requirement	Design Goal
RF Frequency Range	2.4 to 2.5 GHz	2.3 to 2.6 GHz
LO Frequency Range	2.3 to 2.6 GHz	2.3 to 2.6 GHz
IF Frequency	100 MHz	100 MHz
LO Input Power	+7 dBm	+7 dBm
Conversion Loss	10 dB	10 dB
Isolation (LO/RF)	Not Specified	20 dB
Return Loss/VSWR	Not Specified	9.54 dB/2.0:1 VSWR

In order to best meet the above design requirements, the following design approach was taken: Generate ideal models for each part of the design and slowly add non-ideal elements. This was done for the 180° hybrid rat race coupler, IF filter, diodes and finally the overall mixer with extracted RF traces in the finalized layout.

### 2.3. 180° Hybrid Rat Race Coupler Design

The rat race coupler was first designed ideally centered in the 2.3 to 2.6 GHz band or at 2.45 GHz. This ideal design was then implemented using non-ideal TriQuint elements. The figures below show the schematics and Sparameters for the non-ideal optimized circuit only.

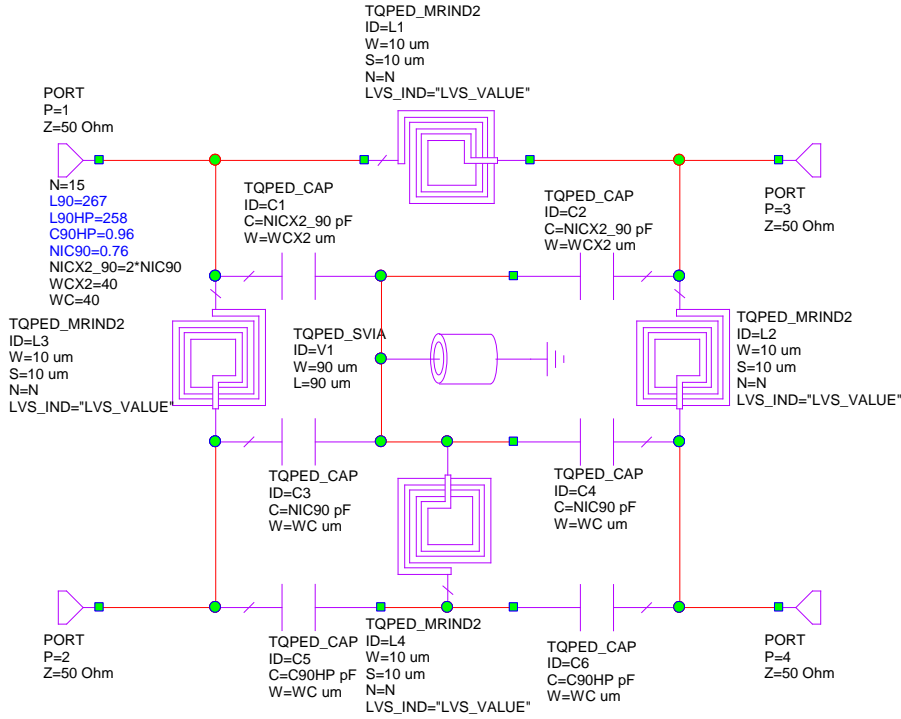


Figure 3: Non-ideal 180° Hybrid Rat Race Coupler

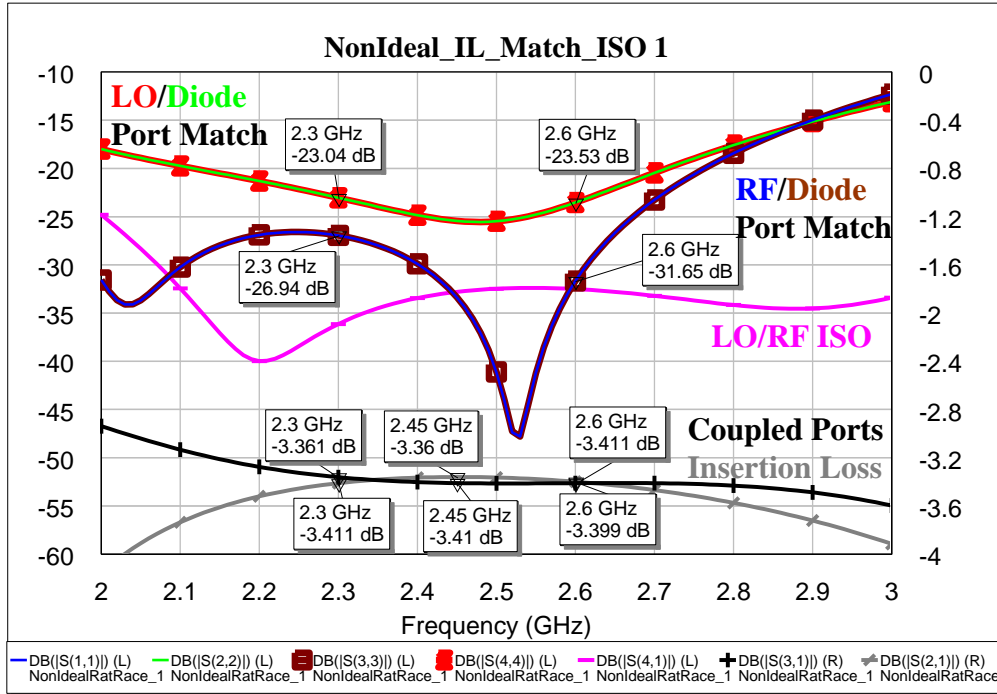


Figure 4: Sparameters for non-ideal rat race coupler design

## 2.4. IF Filter Design

Since a large inductor was required to create the IF port on the rat race coupler, a simple second order IF filter was designed to reduce the RF and LO present on the IF output. Ideal and non-ideal filter responses are plotted in Figure 5 below.

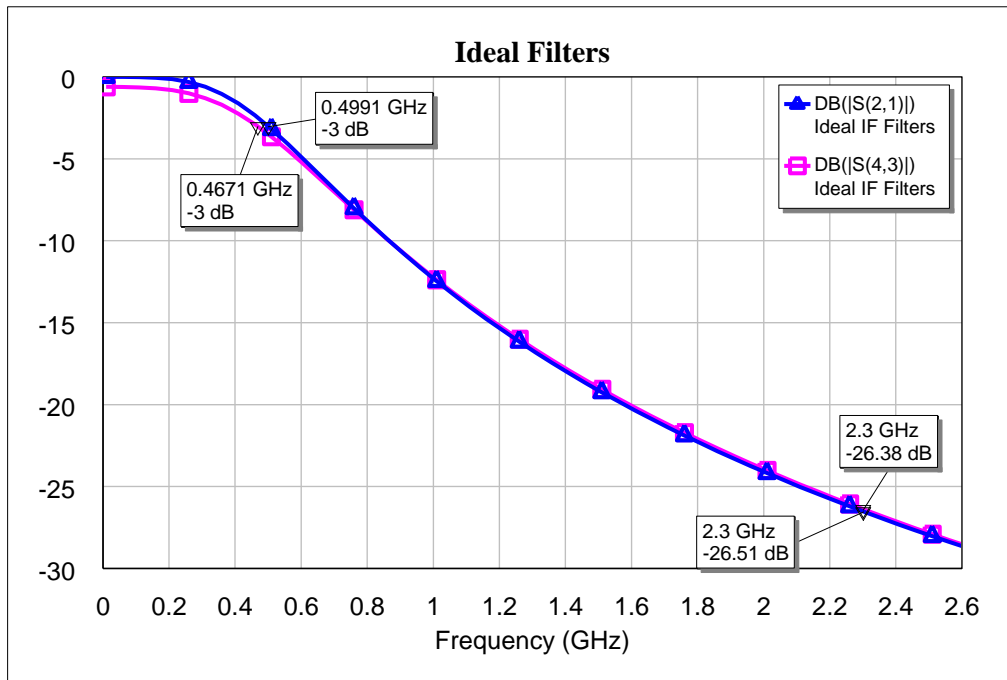


Figure 5: IF filter responses ideal (blue) and non-ideal (pink).

## 2.5. Diode Design

Both D-mode and E-mode PHEMT transistors were available for use in a diode configuration. Transistors can be utilized as diodes by shorting drain and source together to form the cathode and the gate becomes the anode. To have the least impact on the rat race coupler performance, the diodes would ideally look like  $50\Omega$  loads. However, these diodes look like low value series RC's when plotted on a Smith chart. Matching networks could be designed to match the diode to the  $50\Omega$  rat race coupler, but they consume valuable real estate on the 60 X 60 mil anachip layout. For this reason the periphery of the transistor was optimized to provide the best performance.

After simulating both D-mode and E-mode diodes with the rat race coupler, an E-mode diode was selected with three, 30um long gates ( $3 \times 30\text{um} = 90\text{um}$  periphery). The IV characteristic of this E-mode diode is plotted in Figure 6 below.

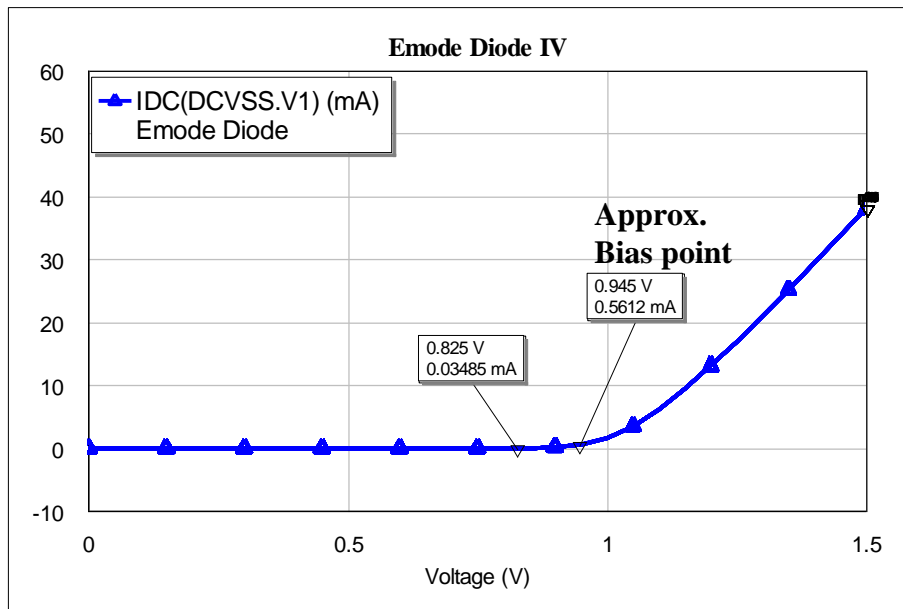


Figure 6: 3 x 30 um Emode diode bias point in mixer design.

## 2.6. Mixer Design

The E-mode diodes were added to the rat race coupler to create the ISM band up/down mixer configuration. The diodes were added to ports 2 and 3 in an anti-parallel configuration. The IF filter was also added to port 2 of the rat race coupler to create the IF port of the mixer. Diodes were biased at the turn on threshold in order to reduce the amount of LO input power required to turn them on and off. This diode bias made it necessary to add DC blocking capacitors to the RF, LO and IF ports to prevent the bias current from flowing into the RF terminations. This allowed the diodes to be properly biased, while preserving the RF performance of the mixer. Sparameters of the final mixer design are shown in Figure 7 below.

## 2.7. Trade Offs

Many trade offs had to be made during the design of the ISM band up/down mixer. The main performance trade made was the balance between conversion loss and port match. Diode size and bias could be optimized for conversion loss or port match, but not both. Ultimately, I chose to sacrifice the 10 dB conversion loss requirement in order to provide a better match to the rest of the ISM band transceiver. The 3 dB increase in conversion loss could be absorbed by an amplifier on either side of the mixer without impacting the overall transceiver performance. The lack of space on the anachip layout also impacted this performance trade by not having enough space to add diode matching networks.

### 3. Simulations

A summary of simulation results is shown in Table 2.

Table 2 : Summized Simulation Results

Mixer Property	Simulated Result	Minimum Requirement/Goal
Conversion Loss	13.3 dB	10 dB
LO Input Power	+7 dBm	+7 dBm
Isolation (RF/LO)	> 24 dB	20 dB
Match/VSWR	9.9 dB/1.94:1 VSWR	9.54 dB/2.0:1 VSWR

#### 3.1. Linear Simulations

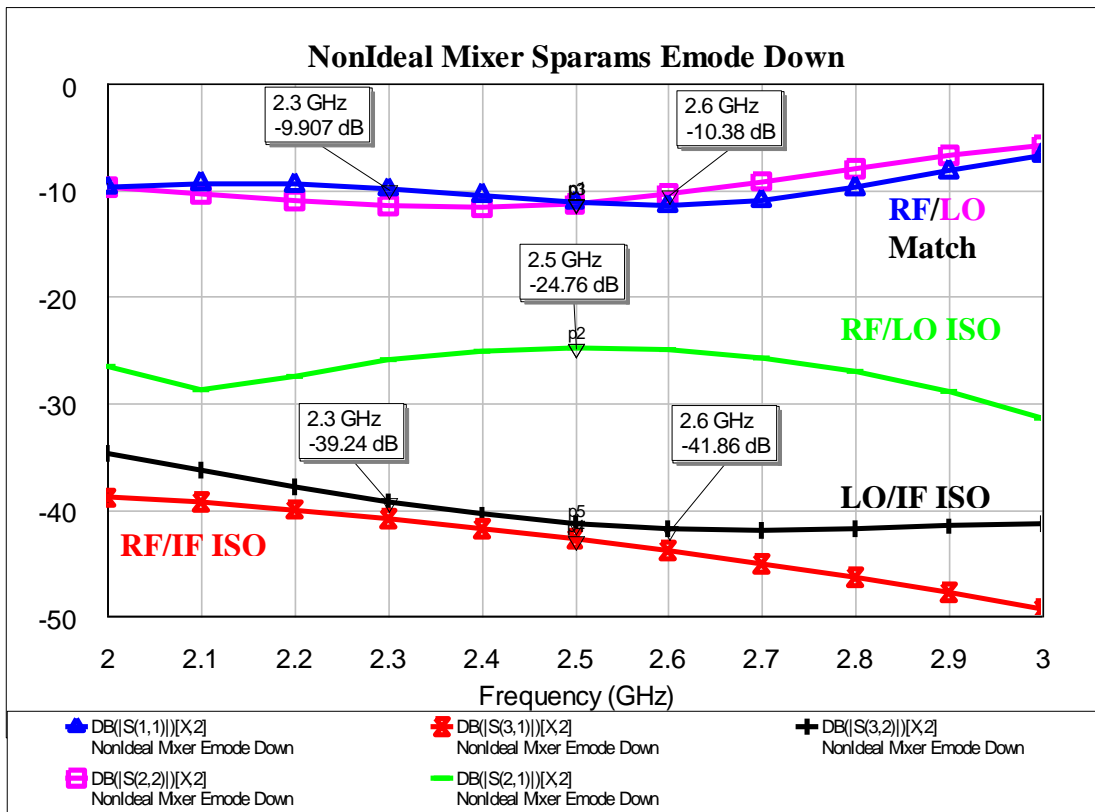


Figure 7: Final ISM band up/down mixer linear Sparams.

## 3.2. Non-Linear Simulations

### 3.2.1. Up Conversion Loss

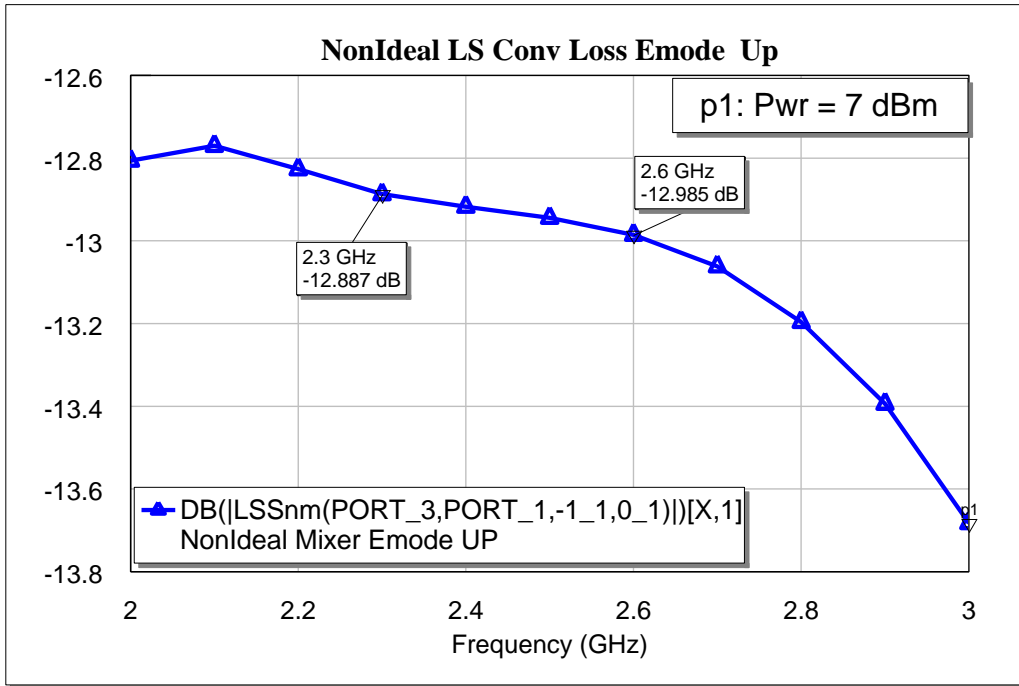


Figure 8: Up conversion loss vs. frequency

### 3.2.2. Down Conversion Loss

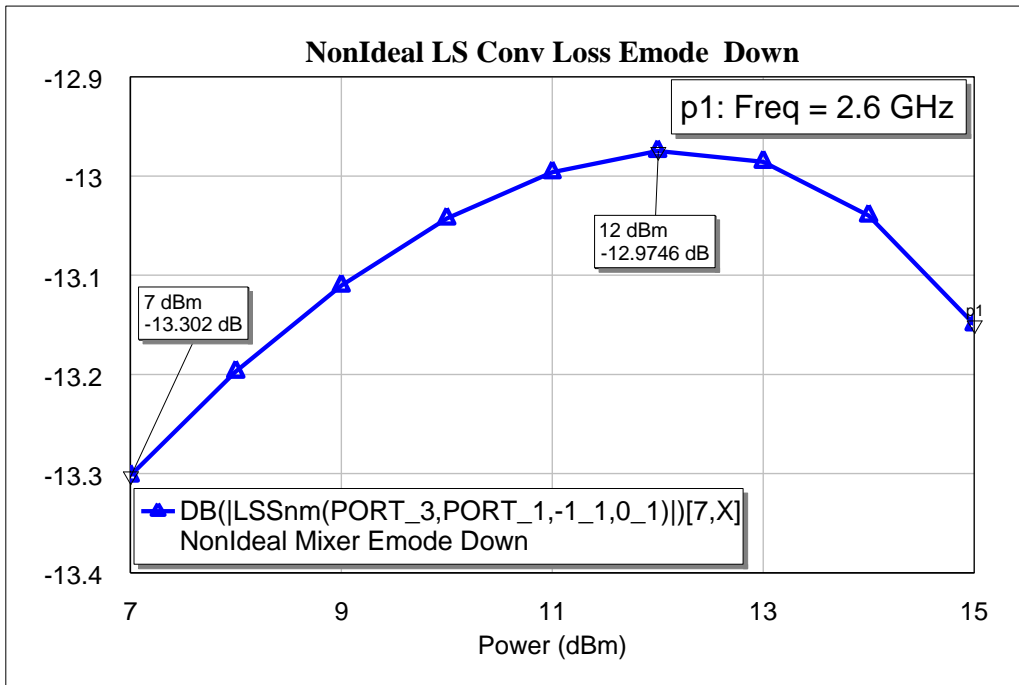


Figure 9: Down conversion loss vs. LO input power

### 3.2.3. Up Conversion RF Spectrum

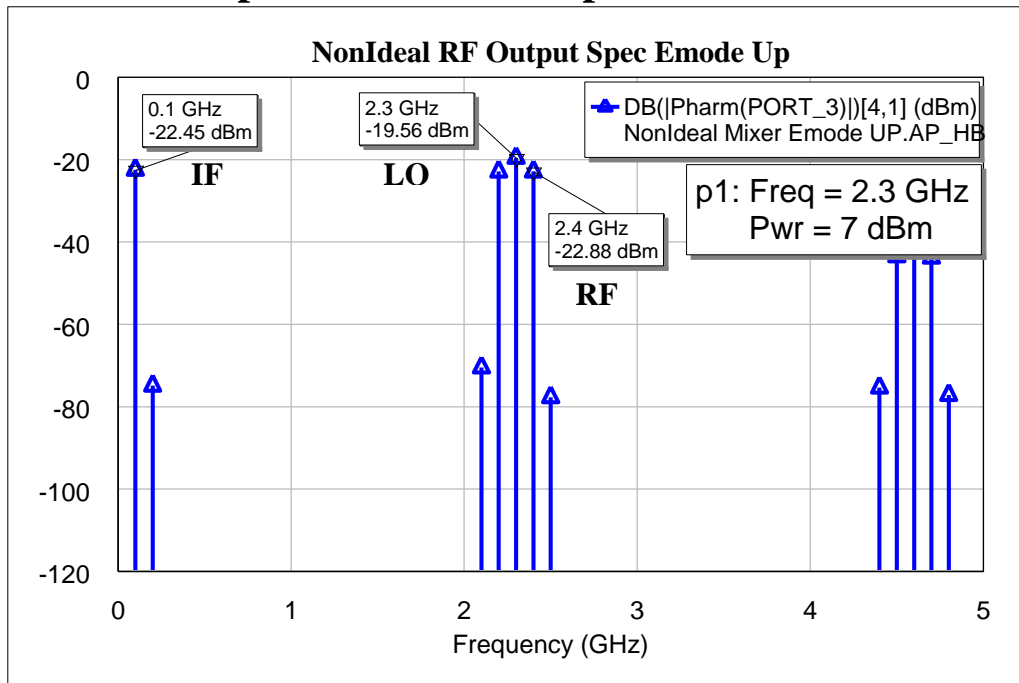


Figure 10: Low band Up conversion RF Spectrum IF=-10 dBm, LO=7 dBm

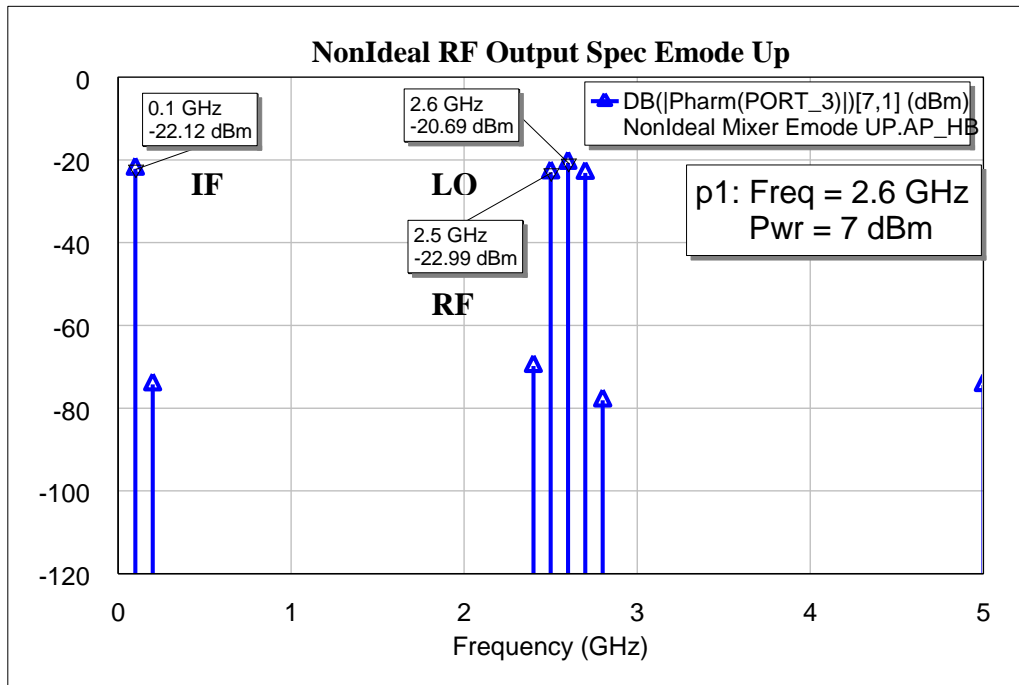


Figure 11: High band Up conversion RF Spectrum IF=-10 dBm, LO=7 dBm

### 3.2.4. Down Conversion IF Spectrum

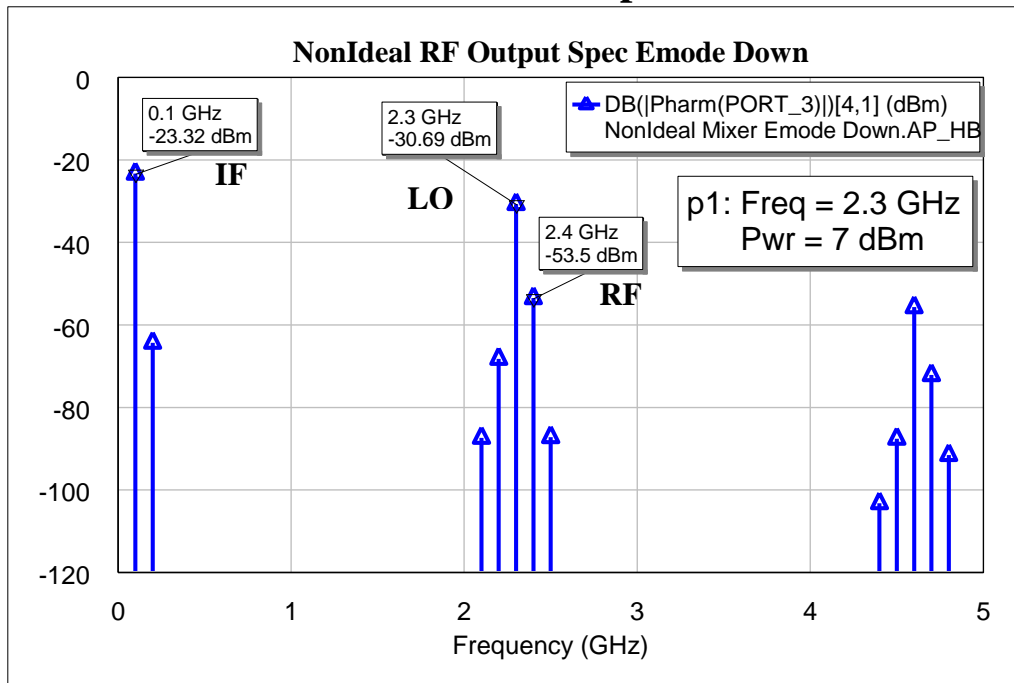


Figure 12: Low band Up conversion IF Spectrum RF=-10 dBm, LO=7 dBm

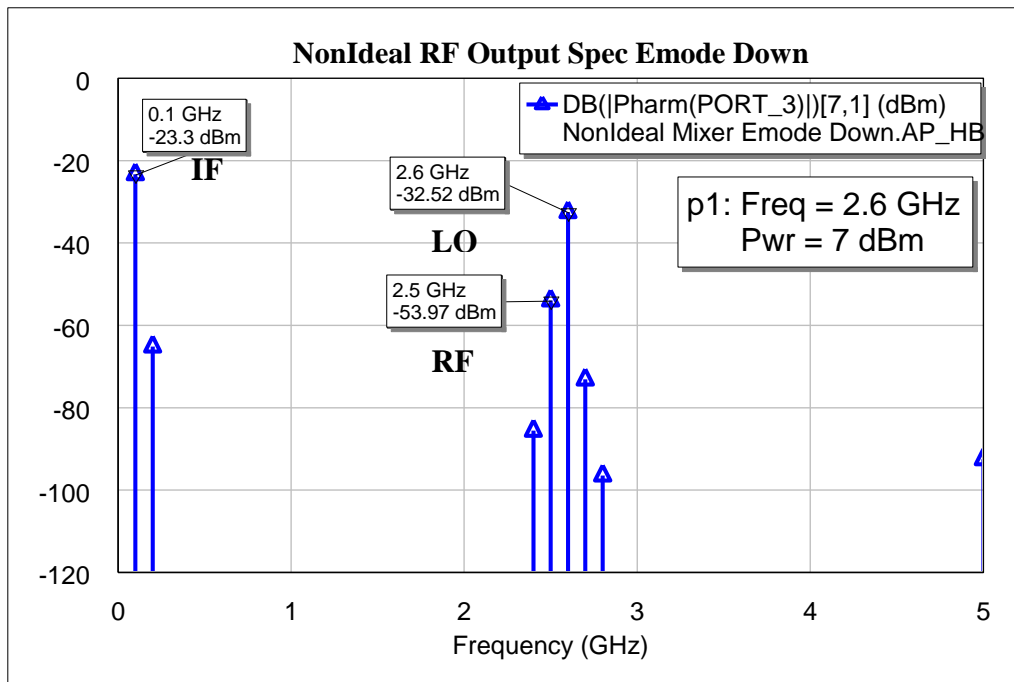


Figure 13: Low band Up conversion IF Spectrum RF=-10 dBm, LO=7 dBm



### 3.3. DC Bias (1.89V @ 0.528 mA)

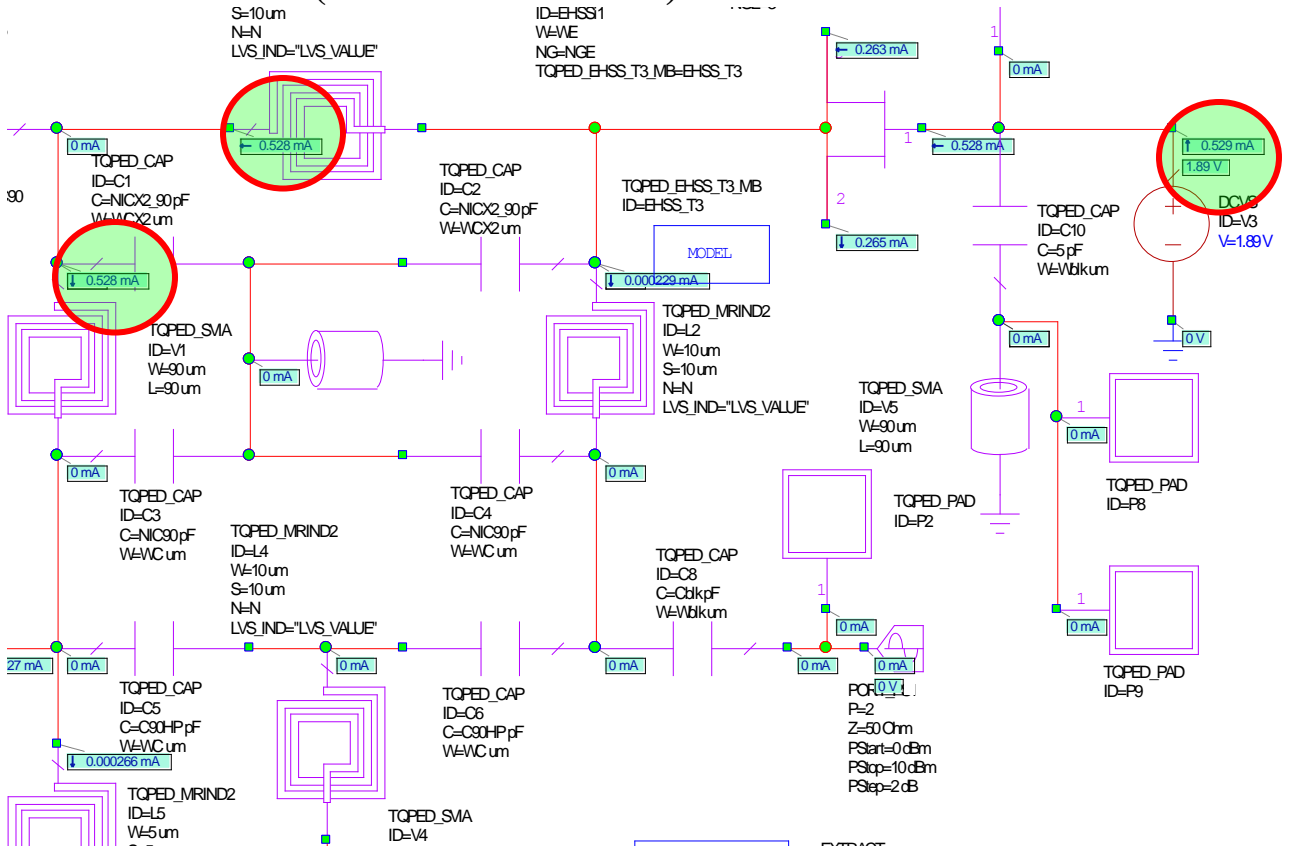


Figure 14: DC Bias Analysis

# 4. Schematics

## 4.1. RF Schematic

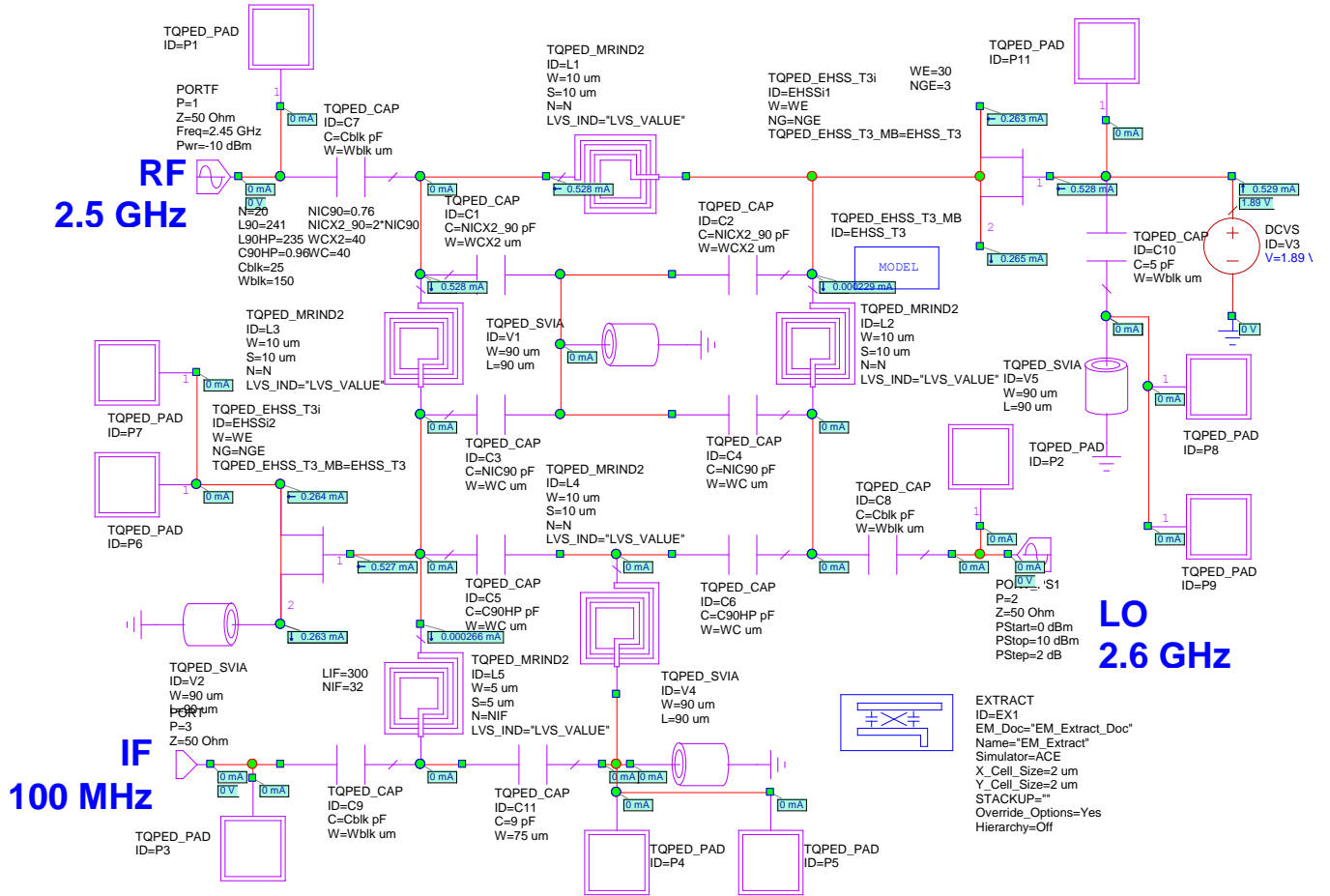


Figure 15: ISM band up/down mixer RF schematic

## 4.2. Simple DC Schematic

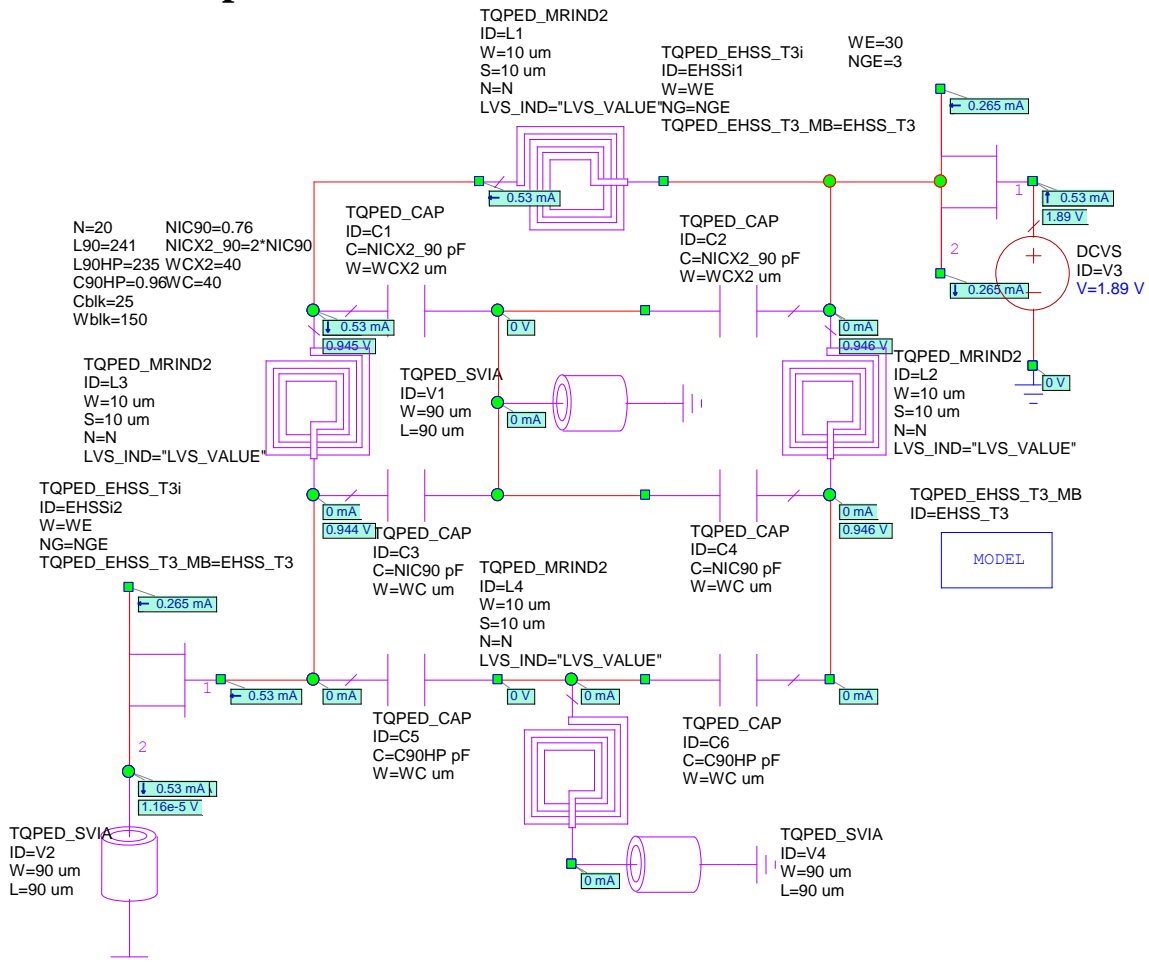


Figure 16: Simple DC schematic of ISM band up/down mixer

## 5. Layout

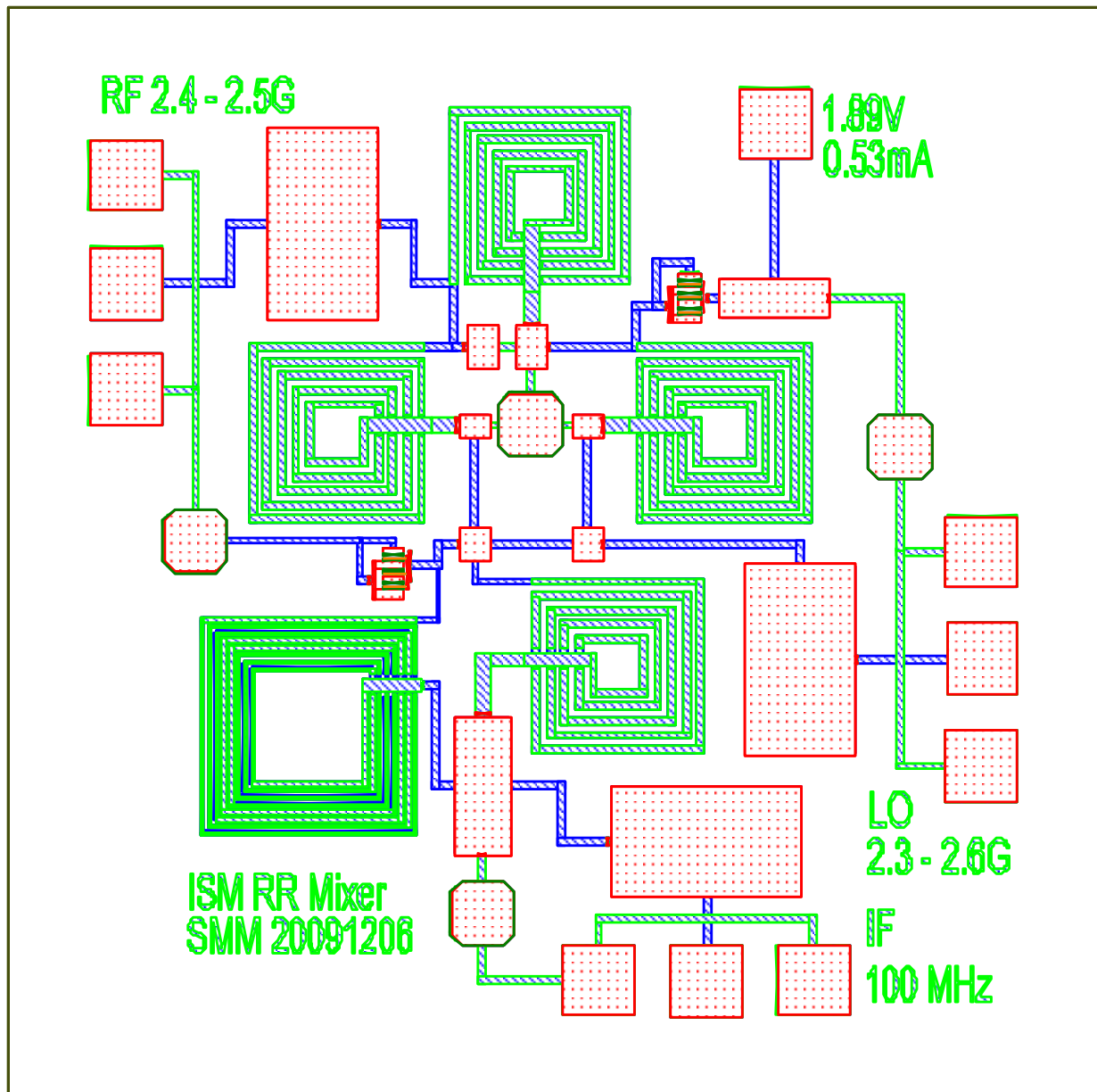


Figure 17: Final layout of ISM band up/down mixer on 60 x60 mil anachip.

## 6. Test Plan

### 6.1. Sparameter Testing

1. Connect network analyzer to the appropriate ports. Use RF as port 1 and LO as port 2. Setup to sweep from 2.0 – 3.0GHz.
2. Terminate IF port into a 50 ohm load
3. Apply 1.87 Vdc to the DC bias terminal. Should see 0.528 mA current draw.
4. Measure the s-parameters

## 6.2. Up Mixer Testing

1. Connect a signal generator to the LO port. Setup sweep from 2.3 – 2.6GHz in 0.1GHz increments. Set power output to +5dBm.
2. Connect a signal generator to the IF port. Set the frequency to 100MHz. Set power output to -10dBm.
3. Connect a spectrum analyzer to the RF port
4. Apply 1.89Vdc to the DC bias terminal. Should see 0.528 mA current draw
5. Measure RF output power at each LO frequency
6. Repeat above measurements for LO input powers of 7, 9, 11, and 13 dBm

## 6.3. Down Mixer Testing

1. Connect a signal generator to the LO port. Setup sweep from 2.3 – 2.6GHz in 0.1GHz increments. Set power output to +5dBm.
2. Connect a signal generator to the RF port. Setup to sweep from 2.4 – 2.5GHz in 0.1GHz increments. Set power output to -10dBm.
3. Note: Keep the RF and LO signals consistent with a 100MHz IF output signal
4. Connect a spectrum analyzer to the IF port
5. Apply 1.89 Vdc to the DC bias terminal. Should see 0.528 mA current draw.
6. Measure the 100MHz IF output power at each frequency interval
7. Repeat above measurements for LO input powers of 7, 9, 11, and 13 dBm

## 7. Summary & Conclusions

The ISM band up/down mixer design meets almost all requirements at +7 dBm LO input power. The requirement that could not be met was the 10 dB conversion loss requirement. The design could be further optimized to center the best conversion loss performance around +7 dBm LO input power and the center of the RF frequency band. However, I'm not completely sure that the 10 dB conversion loss requirement could be met. Future work would include further tuning of the rat race coupler to center the conversion loss performance. Additionally, a resistor network could be added to allow a standard battery supply voltage of 3.0 V or 3.6V to be used. Finally, given more space diode matching networks could be utilized to improve the LO and RF port matches.

**2.4 GHz Low Noise Amplifier**

**EE 525.787 MMIC Design**

**Fall 2009**

**Michael Dauberman**

## **ABSTRACT**

The purpose of the low noise amplifier is to take in a weak signal acquired by a RF receiver antenna, and provide a good amount of gain without adding much additional noise. This helps create a robust signal that can be passed through the rest of the receiver system and be accurately demodulated.

## **INTRODUCTION**

The following report details the design of a low noise amplifier chain at 2.4 GHz using a TriQuint 6 x 50, 0.5um Dmode PHEMT FET. In order to optimize noise figure while still achieving a sufficient amount of gain to overcome any additional noise added further in the receiver system, two stages of amplification are used. Combined, this design achieves a noise figure of less than 1.0 dB and gain of 20 dB. Each FET is biased at 3.0V VDS and ~25% IDSS (15mA). Also heavily considered in this design was unconditional stability at all frequencies. If the amplifier turns out to be unstable even outside of the working bandwidth, this can ruin the in-band performance. Since we rely heavily on linear simulations for noise figure, any instability outside of the frequency of interest won't show a degradation of performance elsewhere.

## **DESIGN APPROACH**

The simplest approach in designing a low noise amplifier is to simply stabilize the output of the FET using resistors, design an input matching circuit to match to the  $\Gamma_{opt}$  of the device, and then design an output matching circuit to the devices conjugate impedance. However, in order to meet the design goals set, a different method of stabilization must be explored.

After a few design iterations, it became evident that using a small amount of source inductance combined with output stabilization resistors, led to achieve the lowest noise figure while maintaining wideband stability and a good amount of gain.

This method was again used on the second stage amplifier, but increasing the source inductance to further guarantee a more stable cascaded design.

## **SPECIFICATIONS AND GOALS**

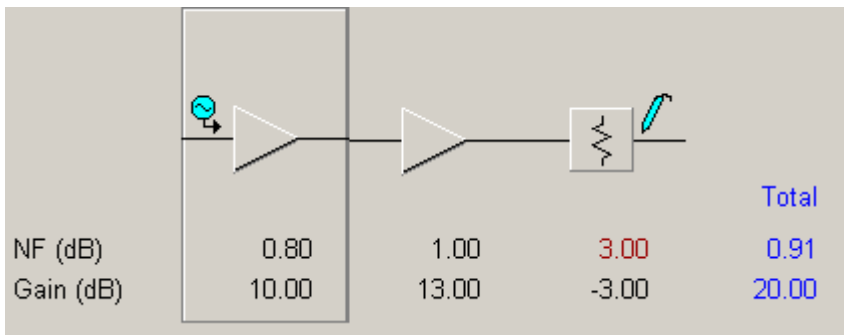
The major goal of this design was to achieve a minimal noise figure (less than 1.0 dB) while maintaining a very broadband unconditional stability requirement.

The specifications and goals for this LNA design are as follows:

<b>PARAMTER</b>	<b>SPECIFICATION</b>	<b>GOAL</b>
Noise Figure	1.5 dB	1.0 dB
Gain	20 dB	23 dB
Input VSWR	-	1.8 : 1
Output VSWR	1.5 : 1	0.7 : 1
Supply Voltage	3 V	-
Current Consumption	30 mA	
Stability	Unconditionally stable at 2.4 GHz	Unconditionally stable from 100MHz to 10 GHz



For each stage of the design, the following block diagram roughly shows what the goal of each stage is:



## TRADEOFFS

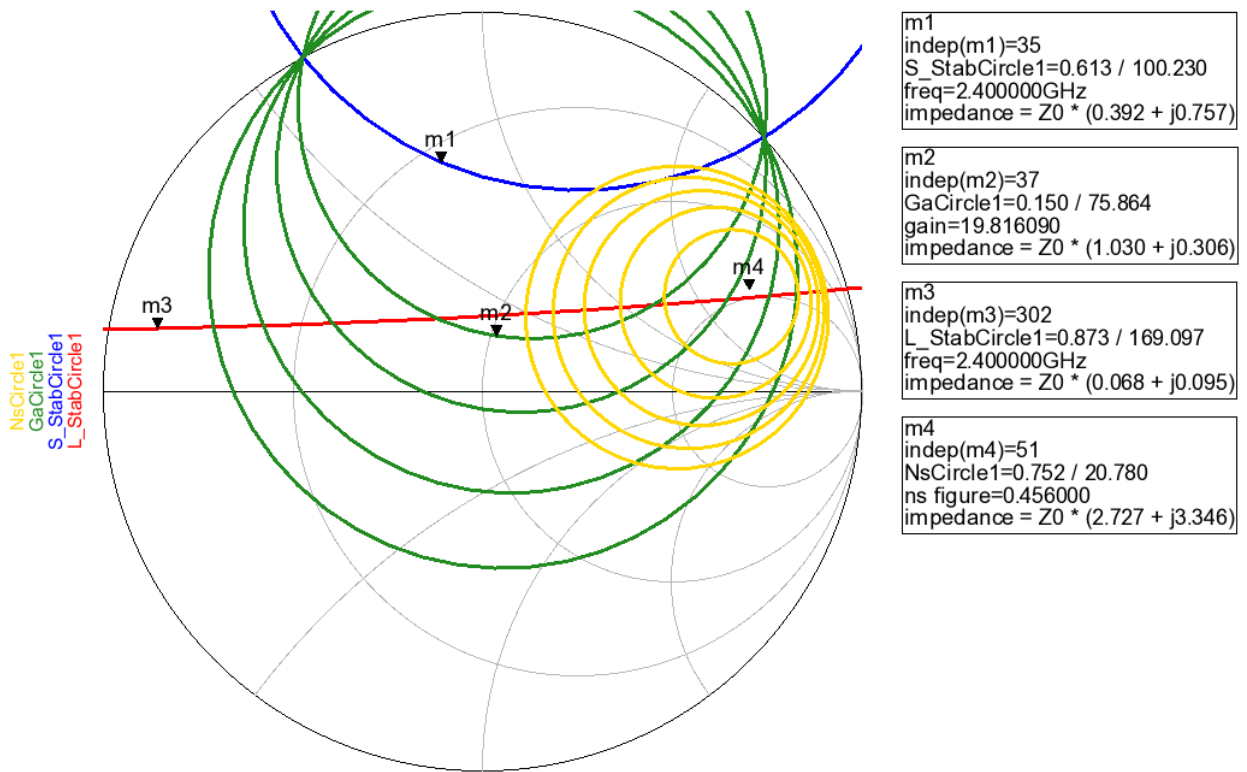
There are always some tradeoffs when designing a low noise amplifier. Depending on what the systems requirements are, certain tradeoffs must be made in the design.

One of the major tradeoffs typical of a low noise amplifier is the input return loss. Depending on the amplifier used,  $\Gamma_{opt}$  can be pretty far away from the  $S_{11}$ . This design optimizes for the lowest noise figure without paying much attention to the input return loss. Depending on the receiver system, we usually don't care much about the input return loss because any reflected signal will just travel back out of the antenna and not affect any downstream receiver performances

Because of the design goal of unconditional stability over a very wide frequency band, stabilizing the device became more of a challenge. It is possible to achieve a lower noise figure and a higher gain with the TriQuint 6 x 50, 0.5um Dmode PHEMT device, but the chances for any instabilities that could ruin its entire performance would be much greater. In order to guarantee unconditional stability over a broader range, the noise figure and gain of this design were degraded.

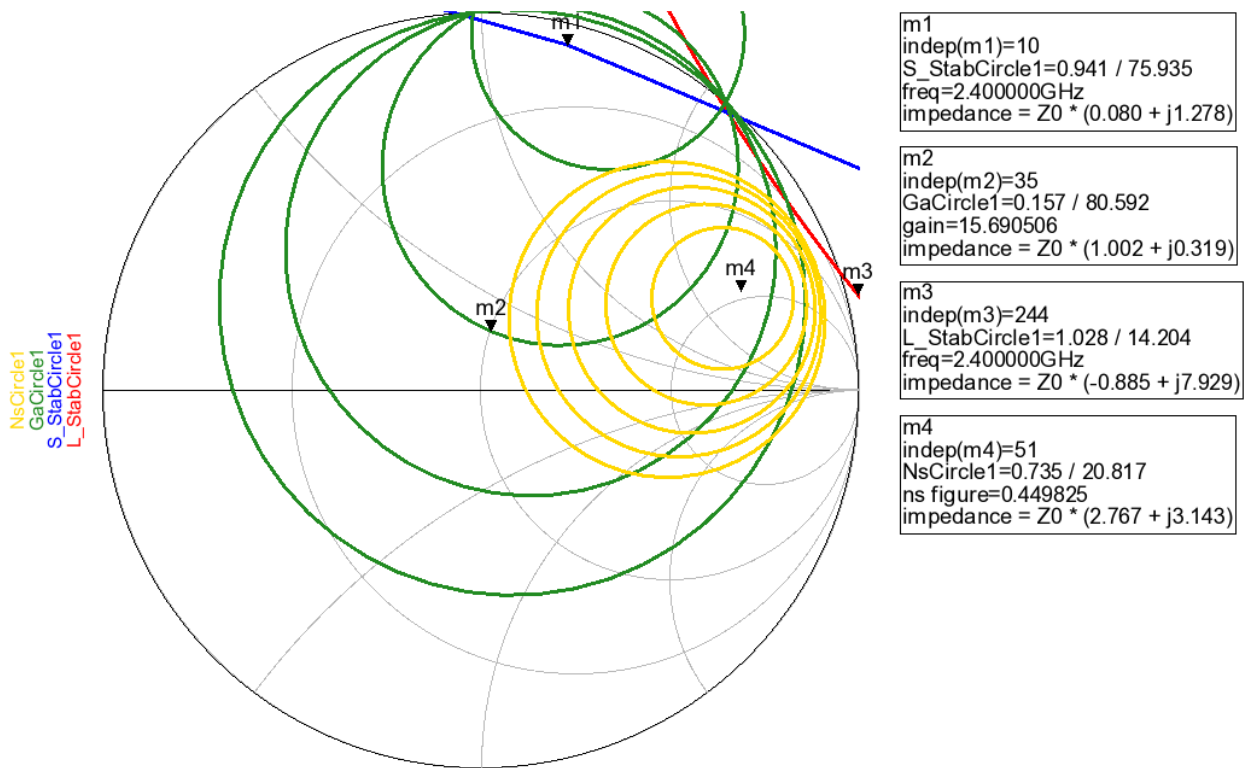
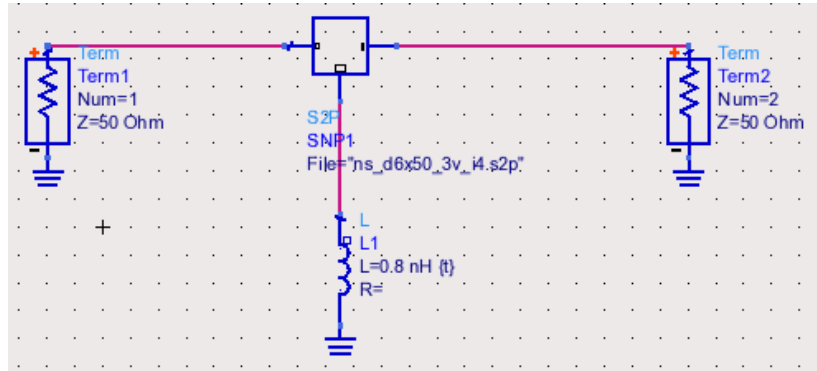
## SIMULATIONS

Beginning with a simulation of Noise Figure and gain circles along with stability circles:



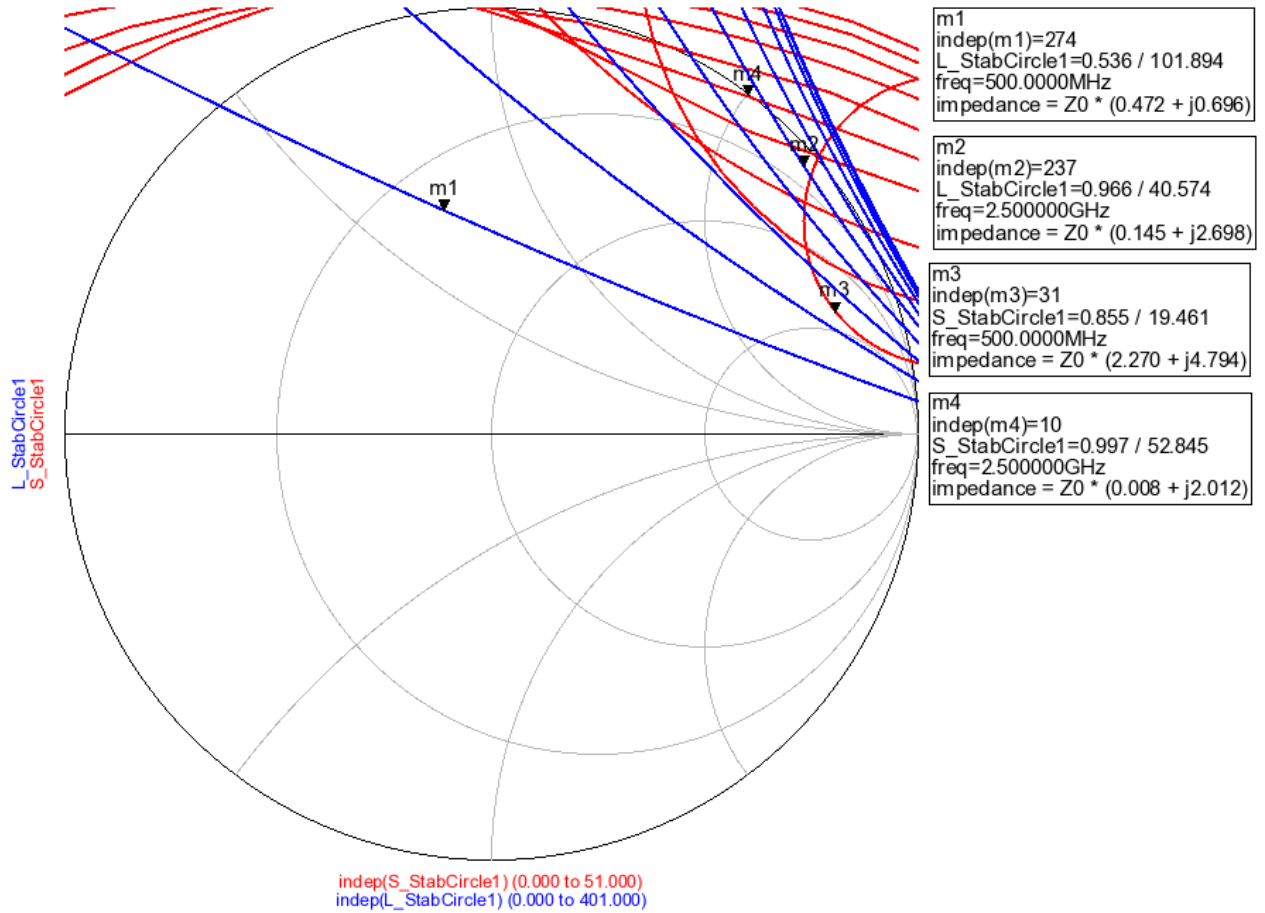
It is evident that the in-band response alone looks fairly unstable; especially if a  $\Gamma_{opt}$  input match is applied, which is fairly close to the source stability circle.

Adding some source inductance pushes the stability circles out and up to a certain amount of inductance, doesn't affect the noise figure and gain too much.

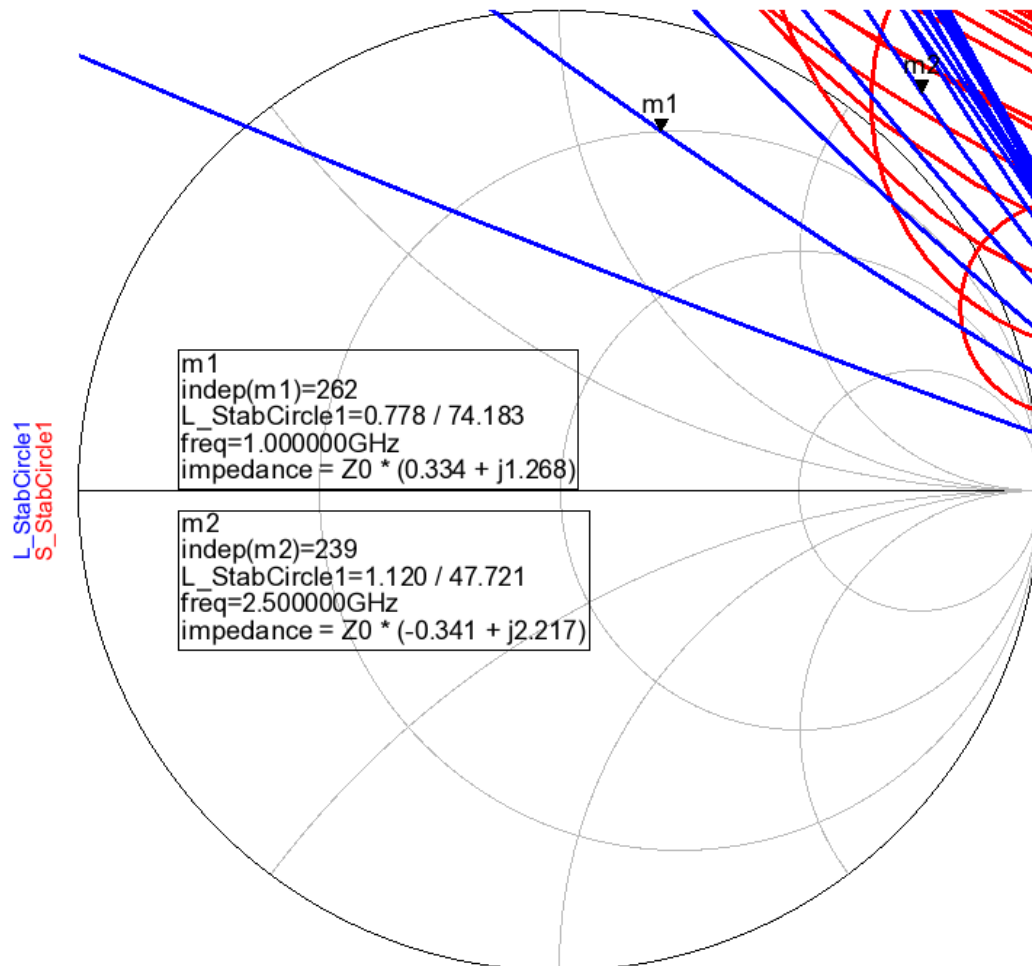
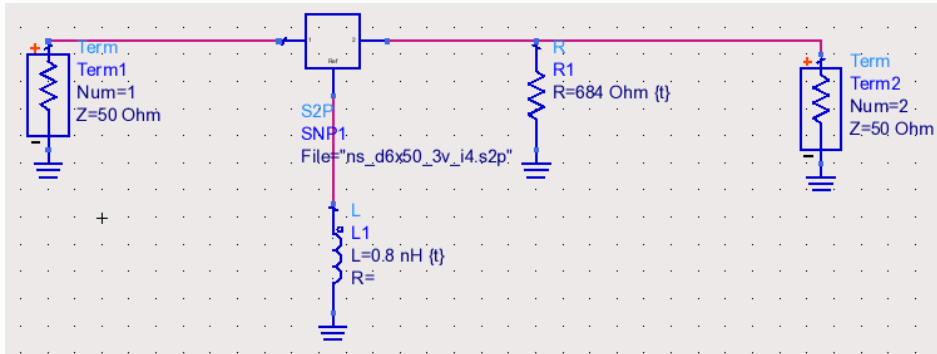


Now the circuit is almost unconditionally stable at 2.4 GHz and the minimum noise figure of the device is still achievable.

Now taking a wider look at stability, it's evident that there is more potential for instability at lower frequencies, and the device still isn't unconditionally stable at 2.4 GHz.

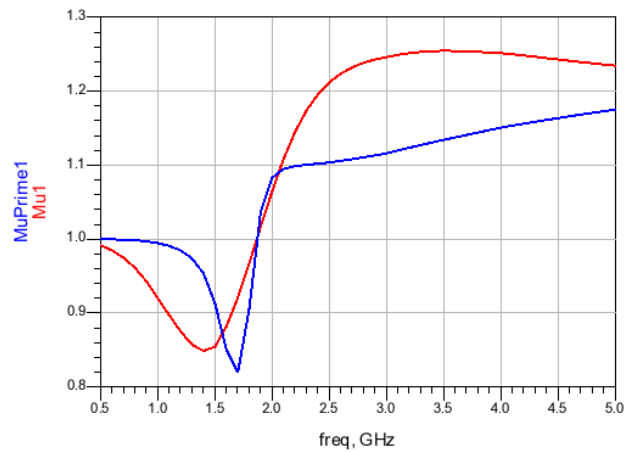
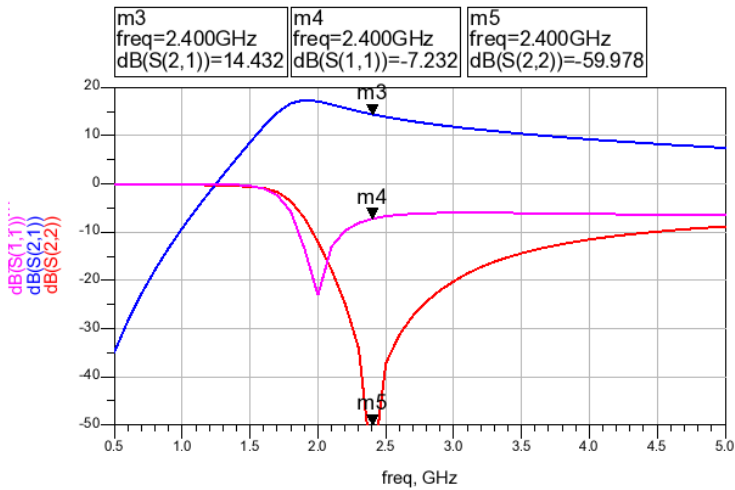
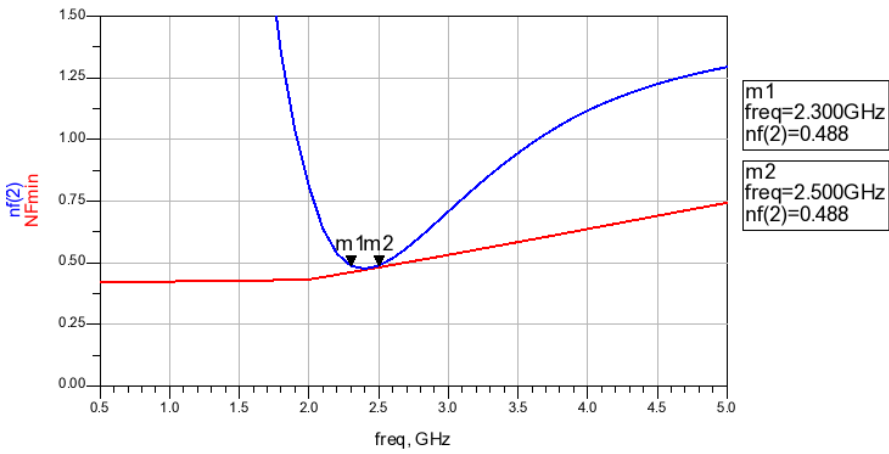
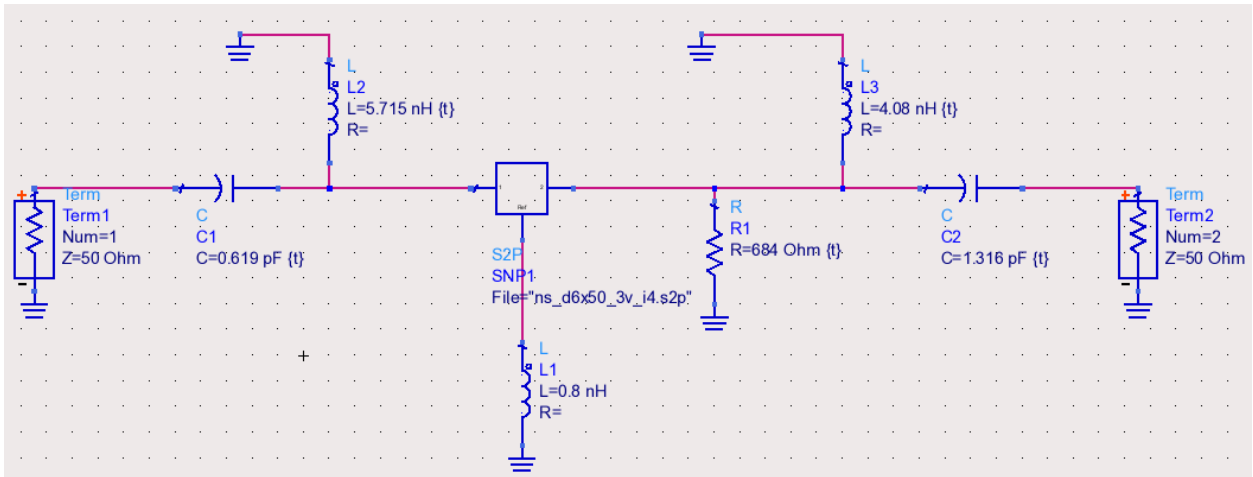


Adding a shunt resistor at the output to help further improve stability without impacting noise figure much:

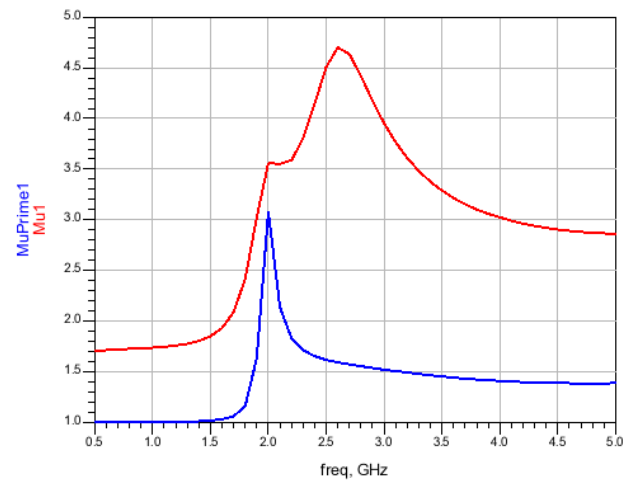
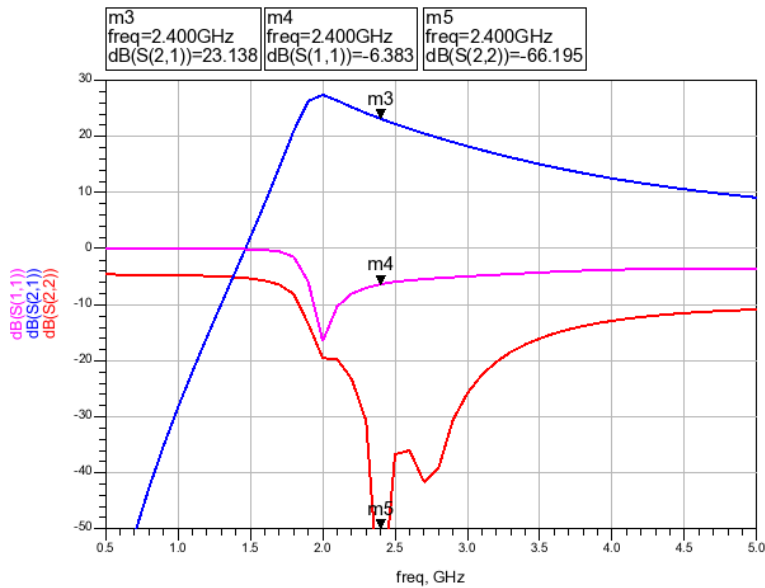
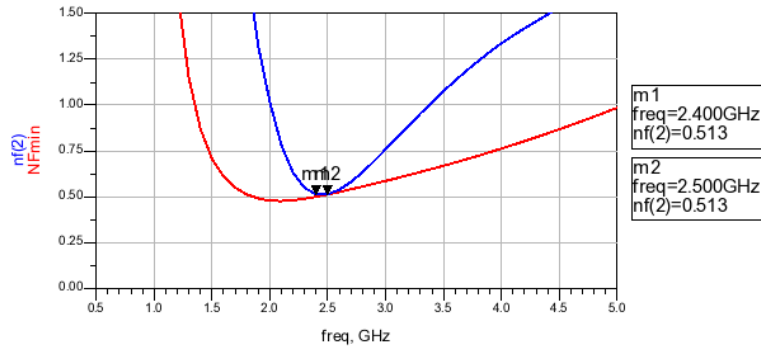
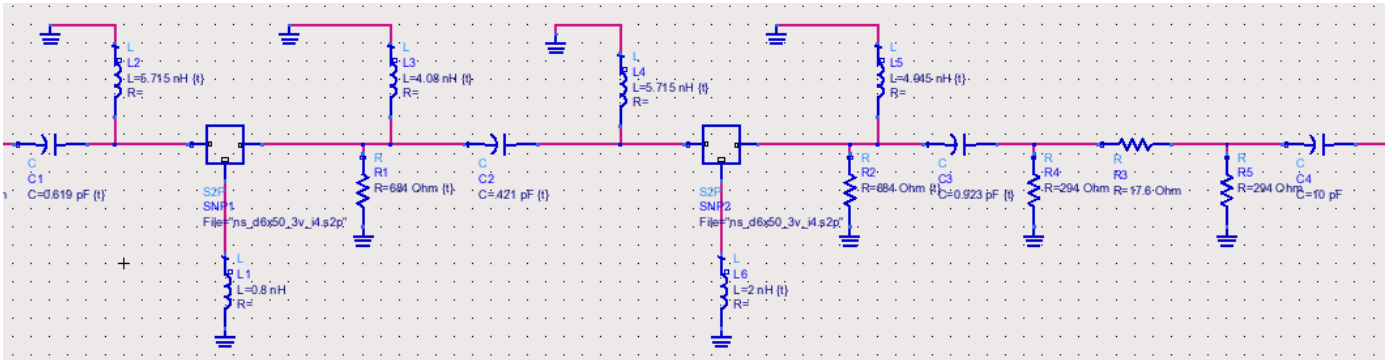


The device is now unconditionally stable at 2.4 GHz, and almost unconditionally stable elsewhere.

# Initial ideal matching network; matching to $\Gamma_{opt}$ and $S_{22}^*$

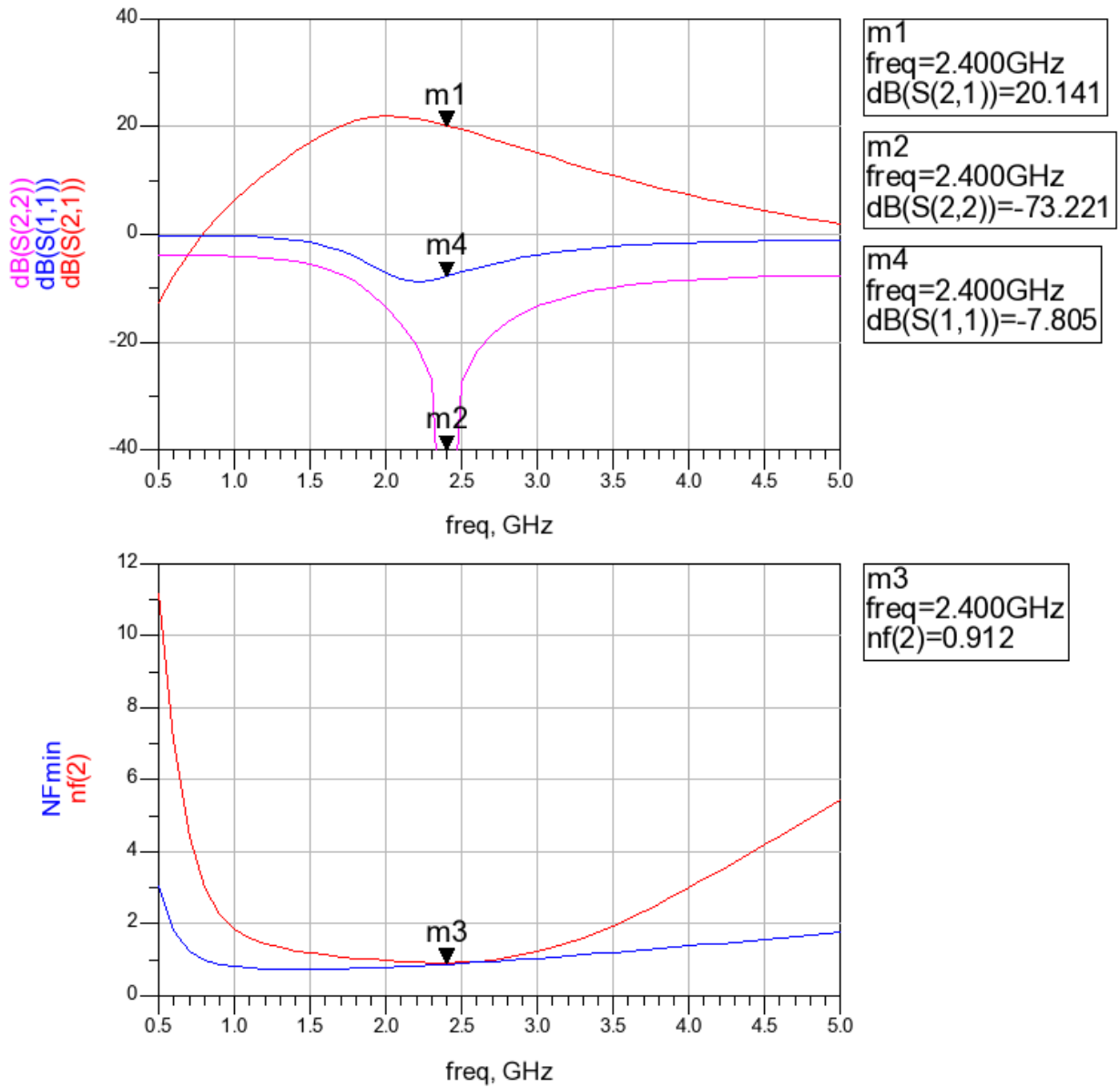


Cascading an almost identical second stage, but with increased source inductance for more stability:



The ideal simulation shows great noise figure and gain, and unconditional stability across all frequencies.

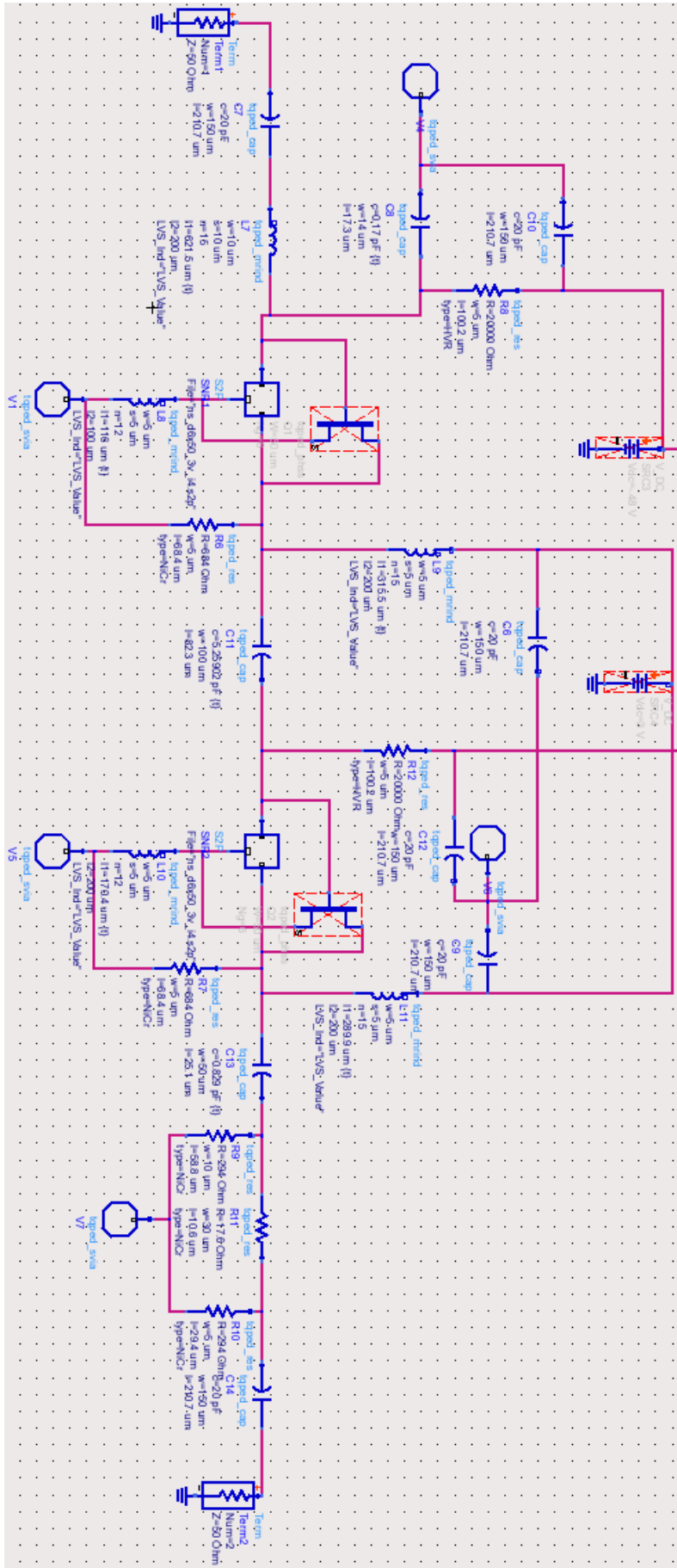
After converting all ideal elements to real Triquint :



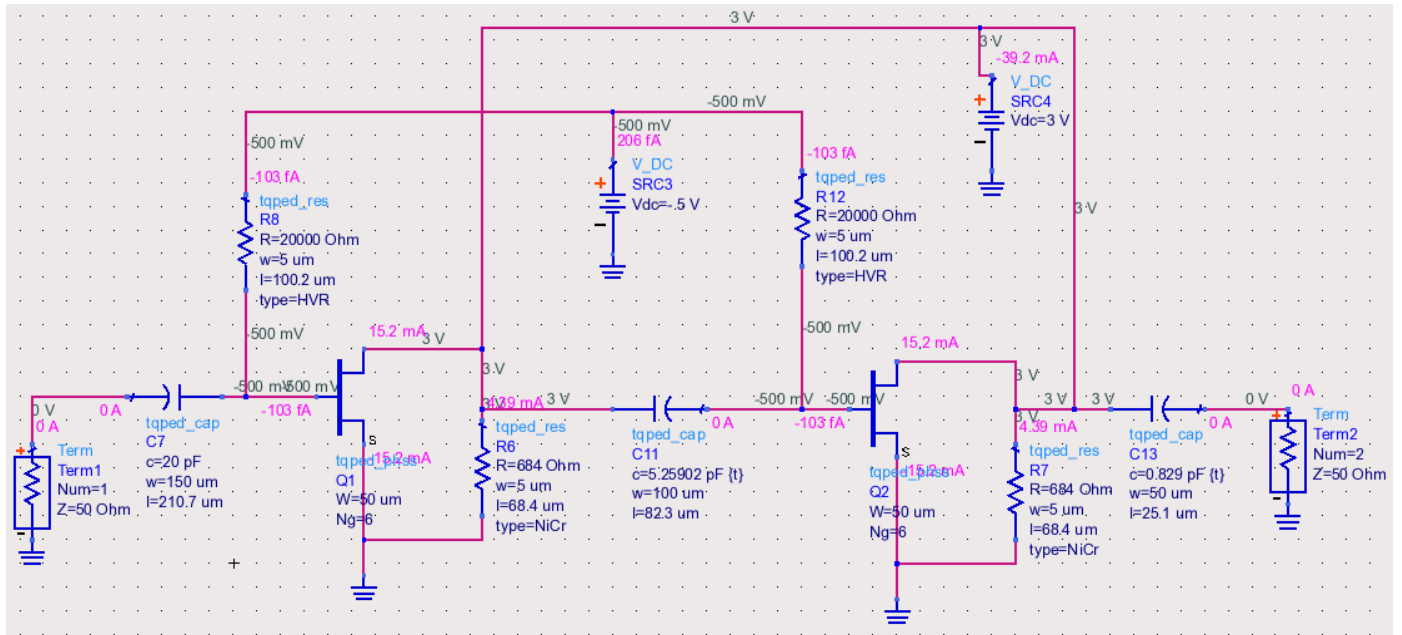
Using real elements increased the overall noise figure by 0.4 dB and lowered the gain by 3 dB. This is mainly due to the decent sized spiral inductors which have an appreciable inherent series resistance.



# Final Schematic



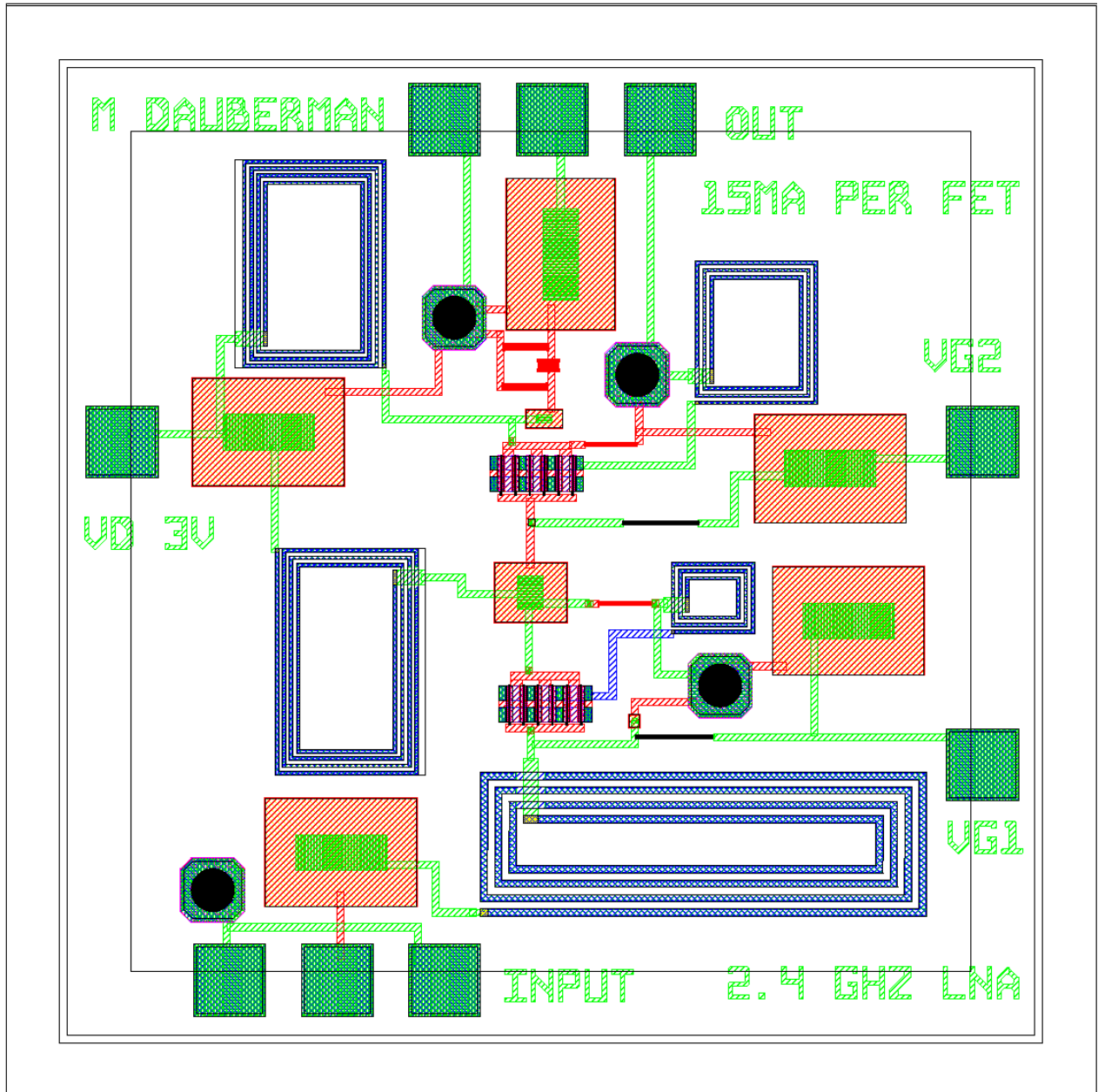
## Simple DC Bias Schematic



$V_D = 3\text{ V}$ ,  $I_D = 15\text{ mA}$  per FET

$V_G = -0.5\text{ V}$  for each FET

# LAYOUT



## TEST PLAN

To thoroughly test this Low noise amplifier, we will need a DC power supplies, a Network Analyzer, and a Noise Figure Analyzer.

1. Bias up the each Gate to -1.5 V to make sure both FETS are completely off before applying the Drain voltage
2. Bias up the Drain to 3V, note the current draw through the stabilization resistors,  $\sim 4.5$  mA per resistor, so with both FETS off the 3V supply should draw around 10mA.
3. Slowly increase the voltage on each Gate until both FETS draw 15mA each. The total 3V current draw should be around 40mA.
4. Run a full 2 port s-parameter sweep from 0.5 – 5GHz on the device and record.
5. Sweep the device on the Noise figure analyzer from 2 – 3 GHz.
6. If performance doesn't look to be as expected, check for oscillations on the spectrum analyzer.

## SUMMARY

This report summarized the design, simulation, and testing of a 2.4 GHz Low Noise Amplifier focusing on minimizing noise figure, while achieving wide-band stability. Although the device used shows the potential for a Noise figure below 0.5 dB, with this approach only 0.9 dB Noise Figure was achievable. This was mainly due to the large, lossy inductor used for the input match to  $\Gamma_{opt}$ . In order to avoid this loss, it may be possible to use some type of feedback circuit to move  $\Gamma_{opt}$  so that a smaller inductor can be used. However, this basic design should be very robust and meet the requirements for a wide range of applications at this frequency range.

# **Doherty Power Amplifier Design**

By

**Ken Mcknight**

Microwave Monolithic Integrated Circuit (MMIC) Course  
Johns Hopkins University  
Fall 2009

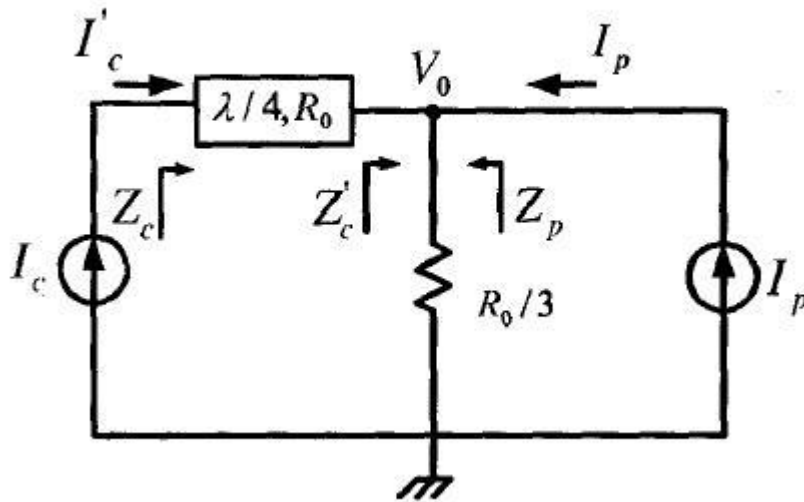
## **Abstract**

A Doherty Amplifier operating at 2.4 GHz and a supply voltage of 3-3.6V is described in this paper. The amplifier was designed in the Triquet GaAs process using the ADS software package. Simulation results show high output power and good power gain linearity up to the 3dB compression point. The results also show good 2<sup>nd</sup> and 3<sup>rd</sup> harmonic suppression. A physical layout of the design is also included in this paper.

## **Introduction**

Doherty amplifiers have demonstrated high efficiency over a wide output power range. These structures can also be used to meet high Linearity specifications over a wide output power range. It is difficult to simultaneously get high efficiency, high output power and good linearity in the same design. This design focuses on high output power and good linearity over an extended output power range. The Doherty amplifier consists of carrier and peaking amplifiers connected by a quarter-wave transmission line. The carrier amplifier is typically biased class A or class A-B and the peaking amplifier is typically biased at class C so that the peaking amplifier turns on at the power on just before the carrier amplifier starts to go into compression. The current contribution from the peaking amplifier reducing the effective load impedance of the carrier amplifier and drawing more current from the the device.

### Operational Diagram of the Doherty Amplifier



The simulation results show close to a 4dBm improvement in output power and more than 30dB suppression of 2<sup>nd</sup> and 3<sup>rd</sup> order harmonics.

### Design Approach

The Doherty amplifier was implemented using a class A structure and class C joined by the lumped element equivalent of a quarter-wave transmission line. The two amplifiers were driven from a Wilkinson power splitter with a 3dB attenuator preceding the class C amplifier.

The preliminary specifications for the design were as follows.



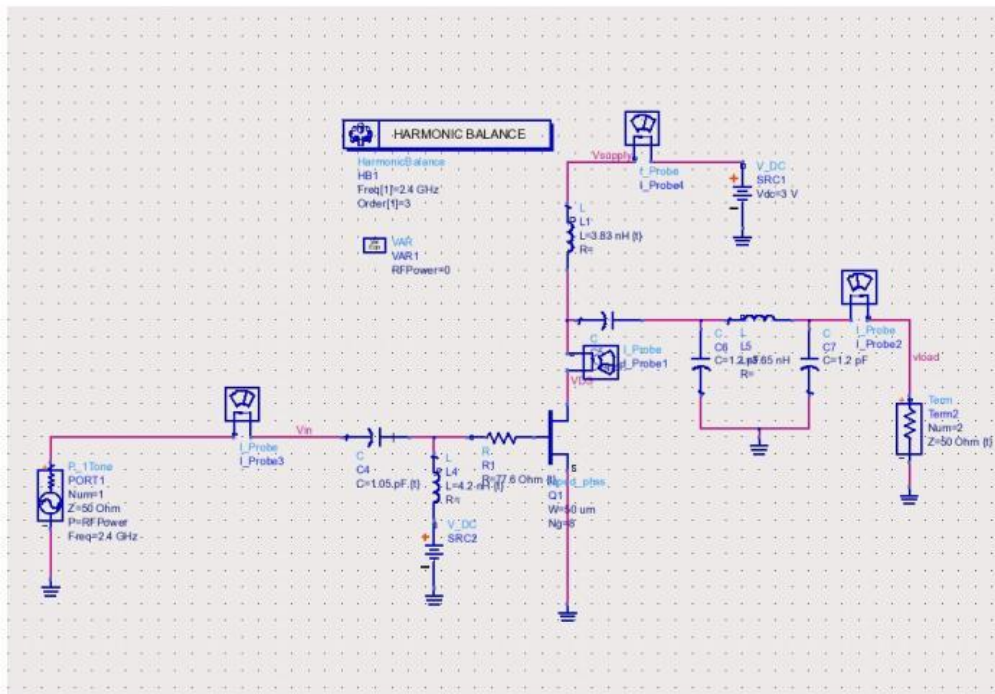
Frequency	2.3GHz to 2.5GHz
PAE	> 50%
Gain	20dB
Pout	> 20dBm
VSWR	< 1.5:1
Vsupply	3V to 3.6V

During the design process, I realized that I could not achieve output power in excess of 20dBm and achieve a power gain of 20dB with a single-stage amplifier. A cascade structure would provide 20dB of gain but not over 20dBm of power with a 3V supply. I opted to go with lower gain and lower efficiency numbers while achieving higher output power. Inserting a driver amplifier will compensate for the lower gain and the lower efficiency performance is a design tradeoff. The final performance is as follows.

Frequency	2.3GHz to 2.5GHz
PAE	43.6%
Gain	10dB
Pout	25dBm
VSWR	< 1.5:1
Vsupply	3V to 3.6V

The class C amplifier topology is standard. The device is biased in the pinch off region and conducts as the input signal increases. The pull up inductor is used resonate out the drain to bulk capacitance and to provide current to the load via a dc blocking cap. Since the operation of the class C amplifier is non-linear, I needed a network to filter out the higher order harmonics of the output voltage. I used the low pass quarter-wave equivalent network for this purpose. I could tune the characteristic impedance of this network for optimum power or efficiency for the class C amplifier.

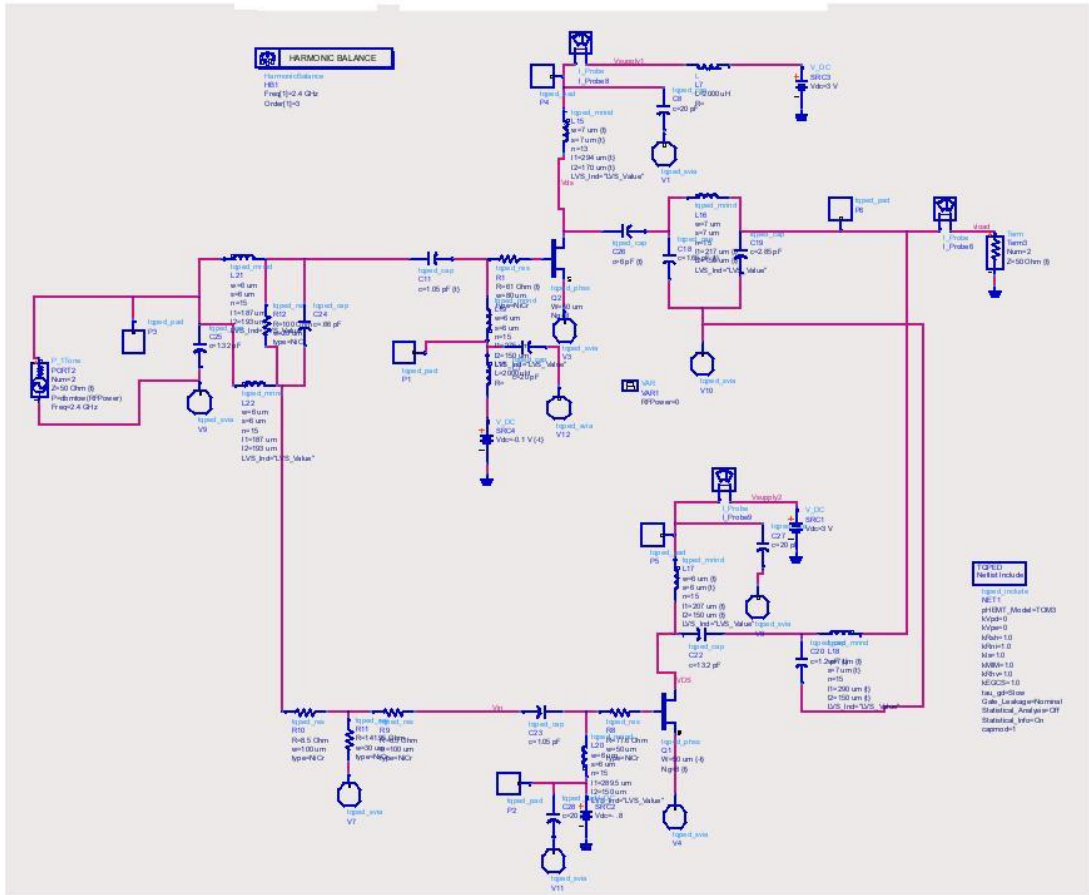
### Class C Amplifier Schematic



I used a similar approach for the class A amplifier. Initially, I used the pull up inductor to resonate out the drain to bulk capacitance. I connected the quarter-wave equivalent directly to the pull up and tuned the characteristic impedance such that the parallel equivalent of  $R_{ds}$  and the network impedance equaled the Cripps resistance. I later included the dc blocking cap in the class A amplifier because I noticed that I could get more power out of the amplifier as I drove it harder. Basically I left the class A operating regime as I got closer to saturation for the Doherty Amplifier.

The Doherty Amplifier schematic shows the class C amplifier at the bottom and the class A amplifier at the top. Both structures are the same but biased in different regimes. I've also included an attenuator before the class C amplifier in order to control the turn on voltage with respect to the class A structure. This "turn on" point determines the overall linearity of the output versus input power curve.

# Doherty Amplifier Schematic

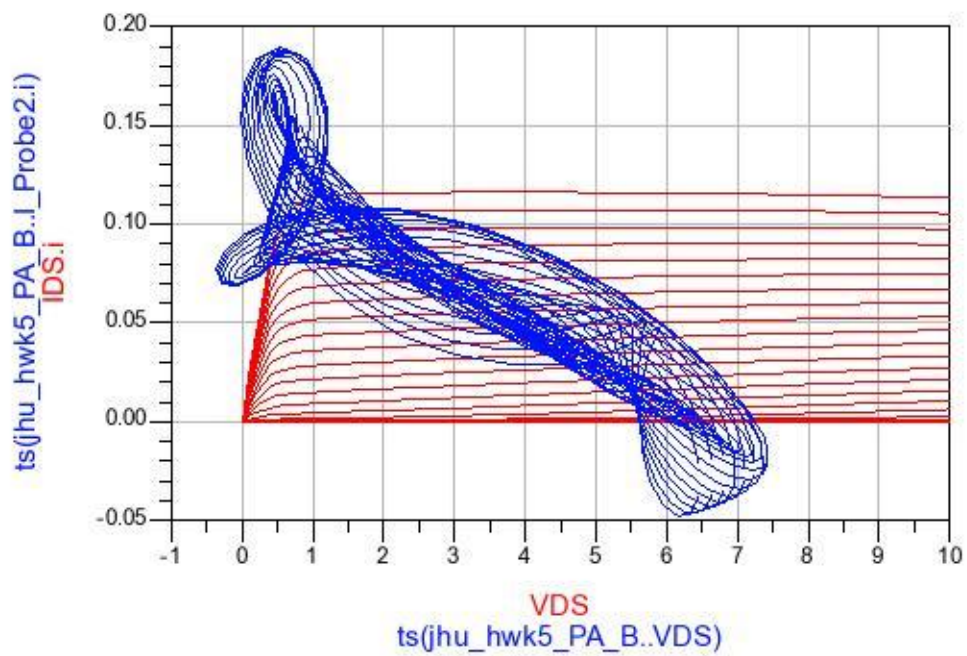


# Simulations

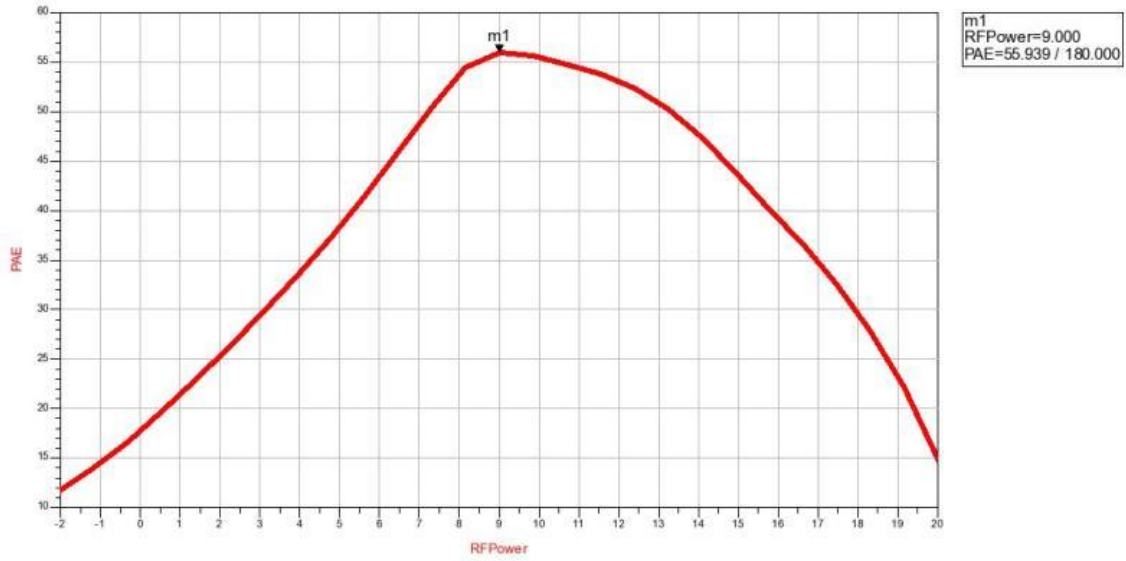
## Class A Amplifier

DC Simulations:

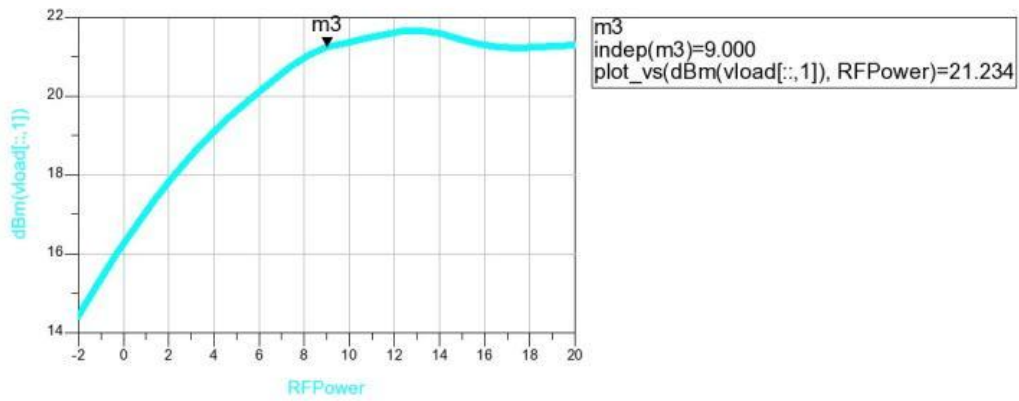
**Dynamic Load Line for Class A Amplifier**



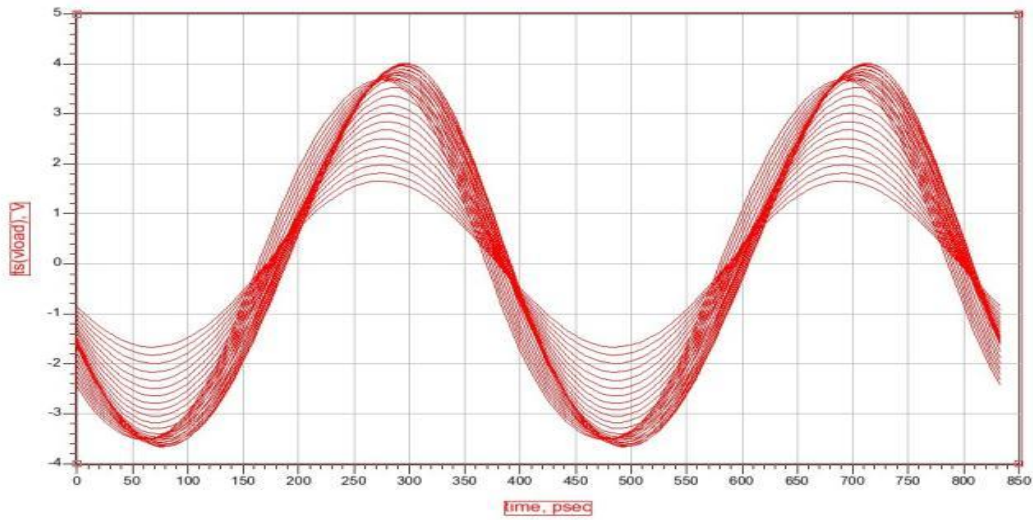
### PAE for Class A Amplifier



### Pout vs Pin for Class A Amplifier

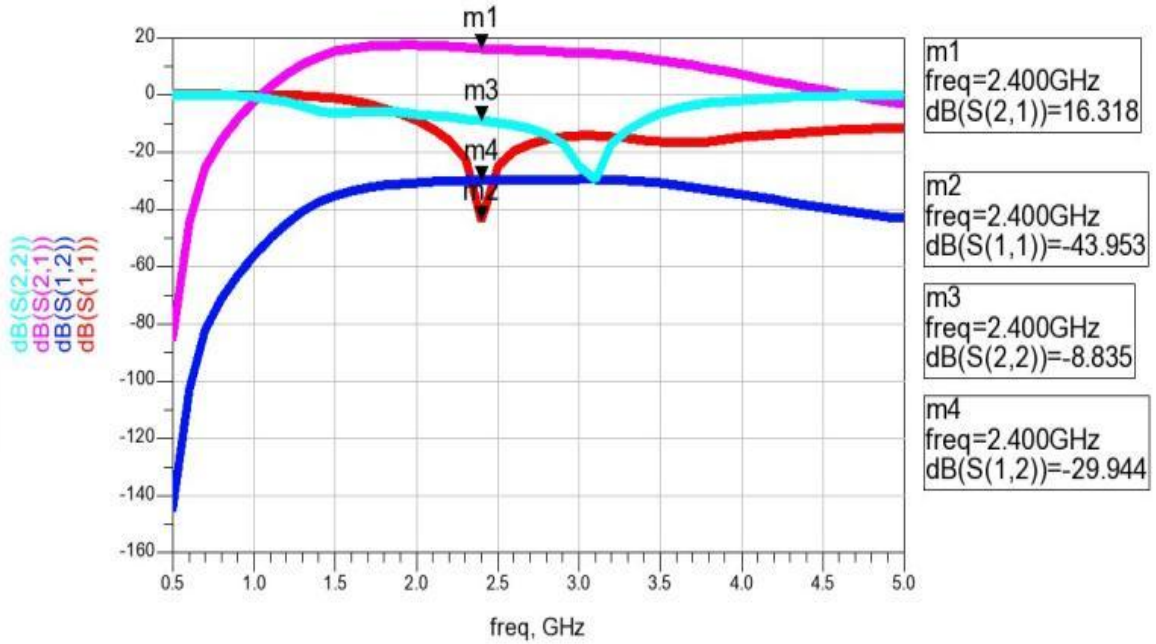


### Vload for the Class A Amplifier



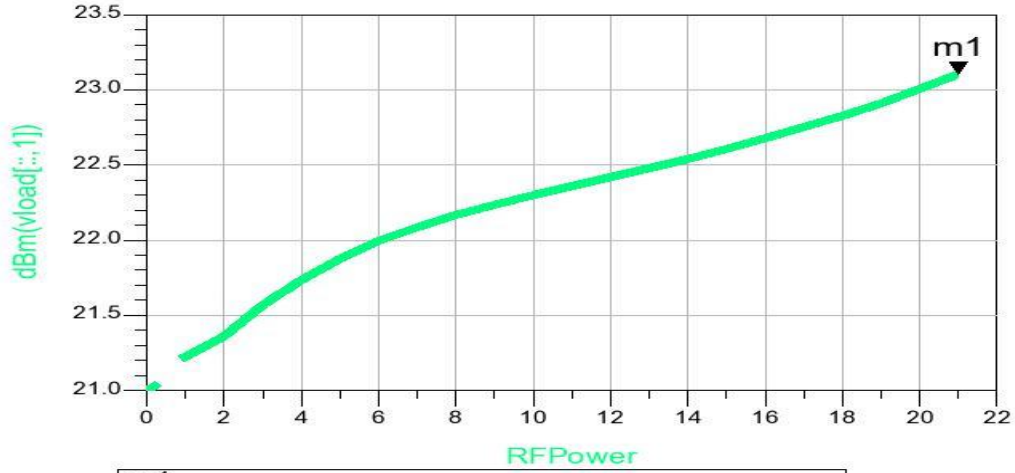
### AC Simulations:

#### S Parameters for the Class A Amplifier



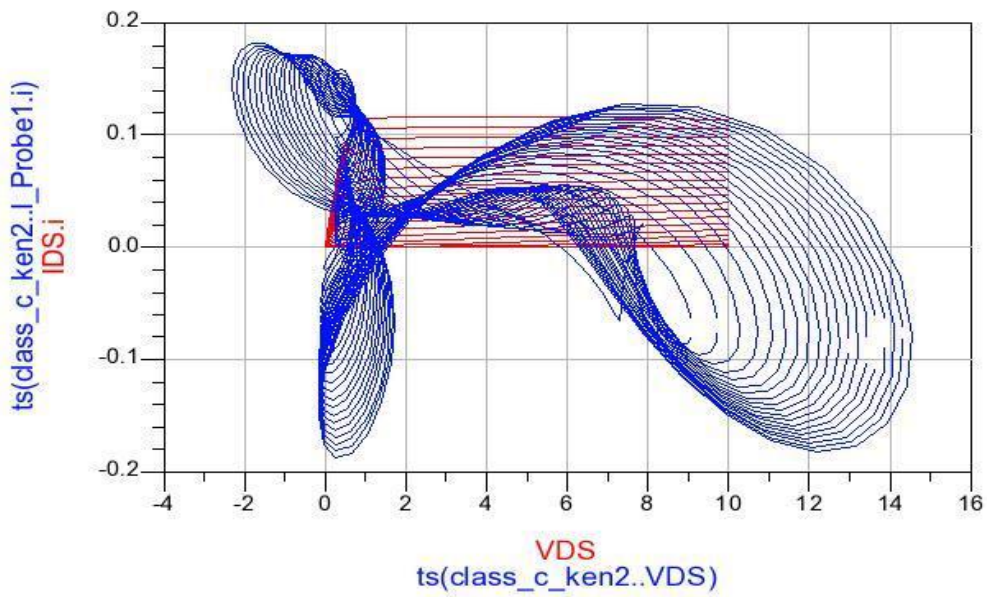
# Class C Amplifier

### Pout vs Pin for Class C Amplifier



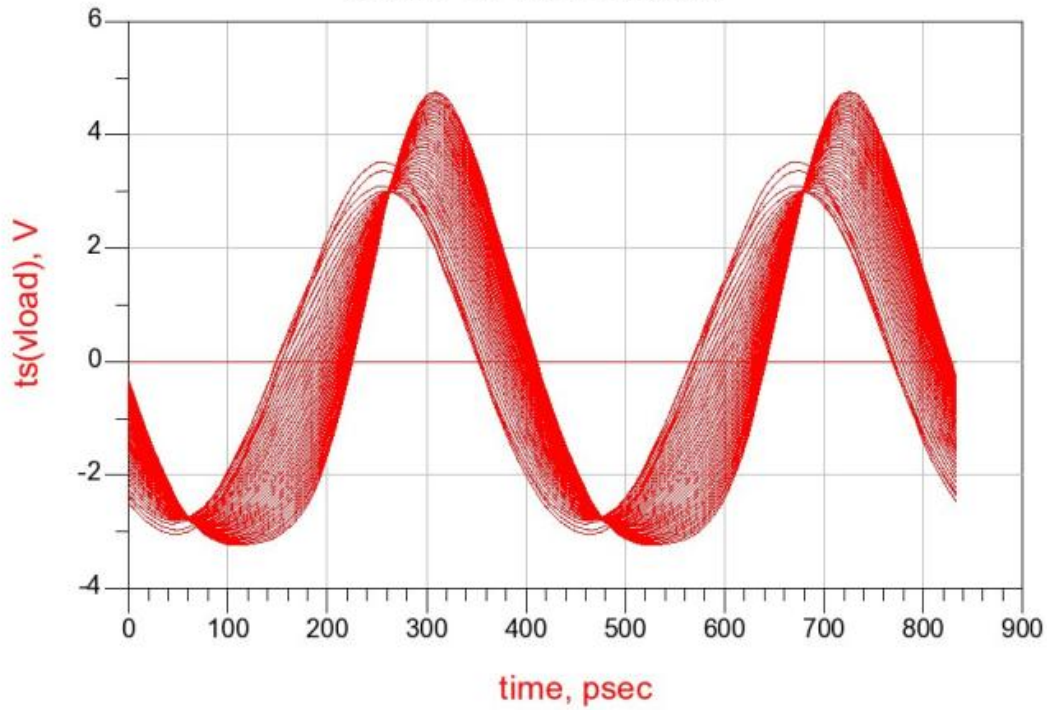
```
m1  
indep(m1)=21.000  
plot_vs(dBm(vload[::,1]), RFPower)=23.102
```

### Dynamic Load Line for Class C Amplifier



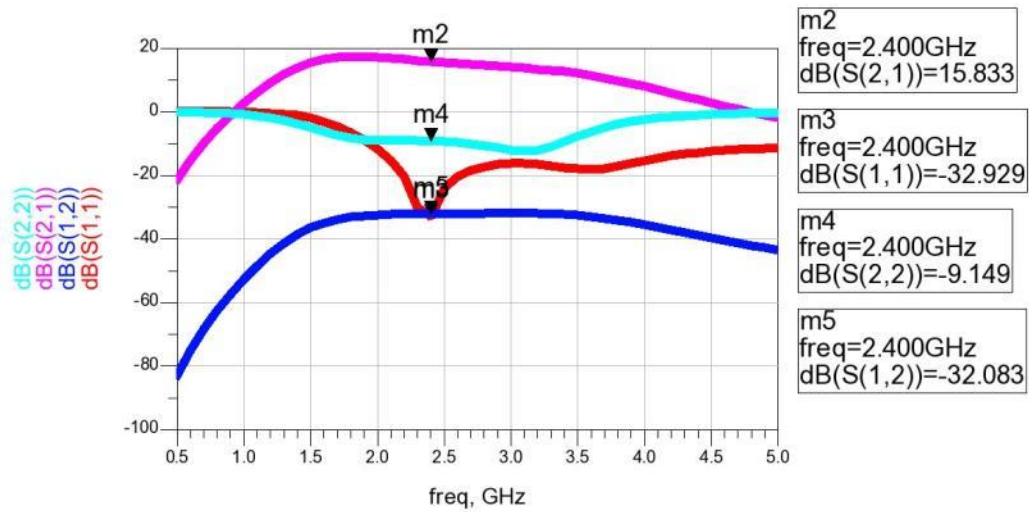


### Vload for the Class C Amplifier



### AC Simulations

#### S Parameter for Class C Amplifier @ Vgs=0V

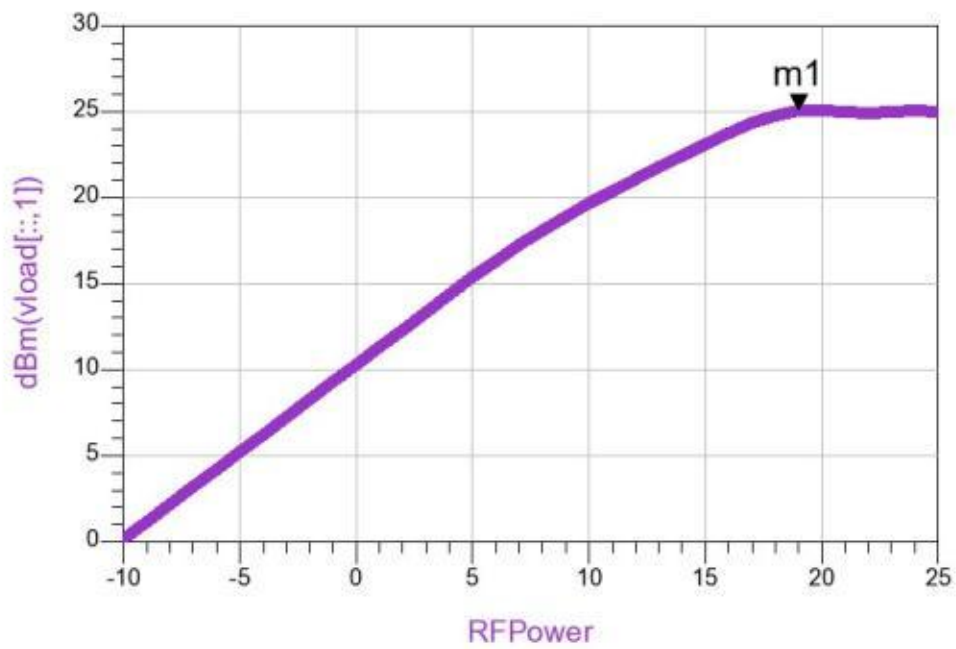


## Doherty Amplifier

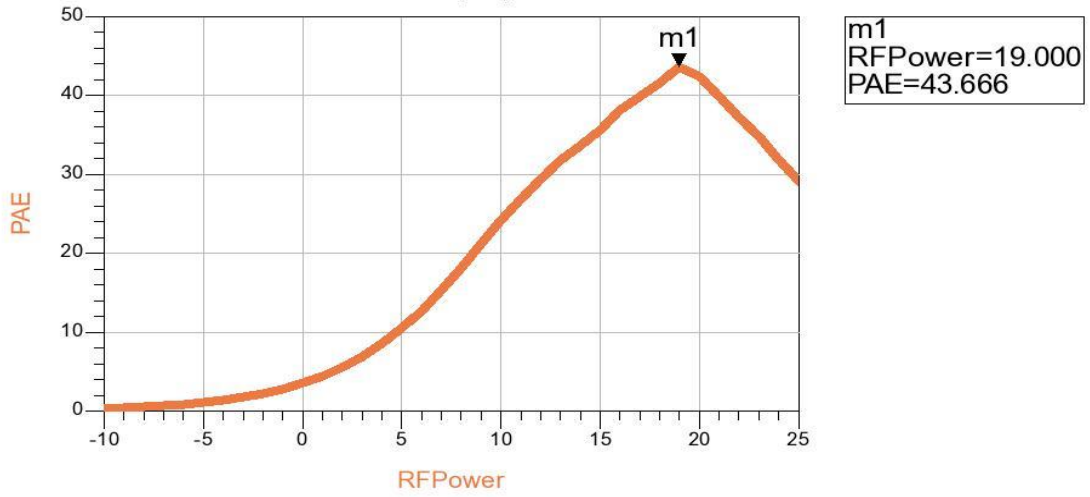
DC Simulations:

### **Pout vs Pin for the Doherty Amplifier**

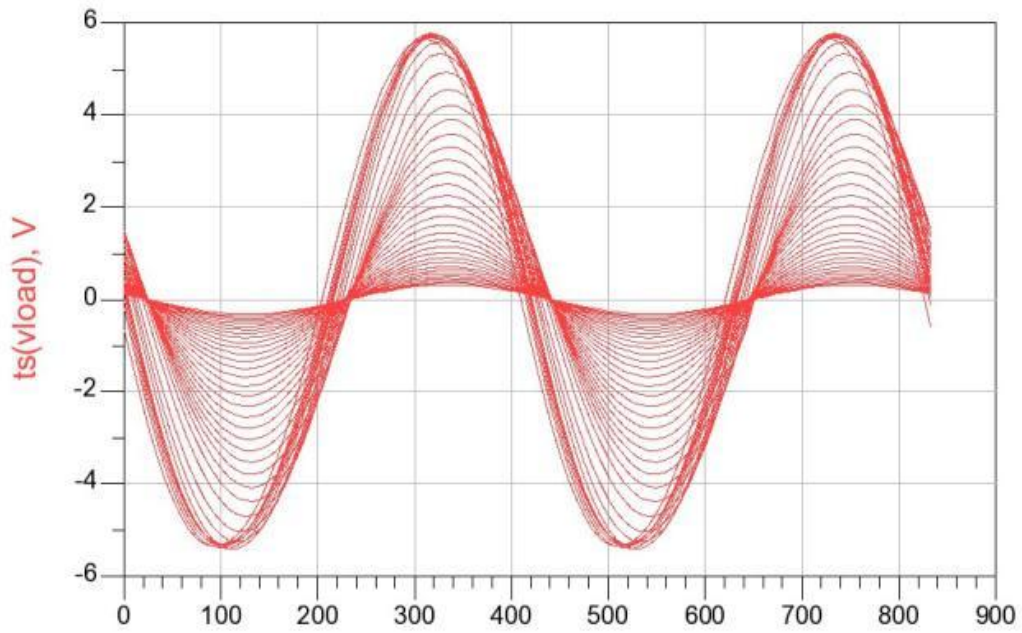
```
m1  
indep(m1)=19.000  
plot_vs(dBm(vload[:,1]), RFPower)=25.021
```



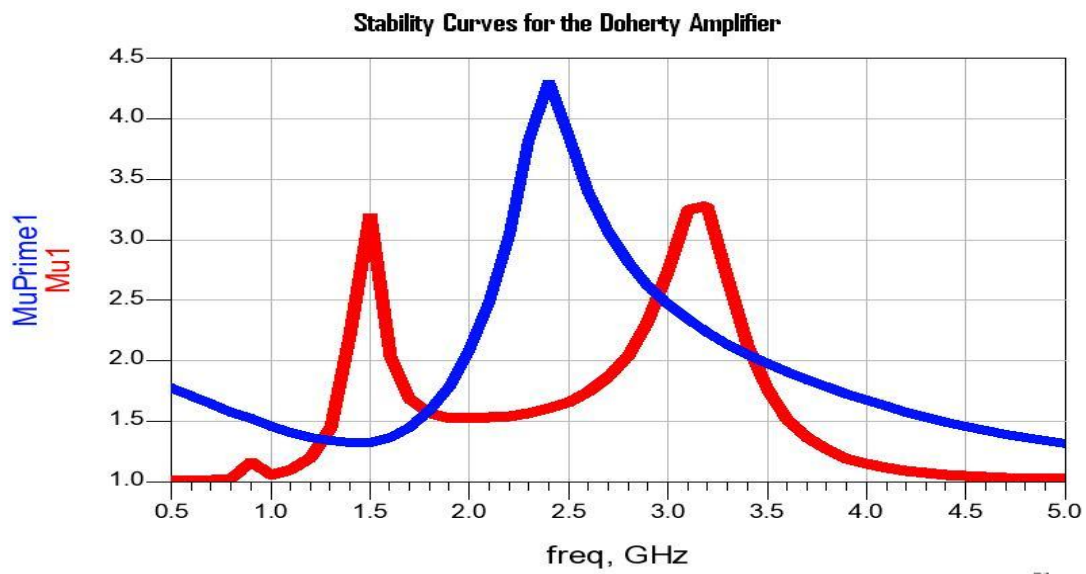
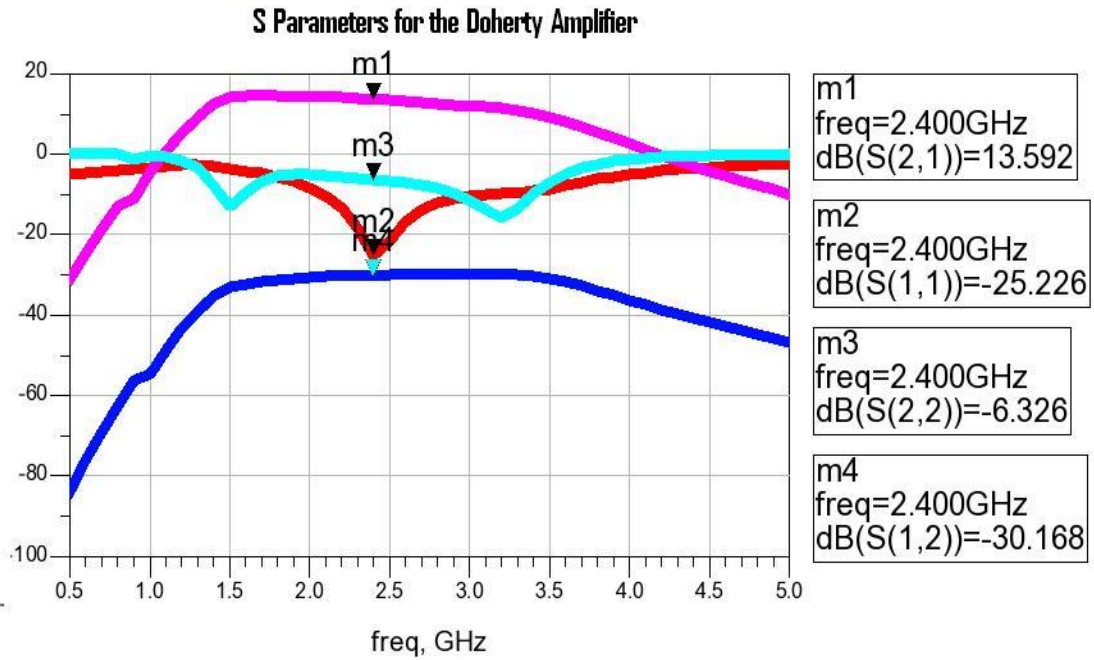
PAE for the Doherty Amplifier



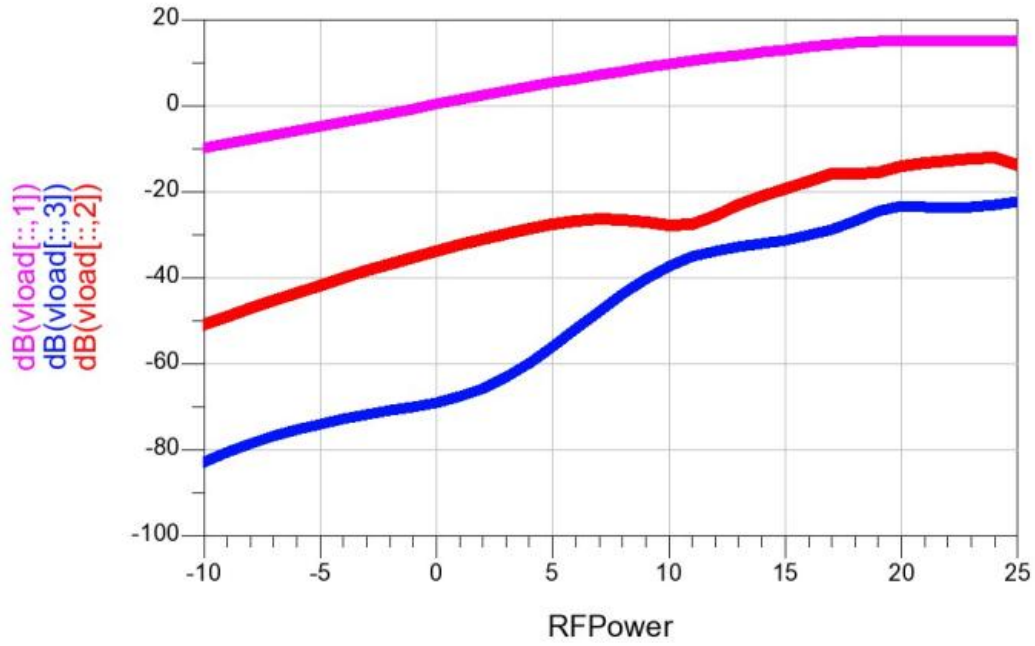
Vload for the Doherty Amplifier



## AC Simulations:

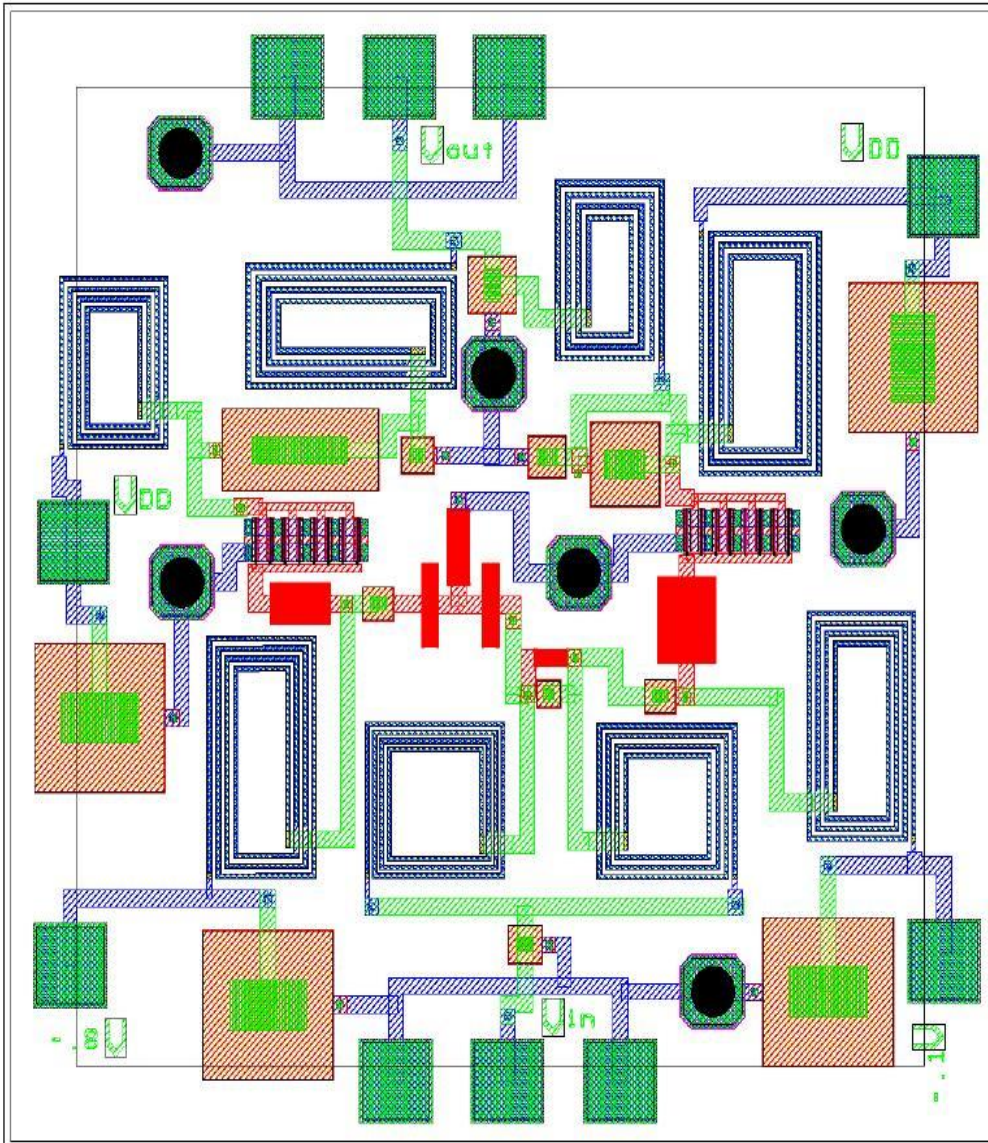


### The 1st, 2nd and 3rd Harmonics of Vload for the Doherty Amplifier



Layout:

**Final Layout for Doherty Amplifier**



## **Test Plan:**

1. Power Out versus Power In measurements.
2. S-parameter Measurements
3. Measure 2<sup>nd</sup> and 3<sup>rd</sup> Harmonics
4. Power Out versus V<sub>supply</sub>.

### Equipment Needed.

1. 8510 Network Analyzer
2. Probe Station + Probes
3. Dc Power Supply ( 2 Supply probes, 2 gate bias probes)
4. Spectrum Analyzer
5. Current meter
6. High Frequency Source.

## **Summary**

Tradeoffs were made in the design of the power amplifier.

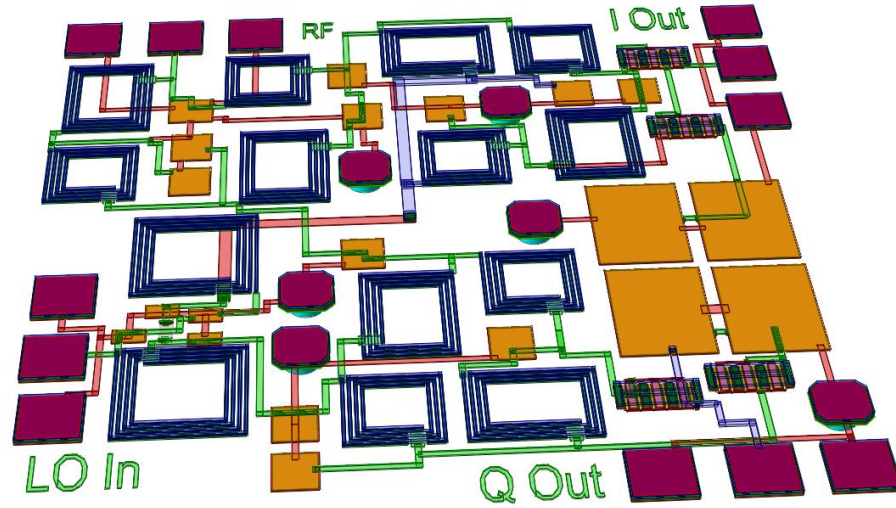
It is extremely hard to get both high efficiency and high output power. The Doherty amplifier is a good structure to use when high power and high linearity are the design goals. Even though the Doherty structure is 70 years old, it still has use in today's MMIC design.





# IQ Demodulator

David C. Nelson  
14 December 2009



## **ABSTRACT**

The IQ Demodulator is an RF down-converter that converts an RF input into two IF outputs with a 90 degree phase difference. The demodulator has two inputs. The RF input ranges from 2.4 to 2.5 GHz, and a fixed LO of 2.45 GHz is used. The IF outputs range from 1 to 50 MHz. The phase shift in the RF input is implemented using a hybrid coupler. The down-conversion is performed by two single-balanced mixers. The LO input is split between the two mixers using a Wilkinson Divider. Using an RF input power of 10 dBm and an LO input power of 15 dBm, a conversion loss of 10 to 14 dB was achieved at the IF output. The I and Q outputs have a phase difference of between 125 and 133 degrees.

## **INTRODUCTION**

An IQ demodulator splits the received signal into two paths. A phase shift of  $90^\circ$  is applied to one signal path while the other is passed with no phase shift, essentially performing a Hilbert transform on the "Q" path. A down-conversion is performed on each path.

In a receiver, if the received signal were

$$A\cos(\omega_1 t)$$

In order to sample this signal directly the Nyquist theorem must be adhered to because the signal has both positive and negative frequency content. The minimum sampling rate would thus be limited to:

$$f_s \geq 2f_1$$

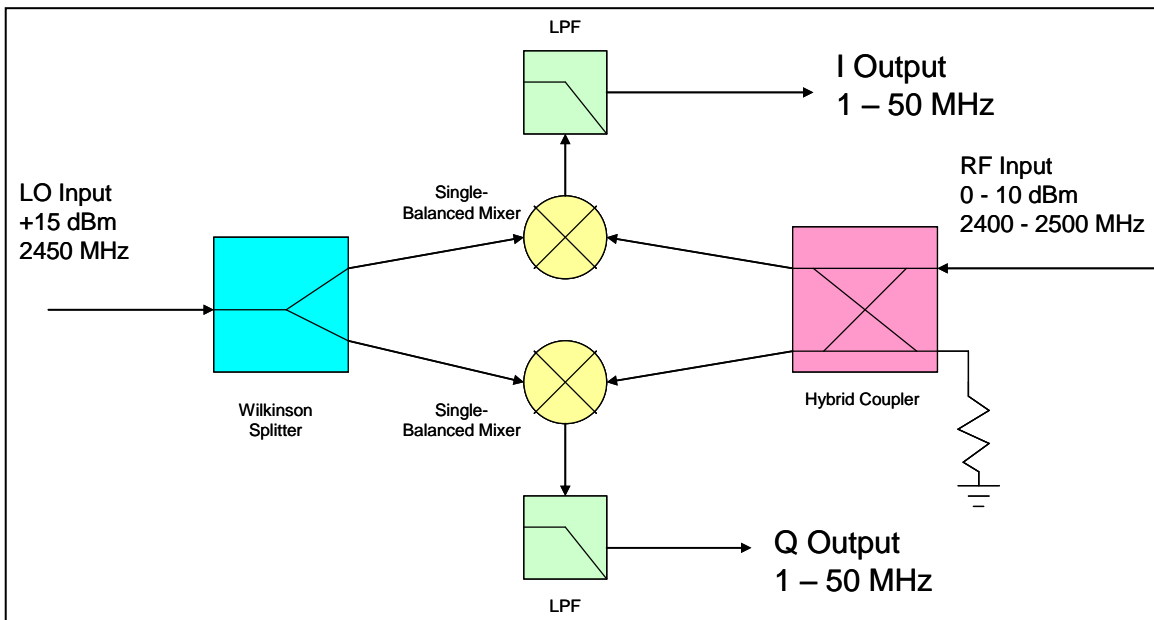
However, by summing the I and Q paths of the IQ Demodulator the received signal becomes:

$$A\cos(\omega_2 t) + jA\sin(\omega_2 t) = A\exp(j\omega_2 t)$$

Where  $\omega_1 > \omega_2$

This signal has only positive frequency content and sub-sampling can be performed without harmful aliasing.

This IQ demodulator was implemented using a hybrid coupler, a Wilkinson divider, and two single-balanced mixers. A block diagram is shown in Figure 1.



**Figure 1: IQ Demodulator Block Diagram**

## Design Approach

This design was not given a lot of specifications, so the designer derived some self-imposed goals.

Specifications	
RF Frequency	2.4 – 2.5 GHz
LO Frequency	2.3 – 2.6 GHz
LO Power	+7 dBm
IF Frequency	1 – 50 MHz
Goals	
Conversion Loss	About 10 dB
IQ Phase Difference	90 +/- 5 degrees
Input Return Loss	15 dB

The following procedure was used to design the IQ demodulator:

- Design and Simulate Sub-Circuits
  - Hybrid Coupler
  - Wilkinson Divider
  - Single-Balanced-Mixer
- Integrate Sub-Circuits
- Simulate IQ Demodulator
- Iterate as needed

The hybrid coupler designed in Homework 1 was re-tuned and used in the I-Q Demodulator. The coupler was used for two purposes. The first was to split the RF input into the I and Q paths of the demodulator and provide the Q path with a 90 degree phase shift. The coupler was also used as the balun in the single-balanced mixers.

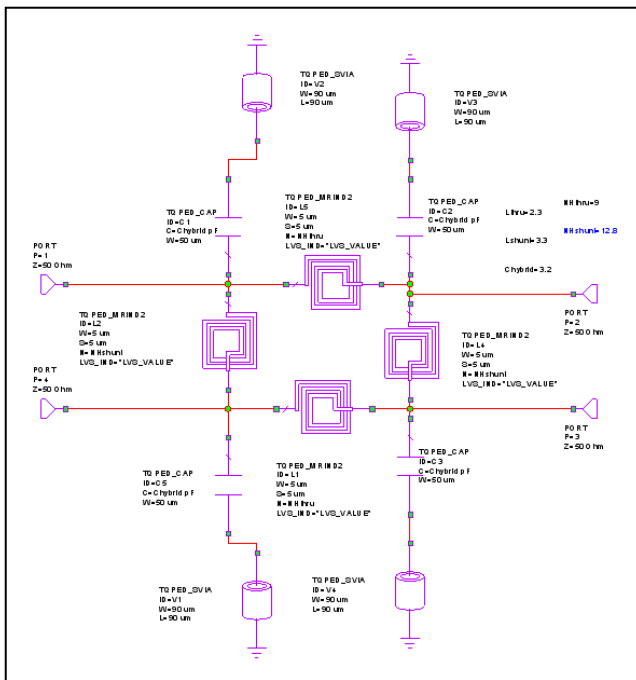


Figure 2: Hybrid Coupler Schematic

It can be seen in Figure 2 that pi networks were used for the quarter-wave lumped-element equivalent circuits. The pi networks were chosen in order to minimize the number of inductors in the design. The coupler was designed for a center frequency of 2.4 GHz.

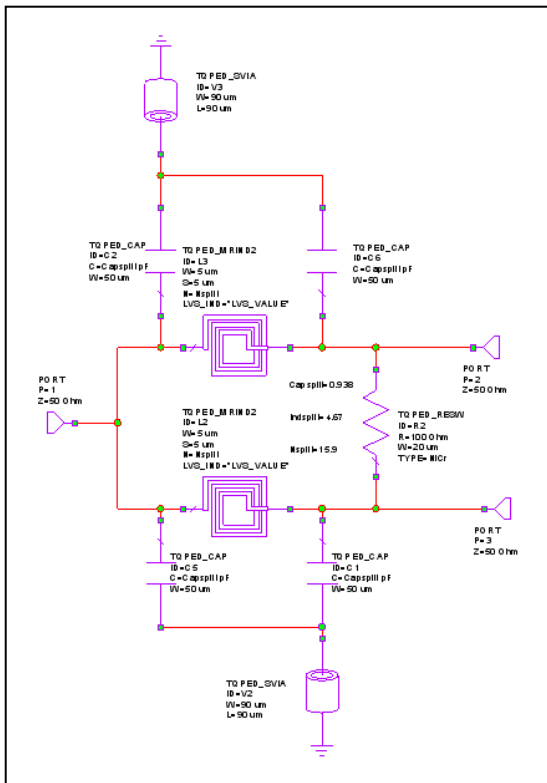


Figure 3: Wilkinson Splitter Schematic

The splitter shown in Figure 3 was designed for a center frequency of 2.4 GHz. Pi networks were used for the quarter wave lumped-element equivalent circuits to minimize the number of inductors in the design.

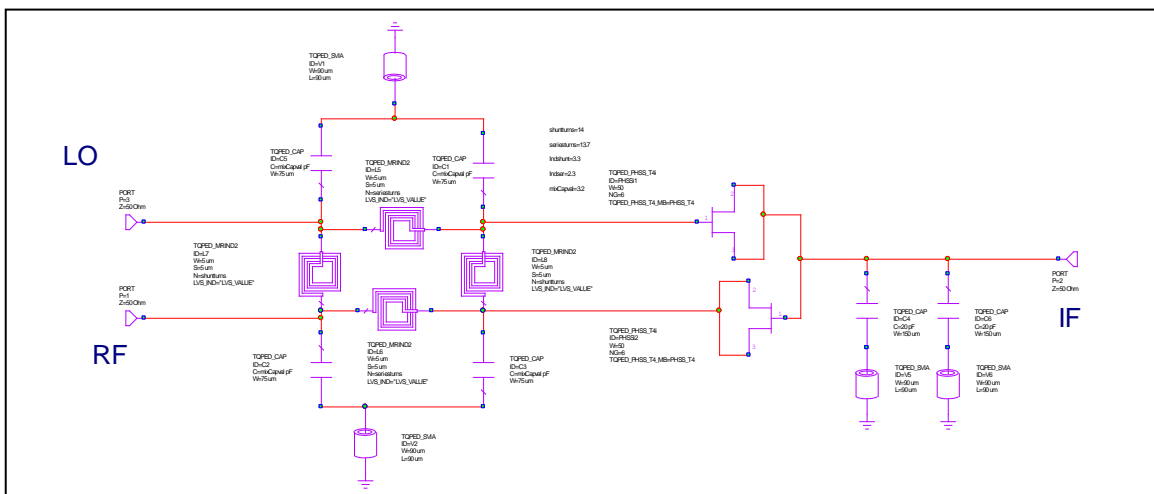
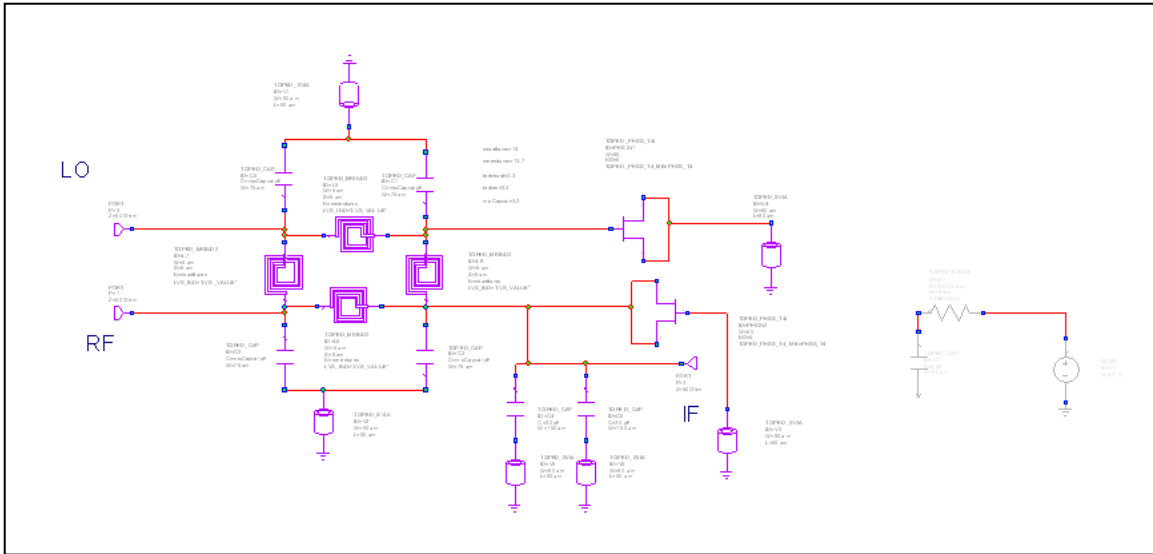


Figure 4: Single-Balanced Mixer

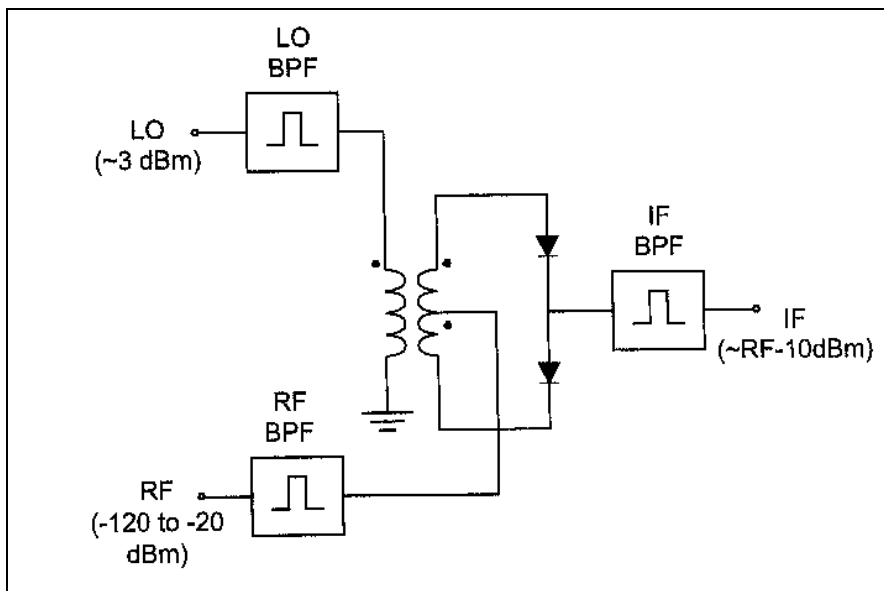
A rat-race coupler would have provided better isolation, but a hybrid coupler was used in the SBM design because it was already being used elsewhere in the modulator. The rat-race coupler would have added another inductor, which probably would not have fit on the 60x60 mil substrate that was used.

The topology used for this mixer is somewhat different than what was suggested in class.



**Figure 5: Mixer topology suggested in class**

It can be seen in Figure 4 that rather than connecting the diodes to ground the diodes were connected in series between the two output ports of the coupler. This topology was derived from McClaning's design in *Radio Receiver Design* Shown in Figure 6.

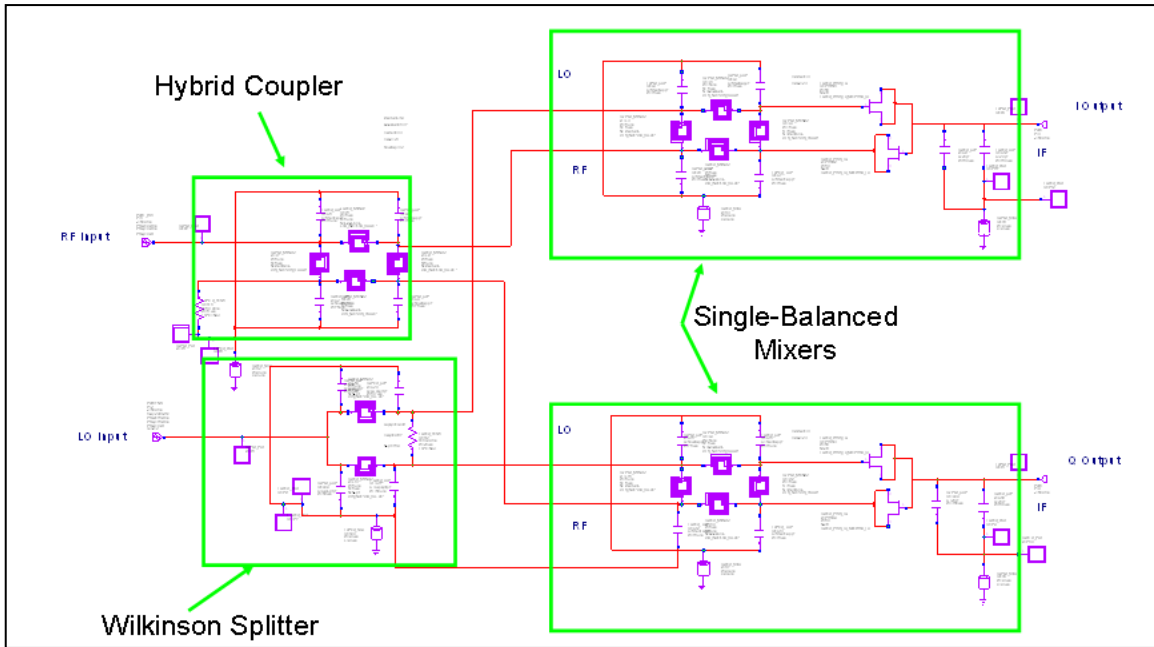


**Figure 6: Single-balanced mixer from *Radio Receiver Design*<sup>1</sup>**

<sup>1</sup> McClaning, Kevin and Tom Vito. *Radio Receiver Design*. Noble Publishing Corporation, Atlanta GA. 2000.

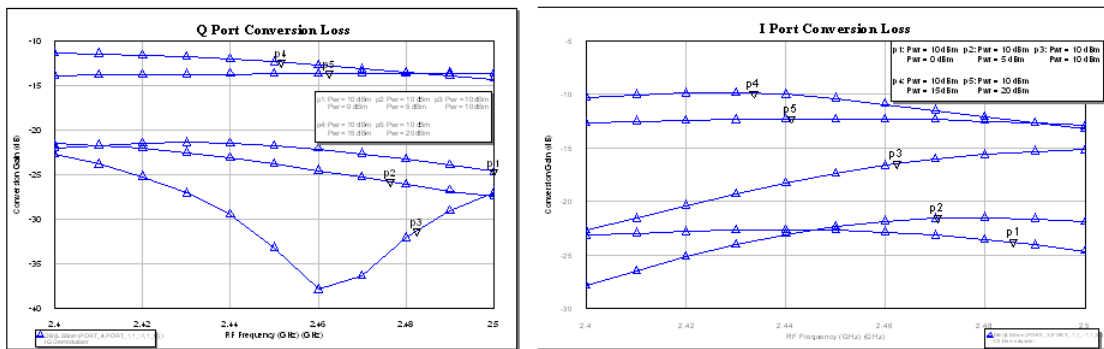
Changing the design from the topology shown in Figure 5 to the topology shown in Figure 4 resulted in a 5 dB improvement in conversion loss with the same RF input powers.

Combining the three sub-circuits resulted in the IQ demodulator schematic shown in Figure 7



**Figure 7: IQ Demodulator Schematic**

The demodulator was simulated with the RF frequency swept from 2.4 to 2.5 GHz and a fixed LO of 2.45 GHz. The RF Power was set to 10 dBm and the LO power was stepped from 0 to 20 dBm to determine the necessary LO power.



**Figure 8: Conversion loss for different LO input powers**

Figure 8 shows that with an LO input power of 7 dBm that was specified initially the demodulator would not be able to achieve the goal of 10 dB conversion loss. Using the ideal LO input power of 15 dBm the demodulator can come close to meeting the goal of 10 dB conversion loss.

With a fixed LO power of 15 dBm the RF power was then stepped from 0 to 10 dBm to see what effect that would have on the conversion loss.

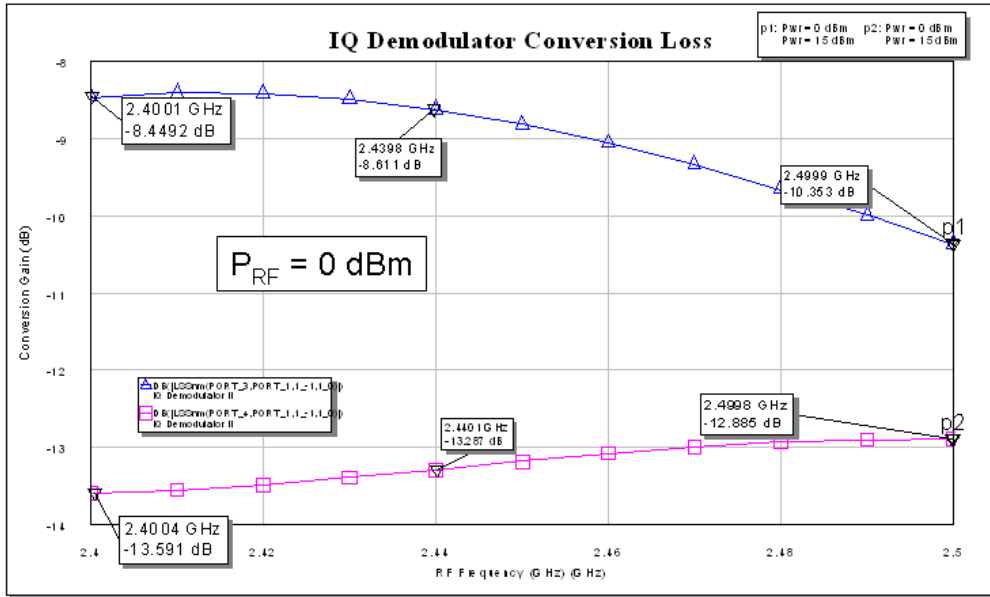


Figure 9: Conversion loss with 0 dBm RF input

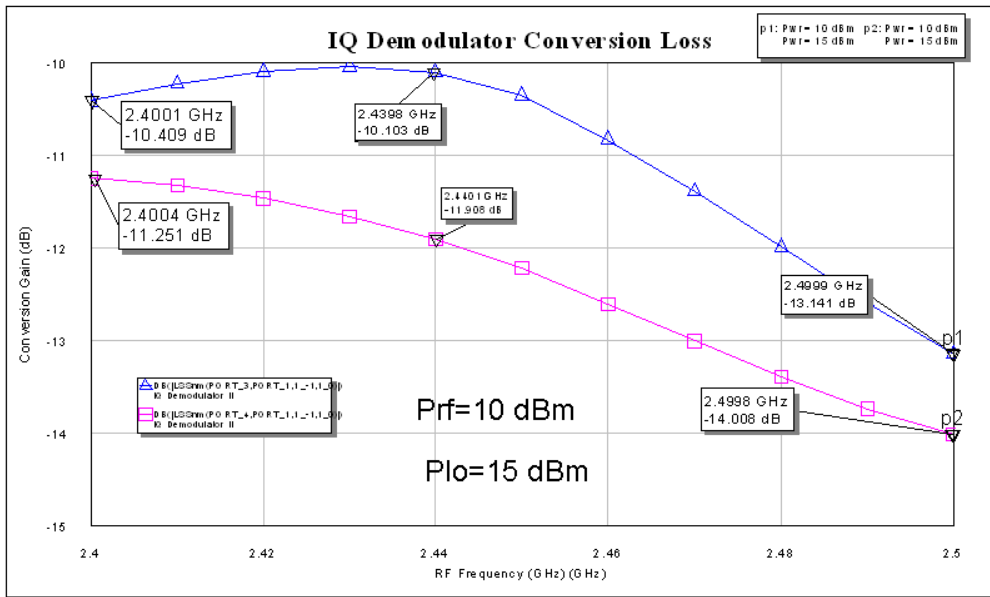
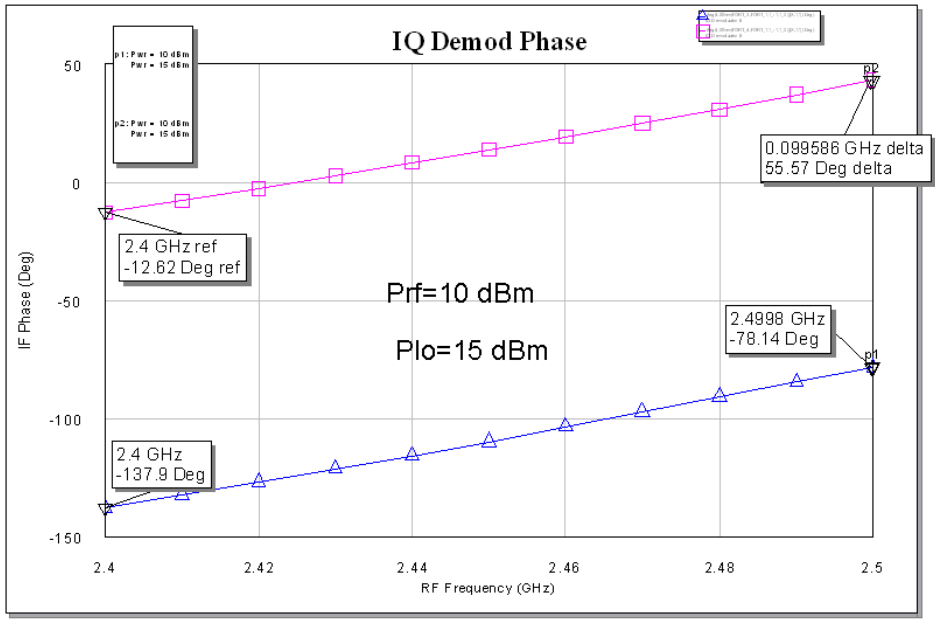


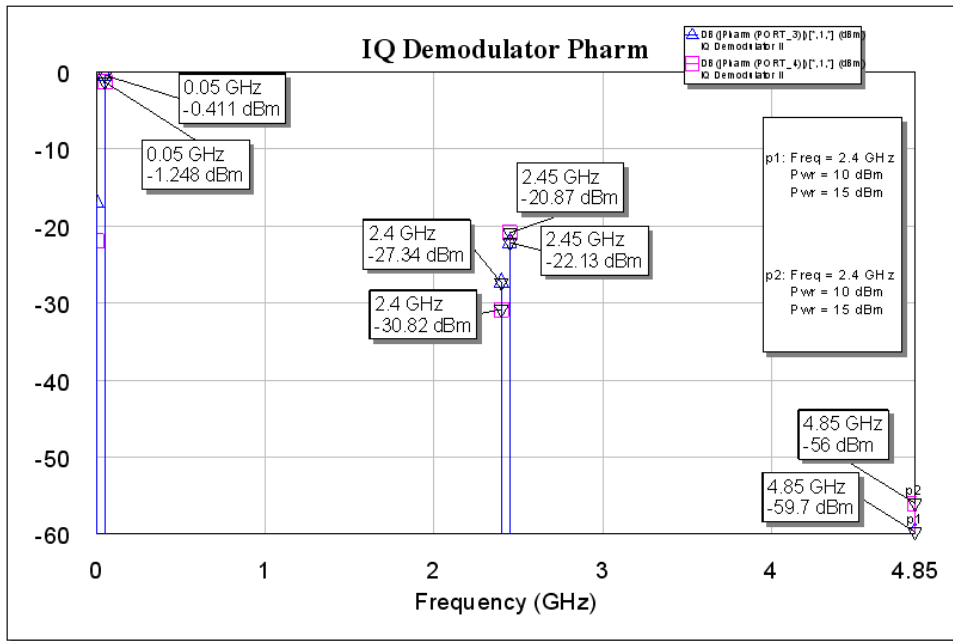
Figure 10: Conversion Loss with 10 dBm RF Input

Figures 9 and 10 show that with a 0 dBm input, there was a five dB difference between the conversion loss on the I port and the conversion loss at the Q port. As the RF power increased the difference in the output powers decreased to about 1 dB.



**Figure 11: IQ Demodulator Phase**

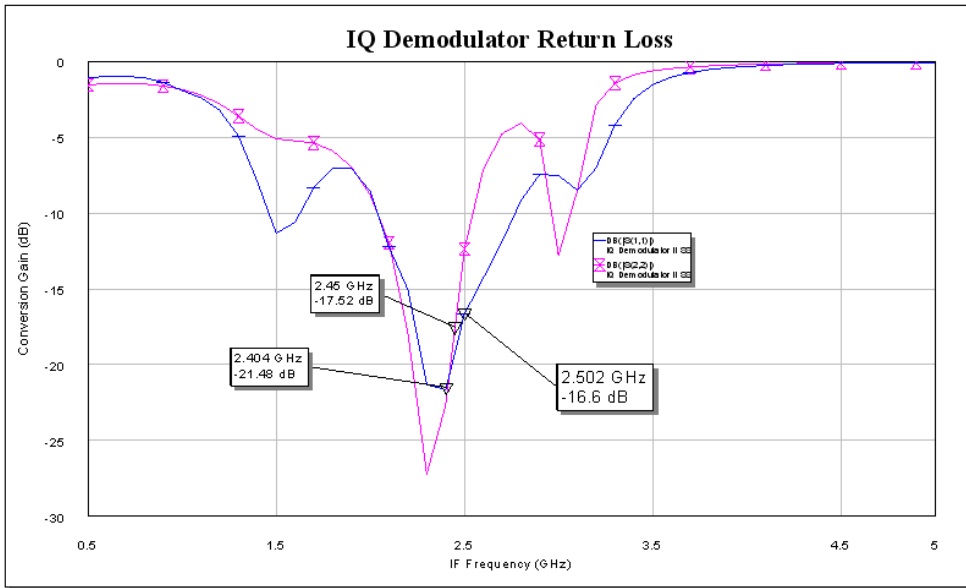
The phase difference between the I and Q ports ranged from 125 degrees to 133 degrees which did not meet the goal of 90 +/- 5 degrees.



**Figure 12: IQ Demodulator Output Spectrum**

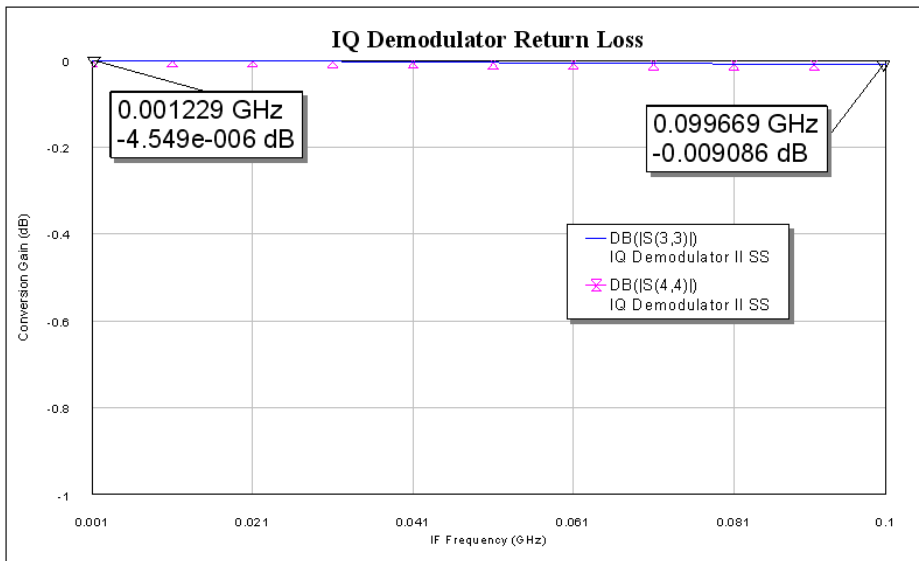


<b>I Port RF-IF Isolation</b>	<b>-37.3 dBc</b>
<b>Q Port RF-IF Isolation</b>	<b>-40.8 dBc</b>
<b>I Port LO-IF Isolation</b>	<b>-37.1 dBc</b>
<b>Q Port LO-IF Isolation</b>	<b>-35.9 dBc</b>
<b>I Port LO + RF Suppression</b>	<b>-59.3 dBc</b>
<b>Q Port LO + RF Suppression</b>	<b>-57.2 dBc</b>



**Figure 12: Input Return Loss**

The input return loss for both the RF and LO ports meets the 15 dB goal.



**Figure 13: Demodulator Output Return Loss**

The demodulator output return loss is very poor (0 dB for all output frequencies). This is due to the large filter caps and diodes at the output of the mixers.

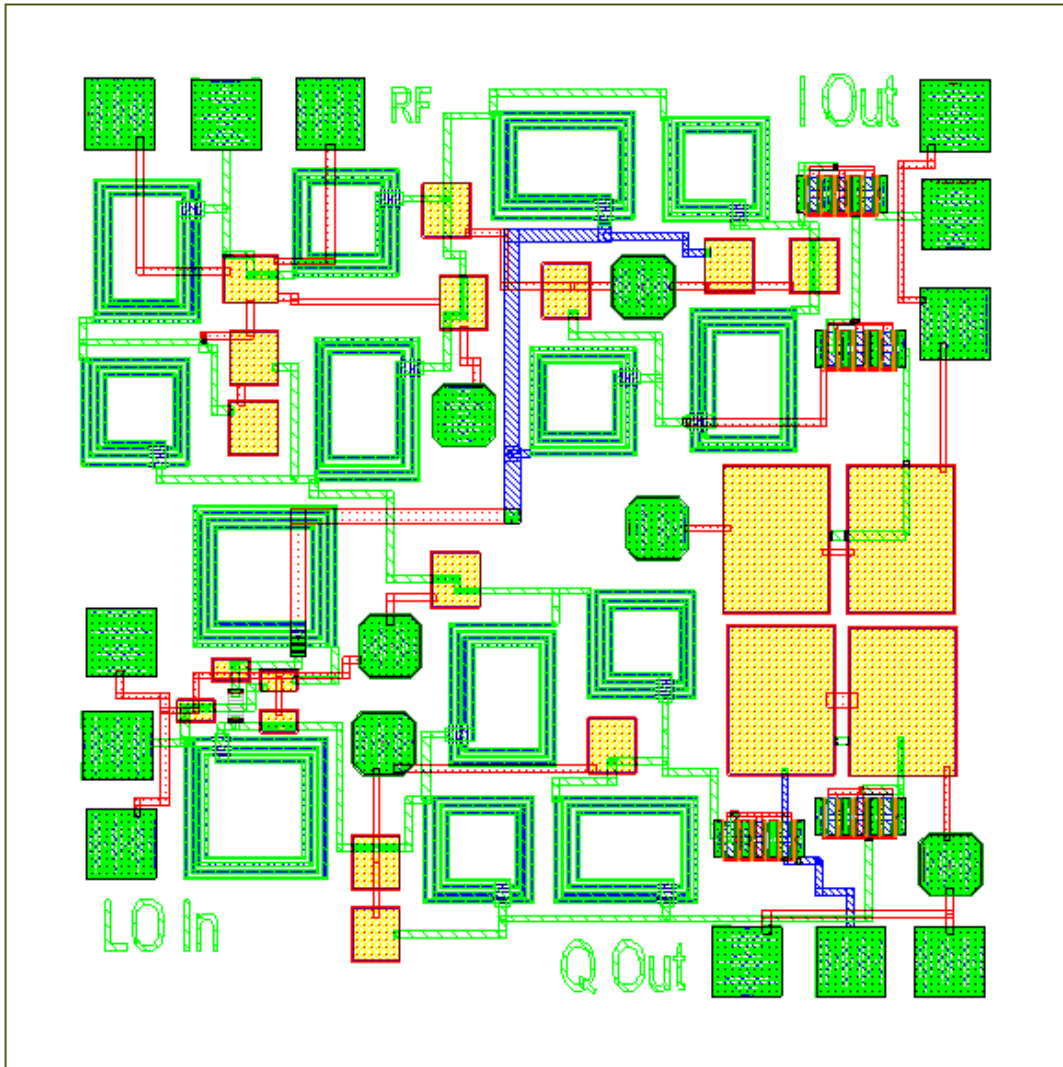


Figure 14: Demodulator Layout

## **Test Plan**

$f_{lo} = 2.45 \text{ GHz}$

$f_{rf} = 2.4 - 2.5 \text{ GHz}$

$P_{lo} = 15 \text{ dBm}$

$P_{rf} = 0 - 10 \text{ dBm}$

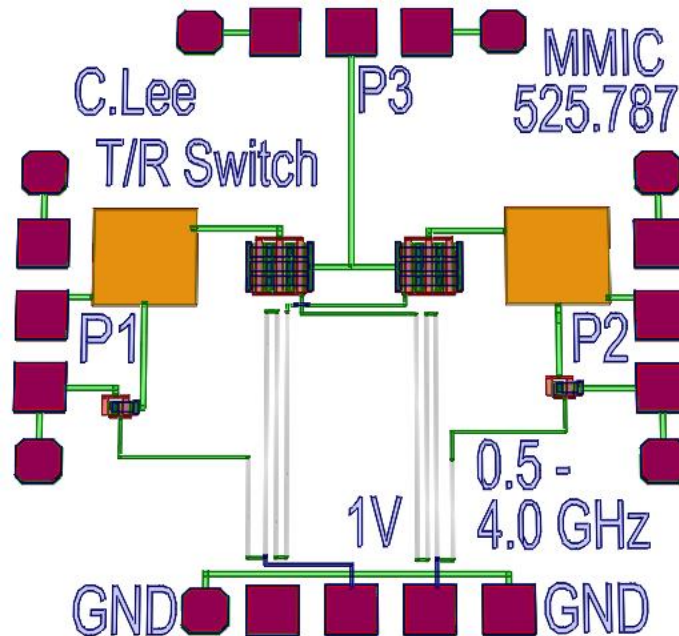
- 1) Use a network analyzer to measure the return loss at all four ports.
  - a. RF and LO: 0.5 – 5 GHz
  - b. I and Q: 1 – 100 MHz
- 2) Sweep the RF from 2.4 to 2.5 GHz and record the conversion loss.
- 3) Apply a fixed RF at 2.4 GHz. Record the output spectrum. Determine RF-IF and LO-IF isolations.

## **Conclusion**

I was able to achieve a conversion loss of approximately 10 dB. The RF inputs required to achieve this were higher than desired however. The input ports had good return losses but the output match was very poor.

I would have liked to have designed some matching circuits for the output ports, but there was not enough room on the chip. Another improvement that could be added is an LO amplifier, which would allow this demodulator to be used with the VCO being designed. Finally, changing the mixers to include a rat-race coupler instead of the hybrid coupler would improve the performance as well. All of these changes would require a larger substrate.

JOHNS HOPKINS UNIVERSITY  
WHITING SCHOOL OF ENGINEERING  
ENGINEERING AND APPLIED SCIENCE PROGRAMS FOR PROFESSIONALS



**Monolithic Microwave Integrated Circuit**  
**Course 525.787**

Broadband Tx/Rx Switch: Final Report

Submitted by:

Chue Lee  
December 2009

Instructors: Professor John Penn  
Dr. Michel Reece

## **Abstract**

A broadband monolithic microwave integrated circuit (MMIC) Tx/Rx switch is presented in this paper. The switch exhibits very low insertion loss ( $IL < 0.5$  dB) parameters for the RF ISM Bands of 2.4 GHz – 2.5 GHz. Simulations performed using Microwave Office (AWR corp.) exhibit a insertion loss of  $< 0.8$  dB for the RF frequency range from 0.5 GHz to 4.0 GHz and  $< 0.5$  dB for the ISM Bands mentioned above. The MMIC switch fits on a 60 mil x 60 mil GaAs chip with a +1V power supply. The transition between transmit (Tx) and receive (Rx) paths are controlled using two logic control BITS, either +1V “on” or 0V “off”, to turn a path on and off. Enhancement (E-mode) pHEMTs are used for the switch and are to be fabricated by TriQuint Semiconductor Inc.

## TABLE OF CONTENTS

Abstract .....	2
Table of Contents .....	3
1.0 Introduction .....	4
2.0 Design .....	5
2.1 Circuit Approach.....	5
2.2 Design specifications .....	6
2.3 Trade-offs.....	6
3.0 RF Performance .....	7
3.1 pHEMT Model Performance .....	7
3.1.1 Ideal Switch RF Performance Results .....	8
3.1.2 Real Switch RF Performance Results .....	8
4.0 Tx/Rx Switch Schematic.....	11
4.1 Final Layout .....	12
5.0 Test Plan.....	13
5.1 Test Equipment Configuration.....	13
5.2 RF Tests .....	13
5.2.1 Insertion Loss Test.....	14
5.2.2 Isolation Test.....	14
6.0 Conclusion .....	15



## 1.0 Introduction

The broadband Tx/Rx switch was designed as a part of an S-band transceiver as depicted in Figure 1, System Block Diagram. It will be used to receive and transmit data within the ISM band frequencies of 2.4 GHz to 2.5 GHz. The broadband versatility of this switch allows for it to be used for multiple ISM bands. The switch covers the wireless communications service (WCS) frequencies from the lower ISM band range of 902 MHz to 928 MHz to the upper ISM band range of 2.4 GHz to 2.5 GHz. The design of this switch was tailored for low voltage-low power applications such as battery operated mobile devices. The design utilizes two control BITS for independent enable/disable operations of the Tx/Rx paths. This report details the design, simulation, layout, and test plan for the switch design.

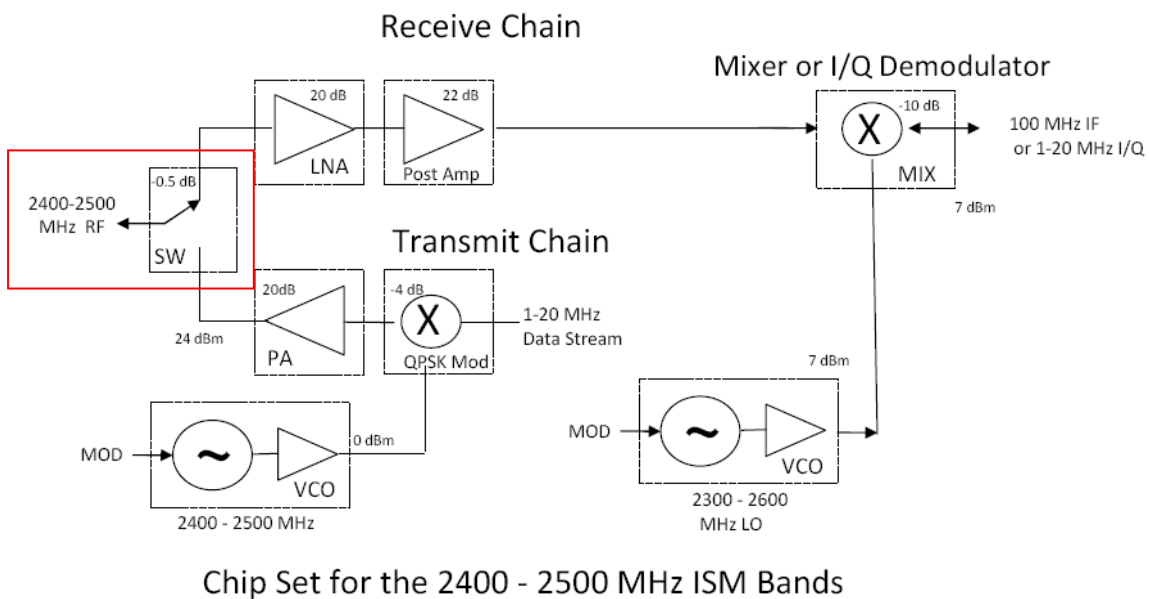


Figure 1. System Block Diagram

## 2.0 Design

The design for this switch was first modeled as a pure resistor when in the “ON” state and a capacitor when in the “OFF” state as shown in Figure 2.

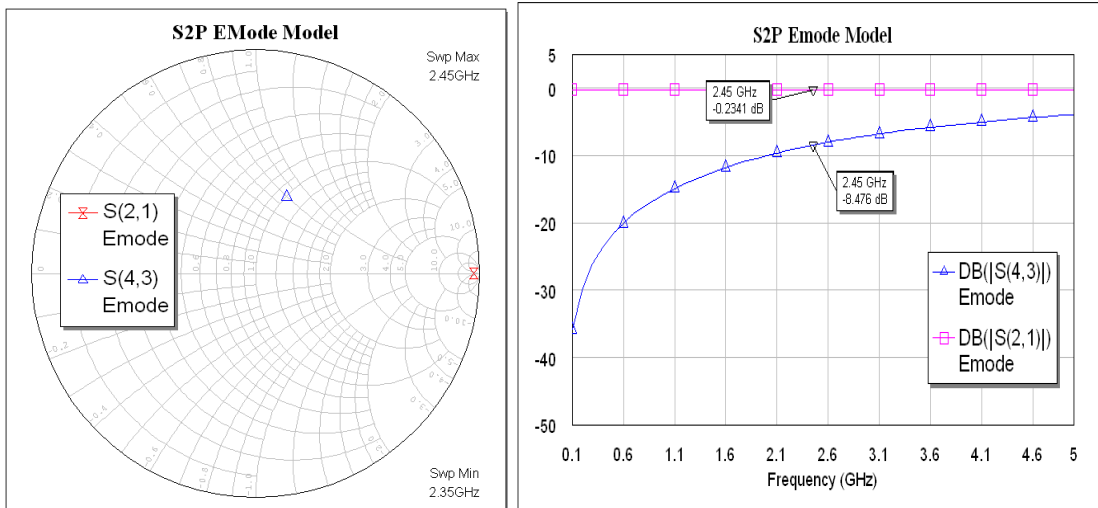


Figure 2. “ON” state-S21 measurement, “Off” state- S43 measurement

## 2.1 Circuit Approach

A single pHEMT device was size appropriately to match the “ON”, “OFF” state RF characteristics shown in Figure 2.

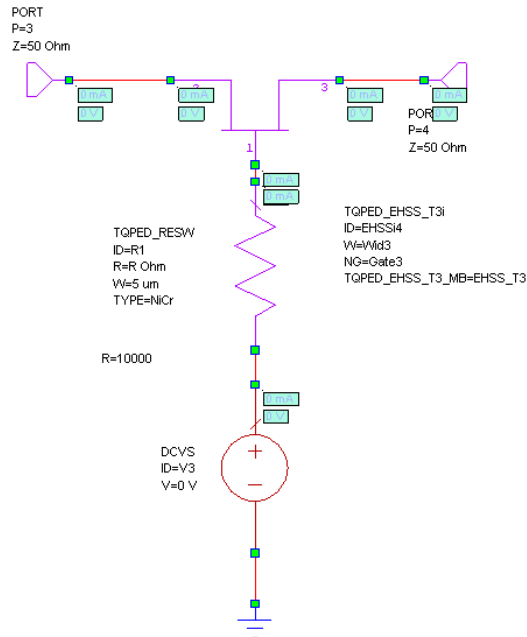


Figure 3. pHEMT device, sized to match RF performance of Figure 2.

## **2.2 Design specifications**

Table 1, below shows the specifications for this design. These values were estimate “target” values set as an initial goal. With time permitting, these specifications would generally be improved upon. The mind set was to achieve these specifications first.

Specification	
Frequency range	2.4 to 2.5 GHz
Insertion Loss	<0.5 dB
Tx/Rx Port Isolation	20 dB
Power handling	20 dBm
Size	60mil X 60mil
Control Logic	3V supply

**Table 1. Design specifications**

## **2.3 Trade-offs**

Two circuit typologies where initially simulated with varying results. Circuit A incorporated external input (IMN) and output matching networks (OMN) shown in Figure 4A. The simulation (not provided) for this typology met the IL <0.5dB using ideal microwave elements for the specified bandwidth, however, sharply increased once outside the specified bandwidth. Once lossy elements were introduced this typology failed the IL specification for the specified bandwidth. This typology was bandwidth limited since the IMN/OMN circuits were tuned for a center frequency of 2.45 GHz. The benefit to this typology was good input/out matching (-60 dB return loss).

Ultimately the design chosen (circuit B) was to incorporate the IMN/OMN into the pHEMT devices. By sizing the pHEMT devices appropriately the IMN/OMN could be achieve to a limited degree. The benefit from this typology provided for a greater bandwidth and less IL across the greater bandwidth. Once real elements were introduced, the IL was relatively maintained and still met the specified IL for the given bandwidth. Circuit B is shown in Figure 4B.

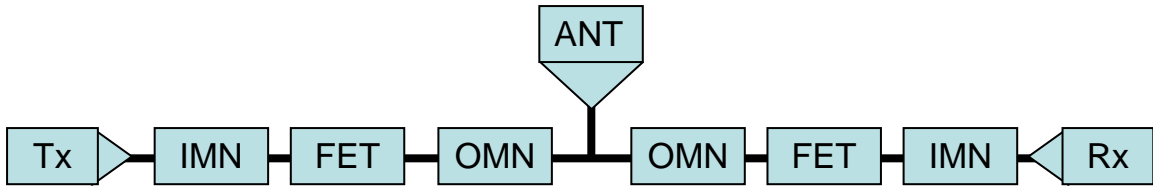


Figure 4A, Circuit A Block Diagram

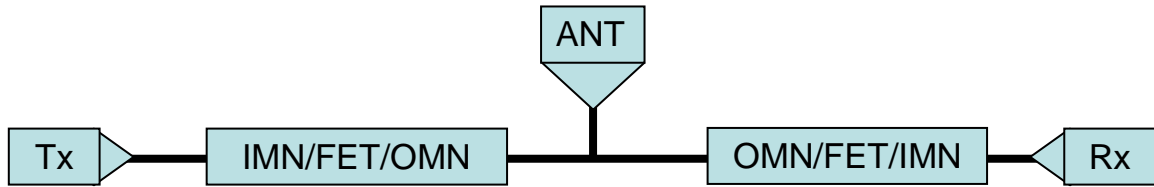


Figure 4B, Circuit B Block Diagram

### 3.0 RF Performance

Shown below are the simulation results for the pHEMT Model, Ideal Switch Model and Real Switch.

#### 3.1 pHEMT Model Performance

Figure 5 shows the RF performance for the “sized” pHEMT device itself. The simulated IL for the “sized” pHEMT was 0.23 dB at a center frequency of 2.45 GHz, when turned “ON”.

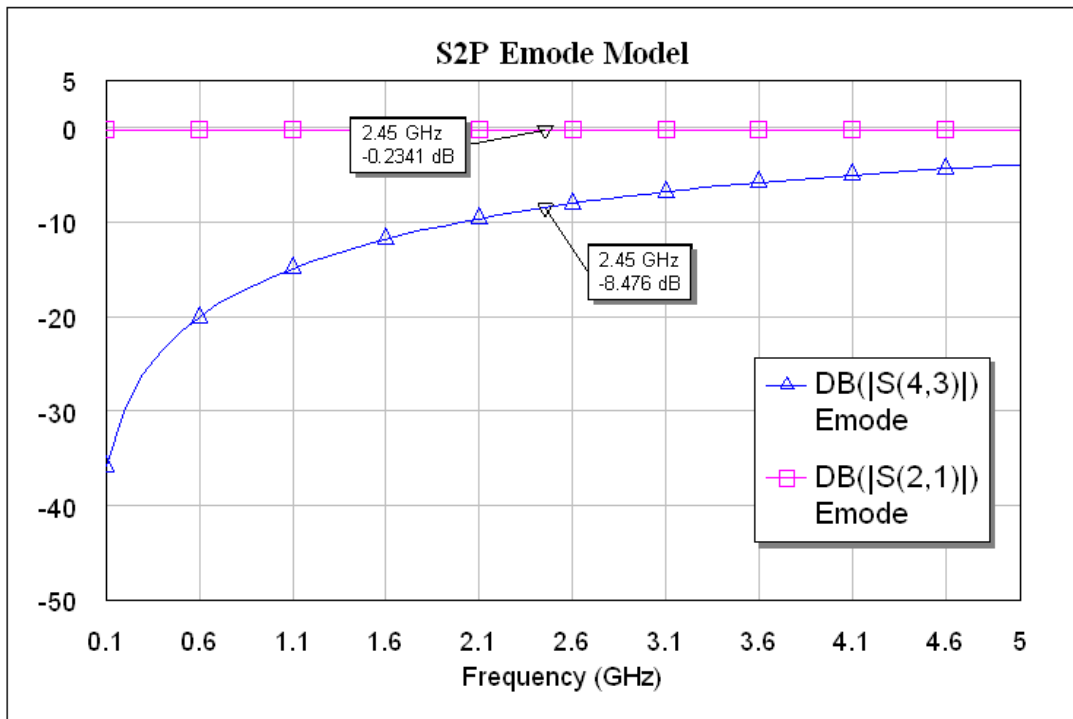


Figure.5. S-parameter performance of the “sized” pHEMT model. S21-“ON”; S43-“OFF”

### 3.1.1 Ideal Switch RF Performance Results

Figure 6 shows the RF performance for the Ideal Switch. With the Tx path “ON”, Rx path “OFF”, the simulated IL for the Ideal switch was 0.43 dB. The Isolation from Tx/Rx Ports was ~26.5 dB.

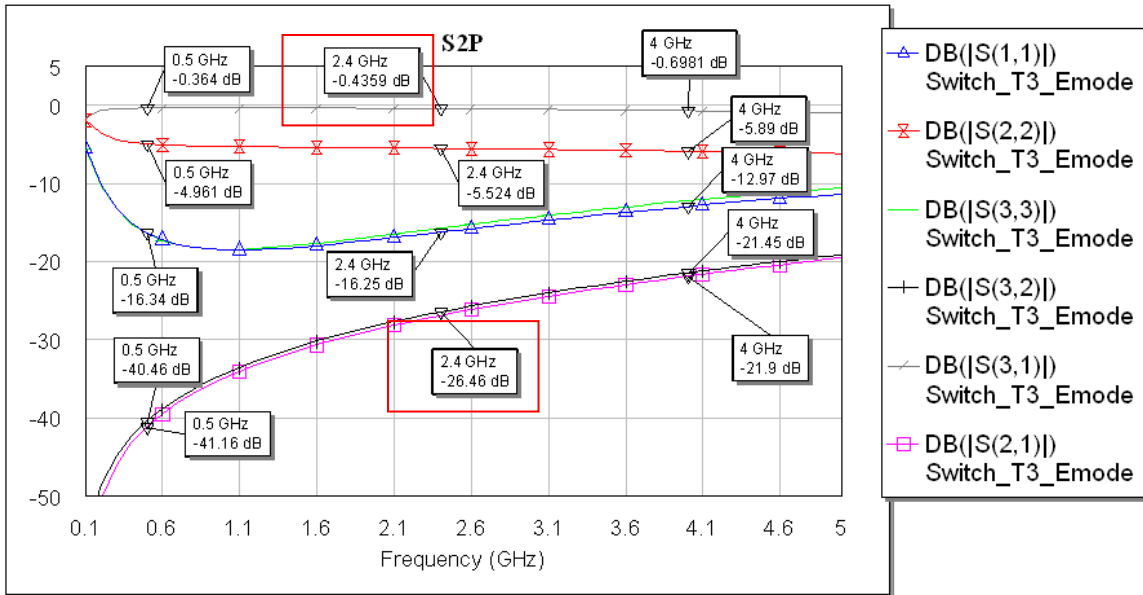
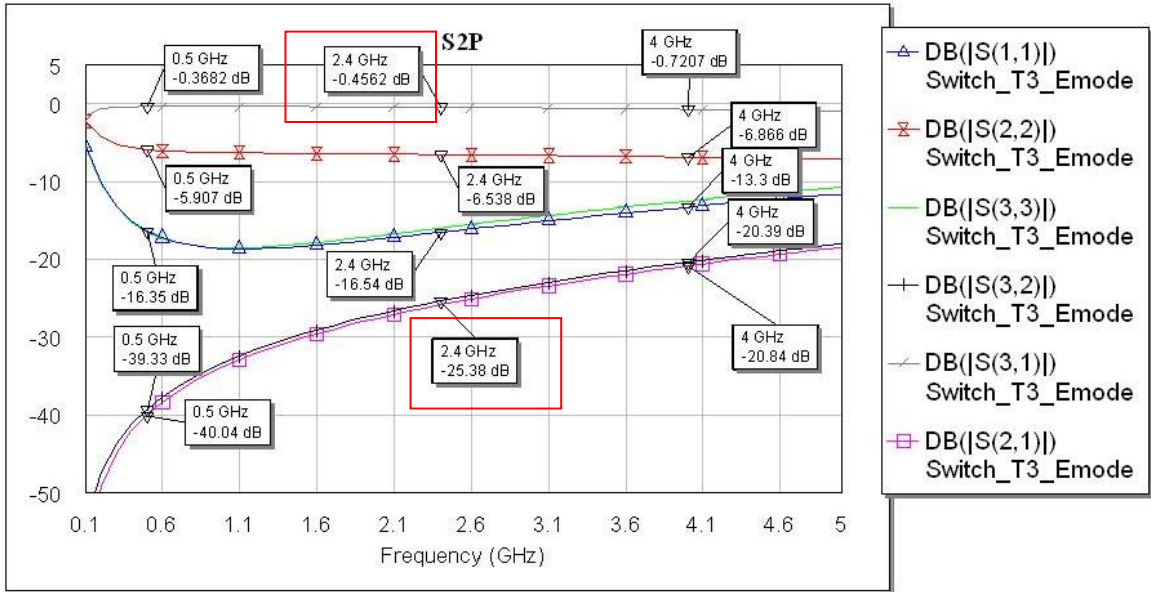


Figure 6. RF simulation results of Ideal Tx/Rx Switch. Tx = Port 1, Rx = Port 2, ANT = Port 3  
Tx “ON”, Rx “OFF”

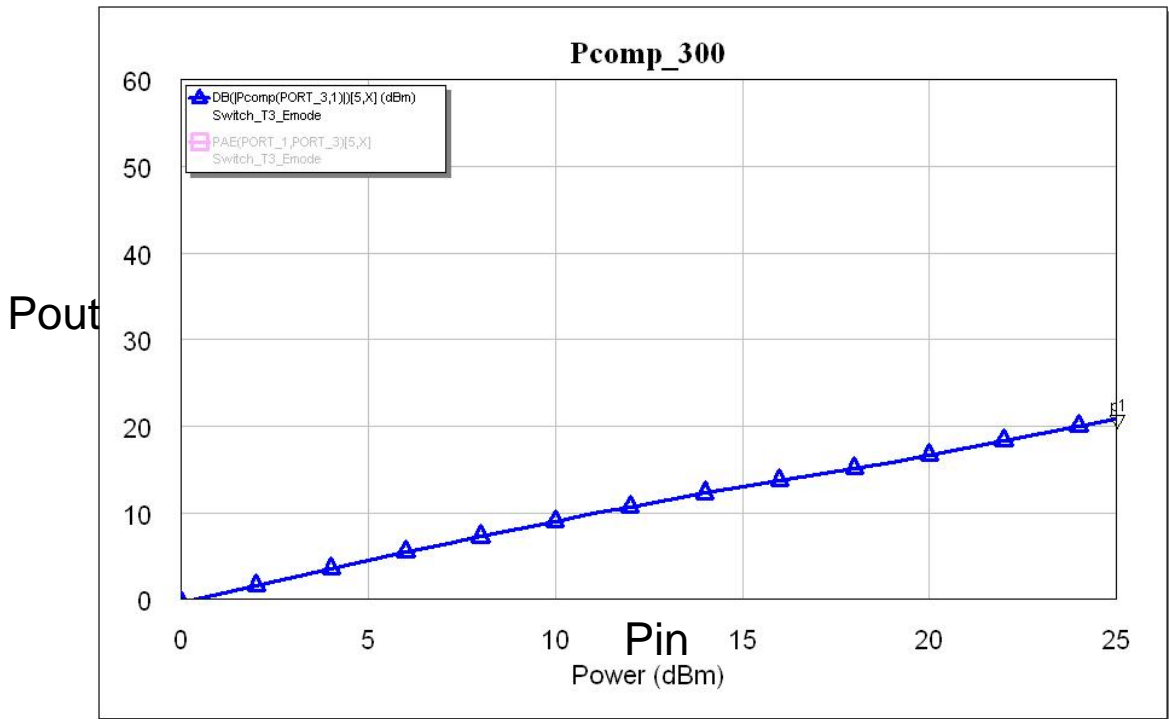
### 3.1.2 Real Switch RF Performance Results

Figure 7A, 7B, and Table 2 summarizes the results of the real element switch circuit. With the same Tx/Rx settings as the Ideal switch for Figure 6, the real switch’s IL was 0.45 dB, a delta of 0.02 dB. The isolation also changed from ~26.5 dB to ~25.4 dB, a delta of 1.1 dB.



**Figure 7A. RF simulation results of real Tx/Rx Switch. Tx = Port 1, Rx = Port 2, ANT = Port 3  
Tx “ON”, Rx “OFF”, Reciprocal values were verified with Rx “ON” and Tx “OFF”.**

The power handling capability for this switch was simulated to be fairly linear up to  $P_{out} = 20$  dBm.



**Figure 7B. Power handling results of Tx/Rx Switch.**

Highlighted in Table 2 are the specification goals as well as the simulated final results. For the specified frequency range, the IL met its requirement of <0.5 dB. From 0.5 GHz to 4.0 GHz, the IL increased linearly from 0.3 dB to 0.7 dB. The Isolation decreased from 40 dB to 20 dB across frequency.

Specification		Simulation Results	
Frequency range	2.4 to 2.5 GHz	2.4 to 2.5 GHz	0.5 to 4.0 GHz
Insertion Loss	<0.5 dB	0.45 dB	0.3 to 0.7 dB
Tx/Rx Port Isolation	20 dB	25 dB	40 to 20 dB
Power handling	20 dBm	20 dBm	20 dBm
Size	60mil X 60mil	60mil X 60mil	60mil X 60mil
Control Logic	3V supply	1V, 0V control	1V, 0V control

**Table 2. Specification Vs simulation results.**

## 4.0 Tx/Rx Switch Schematic

Figure 8 below shows the schematic for the Tx/Rx Switch. The switch composes of a DC blocking capacitor in series with a shunt FET and series FET for each Tx/Rx path. The shunt and series FETs were sized to appropriately best match the input and output to a 50 ohm load, while maintaining the low IL. Per each Tx/Rx path, the shunt and series FETs are in opposite states, i.e. when one FET is “ON”, the other is “OFF”. This feature was incorporated to increase isolation from Tx Port to Rx Port and vice versa. For example, when the Tx series FET is “ON”, we have a “thru” path from the Tx Port to the Antenna Port, since the Tx shunt FET is “OFF”. At the same time, the Rx series FET is “OFF”, creating a “RF Block”. Any unwanted signal that leaks through from either Tx or Antenna Ports to the Rx Port is shorted to ground since the Rx shunt FET is “ON”. Port 1 = Tx, Port 2 = Rx, Port 3 = Antenna.

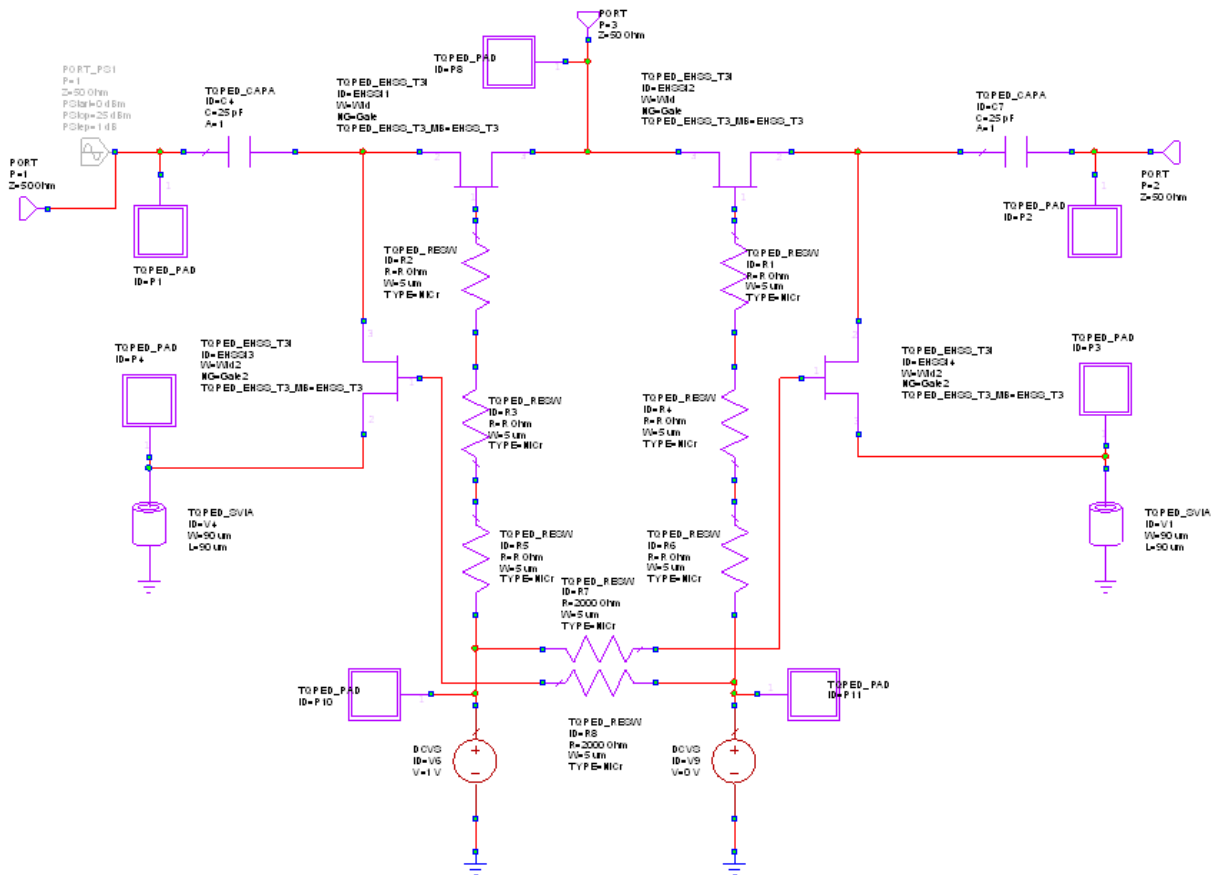


Figure 8. Schematic of the Tx/Rx Switch.



## 4.1 Final Layout

Figure 9 shows the final layout of the Tx/Rx Switch. With Port 1 or Port 2 as Tx or Rx and Port 3 as Antenna Port. The BIT logic port is shown as well.

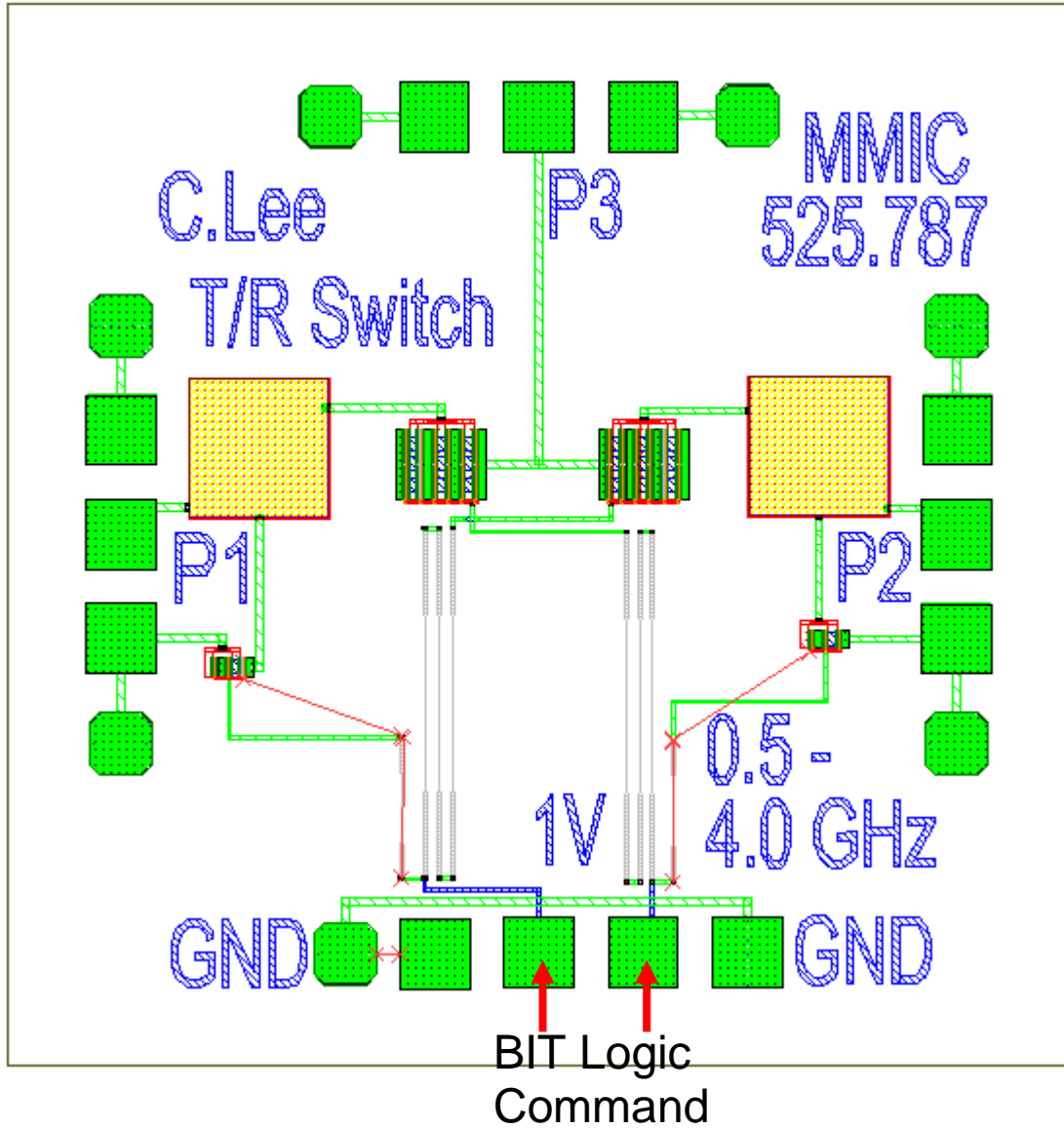


Figure 9. Layout of the Tx/Rx Switch.

## **5.0 Test Plan**

The test plan for this switch assumes that the tester has the knowledge of performing a full 2-port SOLT calibration of the VNA/ test equipment and therefore the calibration process will not be explained here. The test equipment required for testing this switch are:

- 1) Network Analyzer capable of measuring and recording s2p parameters up to 4.5 GHz
- 2) DC power for Logic Command
- 3) Probe station for the device under test (DUT).

## **5.1 Test Equipment Configuration**

Figure 10, shows the test setup required for performing the required RF tests.

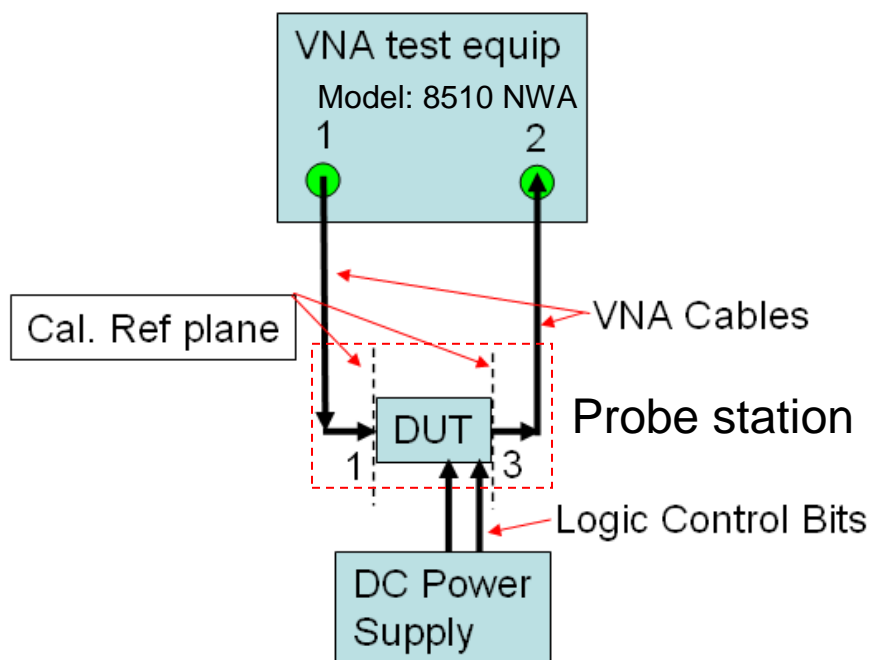


Figure 10, Test setup diagram.

## **5.2 RF Tests**

Setup the NWA to sweep from DC (or the minimum frequency of the NWA) to 4.5GHz with 1601 pts, RF Input Power level of 0 dBm, IF BW of 5kHz, sweep time of 2 sec. Perform a full 2-Port SOLT calibration on the test setup shown in Figure 10.

### **5.2.1 Insertion Loss Tests**

- 1) Connect the VNA cable attached to Port 1 of the VNA to “Port 1 of the DUT”.
- 2) Connect the VNA cable attached to Port 2 of the VNA to “Port 3 of the DUT”.
- 3) Terminate “Port 2 of the DUT” to a 50 ohm Load.
- 4) Turn on the DC power supply and apply the control bit command “10” to turn the Tx path “ON” and Rx path “OFF”.
- 5) Record the S-Parameters of the DUT into an s2p file. Save with appropriate name to indicate Tx path is “ON”.
- 6) Repeat step 1 with “Port 2 of the DUT”.
- 7) Repeat step 3 with “Port 1 of the DUT”.
- 8) Repeat step 4 with the control bit command “01”.
- 9) Repeat step 5 and save with appropriate name to indicate Rx path is “ON”.

### **5.2.2 Isolation Tests**

- 1) Connect the VNA cable attached to Port 1 of the VNA to “Port 1 of the DUT”.
- 2) Connect the VNA cable attached to Port 2 of the VNA to “Port 2 of the DUT”.
- 3) Terminate “Port 3 of the DUT” to a 50 ohm Load.
- 4) Turn on the DC power supply and apply the control bit command “10” to turn the Tx path “ON” and Rx path “OFF”.
- 5) Record the S-Parameters of the DUT into an s2p file. Save with appropriate name to indicate Tx → Rx path Isolation.
- 6) Repeat step 4 with command “01”.
- 7) Repeat step 5 with and save with appropriate name to indicate Rx → Tx path Isolation.

## **6.0 Conclusion**

A complete MMIC design for an S-Band Tx/Rx switch was presented. The specifications outlined in table 1 were met by appropriately “sizing” the pHEMT devices to compensate for input/ output mis-matches. The benefit of using sized pHEMTs allowed for broader bandwidth which is preferred for multiple RF frequency ranges. Another benefit for using this approach allowed for lower Insertion Loss since no additional microwave elements were needed. The trade-off for additional bandwidth and lower Insertion Loss was decreased input/output matching resulting in higher VSWR. All other specifications for the mixer were met as shown in Table 2 and section 3.1.2. Future improvement to this design could be to:

- Cascade frequency specific switches to improve the VSWR matching at various frequencies.
- Designing an inverter between 0V and 1V to be used in conjunction with the Logic command BIT signals so that only one control bit is necessary for controlling the Tx/Rx paths.
- Research the possibility of using different mode pHEMTs and switch topologies to reduce the switch loss while improving the VSWR performance.