

Fall 2010 JHU EE787 MMIC Design Student Projects
Supported by TriQuint, Applied Wave Research, and Agilent
Professors John Penn and Dr. Willie Thompson

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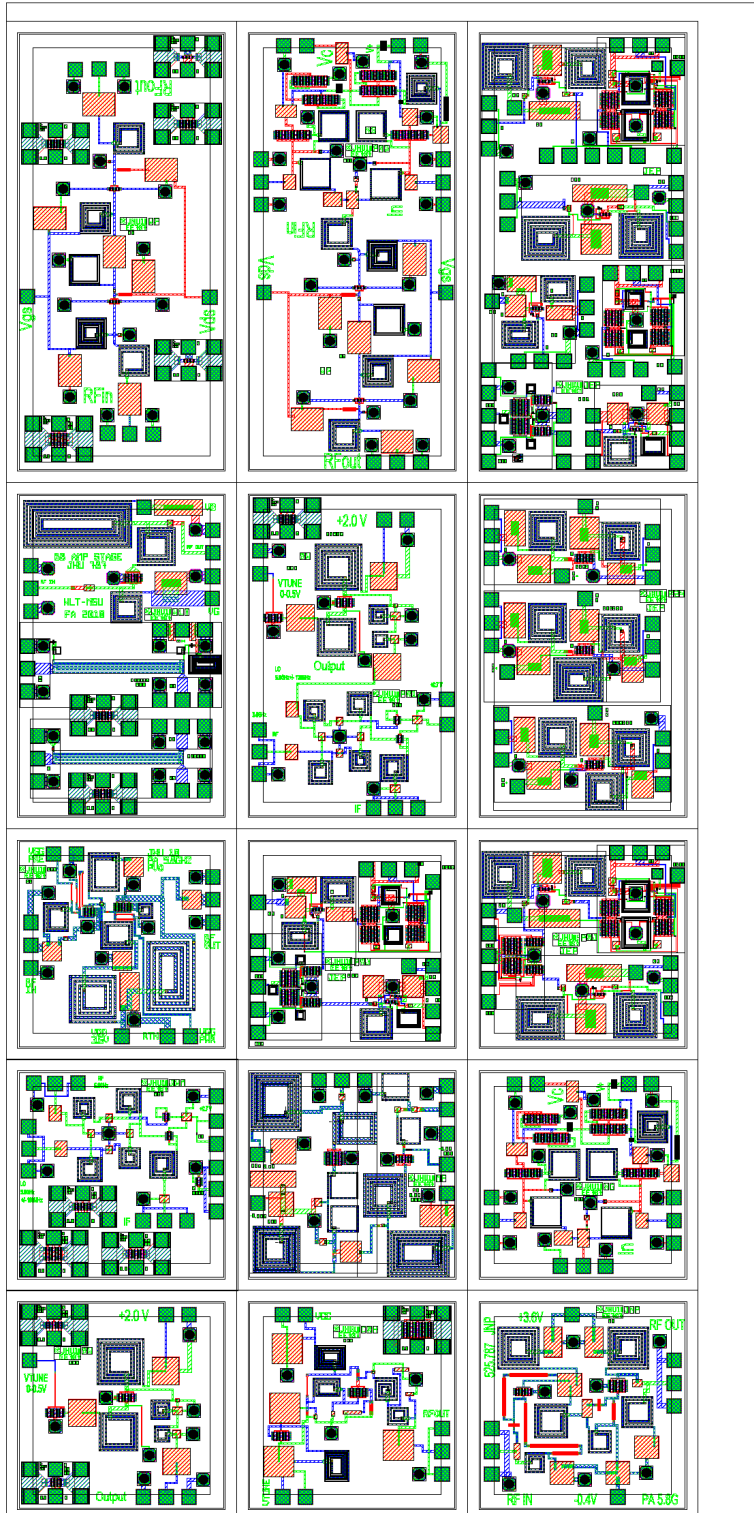
[Low Noise Amplifier— Wade Freeman](#)

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[Voltage Controlled Oscillator— Ben Woodworth](#)

[C-band Mixer—James McKnight](#)

[Presentation for Power Amplifier 1--Paul Van Opens](#)



Two-Stage, C-Band Power Amplifier Design

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ABSTRACT

This report documents the design and performance of a 3.6V, GaAs power amplifier for C-Band frequencies (5.725GHz – 5.875GHz). The goal is for the amplifier to provide at least 20dBm (0.1W) of output power with a gain of at least 20dB. The power amplifier is a two stage design, with the output stage designed for high output power and the input stage designed for high gain. Both are Class A amplifiers, which grants the power amplifier the ability to provide a very low-distortion output tone. Also included in this report is an explanation of the power amplifier’s schematics and layout, as well as a test plan for measuring the performance of the power amplifier.

INTRODUCTION

This power amplifier design is meant to operate in the C-Band frequency range. It is intended for use in hand-held device applications. As such, good efficiency is one important aspect of the design. However, output power and gain are the two most critical parameters. The goals for this power amplifier design are given in the table below.

Parameter	Design Goal
Operating Frequency	5.725 – 5.875 GHz
Small Signal Gain	> 20dB
Output Power at P1dB	> 20dBm
PAE at P1dB	> 30%
Input Match	< -15dB
Output Match	< -6dB
Drain Voltage	3.6V
Chip Area	0.06” x 0.06”

Table 1: Power Amplifier Design Goals

DESIGN APPROACH

The overall approach for this design is to use a two-stage amplifier to reach both the gain and output power goals. The output stage, or power stage, is designed to provide the highest output power possible for a standard size device. The input stage, or preamplifier stage, is designed to have enough gain to allow the overall amplifier to meet the design goal. It also needs to be able to provide sufficient power to the power stage before it begins to enter compression, which could serve to limit the total amplifier’s output power. Although efficiency is a consideration in this design, the goal can be reached with a simple Class A design.

The Power Stage

The power stage was designed to be a Class A amplifier capable of providing 20dBm of output power. A standard 6x50 μ m depletion mode device was chosen for this stage. Lacking Load Pull data, the Cripps approach was used to design the device’s output matching network for the appropriate output power. The depletion mode device is biased at Idss (~65mA). With a 3.6V drain, we would predict roughly 19.5dBm of output power for this load line.

The output matching network for this amplifier was designed for maximum output power. Since the device is biased at I_{dss} , the biasing network is simply a $1k\Omega$ pull-down resistor. Figure 1 shows the ideal implementation of the amplifier. A source inductor is used to improve stability, although at the sacrifice of gain.

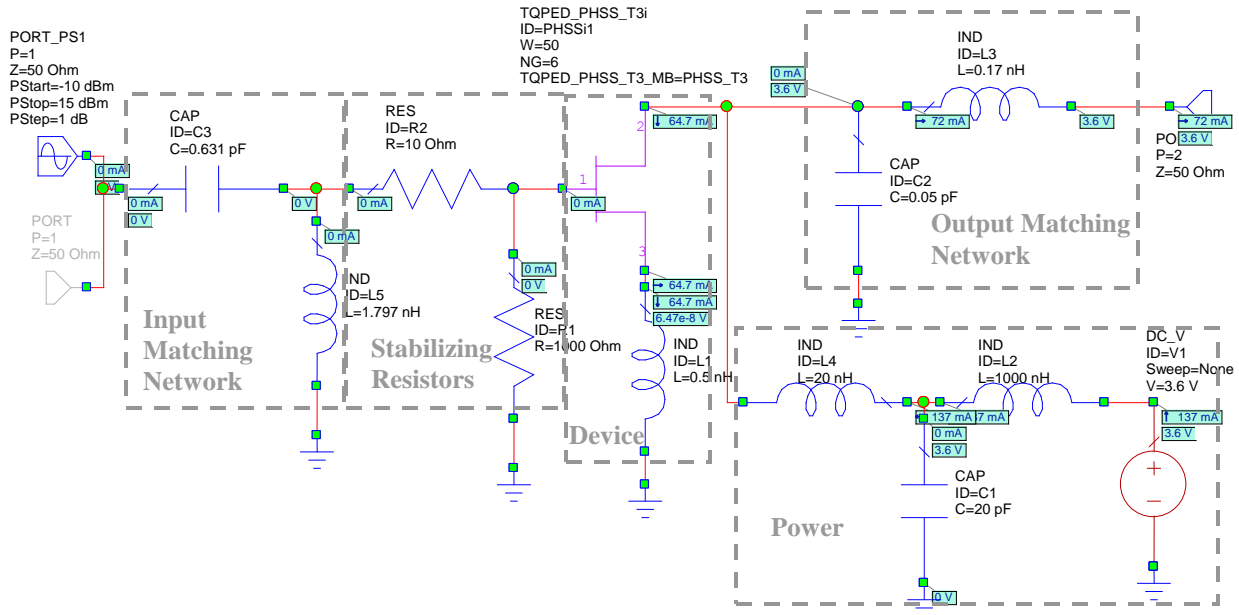


Figure 1: Power Amplifier Stage Schematic with Ideal Components

The circuit was reconstructed using TriQuint components in place of the ideal elements. More details are available in the Appendix, but the salient performance characteristics are summarized in the table below.

Parameter	Ideal	TriQuint
Small Signal Gain	9db	8.591dB
Output Power at P1dB	20.57dBm	20.11dBm
PAE at P1dB	39.14%	36.13%

Table 2: Power Amplifier Stage Performance

The power stage shows very linear Class A operation. This gives confidence that the output matching network and biasing were designed appropriately. Additionally, the stability of this stage seems to be acceptable across the frequencies of interest. The implementation using TriQuint elements appears to be stable over all frequencies, although lower frequencies may be of concern.

The Preamplifier Stage

Given the performance of the power amplifier stage, the requirements for the preamplifier stage become apparent. In order to achieve 20dB overall gain, the preamplifier must have more than ~12dB of gain. Also, the preamplifier must be able to provide up to ~12dBm at its P1dB point to

prevent it from going into compression before the power stage. A $4 \times 50 \mu\text{m}$ Enhancement mode device was chosen for the preamplifier

The load line predicts an output power of 14.5dBm, which should be sufficient for the preamplifier. This will require the gate of the device to be biased at +0.65V, which can be achieved using a simple resistor divider with the drain voltage. Since the output power was more than sufficient for this preamplifier, it was possible to negotiate the power for more gain in the design of the output matching network.

The schematic for the preamplifier using ideal elements is given below.

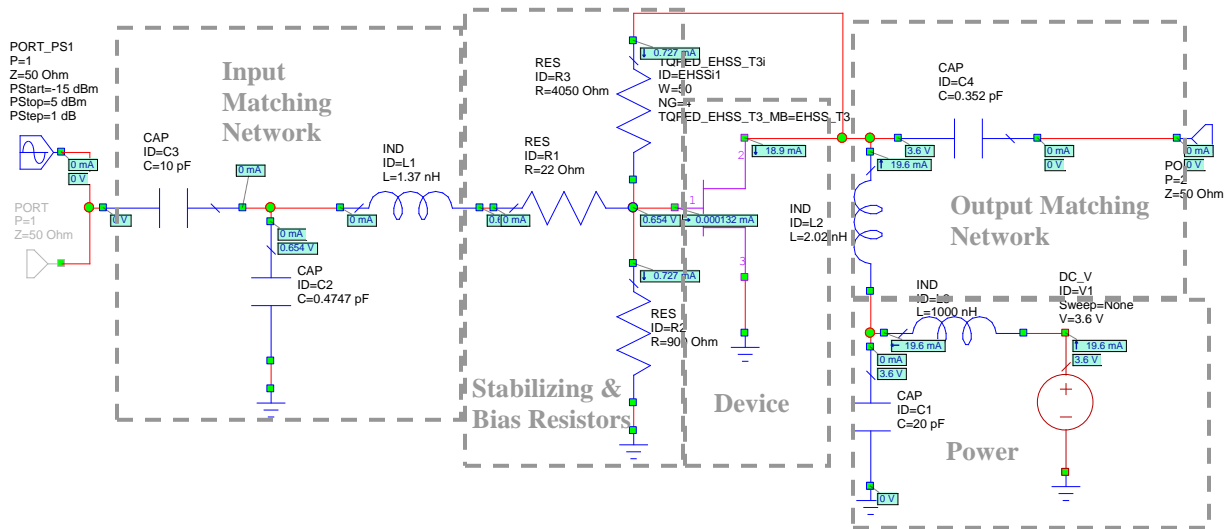


Figure 2: Preamplifier Stage Schematic with Ideal Components

The circuit was reconstructed using TriQuint components in place of the ideal elements. More details are available in the Appendix, but the performance characteristics are summarized in the table below.

Parameter	Ideal	TriQuint
Small Signal Gain	13.72dB	13.39dB
Output Power at P1dB	15.55dBm	15.69dBm
PAE at P1dB	43.11%	42.38%

Table 3: Power Amplifier Stage Performance

As with the power amplifier stage, the preamplifier has very good Class A operation. The stability is adequate at the frequencies of interest, although low frequency stability is marginal.

The Combined Power Amplifier

Cascading both amplifier stages would imply a gain of 21.98dB (13.39dB + 8.59dB) and an output power of 20.11dBm. Cascading the two stages is relatively straightforward since a series capacitor is the last element on the preamplifier's output matching network and the first element in the power amplifier's input matching network.

To maintain the simplicity of this design, both amplifier stages use a single supply. Inductors and a large capacitor were added to isolate the stages from the supply and each other, as shown below.

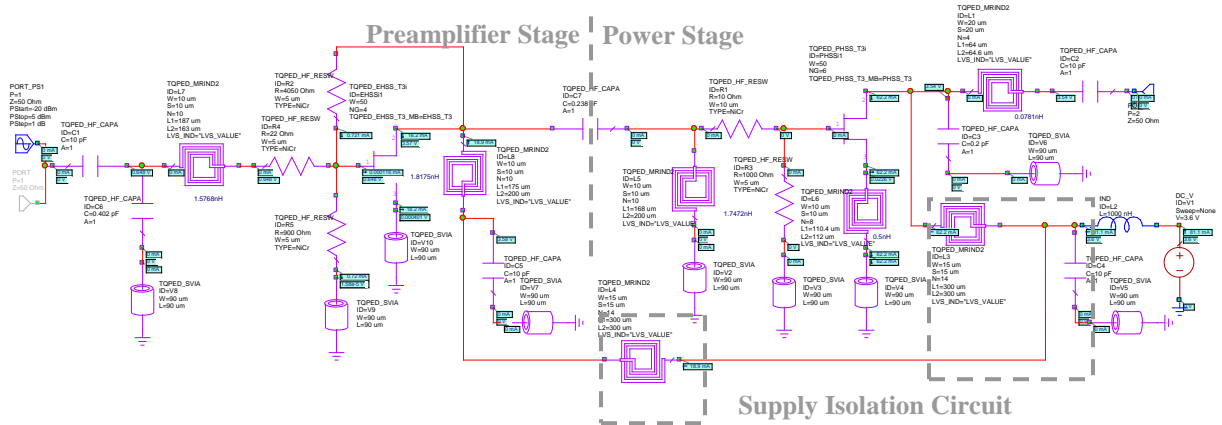


Figure 3: Preliminary Combined Power Amplifier Schematic

Changes were made from this point to finalize the design. Interconnects were added to all input and output ports. The circuit was laid out on a 0.060" x 0.060" ANACHIP substrate. The traces were extracted from the layout and included in the simulation. Subsequent tuning of the matching networks allowed the design to get by with less gain in order to reclaim some power that was lost when the layout elements were included. Additionally, 1k Ω resistors were added to the gates of both devices and connected to open pads on the circuit. Although the circuit is designed to not need any outside biasing, these resistors will allow an external bias to be added if needed.

SIMULATION RESULTS

The following simulation results document the predicted performance of the completed power amplifier. They include the affects of the element interconnects. Additional simulation results can be found in the Appendix.

The plot below shows the S-Parameters of the final power amplifier. The predicted input match at the center frequency is good at -61.6dB (although the actual implementation is not expected to be that good). The output match is relatively poor at -3.2dB.

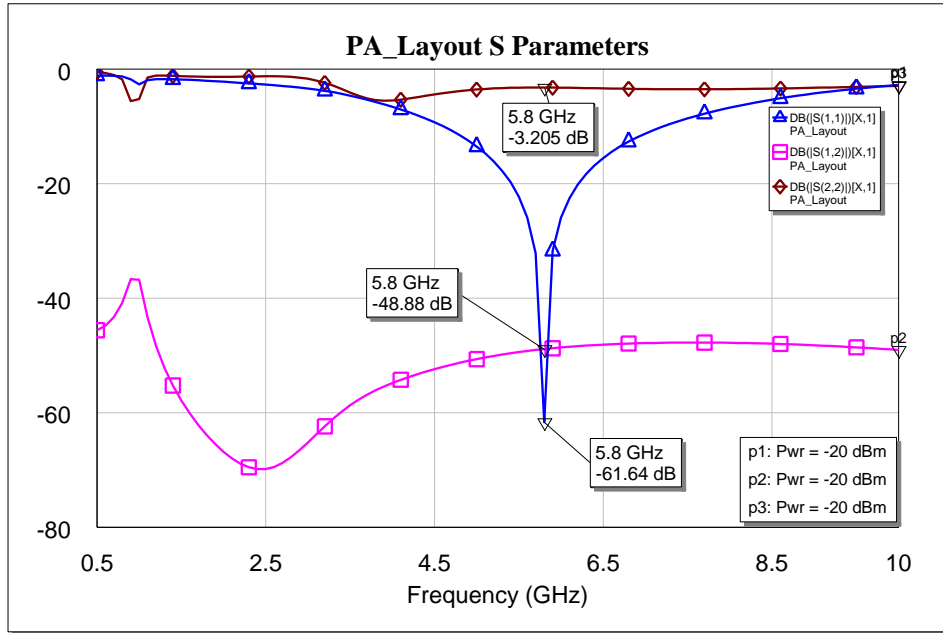


Figure 4: S Parameters for Completed Power Amplifier

The plot below shows the gain of the amplifier to be 21dB at the center frequency.

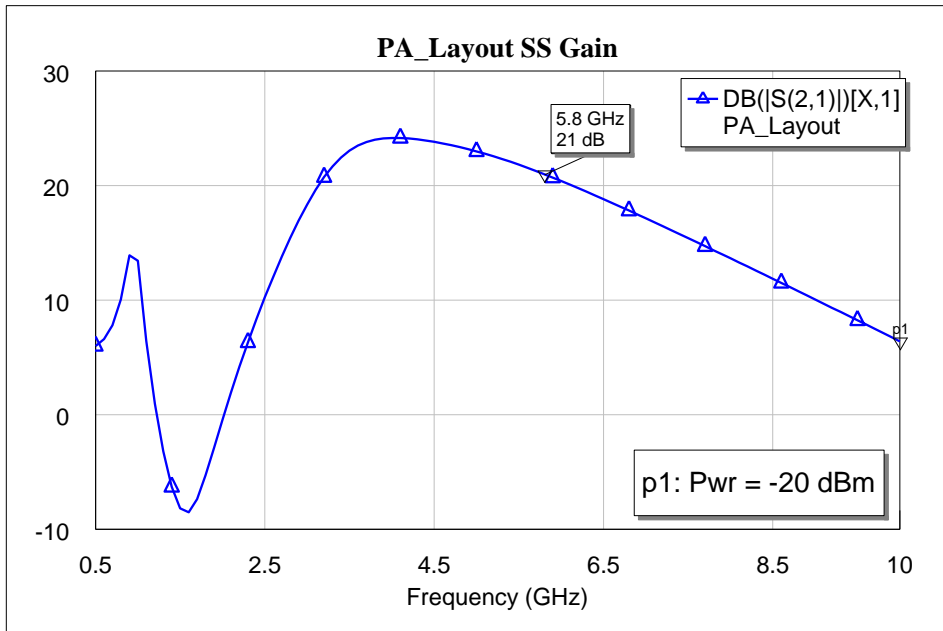


Figure 5: Gain for Completed Power Amplifier

At 5.8GHz, the predicted P1dB power is 20.31dBm at an input power of 0.3203dBm. The P3dB power is 21.58dBm with an input power of 3.596dBm.

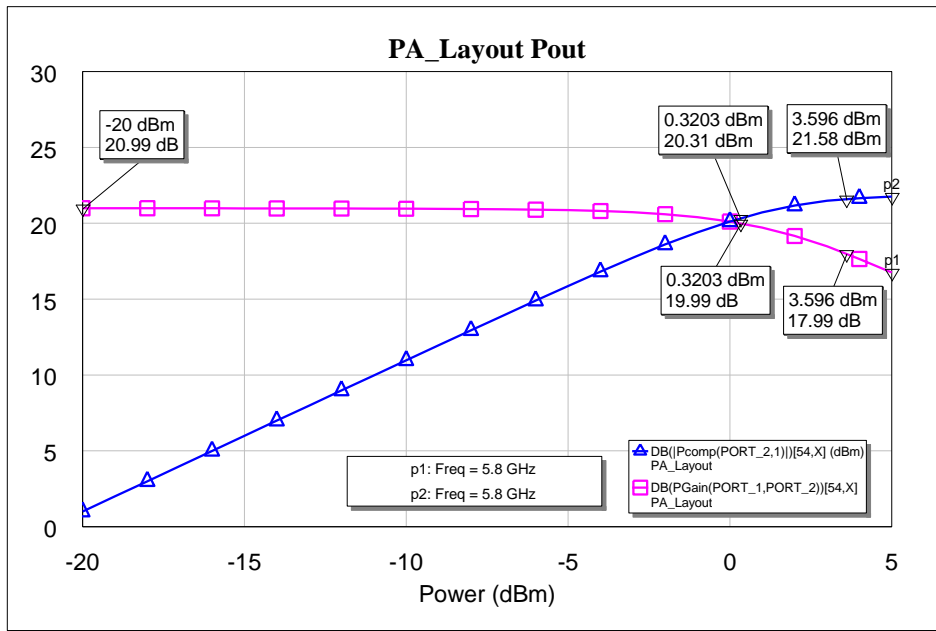


Figure 6: Output Power and Power Gain for Completed Power Amplifier

The PAE of the completed amplifier is 33.66% at the P1dB power and 41.83% at the P3dB power.

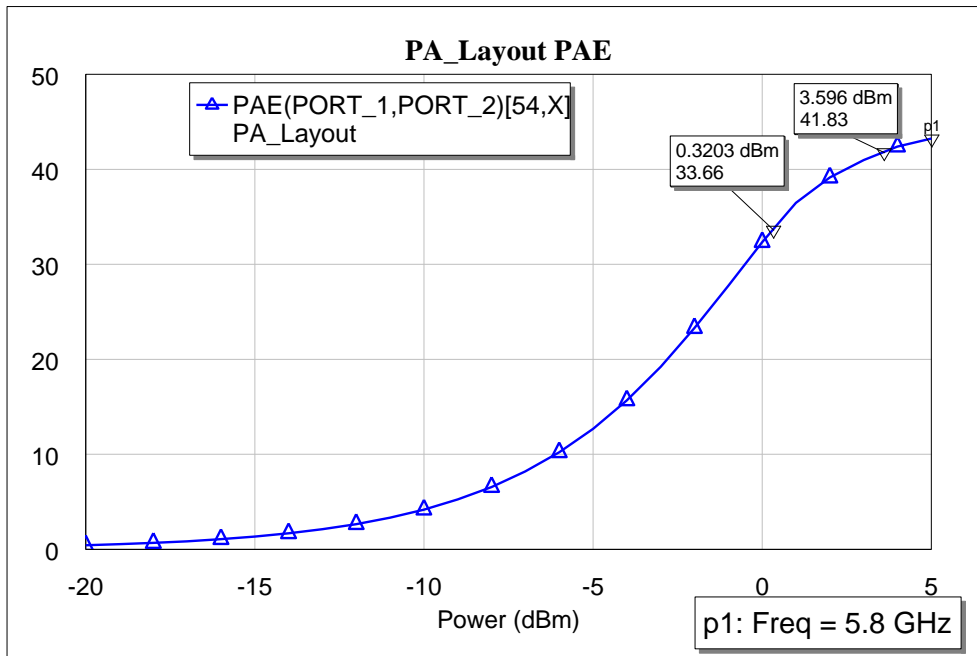


Figure 7: PAE for Completed Power Amplifier

The stability of the overall amplifier is given below. It appears to be stable over all frequencies.

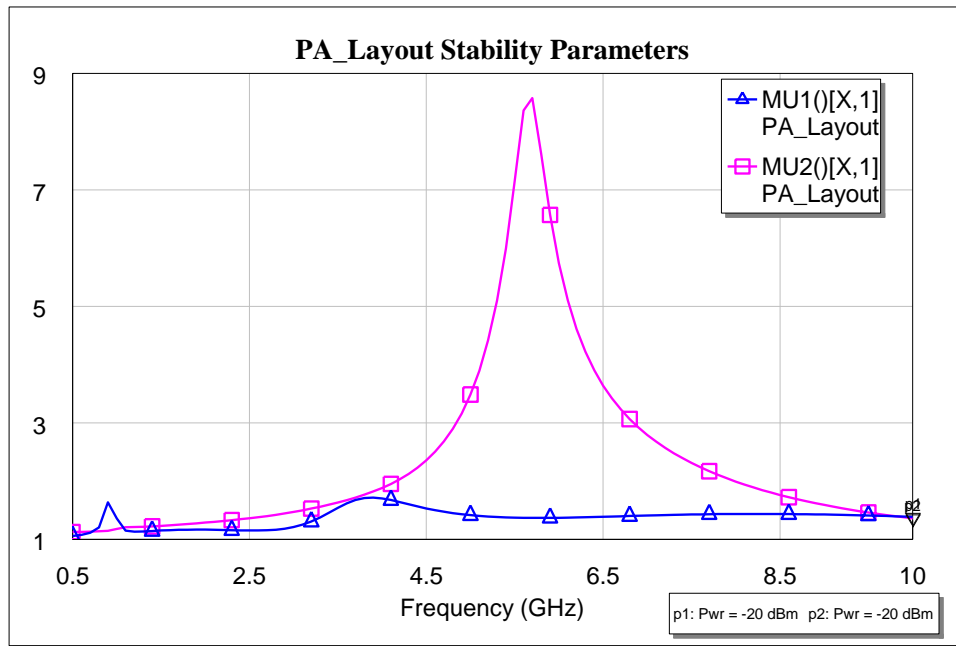


Figure 8: Stability Parameters for Completed Power Amplifier

SCHEMATIC

Below is the overall circuit schematic. The schematic has been annotated to point out certain circuitry and show the anticipated DC voltages and currents.

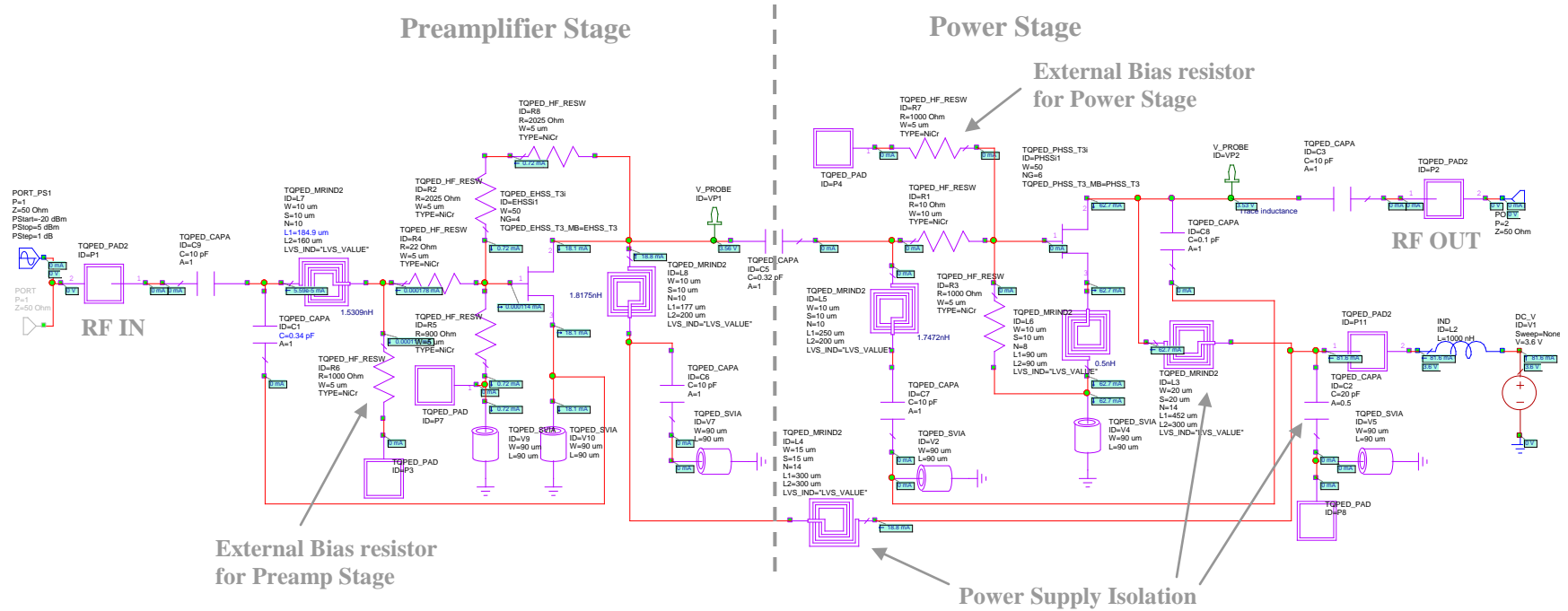


Figure 9: Schematic for Completed Power Amplifier

LAYOUT

The layout for the completed power amplifier is shown below. The pads are labeled.

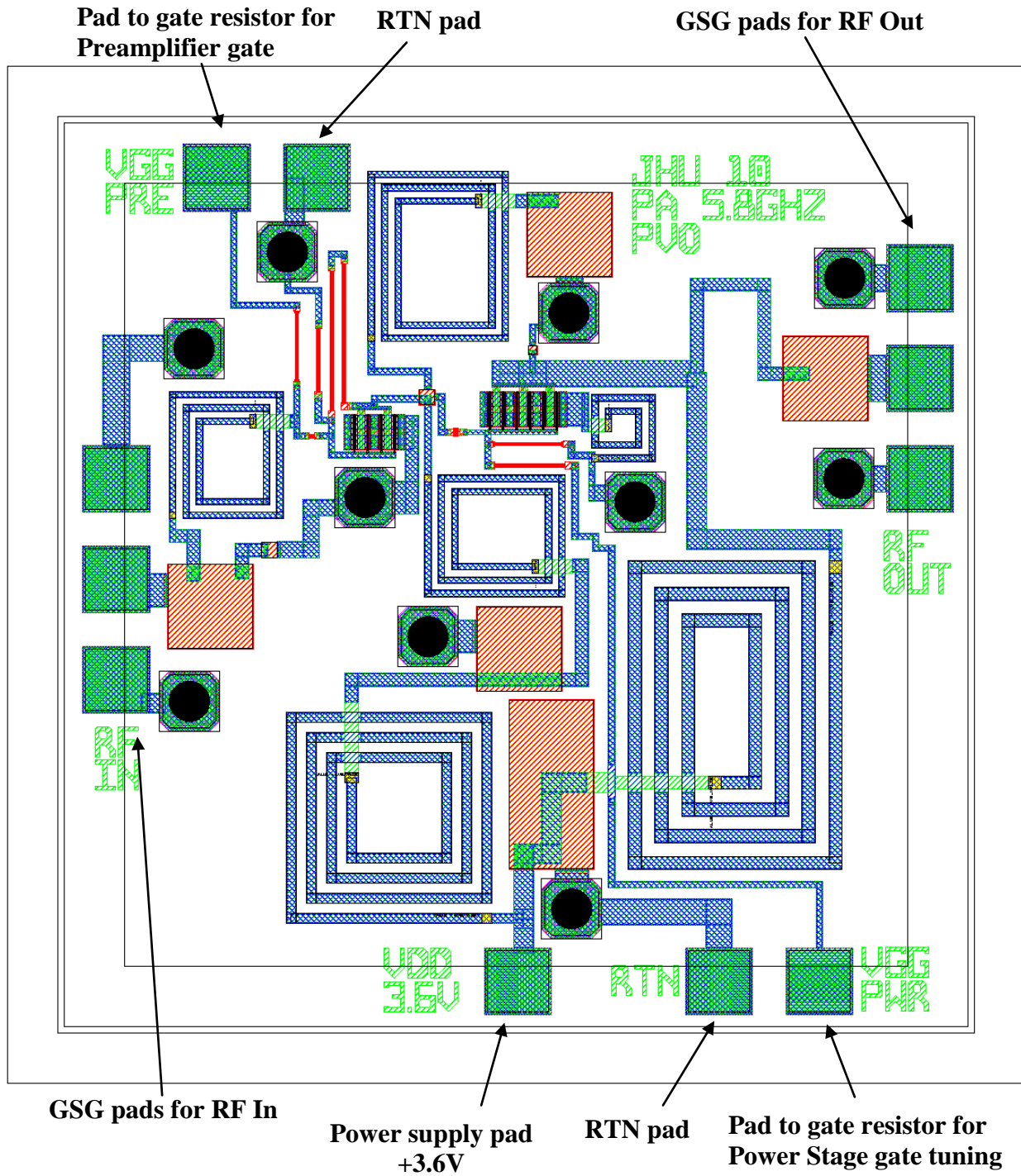


Figure 10: Completed Power Amplifier Layout

TEST PLAN

Test Equipment

The following test equipment will be required to test this power amplifier:

- Three DC Power Supplies capable of providing up to 5V and 100mA
- RF Signal Generator
- Network Analyzer
- Spectrum Analyzer
- Wafer Probe Station with DC Probes
- RF Cables
- Digital Multimeter

Test 1: DC Biasing

The purpose of this test is to examine the DC bias of the devices.

- 1) Connect the positive terminal of the DC power supply to the “VDD 3.6V” pad on the chip and the negative terminal to the “RTN” pad or chip substrate.
- 2) Slowly increase the voltage to 3.6V, being careful to stop if it appears that currents are being drawn which are higher than anticipated. The expected DC current draw is 81.5mA, with 62.7mA for the power stage and 18.9mA for the preamplifier stage.
- 3) If the DC current is not as anticipated, or if time allows, inspect and adjust the current drawn by the preamplifier stage following these steps:
 - a. Turn off the 3.6V power supply.
 - b. Connect probes to the “VGG PRE” and “VGG PWR” pads on the chip.
 - c. Pinch off the power stage by applying -1V to the “VGG PWR” pad on the chip.
 - d. Turn on the 3.6V power supply and observe the current drawn from the supply.
 - e. Adjust the bias voltage for the preamp stage by applying the appropriate voltage to the “VGG PRE” pad until the current draw is approximately 18.9mA.
- 4) If the DC current is still not as anticipated, and if time still allows, inspect and adjust the current drawn by the power stage following these steps:
 - a. Pinch off the preamplifier stage by applying less than -0.9V to the “VGG PWR” pad on the chip. Although this is an Enhancement mode device which requires only 0V at the gate for pinchoff, the resistor divider that biases the gate necessitates that a negative voltage be applied to the external bias gate resistor to achieve 0V at the gate of the actual device.
 - b. Turn on the 3.6V power supply and observe the current drawn from the supply.
 - c. Adjust the voltage for the preamp stage by applying the appropriate voltage to the “VGG PWR” pad until the current draw is approximately 62.7mA
- 5) Set the appropriate bias tuning voltages recorded in steps 3 and 4 and record the overall DC current draw. Use these bias tuning voltages for the remaining tests.

Test 2: S-Parameter Measurements

This test will examine the small signal parameters of the power amplifier.

- 1) Calibrate the network analyzer from 0.5GHz to 10GHz using the proper calibration standards. Include all RF cables in the calibration.
- 2) Place the input RF probe on the chip pads labeled “RF IN”.
- 3) Place the output RF probe on the chip pads labeled “RF OUT”.
- 4) Turn on the DC power supply and adjust its voltage to 3.6V.
- 5) Apply any bias tuning voltages recorded in Test 1. Record the current drawn from the 3.6V power supply.
- 6) Perform an S-Parameter test (s_{11} , s_{12} , s_{21} , s_{22}) using the network analyzer. Record all measurements. Save Network Analyzer plots in an s2p format for later review.

Test 3: Power Measurements

This test will examine the output power performance of the power amplifier.

- 1) Record the insertion loss of the RF cables used in this test.
- 2) Connect the RF Signal Generator to the RF input of the chip by connecting the input RF probe to the chip pads labeled “RF IN”.
- 3) Connect the RF Spectrum Analyzer to the RF output of the chip by connecting the output RF probe to the chip pads labeled “RF OUT”.
- 4) Turn on the DC power supply and adjust its voltage to 3.6V.
- 5) Apply any bias tuning voltages recorded in Test 1. Record the current drawn from the 3.6V power supply.
- 6) Set the RF Source to a frequency of 5.8GHz and an output power of -15dBm.
- 7) Configure the Spectrum Analyzer to display the output power of the amplifier at 5.8GHz.
- 8) Turn on the RF source and record the power coming out of the power amplifier. Increase the power from the RF source in ~1 dBm steps until the power amplifier has compressed or the input power has reached 5dBm. Record the DC current from the power supply at every RF input power step.
- 9) If time permits, configure the Spectrum Analyzer to provide the power of the 2nd (11.6GHz) and 3rd (17.4GHz) harmonics at the 1dB and 3dB compression levels.
- 10) If time still remains, re-run steps 6 through 9 at RF frequencies of 5.725GHz and 5.875GHz. Also, consider testing at different DC supply voltages to determine design robustness.

SUMMARY & CONCLUSIONS

The following table documents the design goals and predicted performance for this power amplifier.

Parameter	Design Goal	Predicted Results		
Operating Frequency (GHz)	5.725 – 5.875	5.725	5.8	5.875
Small Signal Gain (dB)	> 20	21.21	21.0	20.78
Output Power at P1dB (dBm)	> 20	20.31	20.31	20.31
PAE at P1dB (%)	> 30	33.71	33.66	33.59
Input Match (dB)	< -15	-39.51	-61.64	-39.21
Output Match (dB)	< -6	-3.2	-3.2	-3.2
Drain Voltage	3.6V	3.6V		
Chip Area (L x W)	0.06” x 0.06”	0.06” x 0.06”		

Table 4: Power Amplifier Design Goals & Predicted Results

In all, the design performs fairly well against the design goals. There is sufficient gain and output power across the bandwidth. The input match is excellent, and the PAE is adequate at the P1dB power. The PAE at the P3dB power is even better, and future work should investigate the highest compression point and PAE achievable with this design. Also, future investigations should examine the power amplifier’s performance at lower DC voltages (simulating the decay of a handheld device battery) and changes due to processing variations (capacitance, resistance, device size, etc.).

The only deficient parameter is that the output match is fairly poor. Were more design time available, the output matching circuit could be examined to determine if there is a matching point which would allow sufficient output power and gain while still improving the output match. Also, although the predicted output power is greater than the design goal, it was generated using the TOM3 model, which is known to over-predict the output power. The TOM4 model was attempted for this design, but convergence issues prevented its use. As such, the actual output power of this amplifier may not exceed the design goal.

APPENDIX

The following sections include additional resources to describe the design of this power amplifier.

Additional Power Stage Design Details

The power stage was designed to be a Class A amplifier capable of providing 20dBm of output power. A standard $6 \times 50 \mu\text{m}$ depletion mode device was chosen for this stage. Lacking Load Pull data, the Cripps approach was used to design the device's output matching network for the appropriate output power. As shown in the IV curves below, we expect to bias the device at I_{dss} ($\sim 65\text{mA}$). With a 3.6V drain, we would roughly expect 19.5dBm of output power for this load line ($118\text{mA} * 3.6\text{V} / 8 = 88.5\text{mW} = 19.5\text{dBm}$).

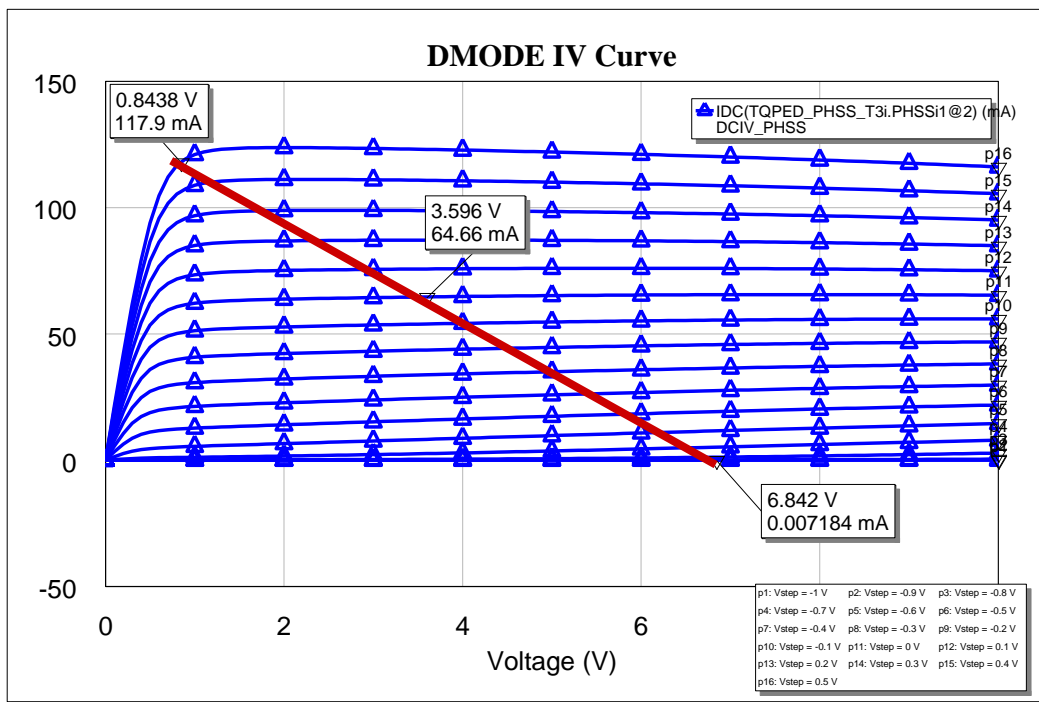


Figure 11: Power Amplifier Stage IV Curves with Load Line

The output matching network for this amplifier was designed for this load line ($6\text{V} / 118\text{mA} = 50.85\Omega$) and maximum output power. Since the device is biased at I_{dss} , the biasing network is simply a $1\text{k}\Omega$ pull-down resistor. Figures 12 and 13 show the ideal and TriQuint implementation of the amplifier. A source inductor is used to improve stability, although at the sacrifice of gain.

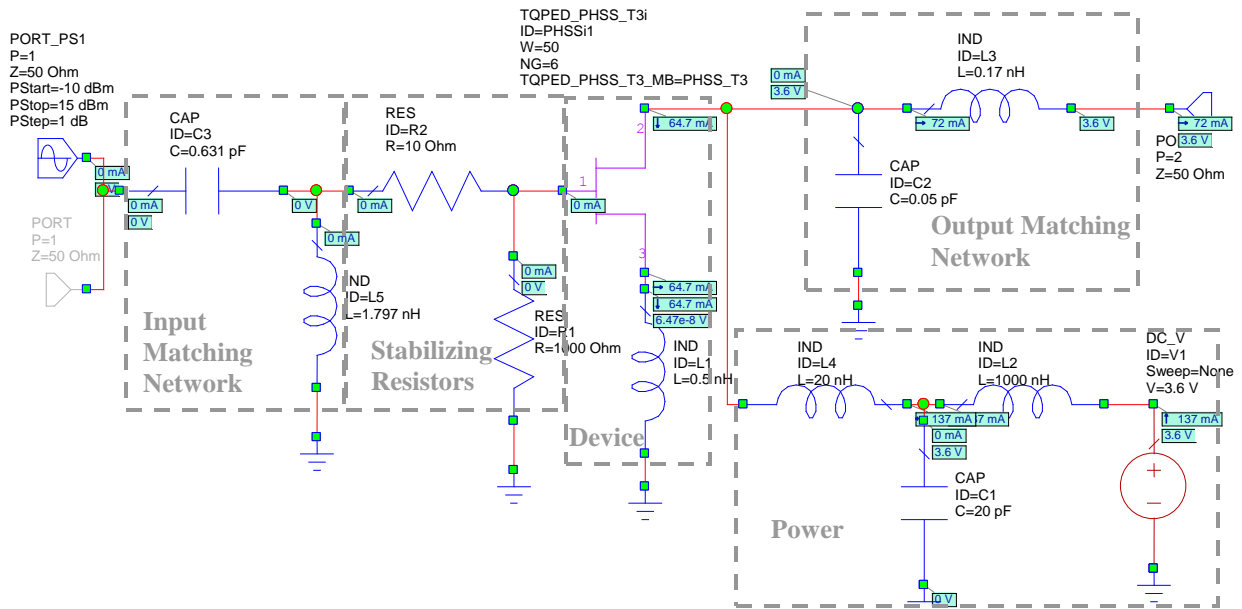


Figure 12: Power Amplifier Stage Schematic with Ideal Components

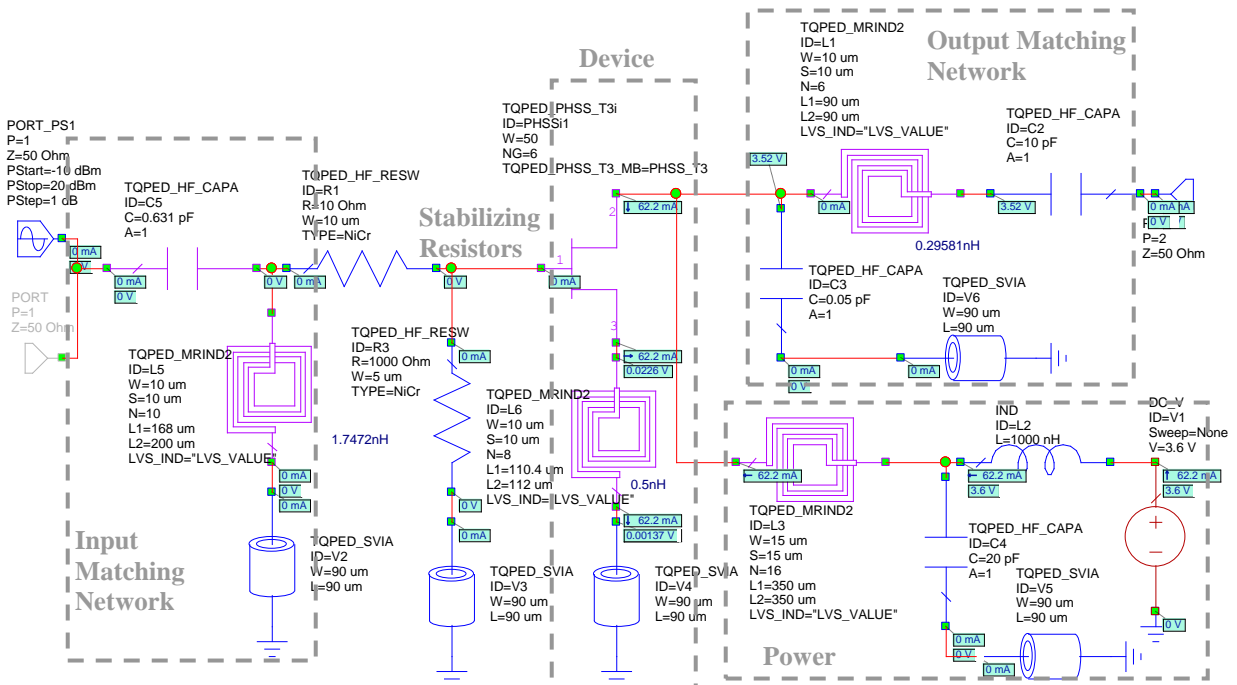


Figure 13: Power Amplifier Stage Schematic with TriQuint Components

The figures below show the power amplifier stage performance based on the AWR simulations.

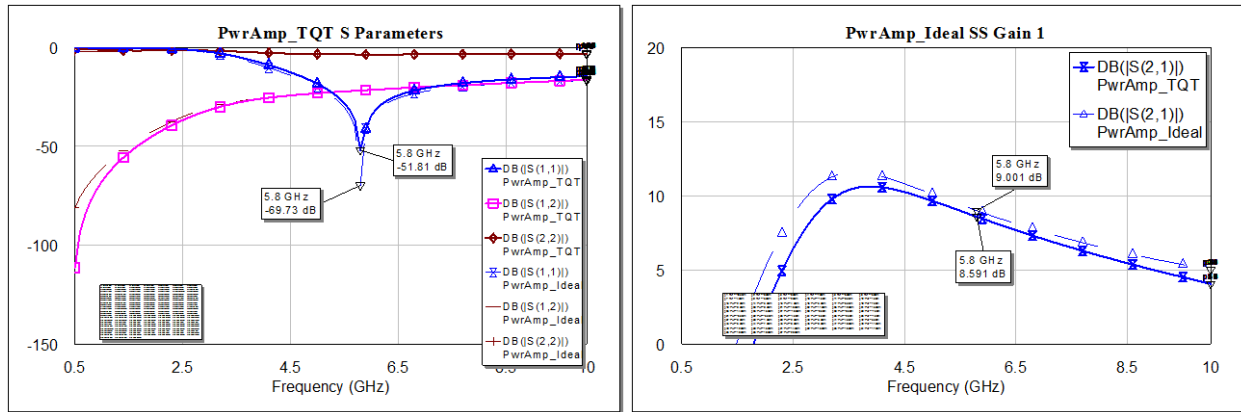


Figure 14: S Parameters for Ideal and TriQuint Implementations of Power Amplifier Stage

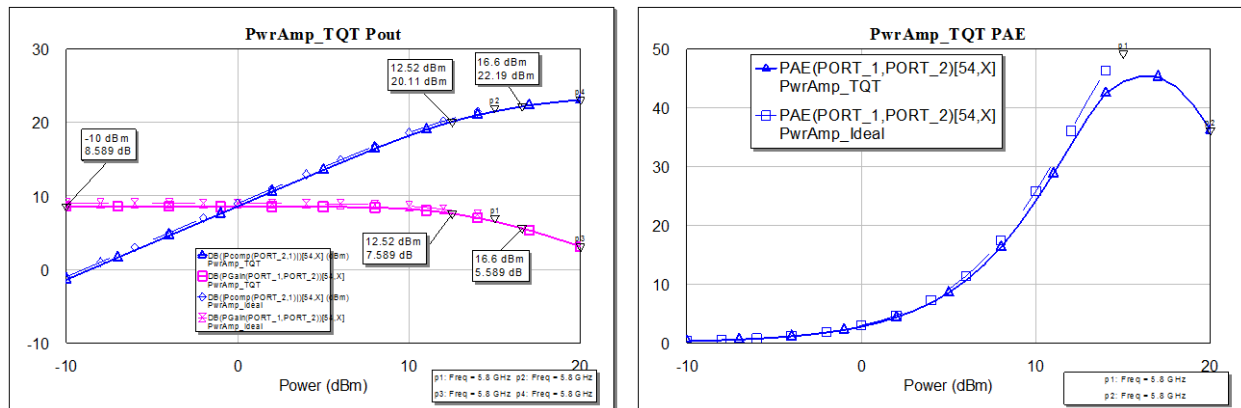


Figure 15: Power and PAE for Ideal and TriQuint Implementations of Power Amplifier Stage

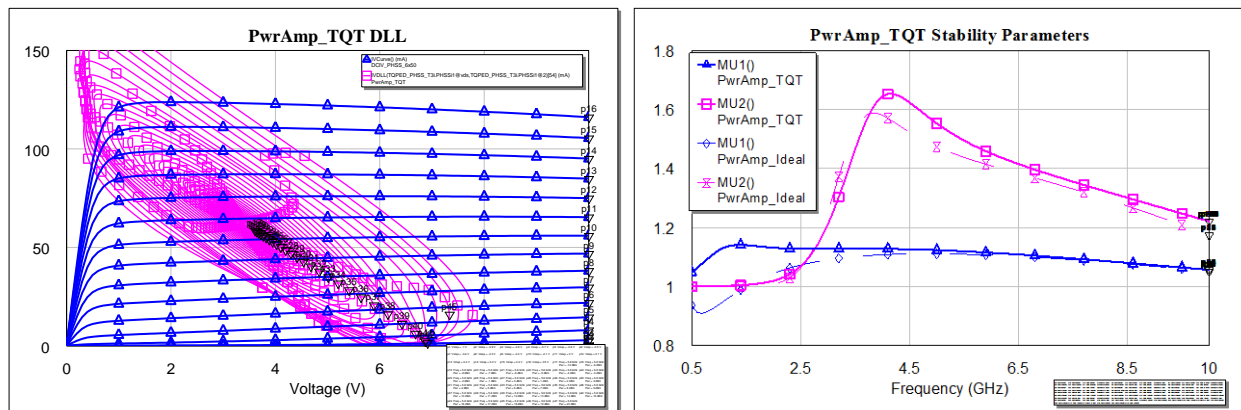


Figure 16: DLL and Stability for Ideal and TriQuint Implementations of Power Amplifier Stage

The performance characteristics are summarized in the table below.

Parameter	Ideal	TriQuint
Small Signal Gain	9db	8.591dB
Output Power at P1dB	20.57dBm	20.11dBm
PAE at P1dB	39.14%	36.13%

Table 5: Power Amplifier Stage Performance

We note that the Dynamic Load Line shows very linear Class A operation. This gives us confidence that the output matching network and biasing were designed appropriately. Additionally, the stability of this stage seems to be acceptable across the frequencies of interest. The implementation using TriQuint elements appears to be stable over all frequencies, although lower frequencies may be of concern.

Additional Preamplifier Stage Design Details

Given the performance of the power amplifier stage, the requirements for the preamplifier stage become apparent. In order to achieve 20dB overall gain, the preamplifier must have more than ~12dB of gain. Also, the preamplifier must be able to provide up to ~12dBm at its P_{1dB} point to prevent it from going into compression before the power stage. For this stage, a 4x50μm Enhancement mode device was chosen. The load line design is shown in the figure below.

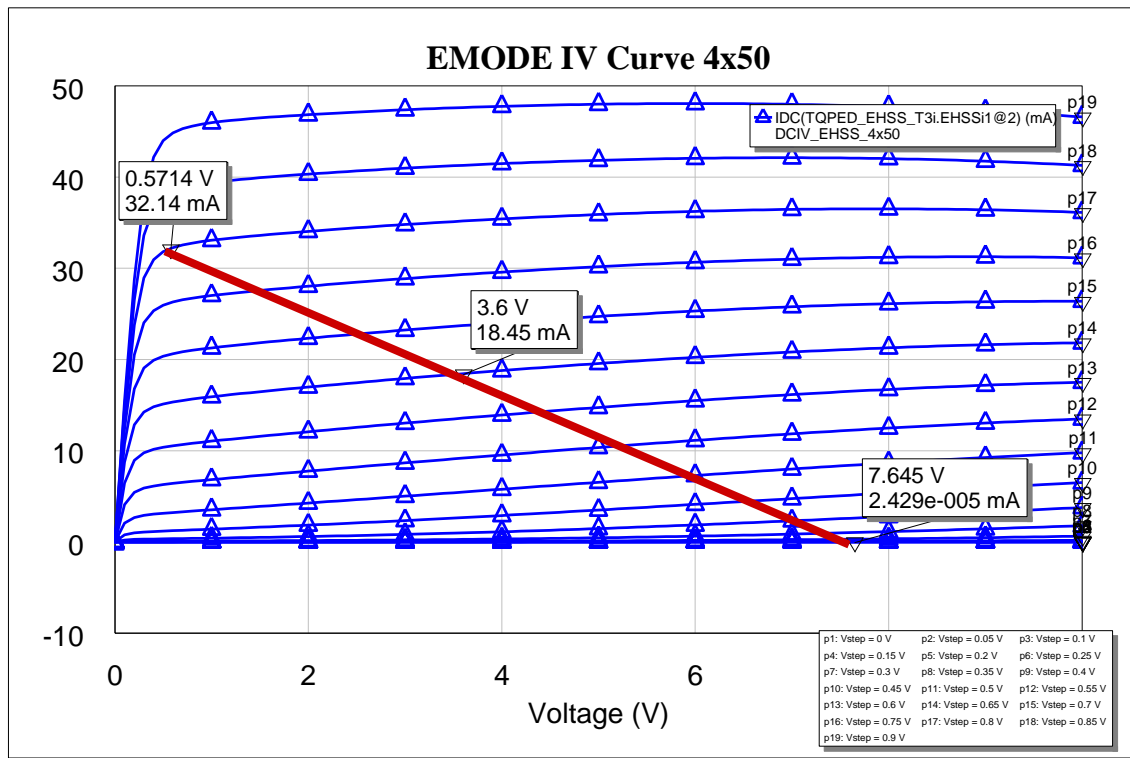


Figure 17: Preamplifier Stage IV Curves with Load Line

This load line predicts an output power of 14.5dBm ($7.07V * 32mA / 8 = 28.3mW = 14.5dBm$), which should be sufficient for the preamplifier. The load line resistance is 221Ω ($7.07V / 32mA$), which was used for the Cripps method for designing the output matching network. This will require the gate of the device to be biased at +0.65V, which can be achieved using a simple resistor divider with the drain voltage.

Since the output power was more than sufficient for this preamplifier, it was possible to negotiate the power for more gain. The figure below shows the maximum gain circles relative to the maximum output power impedance. Also shown is the impedance of the output matching network, which is between the two.

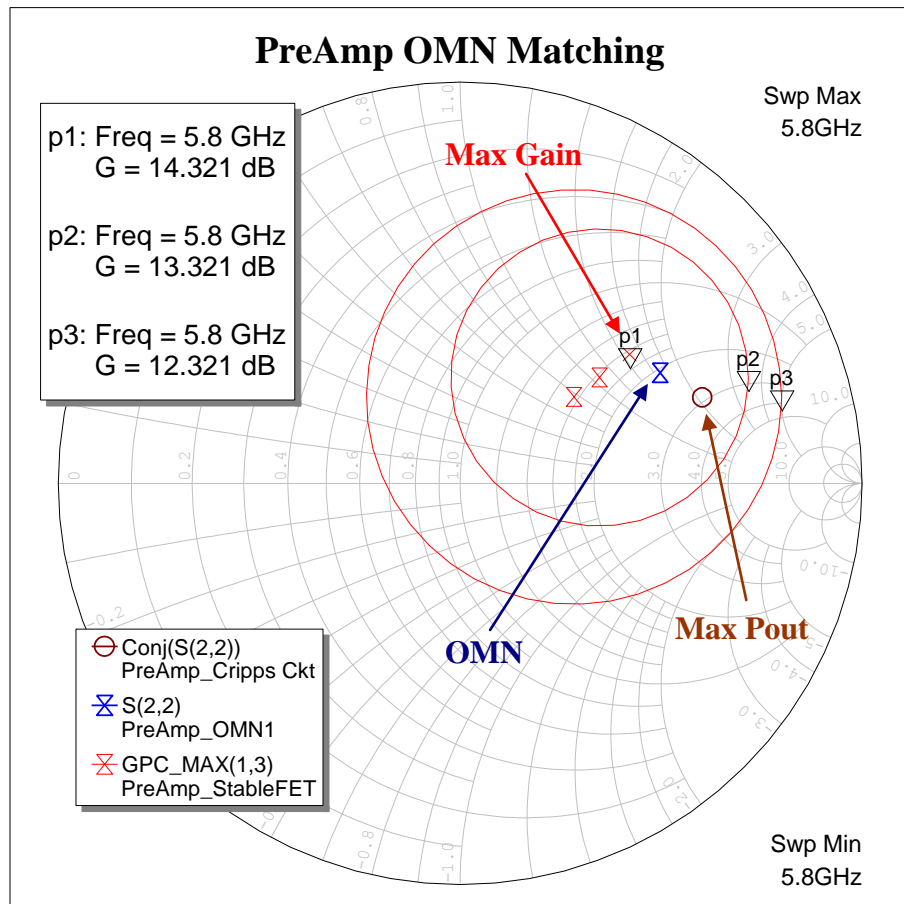


Figure 18: Max Gain, Output Power and Output Matching Network Impedances

The schematics for the preamplifier using ideal and TriQuint elements are given below.

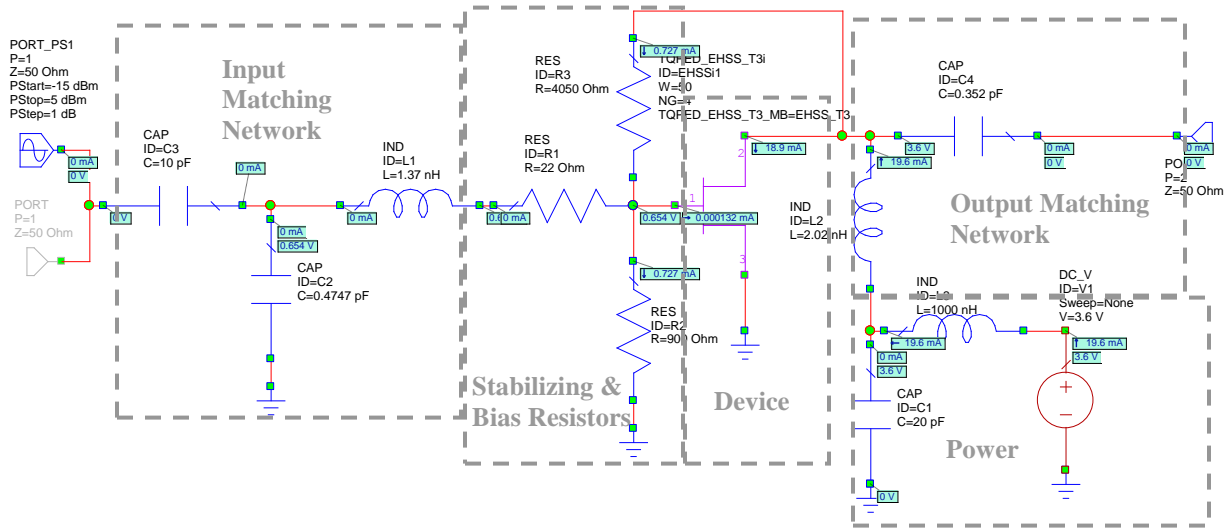


Figure 19: Preamplifier Stage Schematic with Ideal Components

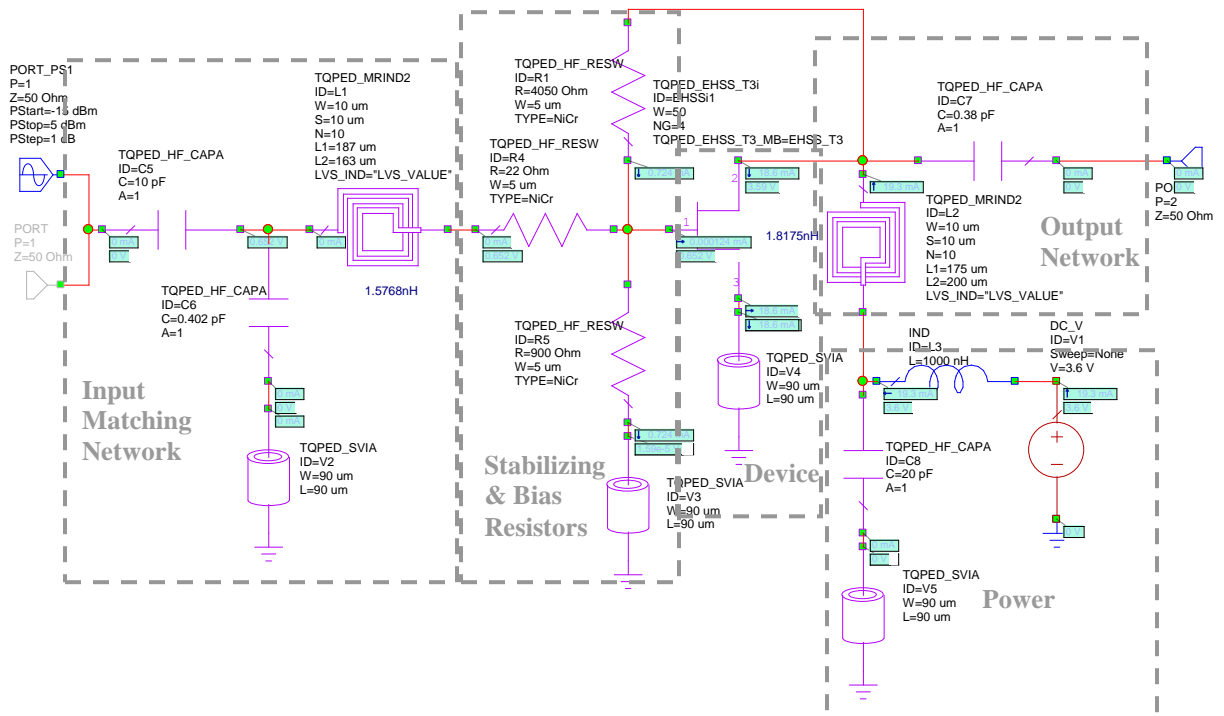


Figure 20: Preamplifier Stage Schematic with TriQuint Components

The figures below show the preamplifier stage performance based on the AWR simulations.

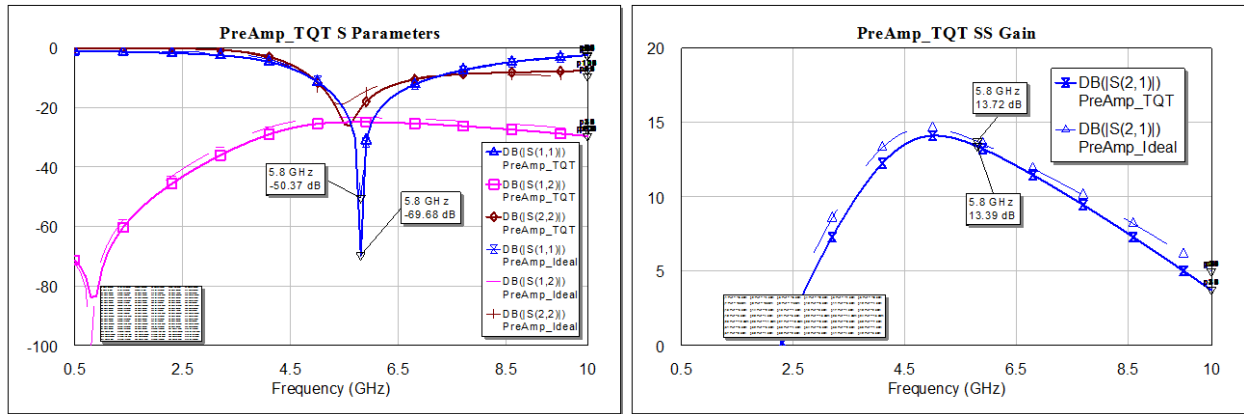


Figure 21: S Parameters for Ideal and TriQuint Implementations of Preamplifier Stage

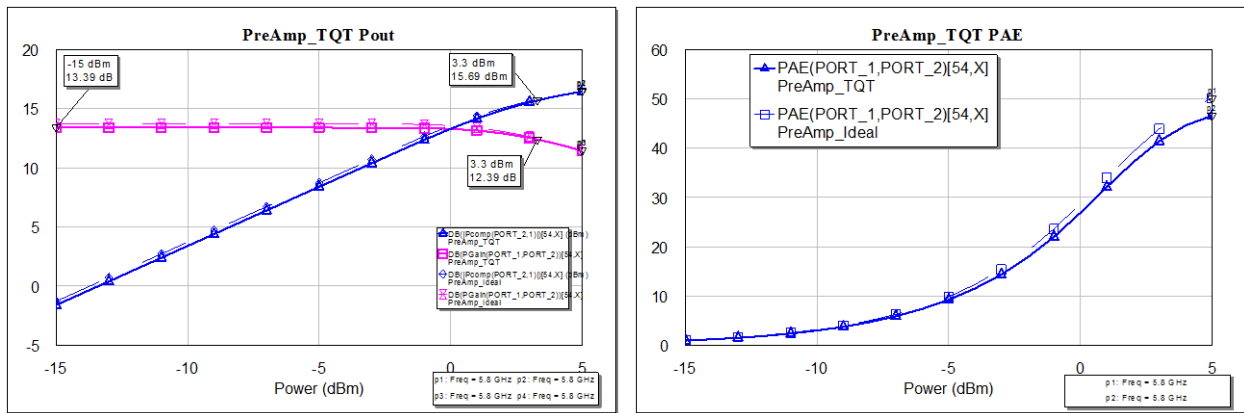


Figure 22: Power and PAE for Ideal and TriQuint Implementations of Power Amplifier Stage

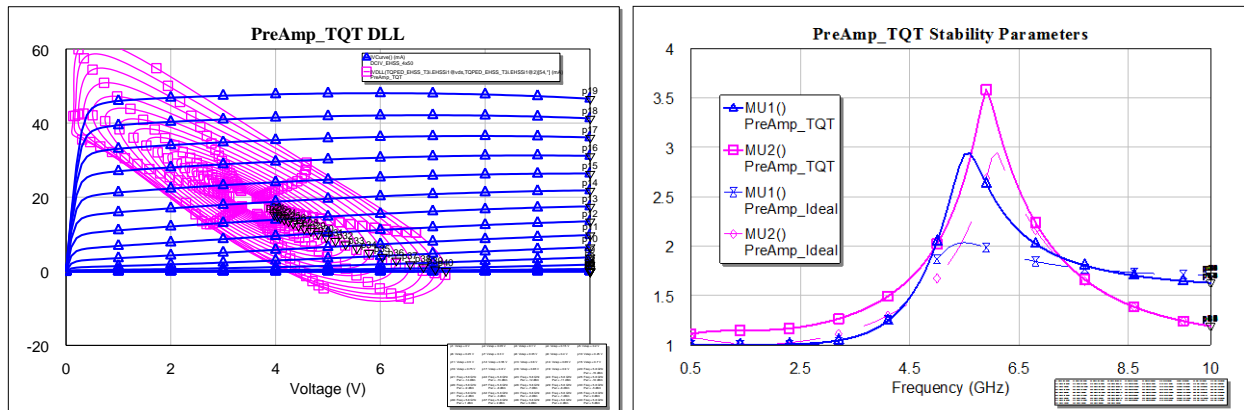


Figure 23: DLL and Stability for Ideal and TriQuint Implementations of Power Amplifier Stage

The performance characteristics are summarized in the table below.

Parameter	Ideal	TriQuint
Small Signal Gain	13.72dB	13.39dB
Output Power at P1dB	15.55dBm	15.69dBm
PAE at P1dB	43.11%	42.38%

Table 6: Power Amplifier Stage Performance

As with the power amplifier stage, the dynamic load line shows very good Class A operation. The stability is adequate at the frequencies of interest, although low frequency stability is marginal.

Additional Combined Power Amplifier Design Details

Cascading both amplifier stages would imply a gain of 21.98dB (13.39dB + 8.59dB) and an output power of 20.11dBm. Cascading the two stages is relatively straightforward since a series capacitor is the last element on the preamplifier's output matching network and the first element in the power amplifier's input matching network.

To maintain the simplicity of this design, it was decided that both amplifier stages will use a single supply. Inductors and a large capacitor were added to isolate the stages from the supply and each other, as shown below.

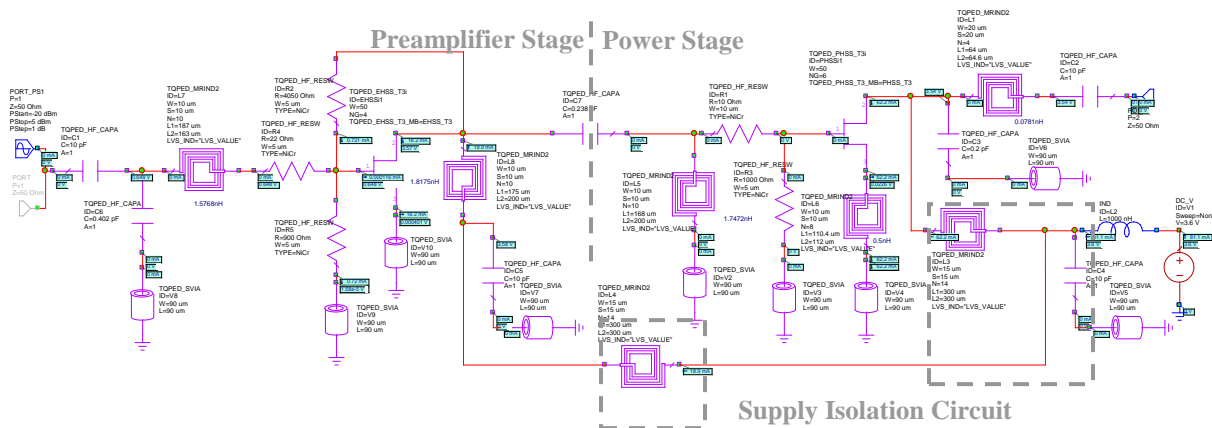


Figure 24: Preliminary Combined Power Amplifier Schematic

The performance of this amplifier is shown below. It is interesting to note that noticeable gain has appeared at lower frequencies due to the power supply interconnection.

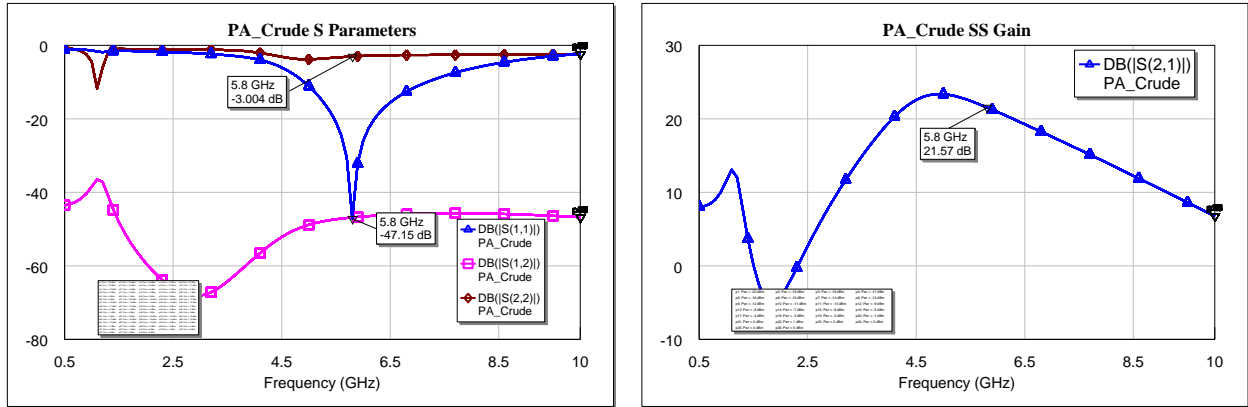


Figure 25: S Parameters for Preliminary Power Amplifier

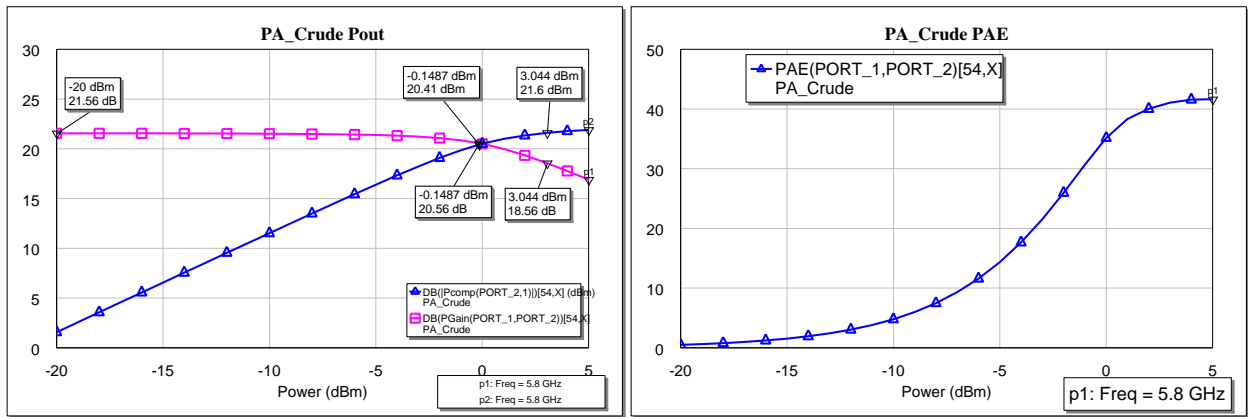


Figure 26: Power and PAE for Preliminary Power Amplifier, 5.8GHz

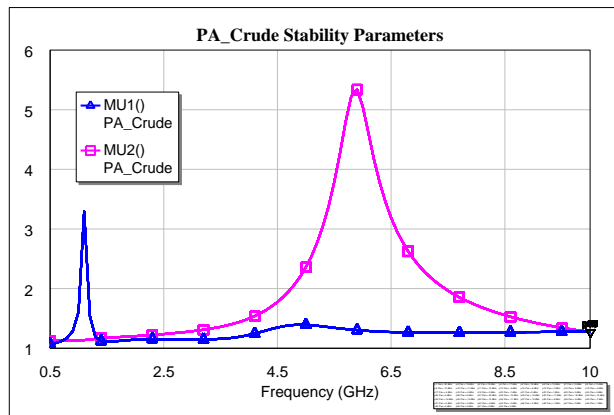


Figure 27: Stability Parameters for Preliminary Power Amplifier

The gain is slightly lower and output power is slightly higher than would be expected by cascading the individual stages. That is because the output matching network has been modified to increase output power at the cost of gain. The above results do not account for the losses and re-tuning that is associated with the layout of the amplifier.

Additional Simulation Results for Completed Power Amplifier

Below are the predicted output voltage waveforms for different values of input power. The P1dB and P3dB waveforms are highlighted.

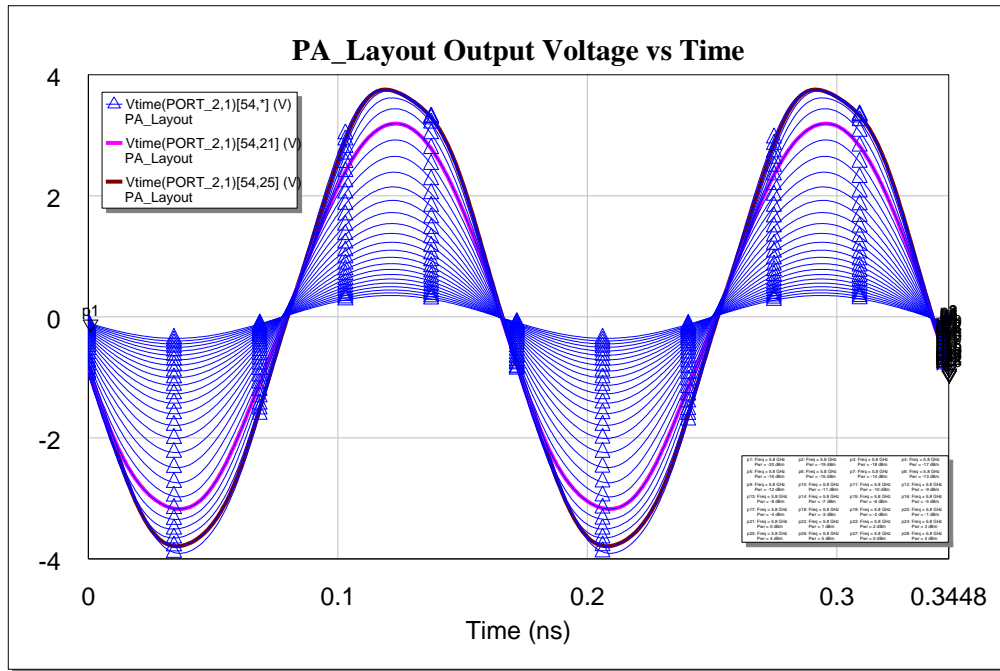


Figure 28: Output Voltage Waveforms for Completed Power Amplifier, 5.8GHz

The amplitudes of the voltage harmonics are given below. Note that the highly linear operation of the Class A amplifier results in very low amplitude harmonics.

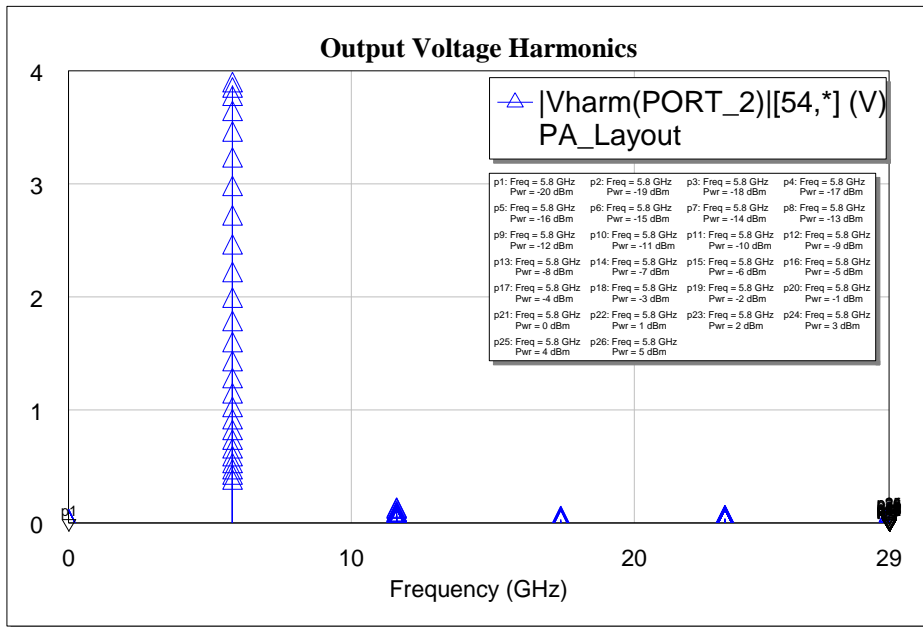


Figure 29: Output Voltage Amplitudes of Harmonics for Completed Power Amplifier, 5.8GHz

The powers of the fundamental, 2nd and 3rd harmonics are given below. Note that the highly linear operation of the Class A amplifier results in harmonics with very little power.

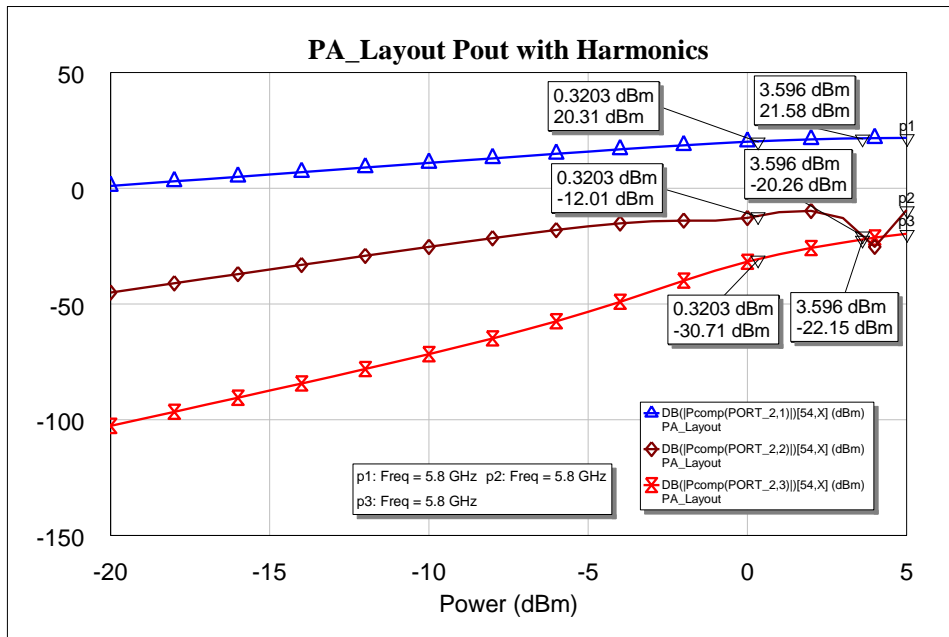


Figure 30: Output Power of Harmonics for Completed Power Amplifier, 5.8GHz

The plots below show the predicted S-Parameters over the amplifier's bandwidth.

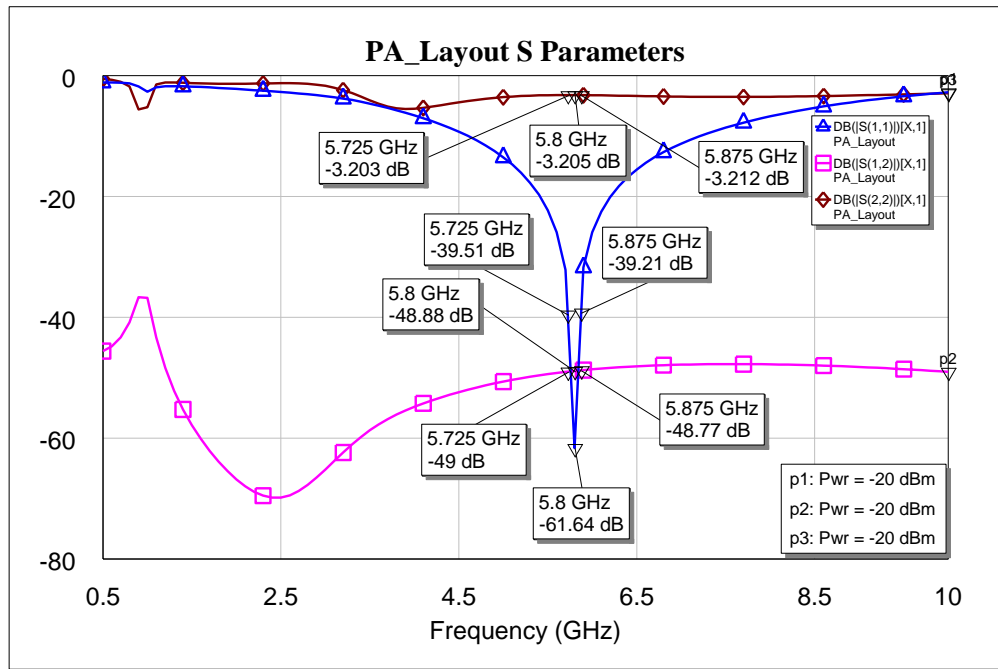


Figure 31: S-Parameters for Completed Power Amplifier

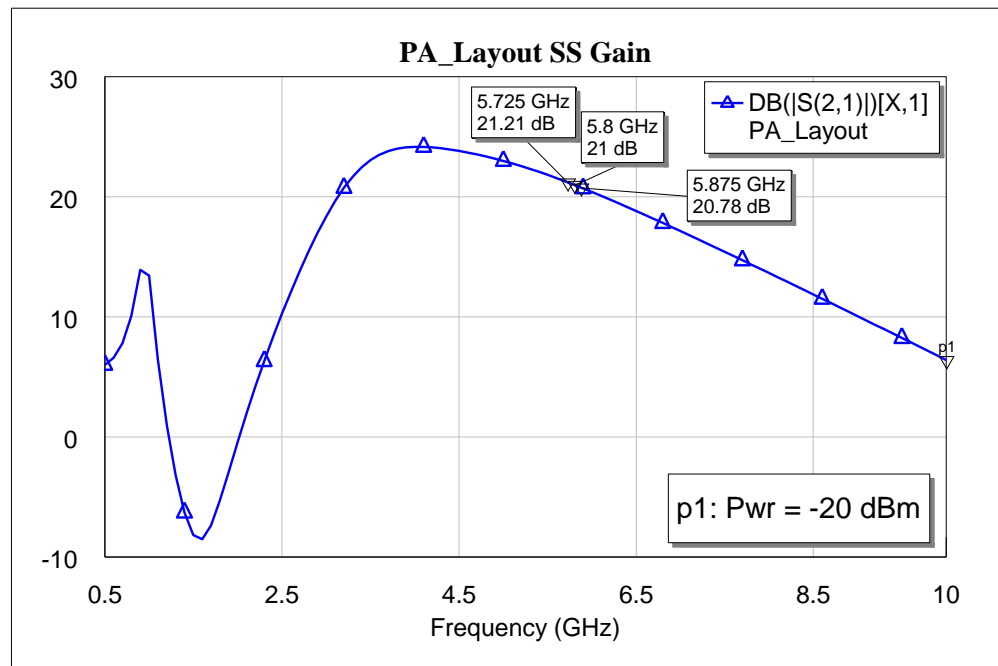


Figure 32: S-Parameters for Completed Power Amplifier

The two plots below show output power, power gain and PAE of the completed amplifier at 5.725GHz

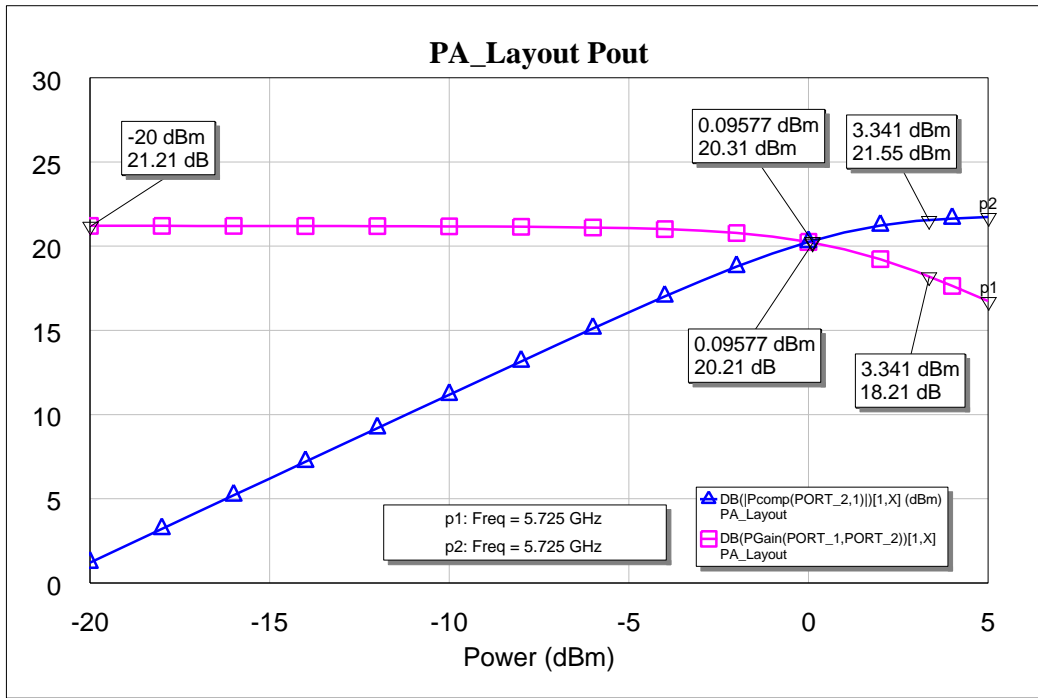


Figure 33: Output Power and Power Gain for Completed Power Amplifier, 5.725GHz

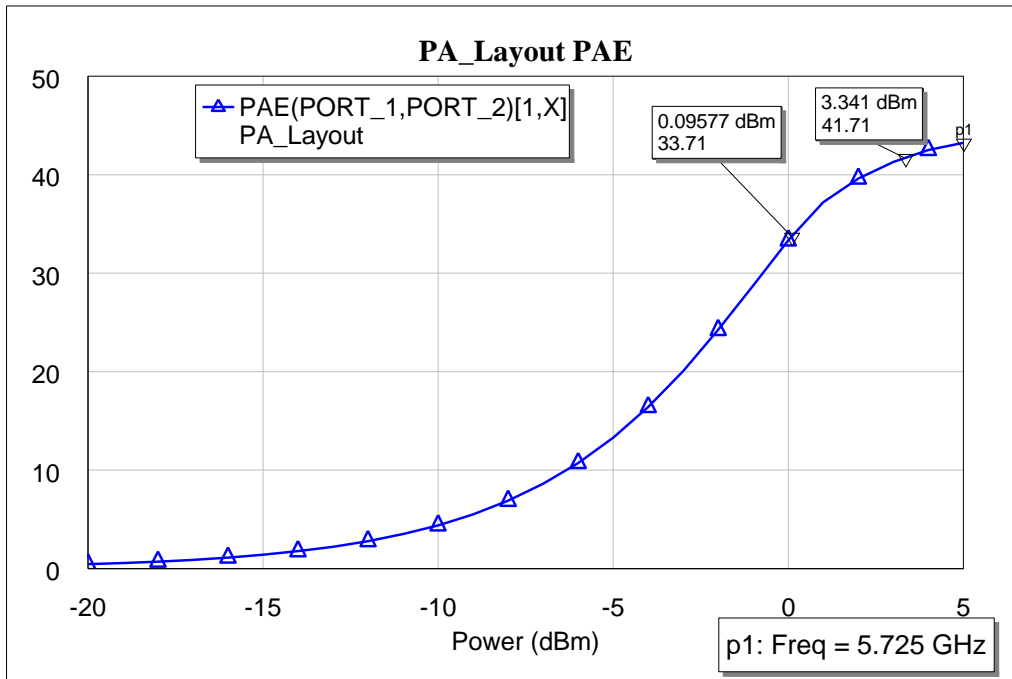


Figure 34: PAE for Completed Power Amplifier, 5.725GHz

The two plots below show output power, power gain and PAE of the completed amplifier at 5.875GHz

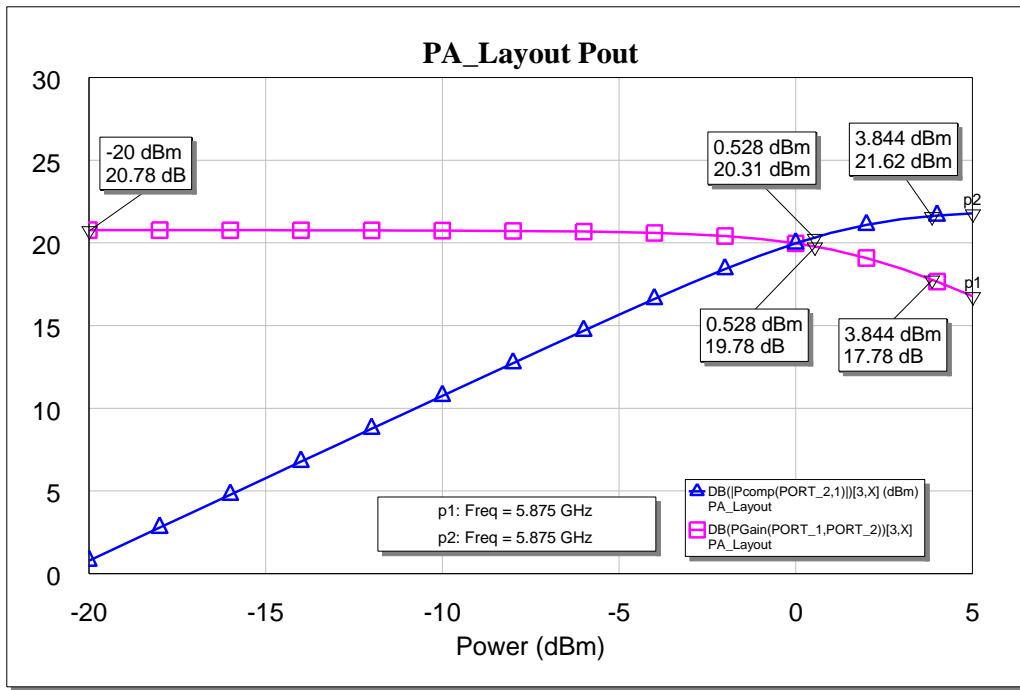


Figure 35: Output Power and Power Gain for Completed Power Amplifier, 5.875GHz

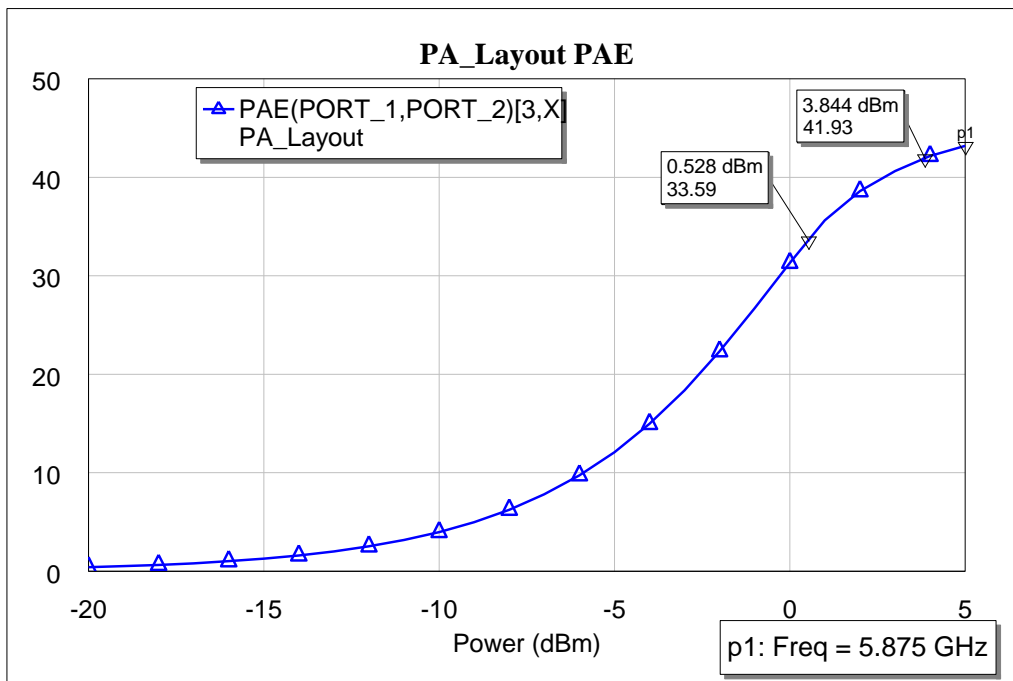


Figure 36: PAE for Completed Power Amplifier, 5.875GHz

Additional Layout Details

Below are additional details of the layout of the power amplifier,

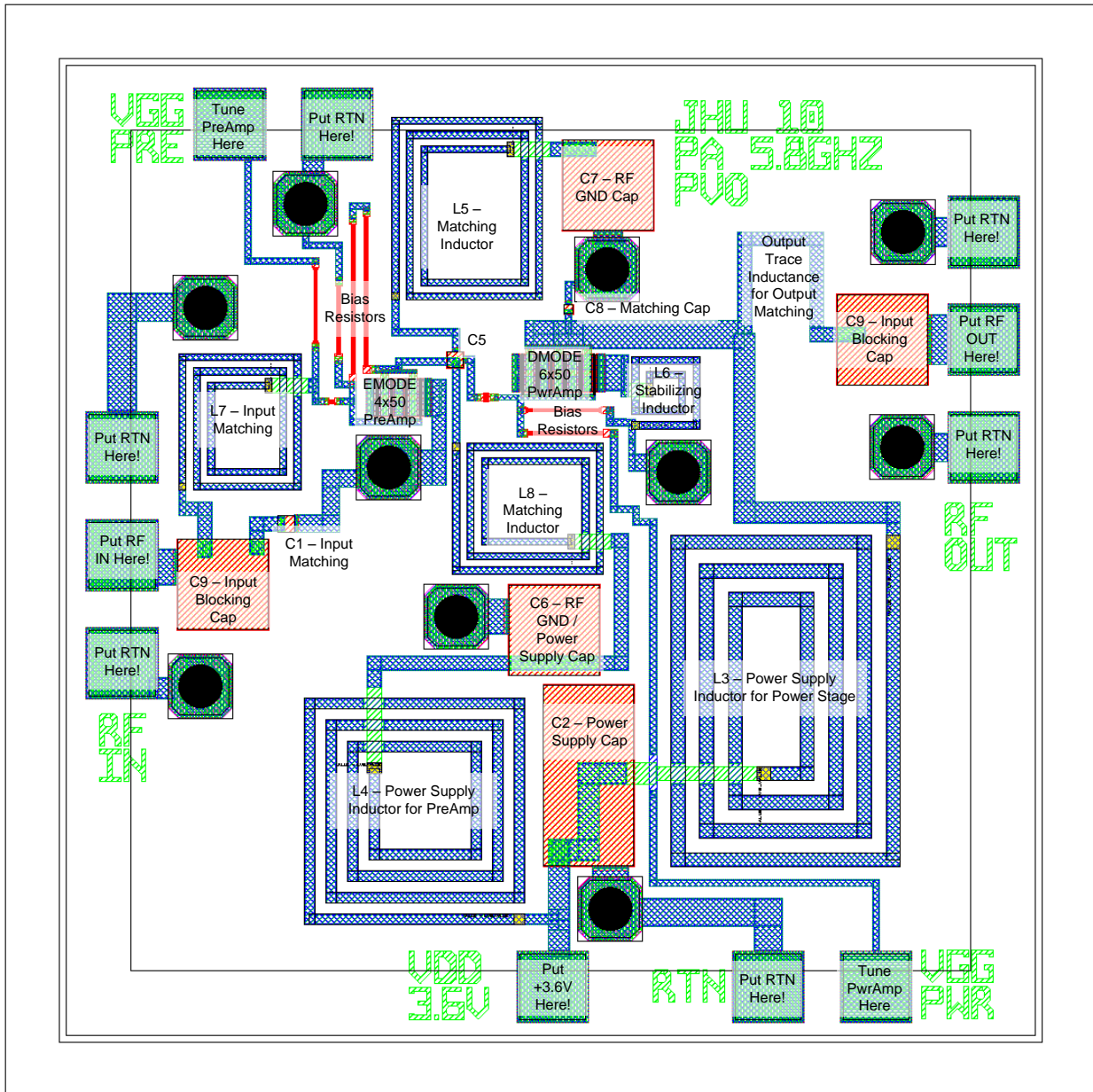


Figure 37: Annotated Layout of Completed Power Amplifier

Below is an isometric view of the power amplifier layout.

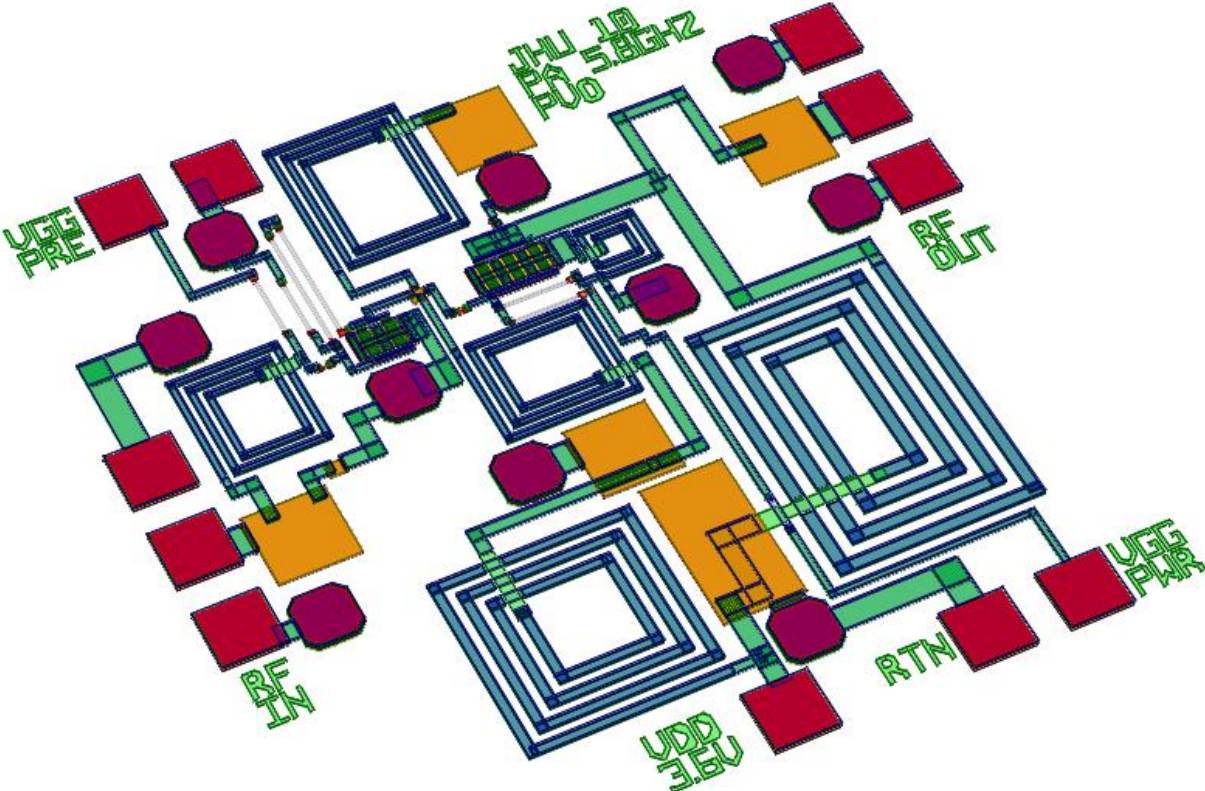


Figure 38: Isometric View of Completed Power Amplifier

Test Plan Datasheets

Test #1: DC Biasing

Step	Measurement	Value
2	Initial Combined DC Current @ 3.6V	
3d	Initial PreAmp DC Current @ 3.6V	
3e	Bias Tuned PreAmp DC Current @ 3.6V	
3e	Bias Tuning Voltage for PreAmp	
4b	Initial PwrAmp DC Current @ 3.6V	
4c	Bias Tuned PwrAmp DC Current @ 3.6V	
4c	Bias Tuning Voltage for PreAmp	
5	Bias Tuned Combined DC Current @ 3.6V	

Table 7: Data Table for Test #1: DC Biasing

Test #2: S-Parameter Measurements

DC Current @ 3.6V: _____

Frequency	S-Parameter	Value
5.725 GHz	S11	
5.725 GHz	S12	
5.725 GHz	S21	
5.725 GHz	S22	
5.8 GHz	S11	
5.8 GHz	S12	
5.8 GHz	S21	
5.8 GHz	S22	
5.875 GHz	S11	
5.875 GHz	S12	
5.875 GHz	S21	
5.875 GHz	S22	

Table 8: Data Table for Test #2: S-Parameter Measurements

Test #3: Power Measurements

Insertion Loss of RF IN Cable: _____

Insertion Loss of RF OUT Cable: _____

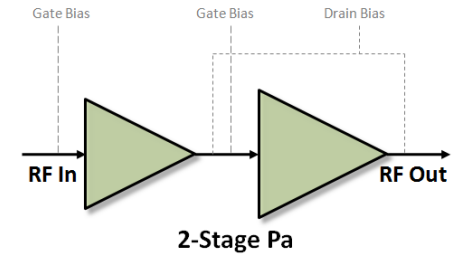
Record all power data in the table below. Adjust input and output powers for cable loss before calculating PAE.

2-Stage Power Amplifier Final Report

Mitch Flowers

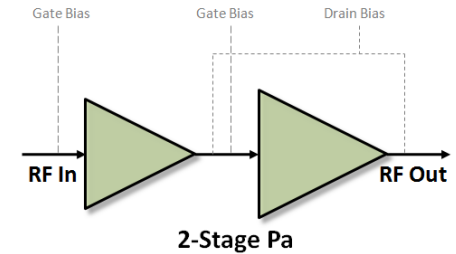
MMIC Design – Fall 2010

Abstract



- A high efficiency, two stage power amplifier putting out 20dBm at 50% PAE and targeting the 5.725 to 5.875 GHz ISM band, with a drain voltage of 3.6V and two independent gate voltages of -0.5V on the first and -0.95V on the second stages, and which fit into a 54x54 mil area, was designed into TriQuint Oregon's 0.5um pHEMT MMIC process.

Introduction



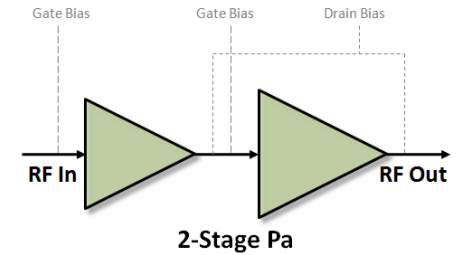
- **What the amplifier does:**

- Puts out 20dBm of power over 5.725 to 5.875 GHz at approximately 1dB compression.
- Achieves 50% PAE at 1dB compression point.
 - Achieves higher PAE at more compressed points.
- Works off of 3.6V drain supply and -0.5 and -0.95V gate supplies.
 - Both gate supplies required
- Requires approximately 0dBm in to achieve 1dB compression point
- Achieves 21 dB of small signal gain

- **Other amplifier details**

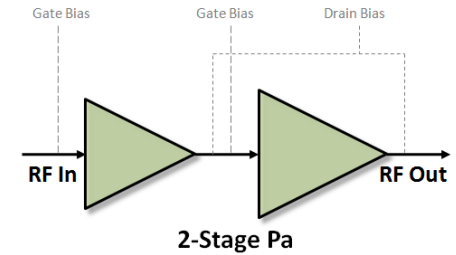
- First stage utilizes 6x44um device.
- Second stage utilizes 6x86um device, for 2:1 drive ratio.
- Amplifier fits into 54x54 mil area
- The circuit was designed in Microwave Office using TriQuint's TQPED design kit.

Table of Contents



- **Specifications**
- **Design Approach**
- **Simulations**
 - Linear:
 - Stability
 - Match
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 - Swept Pin vs. Pout
 - PAE
 - Bias
- **Schematics**
 - RF Schematic
 - DC Schematic
- **Layout**
- **Test Plan**
- **Summary**

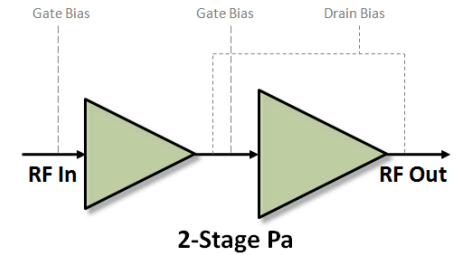
Specifications



- **Specifications:**

	Design Goal	Expected Performance
Power Out	20dBm	20dBm
Small Signal Gain	16 dB	20 dB
Drain Voltage	3.6V	3.6V
Gate Voltage		-0.5V and -0.95V
Frequency Range	5.725 to 5.875 GHz	5.3 to 5.9 GHz
PAE	30%	50%
Stability	Unconditionally stable	Unconditionally stable
Input Match	< -10dB	-10 dB
Output Match	< -3dB	-1.5 dB

Design Approach



- **Output Stage:**

- Started designing output stage as a class E with distributed matching elements.

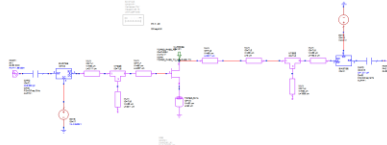


Figure 1. Initial Distributed Design

- Replaced distributed elements with Q elements, using Q of 30 for inductors and 80 for capacitors, then further replaced these elements with design kit elements.
- Tuned circuit to get 20dBm of power out and 60% PAE
- Result ultimately looked like inverse class E topology:

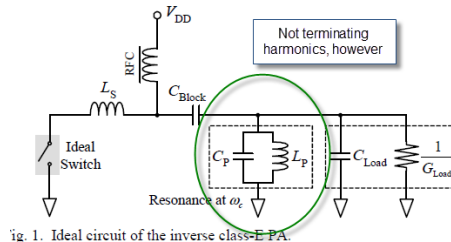
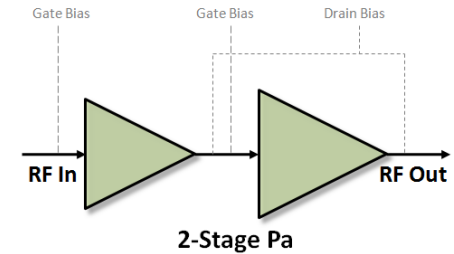


fig. 1. Ideal circuit of the inverse class-E PA.

Figure 1. Inverse Class E

- Achieved best efficiency with pinched off gate, settled on -0.95V.

Design Approach



- **First Stage:**

- Began driver stage next, designing it class A/B using ideal inductors and capacitors as matching elements.
- Replaced ideal elements with Q elements, using Q of 30 for inductors and 80 for capacitors, then further replaced these elements with design kit elements.

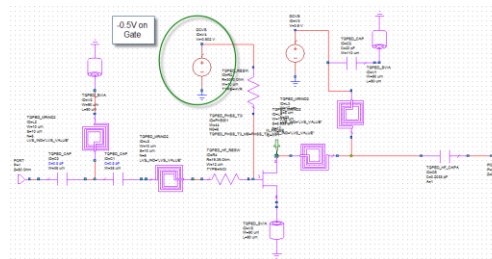
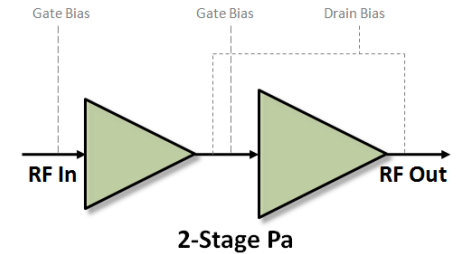


Figure 1. 1st Stage Topology

- Tuned circuit to get 15dBm out at the 1dB compression point, with the intention of operating it backed off from this point.
- Settled on having -0.5V as gate voltage

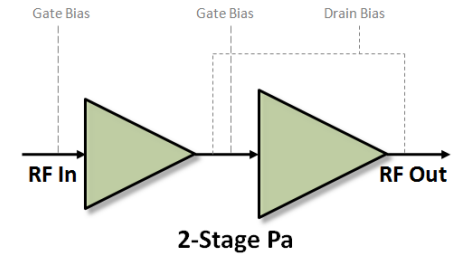
Design Approach



- **Design Trades:**

- Integrated both stages together and re-tuned circuit
- After completely incorporating design kit elements, the class-E operation was no longer seen.
 - Looking at the IV characteristics on the drain of the 2nd stage FET, the operation appeared to be more class B
- The second stage is still operated in pinchoff, which is common to both class E and class B, but the voltage and current waveforms overlap substantially. Regardless of the shift from E to B, high efficiency is still maintained.
- Adding the first stage caused a hit in efficiency of about 10 percentage points.

Simulations



- **Linear: Stability**

- Both stages are unconditionally stable when independently analyzed

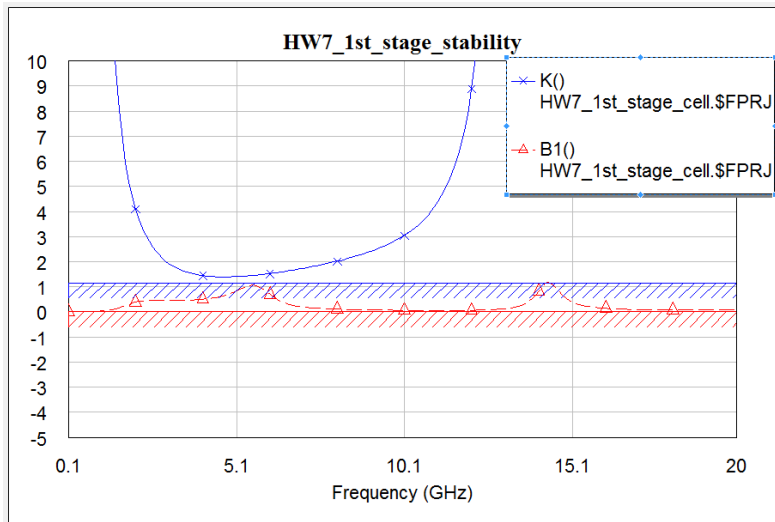


Figure 1. 1st Stage Stability

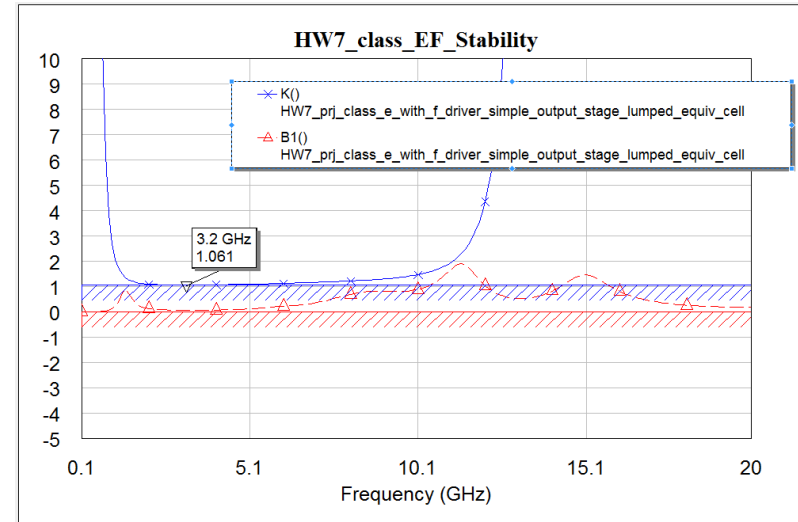
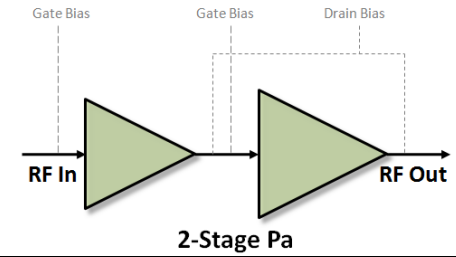


Figure 1. 2nd Stage Stability

Simulations



- **Linear: Match**

- Input is well matched, < -10 dB

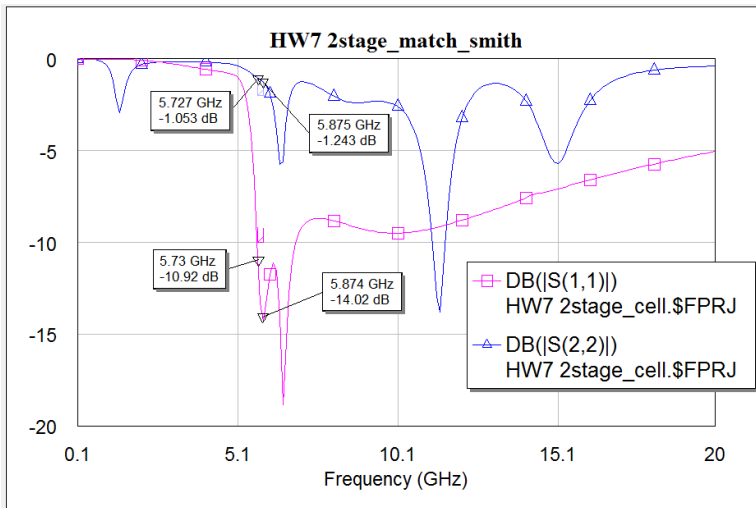


Figure 1. Match

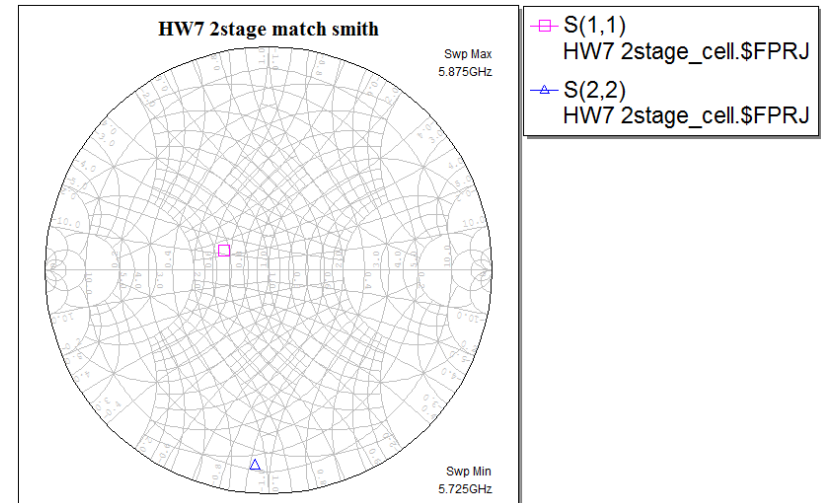
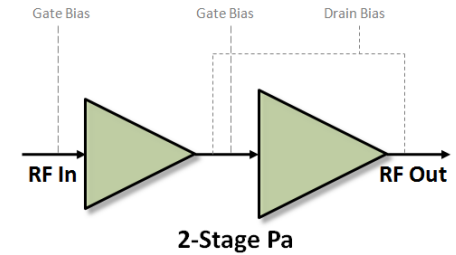


Figure 1. Smith chart match

Simulations



- Non-linear: Pin vs. Pout

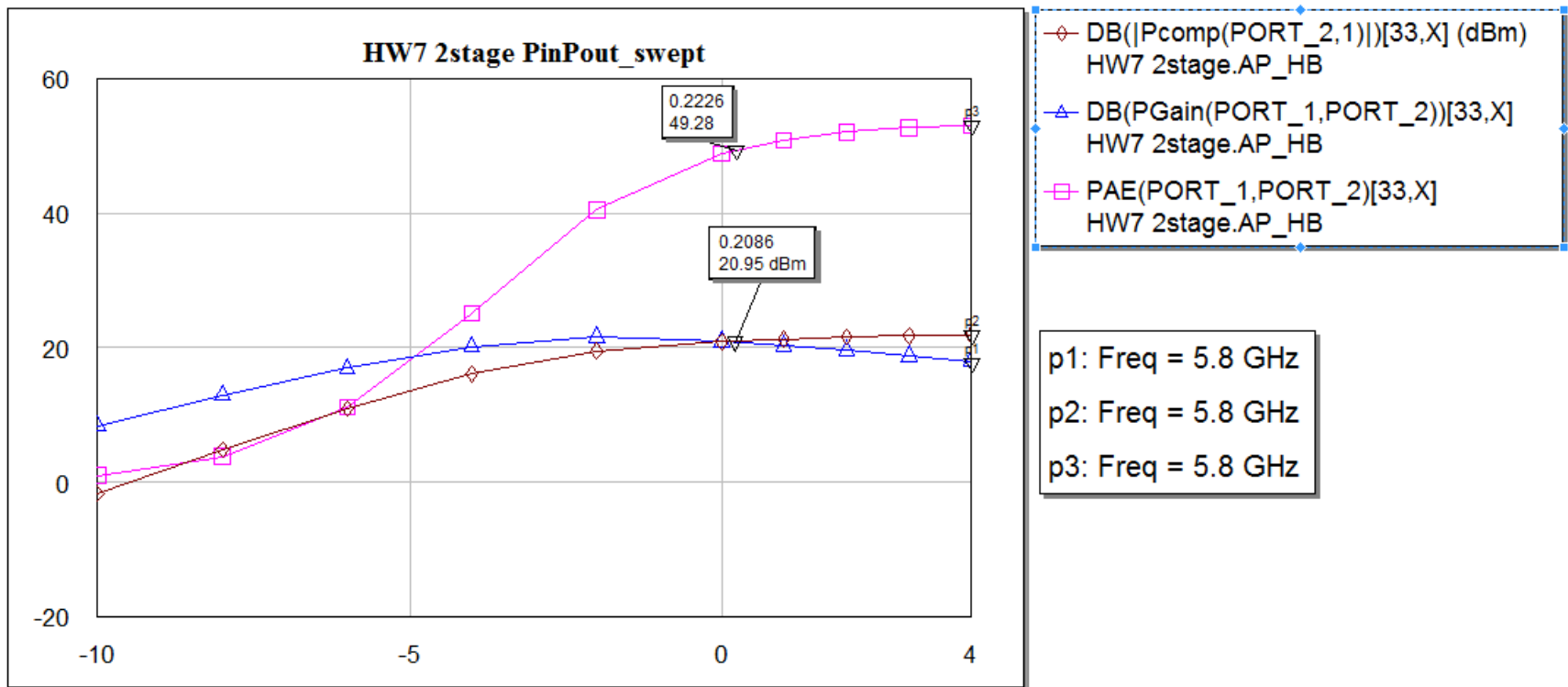
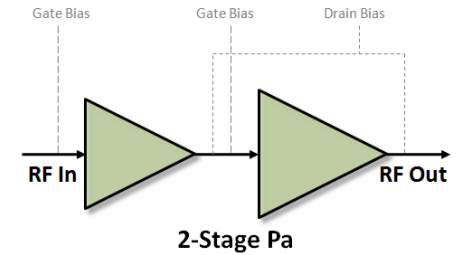


Figure 1. Pin vs. Pout

Simulations



- Non-linear: Pout vs. Frequency

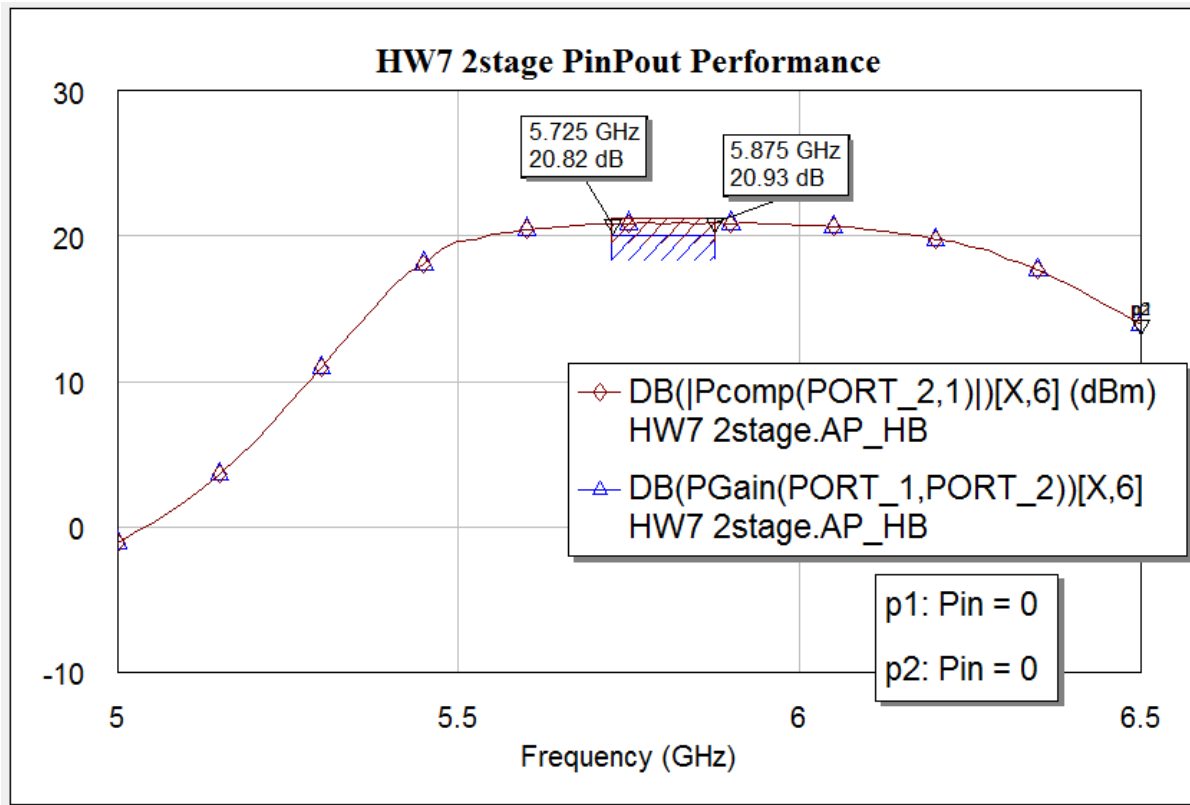
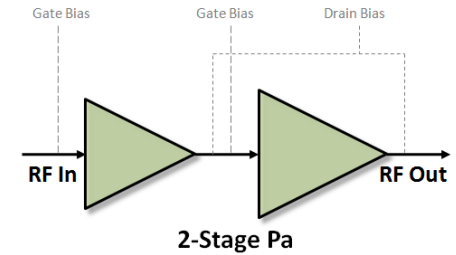


Figure 1. Pout and Gain vs. Frequency

Simulations



- DC Bias
 - Class B bias point was ultimately settled on

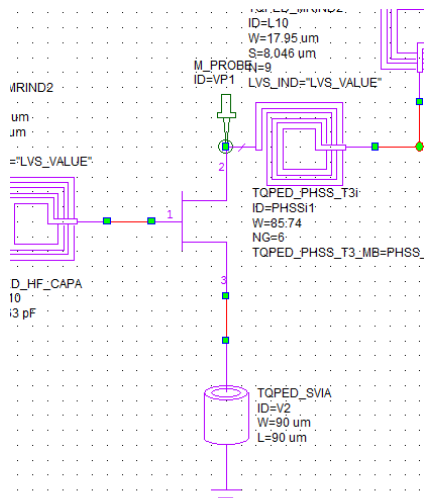


Figure 1. Probe at drain of 2nd stage FET

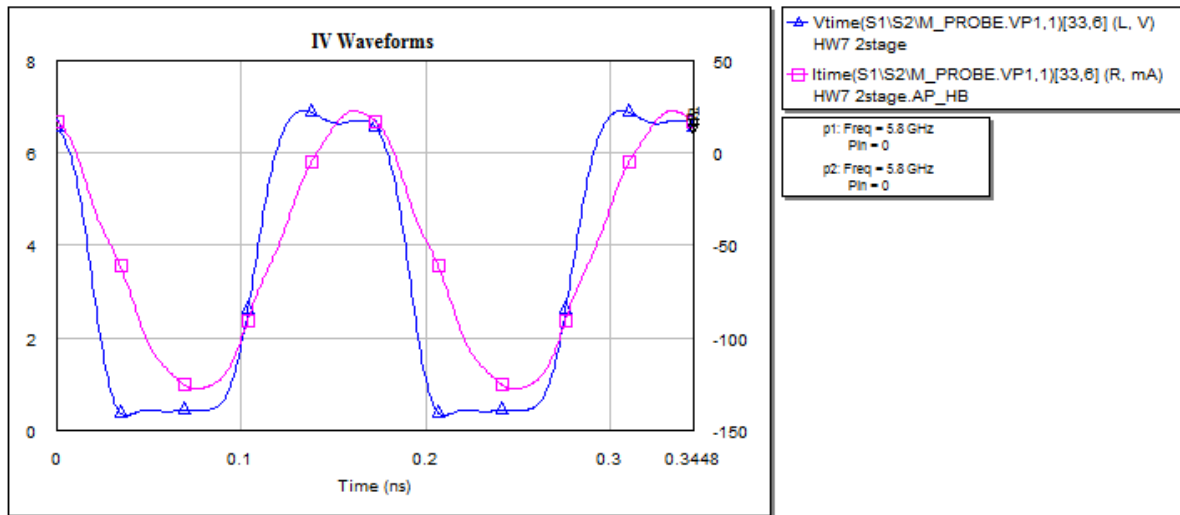
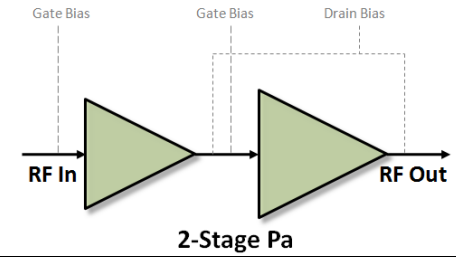


Figure 1. IV Waveforms at drain of 2nd Stage FET

Schematics



- RF Schematic

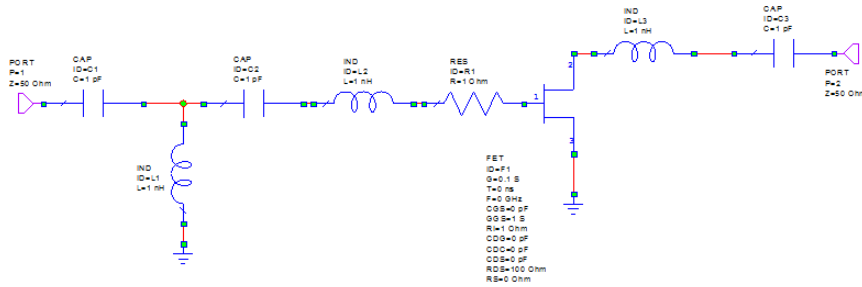


Figure 1. Stage 1 RF schematic

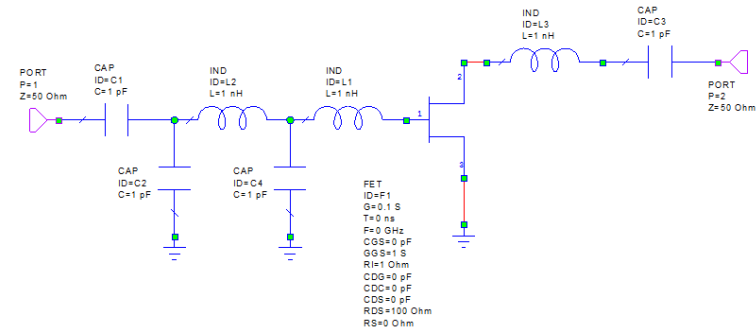
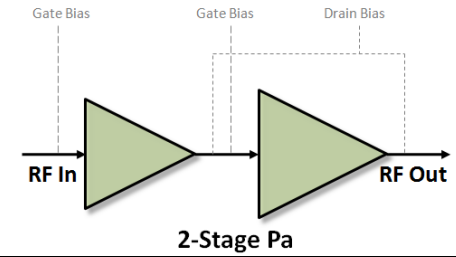


Figure 1. Stage 2 RF schematic

Schematics



- DC Schematic

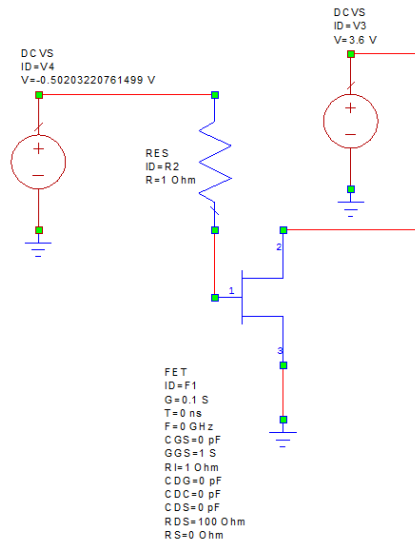


Figure 1. Stage 1 DC schematic

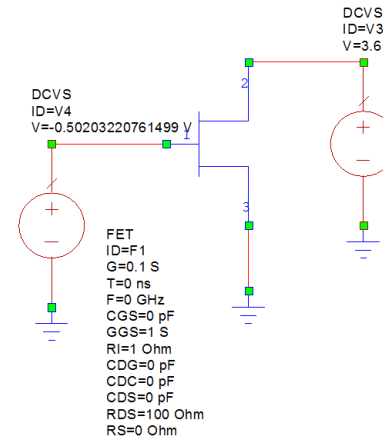
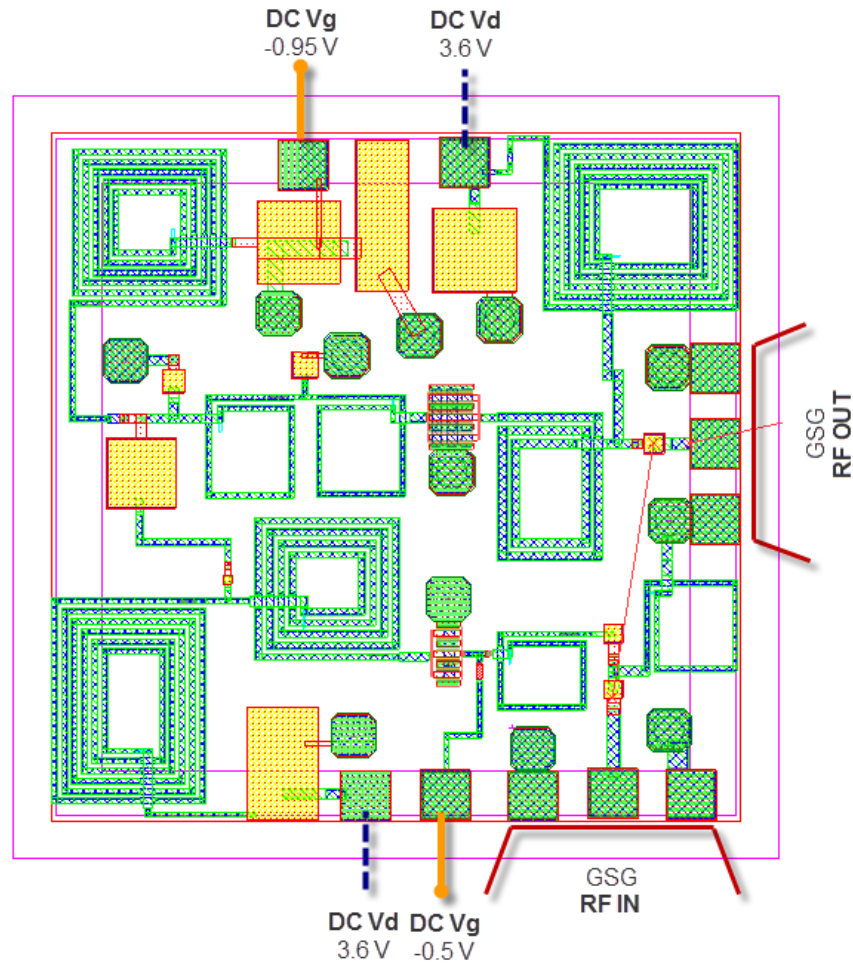
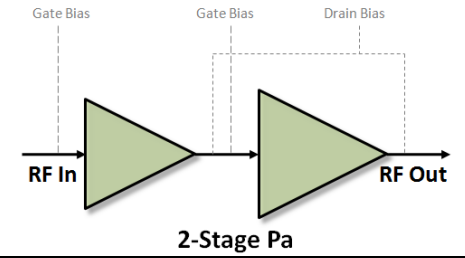
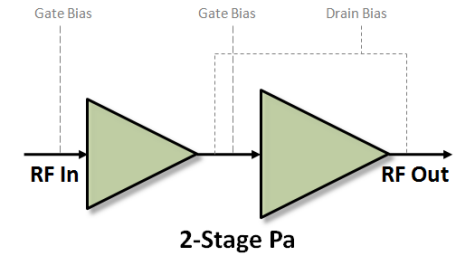


Figure 1. Stage 2 DC schematic

Layout

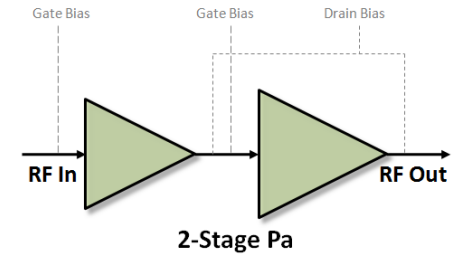


Test Plan



- **Apply gate voltages**
 - -0.5V on first stage
 - -0.95V on second stage
 - If this bias point produces no good result, increase it in 0.5V steps, i.e. to -0.9, until a useful result is found
- **Apply drain voltages**
 - 3.6V for each stage
 - Drain for each stage is not tied together
- **Touch down with GSG Probes**
- **Capture s-parameters**
 - Sweep frequency from 2 to 10 GHz, 0.1 GHz steps
 - Very little or no gain expected here due to 2nd stage bias point.
- **Sweep pin at 5.8 GHz**
 - Expected 1dB compression point is at 0dBm in
 - Start small signal to get a baseline
 - -20 dBm in
 - Slowly increase Pin until part compresses by 1dB
 - Record Pout and PAE
 - Slowly increase Pin until part is 3dB compressed
 - Record Pout and PAE
 - Record Pin level which generates 20dBm out of the chip
 - Repeat for 5.725 and 5.875 GHz

Summary



- An efficient, compact 2-stage PA was designed and implemented in TriQuint Oregon's 0.5um TQPED process. The amplifier produces 20dBm of power across the 5.725 to 5.875 GHz ISM band at p1dB with 50% power added efficiency. It is powered off of a 3.6V drain supply, and two gate supplies, -0.5V on the first stage and -0.95V on the second stage.

Johns Hopkins University
Electrical and Computer Engineering Dept
525.787 - MMIC Design

NAME: Chris Hinton
TITLE: 5.625-5.975 MHz LO
DATE RECEIVED: 12/14/2010

Abstract:

A voltage controlled oscillator [5.625GHz to 5.925GHz] was designed using a common source topology with the TriQuint Semiconductor TQPED Commercial Foundry Process. Both the pHEMT Varactor diode and the pHEMT common source FET were simulated using the Tom 3 Model in Microwave Office (AWR Design Environment 2010 9.04r build 4969 Rev 2). The final simulation results show an ability to tune the oscillation frequency across the required band using the bias [0V to 0.6V] to the Varactor diode.

Design Approach:

The primary goal for this oscillator was simply to cover the frequency range of interest [5.625GHz to 5.975GHz]. Another goal for the VCO was to be incredibly low powered for battery or hand-held operation. The final goal was to only have one supply line as opposed to two.

Unfortunately, the author could not get the non linear OSCAProbe simulation to converge and accurately simulate the non-linearities of the oscillator. Therefore measurements such as phase noise and harmonic rejection were not presently available. The frequency of oscillation was verified and designed equating the angle of Z11 to zero.

To accomplish the secondary DC goals listed above; the VCC was chosen to be 3V with approximately 10mA of DC current and a resistive divider was chosen to supply the correct amount of gate voltage. In addition, an inductor was implemented in the DC Biasing Circuit as opposed to a very large resistor. Using an inductor would not drop as much voltage as opposed to using a large resistor.

Schematics and Simulations:

A large shunt capacitor and a large series inductor were used to bias both the common source pHEMT as well as the Varactor pHEMT (see Figure 1). The Varactor circuit was implemented using a 6x50 pHEMT (see Figure 2). Varying the voltage from 0V to 0.6V caused a change in capacitance from 0.33pF to 0.89pF (see Figure 3).

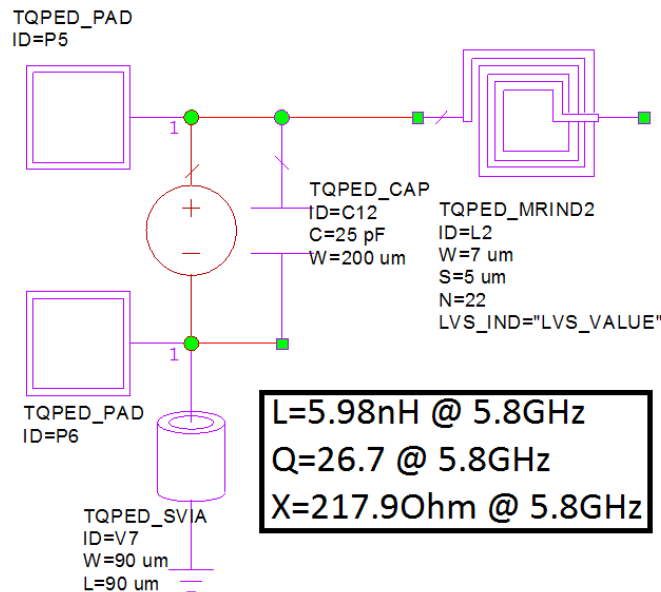


Figure 1: DC Biasing Circuit

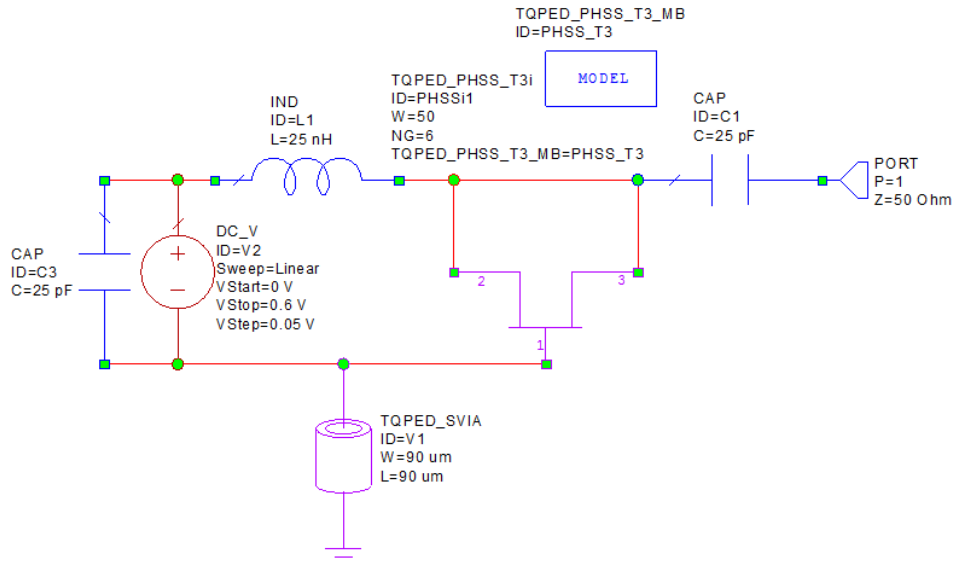


Figure 2: Varactor Circuit

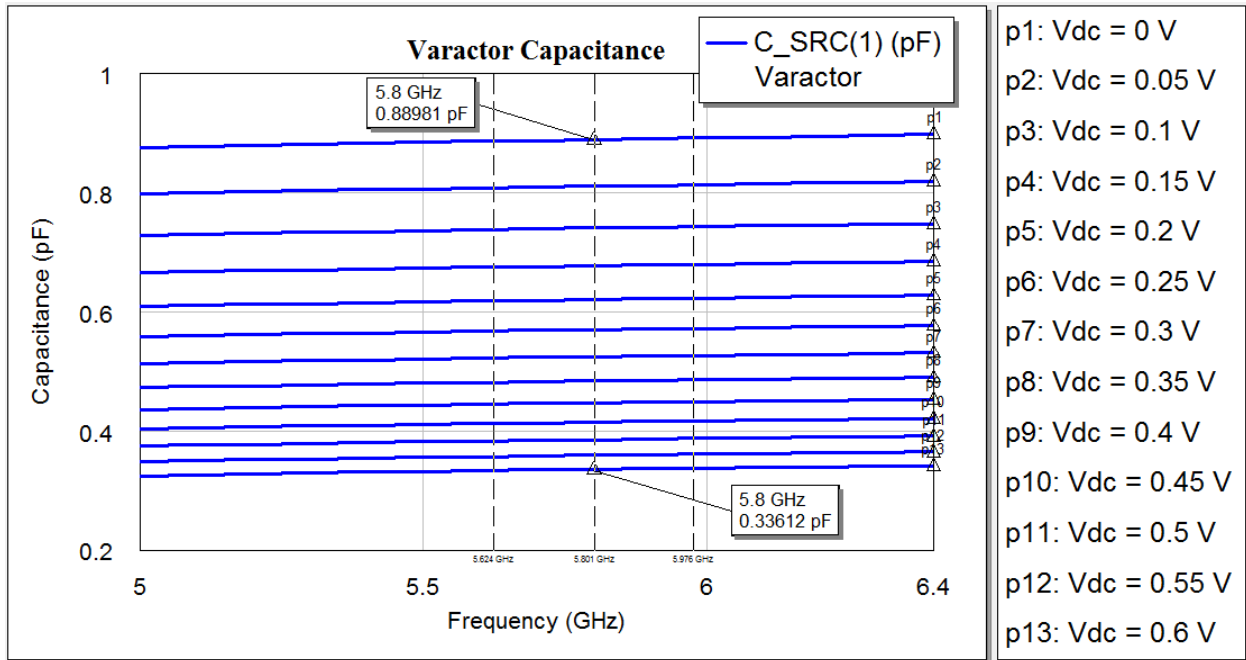


Figure 3: Varactor Response

The final size of the pHEMT (chosen after interconnects were simulated) was 6x55. The final bias chosen for the common source pHEMT was: $V_{ds}=2.02V$, $V_{gs}=-0.59V$, and $I_{ds}=8.26mA$ (see Figure 4 and 5).

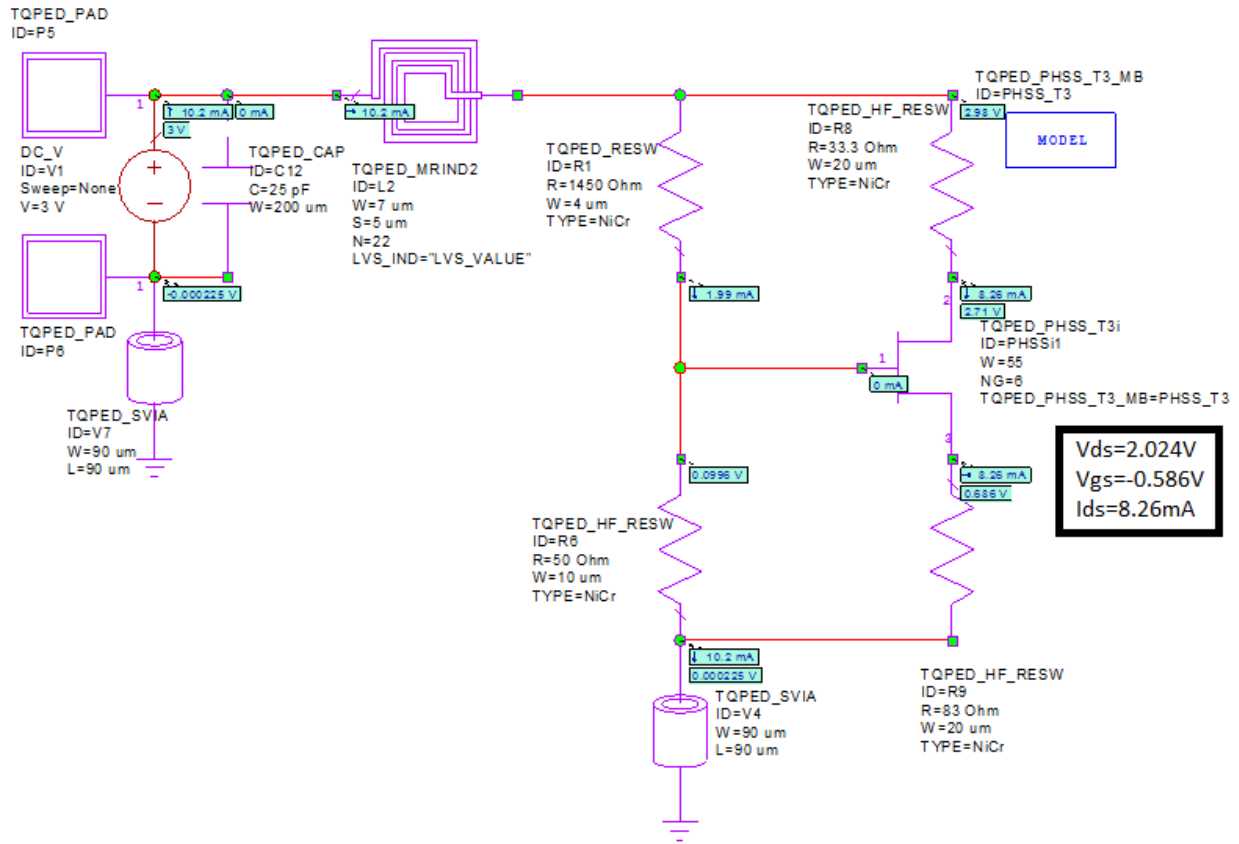


Figure 4: DC Biasing of pHEMT

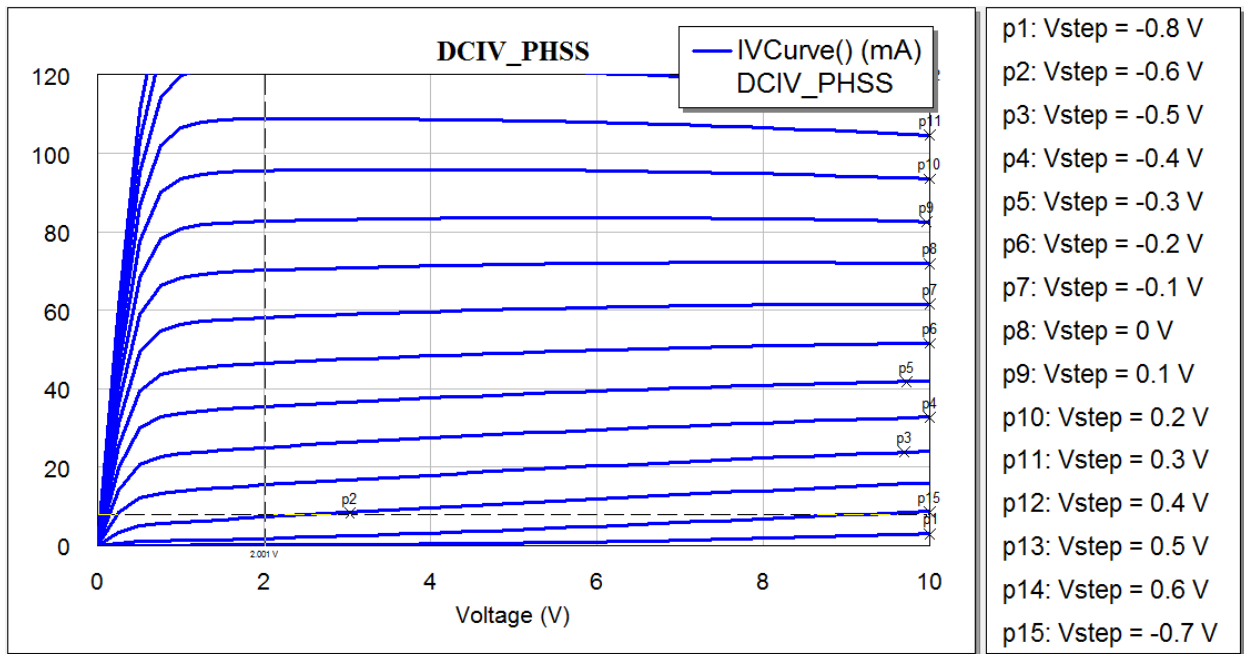


Figure 5: DC Bias Point shown on DCIV Curve

The final circuit consisted of all the above parts being placed together in addition to replacing the ideal transmission lines with lumped equivalents (see Figure 6) using the ABCD matrix calculations. In order to minimize the number of inductors needed the networks used to replace the ideal transmission lines were pi networks with shunt capacitors.

Tuning the Varactor diode from 0V to 0.6V shifted the frequency of S11 (see Figure 7) across the required range [5.625GHz to 5.975GHz]. Unfortunately the zero crossings of the angle of Z11 did not cross zero throughout the tuning range (see Figure 8). One can see that the zero crossing occurs at 5.8GHz with a tuning voltage of 0.25V. Unfortunately when the Varactor is tuned down to 0V the angle does not cross zero (although it gets close) which will cause a lack of oscillation. The high end of the tuning range (0.6V) does cross zero at 5.934GHz (see Figure 8).

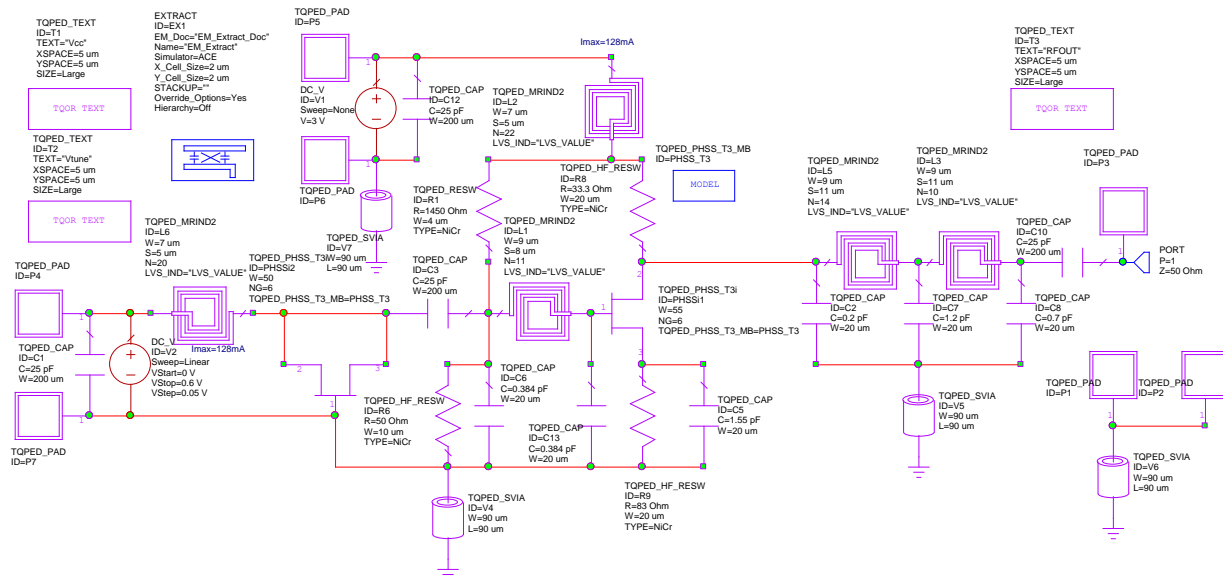


Figure 6: Final VCO Circuit

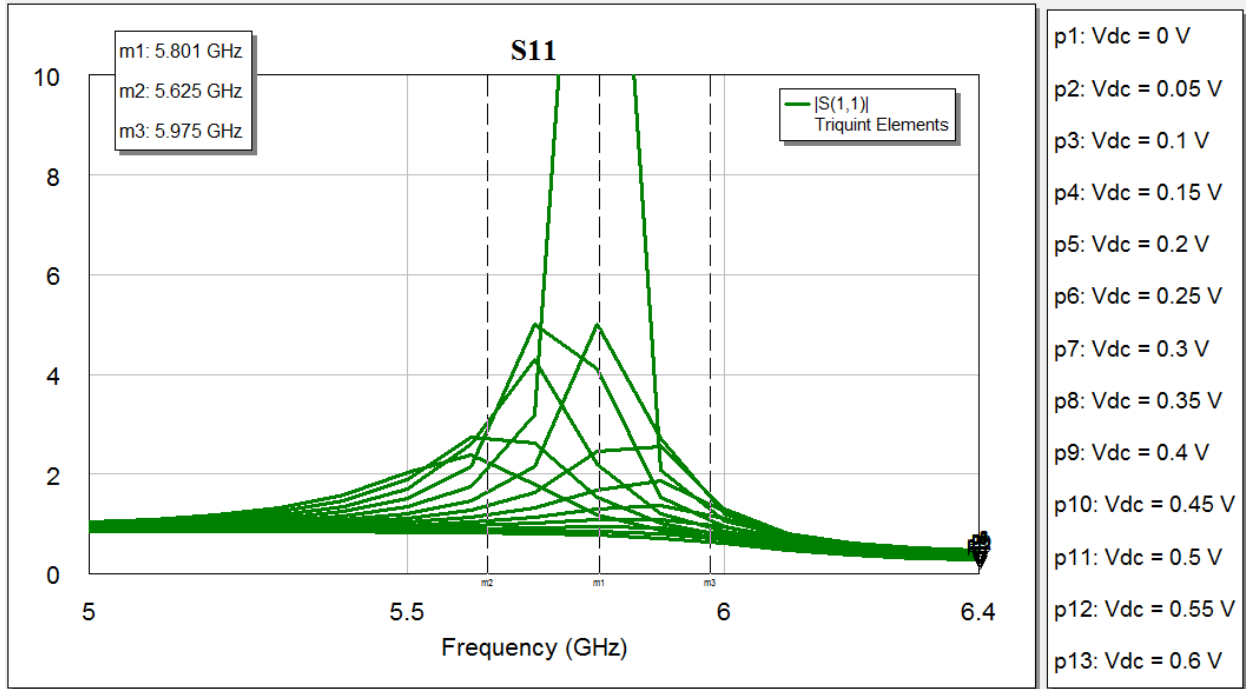


Figure 7: S11 of VCO with Varactor tune Voltages

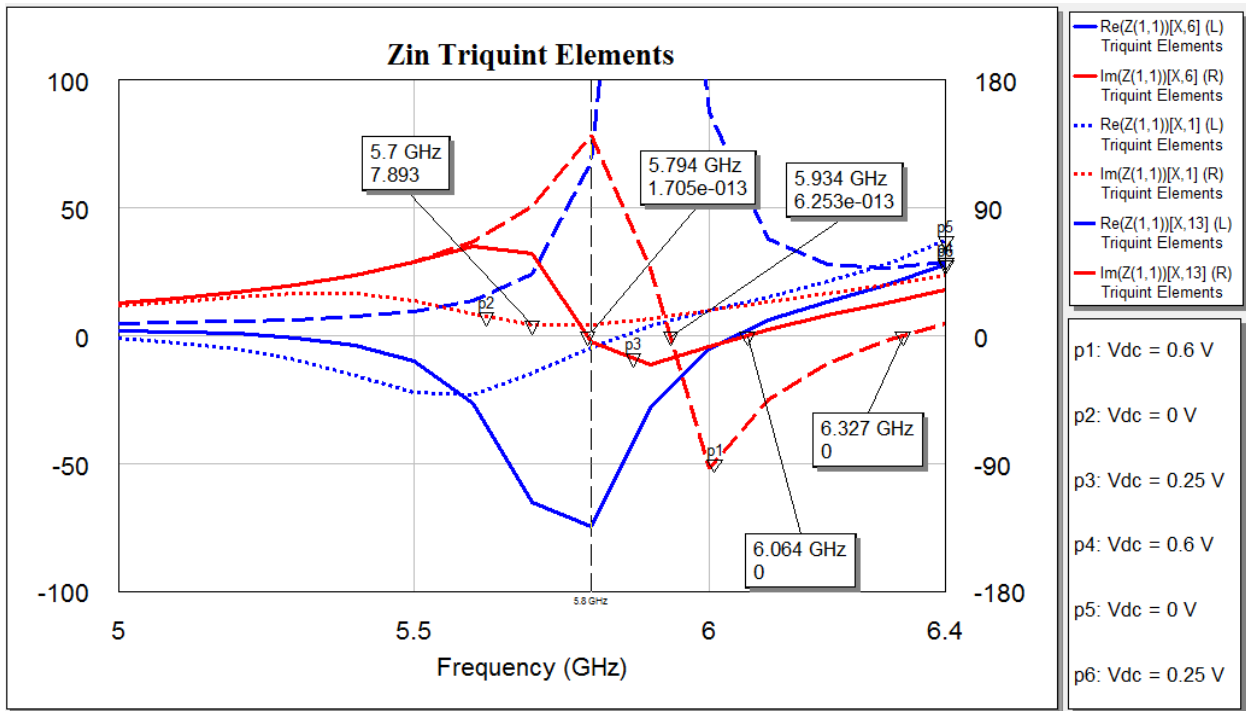


Figure 8: Input Impedance showing potential Oscillations Frequencies

Layout Plot:

In order to keep the layout generic and simple, Metal1 was used for signals (for the most part) while Metal0 was used mostly for grounding purposes (excluding the inductor macros). Metal0 was used to connect to the resistors so the GDS file would pass DRC.

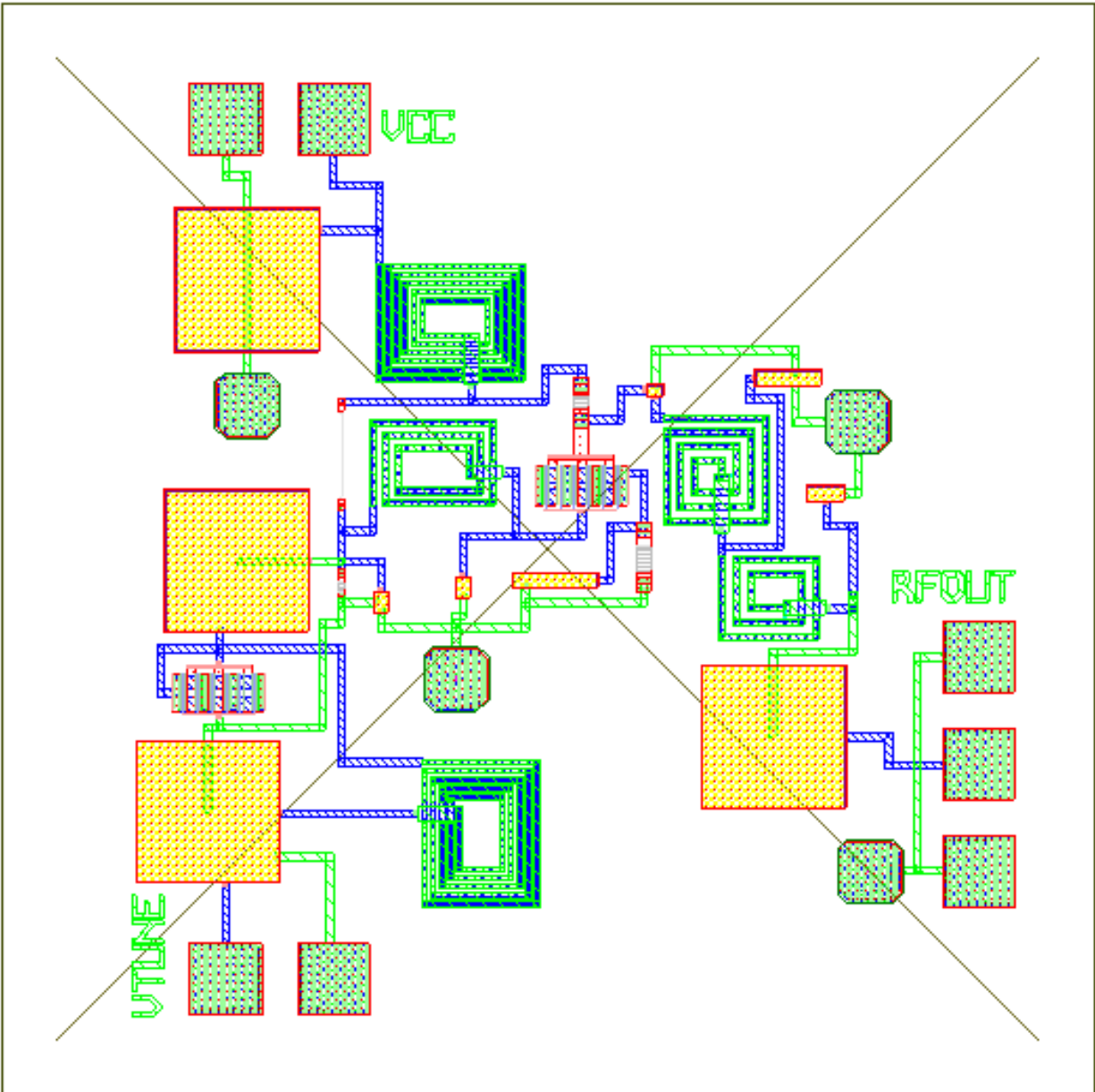


Figure 9: Final VCO Layout 2D

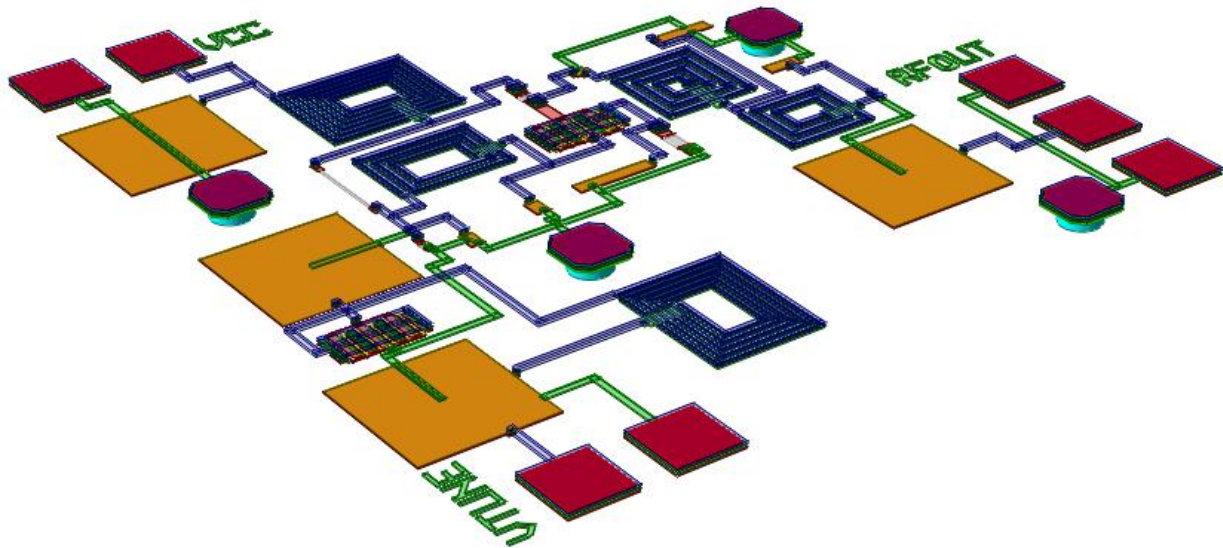


Figure 10: Final VCO Layout 3D

Test Plan:

- 1.) Apply DC Voltages ($3V@V_{cc}$ and $0.25V@V_{tune}$) check that 10-12 mA of DC current is flowing from power supply to V_{cc}
- 2.) Load RF OUT with 50Ohm resistor and check any change in Current or voltages
- 3.) Connect RF OUT to a spectrum analyzer with an adequate SMA cable
- 4.) Monitor and track oscillation frequency and level against tuning voltage
- 5.) Tune back to center frequency and measure the SSB phase noise

Summary & Conclusions:

A major concern with this oscillator is how changing of the tuning voltage will change the frequency. Linear simulation has shown that the circuit will oscillate at 5.8GHz with a tuning voltage of 0.25V. Unfortunately at the time of this paper, the circuit did not have a non-linear simulation result. Therefore general oscillator questions such as output power, harmonic suppression, phase noise, and exact tuning range cannot be accurately predicted. It will be interesting to test the circuit after fabrication to see the non-ideal and non-linear results.

4-8GHz Microwave Switch MMIC

Nicholas Garneski

12/19/10

Abstract

A 4-8 Gigahertz (GHz) Monolithic Microwave Integrated Circuit (MMIC) Single Pole Double Throw (SPDT) switch was designed, simulated, and laid out using the Triquint TQPED process. The design was optimized for performance in the 5.8 GHz Industrial Scientific and Military (ISM) band, to be used as a Transmit/Receive (T/R) switch. A parallel switch topology was used, and a differential bias circuit added to allow for a single control voltage. Enhancement mode Field Effect Transistors (FETs) were selected to allow for a single positive supply.

Introduction

The 4-8 GHz SPDT switch was designed to serve as an effective means to switch an antenna between the transmit and receive modes for the 5.8 GHz band. An SPDT switch, as illustrated in Figure 1, allows a single common port to be switched between two isolated ports.

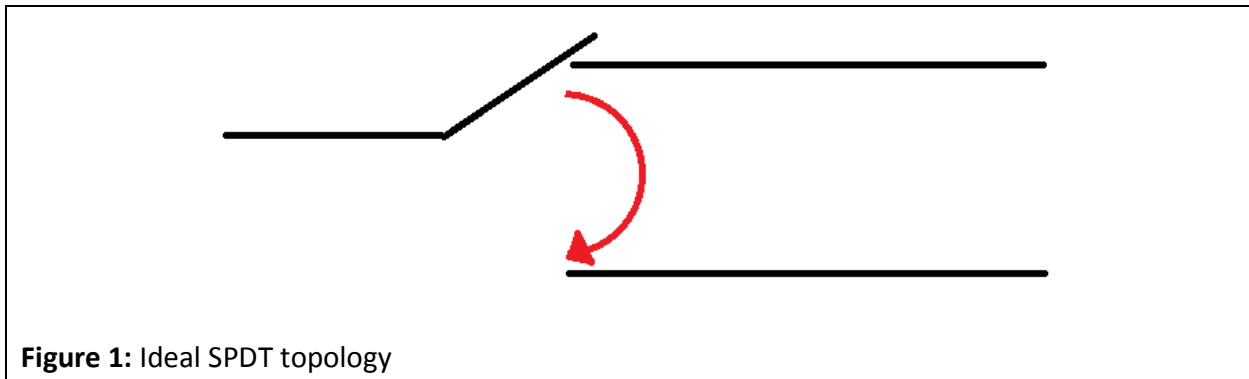


Figure 1: Ideal SPDT topology

The switch is powered by a single +3.3V Direct Current (DC) source, with separate terminals for Radio Frequency (RF) and DC ground. A second +3.3V DC voltage can be applied across the control terminal to switch between the two switched ports, L1 and L2. If the control voltage is disconnected but the power voltage is applied, neither L1 nor L2 will be connected.

Mechanical relays offer reduced loss and wider bandwidth when compared to solid state relays, but suffer from a significantly higher switching time and a reduced life cycle due to the potential risk of mechanical failure. A typical high reliability mechanical switch lifetime is on the order of 10 million cycles, while a solid state switch is not limited by switching lifetime. Because of these factors, a solid state switch, such as the one presented, is a more effective choice for most T/R switching applications, where thousands of switching cycles per second can often be required.

The switch was designed with a first order lumped element shunt topology, illustrated in Figure 2. While other methods offer theoretically better results when used with ideal components, experiments with implementation revealed the simple shunt topology to be a favorable choice at the selected frequency (5.8 GHz). The topology uses a quarter wave transformer, of the same impedance as the system, connected to the drain of a transistor, whose source is grounded. By controlling the DC gate voltage, an ideal transistor is switched between an open and short circuit. The quarter wave transformer transforms the short to an open, and thereby isolates the active branch from the disabled branch.

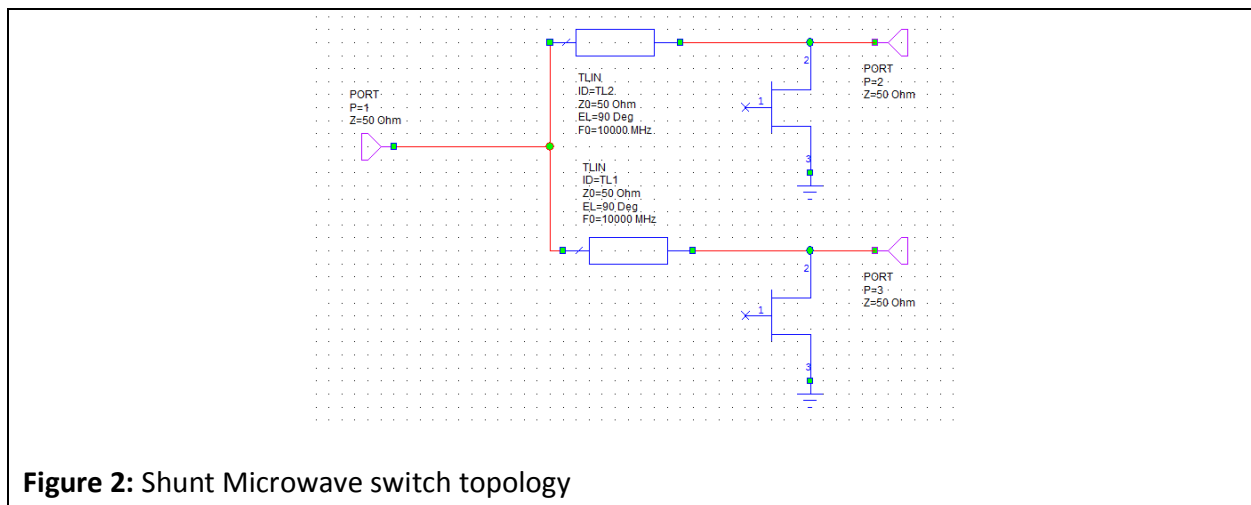


Figure 2: Shunt Microwave switch topology

Design Approach

Numerous candidate designs were researched. Series topologies provide greater bandwidth, yet are impacted more severely by transistor parasitics. This can cause a significant reduction in performance in high frequency applications. Shunt topologies are more complex, have a narrower bandwidth, but are impacted less by the transistors non idealities. A shunt topology was selected after some experimentation.

A series switch stage can be placed in combination with a shunt switch stage, or multiple series and shunt stages can be placed together. These higher order switch topologies can provide greatly improved performance, but at the cost of complexity. While higher order topologies theoretically result in lower loss and greater isolation, their increased complexity actually significantly increased simulated insertion loss. This discrepancy with theory was attributed to component loss. As no benefit outside of isolation was achieved from the higher order topologies, a first order topology was selected.

Enhancement mode FETs were selected to allow for a single positive supply voltage. While this simplifies implementation and operation it significantly reduces the potential power handing of the switch. A single supply voltage allows a differential bias circuit to be constructed,

without significant complexity. This tradeoff was determined to be acceptable and the goals were altered as such.

The quarter wave transformers within the switch topology were transformed into Pi networks of lumped elements by using the transformations listed in equations 1 and 2.

$$C = \frac{1}{Z_0 * \omega} \quad (\text{Eqn. 1})$$

$$L = \frac{Z_0}{\omega} \quad (\text{Eqn. 2})$$

The resulting equivalent lumped element circuit is shown in Figure 3. Pi networks were selected over T networks as they reduce the number of inductors, and allow for multiple parallel capacitors to be combined within the switch design.

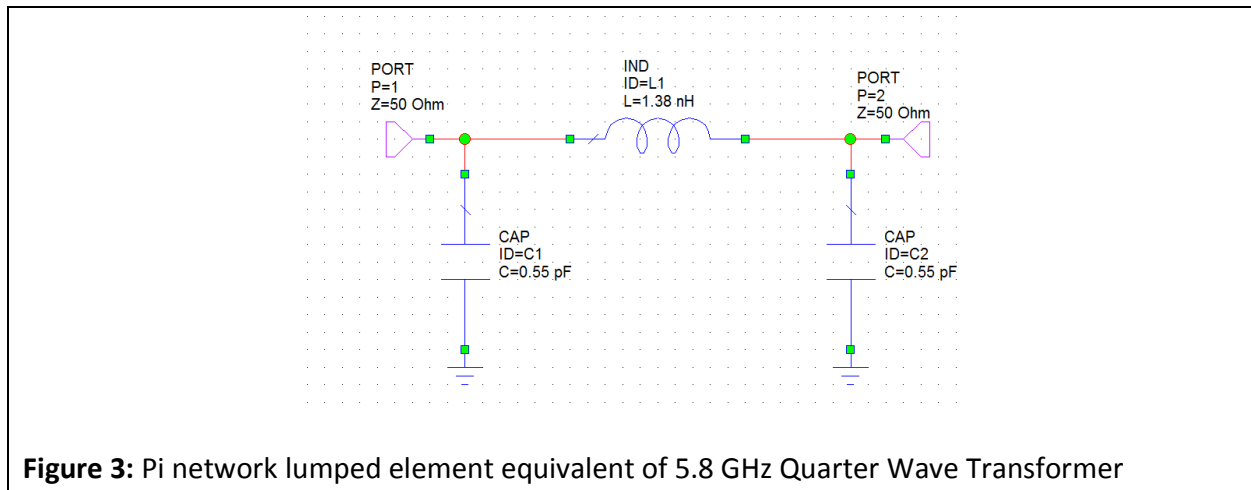


Figure 3: Pi network lumped element equivalent of 5.8 GHz Quarter Wave Transformer

After initial experimentation and schematic simulation, the design specifications were altered into a series of goals. The goals and specifications are listed in Table 1. The insertion loss goal was slightly loosened compared to the specification to allow for more broadband optimization. The power handling specification was significantly reduced due to the selection of enhancement mode FETs.

Design Specifications and Goals		
Category	Specification	Goal
Insertion Loss	<0.5 dB	<1 dB
Return Loss(active branch)	-	>15 dB
Bandwidth(3dB)	-	4 GHz
Switching Time	-	100 ns
Power Handling	24 dBm	10 dBm
Operating Frequency	5.8 GHz	5.8 GHz
Isolation	-	20 dB

Table 1: Microwave Design Specifications and Goals

A differential bias network was designed for the switch. The differential bias allows for simple end user control, yet adds design complexity. The differential bias is also heavily dependent on the control voltage being near to its nominal voltage. Any difference will result in severe performance degradation. The design selected utilizes diodes to provide a saturation voltage to the switch transistors. This provides a fairly stable voltage source for the gate. Minimum and maximum bias requirements were determined through nonlinear device simulation.

DC Operating Requirements	
Nominal Operating Supply Voltage	3.3 V
Minimum Operating Supply Voltage	2 V
Maximum Operating Supply Voltage	6 V
Nominal Operating Control Voltage	0 V or Supply Voltage
Max Differential Control-Nominal Voltage	+/- 0.2 V
Resting Average Current Use	6 mA

Table 2: DC Operating Requirements

A resonant inductor was added in shunt to the switch transistor. A semi-ideal switch circuit, pictured in Figure 4, was created, using a transistor model, in series with an ideal transmission line. This resonant structure resulted in a sacrifice with regards to complexity, and size, due to the large footprint of inductors, but the substantial improvement in RF performance is illustrated in Figure 5. The number of transistor fingers was optimized in a balance between open and short circuit performance.

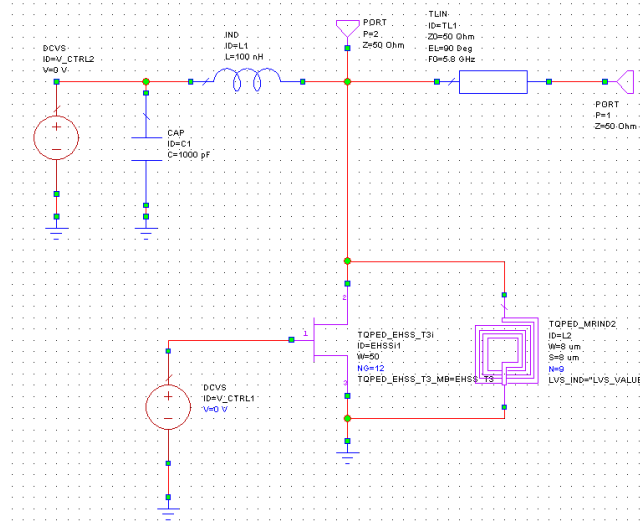


Figure 4: Resonator Design Circuit.

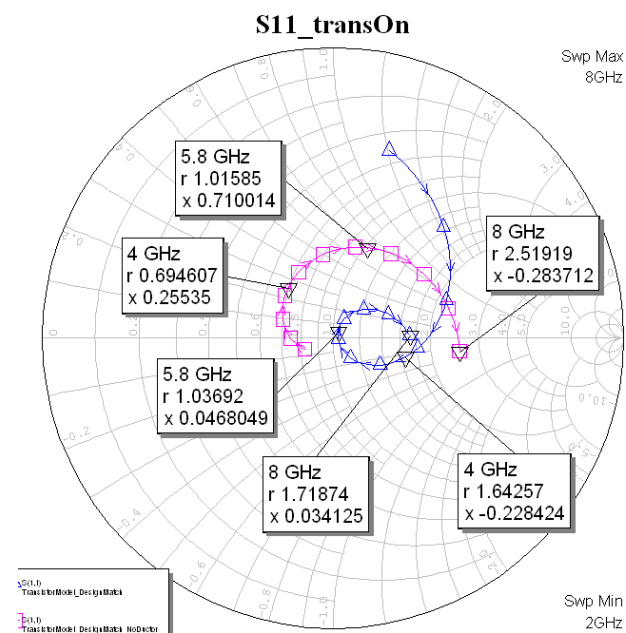


Figure 5: Resonator design circuit performance. Pink trace is input impedance prior to addition of resonator. Blue trace is input impedance after the addition.

The components were replaced by their TQPED library equivalent and nonlinear simulations were performed. Component values were tweaked to re-optimize the RF response. The size of many RF choke and DC block components were reduced to optimize footprint size. The circuit was laid out with emphases on reducing the RF path length as much as possible, and separating the two switch paths from one another to avoid any isolation problems. The DC circuitry was, as a result, compressed to the opposite side of the layout.

Simulation Results

A. Linear Results

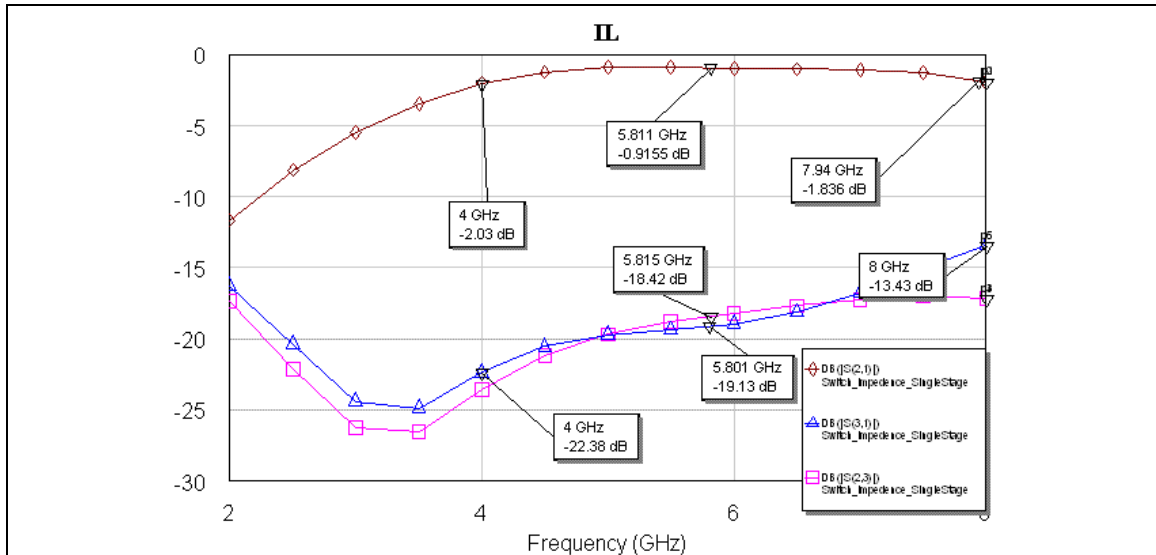


Figure 6: Insertion Loss and Isolation data for “top path,” active when VCTRL = 0. Brown trace is insertion loss. Blue trace is port to antenna isolation, pink trace is port to port isolation. The lower loss makes it ideal for the receive path.

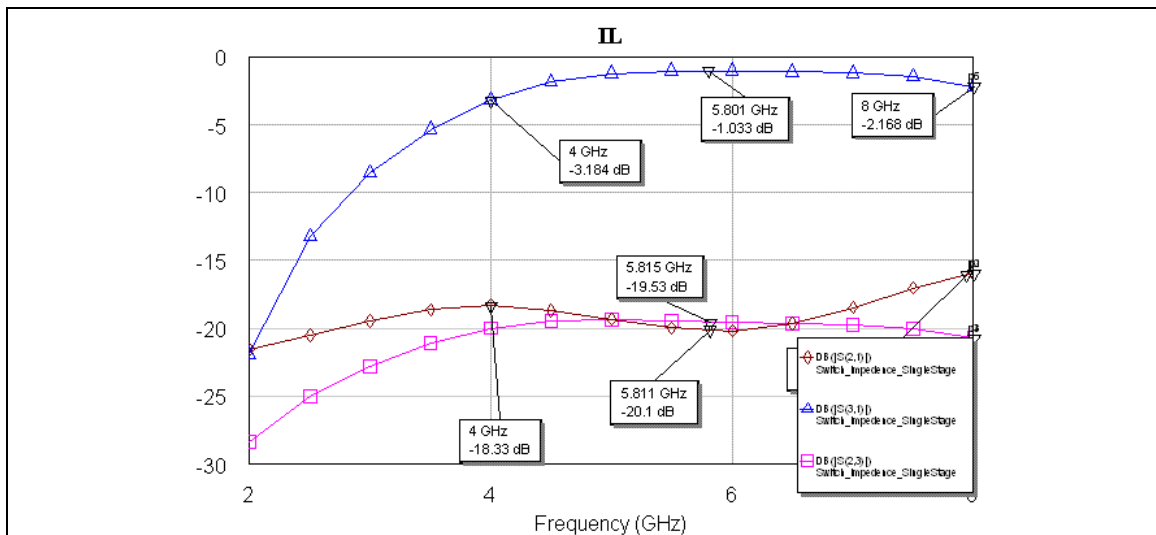
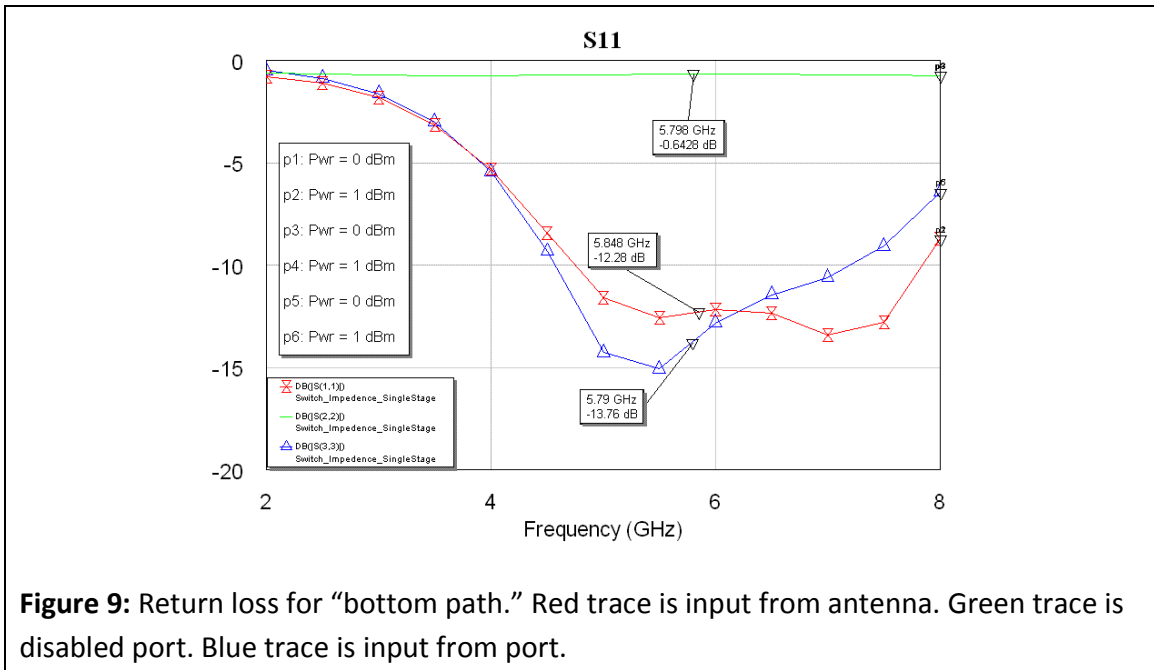
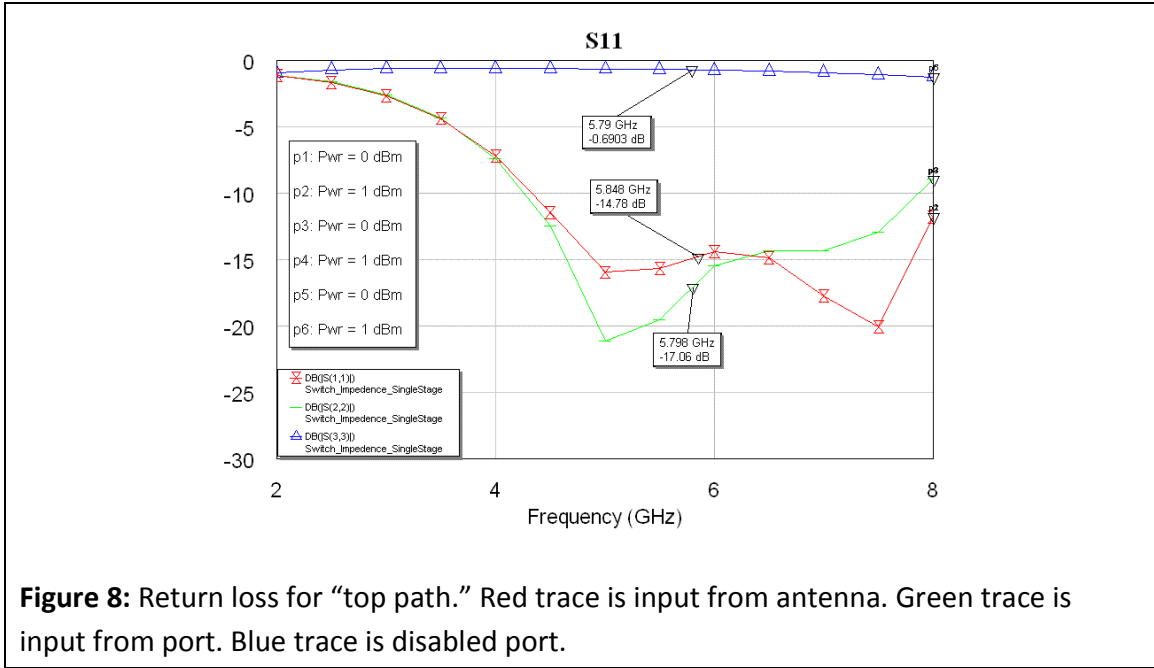
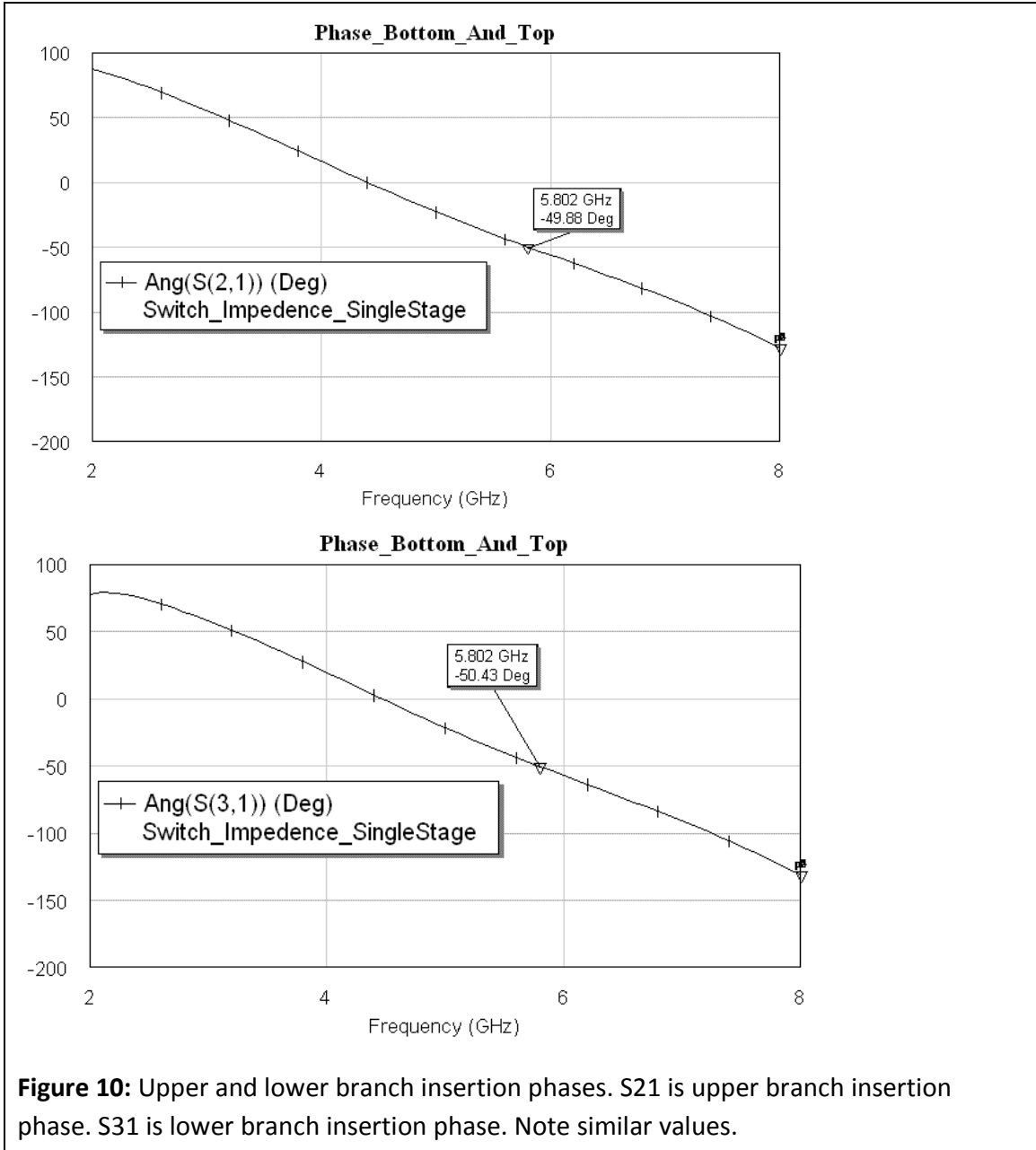


Figure 7: Insertion loss data for “bottom path”, active when VCTRL=3.5V. Blue trace is insertion loss. Brown trace is port to antenna isolation, pink trace is port to port isolation.





B. Nonlinear Results

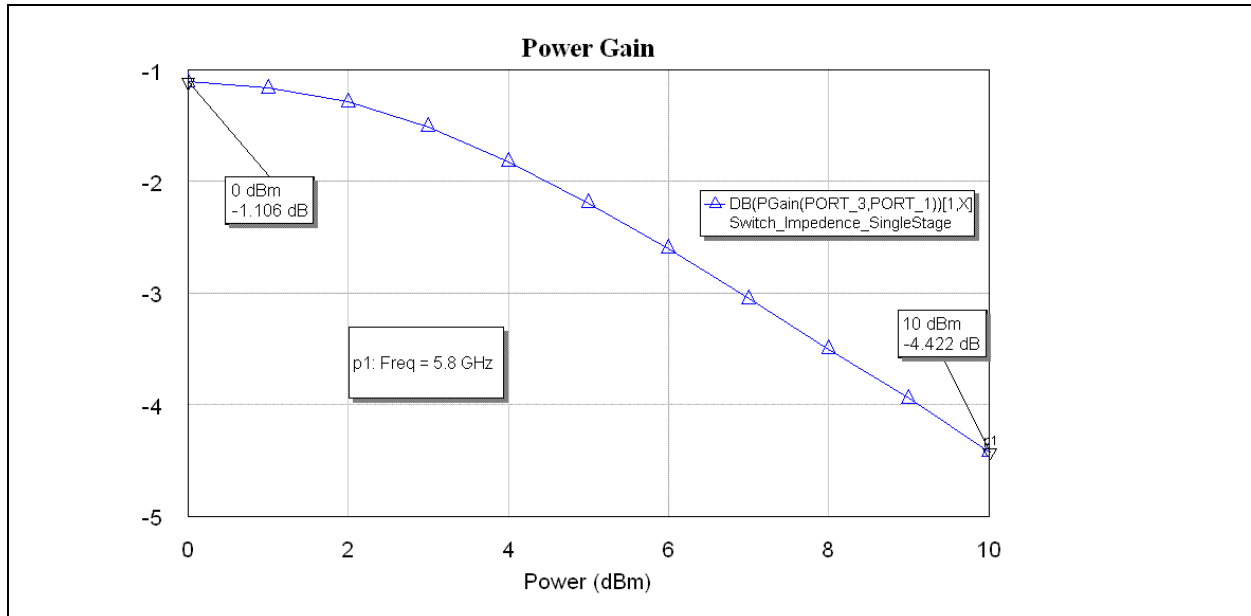


Figure 11: Insertion loss at 5.8 GHz versus input power. It indicates a 3 dB compression point at approximately 10 dBm, and a 1 dB compression at approximately 5 dBm.

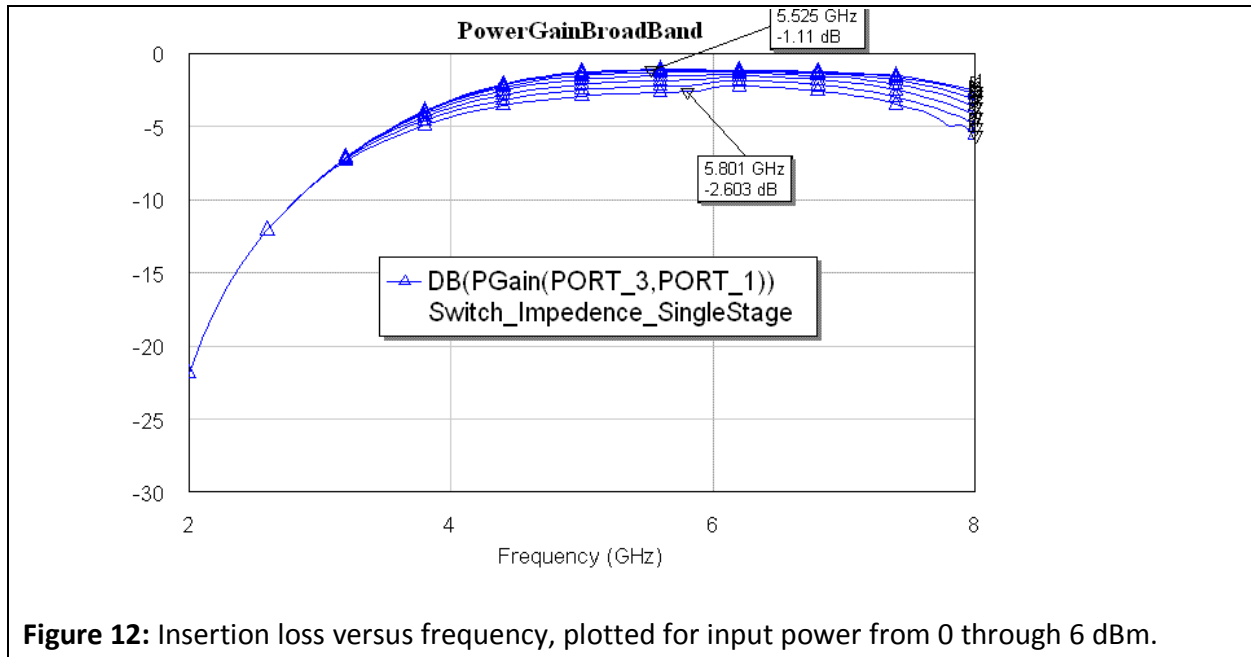


Figure 12: Insertion loss versus frequency, plotted for input power from 0 through 6 dBm.

C. DC Operation Point Data

Parameter	Vctrl = 0	Vctrl = 3.5
Input Current	4.06 mA	6 mA
Vgs_top	0	0.96 V
Vgs_bottom	0.90 V	0

Table 3: DC Operation Points. Gathered from AWR nonlinear simulator

Schematics

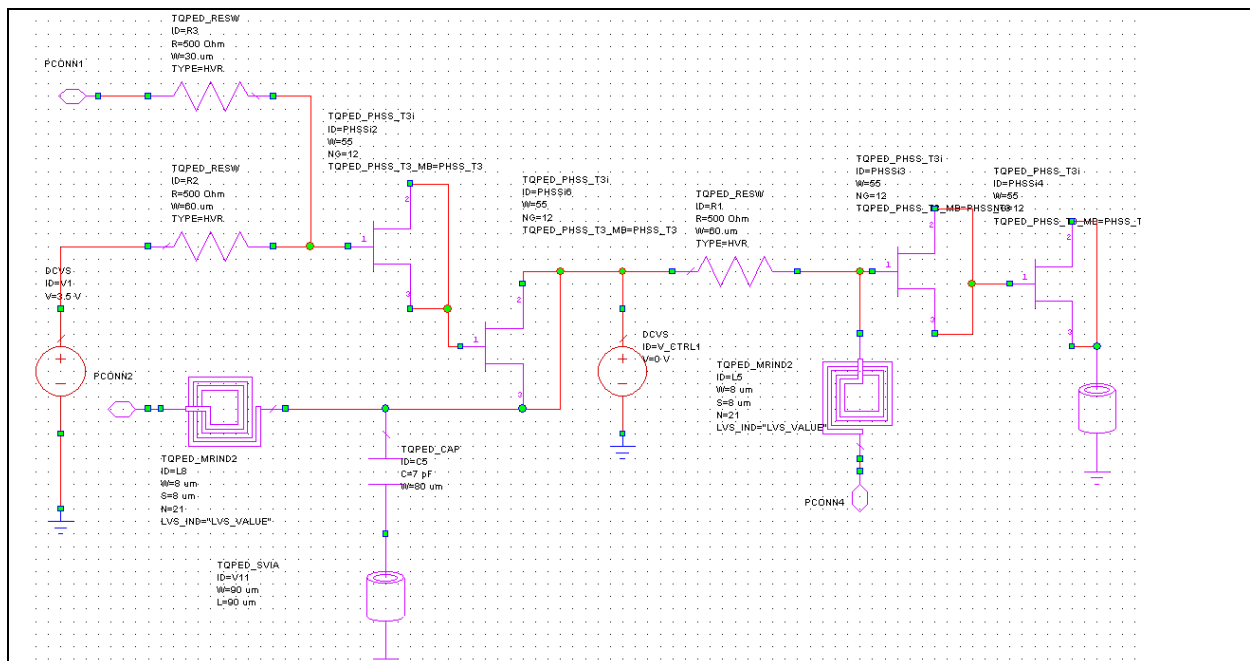


Figure 13: Simplified DC schematic. PConn1(Top Left) is gate voltage for bottom path. PConn2(Bottom left) is source voltage for bottom path. PConn3(Bottom Right) is gate voltage for top path.

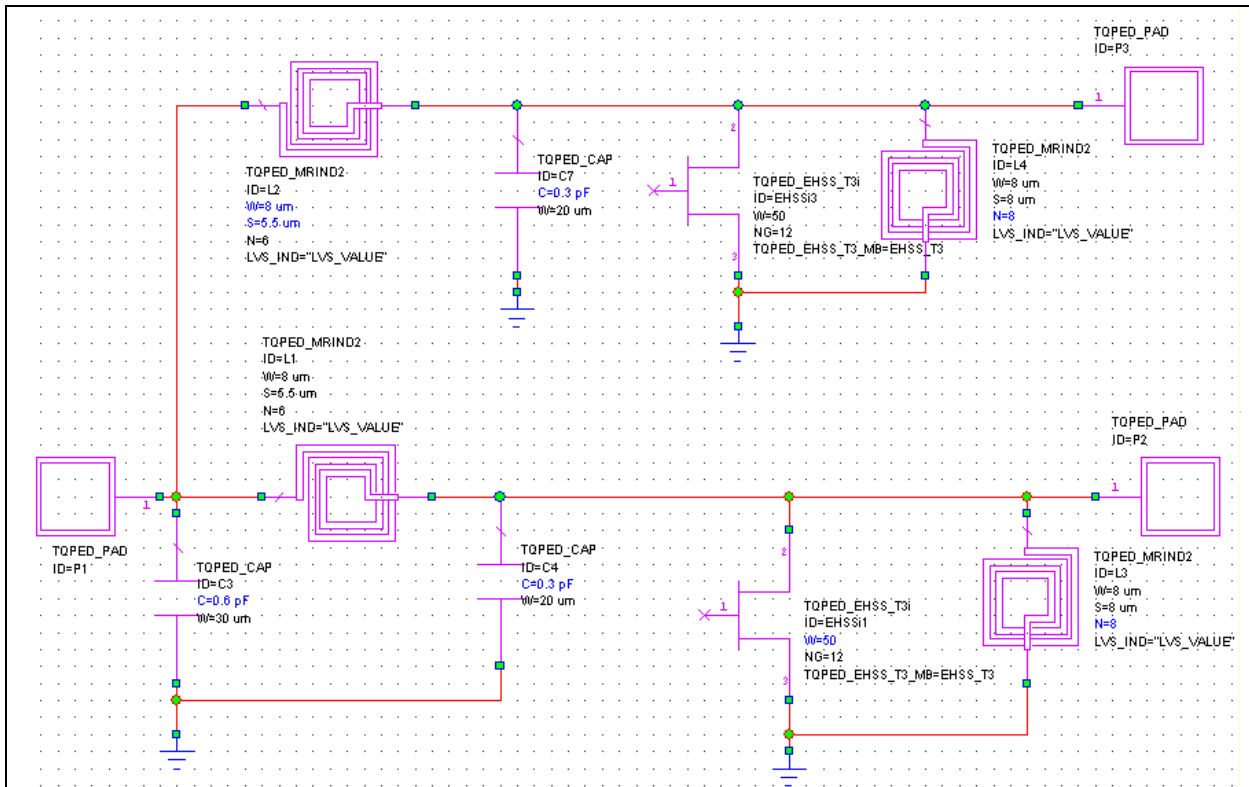


Figure 14: Simplified RF schematic. DC bias, RF chokes, and ground VIAs have been removed for simplicity.

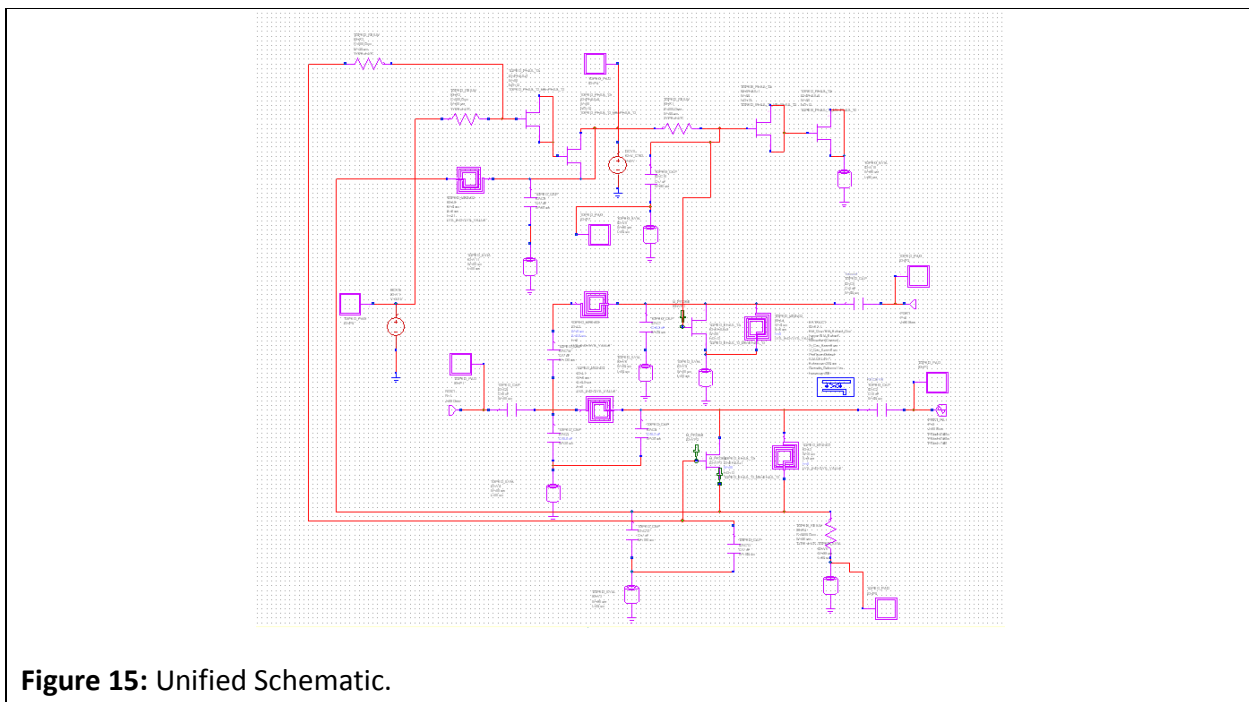


Figure 15: Unified Schematic.

Layout

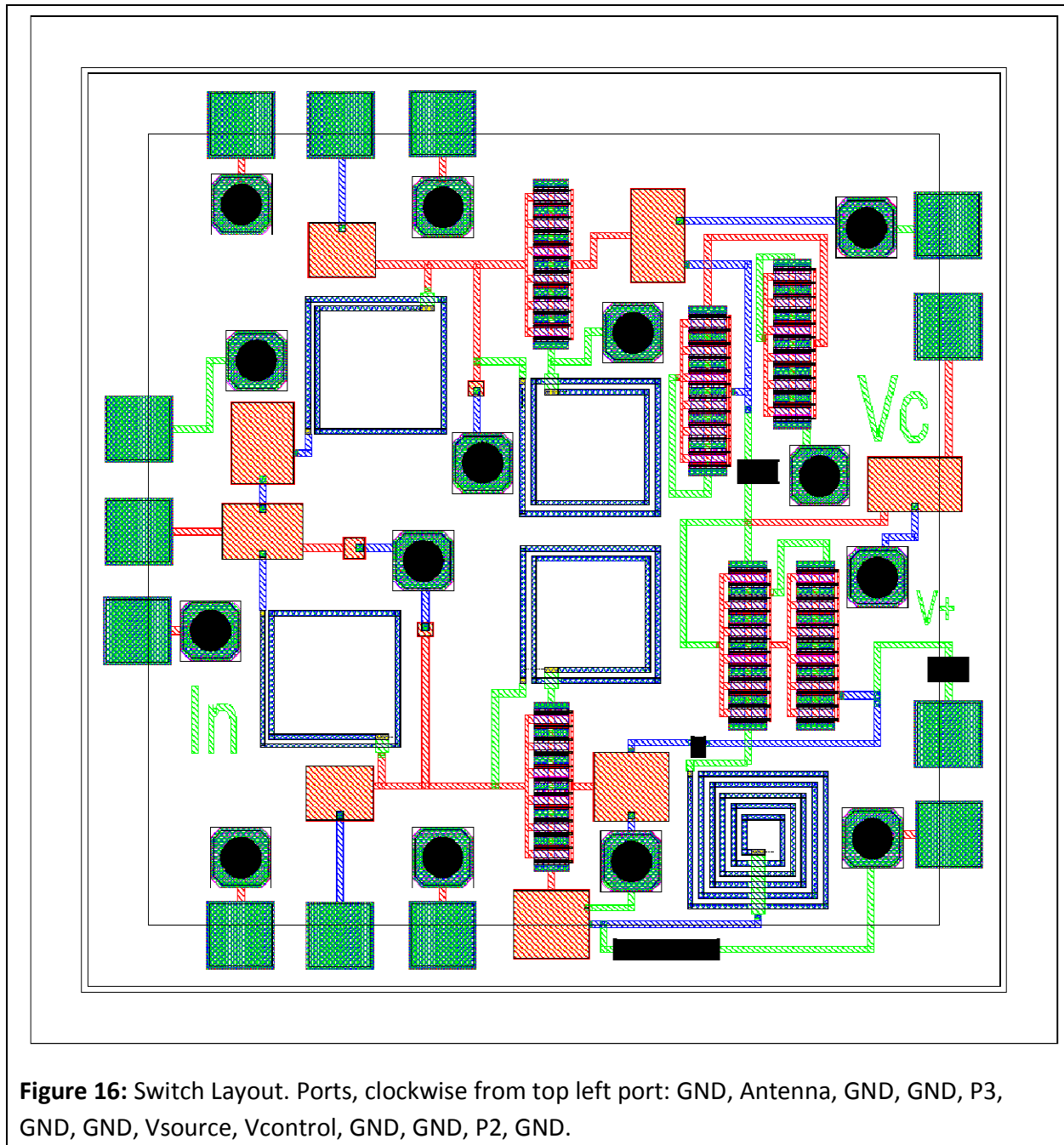


Figure 16: Switch Layout. Ports, clockwise from top left port: GND, Antenna, GND, GND, P3, GND, GND, Vsource, Vcontrol, GND, GND, P2, GND.

Test Plan

1. Probe RF Parameter Testing

The S parameters of the switch will be measured using a network analyzer and appropriate probing kit. The network analyzer will first be calibrated, in accordance with NIST standards and instrument instructions. One of the network analyzer probes will be connected to the common port, and a second to one of the switched ports. Ideally, the remaining RF port will be terminated with a 50 Ohm termination. Appropriate grounds will be connected. While not all grounds are required to be connected, at least one DC ground and one RF ground must be connected. A DC bias voltage of 3.3V will be applied to the source power port, and the control voltage will be connected to a power supply set to 0V. S Parameters will be measured and saved. Control voltage will be changed to 3.3V and S Parameters will be again measured. A probe will be moved from one switched port to the other, and the measurement will be repeated. Finally, the probe will be moved from the common port to a switched port, and the isolation will be measured with both 3.3V and 0V control voltage.

2. Probe Power Testing

The power handling of the switch will be measured with a signal generator and a spectrum analyzer or network analyzer with appropriate power capabilities. In the case of a network analyzer, the probes should be connected to the switch in a similar fashion to section 1, but a 20 dB attenuator will be placed in series with the common lead, or output from the common lead port will be disabled on the network analyzer (scalar mode). Similar measurements to section 1 will be made, with power continually being increased.

In the case of a spectrum analyzer and signal generator combination, the signal generator will be connected to a switched port, and the spectrum analyzer will be connected to the common port, and the remaining RF port will be terminated if possible. Appropriate triggering connections and settings will be made; dependent on the device models. The power and frequency will be swept, and the results recorded.

3. Probe Switching Time Measurement

The switching time will be measured using a high speed oscilloscope, an RF signal generator, and a signal generator capable of square wave output. A 3.3V DC power supply will be connected to the supply port of the switch, and appropriate ground connections will be made. The square-wave signal generator will be connected to the control voltage port, and set to produce a 3.3V P-P square wave. The oscilloscope will be connected to the common port,

and the signal generator will be connected to a switched port. The remaining RF port will be terminated. The trigger of the oscilloscope will be connected to the square wave signal generator's trigger. The period of the square wave generated will be adjusted so that it is greater than twice the switching time, but is not overly long. The envelope of the RF signal will be measured by the oscilloscope and used to calculate switching time. As only the envelope is being measured, the resolution of the oscilloscope will not need to be as high as the RF signal frequency.

4. Test board RF Parameter testing

A test board will be created, dependent on appropriate resource availability. It will have the following features: equal electrical length RF feeds, a through line with electrical length equal to twice the RF feed length, and pads to connect DC leads. 3.5MM/SMA connectors will be attached to provide connection to the network analyzer.

Prior to the MMIC being bonded to the test board the electrical length of the RF feeds and the through line will be measured using a network analyzer's time domain functionality. The loss of the through line will be measured and appropriate de-embedding parameters will be calculated from the measured results. Similar tests to those in sections 1 and 2 will be performed, and the results will be de-embedded from the test board using the parameters previously calculated.

Conclusions

While the simulated results were reasonable, and produced a functional device, they were not as good as anticipated. A major source of the problem was the selection of enhancement mode FETs for use in the switch, which significantly reduced the power handling capabilities. Further research reveals that an intriguing solution could have been a hybrid series-shunt topology. This topology has a series FET in one switch arm, and a shunt FET in the other, and allows for a single control voltage to be used for both arms, with depletion mode FETs. The disadvantage to this solution is the loss of symmetry on the RF path, but, dependent on application, this is not always an important factor.

MMIC Design Final Project
Balanced Low Noise Amplifier
on 4 mil GaAs

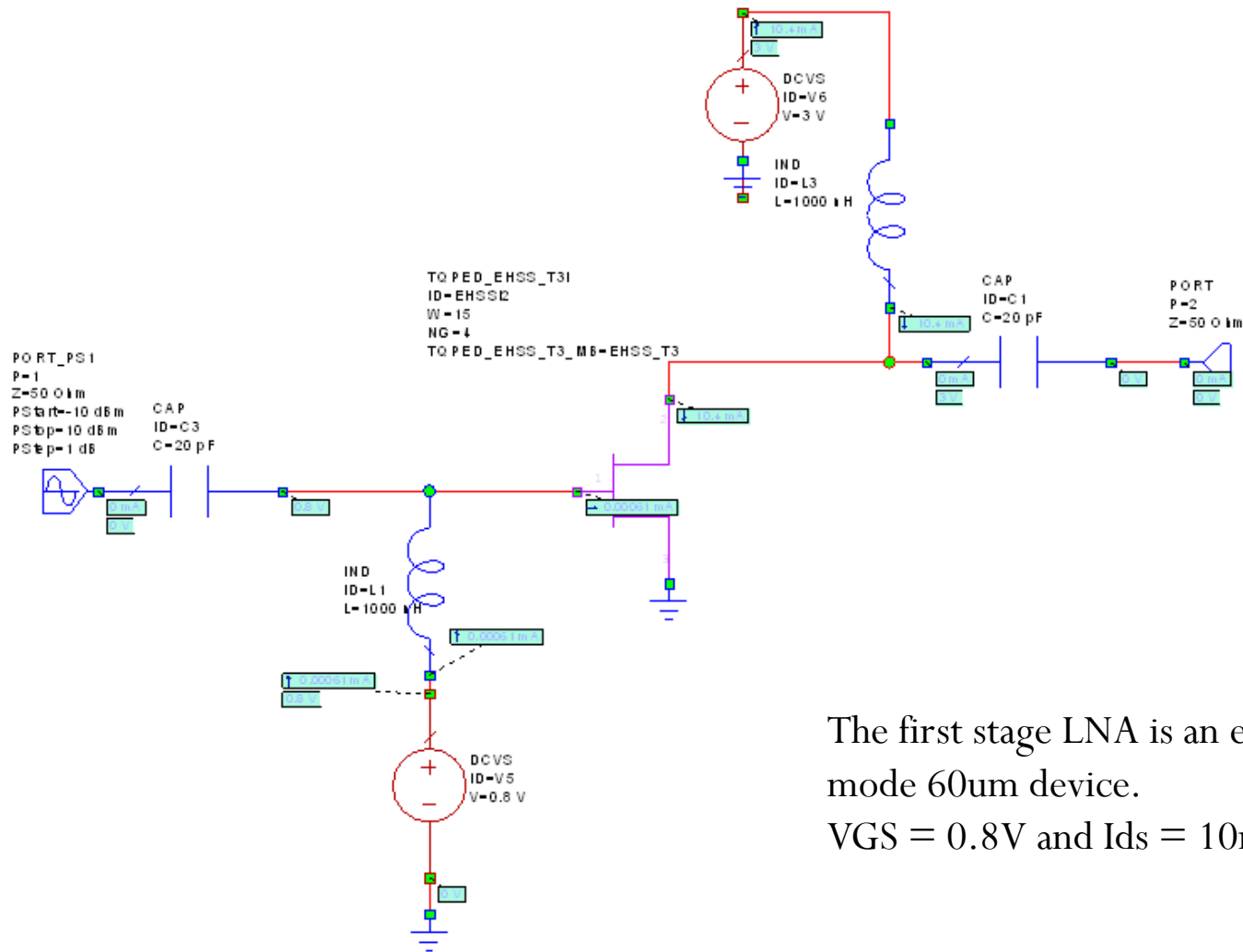
Wade Freeman

Specifications

- System Specifications
 - $F_c = 5.8 \text{ GHz}$
 - $\text{Gain} \geq 22 \text{ dB}$
 - $\text{NF} < 1.5 \text{ dB}$
 - $\text{BW} = \pm 250 \text{ MHz} @ F_c$
 - $\text{Passband Ripple} = 1.5 \text{ dB}$
 - $\text{Supply Voltage} = 3 \text{ v}$
 - $\text{Current Consumption} = 22 \text{ mA}$

First Stage Design

Biased FET with Ideal Elements

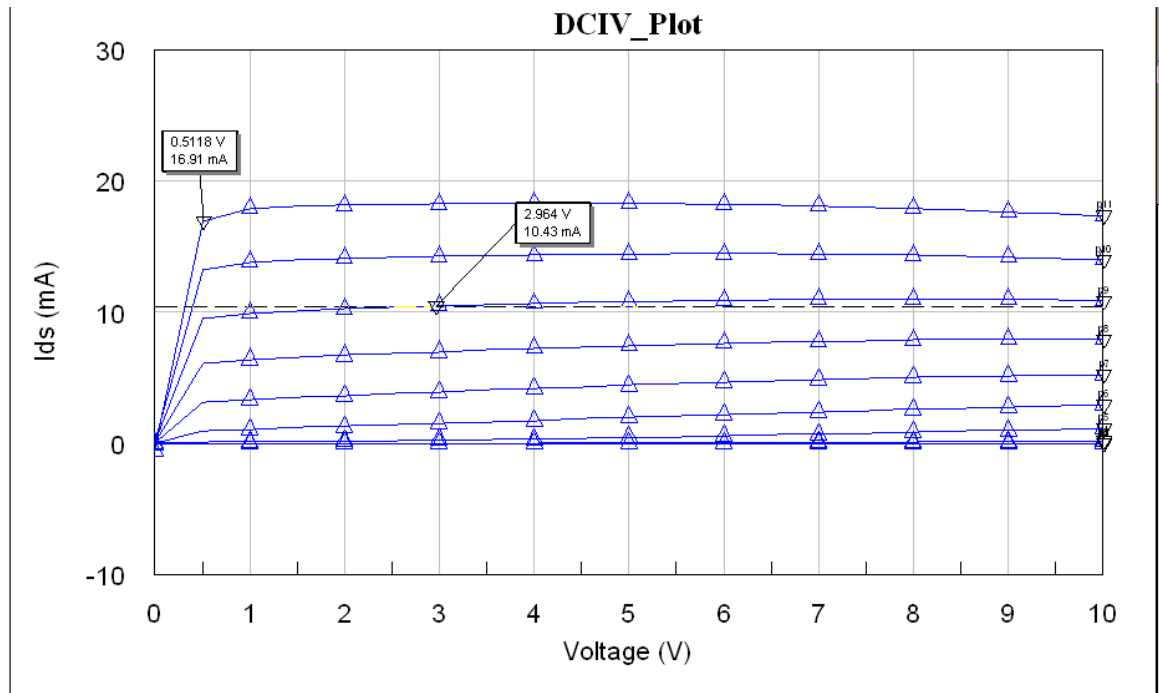


The first stage LNA is an enhanced mode 60um device.

$V_{GS} = 0.8V$ and $I_{ds} = 10mA$

First Stage Design

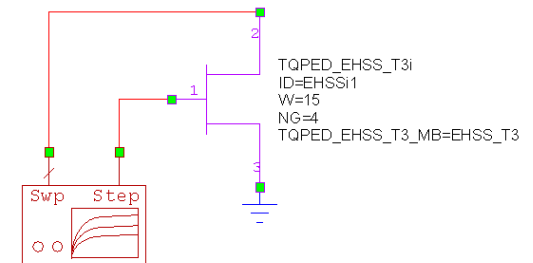
DCIV Curve



The desired bias point for a 3V Vdd is 0.8V.

TQPED_PLSS_T3_MB
ID=PLSS_T3

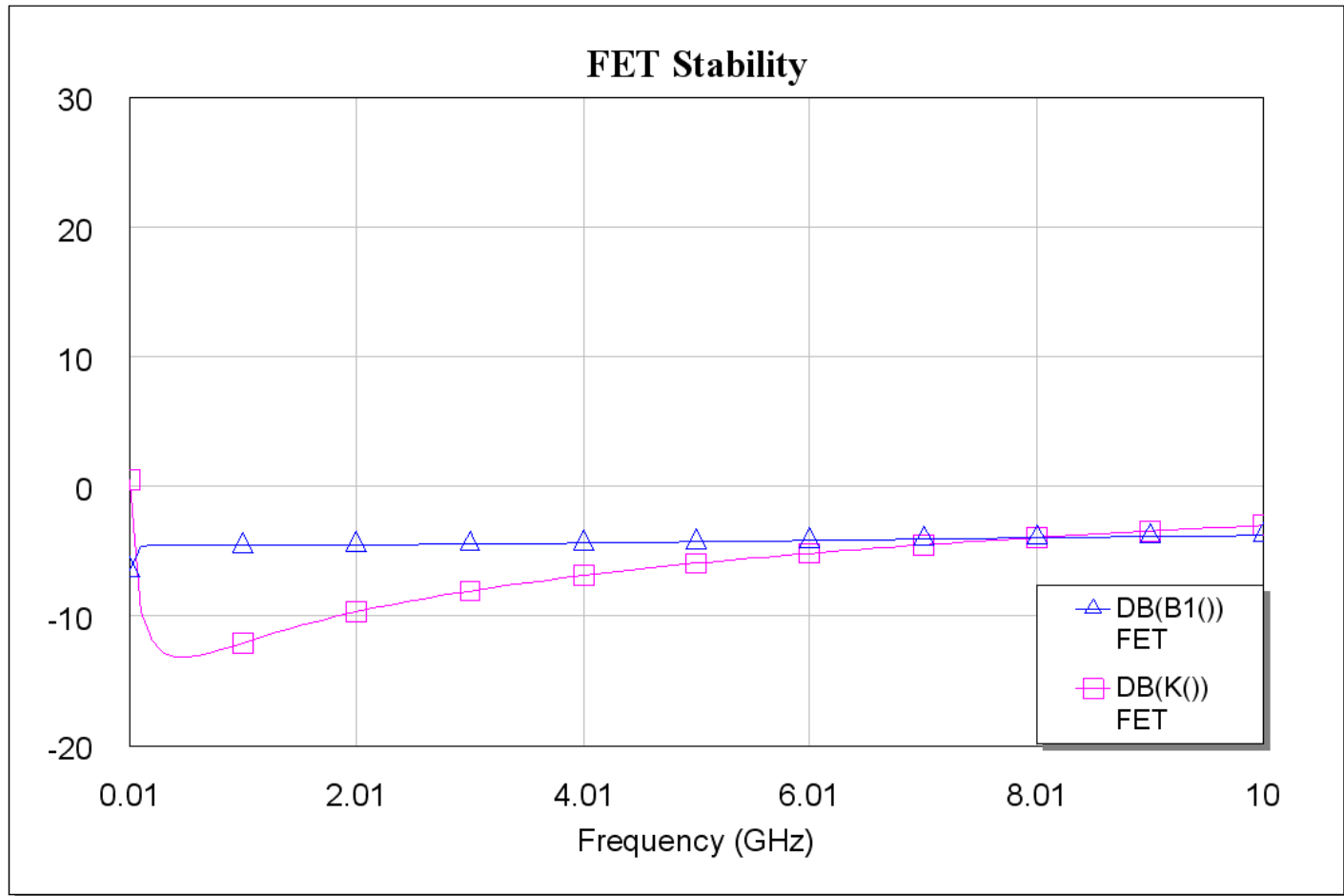
MODEL



IVCURVE
ID=IV1
VSWEEP_start=0 V
VSWEEP_stop=10 V
VSWEEP_step=5 V
VSTEP_start=0 V
VSTEP_stop=1 V
VSTEP_step=0.1 V

First Stage Design

Stability



The FET is naturally highly instable.

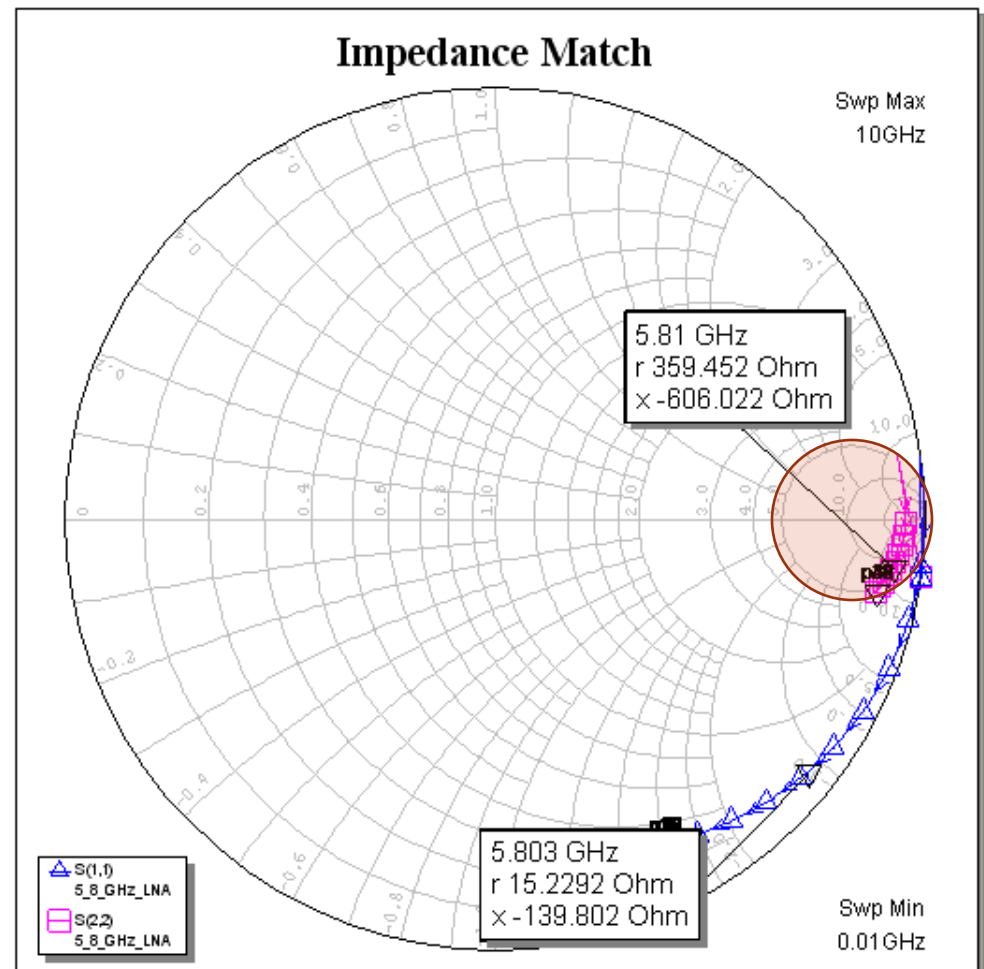
First Stage Design

Unmatched Impedance

This is a plot of the unmatched and unstabilized 60um FET with a non-linear simulation.

The output impedance does raise some concern because it has a high impedance and will be harder to match.

* Note: the orange ring is intended to emphasize the “Hard to Match Area” of the Smith Chart.



First Stage Design

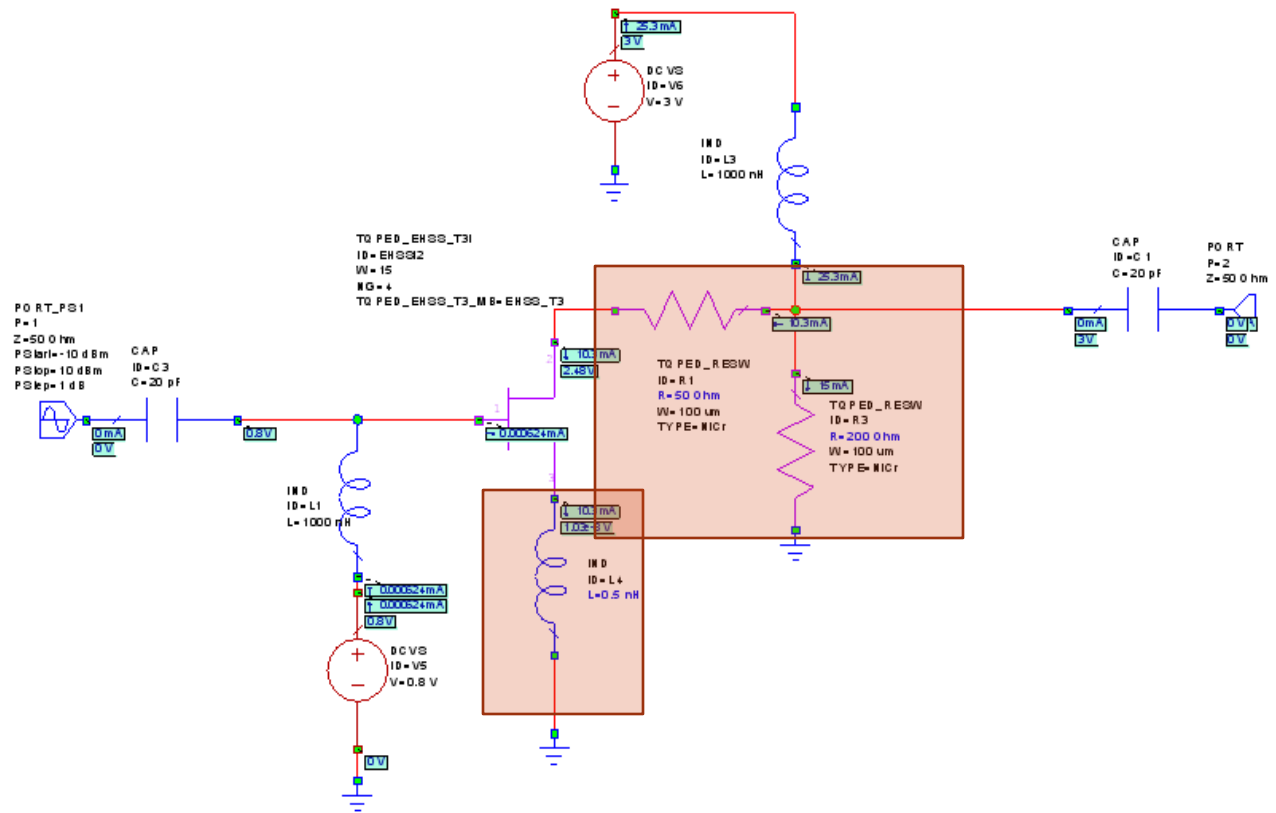
Ideal Stability

The first stage FET was stabilized using ideal elements.

A 0.5nh inductor in the source path of the FET.

Because this is an LNA design, a 50ohms series and 200 ohm shunt resistors were added to the drain side of the FET.

The down side to this matching network is that the shunt resistor will draw current and this is intended to be a low power design.



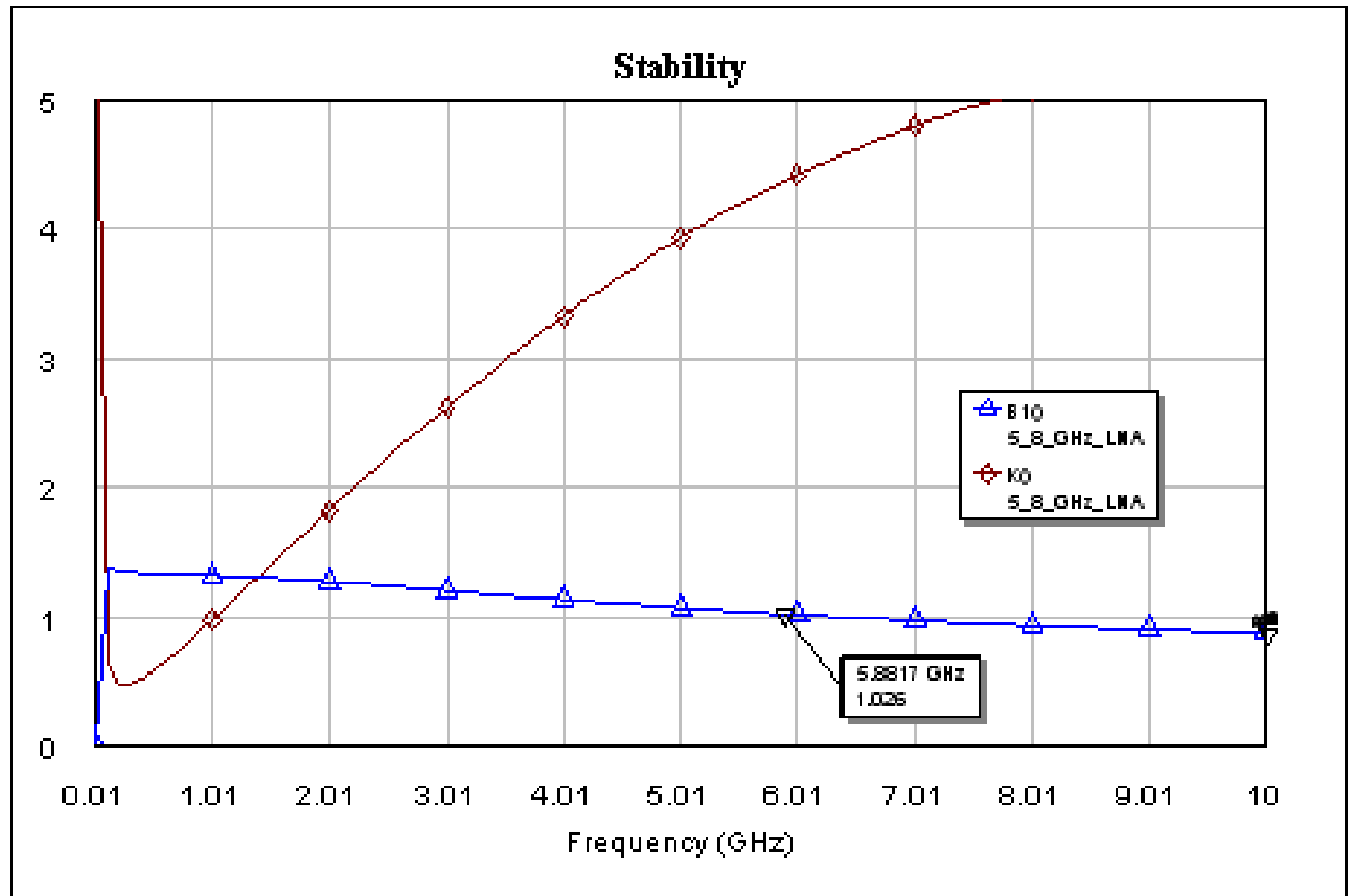
First Stage Design

Stability Plot

The goal for stability is to have $K > 1$ and $B1 > 0$.

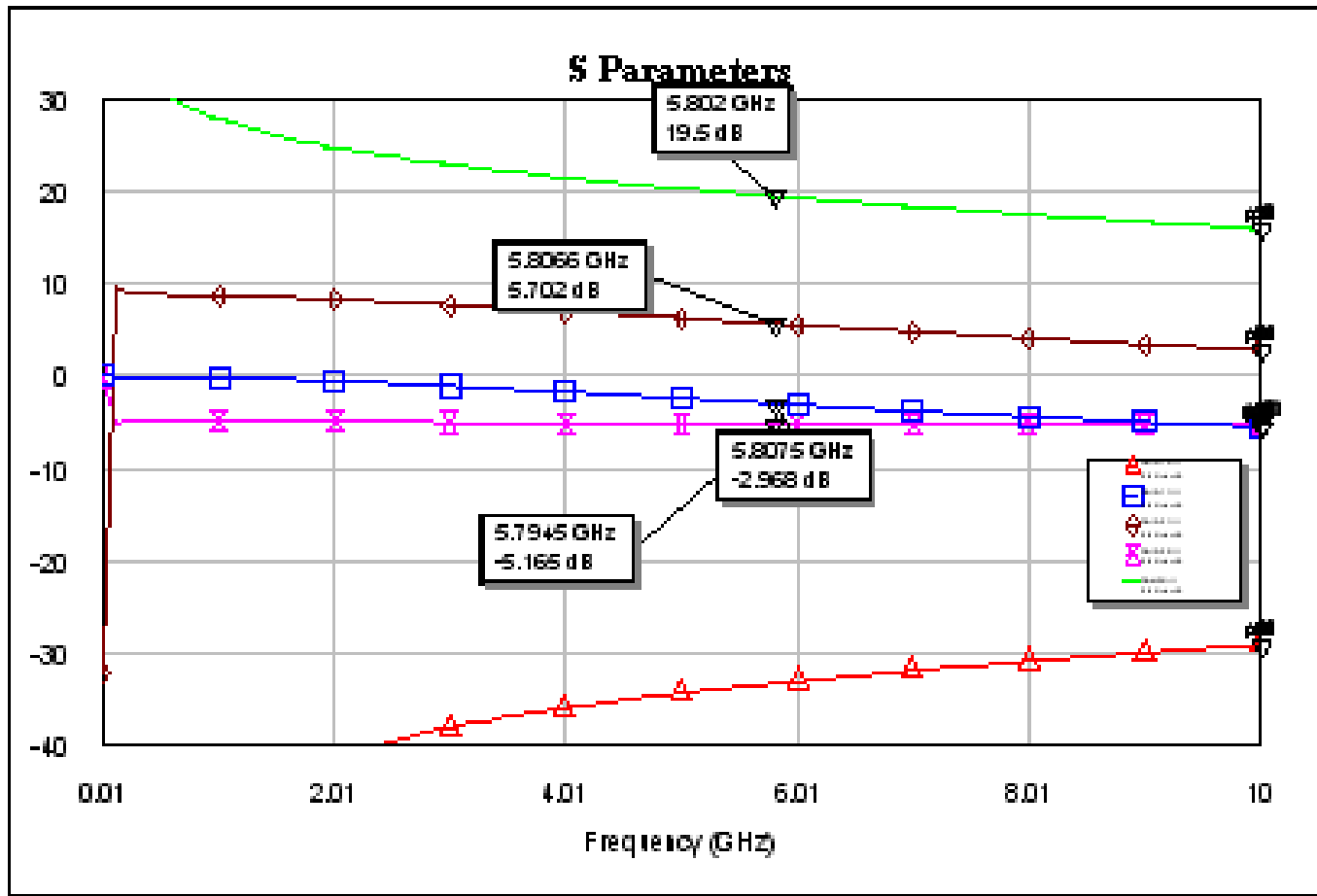
This design is conditionally stable over the entire pass band but seems to have some issues with stability around 1GHz.

Stability will be reevaluated after the Bias Tee and Matching Networks have been added



First Stage Design

S-Parameters



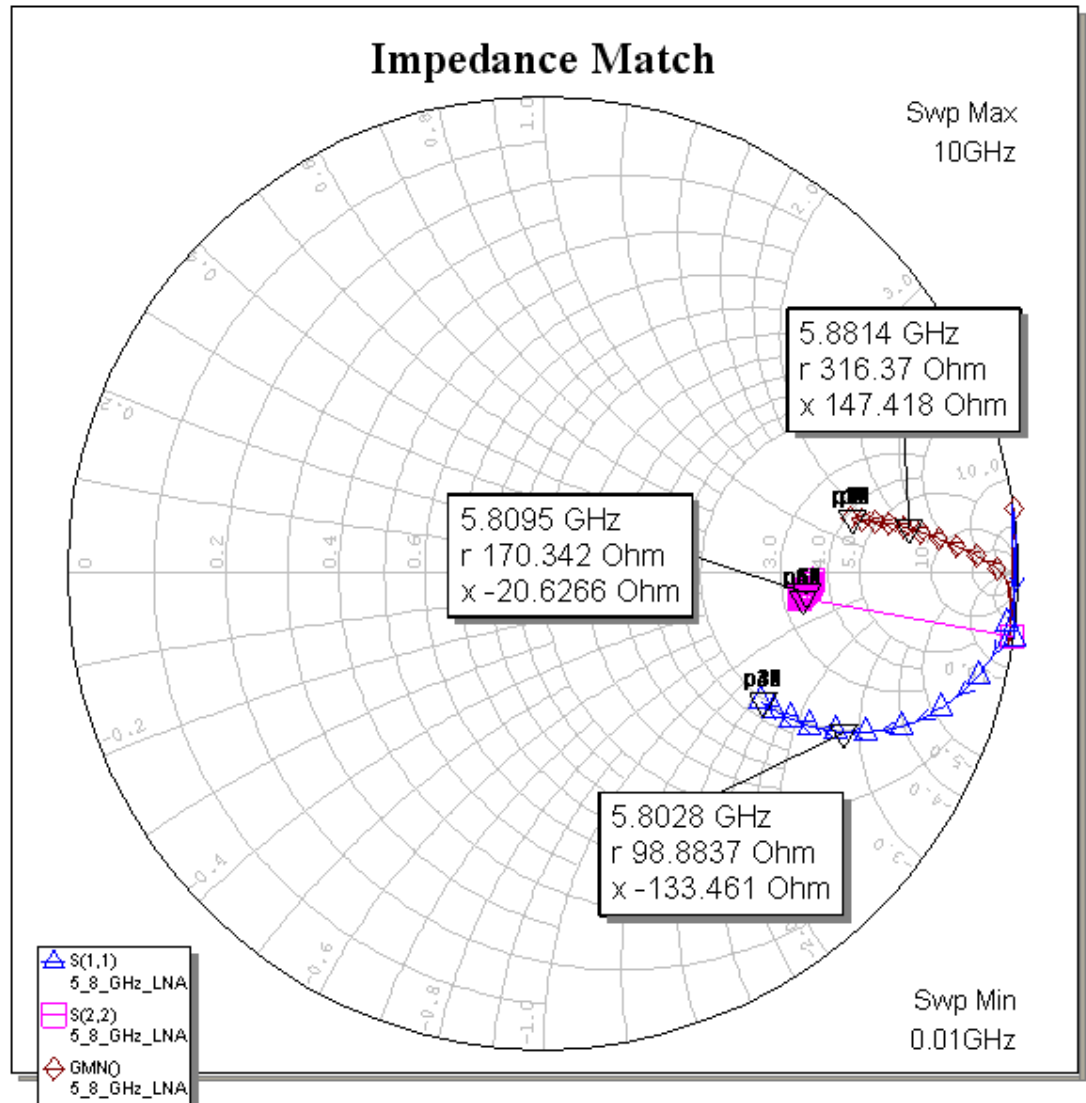
The maximum gain of the stabilized FET is 19.5 dB.

First Stage Design

Stabilized Impedance Plot

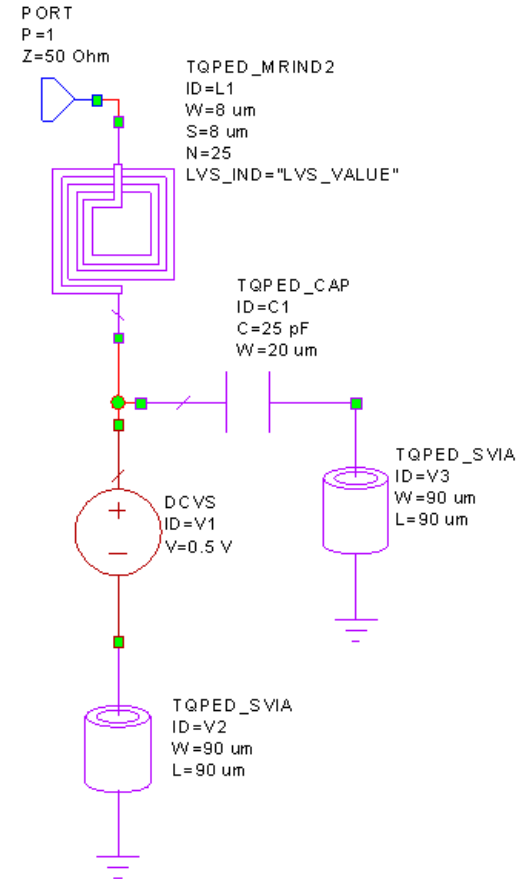
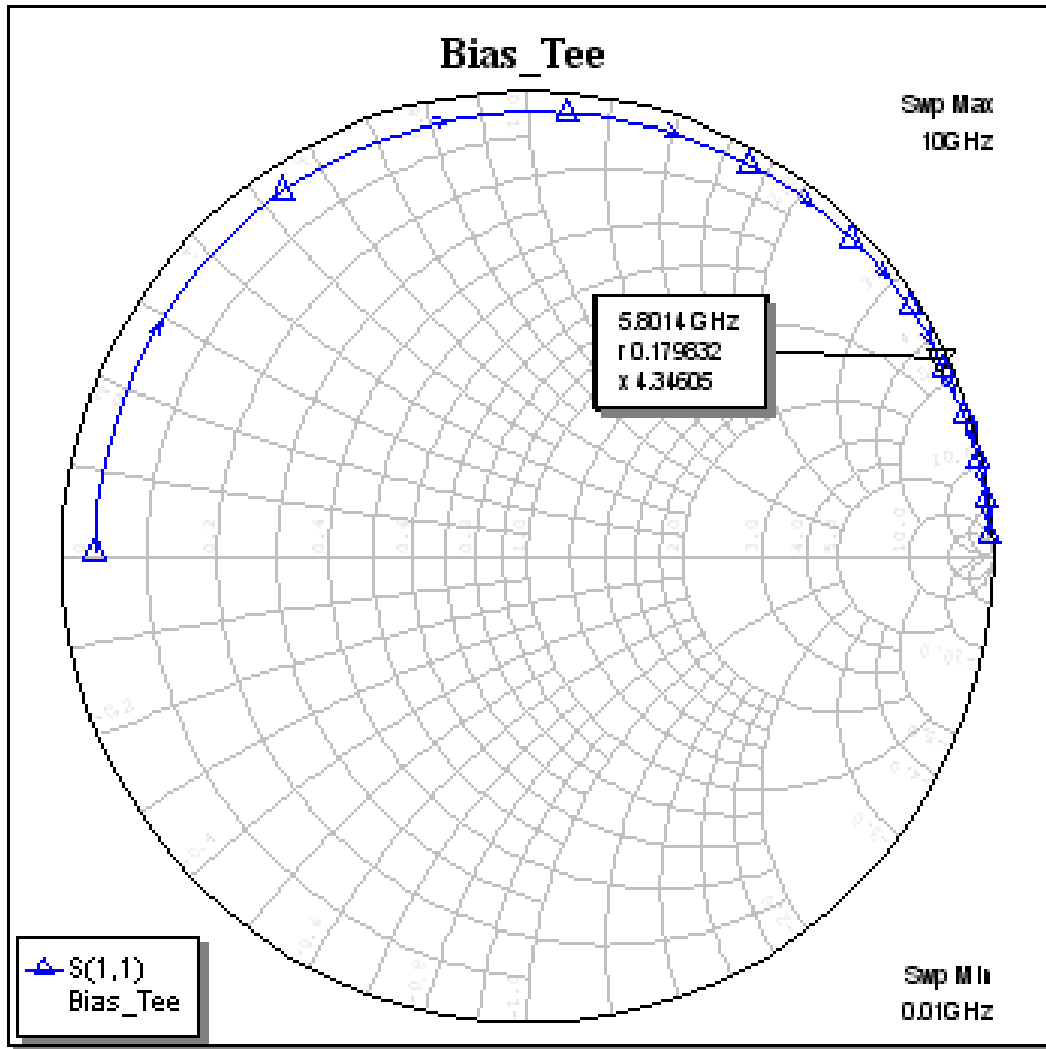
The stabilizing elements has shifted the impedance match.

To achieve the minimum possible noise figure, Gamma Optimum* will be transformed to 50 ohms.



First Stage Design

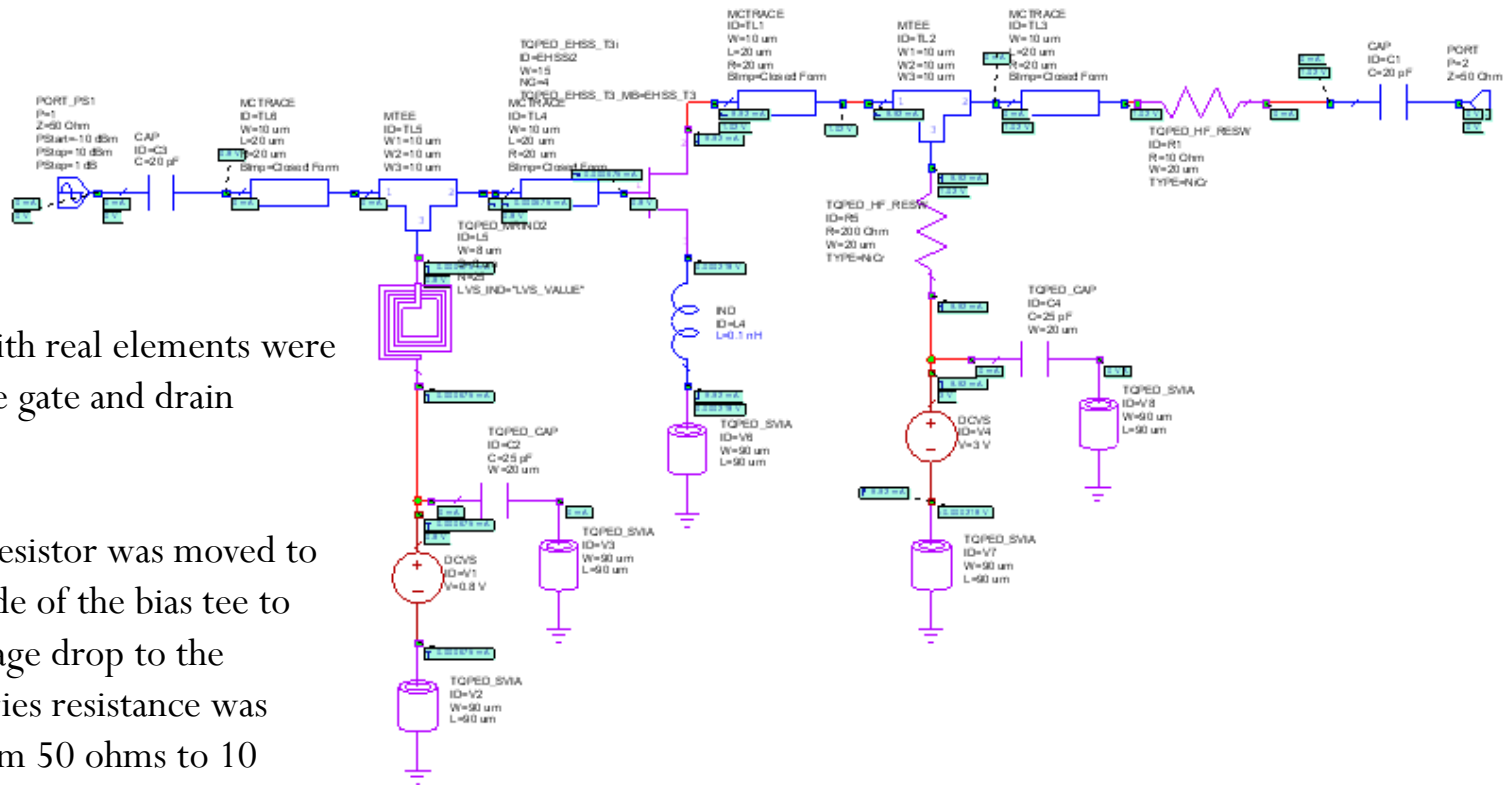
Bias-Tee



The Bias-Tee was designed using elements from the TQPED Library.

First Stage Design

Schematic with Bias-Tees



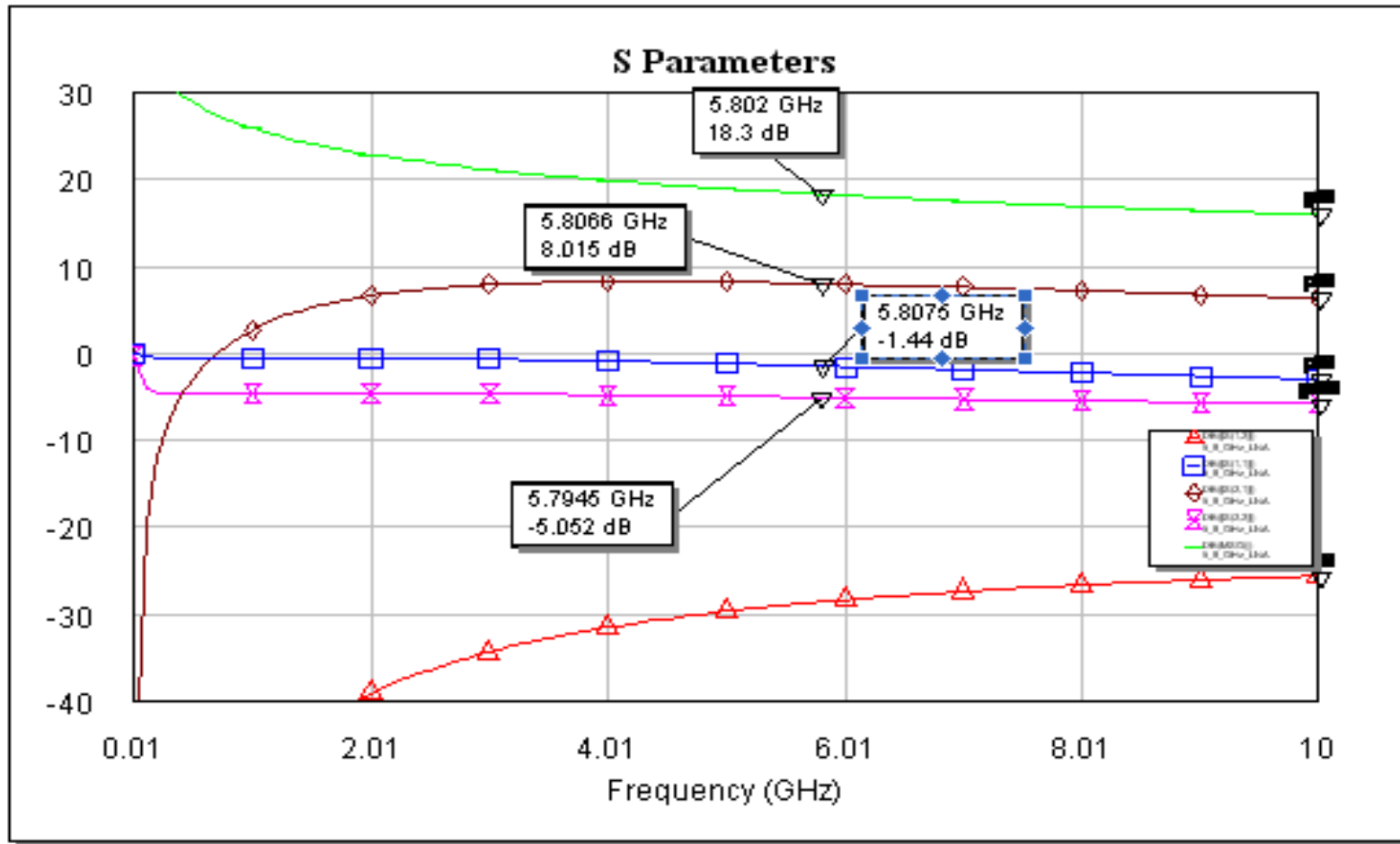
Bias-Tees with real elements were added to the gate and drain supplies.

The series resistor was moved to the other side of the bias tee to avoid a voltage drop to the Source. Series resistance was reduced from 50 ohms to 10 ohms.

Drain voltage is reduced to 1.02V and the drain current is 9.92mA.

First Stage Design

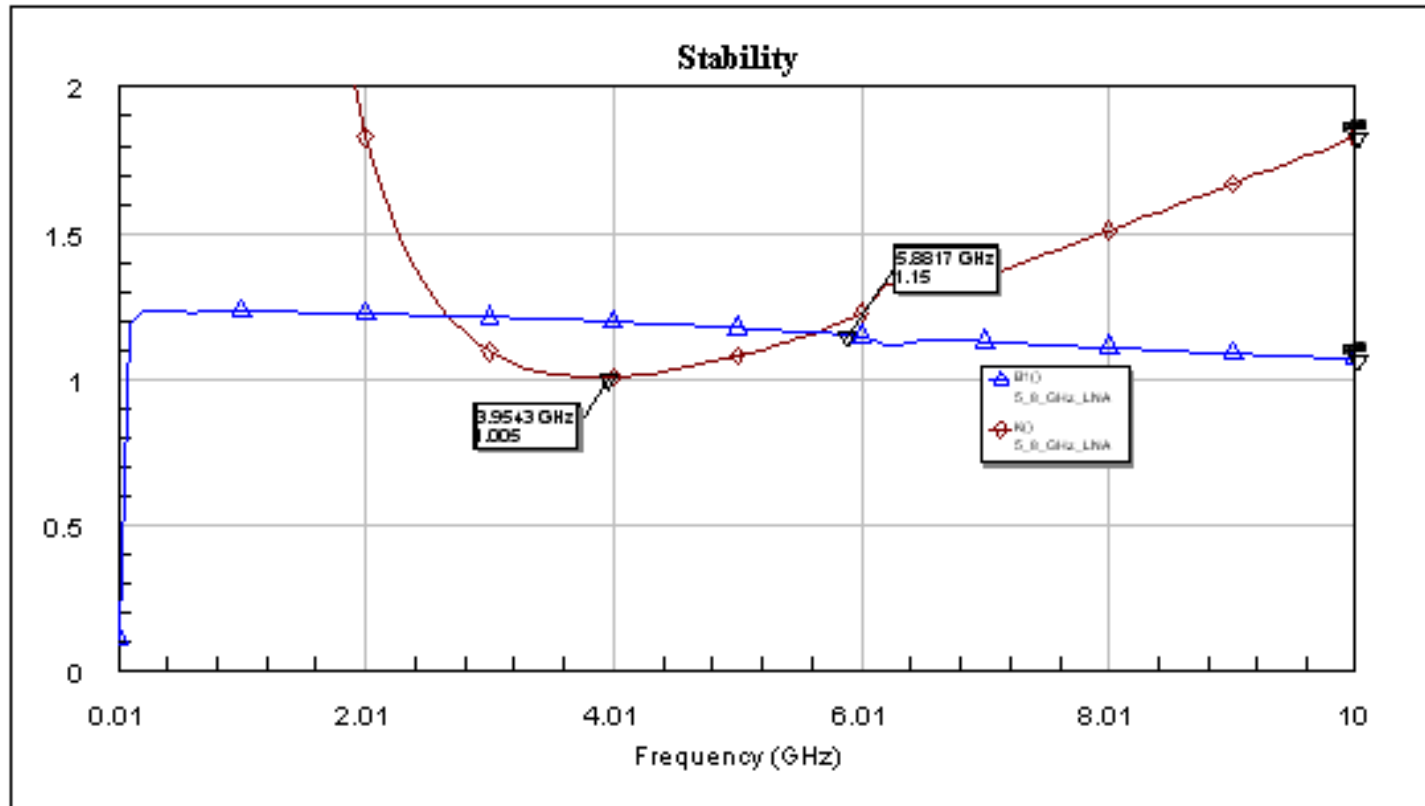
S-Parameter Plot with Bias-Tees



The First stage maximum gain is 18.3 dB. The goal is 11-12dB with a low noise figure. There should be enough overhead to meet both the desired gain and noise figure.

First Stage Design

Stability with Bias Tees

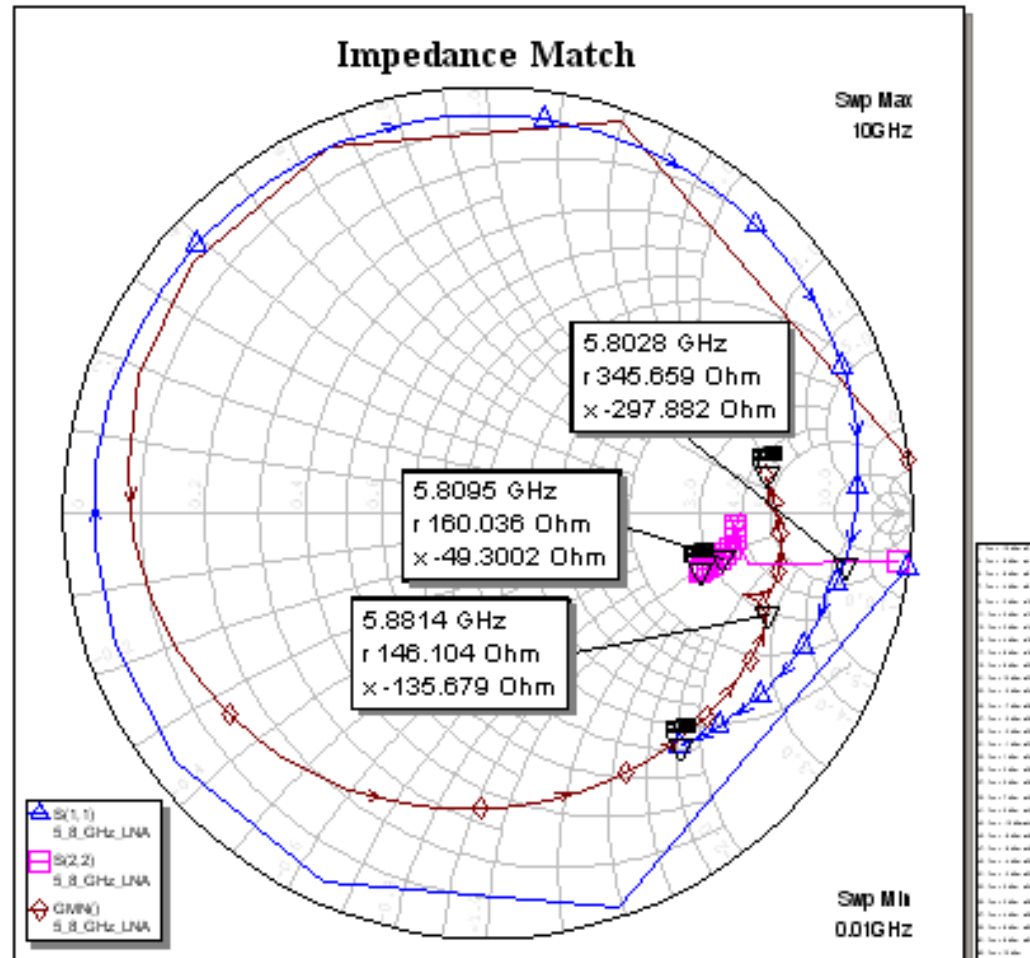


The goal for stability is for $K > 1$ and $B1 > 0$.

First Stage Design

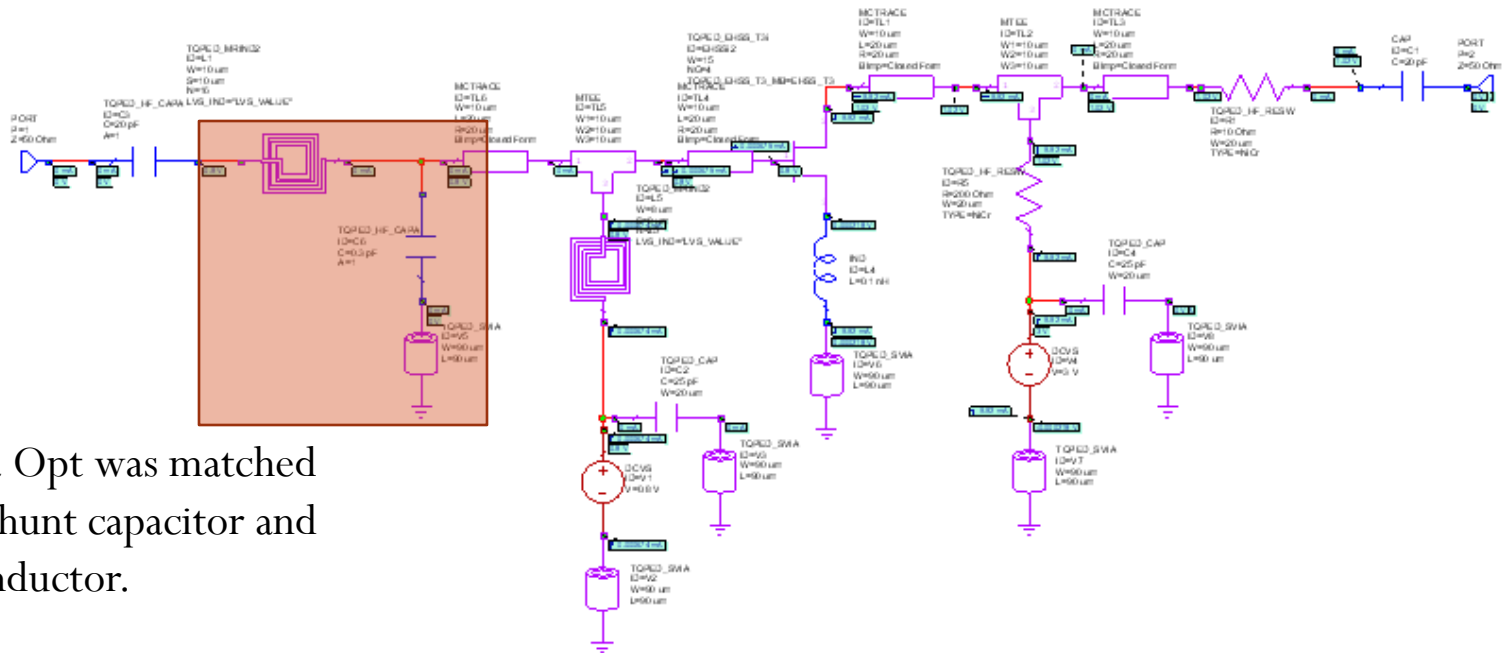
Impedance Plot with Bias Tees

The bias tees seemed to have spread out S11 and Gamma Opt.



First Stage Design

Input Matching Network

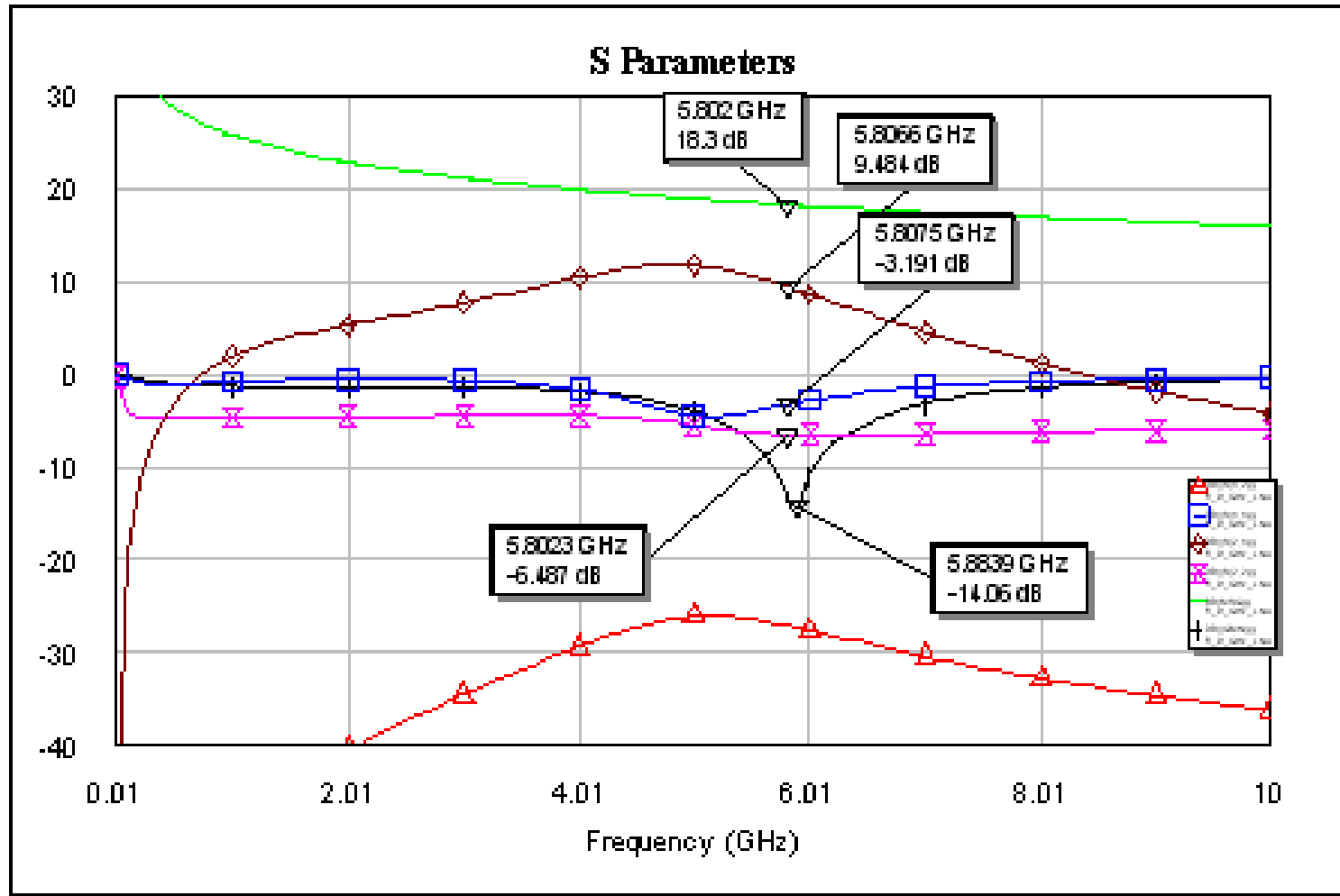


Gamma Opt was matched with a shunt capacitor and series inductor.

Matching elements were from the TQPED library.

First Stage Design

Input Matching Network

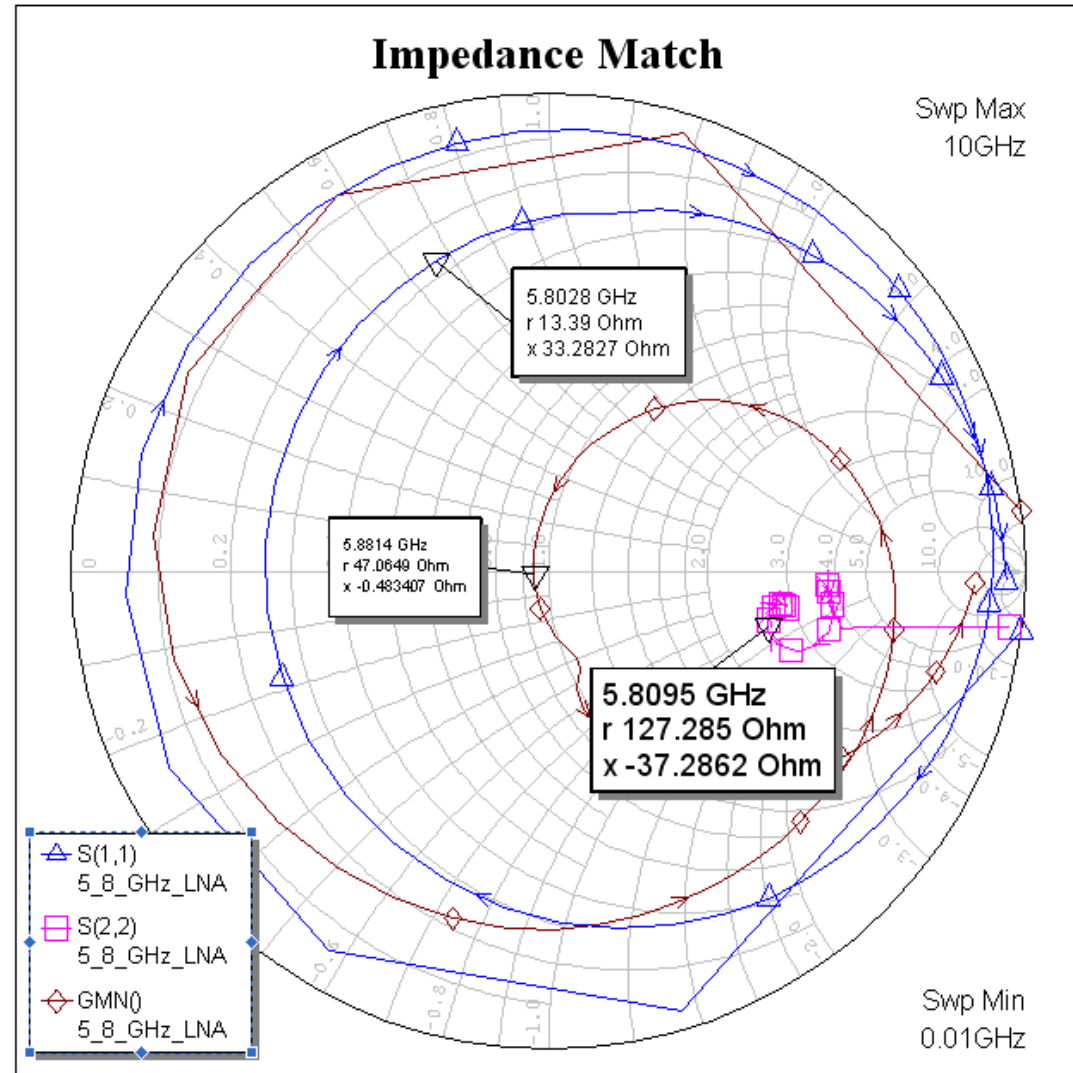


The black line is Gamma Opt. The gain is low but should improve once the OMN is added. The flatness of S21 is a concern.

First Stage Design

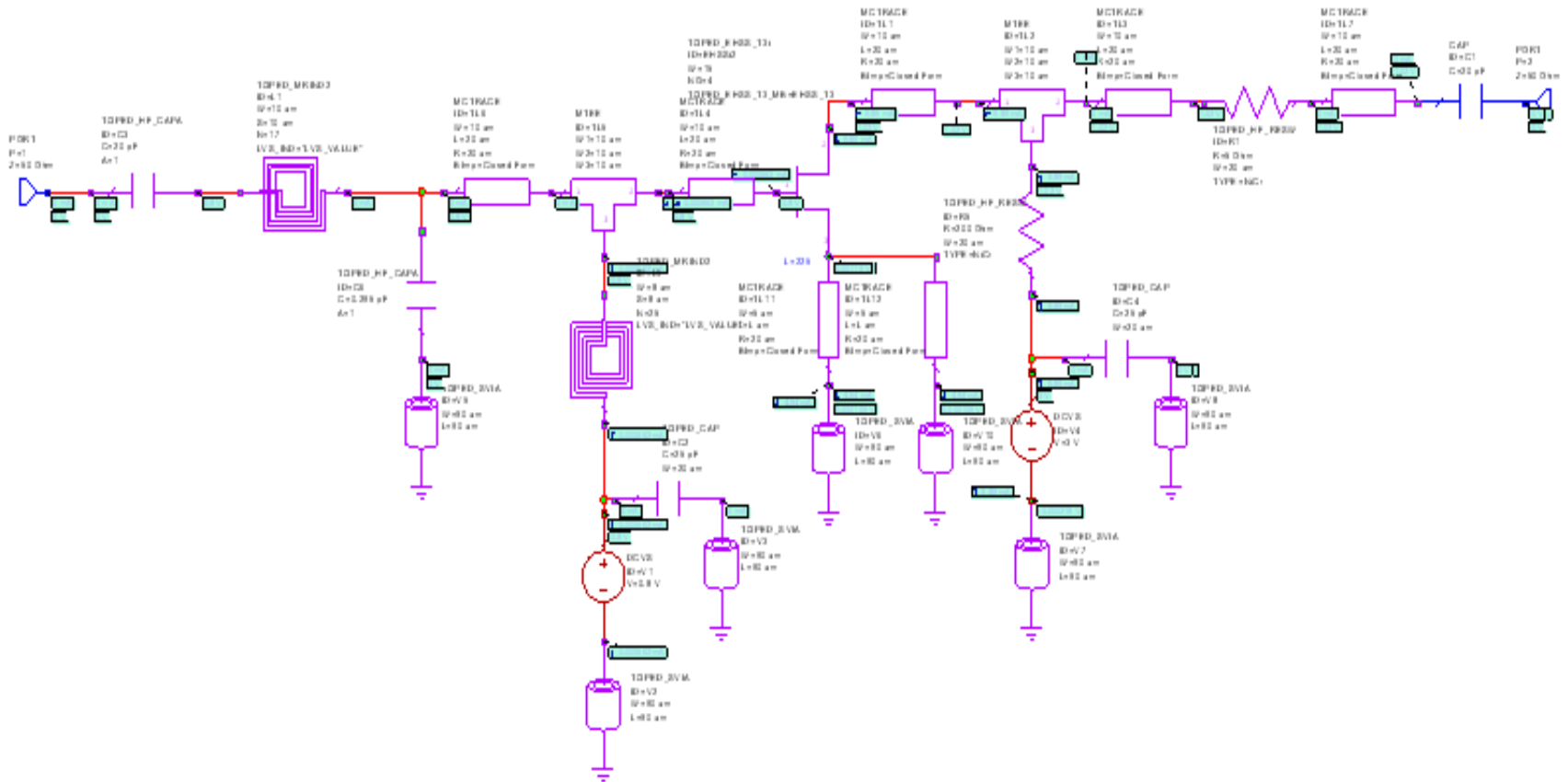
Input Matching Network

The red trace is a plot of Gamma Opt. It is well matched to 50 ohms.



Two Stage Design

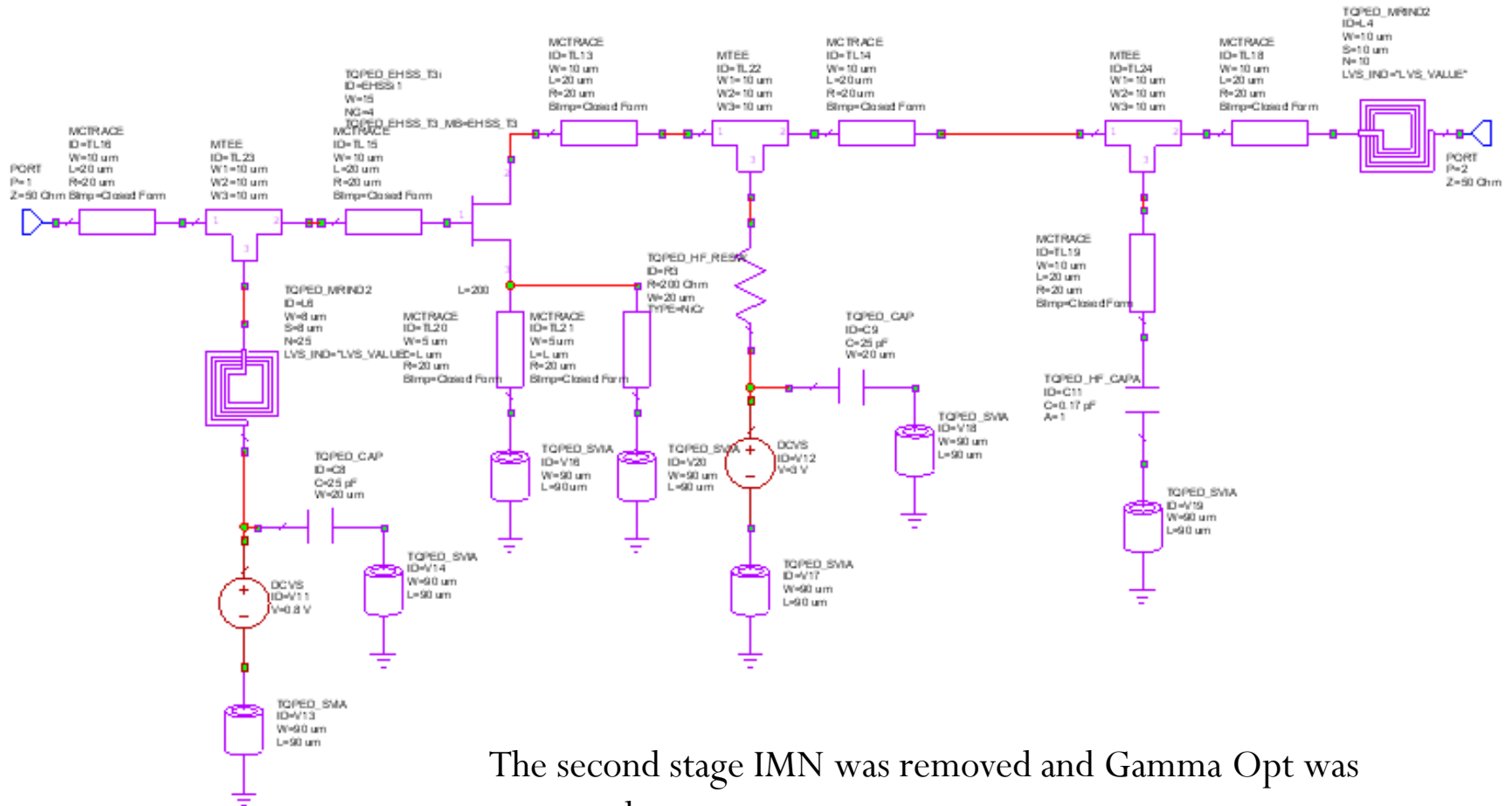
First Stage without OMN



With the IMN connected the output was measured.

Two Stage Design

Second Stage without IMN

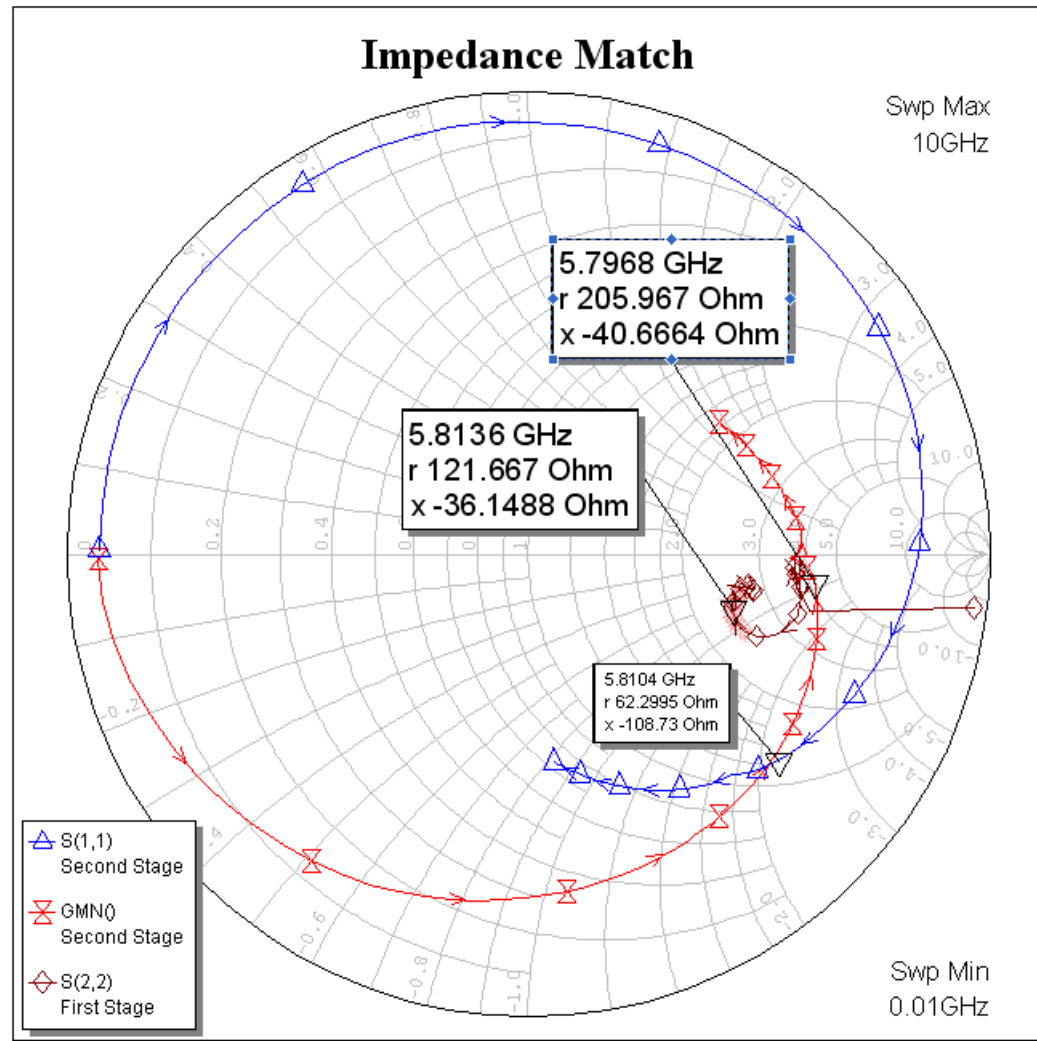


The second stage IMN was removed and Gamma Opt was measured.

Two Stage Design

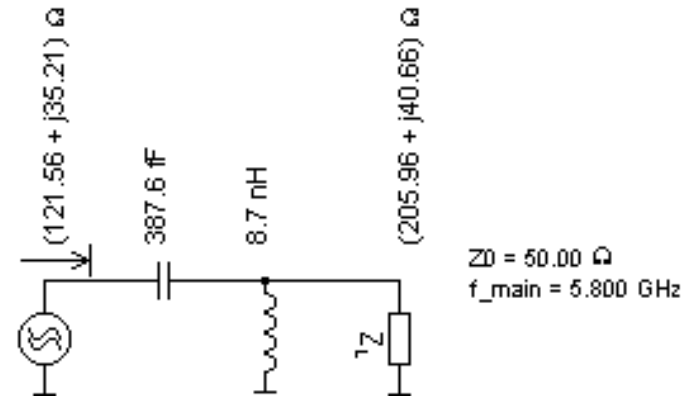
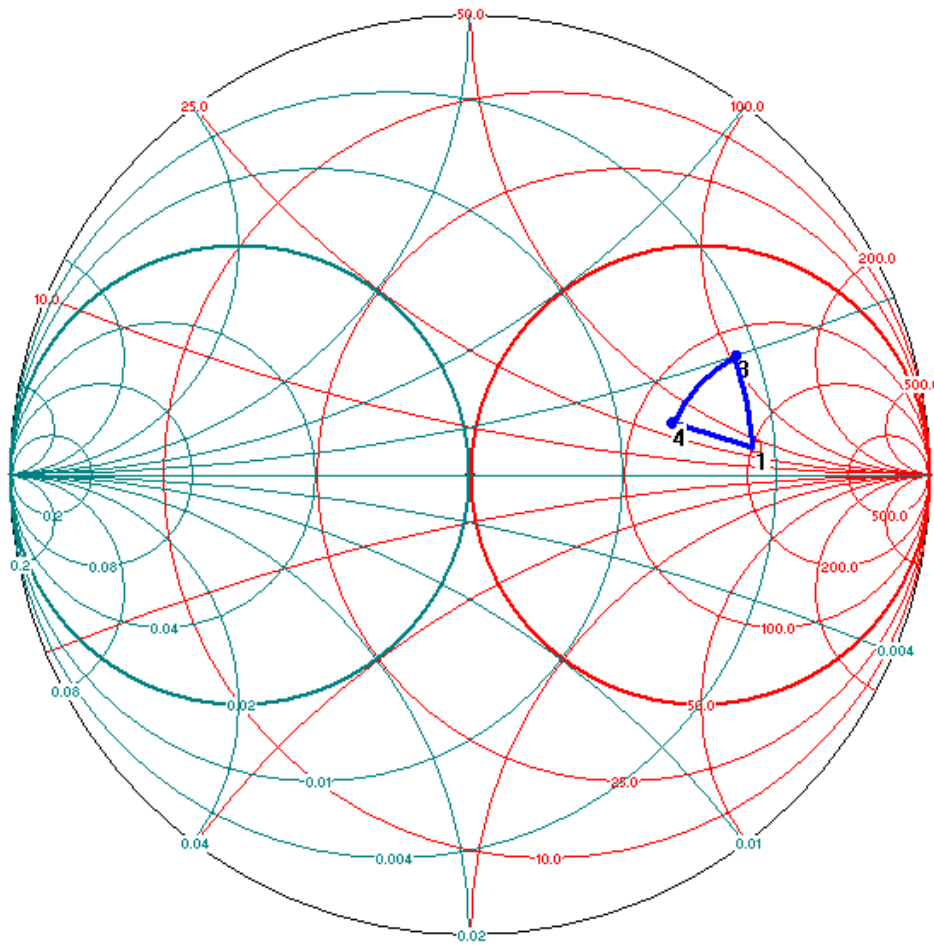
Inner-Stage Matching Network

The goal of the matching network between the two stages is to match S_{22}^* (121.66 + 36.15 ohm) of the first stage to Γ_{opt}^* (205.96 + 40.6 ohm) of the second stage.



Two Stage Design

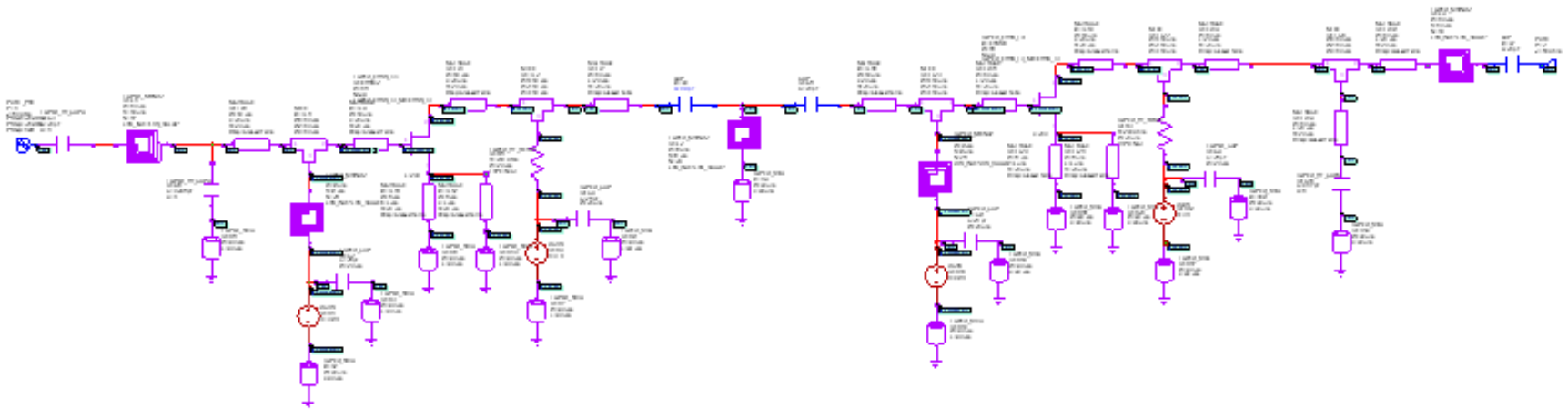
First Stage OMN Second Stage IMN



This is the ideal matching network which transforms the first stage S_{22}^* to the second stage Γ_{Opt}^* .

Two Stage Design

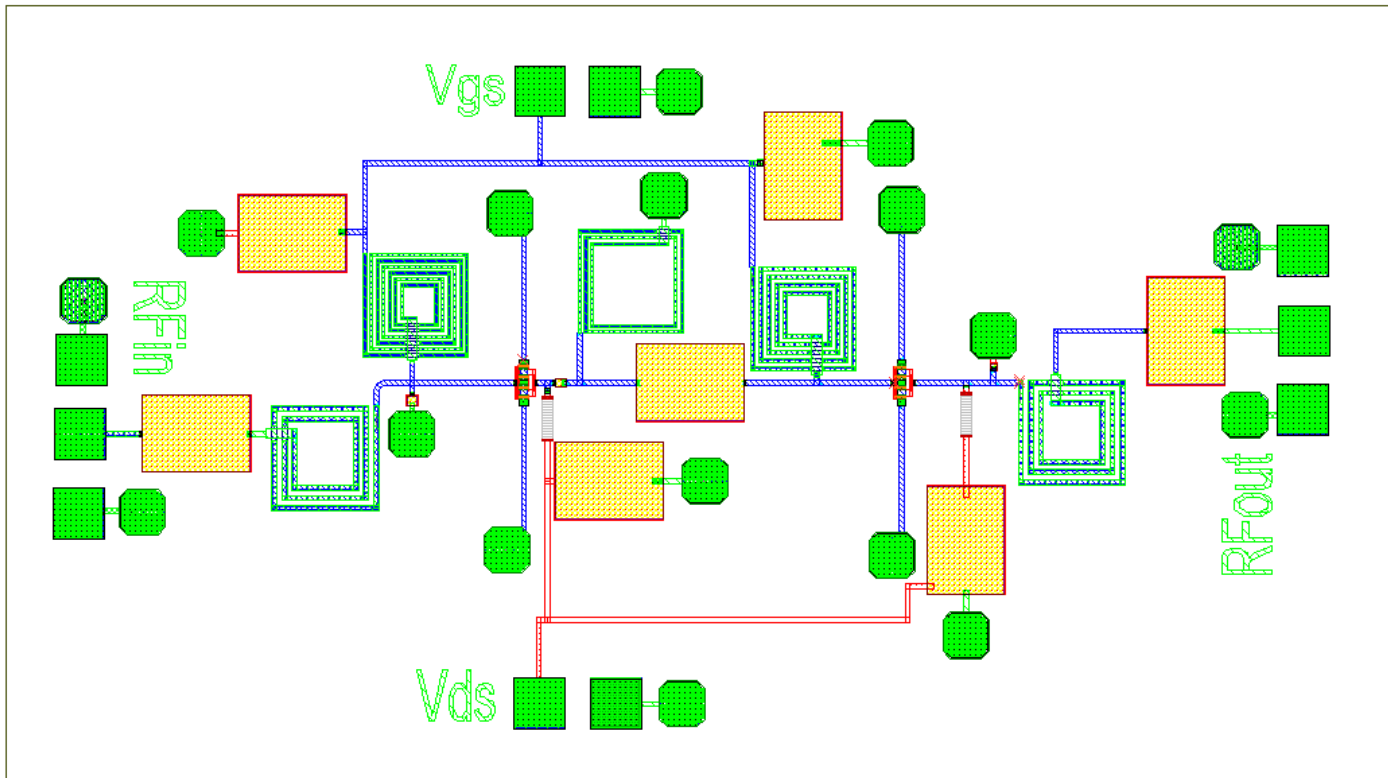
Two LNA's Cascaded Together



The first stage LNA was copied and cascaded with itself. The OMN of the first stage was removed and the INM network of the second stage was removed. The goal was to design a conjugate match between the output of the first stage LNA and Gamma Opt of the second stage LNA. Above is the cascaded network with the inner-stage matching network. Because the stability improved with cascading the two LNA's, the 10 ohm series resistors were removed which helped the noise figure performance.

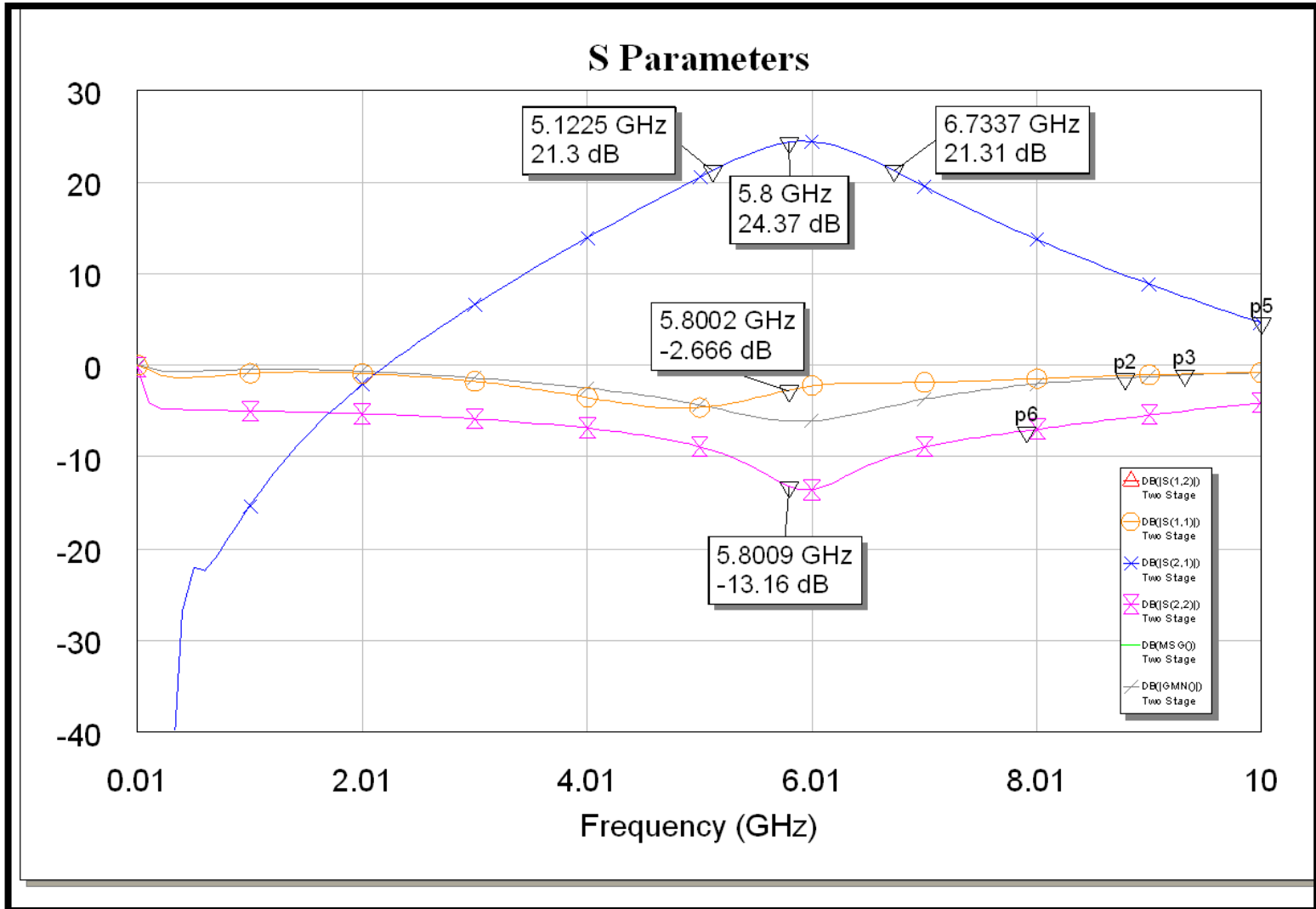
Two Stage Design

Two Stage Layout



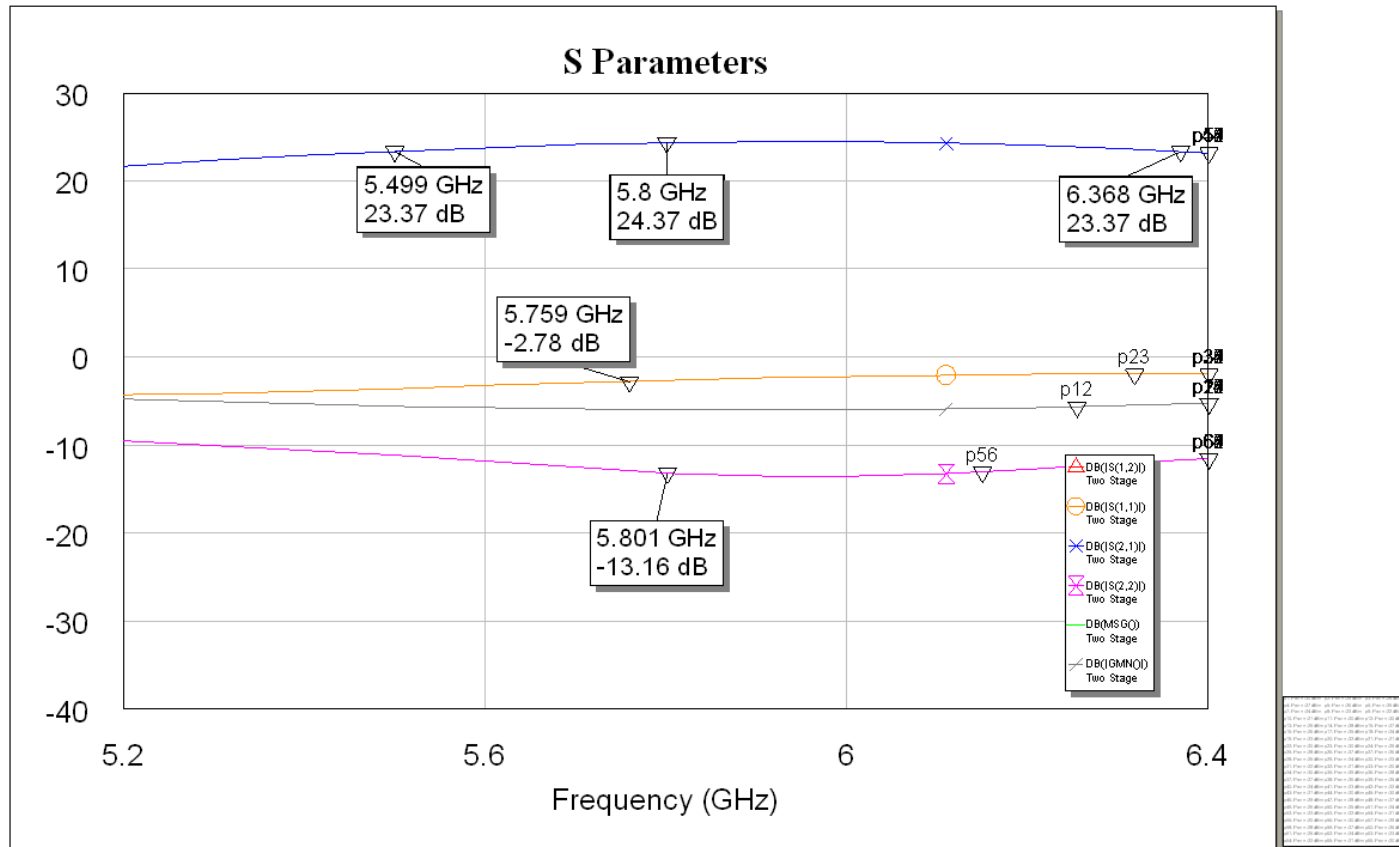
Two Stage Design

S-Parameters



Two Stage Design

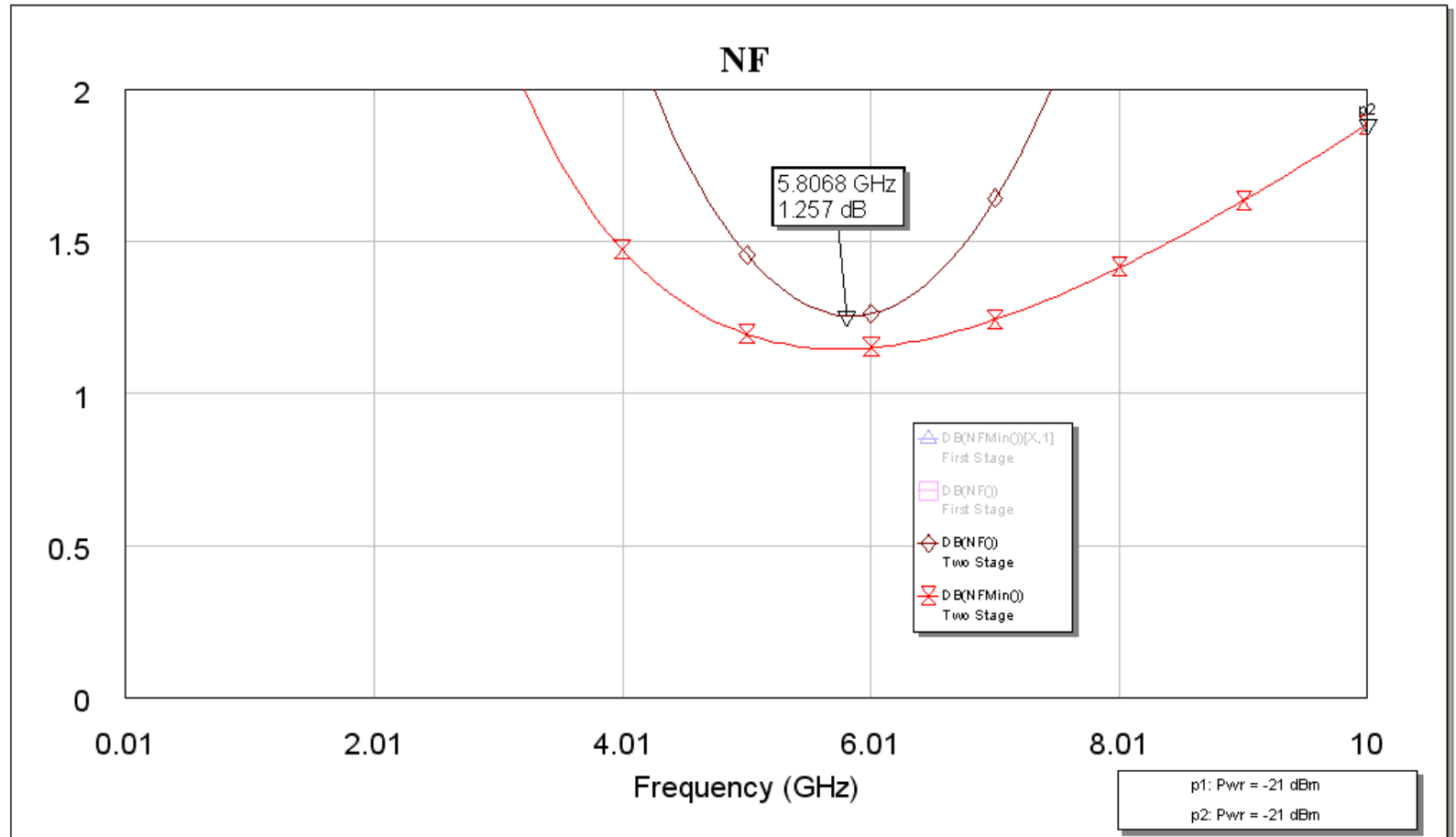
Pass Band Bandwidth



The 1 dB bandwidth is approximately 800 MHz (5.5 GHz to 6.3 GHz)

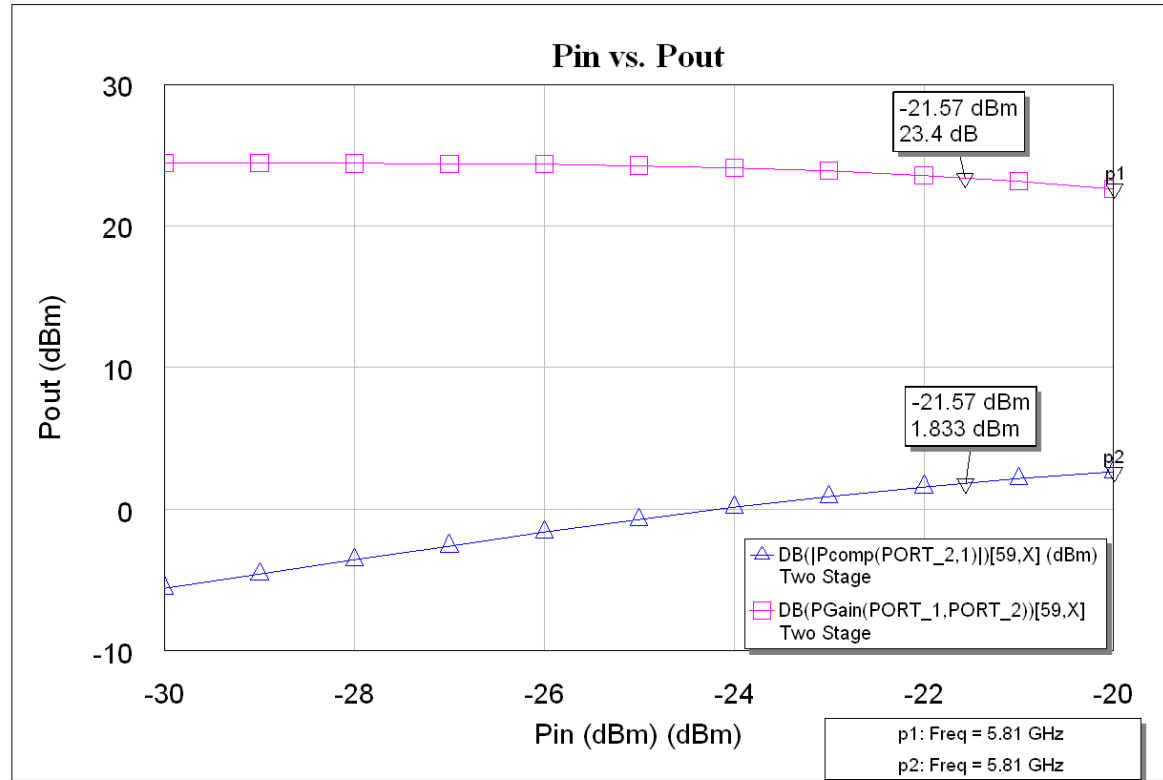
Two Stage Design

Noise Figure



Two Stage Design

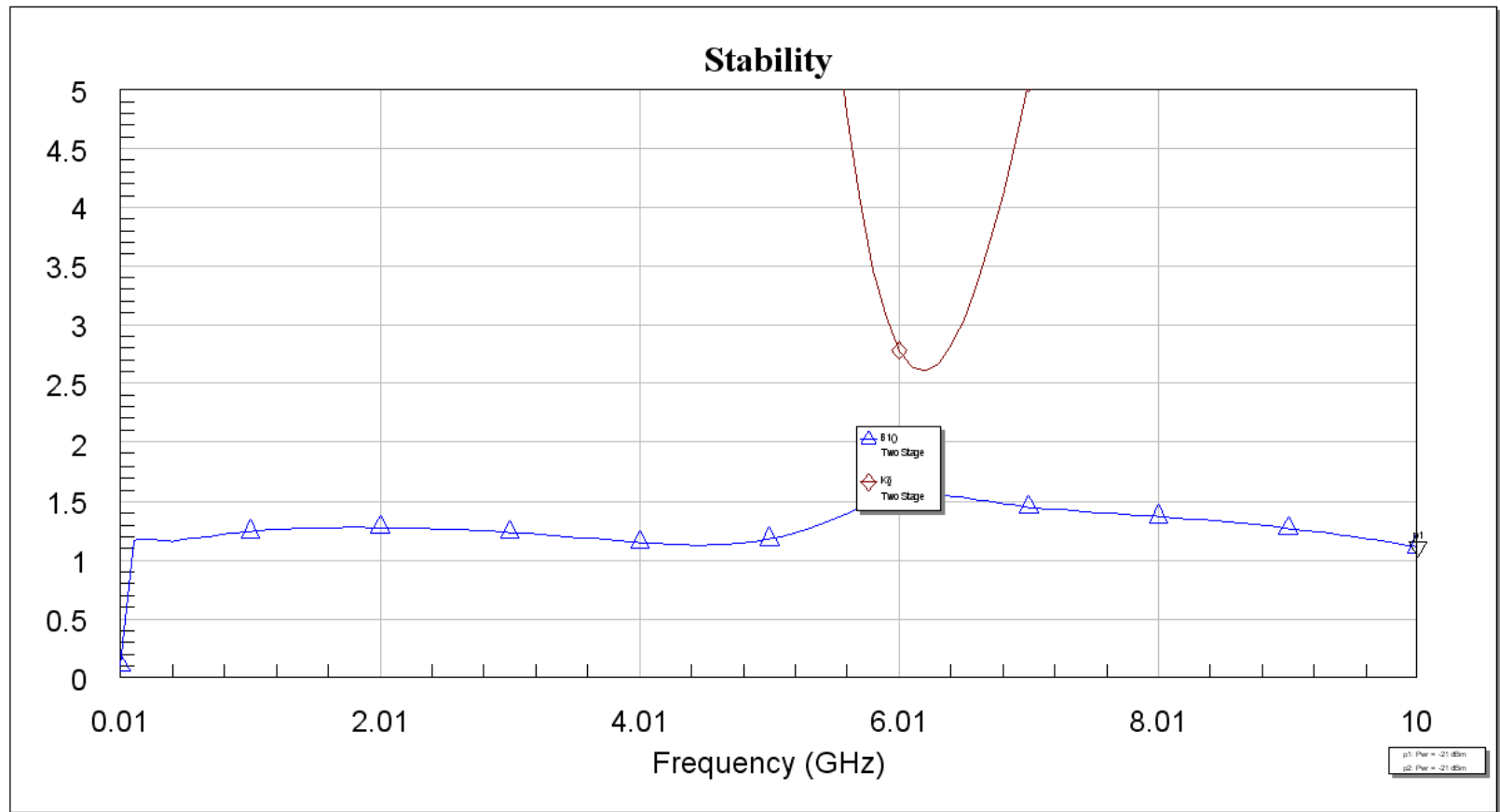
P1dB and Gain Measurements



The output P1dB point is estimated to be 1.8 dBm with a gain of 23.4 dB.

Two Stage Design

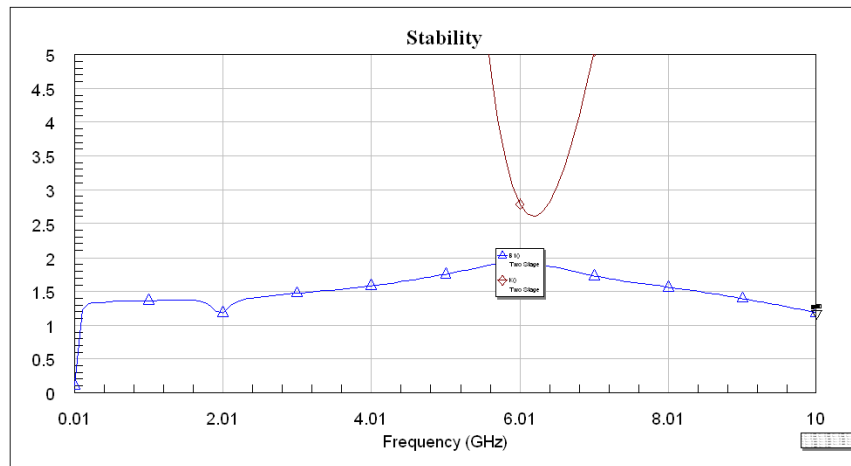
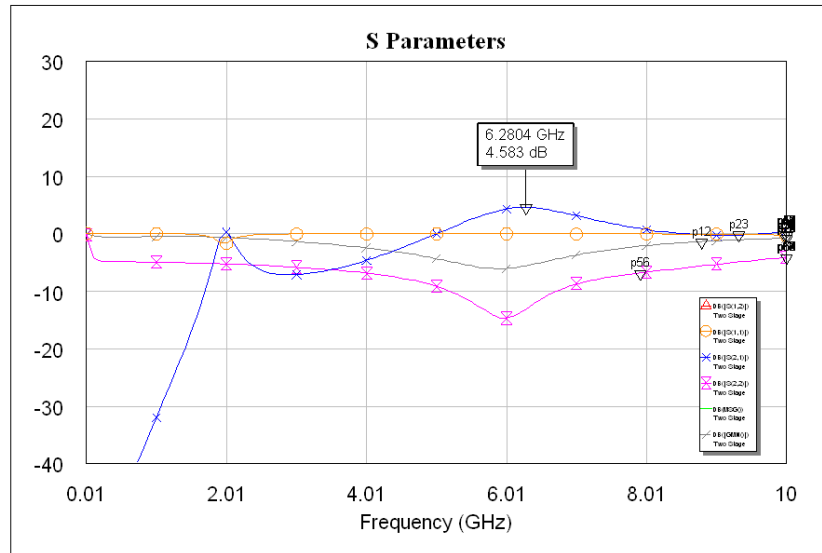
Stability Performance



Input Impedance Analysis

Low Resistance High Capacitance

- The input impedance was changed to $10-j300 \Omega$
- The gain was significantly degraded but the device didn't start to oscillate.



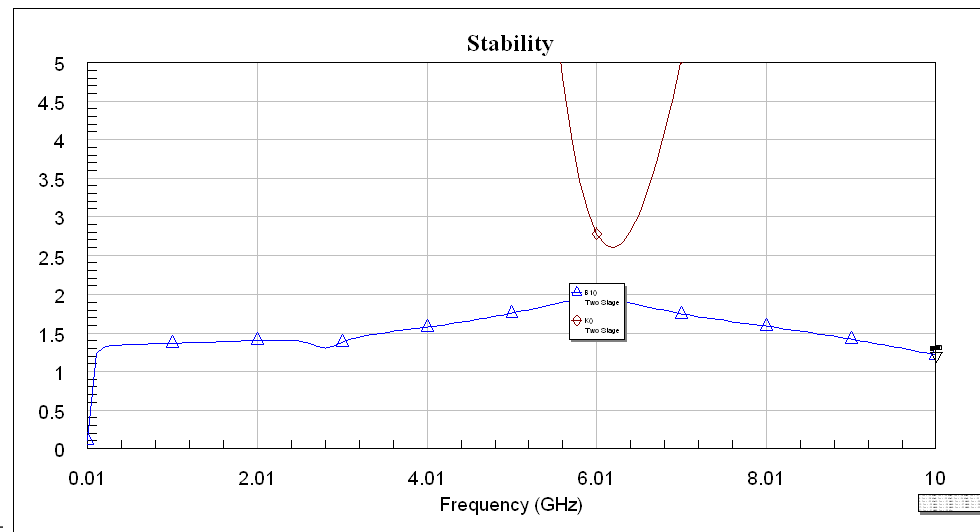
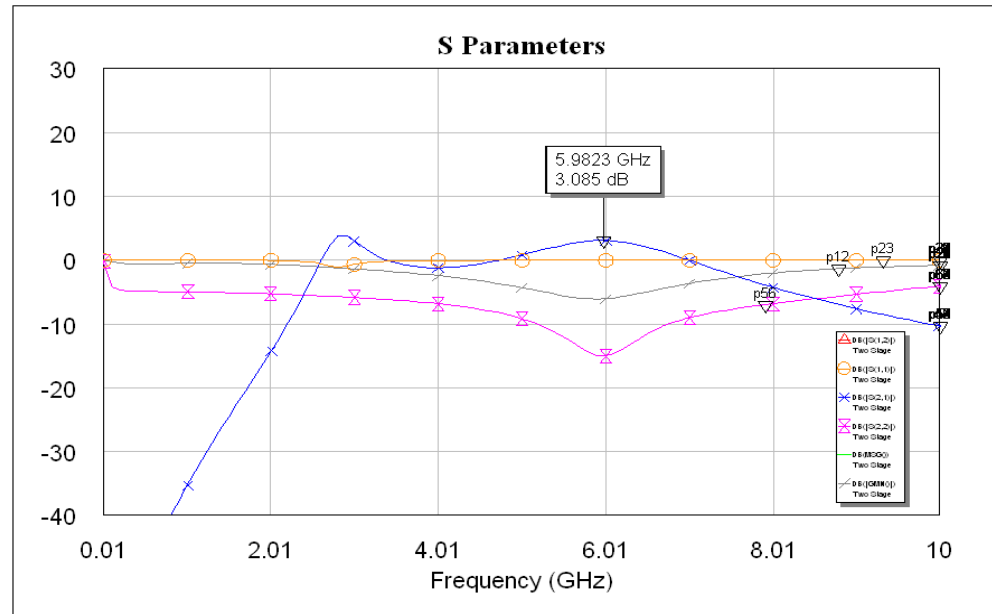
Input Impedance Analysis

Low Resistance High Inductance

The input impedance was changed to $10 + j300\Omega$

The performance is similar to that of the previous example.

The device didn't oscillate.

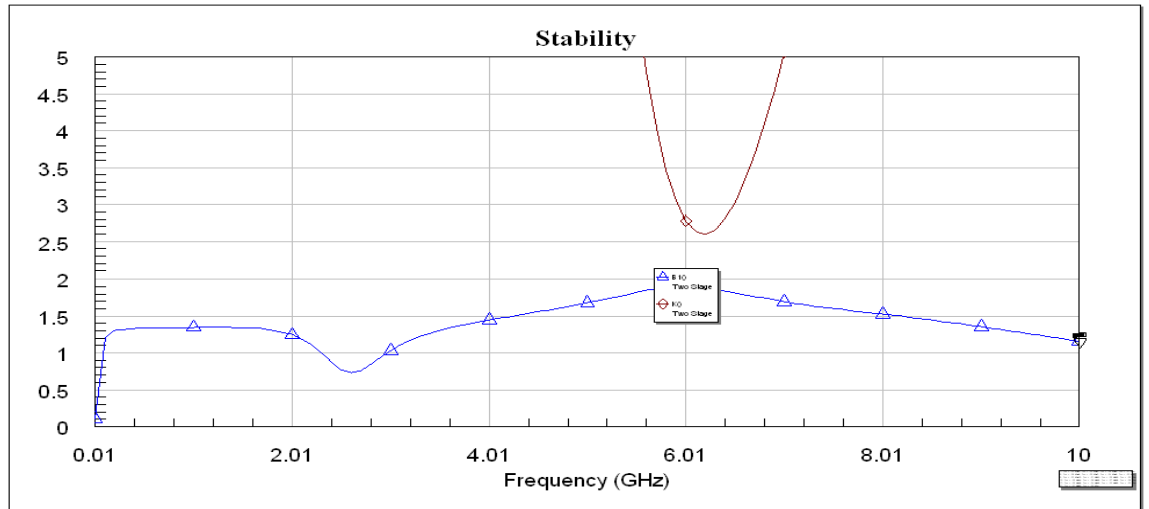
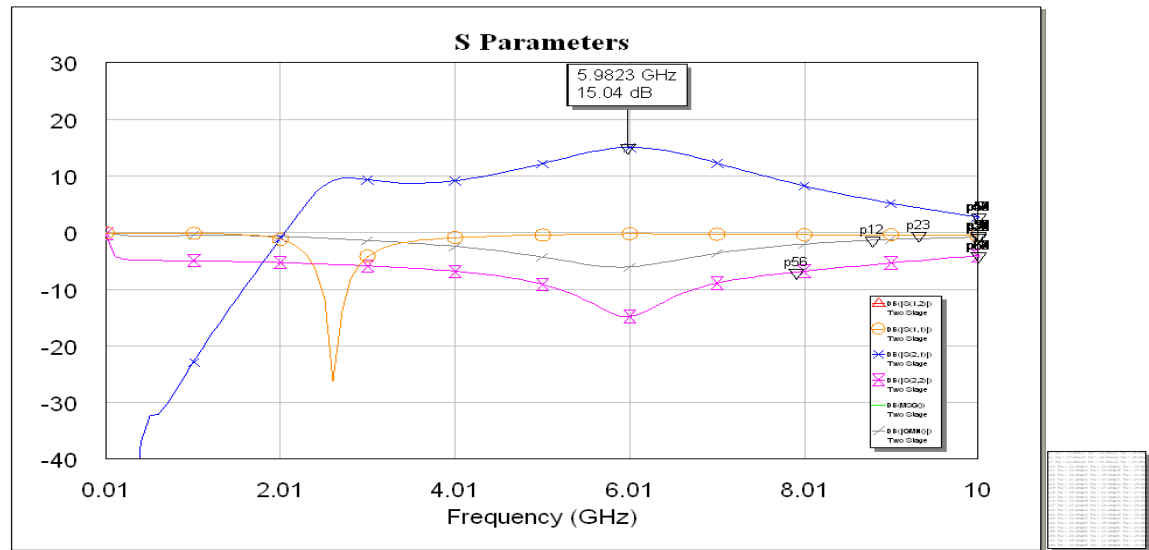


Input Impedance Analysis

Hi Resistance High Inductance

The input impedance was set to $300 + j300 \Omega$

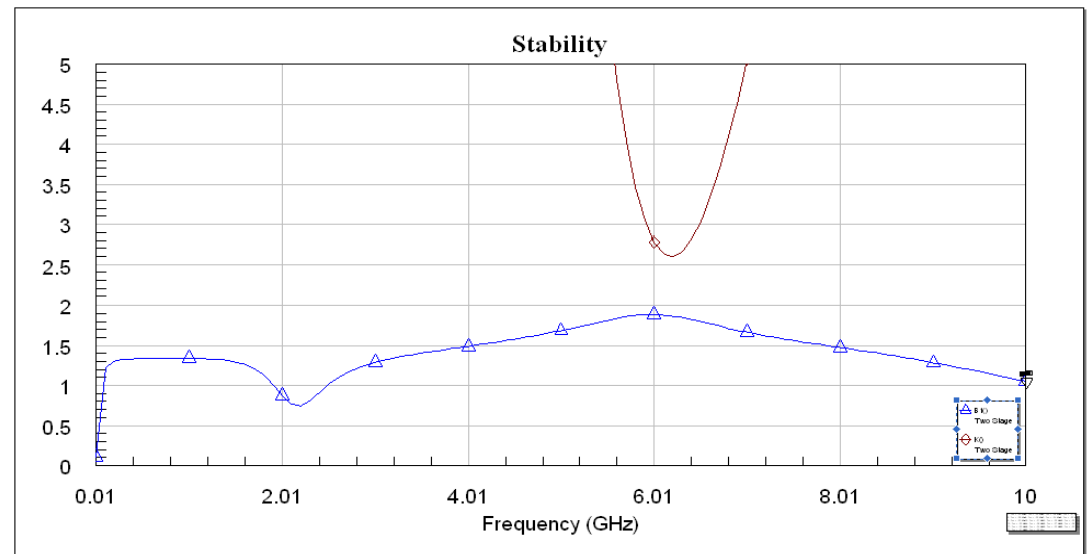
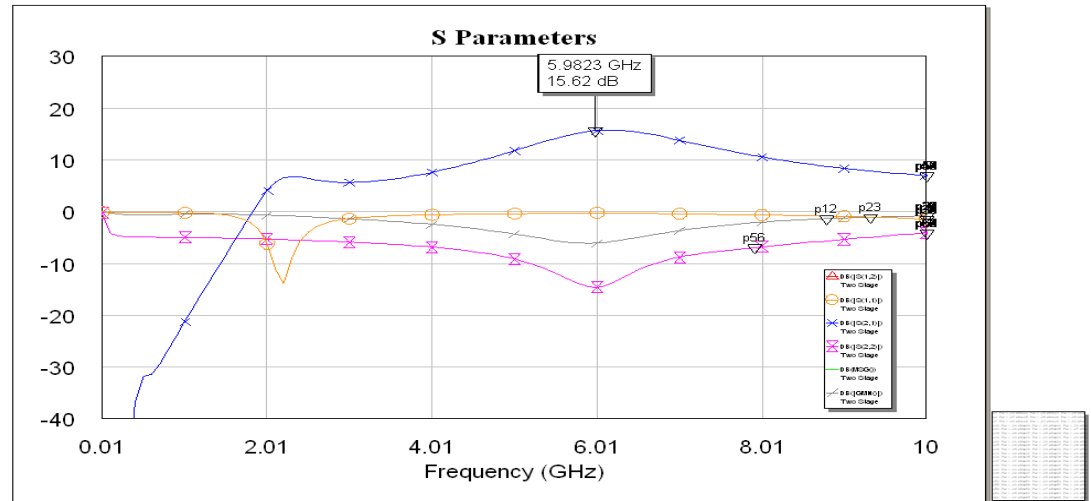
The gain at 5.8 GHz is much better than the previous examples but there is some risk of oscillation around 2.3 GHz.



Input Impedance Analysis

The input impedance was set to $300-j300 \Omega$

This performance is very similar to that of the pervious slide, my assumption is that the real portion has more of an effect then that of the reactive portion.



Design Requirements

Conclusion

Description	Design Requirement	Design Result
Center Frequency	5.8 GHz	5.8 GHz
System Gain	22 dB	24.4 dB
Noise Figure	< 1.5 dB	1.26 dB
Bandwidth (1dB)	± 250 MHz @ F_c	> 800 MHz @ F_c
Passband Ripple	< 1.5 dB in 1dB BW	< 1.5 dB
Supply Voltage	3 V	3 V
Current Consumption	22 mA	< 22 mA

A 100mW Power Amplifier for ISM C-Band Applications

525.787 MMIC Design

James Pociluyko

12/12/10

Abstract

This paper describes a C-Band 100mW amplifier which was designed in fulfillment of the final requirements of the MMIC design course (525.787) at Johns Hopkins University. The amplifier is a two-stage circuit tuned optimally for operation in the 5.725 to 5.875GHz ISM frequency band, and achieves a combined 45% power-added efficiency (simulated performance). The layout is for 100 μ m thick GaAs on a 60 x 60 μ m die and assumes the Triquint Oregon TQPED 0.5 μ m process. Simulations were performed in AWR's Microwave Office using a Triquint library design kit.

Introduction

Envisioned as part of a battery powered communications chipset based in the 5.725-5.875GHz ISM band, the power amplifier (PA) is the final part of the transmit chain. Fed from a modulation source, the PA provides the amplification necessary to transmit the data signal from the transmitter antenna to the receiver. The construction of such a power amplifier is described in the following.

The design tradeoffs in a power amplifier design are well documented in many sources. Sufficient output power and gain are obvious requirements, but the balancing act is in achieving the power with a manageable efficiency. In a communication system PA, the nonlinear response of a highly efficient amplifier design certainly has the potential to cause spectral problems for the receiver. Although the modulator for our chipset is not completely defined, a form of QPSK modulation is specified. This demands a largely linear response, especially if the amplifier needs to contend with the level changes which occur when the phase modulation crosses the origin. On the other hand, the only power source available is a battery, and this highlights the importance of an efficient methodology.

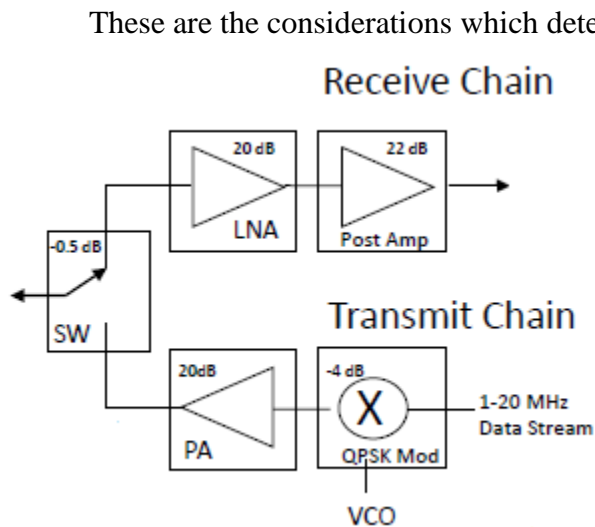


Figure 1: Communications Chipset

Minimum required gain is shown as 20dB and an output power of around 100mW was suggested. Additional goals were established by the designer. These will be discussed next along with the steps used in designing the circuit. Simulation results will be shown which demonstrate the predicted performance including nonlinear effects such as gain compression and harmonics which are possible with modern design simulation

tools. The final performance will then be examined in light of the design goals. Finally a test plan will document the steps necessary to test the fabricated design in a microwave laboratory.

Design Approach

With the frequency band, gain and output power established, the amplifier began to take shape. The required gain and output power required a two-stage design. Furthermore in order to remain mostly linear, while gaining additional efficiency, it was decided to pursue a heavy class AB design as fully class B was considered to be too nonlinear. The bias point would be backed off of class A to a point which hit the required output power while optimizing efficiency, at least for the output stage. It was assumed that the driver would operate close to linear (class A). Its contribution to the overall efficiency would not be as great as the output. The power source was established as a battery and a Li-On source at 3.6V was chosen for the drain voltage. All transistors are depletion mode pHEMTs mainly for the additional current swing (vs. the process' enhancement-mode part) in order to get the required output power. For margin, an extra 1dB was added to the required 100mW output. Some additional performance goals were also established including input return loss, efficiency, and amplitude ripple over the design bandwidth. Also, a goal was set for harmonic performance despite the fact that this was not something that was going to be explicitly controlled in the design except to the extent that the amplifier was operated into compression i.e. harmonic terminations in the output matching were not defined for this design. The goals are seen in Table 1.

Parameter	Requirement/Goal
Operating Band	5.725 to 5.875GHz (ISM)
Minimum Gain	+20dB
Pout (at 0dBm in)	+21dBm
Input Return Loss	-15dB
Power-Added Efficiency (at 0dBm in)	40%
Maximum Amplitude Ripple	0.5dB
Harmonic Levels: 2F, 3F and greater	20dBc or greater

Table 1: Design Goals

Design of the output stage was the first priority since this establishes the output power and largely, the efficiency. Various FET sizes were simulated in a virtual curve tracer in order to select a device that would be able to achieve the required output power. A 6x75 μ m D-mode transistor was ultimately selected to get there without significant compression. In fact the device was oversized slightly to provide some margin as the class A load line predicts 123mW. This was felt to be necessary due to the inevitable resistive losses which will be present in the matching circuit elements as well as the fact that simulated performance tends to overestimate the output power. The curves are shown in Figure 2 for gate drives from -0.5 to +0.5V (0.2V steps).

Output matching was performed using the method described by Steve Cripps. The output S22 of the FET is examined and assumed to be of the form $R+jX$, where X is the reactance of the parasitic drain-source capacitance (Cds). A match is then constructed

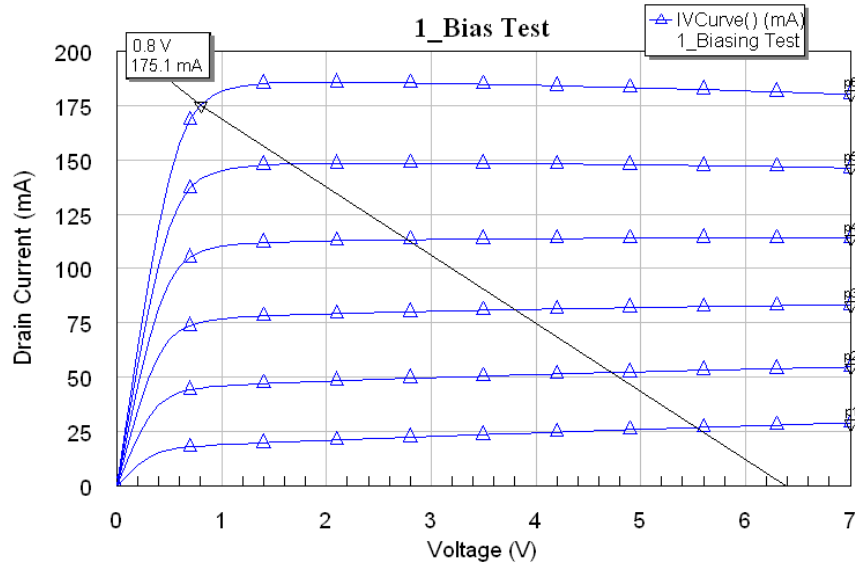


Figure 2: Output FET IV Curves

which appears to the device as the opposite of this parasitic (canceling its effect) plus a real component. This resistive element is the desired operating loadline of the transistor. A loadline for improved efficiency involves reducing the current and would have less slope than the standard class A line depicted in Figure 2. This line has a resistive value of 32Ω , while a line for improved efficiency should have a higher resistance. A circuit was constructed (not shown) consisting of the chosen FET with a pure resistance attached to the drain to test this. The transistor was biased at $IDSS/3$ where $IDSS$ is the drain current when the gate-source voltage is $0V$. It was found that with increasing load resistance (above 32Ω), power output is decreasing and efficiency is increasing. Around 37Ω , efficiency begins to plateau while output power continues to decrease. This would seem to be an ideal load to present to the transistor. These results are shown in Figure 3.

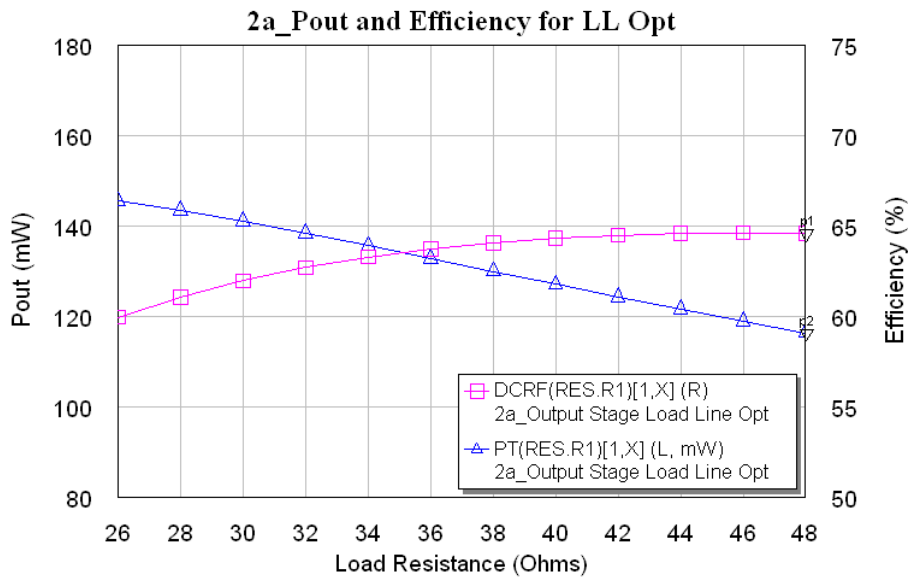


Figure 3: Simulation with Various Resistive Loads

The Cripps impedance was determined as described by first measuring S22 of the unmatched transistor. This impedance was set equal to a parallel RC circuit and values were determined for each. Next the capacitor (in fact, Cds of the FET) was used in a separate RC circuit where the R is the 37Ω found to be desirable in our loadline simulation. An illustration of the circuits is shown in Figure 4. The bias point of the transistor in the simulations had already been established as -0.4V (approx. IDSS/3).

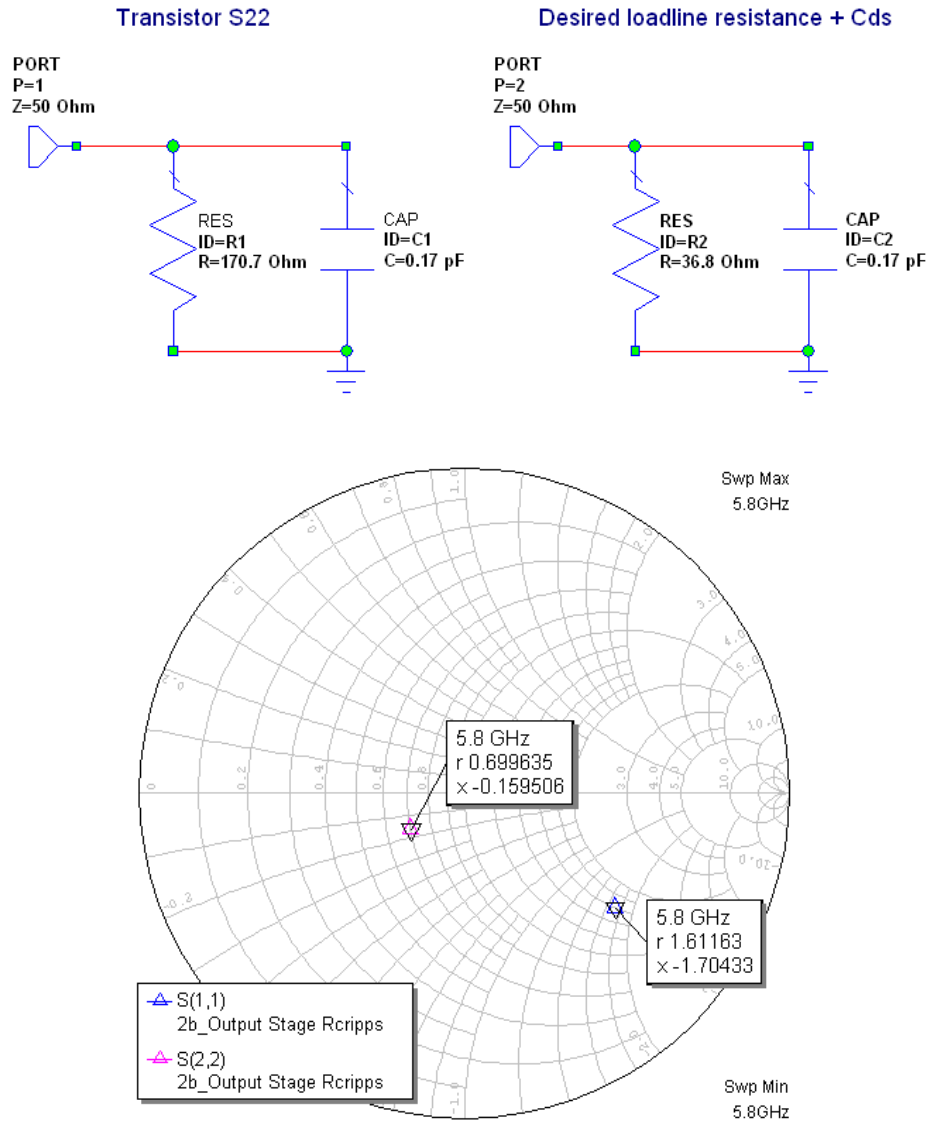


Figure 4: Circuits for determining Cripps impedance and associated plot. (Impedances Normalized)

Having determined the Cripps impedance, output and input matching networks were constructed. The output was matched to $0.70 + j0.16 \Omega$ in order to cancel Cds. A

network consisting of a series 2pF capacitor and shunt 2.3nH inductor creates the desired match. With this connected to the transistor and some series input resistance to stabilize the FET in our design frequencies, the input match was designed to conjugately match to S11. Here, a 0.8nH shunt inductor and series 5pF capacitor suffice.

Although these values have been presented as a logical progression of calculations, these are actually refined values and the result of an iterative process. For example the bias point of the transistor, the matching networks, and even the desired load resistance for the FET were different in the initial simulations. Although the steps presented will provide a reasonable first cut at the circuit, tradeoffs are necessary for optimization and fortunately this is possible with modern simulation software. Component values and even bias point effects can be tuned to achieve a desired result. The process here worked as follows. The output matching network and bias point of the transistor were simultaneously varied to optimize efficiency while still reaching the required output power. Gain was also considered at the lowered bias point since, despite the increase in efficiency, this meant reduced gain and could have placed an unrealizable requirement on the driver stage. When this was complete, the input was matched. Finally, stability was considered over a wide bandwidth and required several adjustments since the reduced bias voltage made the device more unstable out of band. It was found that some shunt resistance in combination with a lowered series resistance from my initial simulation provided stability. This naturally caused a loop for it was then necessary to make sure that these changes did not ruin the output power and efficiency. Further, these changes to resistors on the device input alter the input match which then had to be retuned. Several cycles were required in order to find an acceptable balance among all of these elements. Figure 5 depicts the final output stage schematic.

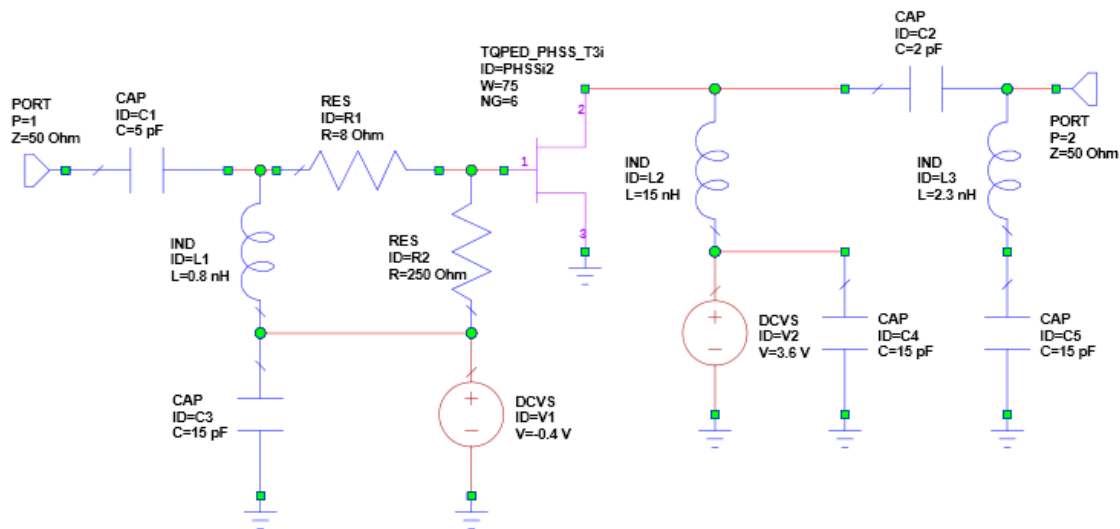


Figure 5: Output Stage Schematic

Design of the driver stage commenced after knowing what kind of performance could be obtained from the output. Figure 6 depicts the power, gain and efficiency of the output stage simulated at the center of the frequency band over a range of input power levels. It should be noted that this simulation is based on Triquint library elements which include losses and other parasitics which are not depicted in Figure 5. Around the 3dB gain compression point, approximately 12dBm input, output power is over 100mW and the efficiency is nearly peaked. The driver was intended to be more linear than the output with regard to bias point and goals of 12dB gain with about 12dBm output at or before compression were established.

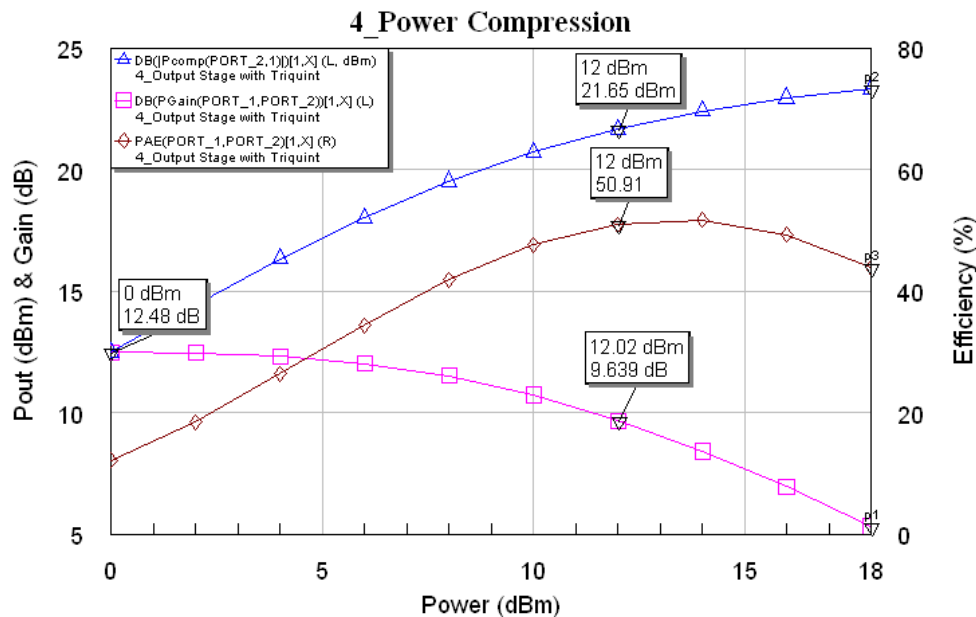


Figure 6: Simulated output stage performance at 5.8GHz

The driver stage was conceived and matched using methods similar to those used for the output stage. The first consideration was the sizing of the FET. The lower power output required from the device is directly related to the FET periphery. Scaling this device down will help to control efficiency by only using the biggest transistor necessary, while preventing the input from overdriving the output stage. A smaller 6x40μm FET appeared to be ideal in simulations, which is about a 2:1 (output to driver) ratio of periphery. Getting the power required to drive the output stage was not an issue here so the output tuning was performed with the aim of peaking efficiency and output power around the +12dBm mentioned previously. It was found, fortuitously, that the bias point of the driver could be set to the same level as the output stage while maximizing the efficiency. This simplifies the layout since it avoids either having more than one input pad for gate bias or a more complicated resistive network to generate separate bias voltages for the two stages. The driver circuit schematic may be seen in Figure 7. A drain-gate feedback resistor helps to limit the gain of this stage to avoid overdriving the output. It also stabilizes the circuit along with a small series input resistance.

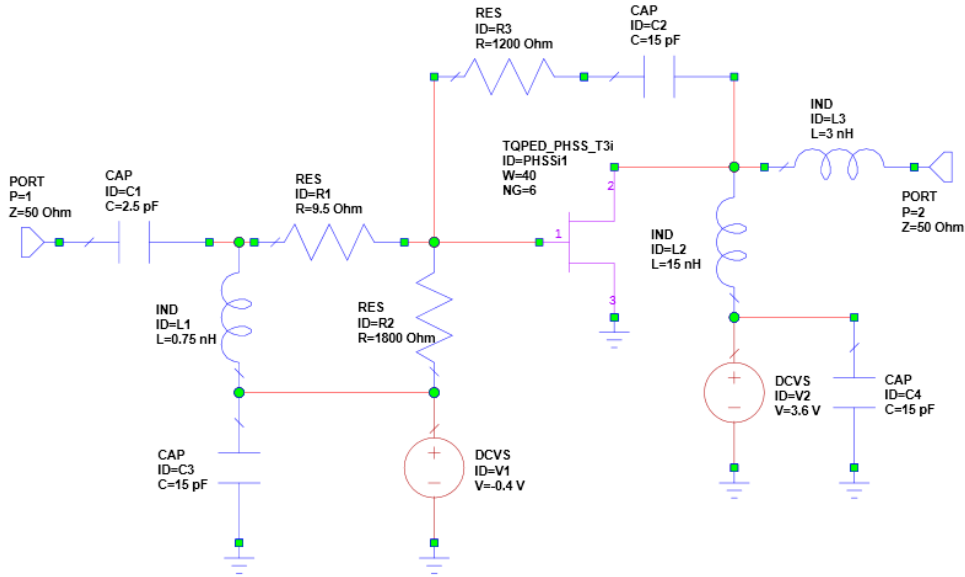


Figure 7: Driver Stage Schematic

The Final Amplifier - Performance

The two stages shown were connected together in order to form the final circuit. Simulation was used to verify the performance of the amplifier and of the earlier design goals. The software employed for this was Microwave Office from AWR Corporation (Ver. 9.04r) with a Triquint-supplied foundry element library (Triquint Oregon TQPED ver. 1.1.21.16). All FETs were simulated using the TOM3 model. The estimated performance is shown in the following graphs.

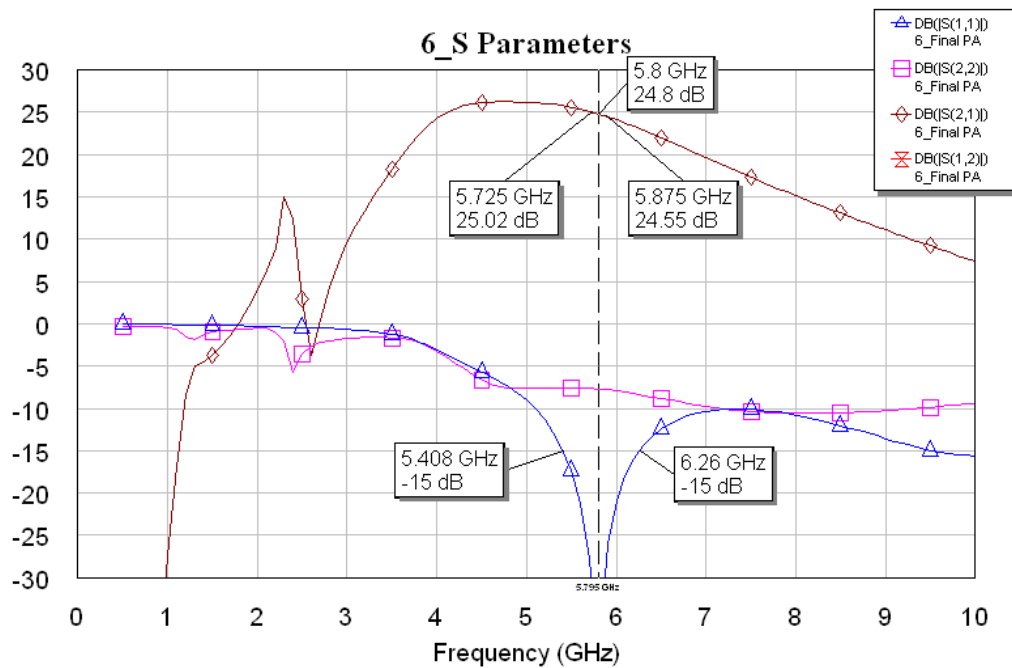


Figure 8: Final Amplifier S-Parameters

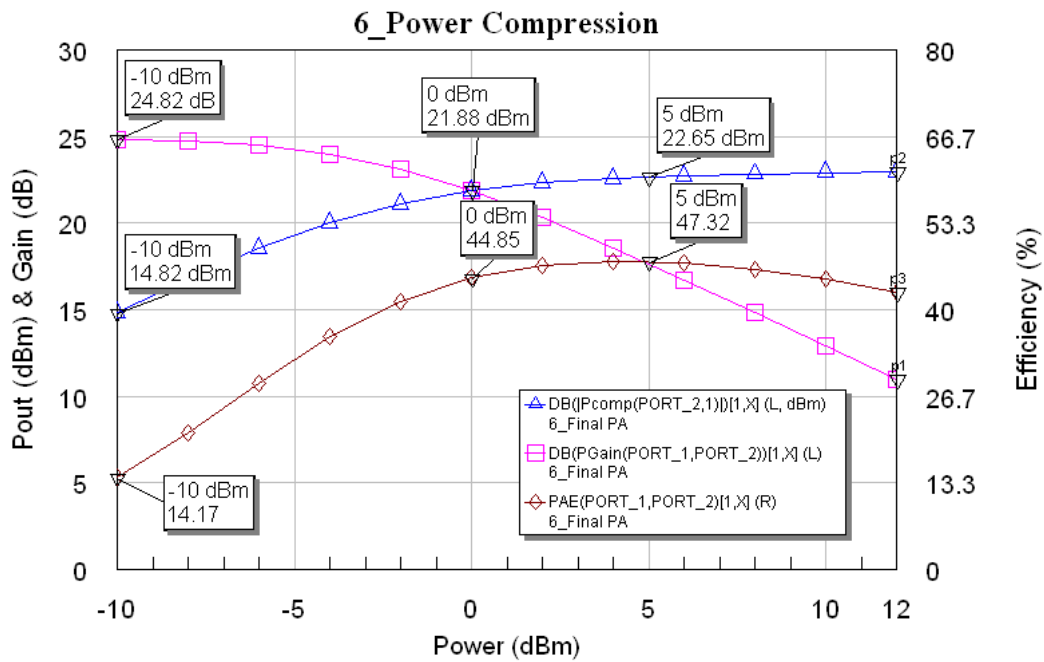


Figure 9: Final Amplifier Power Sweep at 5.8GHz

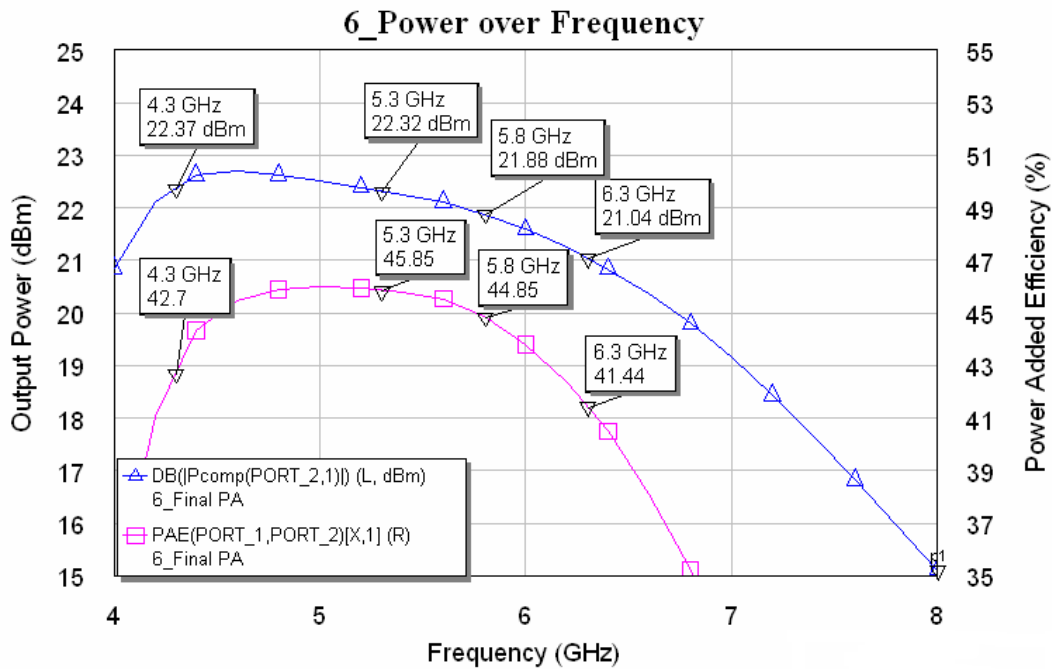


Figure 10: Final Amplifier Frequency Sweep at 0dBm Input

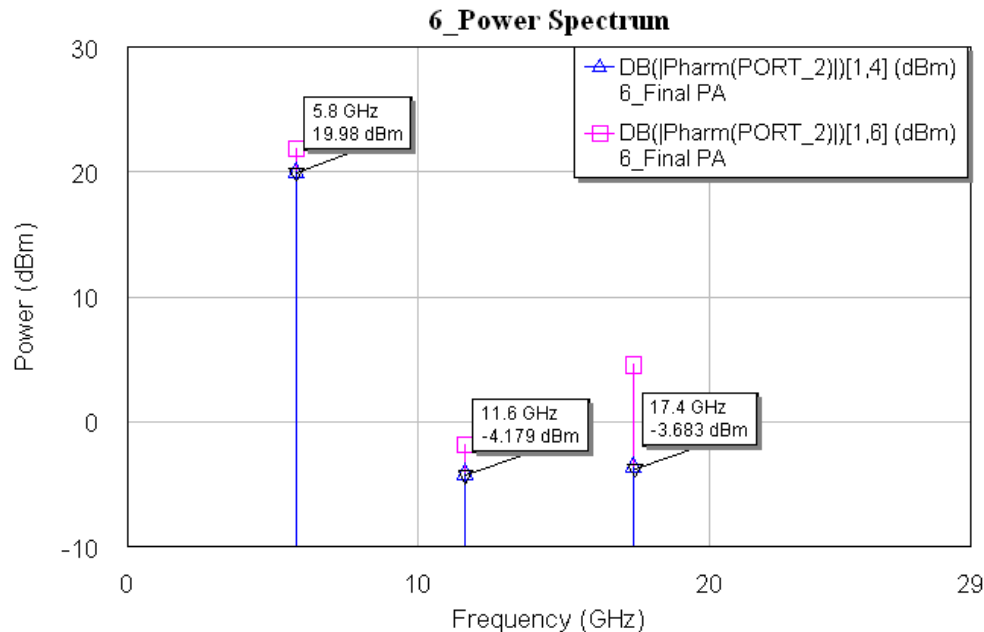


Figure 11: Power Spectrum at -4 (Blue) and 0 dBm (Magenta)

A review of the simulation results presented in Figures 8 through 11 show that the amplifier is meeting its stated goals. Small-signal S-parameters in Figure 8 demonstrate gain in excess of 20dB. Input S11 is well matched and below -15 dB in the ISM band. The -15dB points are shown on the plot, although the bandwidth is better than anticipated. It appears a semi-respectable match can be achieved from roughly 5 to 7 GHz. Gain is certainly available over this wider range as well.

The other figures demonstrate modeled nonlinear performance as the amplifier is driven into compression. The power results of Figure 9 show that at 0dBm input, the amplifier outputs almost 22dBm, providing plenty of margin. As designed, the amplifier is operating into 3dB compression here for better efficiency. That has also met the design goal, with predicted power-added efficiency of around 45%. The gain behavior is the result of the output stage since, by design, the driver is still linear here. The 1dB compression point occurs at roughly +20dBm which corresponds to about -4dBm input. These results (at 5.8GHz) are applicable to our ISM design band, especially since the amp demonstrates very usable performance over a wider frequency band (Figure 10). At our rated input power of 0dBm, the amplifier is capable of 100mW output (with margin) over a 2GHz bandwidth from 4.3 to 6.3GHz, while meeting stated goals of gain and efficiency. The power spectrum plot in Figure 11 shows the relative power of the fundamental (again simulated at 5.8GHz) and its harmonics at the edge of linear performance (-4dBm input) and at 0dBm. While still linear, harmonics are better than -23dBc. However, as we push further into compression, harmonic levels rise as expected. A review of the final overall performance vs. stated goals may be viewed in Table 2. Most parameters have two lines indicating performance in the design band and

then over a wider bandwidth of 5.0 to 6.3GHz. The bounds on this range were return loss and power at the low and high ends respectively. However, it is clear that the design has usable output power from 4.0 to 7.0GHz, depending on system requirements. This is a surprisingly good result. A view of the final circuit in schematic form showing the bias point is available as Figure 12. Although the layout has not been discussed, it should be noted that this circuit includes the simulation of the routing traces connecting the circuit elements.

Parameter	Requirement/Goal	Simulated
Operating Band	5.725 to 5.875GHz (ISM)	5 to 6.3 GHz
Minimum Gain	+20dB	+21dB minimum +24.5dB (ISM band)
Pout (at 0dBm in)	+21dBm	+21dBm minimum +22dBm (ISM band)
Input Return Loss	-15dB	-10dB <-20dB (ISM band)
Power-Added Efficiency (at 0dBm in)	40%	41% minimum 45% (ISM band)
Maximum Amplitude Ripple	0.5dB	3dB 0.5dB (ISM band)
Harmonic Levels: 2F, 3F and greater	20dBc or greater	23dBc at -4dBm input (ISM band)

Table 2: Stated Goals vs. Final Simulated Performance

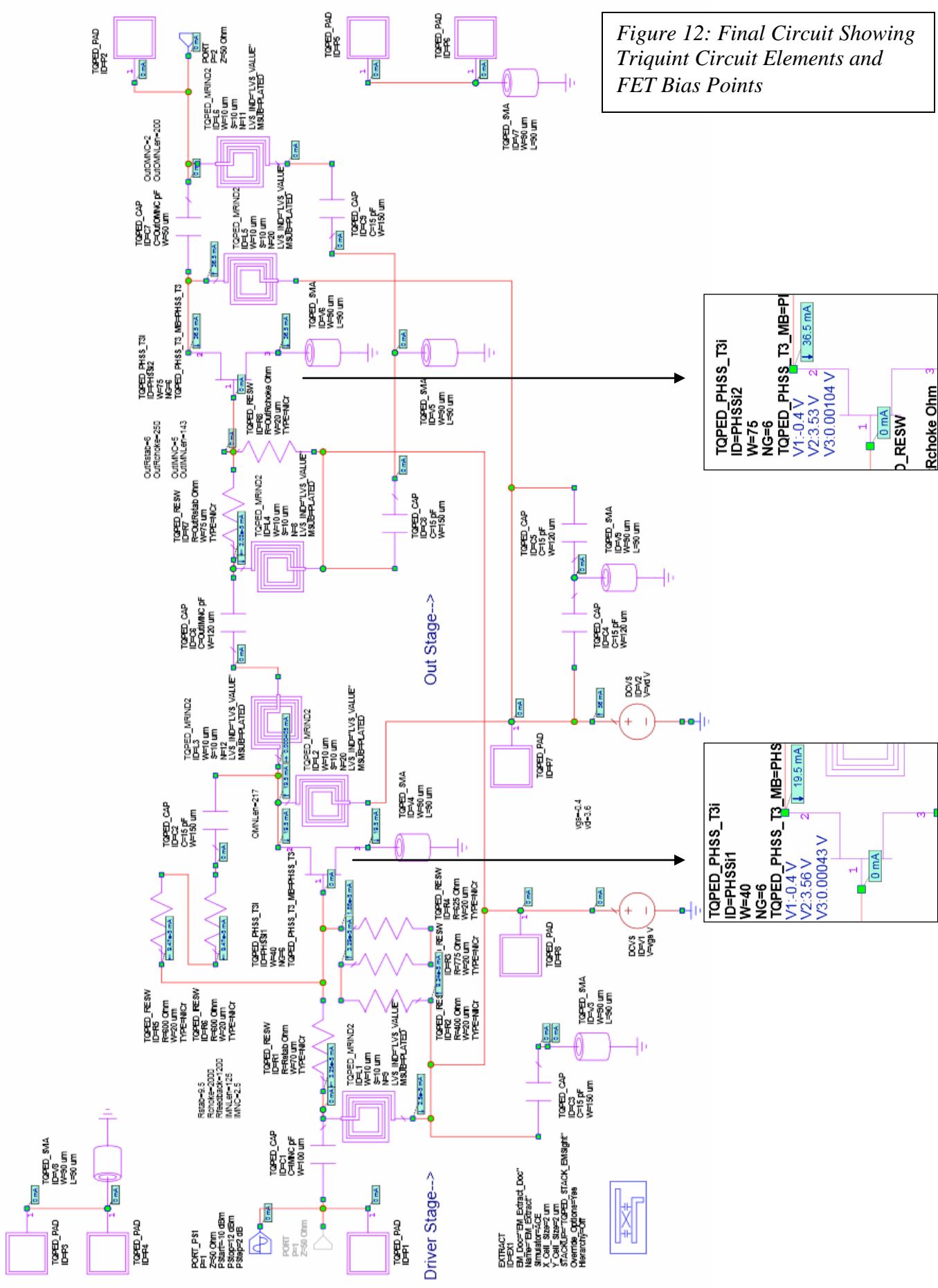
A final aspect to consider is the robustness of the amplifier. Stability was checked on the sub-circuits as well as the final amplifier. The metric used was μ , the geometric stability factor. All circuits were designed to be unconditionally stable up to 10GHz indicated by μ greater than or equal to 1. An indication of this is provided in Figure 13. Additionally, process tolerances were considered by varying a tolerance on all of the passives in the circuit to make sure that the performance did not change dramatically and that the stability conditions remained. Capacitors were varied by 10% and resistors by 5% since these are dependent on material properties and dimensions. Inductors, which are governed more by their length were only varied by 3%. No detrimental effects were observed.

The Final Amplifier – Layout

Layout of the amplifier was accomplished on a 60 x 60 μ m size die. The general idea behind the layout was to proceed with input and output going from left to right across the chip. DC voltages would be brought in from the other sides. As much as possible, each stage was to be grouped together to minimize isolation. Figure 14 shows the final circuit layout.

DC voltages enter with the drain at the top (+3.6V) and the bias (-0.4V) at the bottom. The two RF chokes take up the upper left and right corners. They do not share a common decoupling cap but are each independent for better isolation. A similar

Figure 12: Final Circuit Showing Triquint Circuit Elements and FET Bias Points



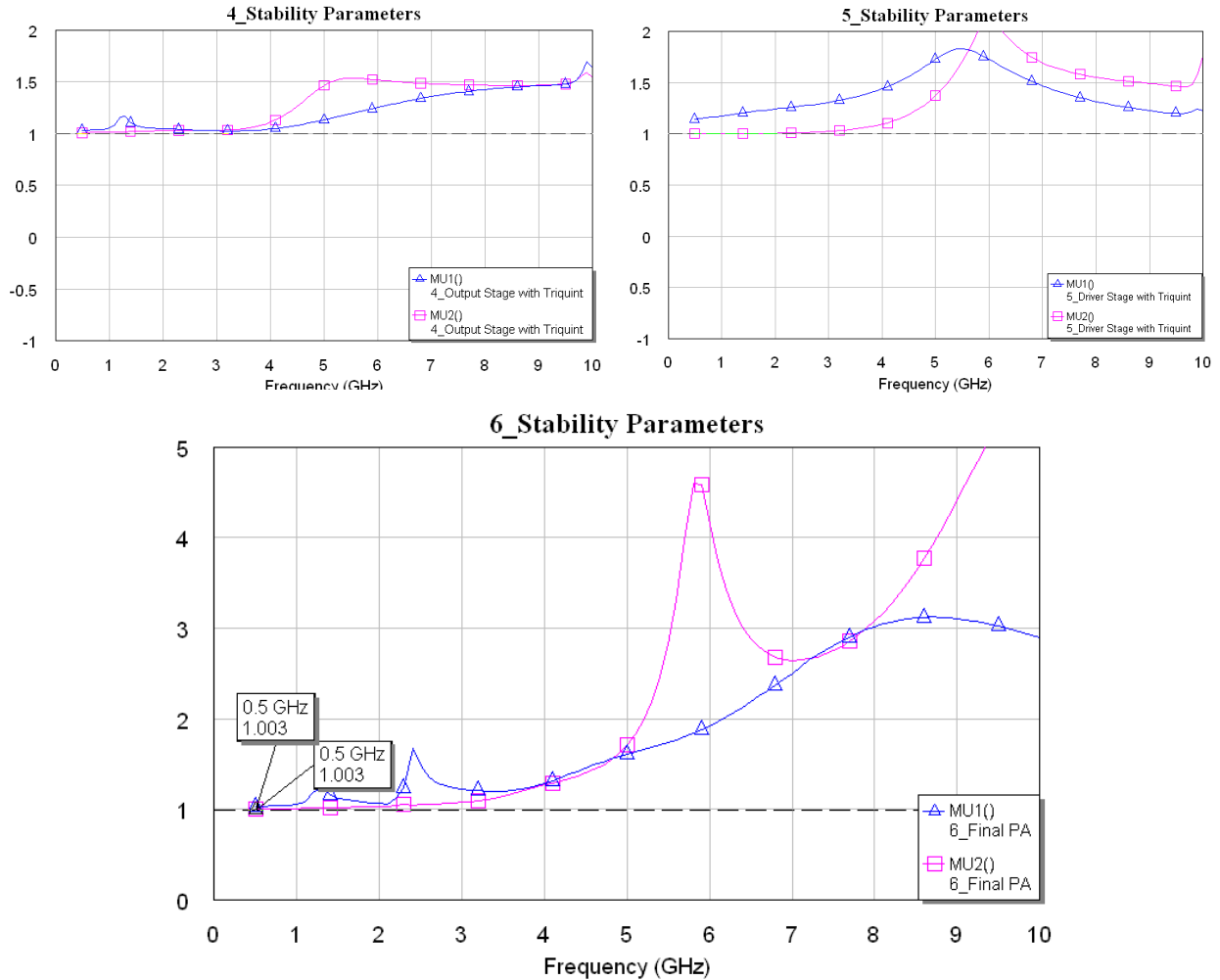


Figure 13: Stability plots – Output Stage, Driver Stage and Final Amp (Starting Clockwise from Top Left)

arrangement was done for the bias. The high value bias choke and feedback resistors for the driver stage were initially a problem but these were split into smaller segments which could be positioned among the RF elements. The driver stage is largely packed into the left half of the chip with the output on the opposite. Ground pads are provided on either side of the RF input and output pads for a probed ground-signal-ground arrangement. All routing was performed in plated metal (metal layers 1 and 2) to minimize loss. The only exceptions are at the input and output RF pads where crossover was deemed necessary and here metal 1 carries the signal while a wide metal 2 ensures a good ground connection to the via.

The layout was a success in the sense that it fit without great changes to the circuit. The main components that were modified were the driver input and output stage output inductors. These were resized to fit better. Another change was that the driver bias choke was changed from its initial value of 2k Ω to 1.8k Ω in order to fit without any

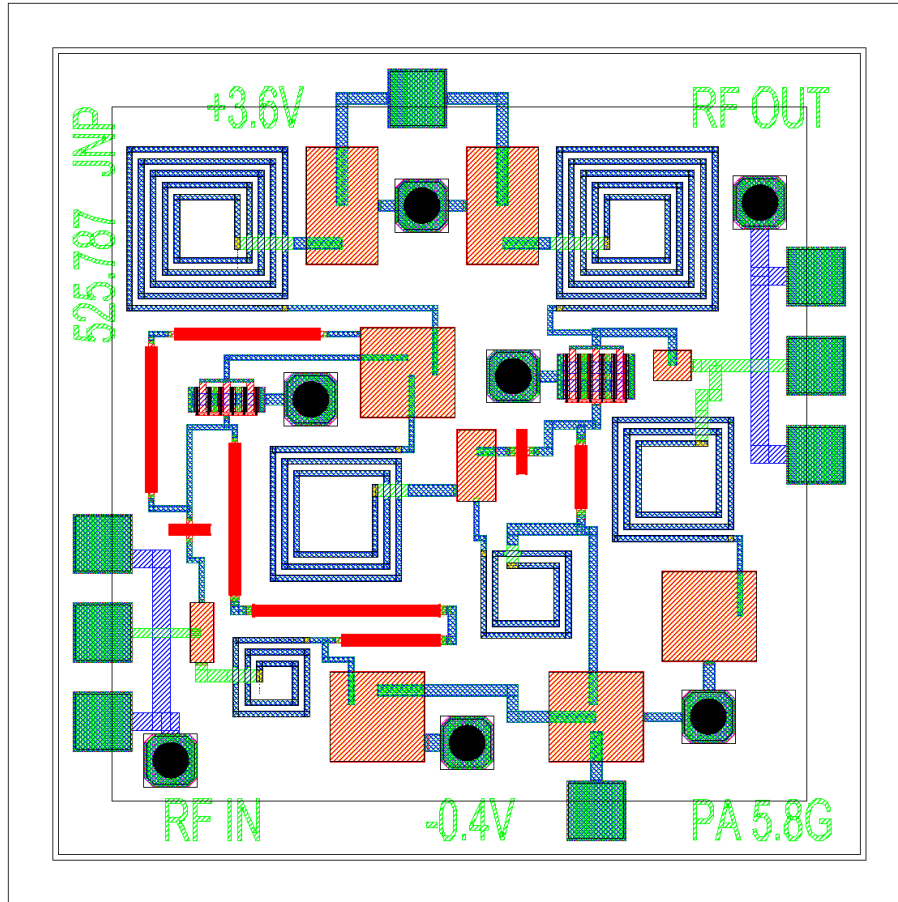


Figure 14: Final Layout

ill effects on gain. All circuit traces were extracted in the ACE EM simulator within Microwave Office. Little change was observed from the original (without circuit traces) other than some frequency shift on the input. This was retuned to continue to provide a good input match.

Test Plan

After fabrication the MMIC will be tested on a microwave probe station. The design parameters will be verified to see how accurately performance was predicted by the simulator. General test equipment and specific tests are identified below.

S-Parameters

Required Equipment: Network Analyzer (HP 8510 or equivalent)
(2x) Power Supplies (0-5V, 1A range)

Procedure:

1. Verify drive level and maximum port power of analyzer to avoid overdrive.
2. Calibrate analyzer for 2-port measurement from 0.5 to 10GHz.
3. Connect analyzer port 1 to MMIC RF In probe and port 2 to RF OUT probe.

4. Apply bias voltage of -0.4V. This must be applied before the drain voltage to avoid burning out the FETs.
5. Apply drain voltage of 3.6V.
6. Measure and record full S-parameters.
7. Measure and record drain and bias currents.

Power Sweep

Required Equipment: Power Meter (HP 438A or equivalent)
Signal Generator (HP 83623B or equivalent)
(2x) Power Supplies (0-5V, 1A range)

Procedure:

1. Calibrate power meter.
2. Connect signal generator output to MMIC RF IN probe.
3. Connect power meter sensor to MMIC RF OUT probe.
4. Apply bias voltage of -0.4V. This must be applied before the drain voltage to avoid burning out the FETs.
5. Apply drain voltage of 3.6V.
6. Set signal generator for 5.8GHz (ISM band center frequency).
7. Set power for -10dBm and apply RF. Record the measured output power and drain current.
8. Repeat for input levels of -4dBm, -2dBm, 0dBm, +2dBm, +4dBm, +6dBm, +8dBm and +10dBm.

Frequency Sweep

Required Equipment: Power Meter (HP 438A or equivalent)
Signal Generator (HP 83623B or equivalent)
(2x) Power Supplies (0-5V, 1A range)

Procedure:

1. Calibrate power meter.
2. Connect signal generator output to MMIC RF IN probe.
3. Connect power meter sensor to MMIC RF OUT probe.
4. Apply bias voltage of -0.4V. This must be applied before the drain voltage to avoid burning out the FETs.
5. Apply drain voltage of 3.6V.
6. Set signal generator for 0dBm output.
7. Set frequency to 4.000GHz and apply RF. Record the measured output power and drain current.
8. Repeat for the following frequencies: 4.250, 4.500, 4.750, 5.000, 5.250, 5.500, 5.725, 5.800, 5.875, 6.000, 6.250, 6.500, 6.750 and 7.00GHz.

Spectrum

Required Equipment: Spectrum Analyzer (HP 8563 or equivalent with 20GHz range)
Signal Generator (HP 83623B or equivalent)
(2x) Power Supplies (0-5V, 1A range)

Procedure:

1. Connect signal generator output to MMIC RF IN probe.

2. Verify maximum input power to spectrum analyzer to avoid overdrive.
3. Connect MMIC RF OUT probe to spectrum analyzer with intermediate attenuator if necessary.
4. Apply bias voltage of -0.4V. This must be applied before the drain voltage to avoid burning out the FETs.
5. Apply drain voltage of 3.6V.
6. Perform broad sweep up to 20GHz to look for oscillations or other anomalies.
7. Clear display and set signal generator to 5.800GHz.
8. Set signal generator power level to -10dBm and apply RF.
9. Record output power of fundamental and relative levels of 2nd, 3rd and 4th harmonic.
10. Repeat for the following power levels: -4dBm, 0dBm, +4dBm

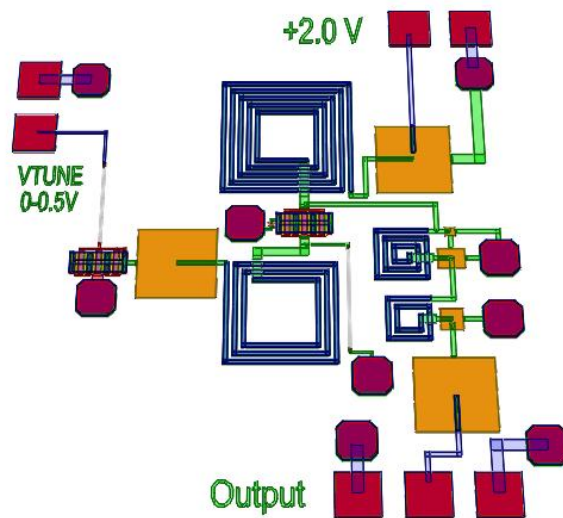
Conclusion

A C-Band power amplifier has been presented capable of 100mW output and >40% power-added efficiency over the 5.725 to 5.875GHz ISM band. The design approach, simulation and layout were detailed and a comparison of the simulated performance to initial goals revealed that the design was successful. In fact, it was a pleasant surprise that similar power and efficiency was found to be available over a wider bandwidth of approximately 4 to 7GHz. Performance will be verified with hardware after MMIC fabrication using the included test plan. However, after witnessing the refinement of the simulation tools and models presented in the MMIC Design class, it is expected that the fabricated chip will also measure well.

References

- Cripps, Steve. *RF Power Amplifiers for Wireless Communications*. Boston: Artech House, 1999.
- Moore, Craig and Penn, John. *MMIC Design Course Handouts*. Johns Hopkins University. 2010.

C-Band Voltage Controlled Oscillator



Ben Woodworth

MMIC Design

525.787

Dec 13, 2010

Abstract

A monolithic microwave integrated circuit (MMIC) C-band voltage controlled oscillator (VCO) is presented in this paper. The MMIC VCO is designed with depletion mode pHEMT devices and the design fits on a 60 mil x 60 mil GaAs chip operating on a +2V power supply. The final design oscillates from 5.4 to 6 GHz over a 0-0.6V tuning range with an approximate output power of +8 dBm. The design process used for this design is the TriQuint TQPED 150mm, 0.5um pHEMT process. Simulations for this design were carried out in Microwave Office and the design is to be fabricated by TriQuint Semiconductor Inc.

Introduction

The VCO was designed as part of the C-band transceiver depicted in the system block diagram shown in Figure 1 below. The designed VCO is to be used as a tunable LO signal for the receive chain I/Q Demodulator. The design of this VCO was tailored for low-voltage operation that could be powered off of a battery. This report details the design, simulation, and layout for the VCO design.

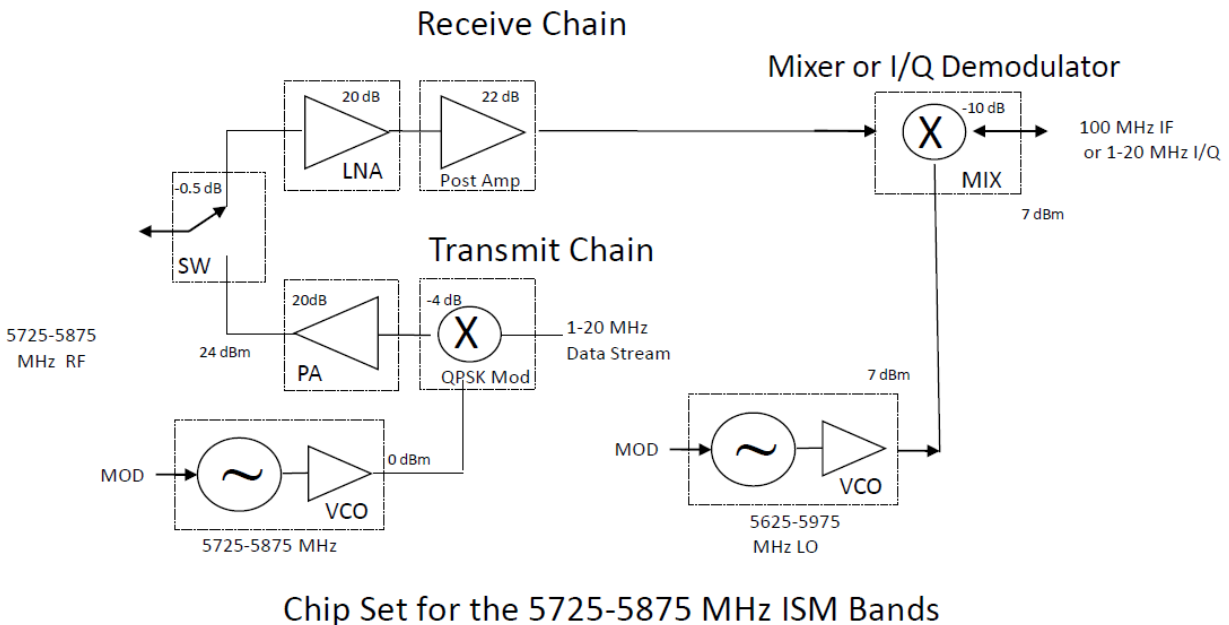


Figure 1: System Block Diagram

Design Approach

There are several different approaches for designing a VCO. The approach chosen for this design was the negative impedance approach. The circuit for this approach consists of two basic parts, an active network and a load network as seen in Figure 2 below. For this circuit the total loop voltage across the networks must equal zero according to Kirchoff's Law. If this is the case, then it can be shown that $Z_L = -Z_D$, and more specifically that $R_L = -R_D$ and $X_L = -X_D$.

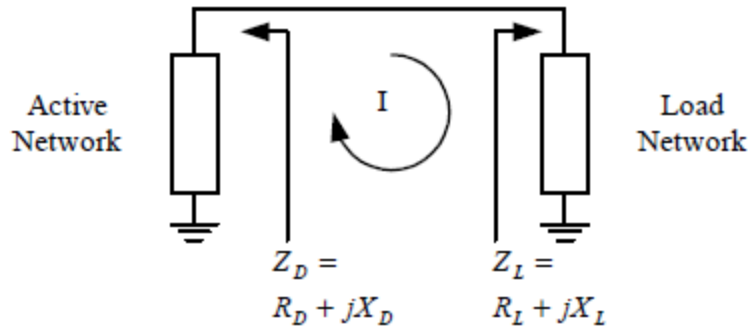


Figure 2: Basic VCO Circuit

The negative resistance, R_D , is obtained by destabilizing active device with an appropriate resonance circuit. The reactive part of the impedance is most conveniently designed such that $X_D = X_L = 0$. In order for the circuit to truly oscillate, the circuit must be adequately destabilized and this is set by the relationship between R_D and R_L . A general rule of thumb to achieve oscillation is the start-up condition for a series resonance oscillator of $|R_D| > 3R_L$ and $X_L = -X_D$. Once oscillation begins the signal will continue to grow as long as the start-up conditions are met. These are the general start-up conditions that were used in the design of the VCO presented in this paper.

Design Specifications

Table 1 below shows the general specifications that the VCO was designed towards.

Frequency Range	5600 MHz to 6000 MHz
Supply Voltage	Battery Powered <3.6V
Tuning Voltage	0 to 1V
Output Power	+7dBm

Table 1: Design Specifications

Simulations

The following sections discuss in detail the design approach taken to design a VCO to meet the above specifications. The design of the VCO is broken down into six major steps: Active device characteristics, Varactor design, Destabilization, Gate Tuning, Drain Tuning, and Output matching circuit.

Device Characteristics

The device chose for this design was a TriQuint Depletion Mode pHEMT. The size of the device chosen was the standard 300 um device that has a $W = 50$ um and $N = 6$. Because the VCO needs to operate with a voltage below 3.6V, the I-V curve is examined to choose a suitable bias point for the circuit. The I-V curve for this device can be seen below.

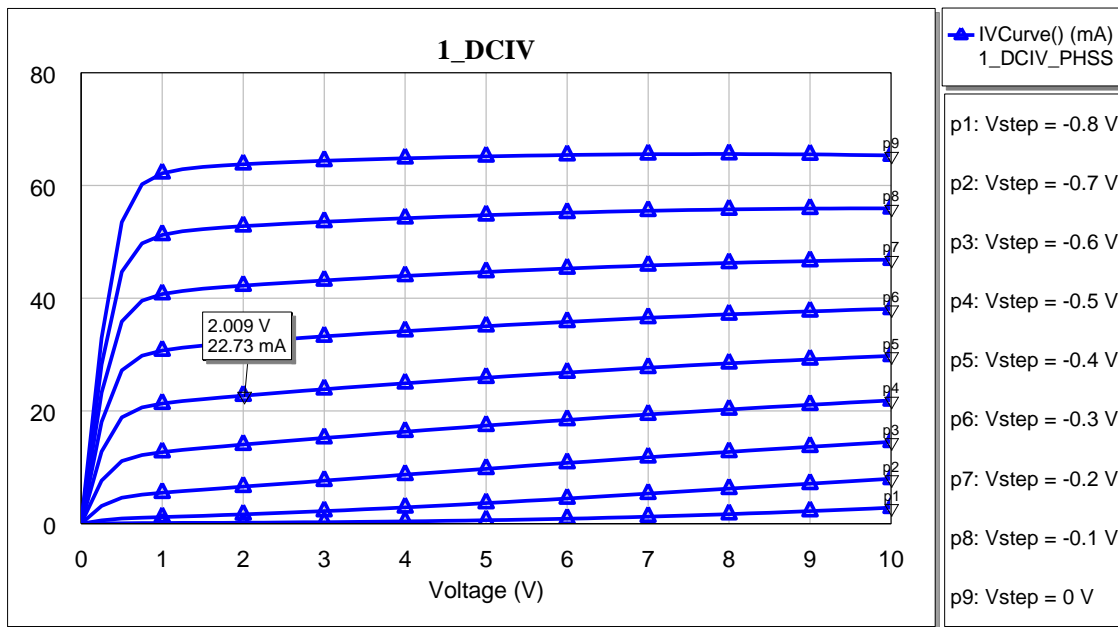


Figure 3: D-Mode, 300um pHEMT DCIV Curve

From the DCIV curve it can be seen that the device can be biased with a drain voltage of +2V with a current draw of about 22mA. This bias meets the design specification for battery operation and it consumes a relatively low amount of power at 44mW.

Varactor Design

A varactor is used in this design to tune the frequency of operation of the VCO. To create a varactor, a reverse biased D-Mode pHEMT was used. To do this, the drain and the source of the pHEMT were tied together and the gate was grounded. Voltage was then applied to the drain through a 2 kΩ resistor.

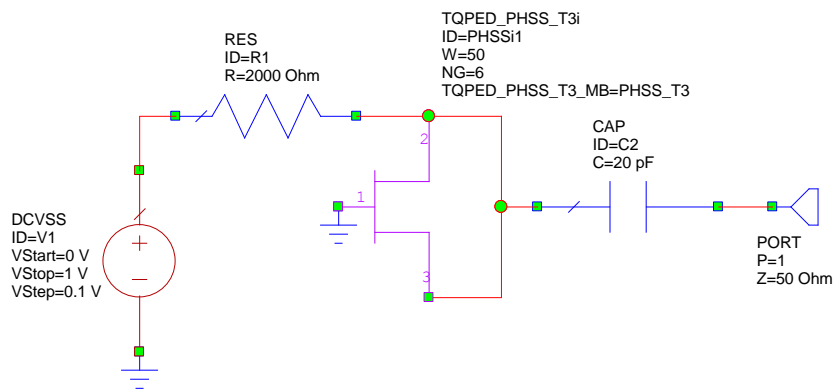


Figure 4: Varactor Circuit

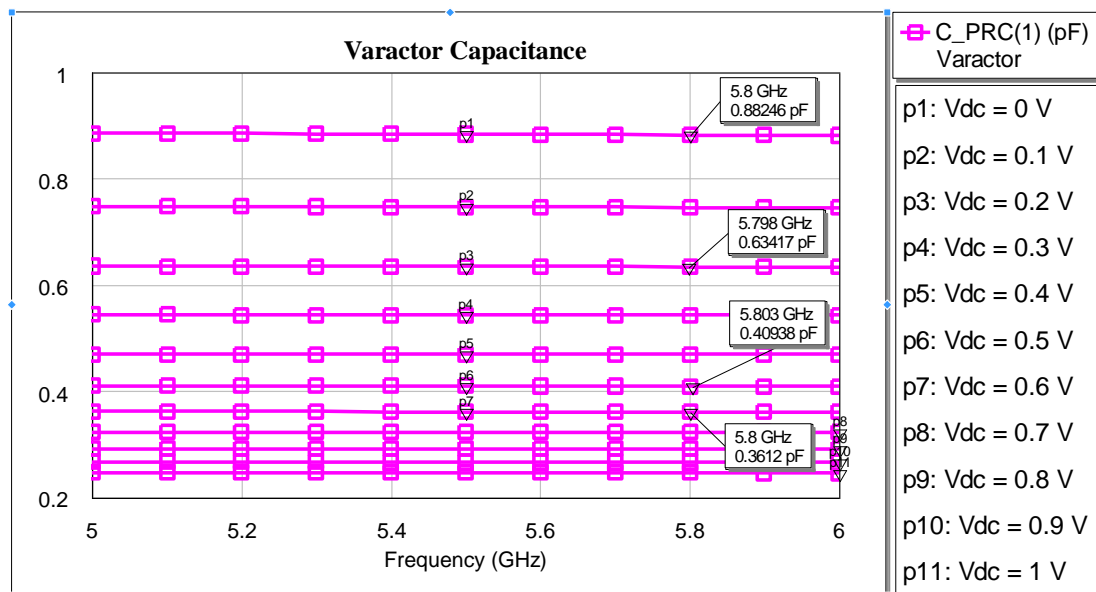


Figure 5: Varactor Capacitance

By varying the voltage between 0 and 1V, the capacitance of the circuit changes and can be seen in Figure 5 above. Looking at the plot it can be seen that the capacitance varies between about 0.9pF and 0.25pF. For this project it was chosen to limit the tuning range to 0 to 0.6V since this range provided the biggest capacitance impact to the circuit and those voltages above 0.6V minimally changed the capacitance.

Destabilized Device

Destabilizing the active device is the key to achieving oscillation. As mentioned above in the design approach, it is desired to have the active circuit resistance be 3 times greater than the load resistance: $|R_D| > 3R_L$ in order to achieve oscillation. To destabilize the pHEMT, a small series resistor to ground was placed at the source port of the device. This provides a feedback path from the drain current to the gate voltage which increases the S12 of the circuit to be greater than 1 and in turn creates a negative resistance circuit.

To simulate the instability of the circuit the SMAP function was used to plot the distance from the center of the smith chart to the farthest away point on the output mapping circle. This is the same as plotting the inverse of the load stability factor. The load stability factor, MU1, was also plotted to determine the level of instability of the circuit.

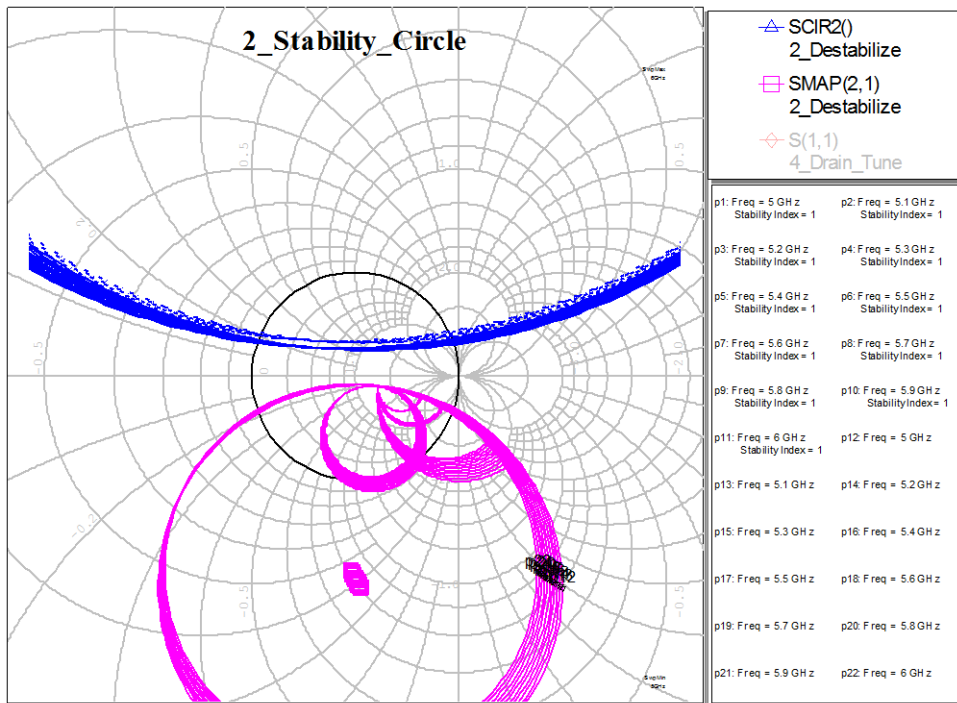


Figure 6: SMAP Circles

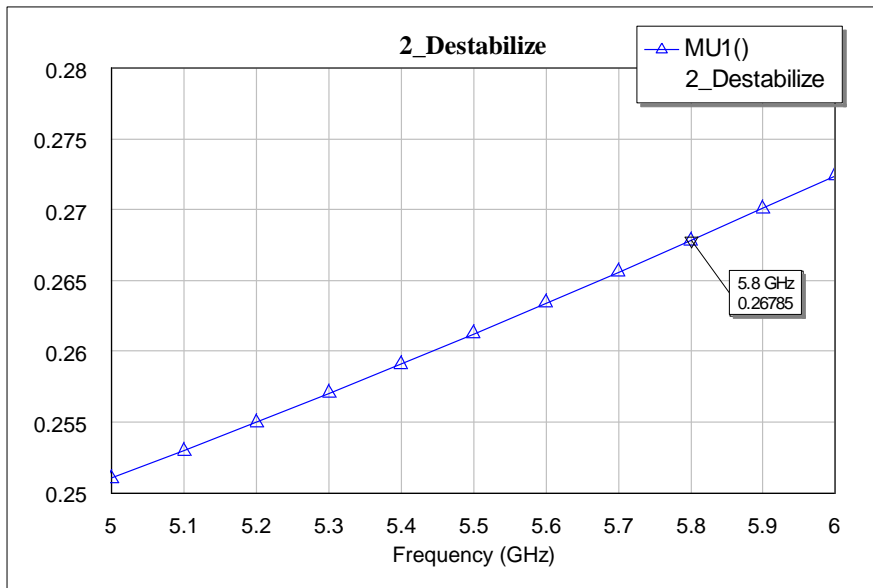


Figure 7: Load Stability Factor

For this design a final source resistance of 18 ohms was chosen. From the Load Stability Factor plot, it can be seen that at 5.8 GHz the load stability factor is equal to about 0.26, whose inverse is 3.86 which indicates that the circuit is adequately destabilized. It should also be noted that from 5 to 6 GHz the load stability factor varies from 0.25 to 0.27 indicating the potential to oscillate across that entire frequency range.

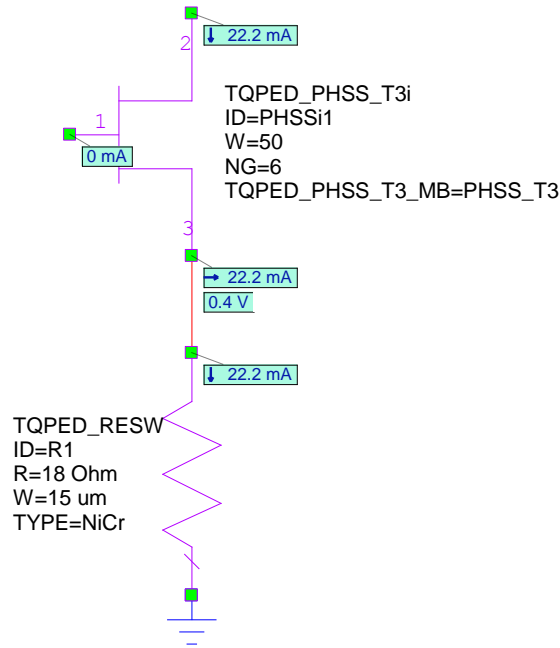


Figure 8: Destabilized pHEMT

Gate Tuning

After destabilizing the active device, the varactor circuit was connected to the gate through a transmission line. This transmission line needs to be adjusted such that the magnitude of S11 at 5.8 GHz is approximately 3. This was done by first using an ideal transmission line to tune the magnitude of S11 until it reached a maximum and then the ideal transmission line was replaced with an appropriate valued inductor.

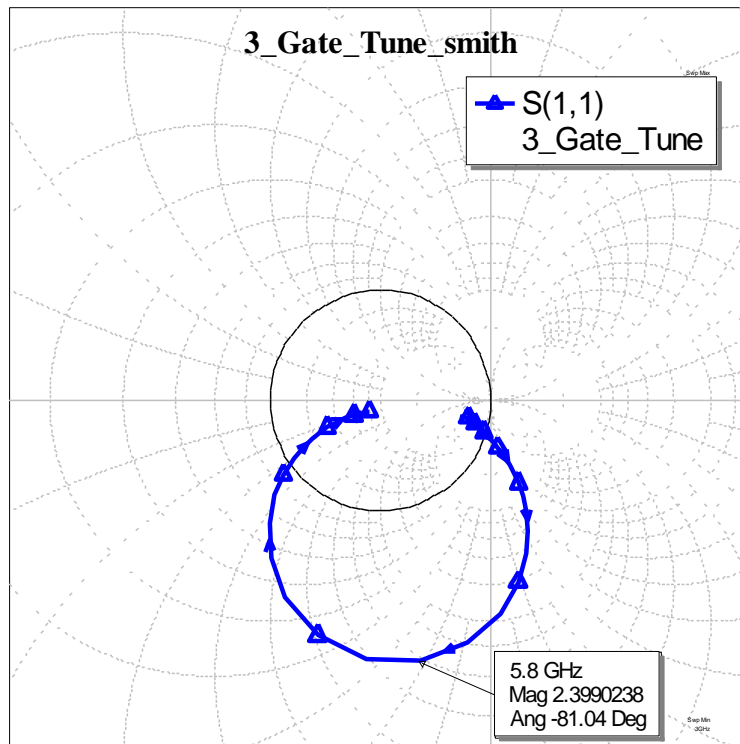


Figure 9: S11 of Gate Tuned Transmission Line

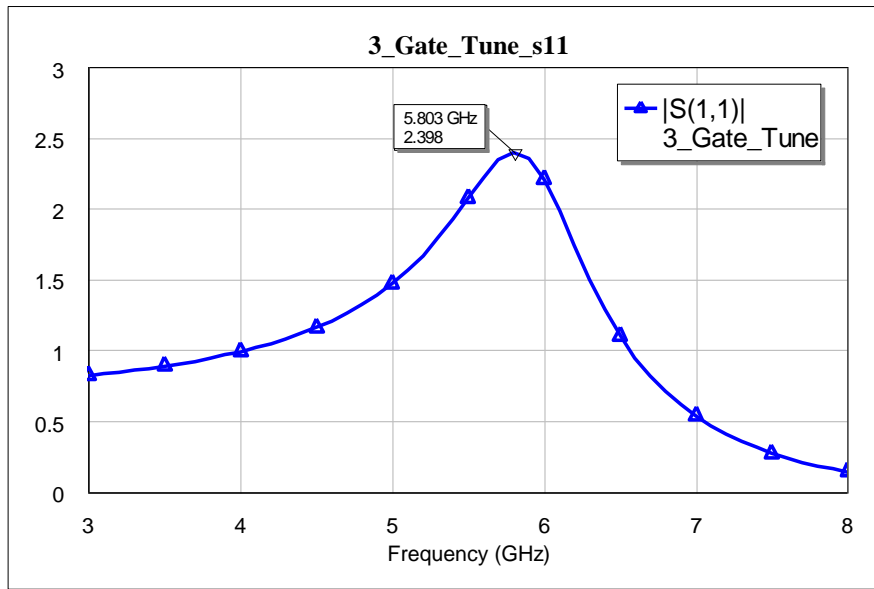


Figure 10: |S11| Rectangular plot showing maximum at 5.8GHz

Drain Tuning

With the circuit now adequately destabilized and the gate tuned to achieve a maximum magnitude of S11, the drain output needs to be tuned so that the reactive impedance satisfies the second start-up condition of $X_D = X_L = 0$. Again, an ideal transmission line was first used to tune the reactive part of the impedance to 0 and then its equivalent lumped element realization was substituted in. Also looking at the imaginary plot of S11 on a rectangular plot, you can see that the circuit demonstrates series resonance which was part of the original start-up conditions.

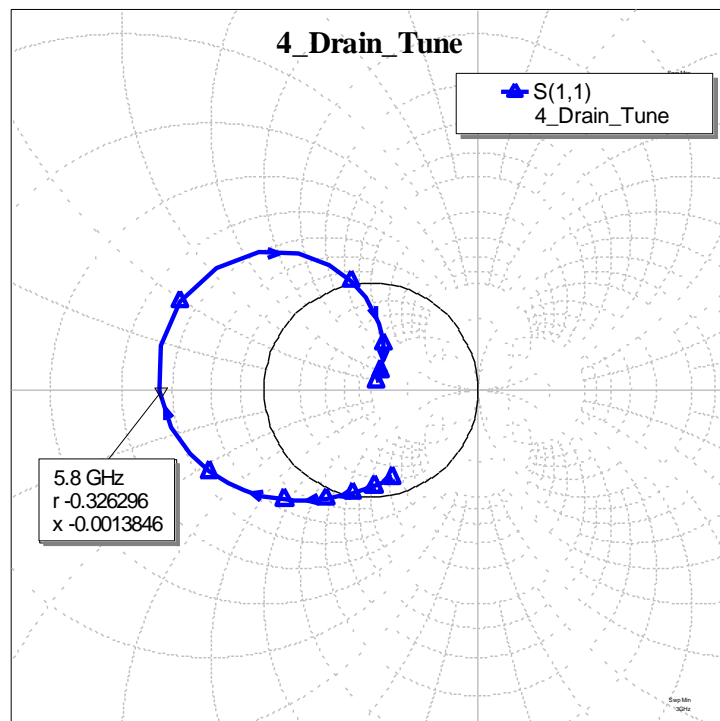


Figure 11: Drain Tuned transmission line

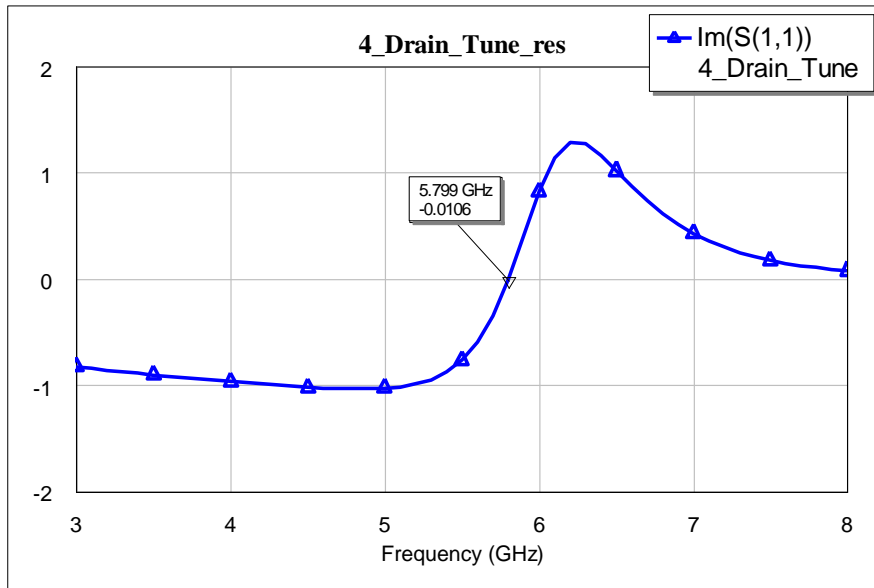


Figure 12: $\text{Im}(S_{11})$ showing series resonance

Output Match

Now that the active network has been designed, a load needs to be designed such that the $|R_p| > 3R_L$ start-up condition is met. From the plot below the resistance of the active network is -13.11Ω . This means that the load needs to be designed such that $R_L = 4.4\Omega$. A quarter wave transformer of $Z_T = 14.8\Omega$ can be used to match the active resistance to the load resistance. Note that Z_{11} resistance of the quarter wave transformer is equal to approximately 4.4Ω as desired.

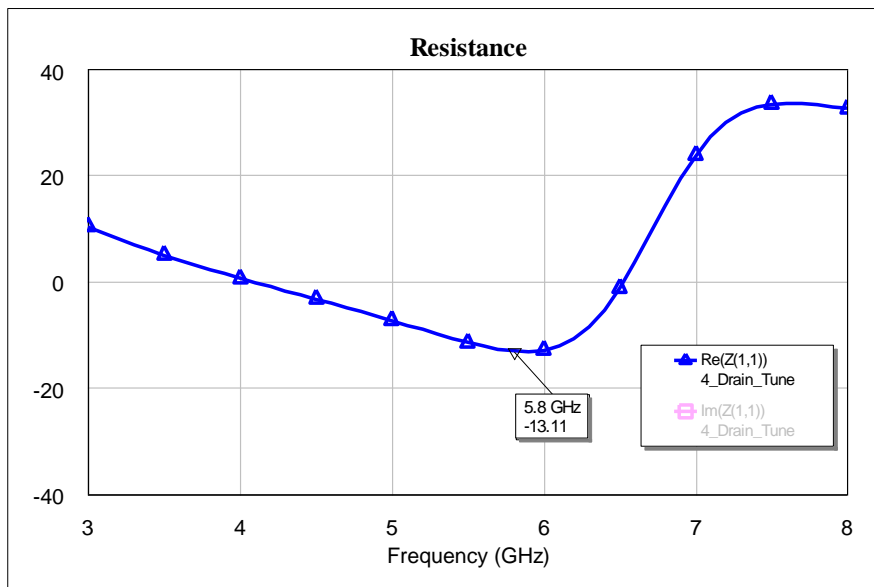


Figure 13: Resistance of Active Circuit

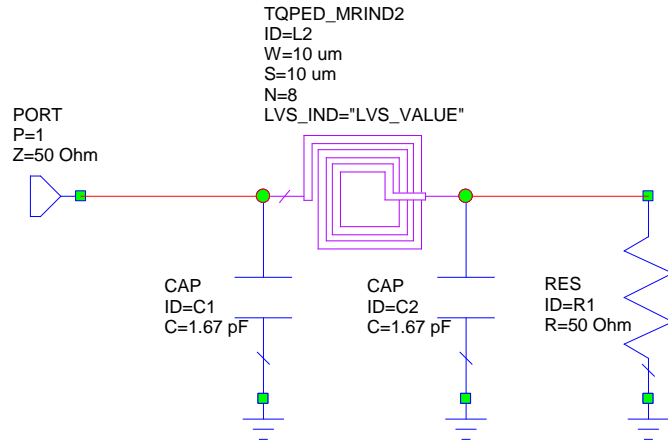


Figure 14: Quarter-Wave Transformer

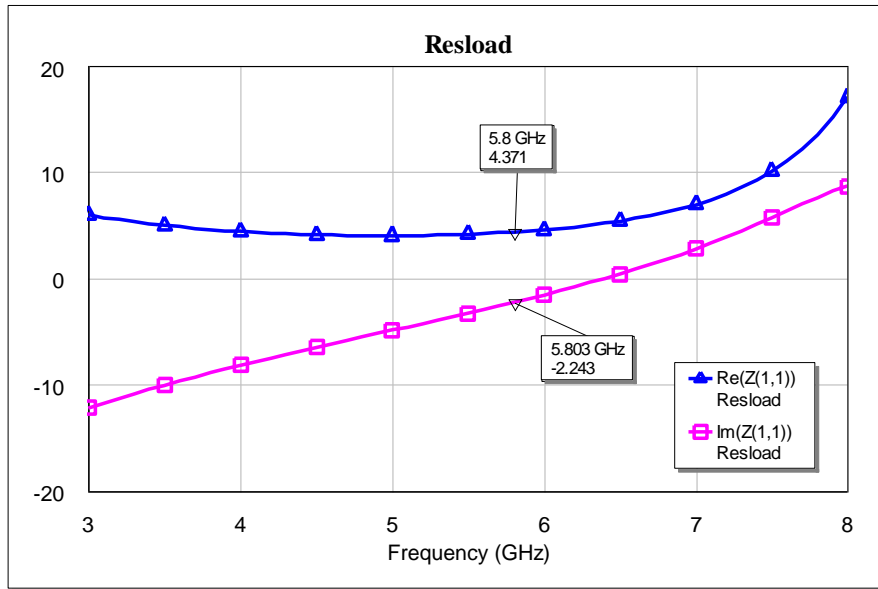


Figure 15: Load resistance of quarter wave transformer

Final Circuit

The final schematic including the output matching circuit can be seen in the figure below.

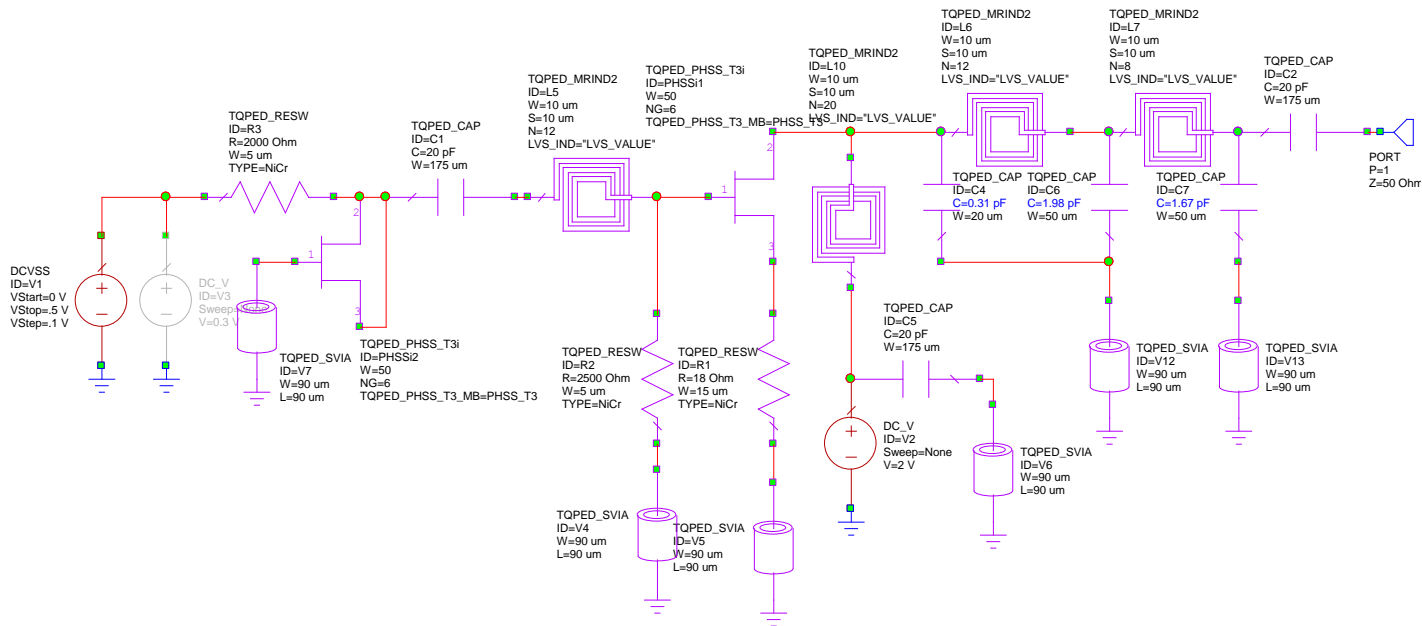


Figure 16: Final Schematic

When simulating the final schematic above, the magnitude of S11 shows where the circuit has the potential to oscillate. Looking at the plot below it can be seen that the circuit has the potential to oscillate anywhere the magnitude of S11 is greater than 1 which is about 5 GHz to 6 GHz. Because the plot below only shows the potential for oscillation, the impedance must also be checked to ensure that the start-up conditions are satisfied.

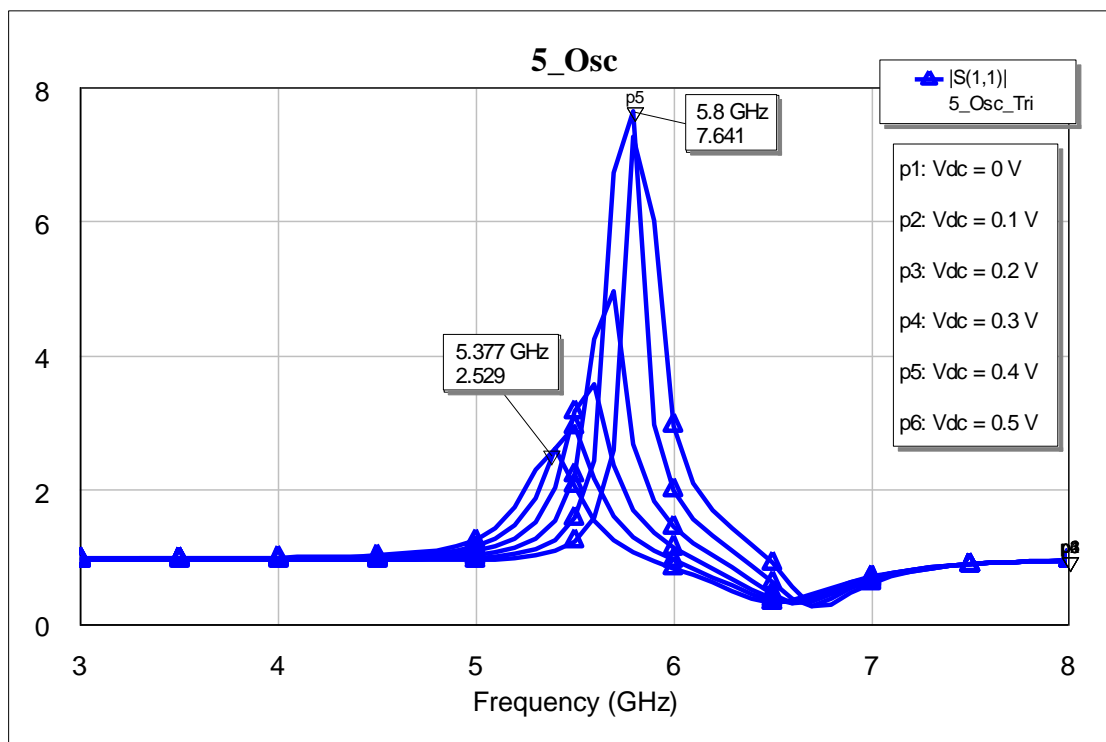


Figure 17: Oscillations

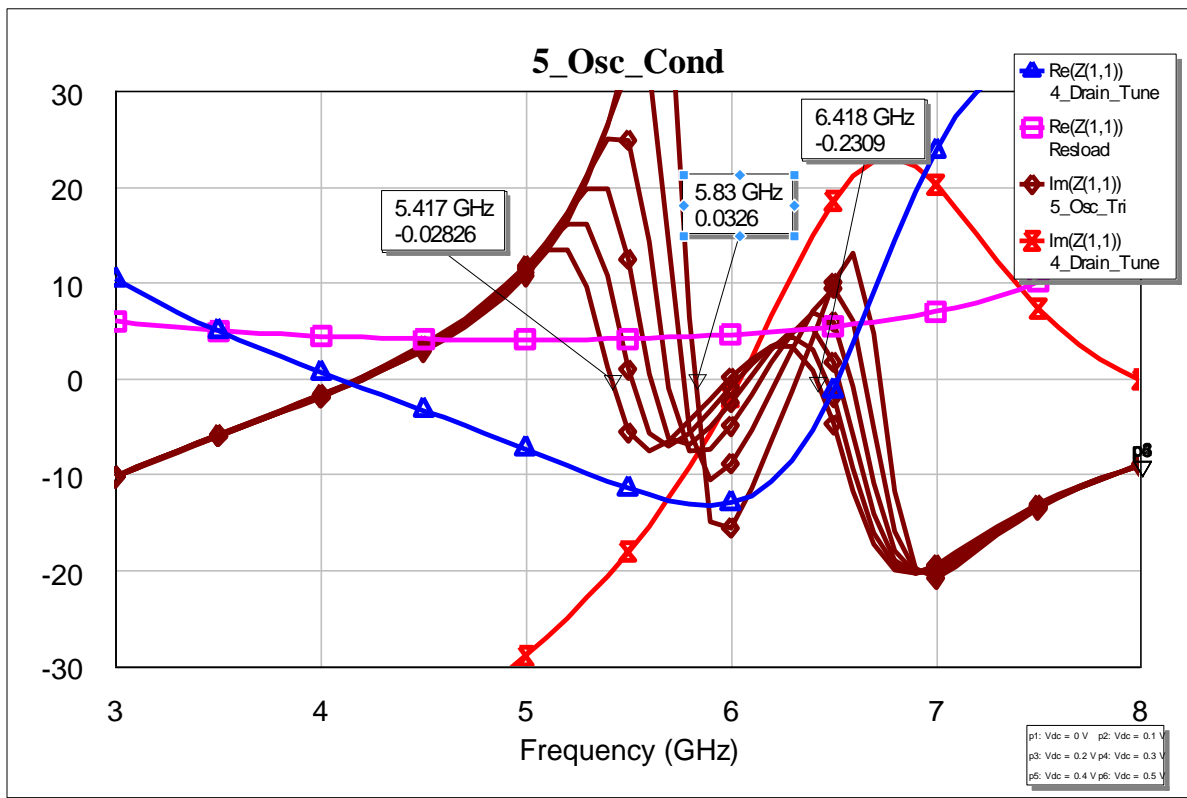


Figure 18: Oscillation Conditions

The plot above details the oscillation conditions. The circuit will oscillate when the active circuit impedance is negative, exhibits series resonance, and the imaginary part of the complete circuit is equal to zero. From the plot above you can see that for the tuning range of 0V to 0.6V, the circuit meets the start-up conditions between 5.4 GHz and 6.0 GHz.

After looking at the linear simulations results, a non-linear simulation was created to see how the results compare. The tool that allows for this non-linear simulation is called OSCAPROBE. From the non-linear simulation you can see that the oscillation frequency matches up very well with the results from the linear simulation. Also from the non-linear simulation you can see that for a tune voltage of 0.5V, the circuit will oscillate at 5.8 GHz with an approximate output power of +8dBm.

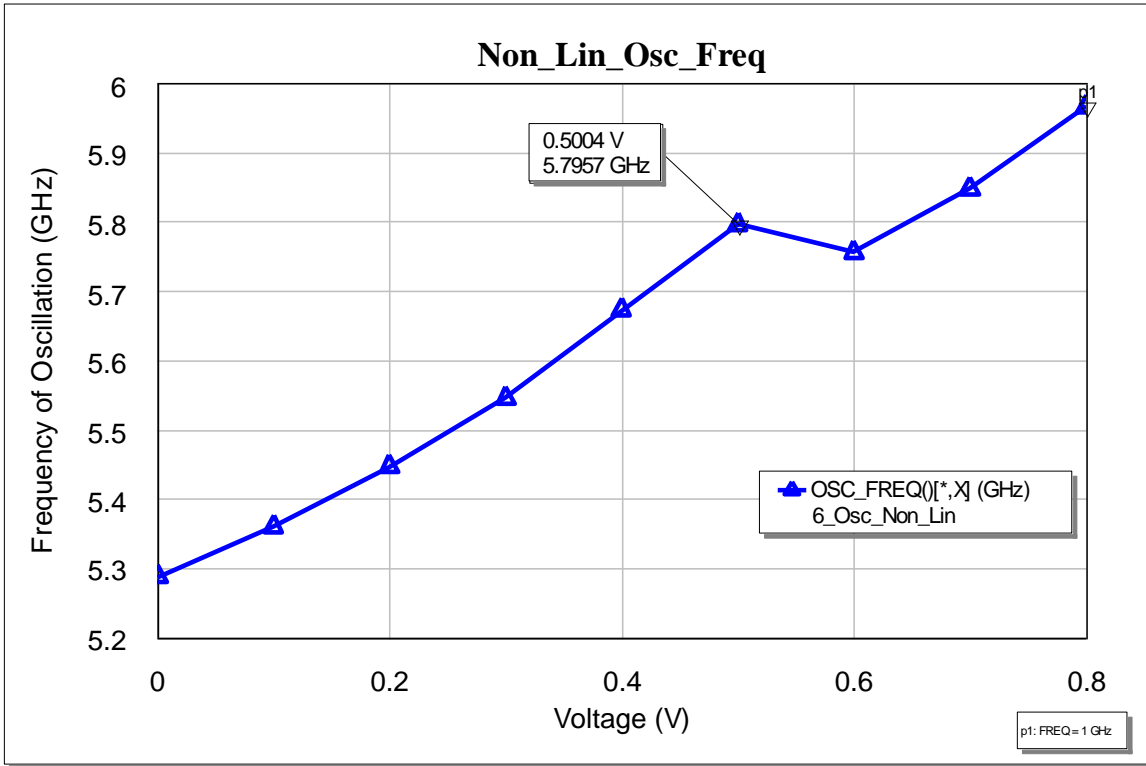


Figure 19: Non-Linear Frequency of Oscillation

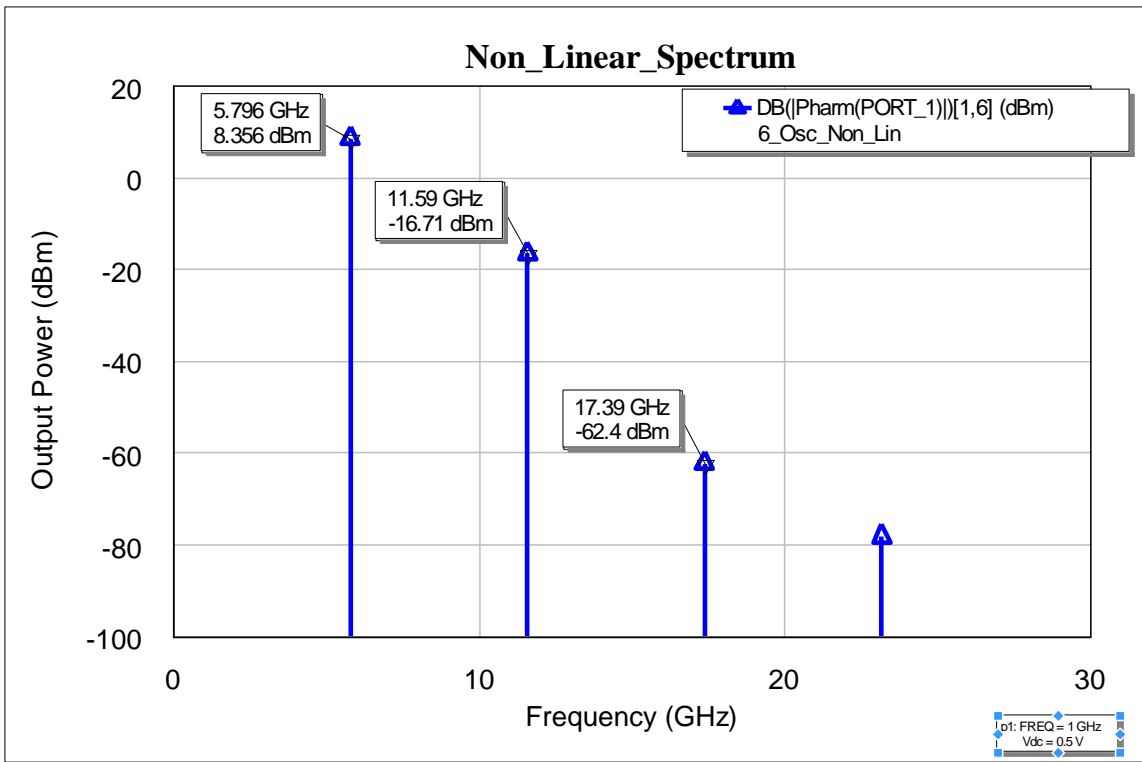


Figure 20: Non-Linear Output Power

A final check of the bias shows that the circuit is indeed operating at 2V at 22mA. The width of the destabilizing resistor is sized to 15um to handle the 22mA of current that are flowing through it.

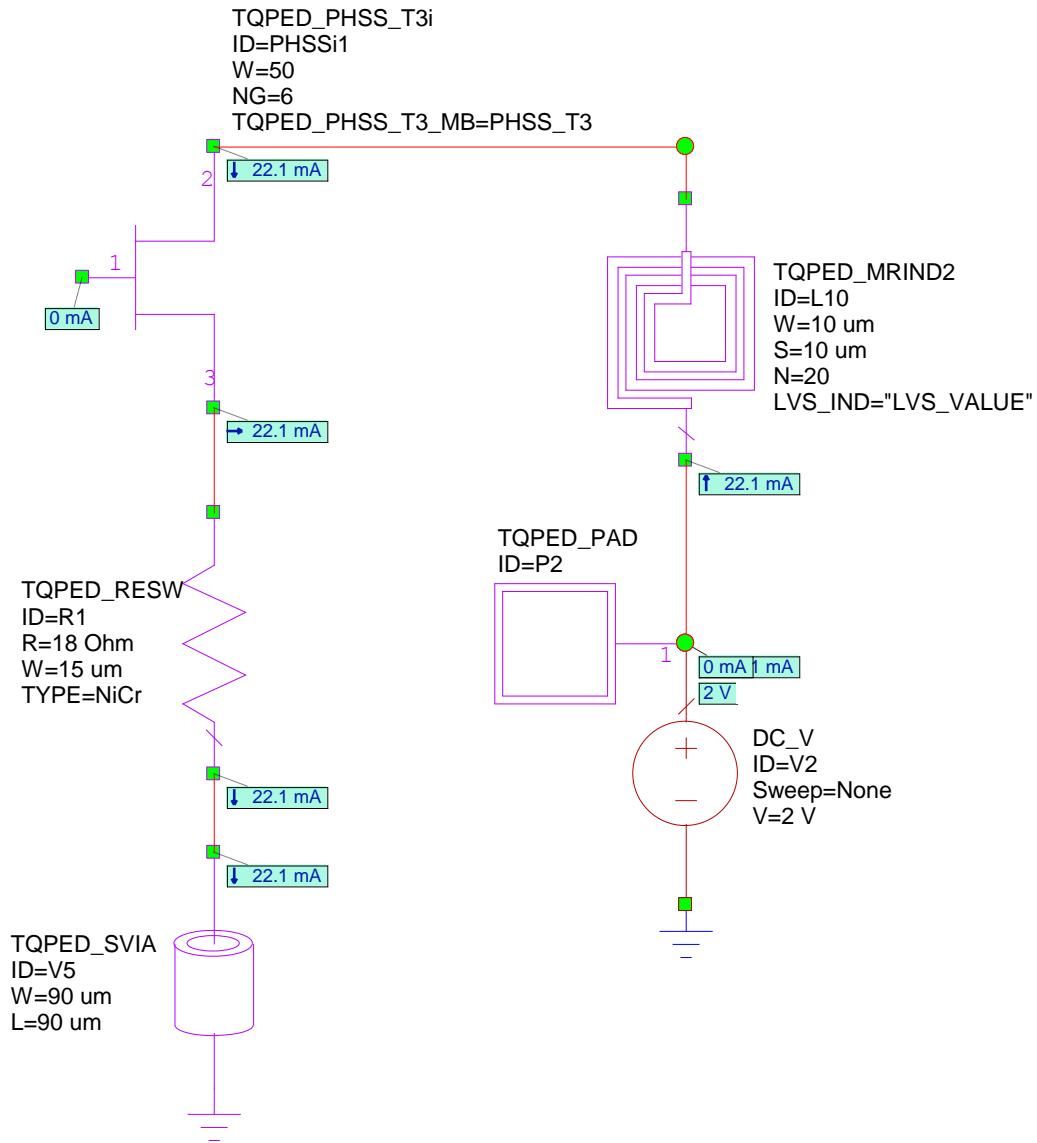


Figure 21: Final DC Bias

Layout

The layout of the design is shown below and fits within the 60 mil x 60 mil ANACHIP layout. All pads are labeled appropriately for the “VDS,” “VTune,” and “Output” pads. The ground-signal-ground configuration is used for the RF output of the circuit. The layout has been arranged to try and minimize the lengths of the route, as well as to avoid and crossovers. The extraction of this layout, including the interconnects is included in the above final schematic simulations. A DRC check was run on this layout with no major issues or violations.

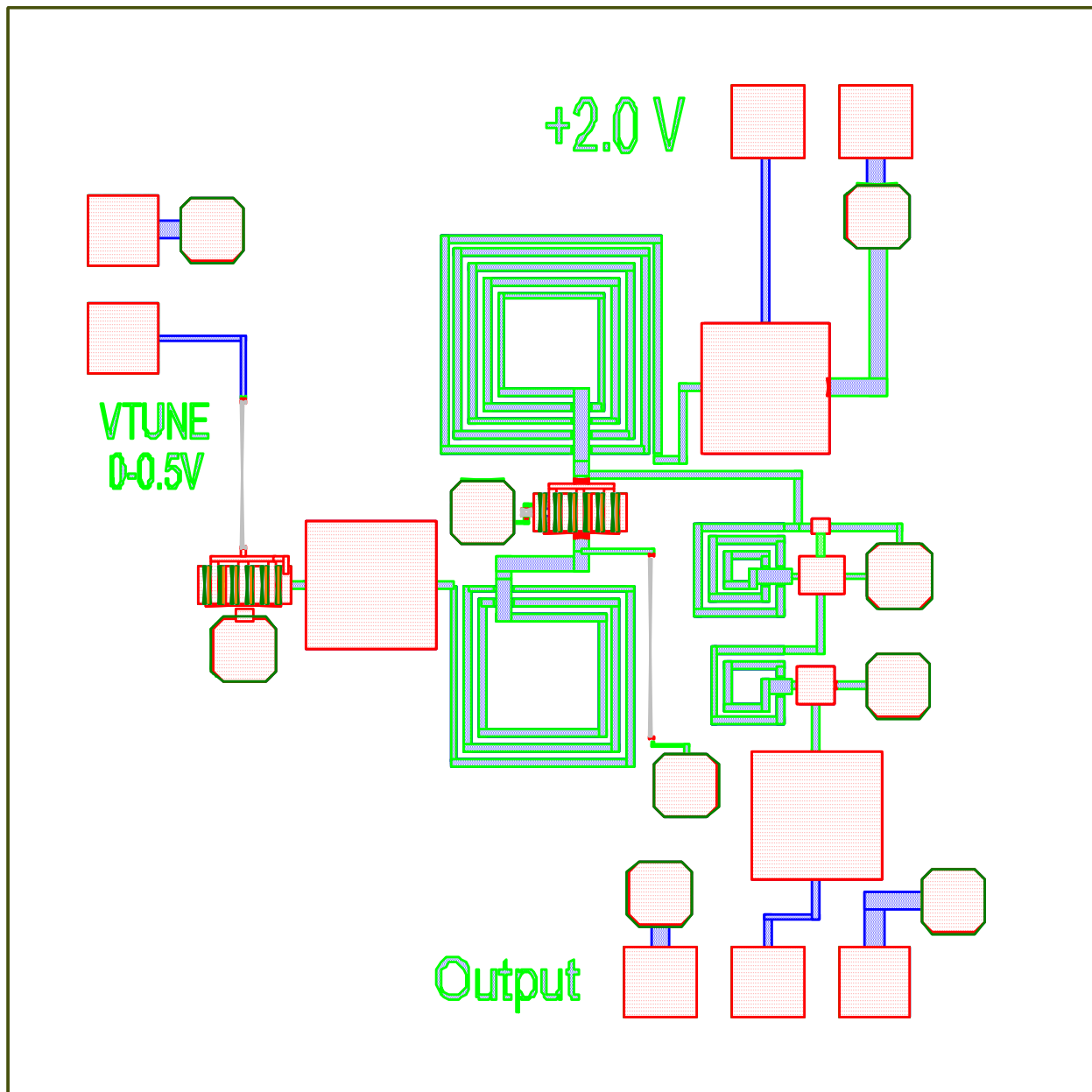


Figure 22: Final Layout

Test Plan

This section of the report will discuss the test plan and procedures that will be used to measure the performance of the VCO. Testing will take place at the John's Hopkins Dorsey Center with equipment available in the lab.

DC Check

The initial check shall be a DC check to ensure that none of the voltage or signal pads are shorted to ground. Once this check is performed and there are no shorts are found, apply +2V to the "VDS" pad and measure the current draw. The expected current draw should be around 22mA.

Spec: No shorts to ground

+2.0 V @ 22mA nominal

Frequency of Oscillation

Once the DC check has been performed, connect a second DC voltage supply to the "VTune" pad at an initial value of 0V. Connect the "Output" pad to a spectrum analyzer. Measure and record the frequency of oscillation as well as the output power. Repeat this process by sweeping the "VTune" voltage from 0.0V to 0.6V in 0.1V steps. Note that the tune voltage range can be extended to see limitations of the varactor.

Spec: Frequency Rand of 5.4 GHz to 6 GHz

Tune Voltage of 0V to 0.6V

Output Power (TBD)

Out of Band Oscillations

This test will confirm that there are no un-expected oscillations occurring. Apply +2V to the "VDS" pad and 0.5V to the "VTune" pad. Sweep on the spectrum analyzer from 0 to 10 GHz and observe if there are any out of band oscillations.

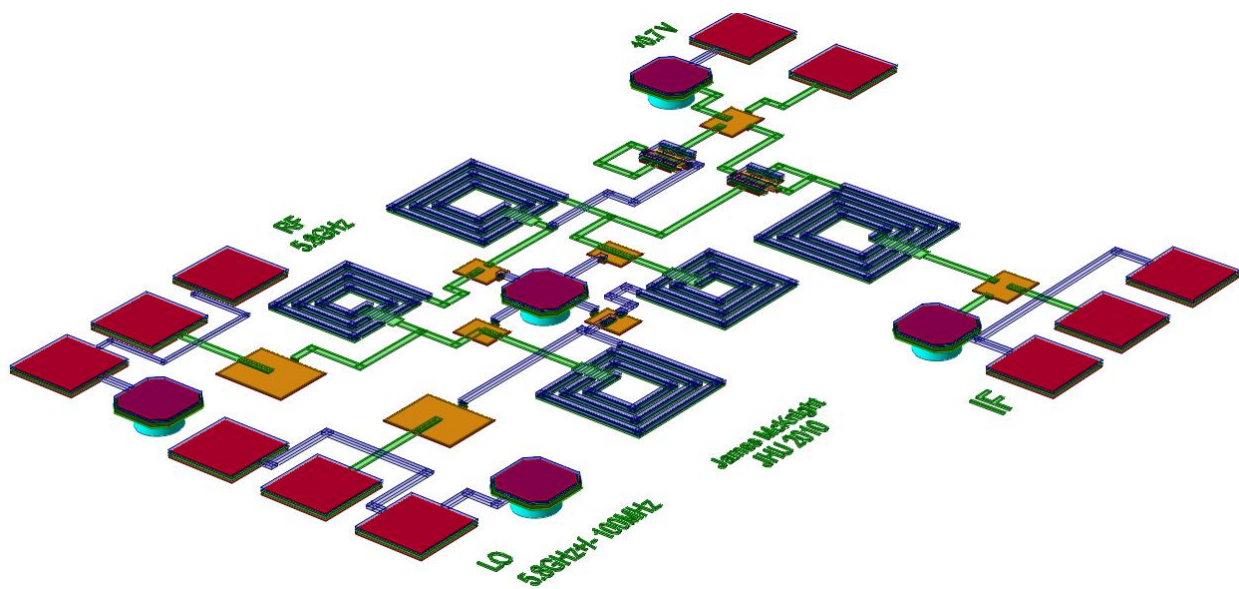
Spec: No out of band oscillations

Conclusion

This report has detailed the design of a Voltage Controlled Oscillator using the theory of negative impedance. The design was realized with TriQuint elements and the TQPED process and was simulated using Microwave Office. The design meets all electrical specifications and the layout fits in the 60 mil x 60 mil ANACHIP layout.

The final design has a tuning range from 5.4GHz to 6.0GHz with an approximate output power of +8dBm. The device is powered off of a +2V supply with a tuning voltage of 0.0V to 0.6V. This particular device is designed for an output impedance of 50 ohms, but it could easily be changed depending on the needs of the system.

5.8 GHz Single-Balanced Hybrid Mixer



James McKnight
MMIC Design – EE 525.787
JHU Fall 2010
Professor John Penn

Abstract

This report details the design of a C-Band monolithic microwave integrated circuit (MMIC) single-balanced mixer. The mixer was designed for a radio frequency (RF) input range of 5.7 – 5.9 GHz and local oscillator (LO) design frequencies from 5.6-5.8(LSLO) or 5.8-6 GHz (HSLO), for a resultant down-converted intermediate frequency (IF) of 100 MHz. This standard mixer topology is constructed on a 4-port 90° hybrid mixer and two Field Effect Transistors (FETs) configured as diodes. The design simulations showed conversion loss <10dB, return loss >10dB and RF-LO isolation >10dB over the entire band of interest. For this performance, however, a large LO drive-level of +10dBm was required. All simulations are based on the Triquint model library parts process and fitting within a 60mil x 60mil Anachip layout.

1 Introduction

RF mixers are 3-port active or passive devices which are designed to yield both sum and differences of input signals. Often referred to as “frequency translation devices”, mixers are most commonly used to convert one frequency to another for ease of transmission or signal processing. In order to produce new frequencies (combinations of RF and LO), mixers require nonlinear devices. The single-balanced mixer employs two diodes whose effects are combined through a hybrid coupler junction (Figure 1). The hybrid network also allows the RF and LO to feed the device while maintaining relatively strong RF-LO isolation.

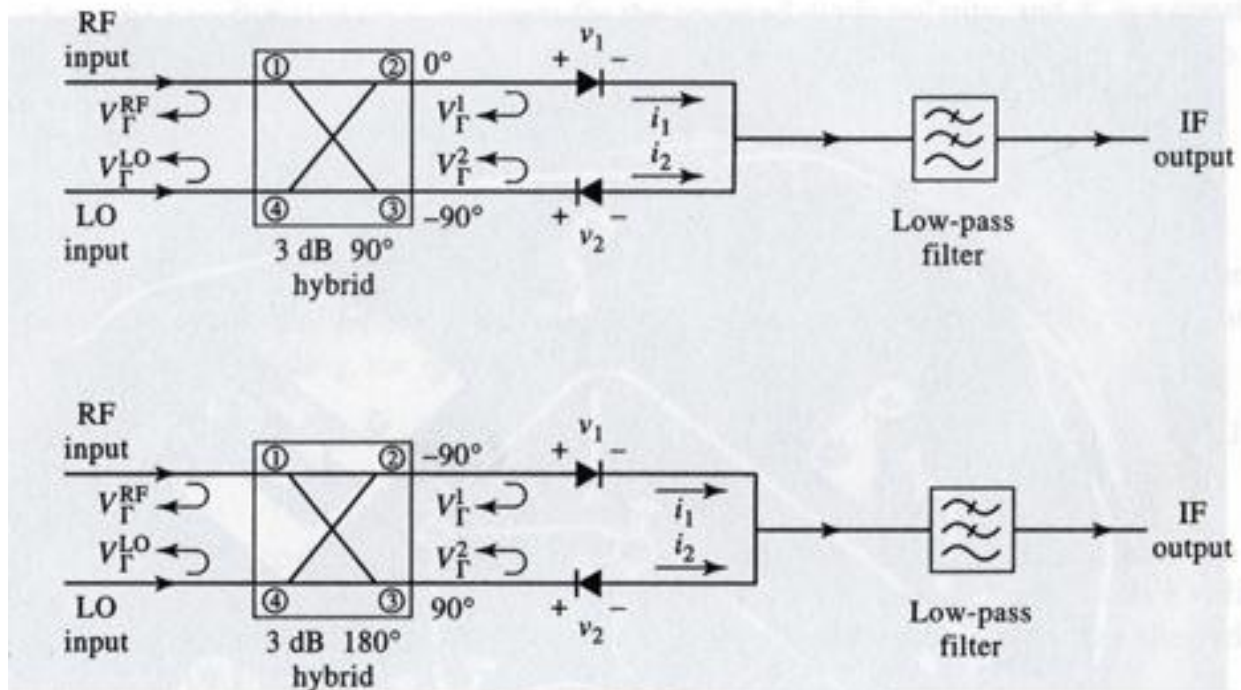


Figure 1 - Balanced mixers topologies (Pozar)

The RF input frequencies range from 5.7 – 5.9 GHz and the LO frequencies range from 5.6 – 6 GHz. The design targeted a maximum LO power of +5dBm, yet simulations showed a functional design at +10dBm. Simulations demonstrate conversion loss approximately 9dB. Each segment of the device, its design and performance is elucidated in subsequent sections.

2 Design Approach

Mixers are an important component in the RF chain for an array of communication systems (i.e. superheterodyne receivers), and, as such, require certain specifications to properly function in concert with other RF components. Outlined in Table 1 are a list of basic mixer specifications.

Table 1: Balanced hybrid mixer design requirements

Mixer Property	Minimum Requirement	Goal
RF Frequency	5.7 - 5.9 GHz	5.7 - 5.9 GHz
LO Frequency	5.6 - 6.0 GHz	5.6 - 6.0 GHz
IF Frequency	100 MHz	100 MHz
RF Power	< 0dBm	< -5dBm
LO Power	< 15 dBm	5-10 dBm
Conversion Loss	< 15dB	< 10dB
Supply Voltage	0-3V	0.7V
RF and LO Return Loss	> 8dB	> 10dB

The design process evolved piecewise, developing the coupler, FET diodes and LPF separately. Initial design began with ideal parts and subsequent iterations incorporated parasitic parts – the device was tuned regularly to compensate for the parasitic effects.

90 Hybrid Coupler Design

Central to the single-balanced mixer is the 90° hybrid coupler. The coupler design hinges entirely on the characteristic impedance and frequency of operation, chosen respectively to be 50Ω and 5.8 GHz. The Balanced mixers made with the 90° hybrid coupler will, in theory, have a better input match over a wide bandwidth relative to those using the rat-race coupler. With the hybrid coupler, either the LO drive or the RF signal is balanced (applied in anti-phase), adding destructively at the IF port of the mixer and providing inherent rejection. The level of rejection is dependent on the amplitude and phase balance of the coupler.

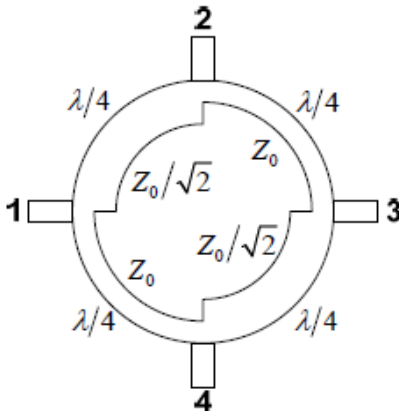


Figure 2 – Distributed Hybrid Coupler

A basic hybrid coupler made of distributed lines is shown in Figure 2. To conserve chip space and for ease of use, a lumped-element equivalent circuit can be used in its place. The coupler was designed with the equations below and simulated with both ideal and parasitic Triquint parts.

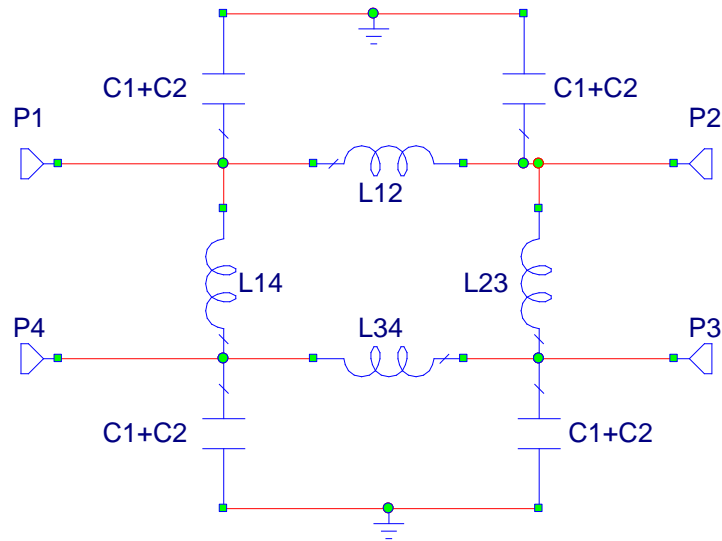


Figure 3 – Lumped Hybrid Coupler

$$L_{12} = L_{34} = \frac{Z_0 / \sqrt{2}}{w}$$

$$L_{23} = L_{14} = \frac{Z_0}{w}$$

$$C_{12} = C_{34} = \frac{1}{w * Z_0 / \sqrt{2}}$$

$$C_{23} = L_{41} = \frac{1}{w * Z_0}$$

$$C_1 + C_2 = C_{12} + C_{23}$$

with,

$$Z_0 = 50\Omega$$

$$w = 2 * \pi * f$$

$$f = 5.8 \text{ GHz}$$

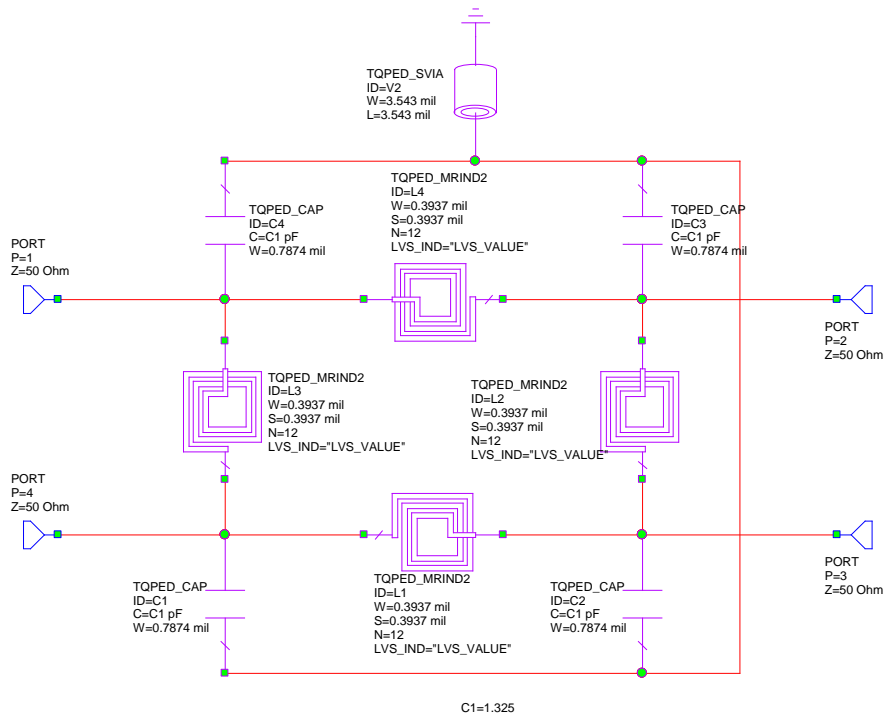


Figure 4 - Hybrid Coupler Schematic w/ Triquint parts

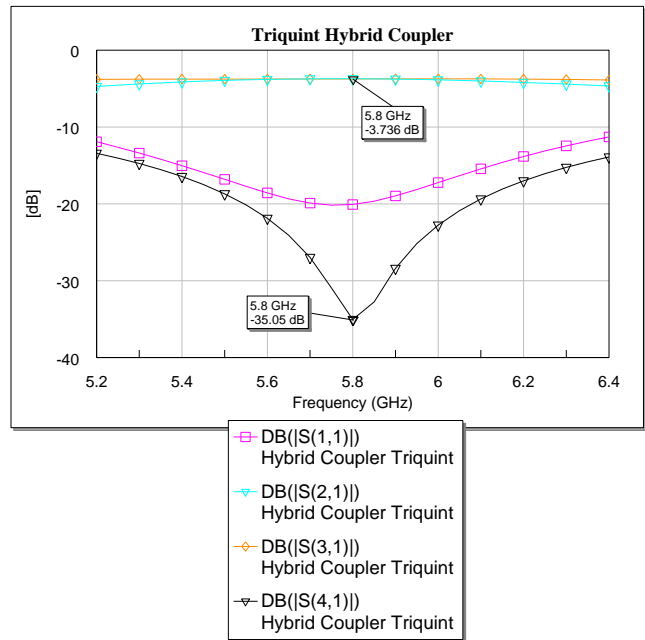
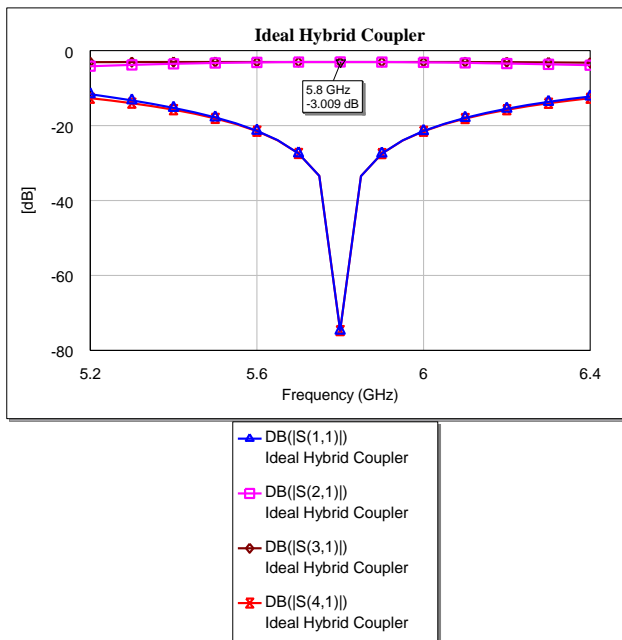


Figure 5 - 90 Hybrid Coupler S-parameters (Mag.)

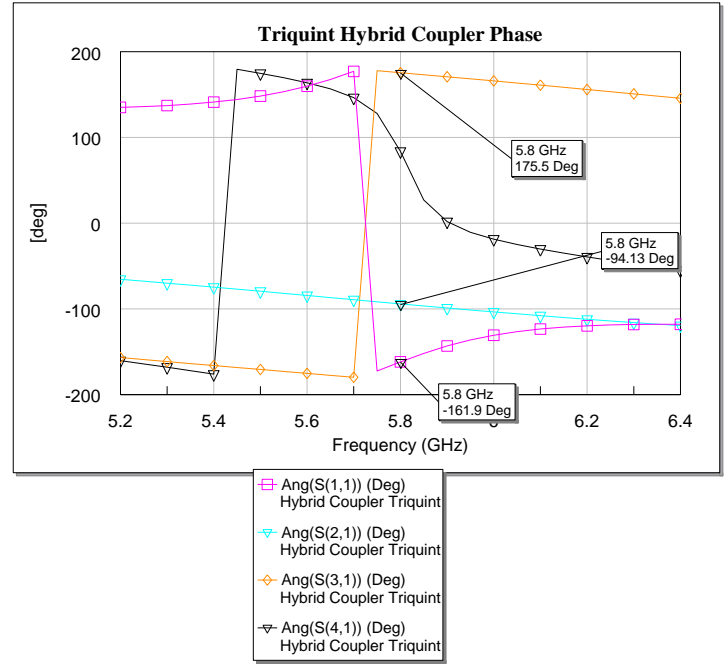
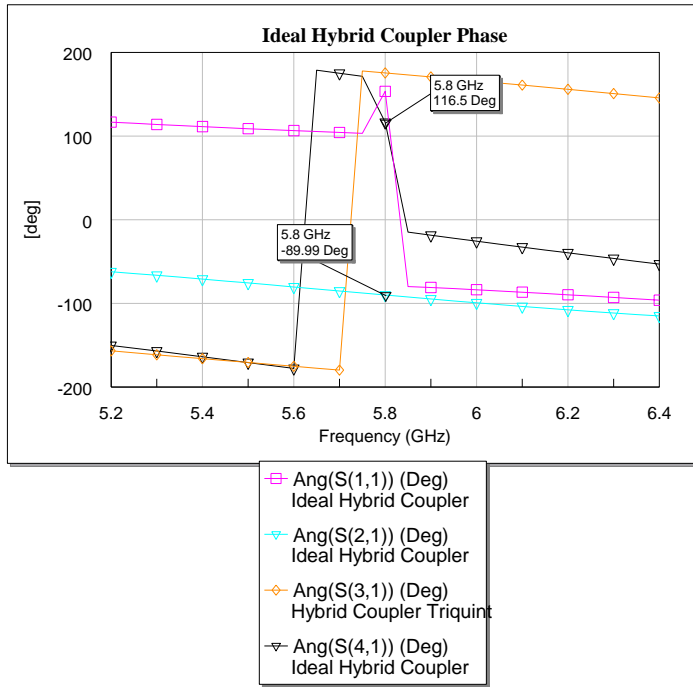


Figure 6 - 90 Hybrid Coupler S-parameters (Phs.)

FET Diodes

The simple P-N junction of a diode can be created by shorting together the drain and source terminals of a FET. For this design, two Triquint, D-mode, PHEMT FETs are used.

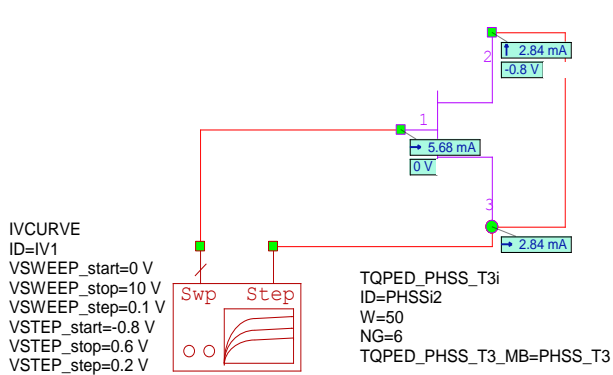


Figure 7 - Triquint FET operating as a diode

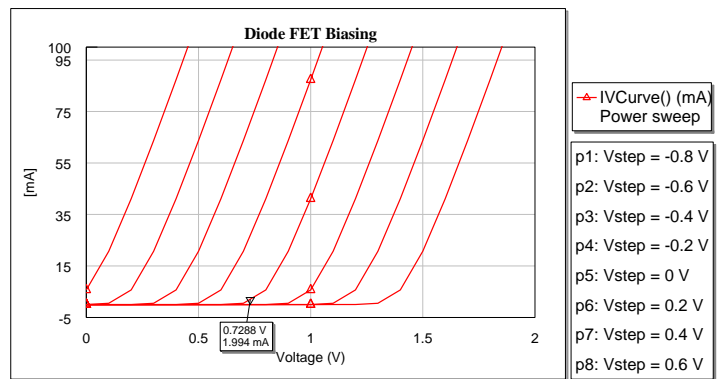


Figure 8 - Diode curves showing +0.7V turn-on

Figures 2 and 3 demonstrate the true diode-like behavior of the Triquint FETs. For the case where Vstep (applied to the “cathode”) is 0V, the device is shown to be forward conducting when +0.7VDC is applied to the “anode”, the nominal diode turn-on voltage.

Mixer Design

When driven properly, the nonlinear devices create a wide variety of harmonics which are pivotal to strong intermodulation products and low conversion loss. However, a common disadvantage of balanced mixers is their greater LO power requirements. To tease out that problem upfront, the complete coupler was built entirely of ideal blocks, but with Triquint FETs. Conversion loss was observed for three diode FETs while sweeping LO power from 0-25dBm - each of the three FETs have a different number of gate fingers. The plots below depict how reducing the number of gates fingers (while maintaining the same gate width), can drastically reduce the LO power needed to drive the diodes for low conversion loss.

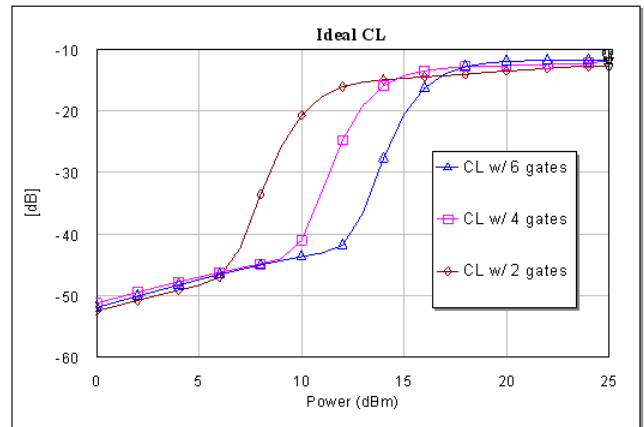
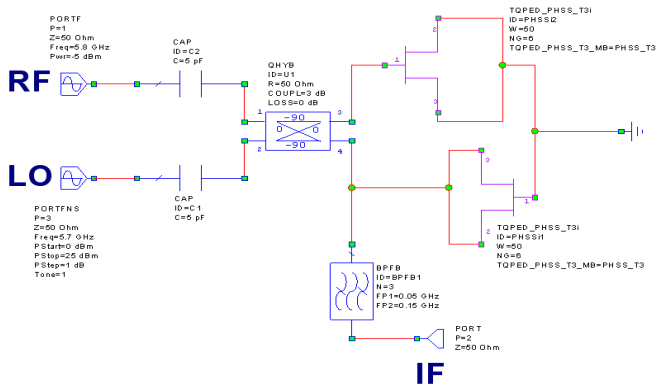
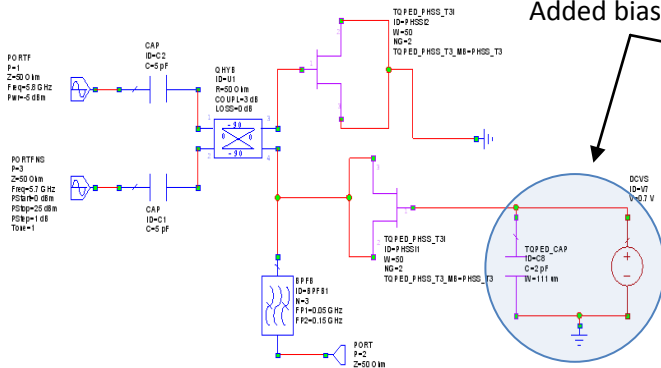


Figure 9 – Conversion Loss vs. LO sweep to determine number of FET gates

Ideal Diode Mixer



Added biasing

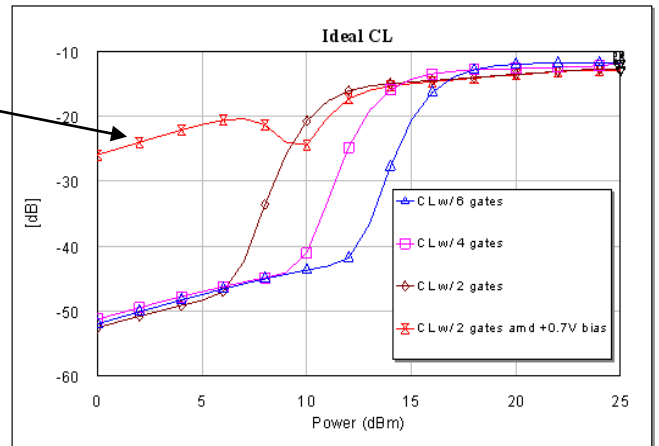


Figure 10 – Conversion Loss vs. LO sweep w/ DC bias

Additionally, a simple 0.7V bias circuit is applied to one of the diodes can bring up the conversion loss by ~25dB for all LO input power levels. Still, the conversion loss is unacceptably low at > 20dB.

Trade-offs

A main focus of this work was to keep the design simple while fully functional. There were many niceties which may have been included for performance increases, but may not have been worth their space on the limited chip size. Reducing the number of gates greatly improved the LO drive level needed, but altering gate width offered up its own trade-offs. A wider gate had lower conversion loss, but only at higher LO power levels. Conversely, a narrower gate was driven better with lower LO power, but had ~5dB more CL. The DC bias only marginally improved the LO power needed for low conversion loss, but was included in the end.

3 Simulations

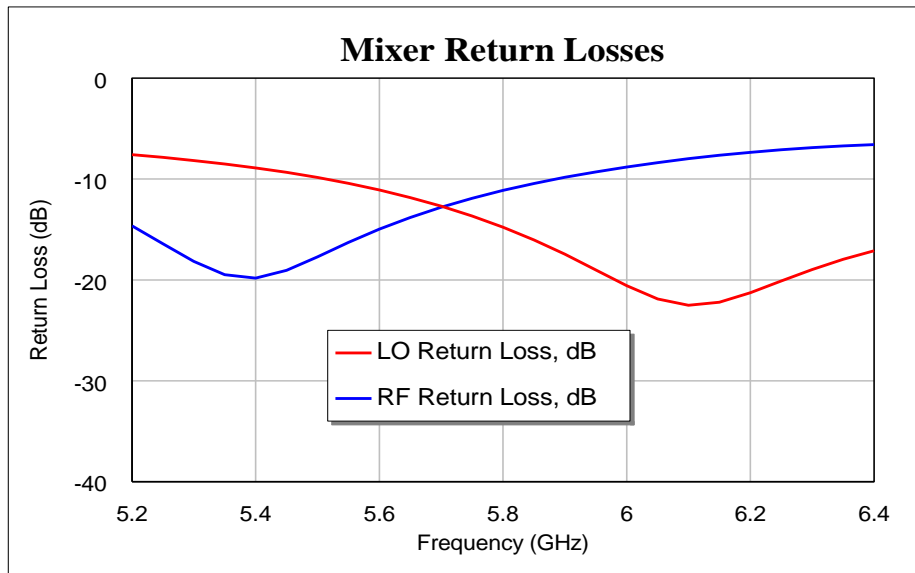


Figure 11 – Return Loss vs. LO sweep w/ DC bias

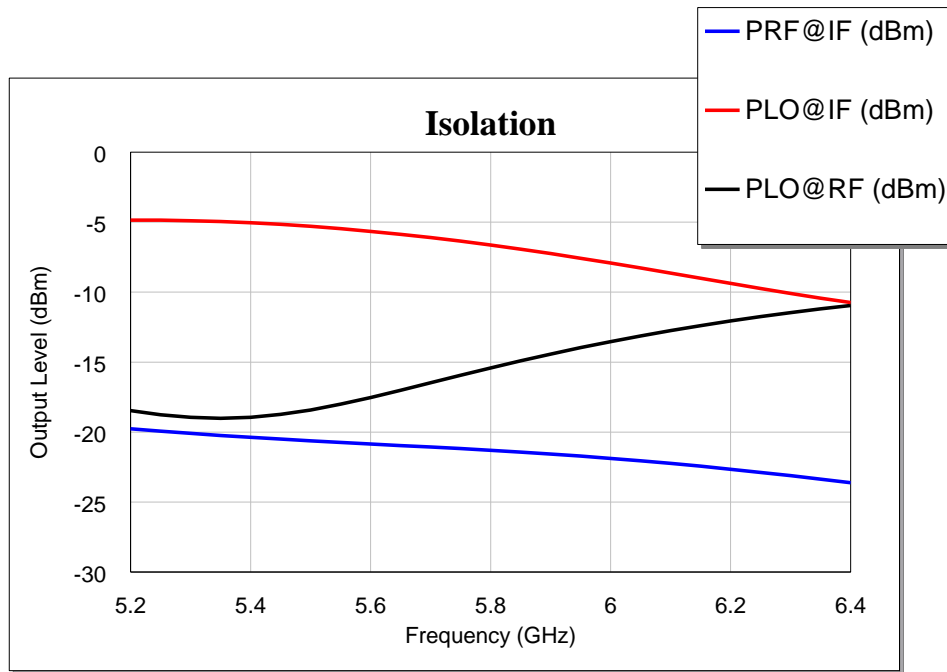


Figure 12 – Mixer Isolation

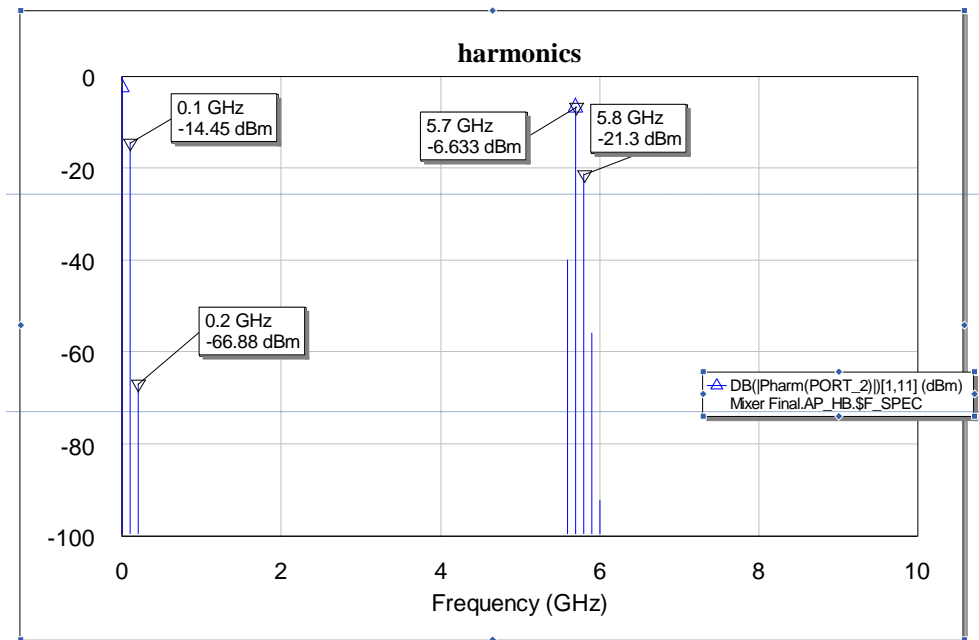


Figure 13 – RF Spectrum

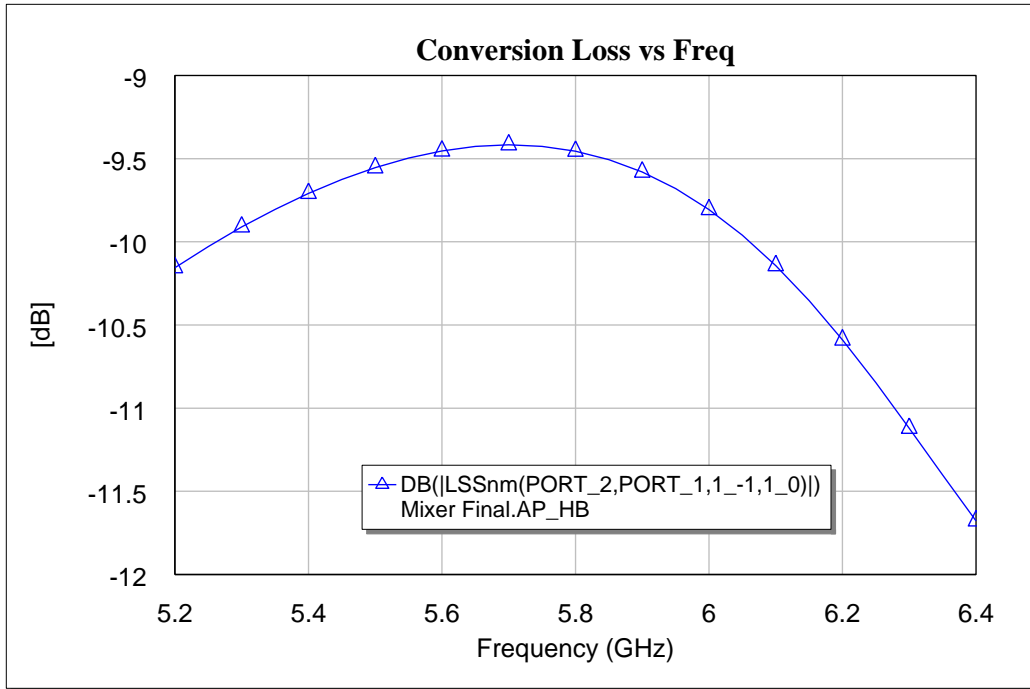


Figure 14 – Conversion Loss over frequency

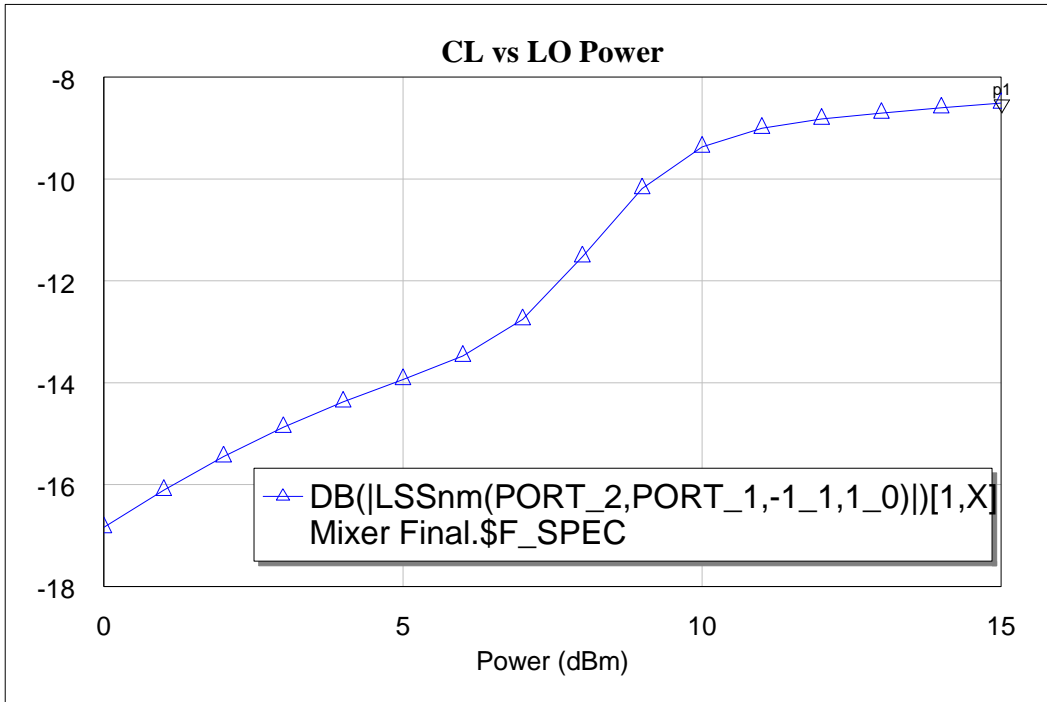


Figure 15 – Conversion Loss vs. LO drive

4 Schematic

RF Schematic

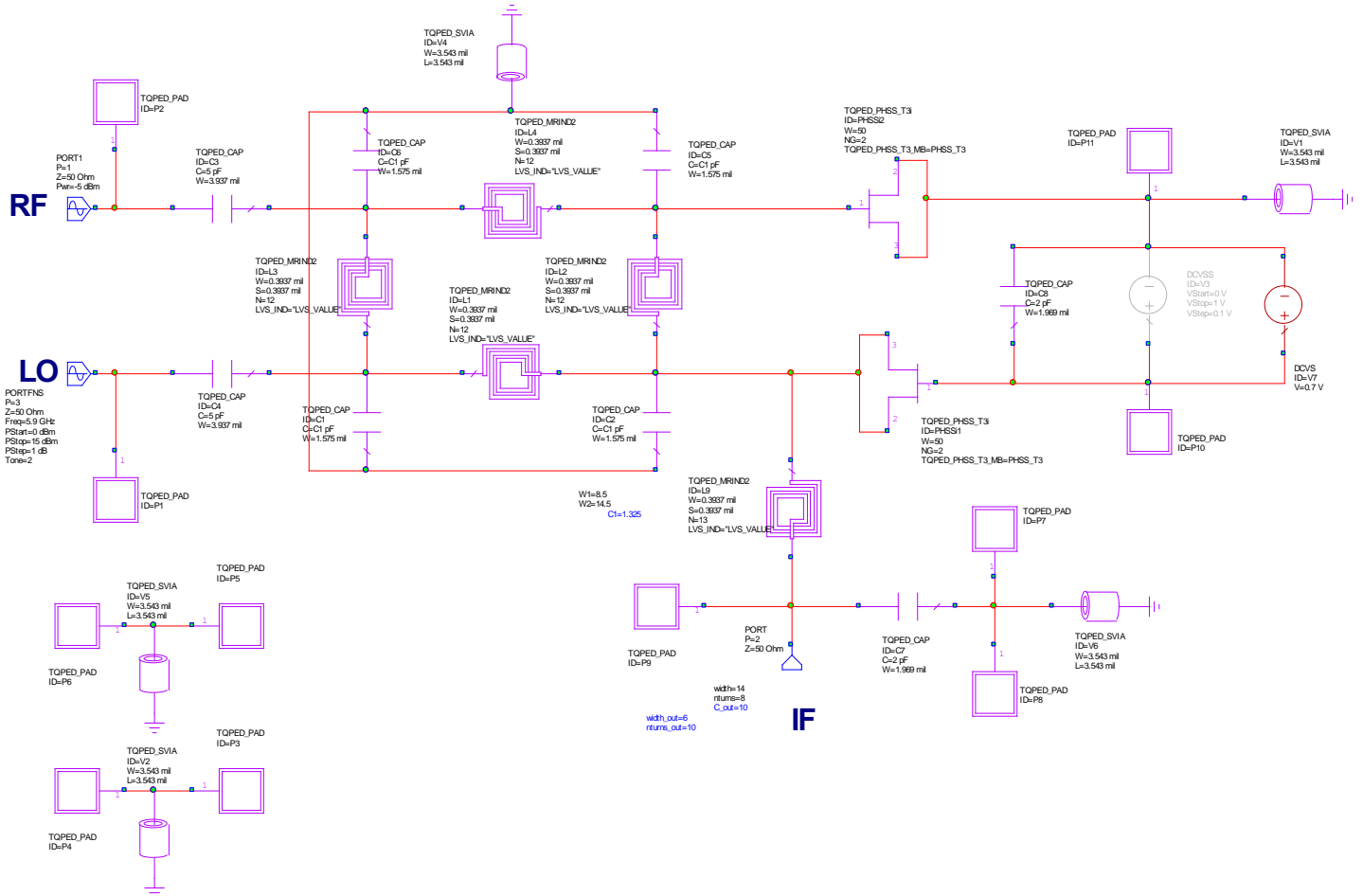


Figure 12 - RF Schematic for Hybrid Mixer

DC Schematic

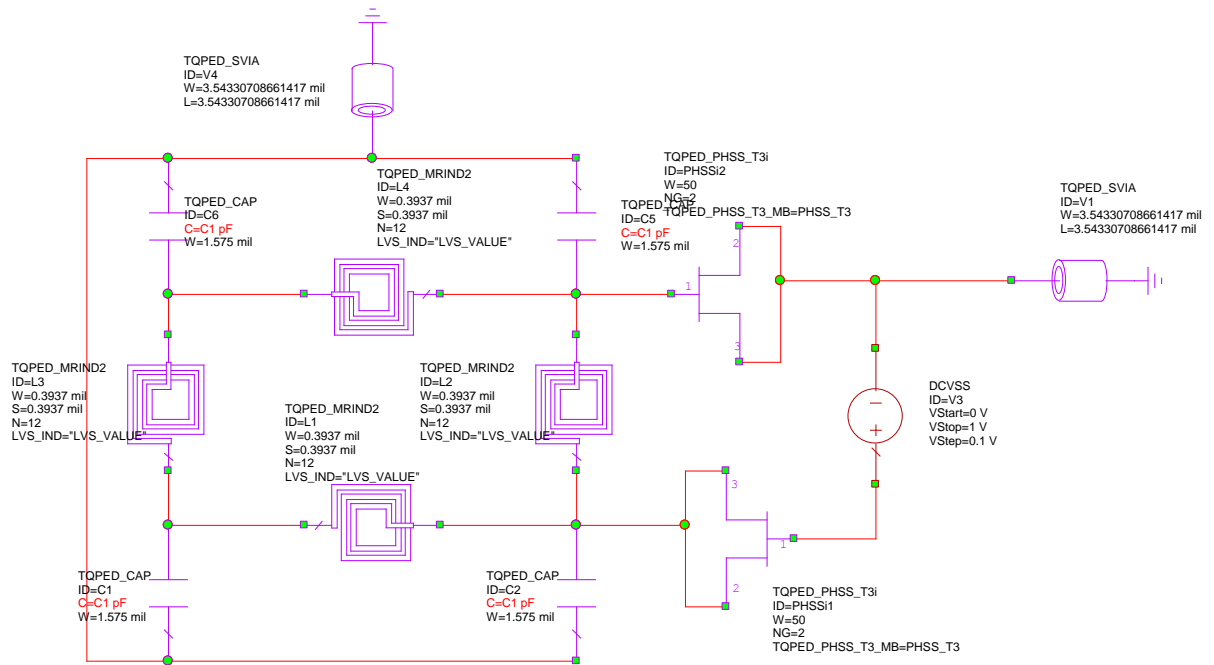


Figure 13 - DC schematic for single-balanced hybrid Mixer

5 Layout

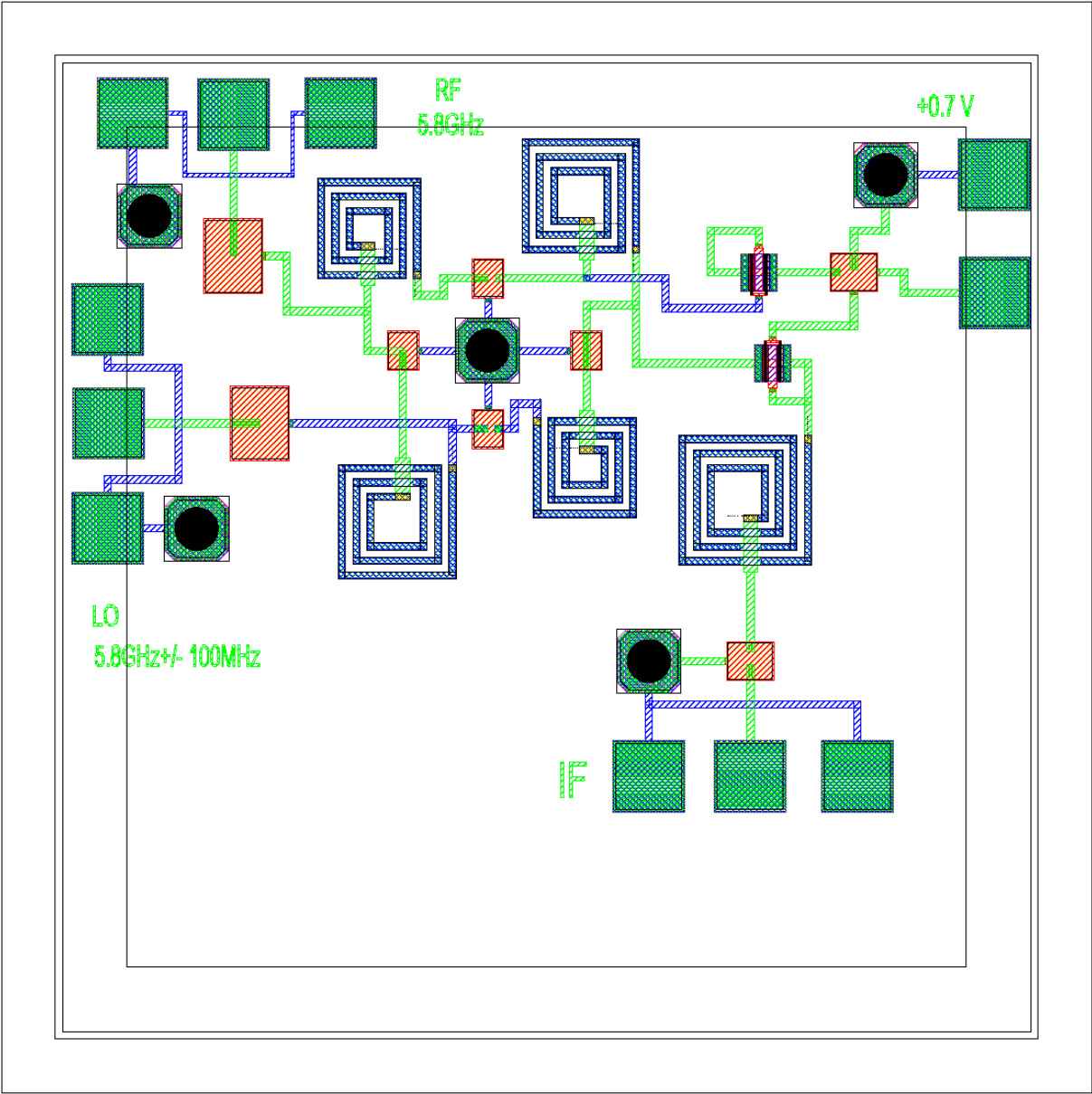


Figure 14 - S-band single-balanced mixer layout

6 Test Plan

DC Testing

1. Apply DC probe to the DC bias terminal
2. Apply power meter to IF port
3. Slowly increase V_{DC} to +0.7V
4. Look for ~0.07V (as was simulated)

Down Mixer Testing

1. Calibrate the network work analyzer for 5.2 to 6.0GHz
2. Connect a signal generator or VNA to the LO port for CW @ 5.7GHz
3. Set LO power to +10dBm
4. Connect a signal generator or VNA to the RF port for CW @ 5.8GHz
5. Set RF power to -5dBm
6. Connect a spectrum analyzer to the IF port
7. Apply +0.7VDC to the DC bias terminal
8. Measure the 100MHz IF output power at each frequency interval

7 Conclusions

A C-band single-balanced mixer was designed and simulated to meet most design requirements. The device was capable of achieving <10dB of conversion loss from 5.3-6.05GHz and >10dB of return loss at f_{center} . A DC voltage was shown to improve conversion loss for lower LO power levels, but not to an acceptable range. With plenty of room left on the chip, additional parts could be added for better impedance matching and higher-order filters (HPF for RF/LO and LPF for IF) for suppression of RF, LO and nearby mixing products.