

JHU EE787 Fall 2008 MMIC Results
JHU MMIC Design EE787
Prof. John Penn and Dr. Michel Reece

Designs Fabricated by TriQuint Semiconductor

MWO Support by Gary Wray and Scott Maynard

**TriQuint TQPED Library, and MWO
software used for student designs**

Eight MMICs were designed by students for the Fall 2008 JHU MMIC Design. The intent was to design low DC power consumption components (i.e. Battery powered) for use with the S-band or C-band wireless communications service (WCS) or industrial, scientific, and medical (ISM) frequencies. All designs were tested in the late Spring of 2009 after fabrication by TriQuint Semiconductor. The MMIC measurements compare favorably to simulations; overall, the designs were very successful. A couple of connection errors cropped up in a few of last year's designs. Two designs from 2007 were corrected and were re-fabricated along with the 2008 designs. All designs used TriQuint's TQPED process with 0.5 um PHEMTs.

Overall, the designs worked well and are documented following. With the high gain of the PHEMT devices, stability can be difficult especially at low frequency. The Power Amplifier by David Durachka was a little low in gain during the NWA measurements but when measured with a signal generator and spectrum analyzer the gain matched simulations after adding some additional capacitance on the gate supply to quell a low frequency problem. Another low noise amplifier showed some stability issues at a higher frequency (~1.76 GHz), so its s-parameters were only measured at a lower DC bias and gain point. Generally small signal parameters were close to simulations for all designs. Output powers tended to be a couple dB below predictions for the amplifier designs.

Thanks again to TriQuint, and Applied Wave Research for their wonderful support of the JHU EE787 MMIC Design Course.

**Fall 2008 JHU EE787 MMIC Design Student Projects
Supported by TriQuint, and Applied Wave Research
Professors John Penn and Dr. Michel Reece**

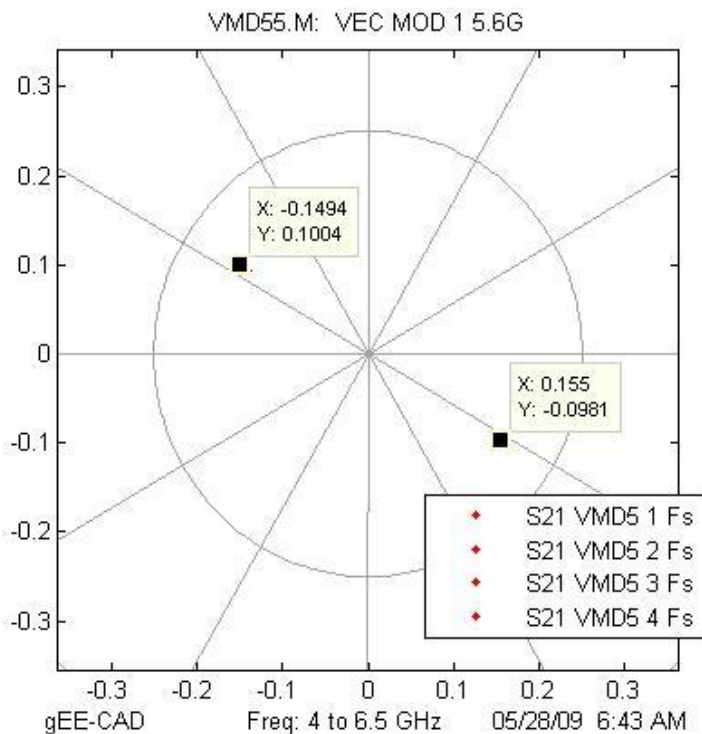
Medium Power Amplifier—Matt Crowne
Phase Shifter C-band – Mitesh Patel
Mixer S-Band – Brendan McElrone
Power Amplifier C-band – Ben Brawley

Low Noise Amplifier – Minhaj Raza
Small Signal Amplifier – Tom Pierce
Power Amplifier C-band – D. Durachka
Volt. Cont. Osc. C-band – Kang Yuan

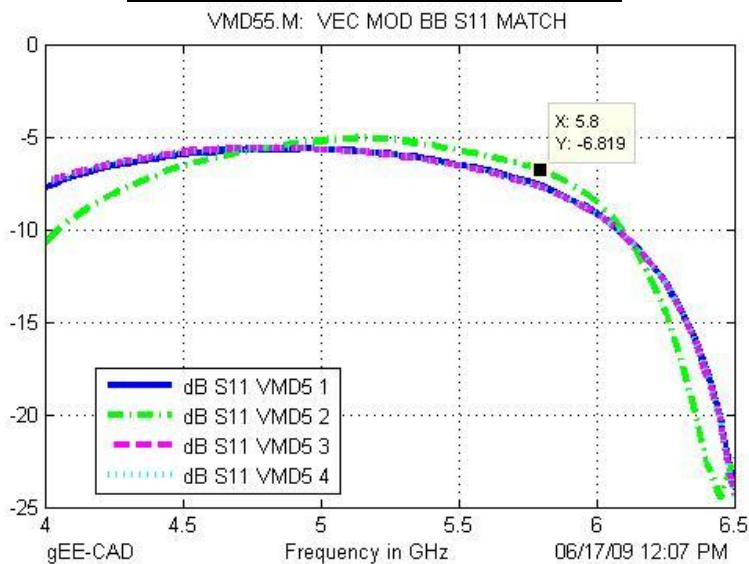


Shawn Seman – Vector Modulator

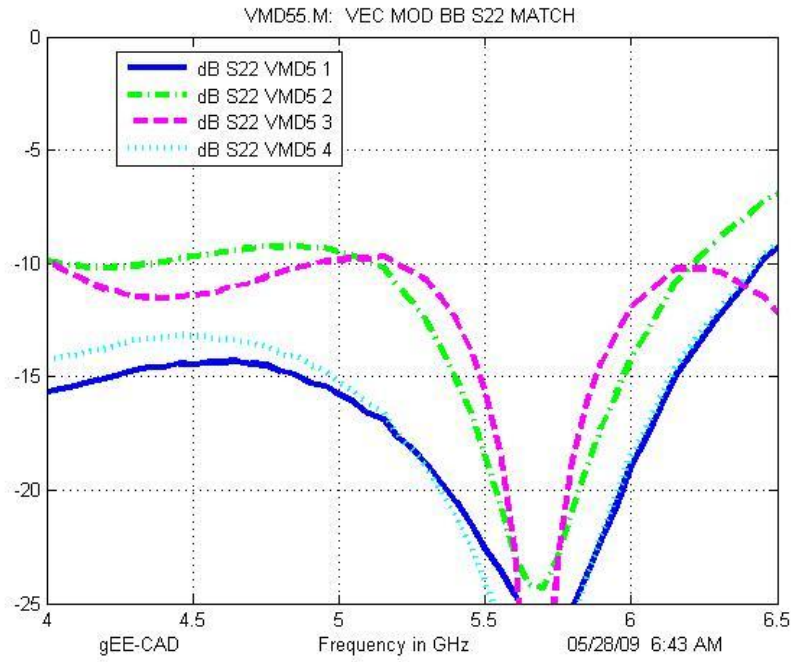
A C-Band Vector Modulator was designed for the 5150 to 5350 MHz WLAN and 5725 to 5875 MHz ISM bands. During testing, a mistake in the layout was discovered. The PHEMT in the “I” attenuator closest to the large capacitor in the upper right of the plot, does not have a ground connection. The original layout had a metal0 line from the PHEMT to the substrate via next to it, but it appears that in massaging the layout, the trace must have been deleted inadvertently. It even passed the LVS checks because of the way substrate vias are handled. After re-running LVS with a labeled substrate via, the LVS software notes that the via labeled “P6” does not have any connections. A corrected design was re-fabbed with the JHU 2008 MMIC Design class fabrication. The RF match seemed reasonable at the two ports. An attempt was made to measure a QPSK pattern at the nominal frequency by applying high and low voltages to the I/Q inputs. The plots shows an approximate 180 degree shift but it appears that possibly only one of the two I/Q inputs was working. Testing should be revisited to see if it was a poor connection on one of the inputs or something with the design.



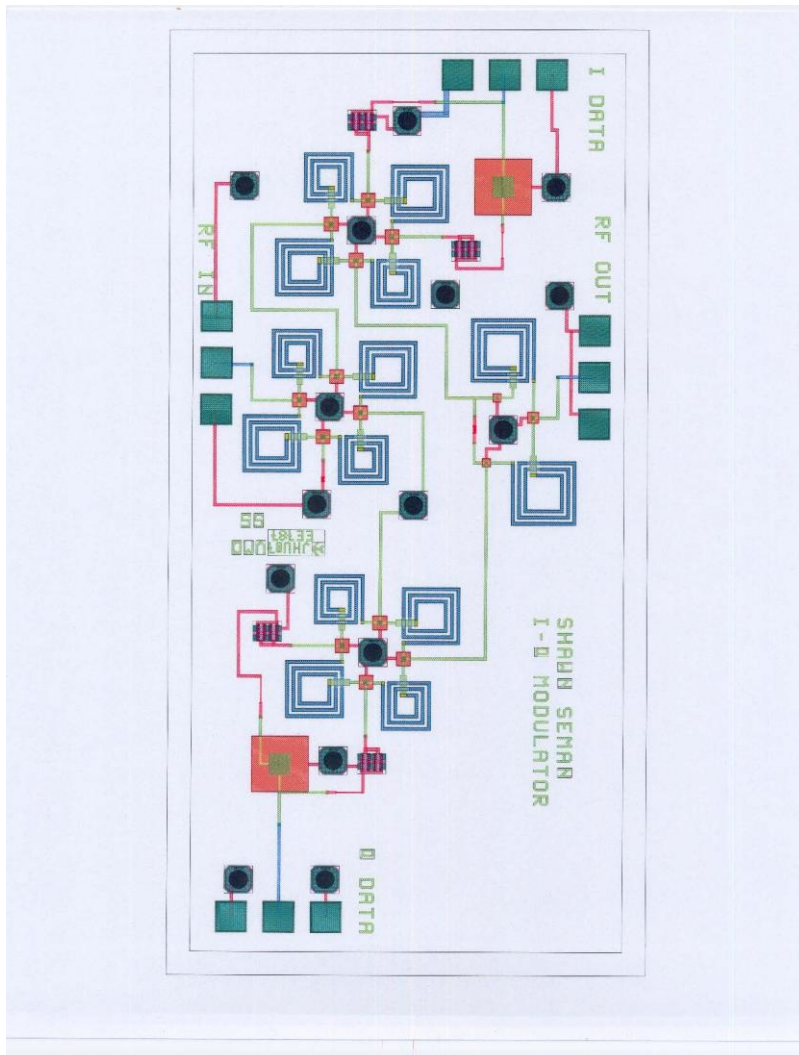
BPSK Pattern Measured at 5.6 GHz



Input Match of Vector Modulator (s11)



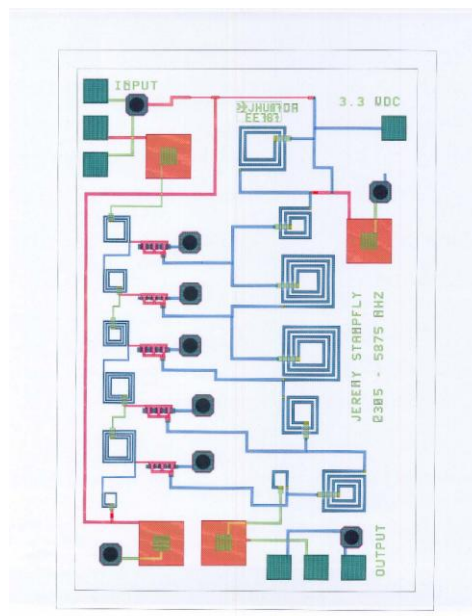
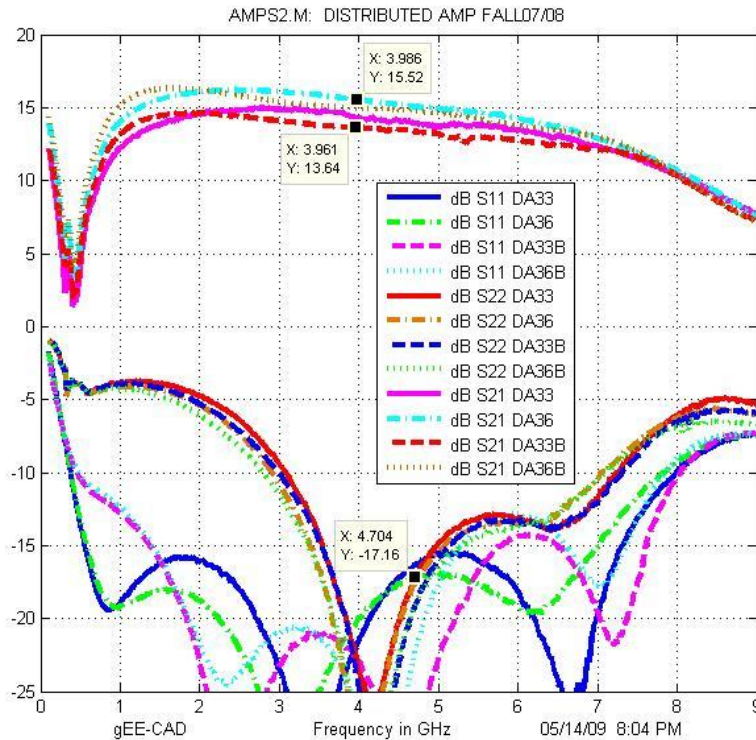
Output Match of Vector Modulator (s22)



Plot of JHU07VMD (Note missing connection at upper right between substrate via and PHEMT):

Distributed Amplifier 2007–Jeremy Stampfly

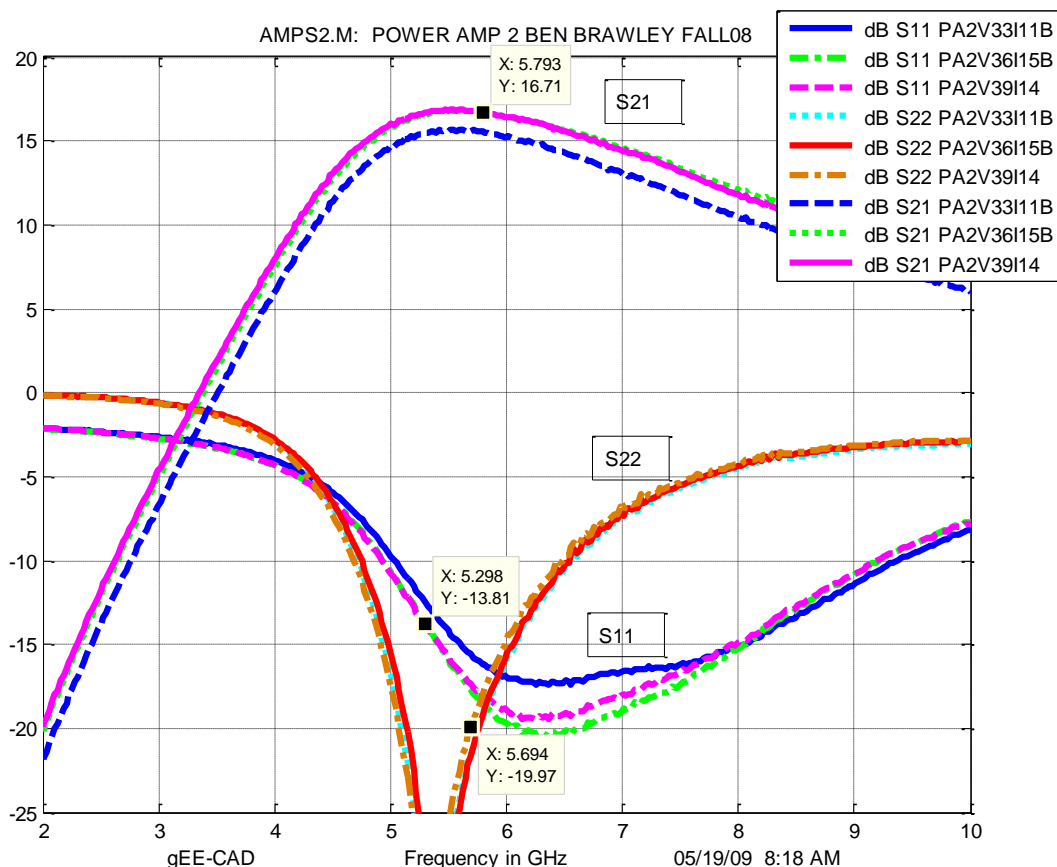
A broadband distributed amplifier was designed in the fall 2007 class to use relatively little DC power. The design was measured to have decent broadband match but the gain was very low. During design checks, the layout did not pass LVS checks, but the error message implied a problem in the gate transmission line. The actual layout gate line was simulated with Sonnet to verify that there were no errors. Given the actual performance, another look discovered the missing connection and it was on the other side of the chip at the drain transmission line. A metal2 connection to the last PHEMT device did not have a via2 layer to connect it to metal1. There was a via1 layer connecting down to metal0, rather than up to metal2. Re-simulations with ADS after removing the one connection compared favorably to last year's measured data. The corrected design was re-fabbed with the 2008 MMIC Design class and it worked as simulated! Data was measured at 3.3V (~18 mA) and 3.6V (~25 mA) with the current closer to simulations at the higher bias voltage. S-parameters plotted for two die shown below are nearly identical.



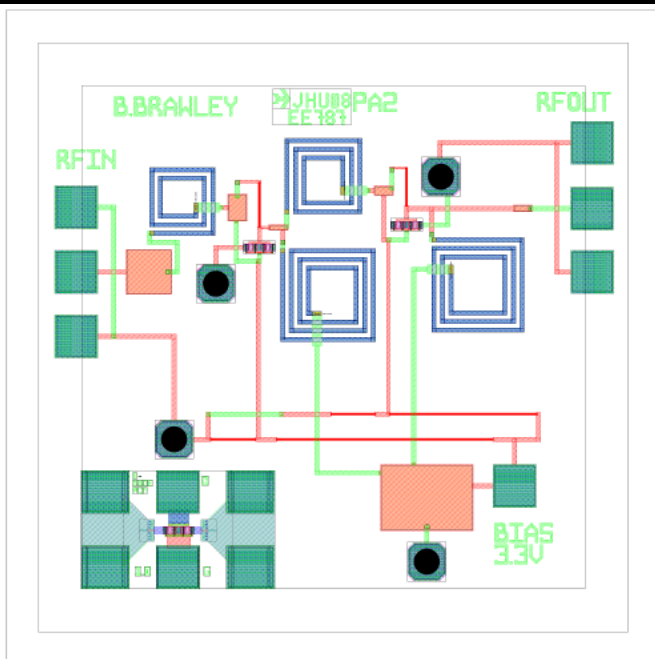
Plot of DA Layout:

Ben Brawley – Power Amp

A C-Band Power Amplifier was designed for the 5150 to 5350 MHz WLAN and 5725 to 5875 MHz ISM bands. The design was intended for lower battery power consumption with good efficiency. Two die were measured at 3.3V, 3.6V, and 3.9V for the first die. Gain was a little better with the second die and bias current was a little higher and closer to the expected value. Shown are plots of measured data which corresponds well with the original simulations.



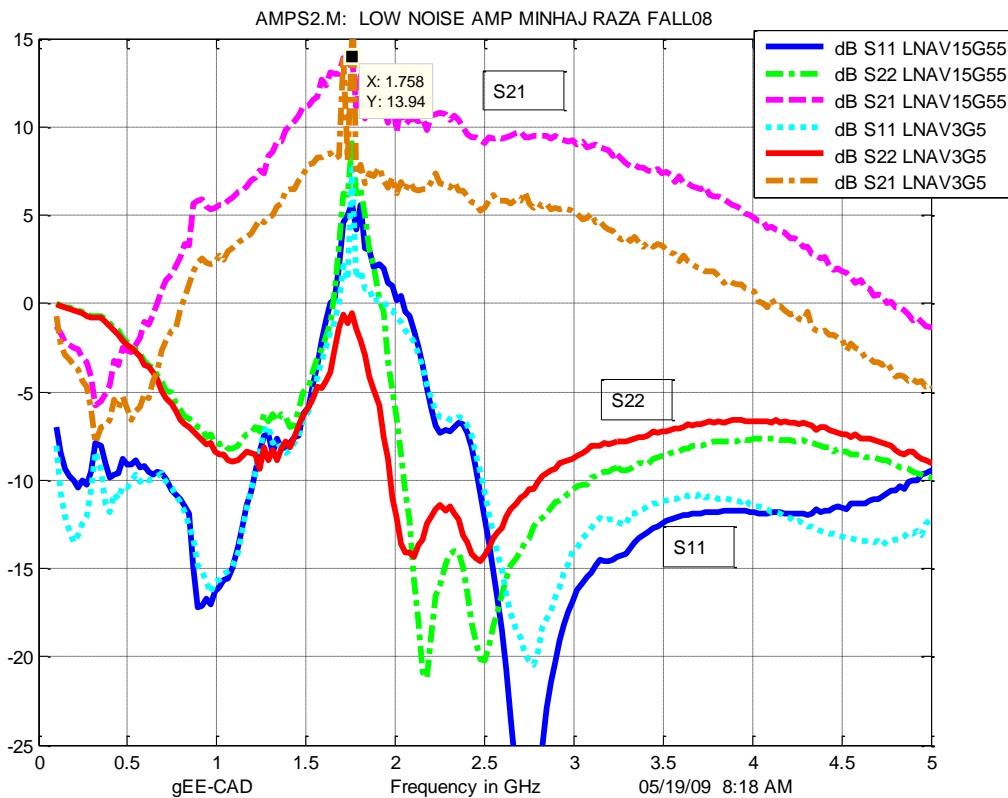
Measured Power Amp 2 at 3.3V 11 mA, 3.6V 15 mA, and another die at 3.9V 14 mA.



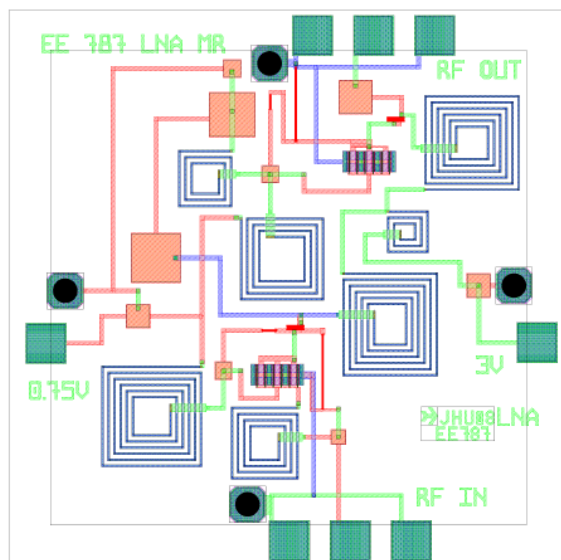
Plot of Power Amp 2

Minhaj Raza – Low Noise Amp

A Broad Band Low Noise Amplifier was designed for approximately 1 to 3 GHz. The design used two stages for high gain and feedback to get good bandwidth. Gain was expected to be around 30 dB which is somewhat aggressive for a two stage and may have resulted in some stability issues around 1.76 GHz. Data was measured at a lower DC bias before the design broke into full oscillations ($s_{21} > 12$ dB). The plot shows an S_{11}/S_{22} that is nearly positive with a 3.0V 9-10 mA bias ($V_{GS} = +0.50V$), but at another bias (1.5V 9mA, $V_{GS} = +0.55V$), S_{11}/S_{22} are very positive and there is a large gain spike. There is measured data for some PHEMTs from this fabrication, possibly a resimulation with measured data may show a stability problem that was not show in the original “nominal” model simulations.



Measured Low Noise Amp showing stability issues mid-band (~1.76GHz)



Plot of Low Noise Amp

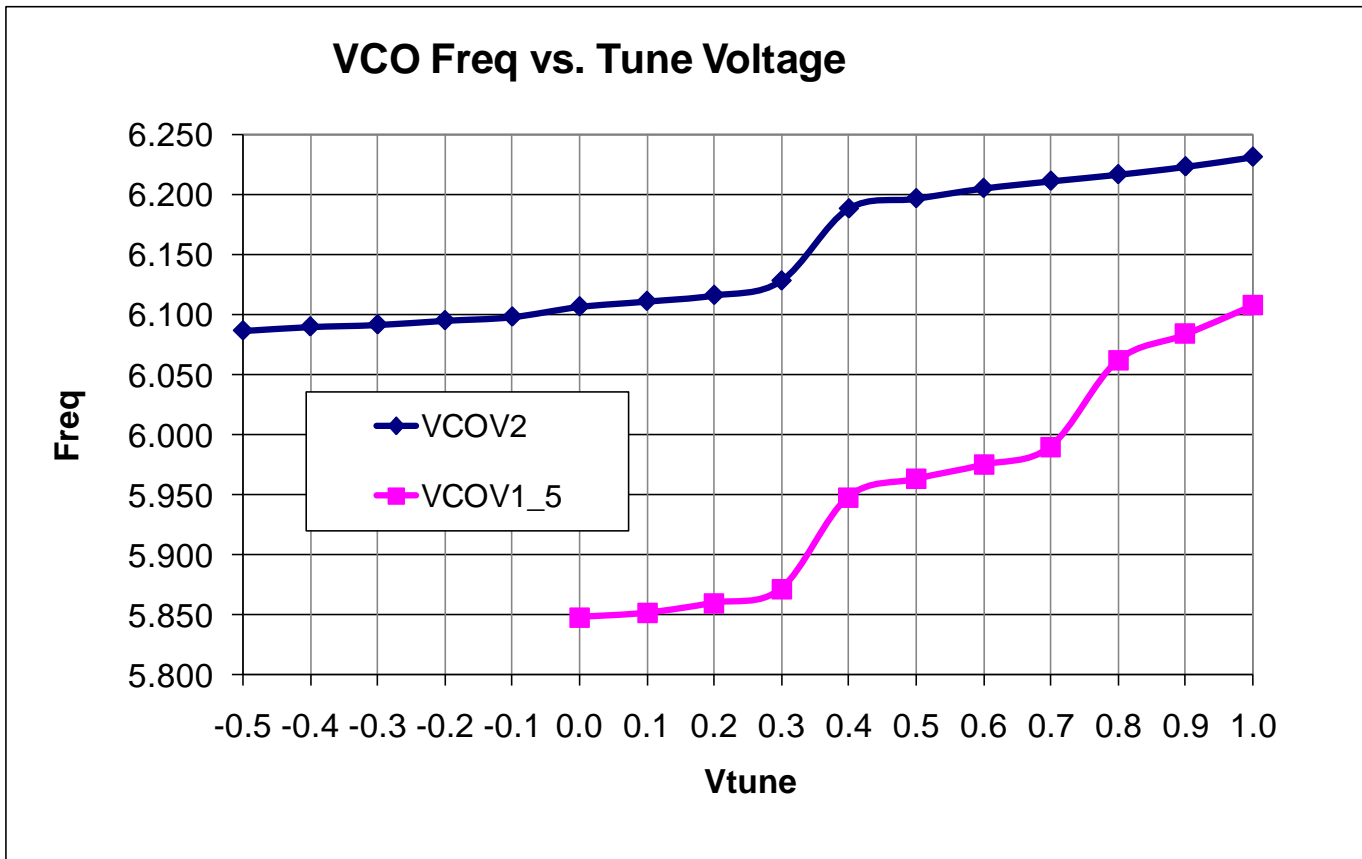
Kang Yuan – Voltage Controlled Oscillator

A C-Band Voltage Controlled Oscillator was designed for about 5.8 GHz nominal. The oscillator worked well but was slightly high in frequency at the nominal 2V bias, so an additional bias at 1.5V was measured which was quite close to the desired 5.8 GHz. Tuning range was good with the varactor varied from -0.5V to +1.0V. Only positive voltages on the varactor were measured for the 1.5V case but presumably the negative varactor settings would have provided a little more tuning range below 5.85 GHz. Output power was nominally 6.5 dBm at the 2V 16 mA bias (~1.5 dB cable/probe loss) and about 4.33 dBm at the 1.5V 15 mA bias.

MWO VCC 2V at 15mA		Die #2	
VBias (V)	Freq (GHz)	Pout(ms)	Pout(corr)
-0.5	6.087	5.0	6.5
-0.4	6.090	5.0	6.5
-0.3	6.092	5.0	6.5
-0.2	6.095	5.0	6.5
-0.1	6.098	5.0	6.5
0.0	6.107	5.0	6.5
0.1	6.111	5.0	6.5
0.2	6.116	5.0	6.5
0.3	6.128	5.0	6.5
0.4	6.188	5.0	6.5
0.5	6.197	5.0	6.5
0.6	6.205	5.0	6.5
0.7	6.211	5.0	6.5
0.8	6.217	5.0	6.5
0.9	6.223	5.0	6.5
1.0	6.231	5.0	6.5

Pout measured ~-2.83 dbm

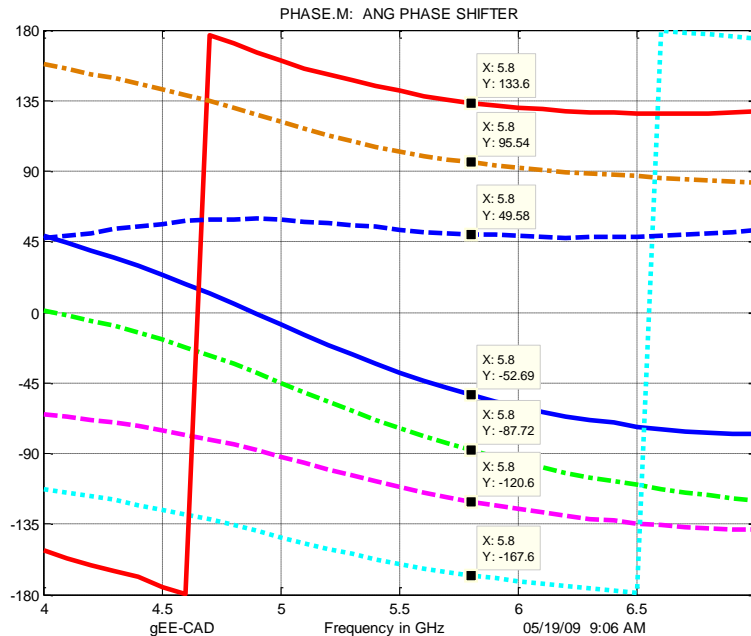
ADS VCO 1.5V at 18mA			Die #2
VBias (V)	Freq (GHz)	Pout(ms)	Pout(corr)
0.0	5.848	2.8	4.3
0.1	5.852	2.8	4.3
0.2	5.860	2.8	4.3
0.3	5.872	2.8	4.3
0.4	5.948	2.8	4.3
0.5	5.963	2.8	4.3
0.6	5.975	2.8	4.3
0.7	5.990	2.8	4.3
0.8	6.062	2.8	4.3
0.9	6.083	2.8	4.3
1.0	6.107	2.8	4.3



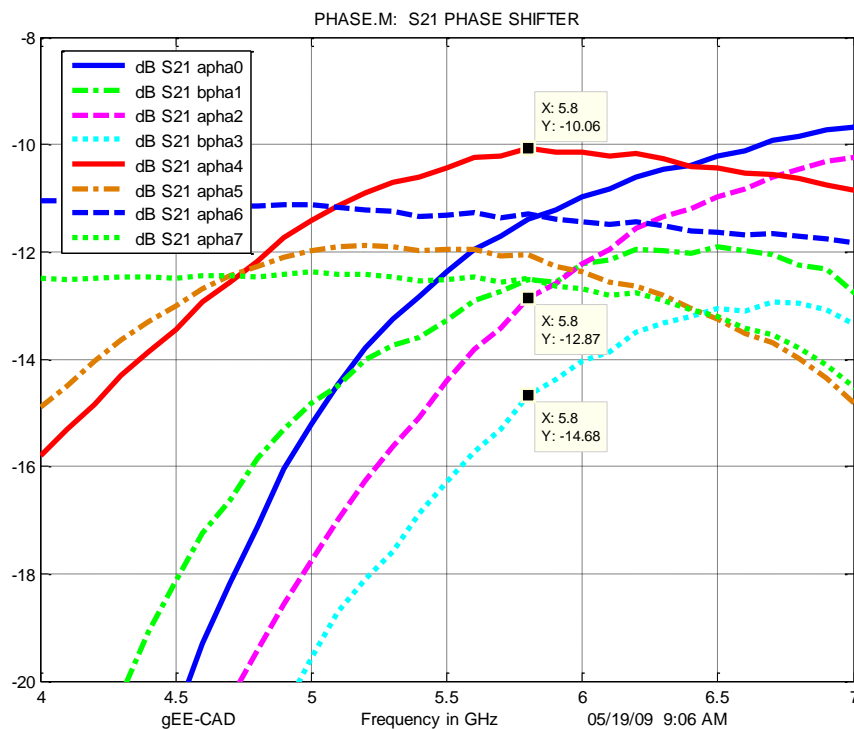
Measured VCO – Frequency vs. Tuning Voltage at 2V and 1.5V bias

Mitesh Patel – 3-bit Phase Shifter

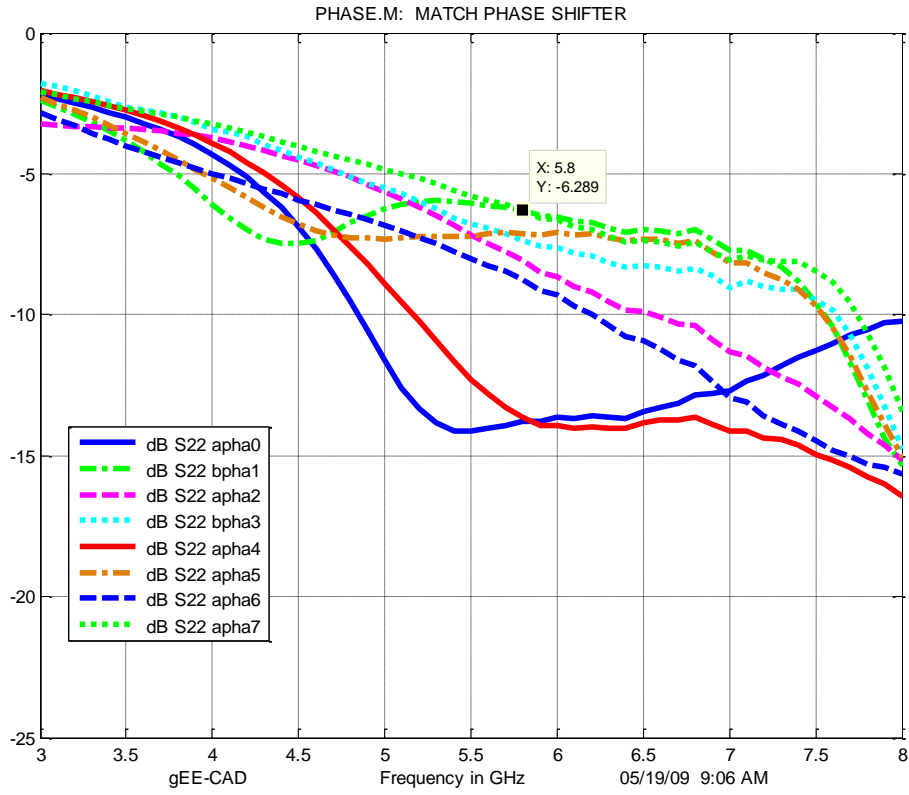
A C-Band 3-bit phase shifter was designed for the 5150 to 5350 MHz WLAN and 5725 to 5875 MHz ISM bands. Since the PHEMT switches use virtually zero DC power, the phase shifter is extremely low in power consumption. Measurements of the 8 phase states were taken and retaken at a couple of points where it appeared that the DC or RF probes were not making a good contact and were indicating higher losses than it should have. Attached is a plot of the measured data. The 45, 90 and 180 bits were pretty close to the expected phase shifts.



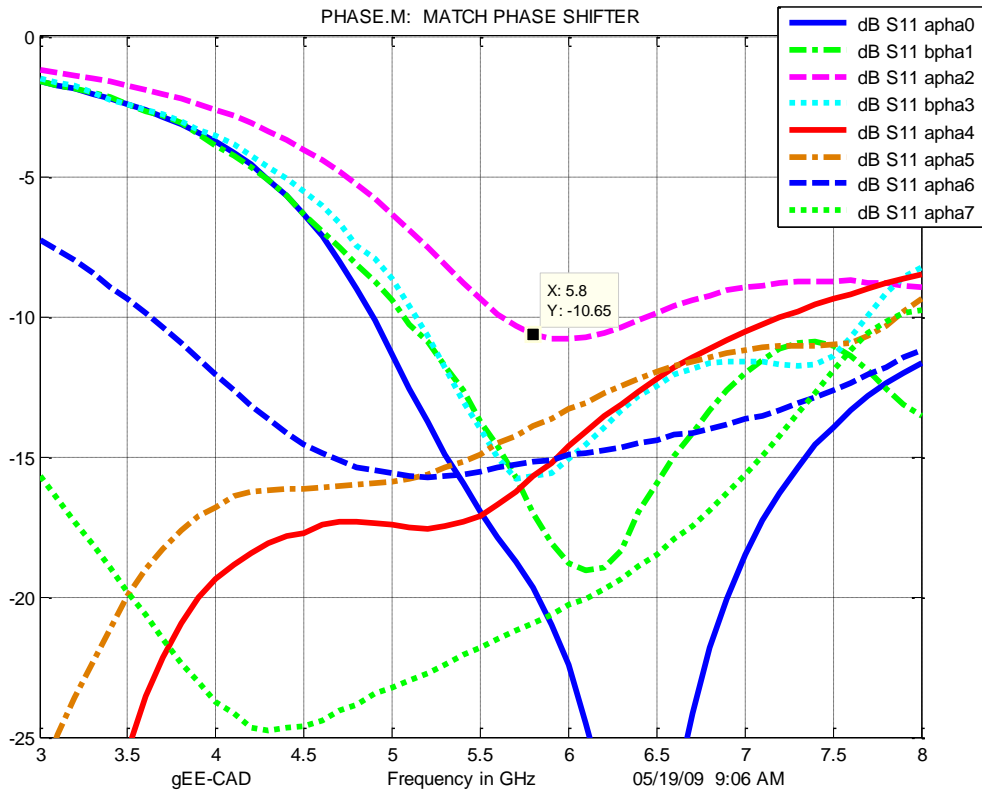
Measured States of Phase Shifter



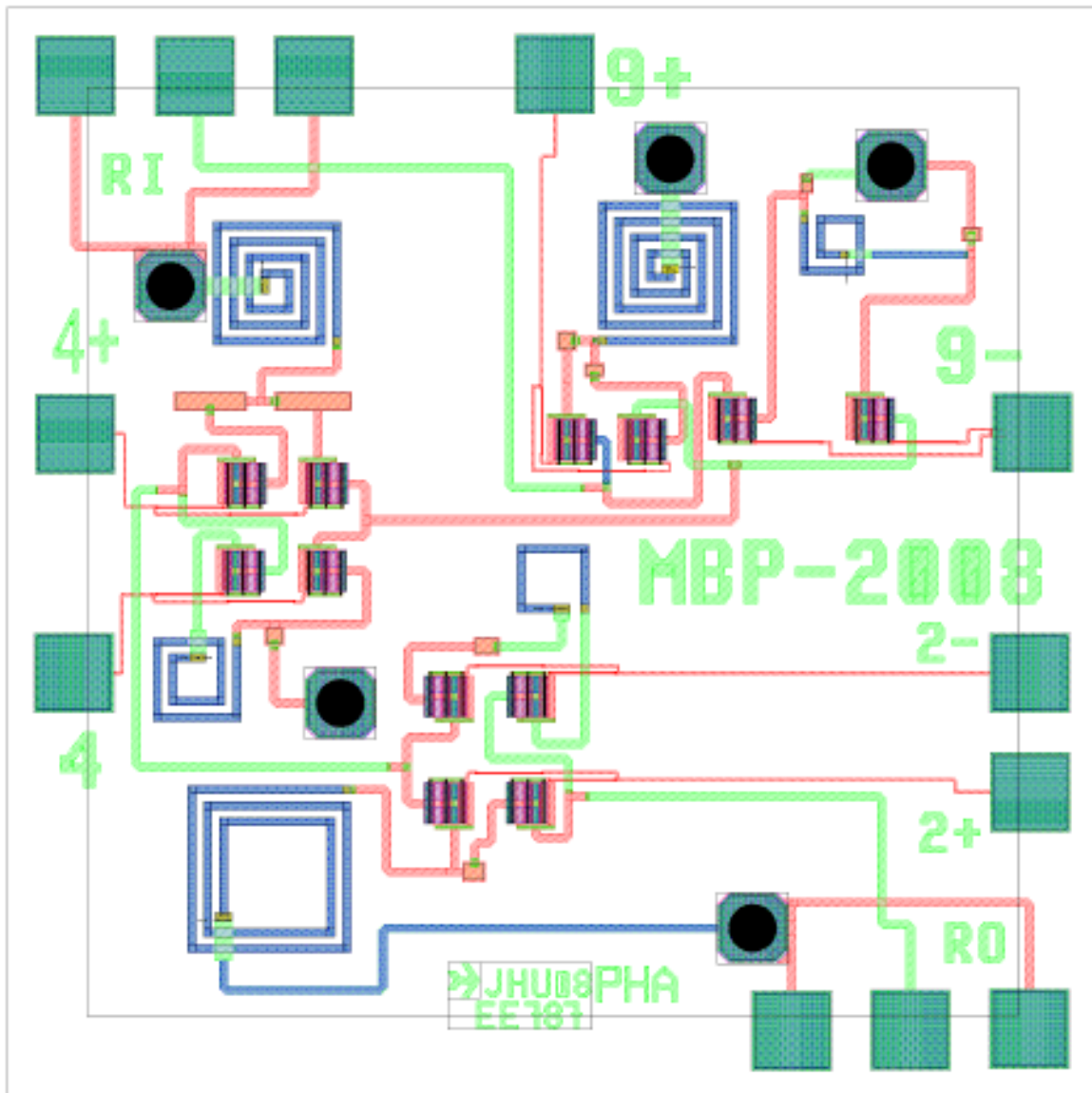
Measured Insertion Loss of Phase Shifter (all states)



Measured Output Return Loss (S22) of Phase Shifter (all states)



Measured Input Return Loss (S11) of Phase Shifter (all states)

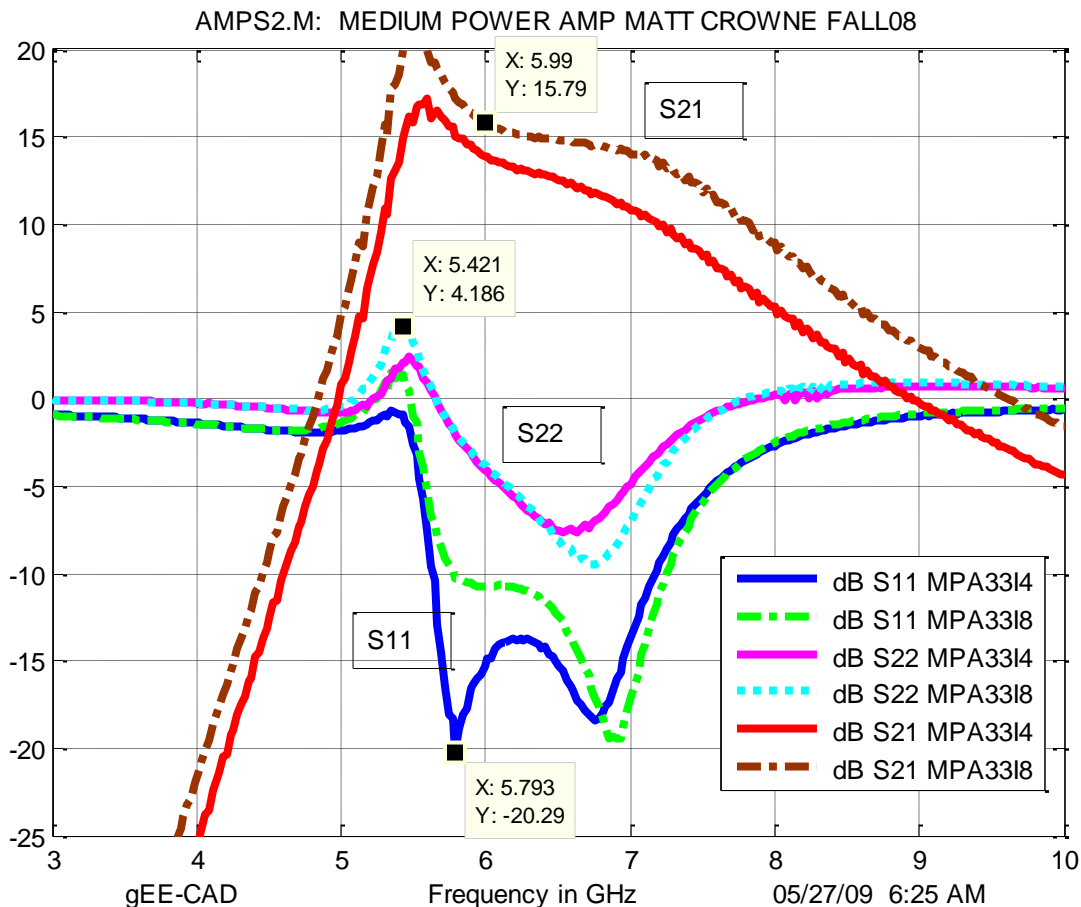


Plot of 3-bit Phase Shifter

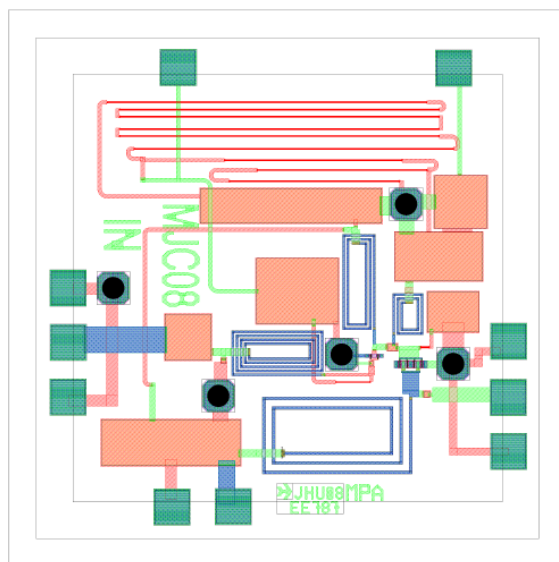
Phase Shifter						
2+	2-	4+	4-	9+	9-	
0	-2V	0	-2V	0	-2V	PHA0
-2V	0	0	-2V	0	-2V	PHA1
0	-2V	-2V	0	0	-2V	PHA2
-2V	0	-2V	0	0	-2V	PHA3
0	-2V	0	-2V	-2V	0	PHA4
-2V	0	0	-2V	-2V	0	PHA5
0	-2V	-2V	0	-2V	0	PHA6
-2V	0	-2V	0	-2V	0	PHA7

Matt Crowne – Medium Power Amp

A C Band Medium Power Amplifier was designed for approximately 5 to 6 GHz. The design used two stages for high gain with good bandwidth. The Emode PHEMTs were biased at about 0.6V and 0.7V VGS with 4-5 mA and 8-9 mA of bias with 3.3V Vdd supply. There appears to be a marginal stability problem near 5.4 GHz as seen in the plots. At the higher gain/DC bias points, both S11 and S22 are starting to go positive with a 50 ohm load. The match does show a nice broadband response. Possibly a small tweak to the design could bring the passband down to the desired range and improve the stability.



Measured Gain and Return Loss of Medium Power Amplifier (3.3V 4/8mA)



Layout of Medium Power Amplifier

Brendan McElrone – Mixer S-Band

A lumped element rat race hybrid is used to create an up/down passive diode mixer at S-band. The IF is intended to be about 100 MHz with an RF between 2.3 to 2.5 GHz and an LO from 2.2 to 2.6 GHz. Conversion loss was measured to be about 12 dB for down conversion with a 2.4 GHz LO and RF at 2.3 and 2.5 GHz for a 100 MHz IF. Conversion loss was higher without forward biasing the diodes (~0.6V at 2 mA), as expected, also the forward bias made the conversion loss less sensitive to LO power levels. An LO power of about +7 dBm was optimal for best conversion loss. The mixer was measured as an up and a down converter. Changing the IF frequency from 10 Mhz to a few hundred MHz seemed to have about the same conversion loss.

6/4/09 Re-measured IF Loss ~0.2dB at 100 mHz; RF loss ~0.75 dB at 2.4 GHz; LO loss 1.65 dB
 2.4GHz RF -10 dBm, 2.3 GHz LO IF =100MHz with bias _0.6V ~2mA

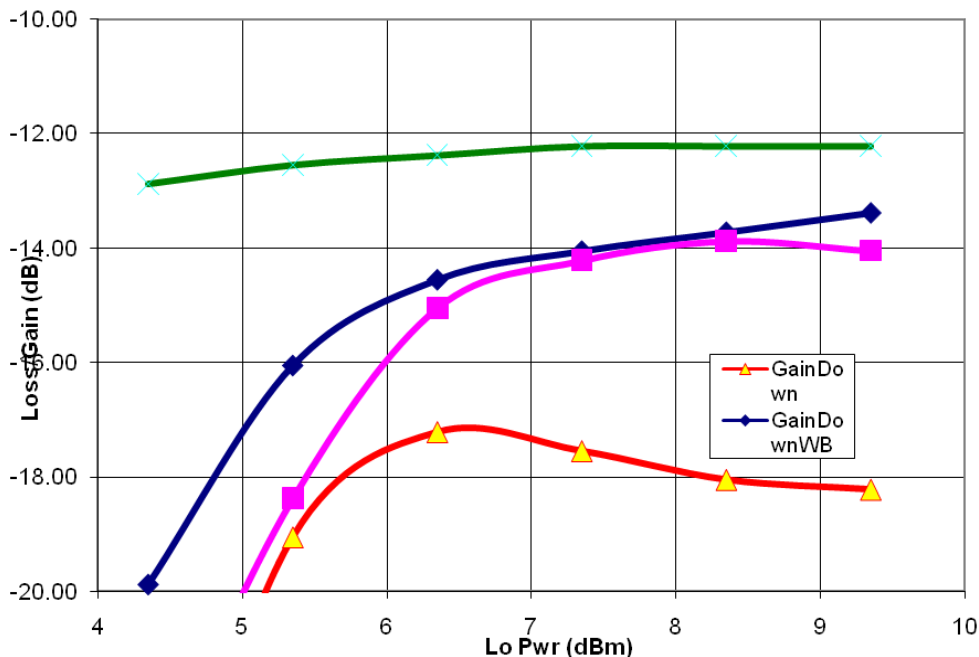
LO	IF	LOIso/corr	RFIso/Loss
7	-28.00	-3.67	-26
LO	IF	LO(corr)	ConvLoss
6	-36.67	4.35	-25.72
7	-30.00	5.35	-19.05
8	-28.17	6.35	-17.22
9	-28.50	7.35	-17.55
10	-29.00	8.35	-18.05
11	-29.17	9.35	-18.22

<u>Down Conversion</u>	
IF(w/bias)	ConvLoss
-30.83	-19.88
-27.00	-16.05
-25.50	-14.55
-25.00	-14.05
-24.67	-13.72
-24.33	-13.38

LO	IF	LOIso/corr	RFIso/Loss
8	-26.50	-5	-28.5
LO	IF	LO(corr)	ConvLoss
6	-34.50	4.35	-23.55
7	-29.33	5.35	-18.38
8	-26.00	6.35	-15.05
9	-25.17	7.35	-14.22
10	-24.83	8.35	-13.88
11	-25.00	9.35	-14.05

<u>Up Conversion</u>	
IF(w/bias)	ConvLoss
-23.83	-12.88
-23.50	-12.55
-23.33	-12.38
-23.17	-12.22
-23.17	-12.22
-23.17	-12.22

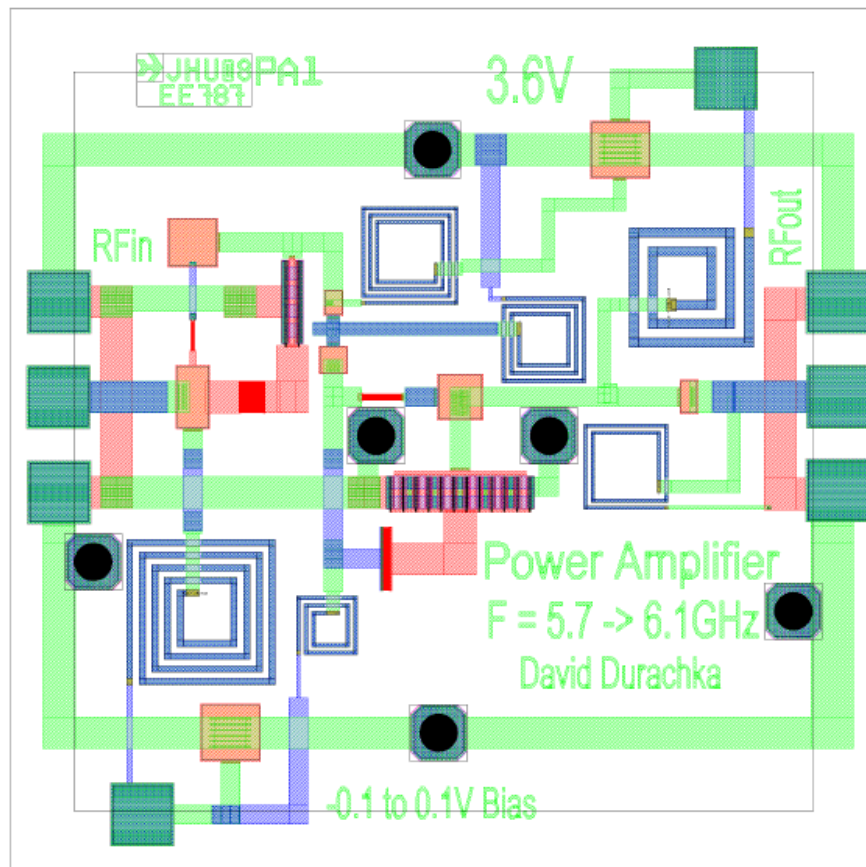
jhu08mix Loss vs. LO Power



Conversion Loss Up/Down Mixer with and without 0.6V Forward Bias on Diodes

David Durachka – Power Amplifier C-band

A C Band Medium Power Amplifier was designed for approximately 5 to 6 GHz. The design used two stages for high gain with good bandwidth and a goal of 20 dbm (100 mW) output power. This amplifier used Dmode PHEMTs for a 3.6V “battery” supply and about -0.1 to +0.1V Vgs on the gate. The gate could be biased at 0V to avoid requiring a negative supply for the -0.1V gate supply. There were some low frequency problems probing the Power Amp design so the gain in the small signal network analyzer measurements is a bit lower than it should be. Measurements of power out vs. power in using a signal generator and spectrum analyzer showed some low frequency oscillations which were quelled with an extra capacitor on the gate supply. Gain was very close to simulations and the current bias was much closer to expected. Power out, and efficiency were good as shown following.



Layout of C-Band Power Amplifier

D Mode Power Amps--5.8 GHz at 3.6 V

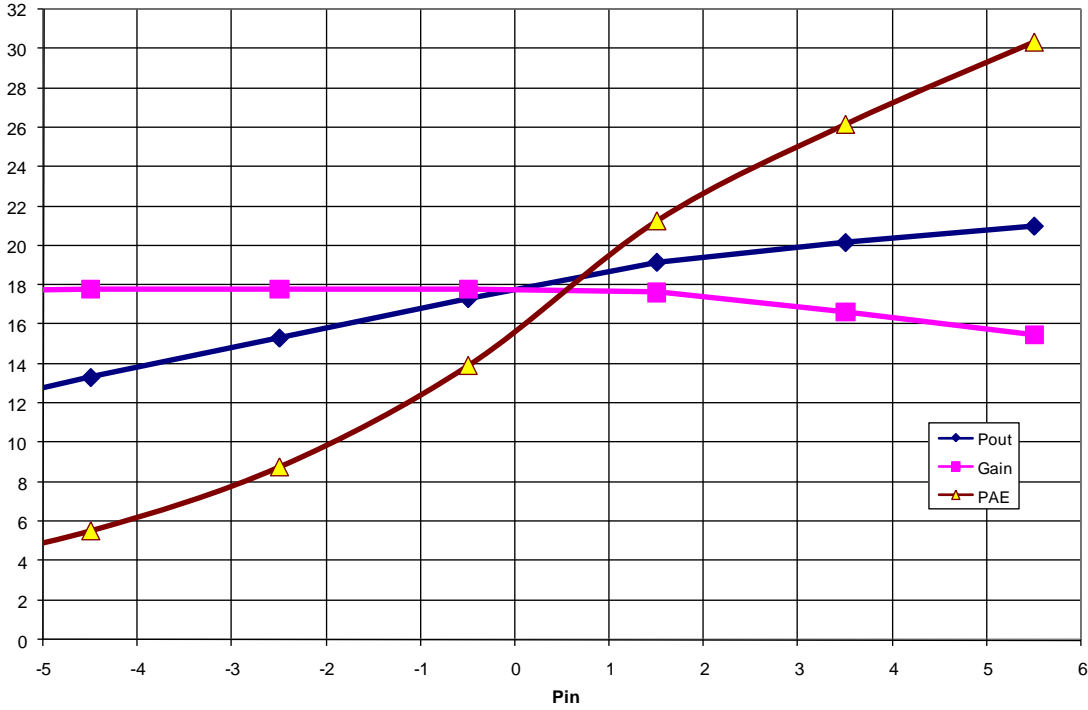
Stability issues at low frequency, OK during Pout measurement

3.0 dB loss on thru plus 2 dB on extra output cabl

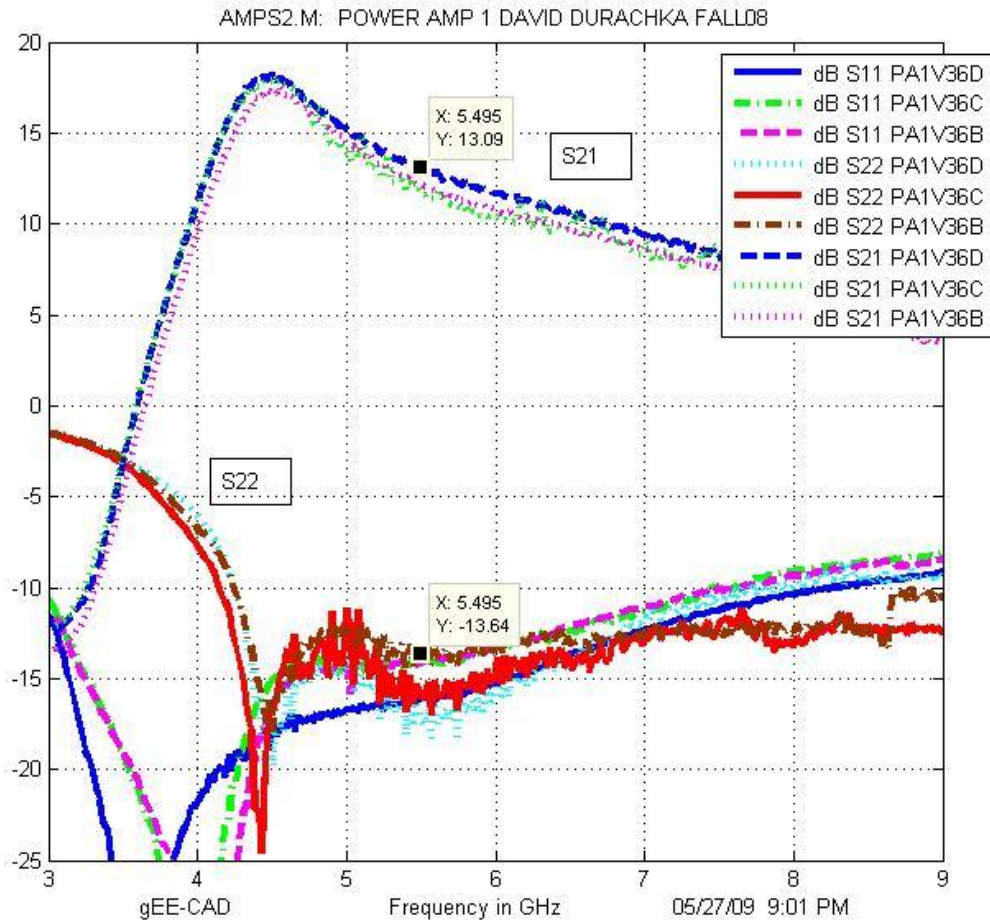
5.8 GHz	Die#1	PA1 GHz	Dmode Fall08	TQPED	vgs=0v	3.6V ; 105 mA				
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(3.6V)	PDC(mw)	Pout(mw)	Drn Eff	PAE	
-5.0	7.67	-6.50	11.17	17.67	105	378.0	13.09	3.5	3.4	
-3.0	9.83	-4.50	13.33	17.83	106	381.6	21.53	5.6	5.5	
-1.0	11.83	-2.50	15.33	17.83	106	381.6	34.12	8.9	8.8	
1.0	13.83	-0.50	17.33	17.83	106	381.6	54.08	14.2	13.9	
3.0	15.67	1.50	19.17	17.67	106	381.6	82.60	21.6	21.3	
5.0	16.67	3.50	20.17	16.67	108	388.8	103.99	26.7	26.2	
7.0	17.50	5.50	21.00	15.50	112	403.2	125.89	31.2	30.3	

Measured Performance of Power Amp

PA1 Meas 08
Dmode 5.8 GHz 3.6V



Plot of Output Power, Power Added Efficiency and Gain for the Power Amplifier



Measured Gain and Return Loss of Power Amplifier (3.6V 30-60 mA)

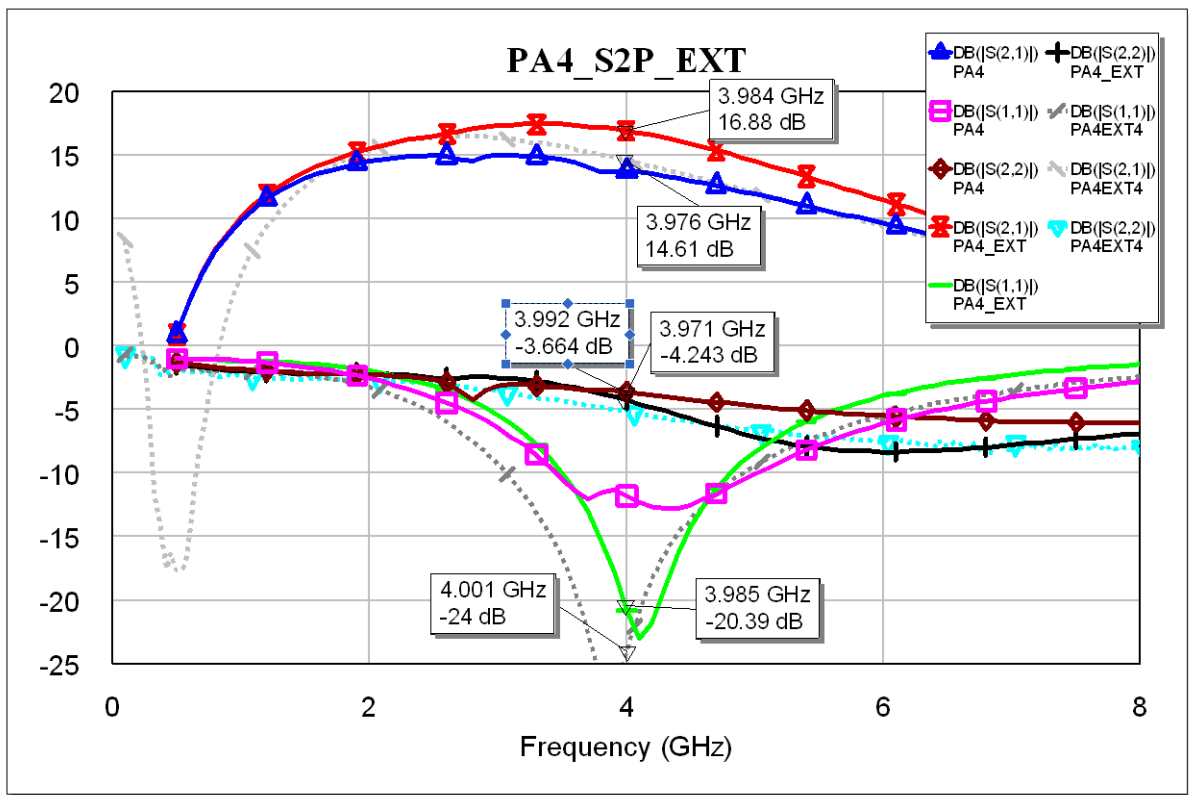
Class Design Examples: Low Noise Amplifier and Power Amplifier (4 GHz) by John Penn

During the course the students are shown a design example of a low noise amplifier and a medium power amplifier at 4 GHz. In previous years, layouts were completed for the LNA and PA design in Agilent’s ADS and later Microwave Office MWO on a single 60 x 60 mil die (54 x 54 after dicing) using TriQuint’s TQTRX MESFET process. In 2005, the LNA and PA examples were re-designed using ADS and TriQuint’s 0.5 um PHEMT (TQPED). Another version of the same LNA was designed in 2008 using Microwave Office (MWO) and it compared nearly identically with the previous ADS design which was refabbed. The same components were used but the layout and interconnect varies slightly.

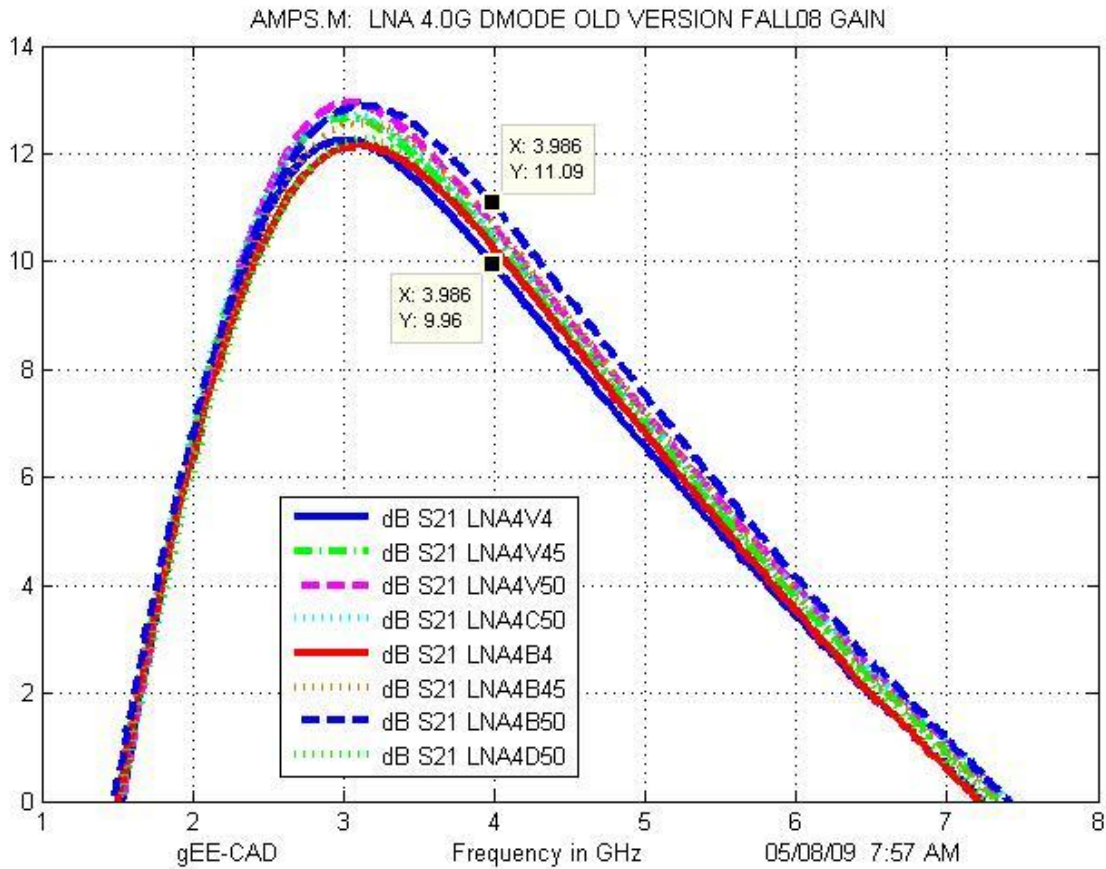
The parasitic extracted layout in MWO matched the measurements well. Attempting to add the interconnect and model it as microstrip did not compare as well. As in past years, output power and efficiency was less than predicted by the Dmode PHEMT model.

The Low Noise Amplifier showed very good agreement between ADS and MWO simulations and measurements. When the Noise Figure meter was used to measure gain and noise figure of the LNA, a through connection was used to subtract out losses for the measurements. There was good agreement between measured and predicted noise figure, though the gain was a little lower than simulated.

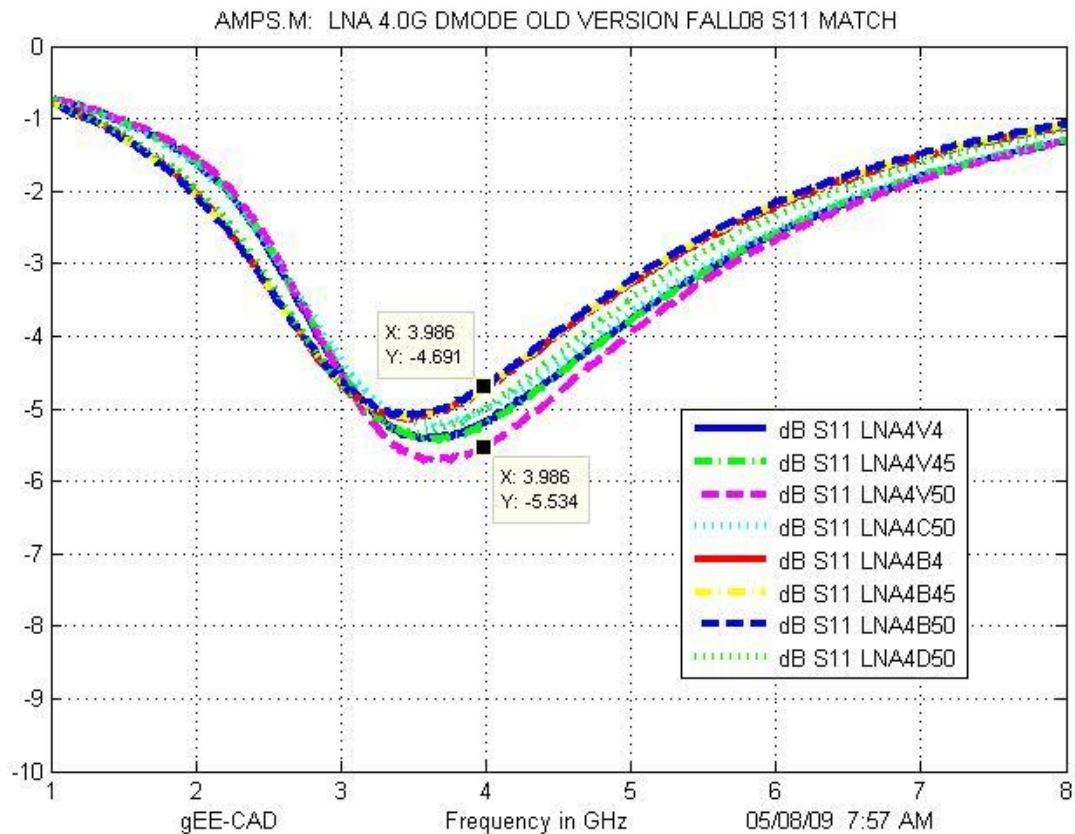
Other test circuits were also designed to be used for future lectures and class examples.



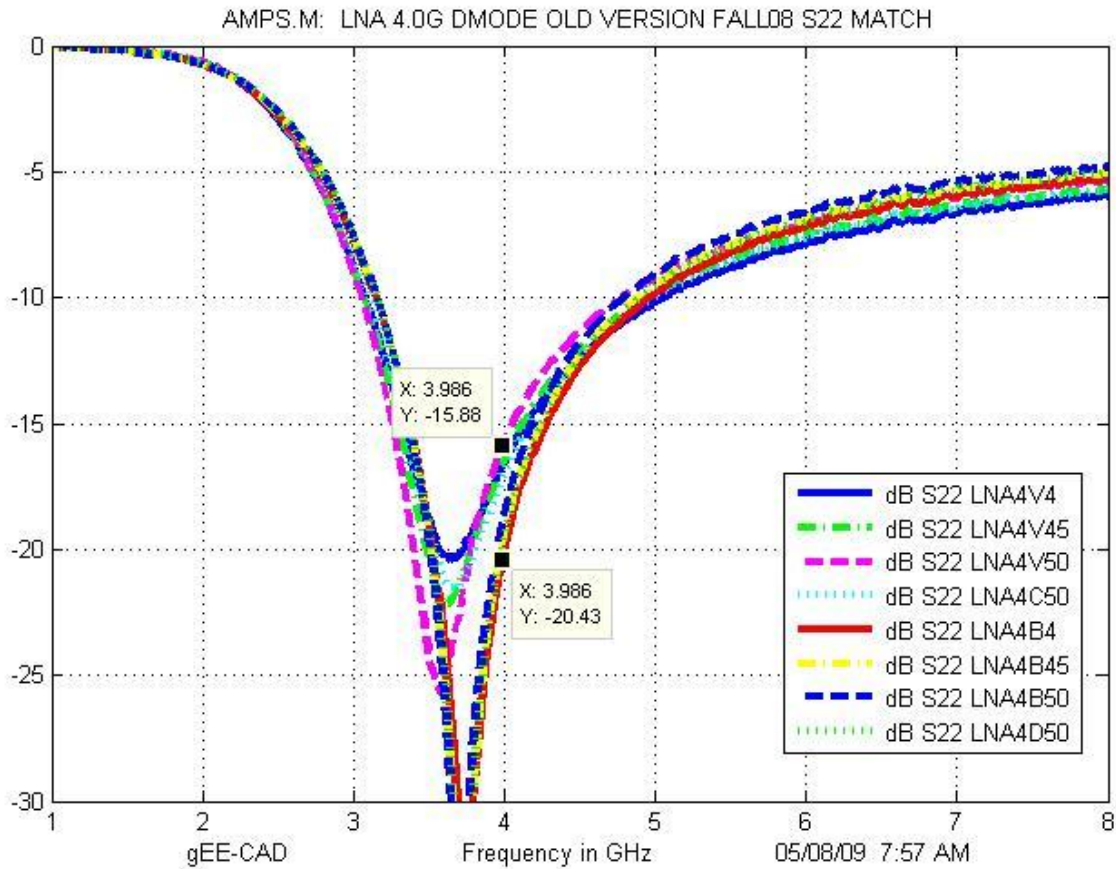
Good Agreement Between Measured and Parasitic Extracted Simulation (MWO) for LNA at 5.0V



Measurements of LNA4 Gain MWO and ADS Layouts (2 die each, 4-5V Vss)

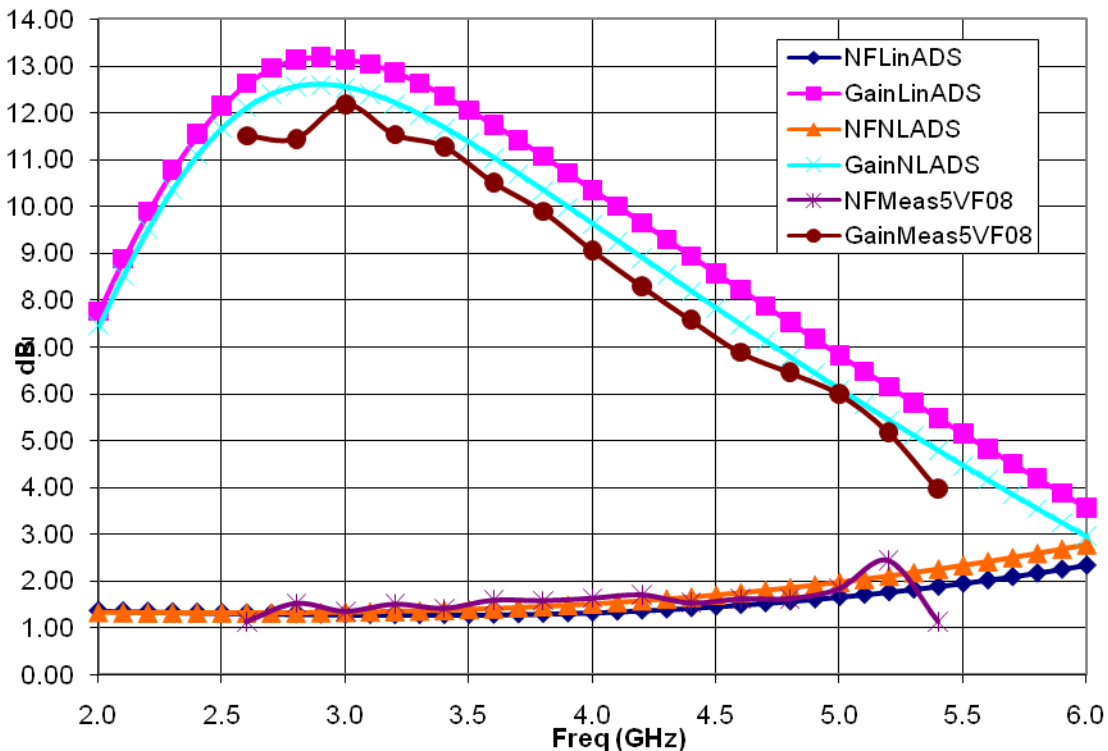


Measurements of LNA4 S11 MWO and ADS Layouts (2 die each, 4-5V Vss)

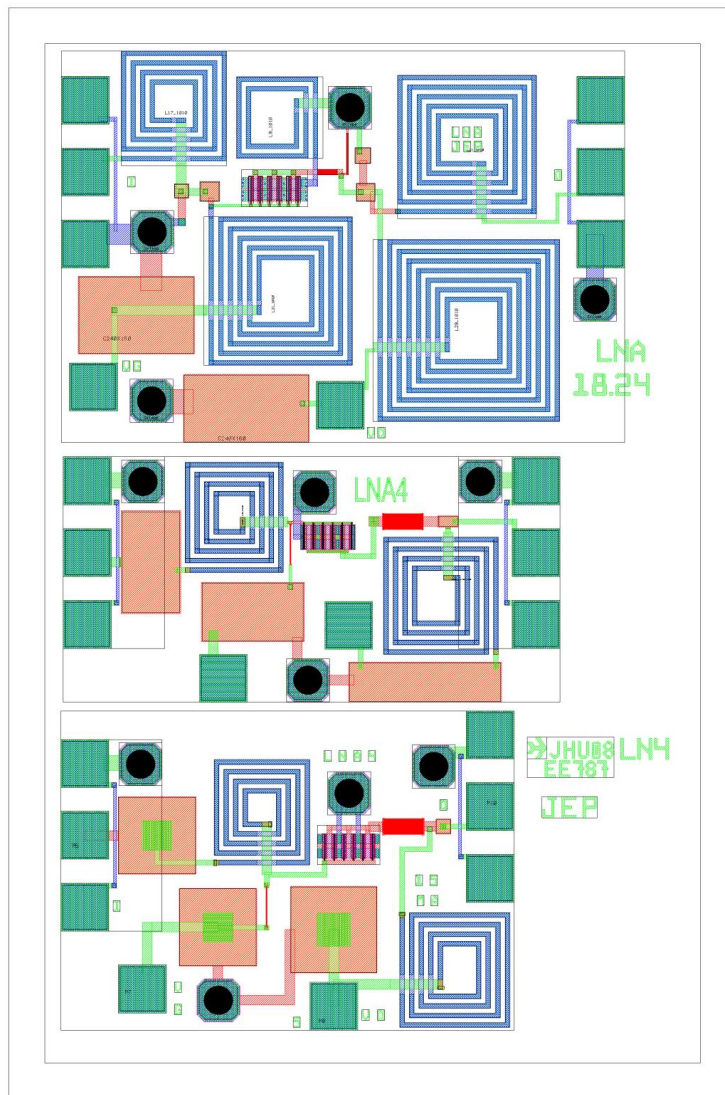


Measurements of LNA4 S22 MWO and ADS Layouts (2 die each, 4-5V Vss)

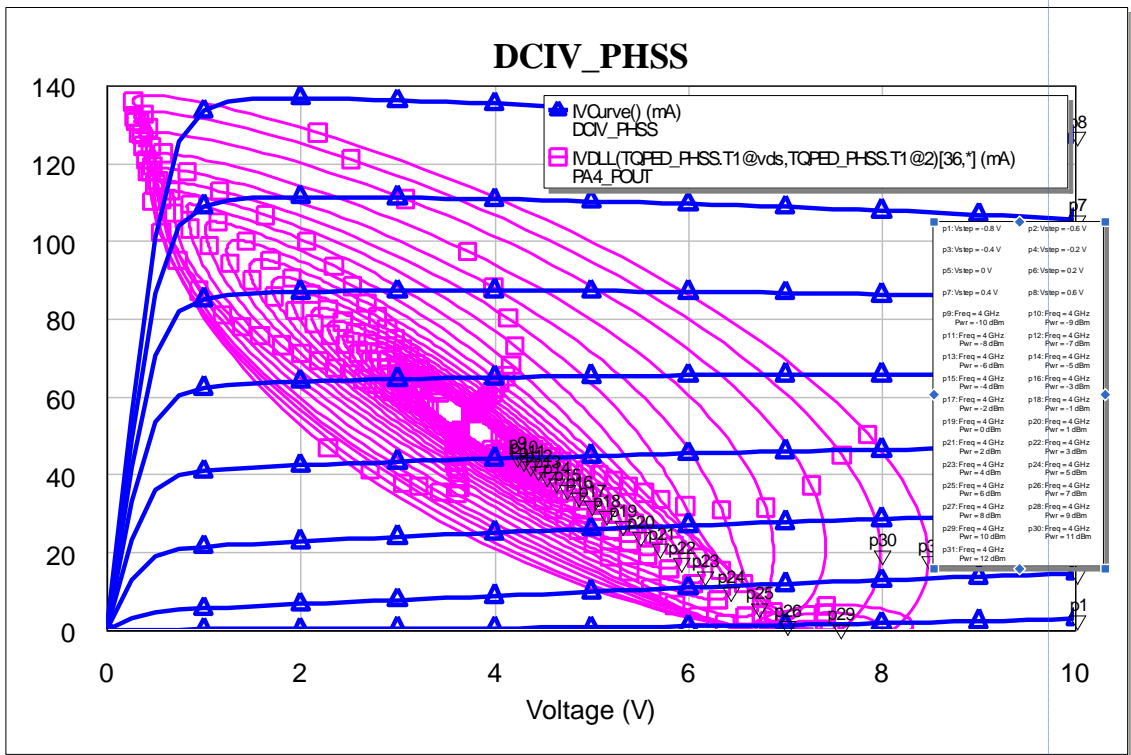
LNA4 Sim vs. Meas -- Corrected with 08 Thru



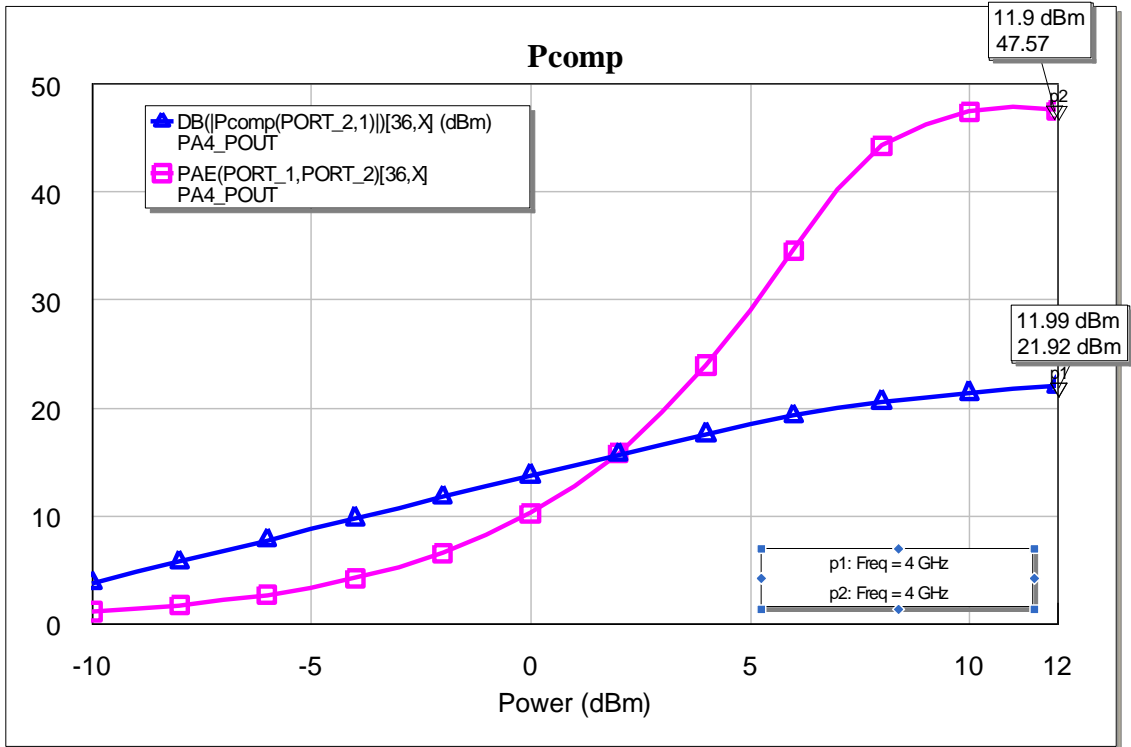
Measured Noise Figure and Gain of LNA4 vs. ADS Simulations



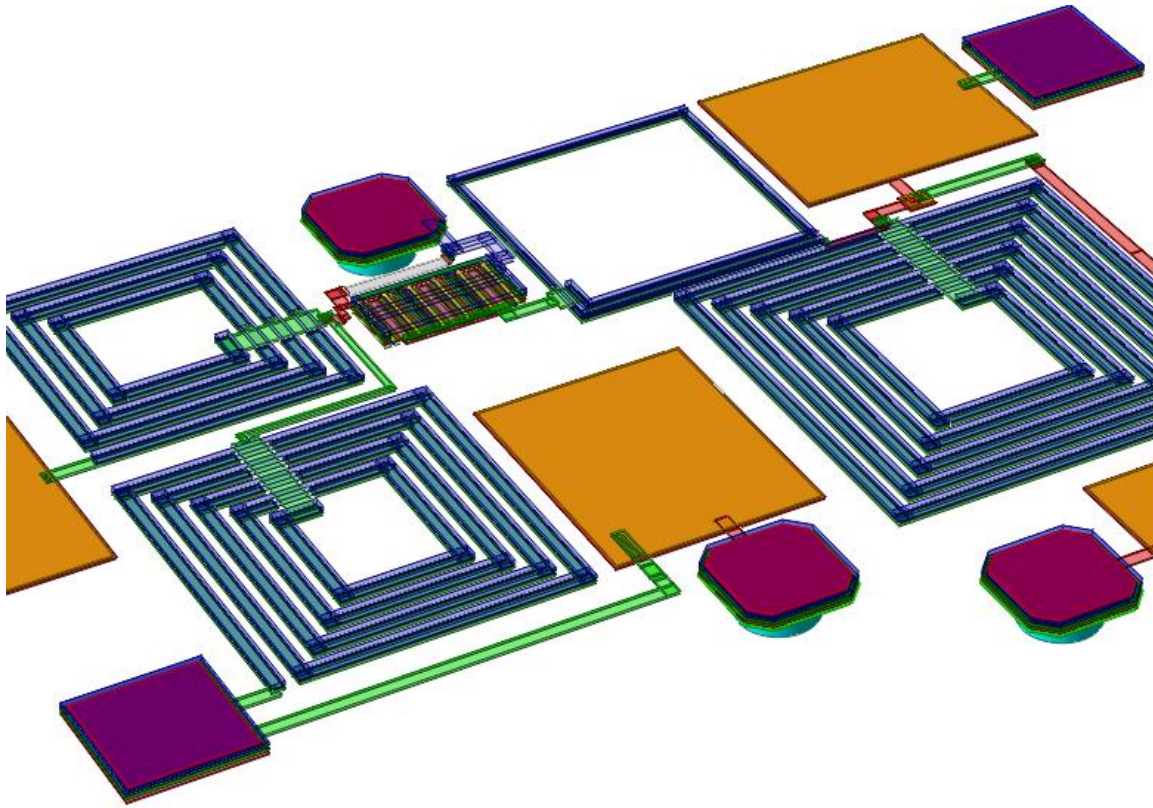
Layout of JHU08LN4: 4 GHz LNA MWO & ADS, plus 1.8-2.4G LNA (54 mil x 84 mil)



Dynamic Load Line Simulation of 4 GHz PA with MWO



Non-Linear Simulation of Pout and PAE for 4 GHz PA with MWO



Layout of 4 GHz LNA with MWO (Extracted Parasitic Simulation)

Performance (PAE, Pout, Gain) of Power Amplifier Design at 4.0V DC Bias and 4.0 GHz

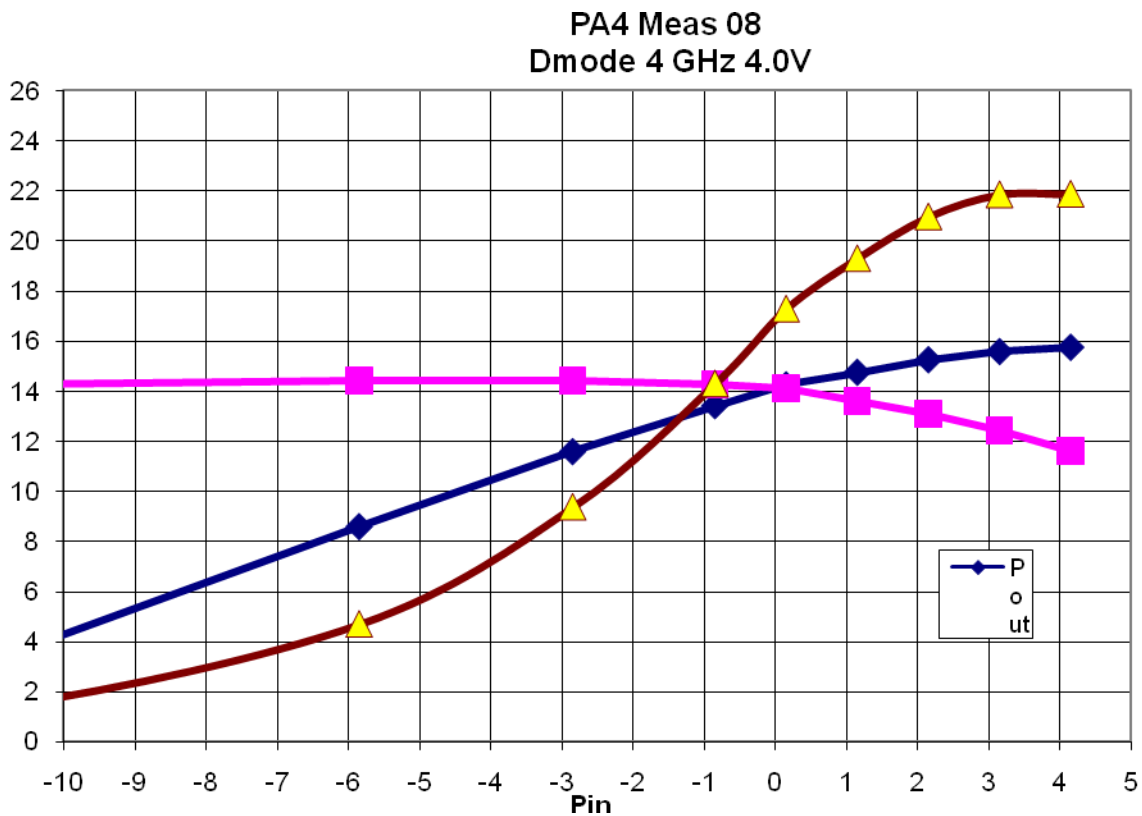
D Mode Power Amps--4.0 GHz example at 4.0 V

Measured better at lower voltages...

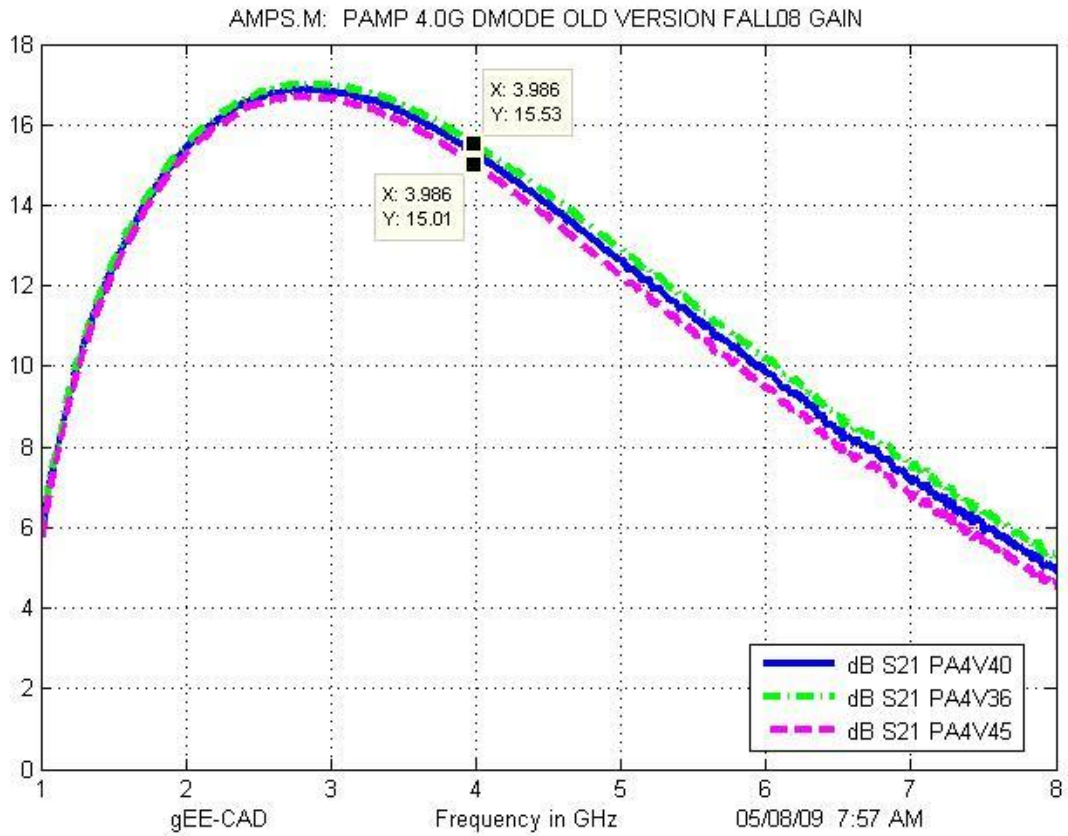
Loss 1.7 dB for thru

4 GHz Die#1 PA4 GHz Dmode Fall06 TQPED 4.0V ; 37 mA Middle DIE vgs=-0.1V

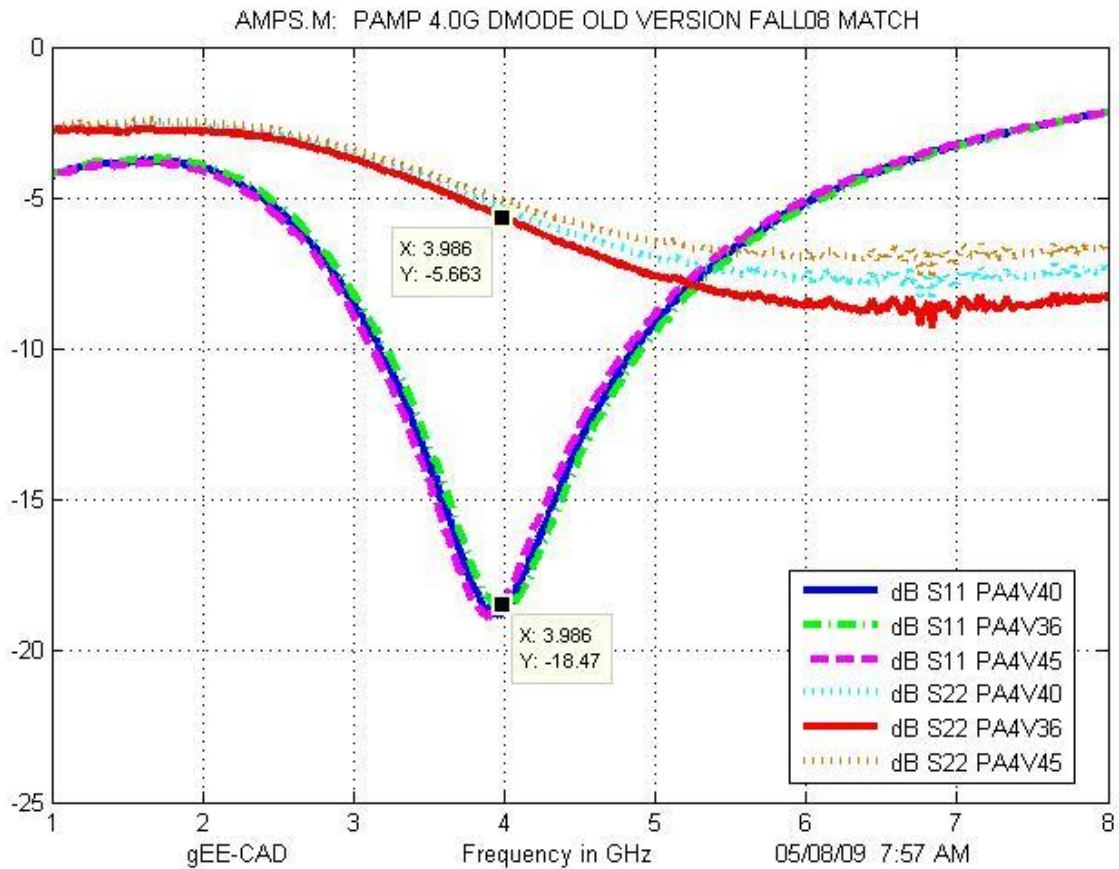
Pin(SG)	Pout(SA)	Pin(corr)	Pout(corr)	Gain	I1(4.0V)	PDC(mw)	Pout(mw)	Dm Eff	PAE
-15.0	-2.50	-15.85	-1.75	14.10	37	148.0	0.67	0.5	0.4
-10.0	2.67	-10.85	3.42	14.27	37	148.0	2.20	1.5	1.4
-5.0	7.83	-5.85	8.58	14.43	37	148.0	7.21	4.9	4.7
-2.0	10.83	-2.85	11.58	14.43	37	148.0	14.39	9.7	9.4
0.0	12.67	-0.85	13.42	14.27	37	148.0	21.98	14.9	14.3
1.0	13.50	0.15	14.25	14.10	37	148.0	26.61	18.0	17.3
2.0	14.00	1.15	14.75	13.60	37	148.0	29.85	20.2	19.3
3.0	14.50	2.15	15.25	13.10	38	152.0	33.50	22.0	21.0
4.0	14.83	3.15	15.58	12.43	39	156.0	36.14	23.2	21.8
5.0	15.00	4.15	15.75	11.60	40	160.0	37.58	23.5	21.9



PA4 Pout, Gain, PAE vs. Pin



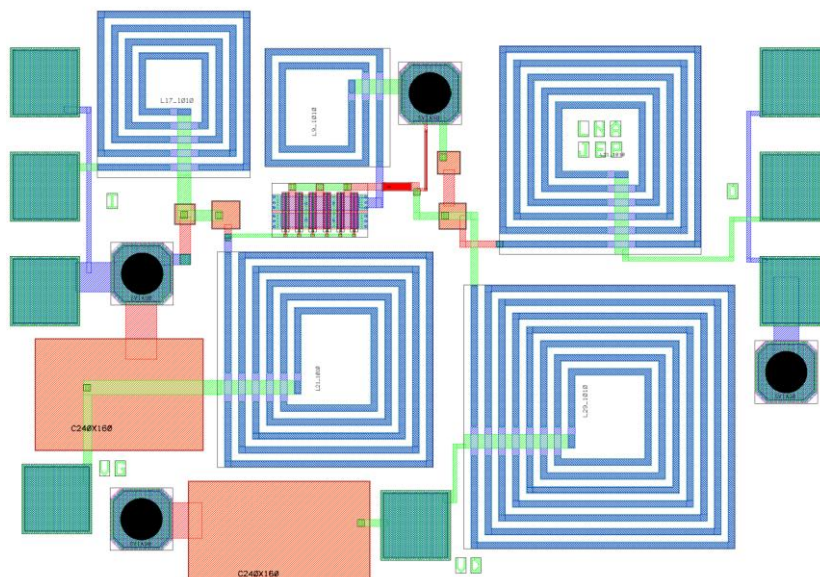
Measurements of PA4 Gain (3.6, 4.0, & 4.5 V Vss)



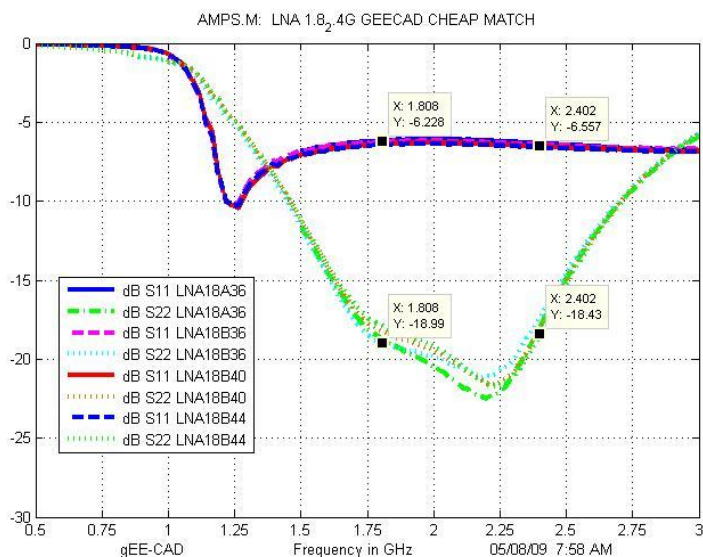
Measurements of PA4 Match (3.6, 4.0, & 4.5 V Vss)

Class Design Examples: Low Noise Amplifier 1.8 to 2.4 GHz by John Penn

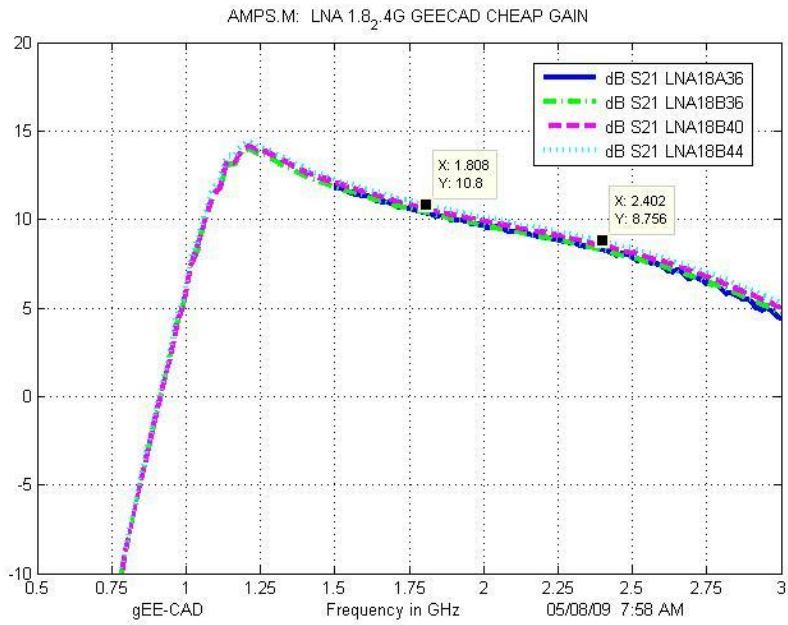
A low noise amplifier was designed for use from 1.8 to 2.4 GHz using inexpensive CAD tools for linear simulation and layout. ICED, which is now open-source, was used for manual layout of the design which was design rule checked and layout versus schematic checked to a netlist generated for the amplifier. GeeCAD created by Dr. Lee Edwards and Sheng Cheng is used by many students in the Johns Hopkins University Engineering Program for professionals. GeeCAD operates with the student version of Matlab. Simulations of the s-parameters and noise figure data were performed using data files provided by TriQuint for their Emode 0.5 um PHEMTs for the TQPED GaAs process. TriQuint also has a simple inductor model calculator which was used to improve the initial ideal simulations by generating lumped element models for the five lossy inductors used in the design. Other simple inexpensive linear simulation tools could be used besides GeeCAD. For comparison, the same design was simulated with MWO, ADS, and the physical layout was EM simulated with Sonnet. Measurements were taken at 3.6, 4.0, and 4.4V at 6 mA for comparison to the simulations. The data file was for 3V at 4.4 mA which is comparable to these measurements when you factor in the voltage drop for a series stabilizing resistor on the drain of the PHEMT and also a shunt stabilizing resistor which “steals” a couple of mA of current. A large capacitor could be used on this shunt resistor to provide an RF ground while reducing the overall power consumption.



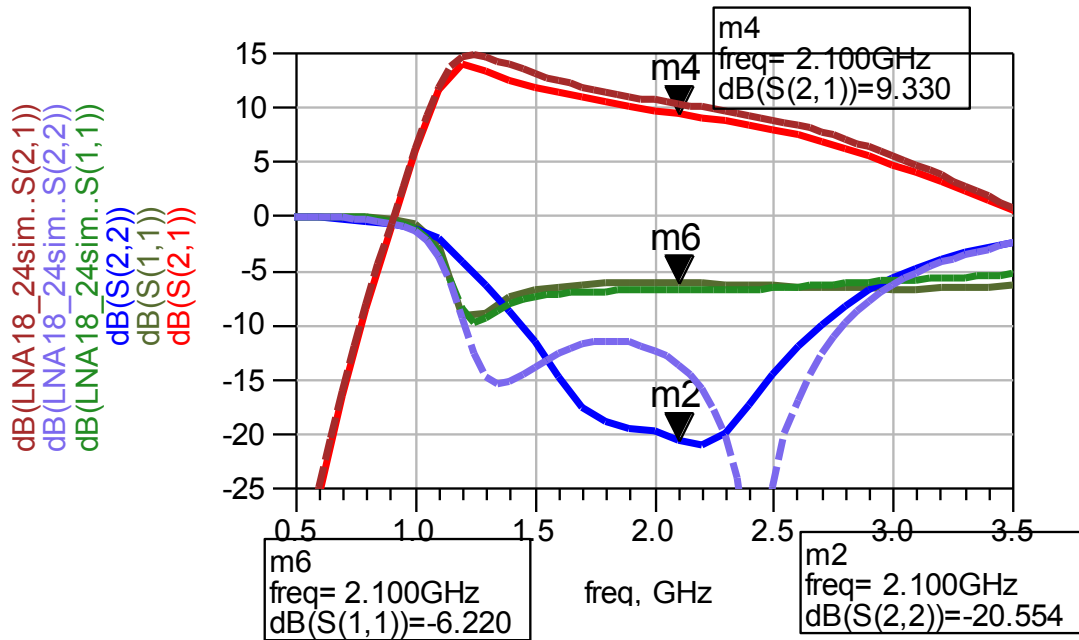
Layout of 1.8 to 2.4 GHz Low Noise Amplifier—Layout with ICED



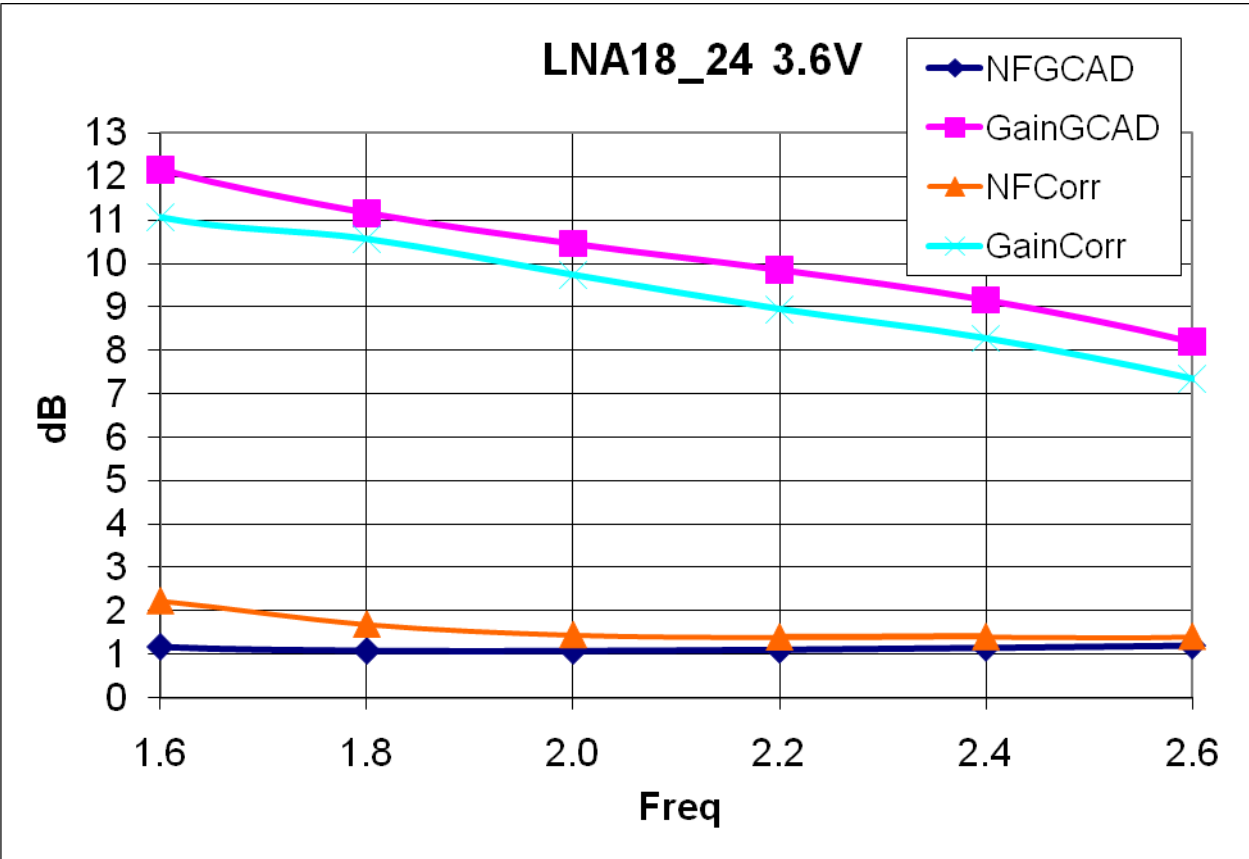
Return Loss s11/s22 of 1.8 to 2.4 GHz Low Noise Amplifier—Measured 3.6, 4.0, 4.4V



Gain s21 of 1.8 to 2.4 GHz Low Noise Amplifier—Measured 3.6, 4.0, 4.4V



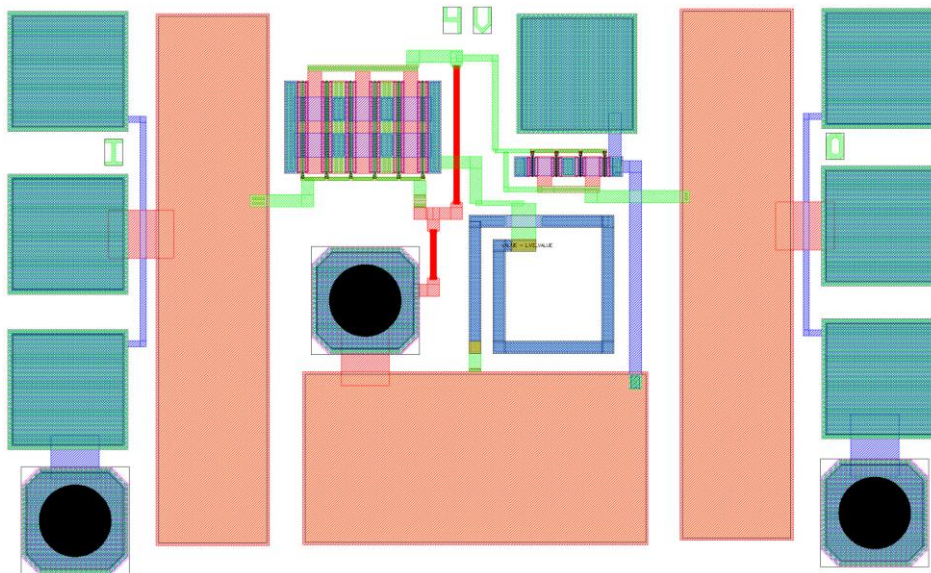
Measured vs. Simulated 1.8 to 2.4 GHz Low Noise Amplifier (ADS Sim)



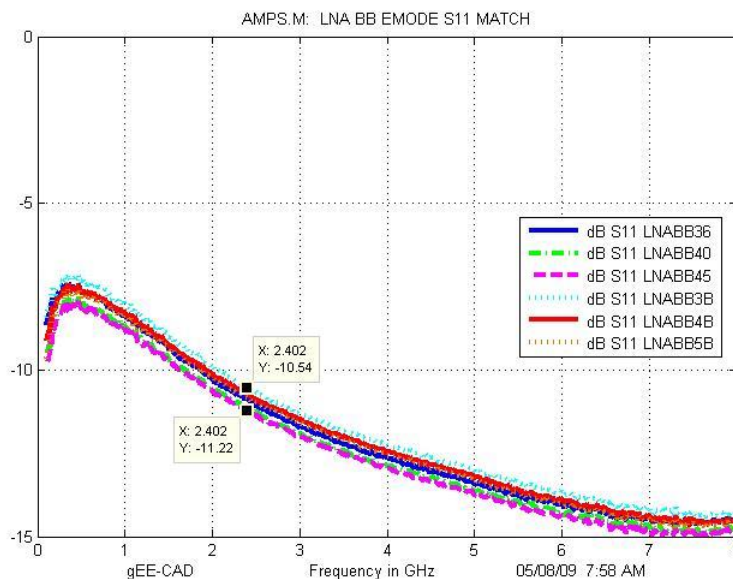
Measured Noise Figure vs. Simulated 1.8 to 2.4 GHz Low Noise Amplifier
(1.4 dB NF Measured--3.6V at 6 mA)

Class Design Examples: Broad Band Low Noise Amplifier by John Penn

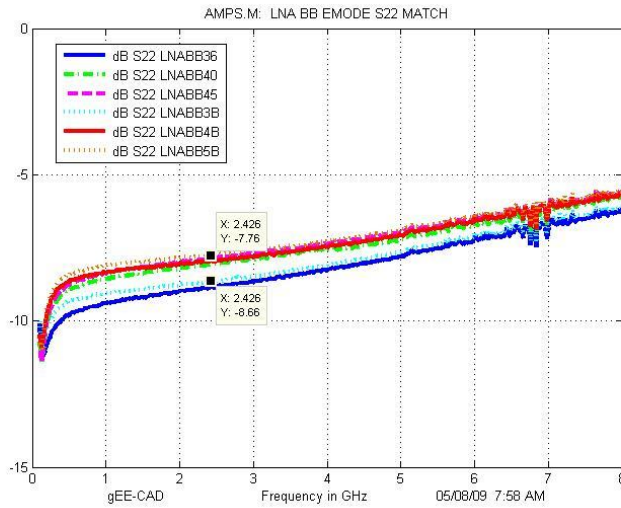
A very broad band low noise amplifier was designed by trading off match and gain while varying the PHEMT device size and using some feedback resistance between gate and drain. Also, the design size was minimized by using a Dmode PHEMT as an active load to set the drain current. An Emode PHEMT was used for the amplifier PHEMT as it tends to have slightly lower noise figure and slightly more gain than the Dmode devices for the same DC power. Also, the Emode device uses a positive voltage for the gate bias which was provided by a simple resistor divider network.



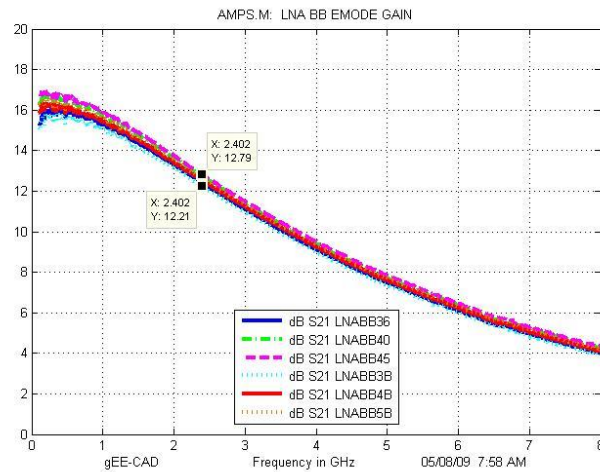
Layout of Small BroadBand Low Noise Amplifier



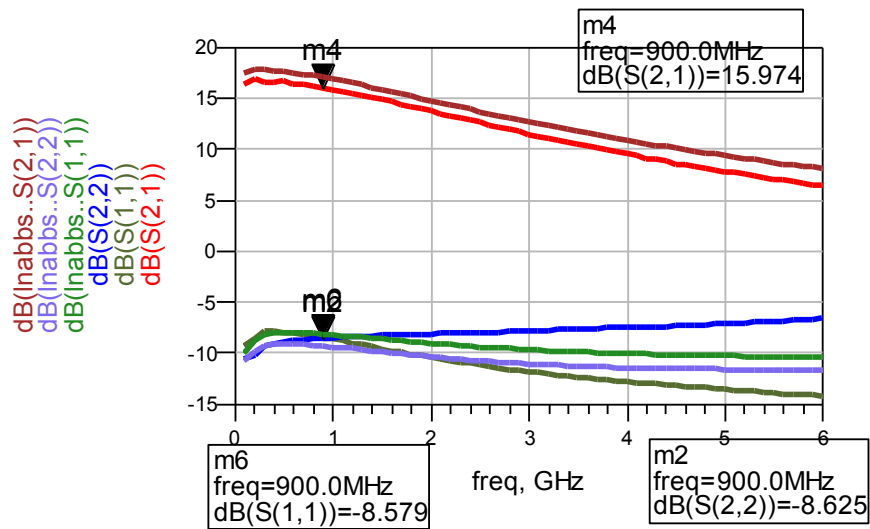
Measured s11 of Small BroadBand Low Noise Amplifier at 3.6V, 4.0V, and 4.5V (2 Die)



Measured s22 of Small BroadBand Low Noise Amplifier at 3.6V, 4.0V, and 4.5V (2 Die)

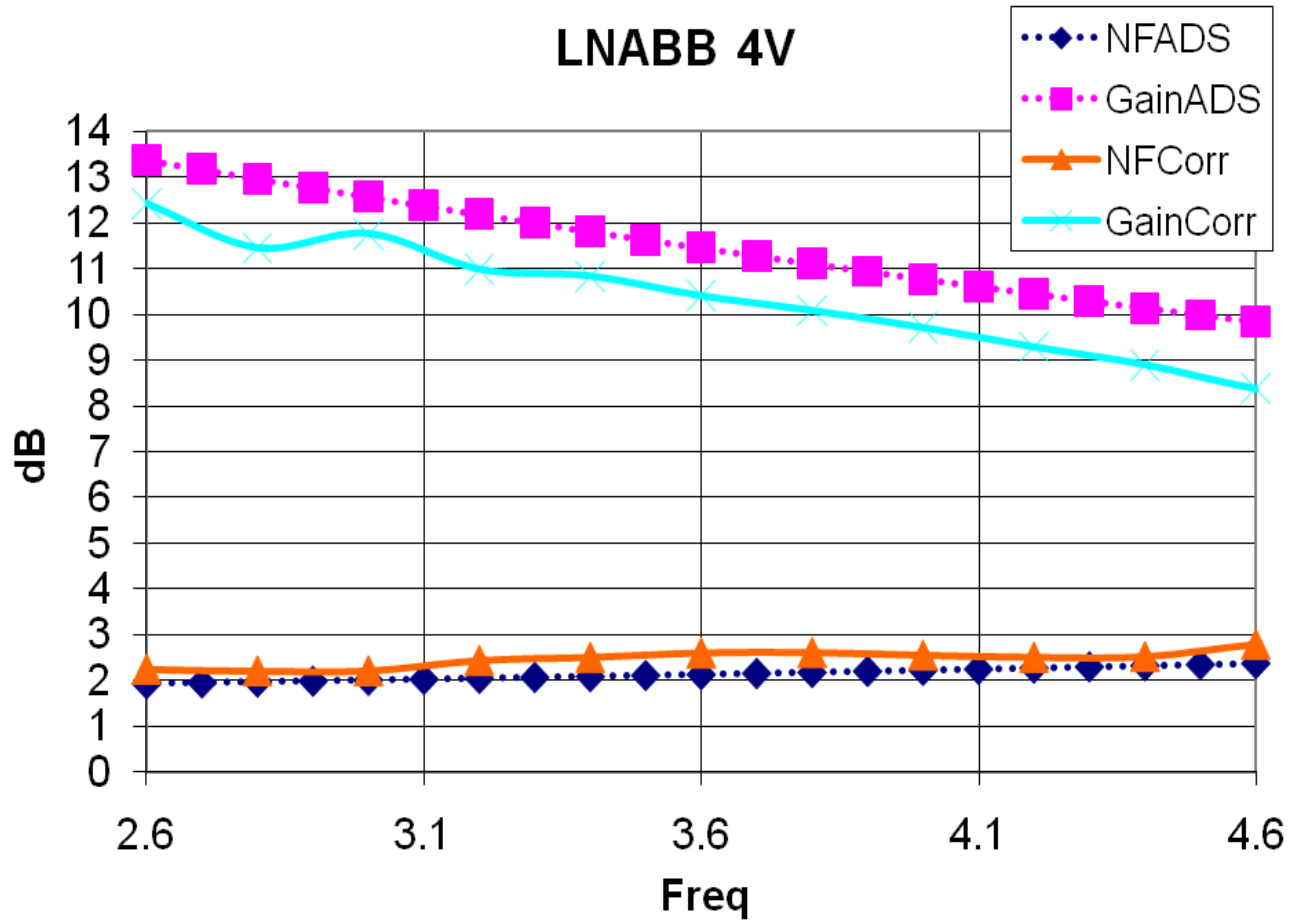


Measured Gain (s21) of Small BroadBand Low Noise Amplifier at 3.6V, 4.0V, and 4.5V (2 Die)



Measured vs. Simulated S-Parameters BroadBand Low Noise Amplifier at 3.6V-4.5V (2 Die)

LNABB 4V



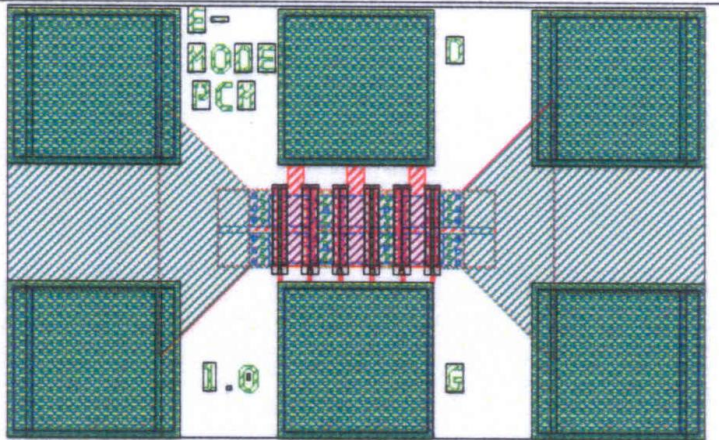
Measured vs. Simulated S-Parameters BroadBand Low Noise Amplifier
(Meas NF 2.2 dB at 3 GHz vs. 2.0 dB Simulated)

Class Test Devices: Dmode 300 um, and Emode 30, 60, 300, and 450 um PHEMTs

Several test structures were measured. There was very good agreement between given s-parameters and measured 300 um Dmode and Emode PHEMTs.

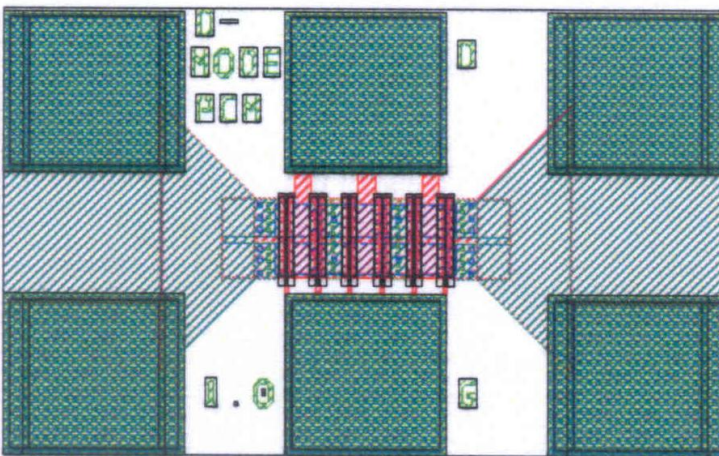
DC Biases for the 300 um Emode were:

3V @ 5 mA	VG = +0.48V	E300V3I5
3V @ 12 mA	VG = +0.55V	E300V3I12
3V @ 27 mA	VG = +0.65V	E300V3I27
4V @ 13 mA	VG = +0.55V	E300V4I13
4V @ 28 mA	VG = +0.65V	E300V4I28



DC Biases for the 300 um Dmode were:

3V @ 7 mA	VG = -0.6V	D3V3I7
3V @ 20 mA	VG = -0.45V	D3V3I20
3V @ 52 mA	VG = -0.15V	D3V3I52
4V @ 21 mA	VG = -0.45V	D3V4I21
4V @ 52 mA	VG = -0.15V	D3V4I52



DC Biases for the 60 um Emode were:

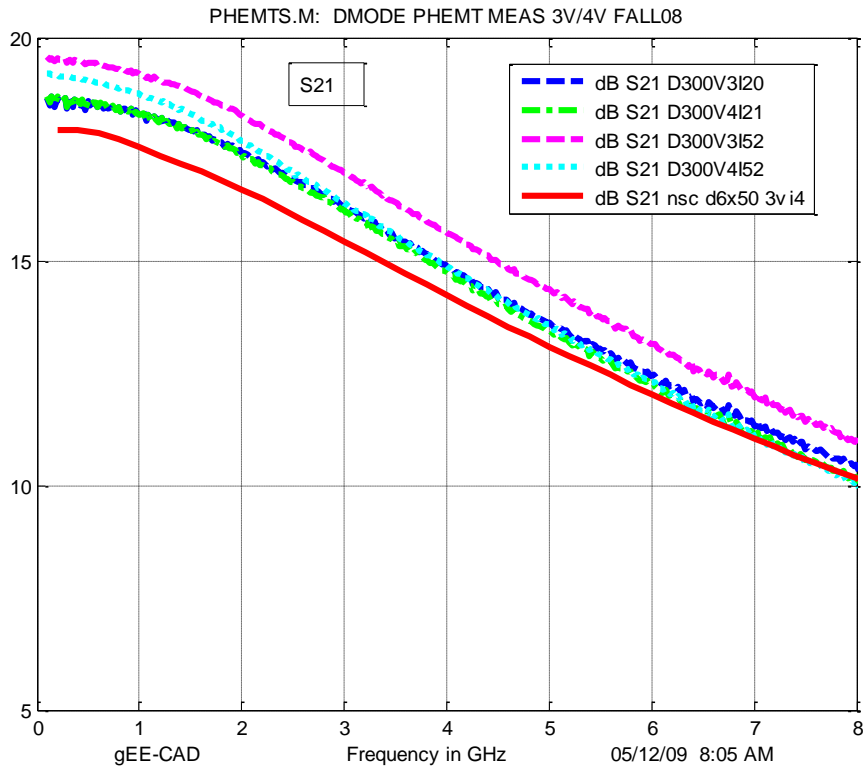
3V @ 5 mA	VG = +0.65V	E60305
4V @ 3 mA	VG = +0.60V	E60403

DC Biases for the 30 um Emode were:

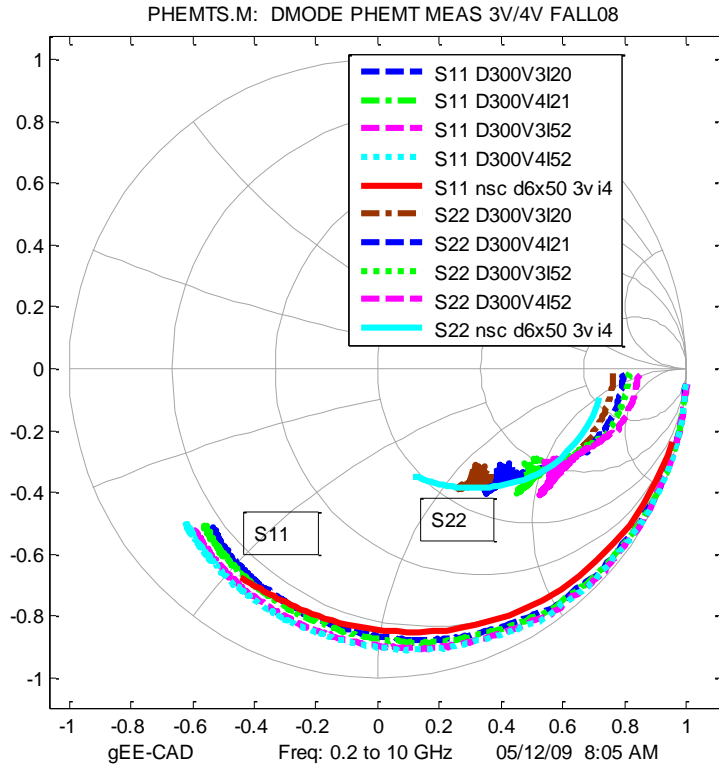
3V @ 2 mA	VG = +0.65V	E30302
4V @ 3 mA	VG = +0.60V	E30403

DC Biases for the 450 um Dmode were:

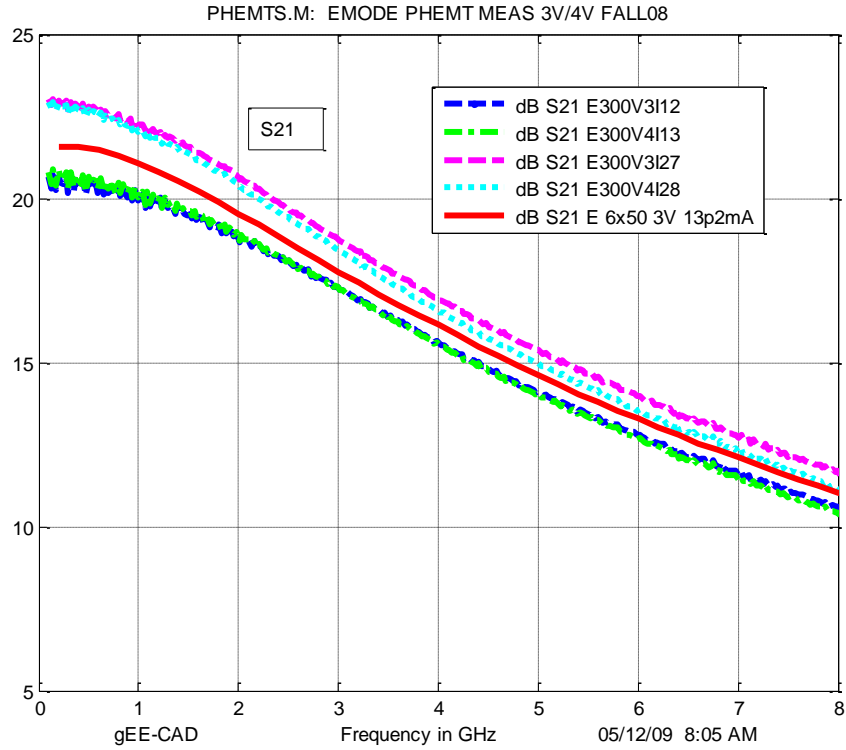
3V @ 21 mA	VG = +0.55V	E450321
4V @ 22 mA	VG = +0.55V	E450422
3V @ 44 mA	VG = +0.65V	E450344
4V @ 45 mA	VG = +0.65V	E450445



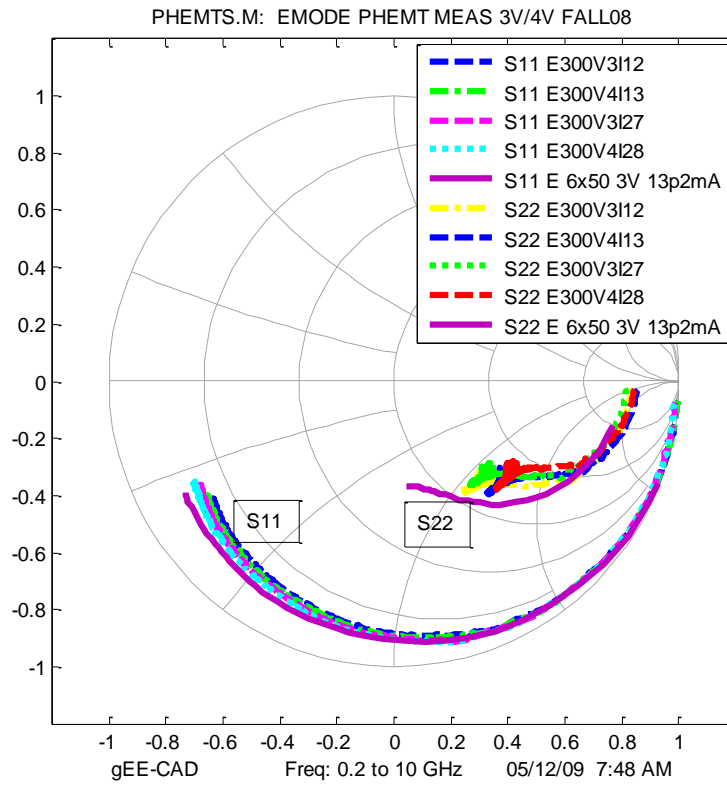
Dmode Gain S21 3V Measured vs. Linear TQS Files



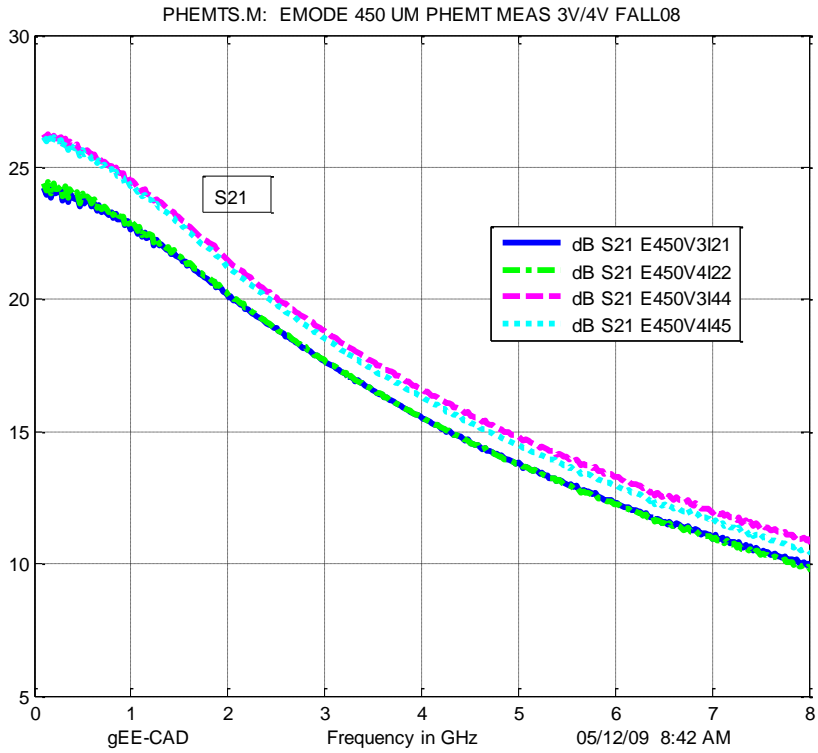
Dmode Match S11/S22 3V Measured vs. Linear TQS Files



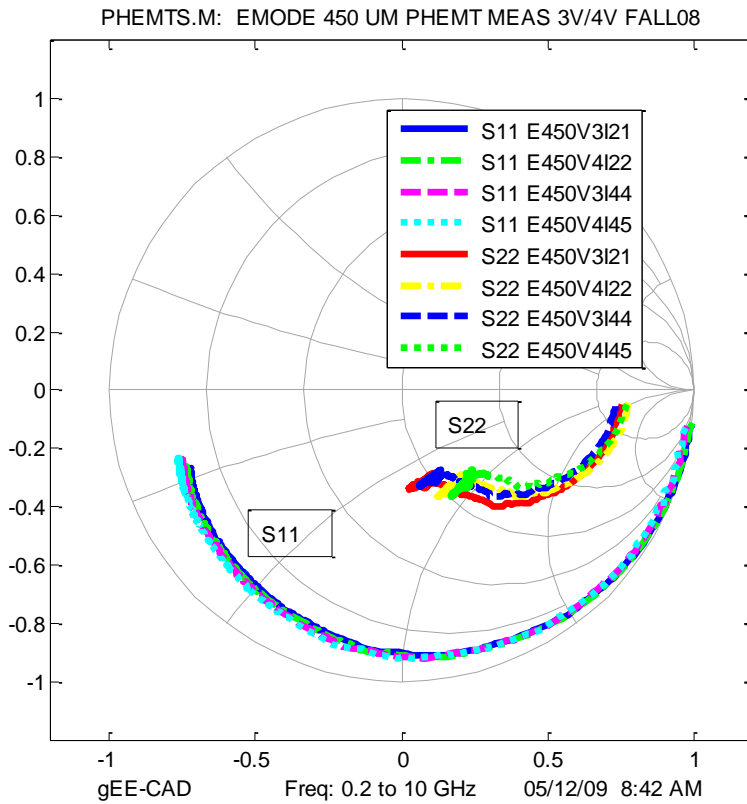
Emode Gain S21 3V Measured vs. Linear TQS Files



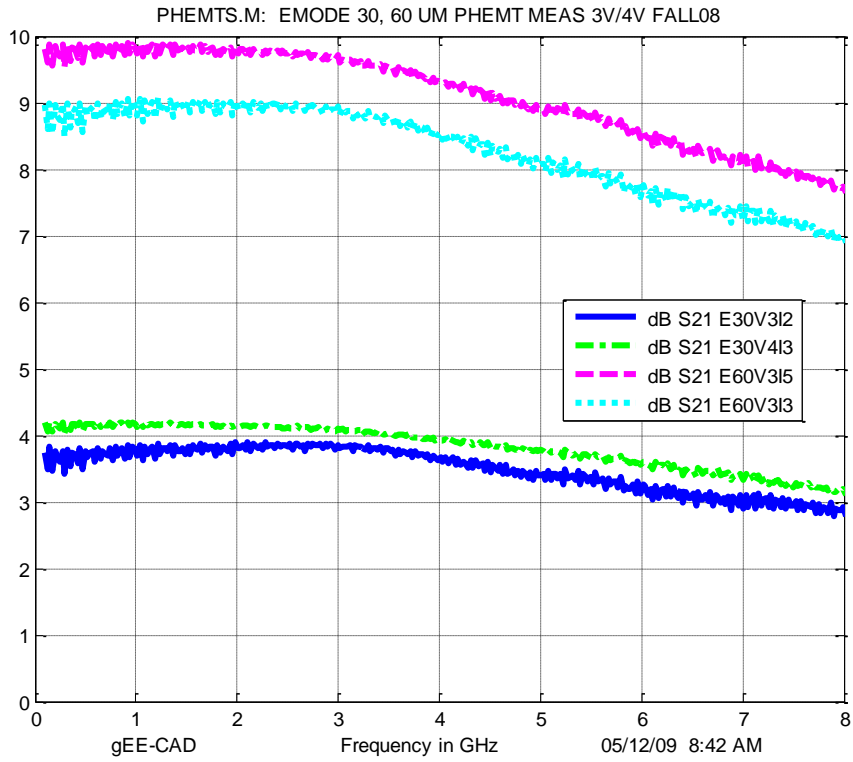
Emode Match S11/S22 3V Measured vs. Linear TQS Files



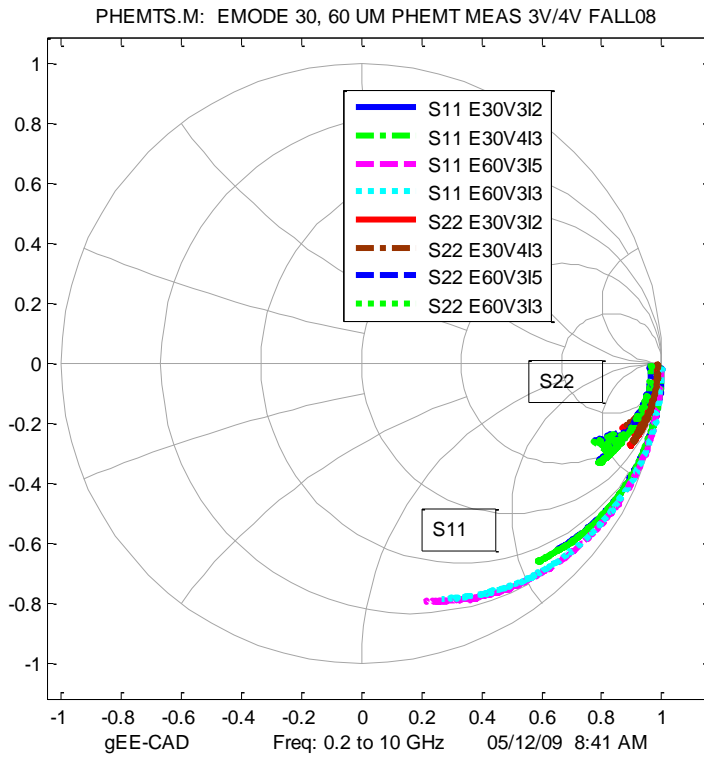
Emode 450 um Gain S21 3V Measured



Emode 450 um Match S11/S22 3V Measured



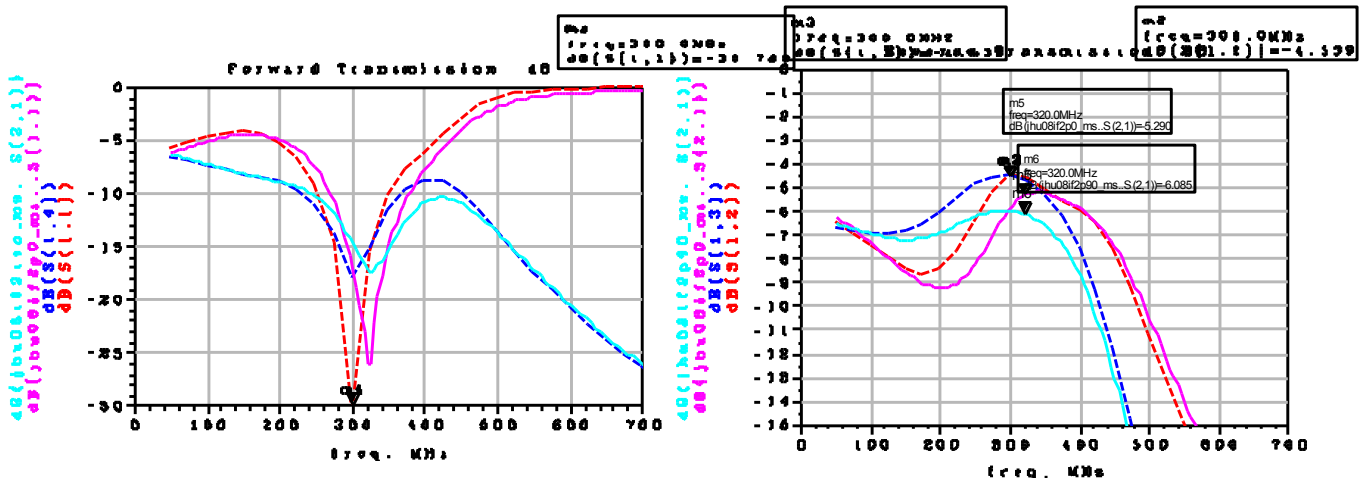
Emode 30 & 60 um Gain S21 3V Measured



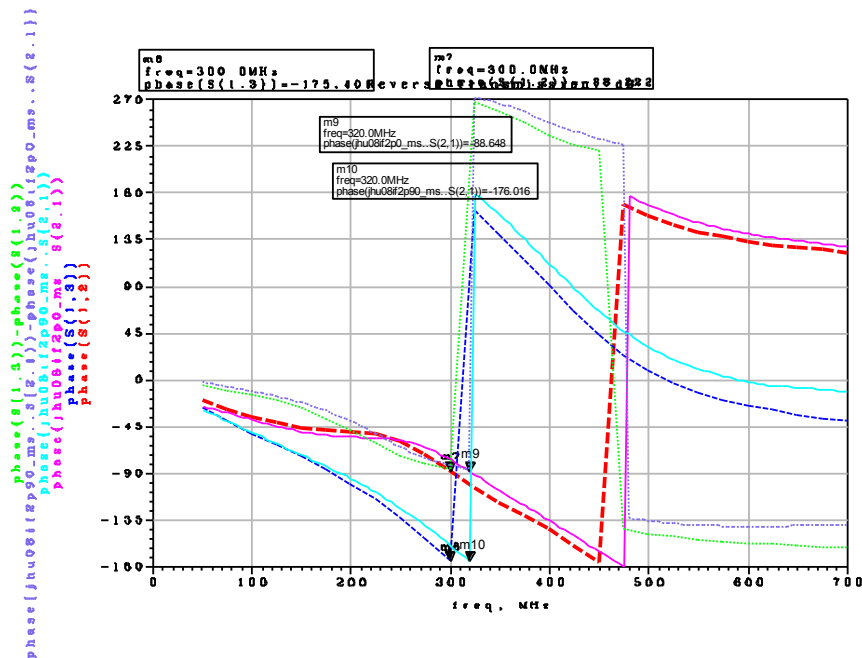
Emode 30 & 60 um Match S11/S22 3V Measured

Class Design Examples: Branchline Hybrid for Image Reject Mixer (300 MHz) by John Penn

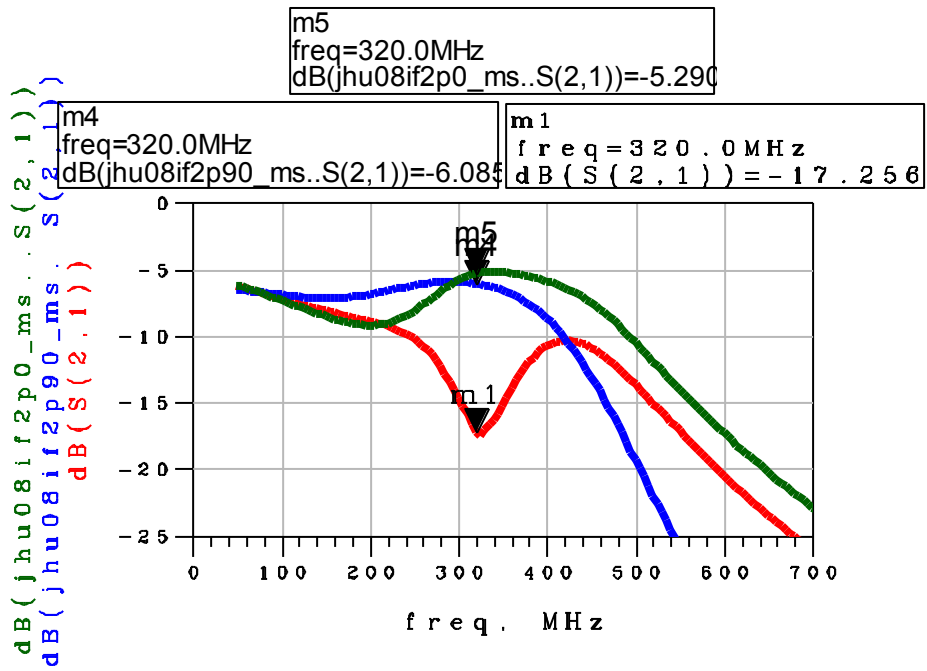
A student in the Fall 2007 MMIC Design course was interested in designing an image reject mixer, but then changed his project to a different topology. Since the branchline hybrid would have large inductor values for an IF combiner as the frequency got lower, an image reject mixer with an IF of 300 MHz was designed. The key limitation for the mixer was size and insertion loss in designing the IF branchline on a GaAs substrate. A couple of designs were performed trading off size versus insertion loss. Following are some measured results of a 300 MHz lumped element hybrid in 60x90 mil die size.



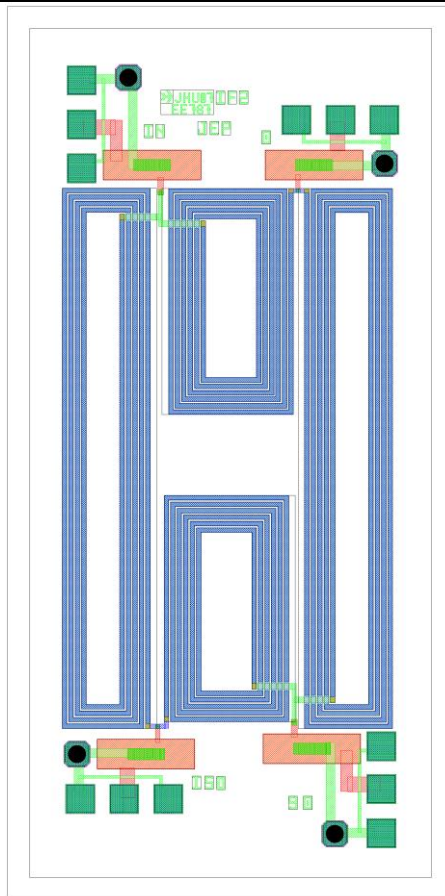
Measured versus Simulated Insertion Loss 300 MHz 90 degree hybrid in GaAs (60x90 mil die)



Measured Insertion Loss and Phase for 300 MHz 90 degree hybrid in GaAs (60x90 mil die)



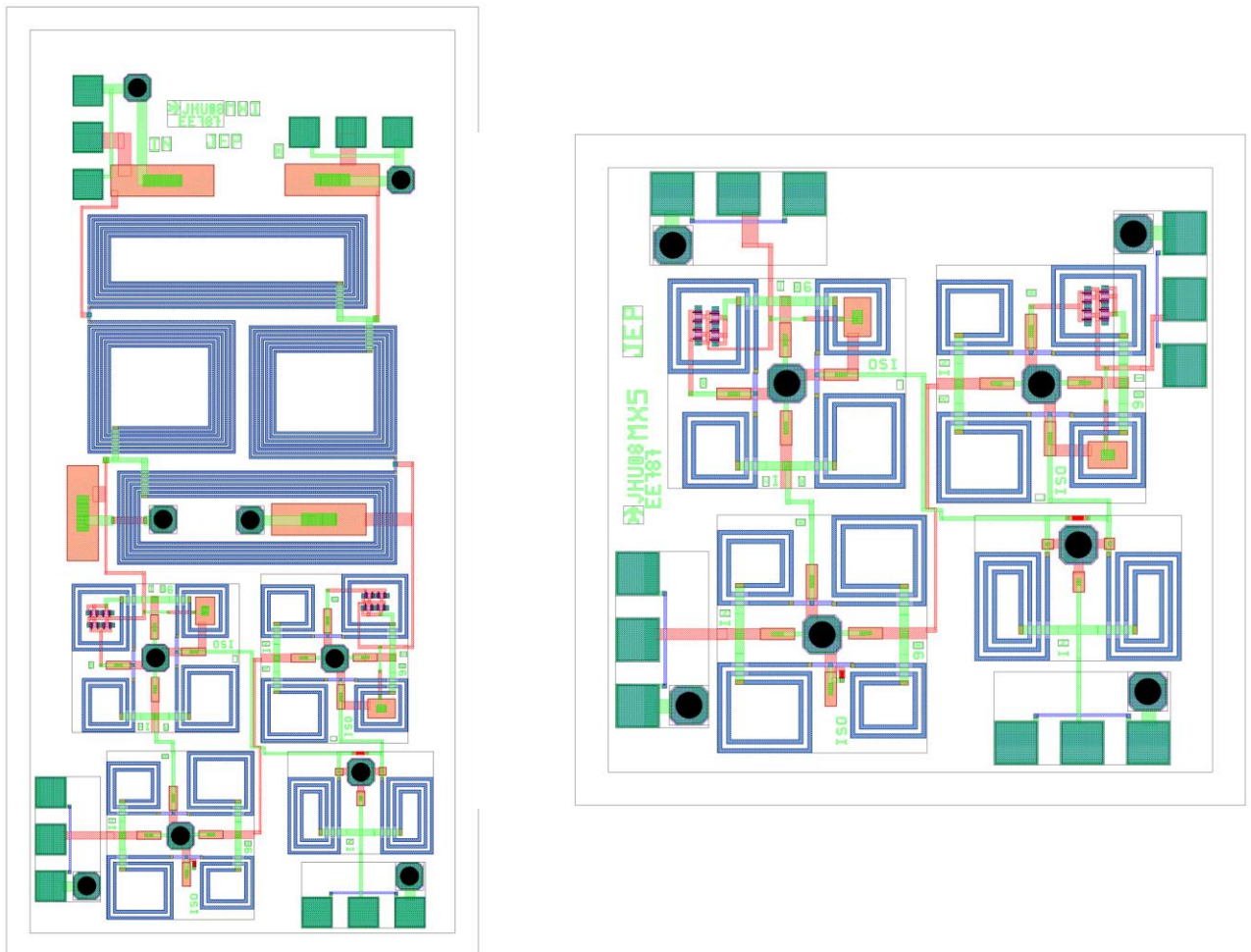
Insertion Loss and Isolation as Measured (320 MHz)



Layout of 300 MHz IF hybrid

C-Band Image Reject Mixer (IF=300 MHz) by John Penn

A C-Band Mixer for an image reject mixer was designed with and without the IF lumped element hybrid combiner. A 54 x 54 mil die contains the mixer minus the IF hybrid and a 54 x 114 mil die combined the C-band mixer plus the smaller IF1 hybrid measured with the fall 2007 MMIC class. Ideally the unused port should be terminated in 50 ohms, but for these measurements, the unused port was left open. In combining the layouts of the IF1 hybrid and the C-band mixer, the GSG probe ports were inadvertently mixed so that only 3 ports could be measured using a manual orthogonal probe station. The C-band mixer could have allowed the fourth port to be terminated but for consistency the port was also left unterminated. The LO was driven as high as possible (~14 dBm) using a signal generator and subtracting cable losses and a GSG probe for the 5.5 GHz LO. RF was tested at 5.19, 5.2, 5.21, 5.79, 5.8, and 5.81 GHz with about 14 dB conversion loss for the Mixer without the hybrid combiner, and about 2.5 to 3 dB more insertion loss with the hybrid. The full image reject mixer with IF combiner was measured at the USB port with about 17 dB rejection at 300 MHz for the LSB signal at 5.2 GHz.



Plot of Mixer with IF Hybrid (left) and C-Band Mixer w/o IF combiner (right)