FALL 1996 EE787 MMIC Design
Johns Hopkins University
Measurement Results
Craig Moore and John Penn

Attached are the measurements from the Fall 1996 MMIC Design Course of Johns Hopkins University. The designs were implemented in Fall of 1996 and were fabricated by TriQuint in the summer of 1997. Measurements were made in late 1997 and early 1998. Overall the designs were very successful. Unfortunately measurements for the RF T/R Switch were not available when these results were compiled. I understand that the device was successfully tested up to 1 Watt but I expect the results at a later date. Craig Moore and I did measure an individual probable FET on that particular part and found that an approximate first cut model for an "ON" 300 um FET is 10.8 ohms and "OFF" is about 110 fF. This is pretty close to the old HA switch model but the pinchoff appears to be a around -1.8V to -1.9V rather than the usual -1.5V. Attached is a smith chart plot of the switch at various biases from 0.0V to -4.0V. The name "fetvXY" implies a bias voltage of -X.Y Volts, i.e. fetv15 is the measurement at -1.5V. Also, attached are some plots of the die attaches from the power devices that were attached to kovar to act as a heat sink. We were able to probe 2 different designs up to 1/2 Watt of output and I think we were limited by our input driver not the devices. Still we were pretty happy with 1/2 Watt since that was our goal for the designs. The kovar heat sink improved the measurements even small signal for the 2 power designs considerably.

Thanks to Gary Wray of HPEEsof particularly for his excellent library development and to all of TriQuint and HPEEsof for all the support.

John E. Penn
Craig Moore
JHU EE 787 MMIC Design

□ v00
S2J2
fetv00
S[2,2]

○ v05
S2J2
fetv05
S[2,2]

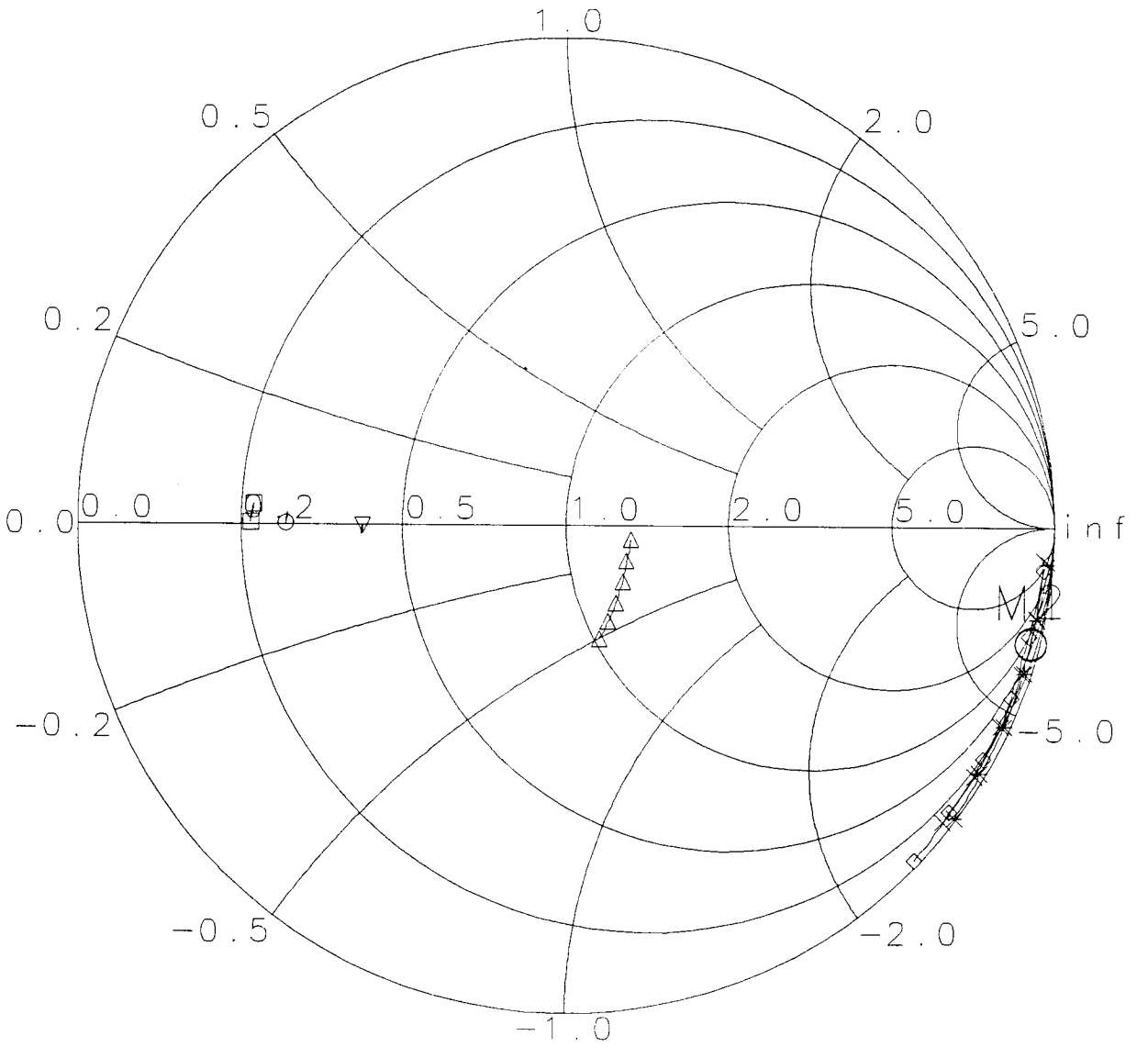
▽ v10
S2J2
fetv10
S[2,2]

△ v15
S2J2
fetv15
S[2,2]

◇ v20
S2J2
fetv20
S[2,2]

✳ v40
S2J2
fetv40
S[2,2]

× swt
S2J2
swtmdl
S[2,2]



Frequency 1.0 to 10.0 GHz

VCO Testing Fall 96 MMIC Projects

The VCO consists of a FET with tuning diodes to create an ocsillator, and a buffer amplifier to provide output matching and additional gain to achieve sufficient output power.

Bias Inputs:
1) +5V to Buffer Amp
2) +5V to VCO FET
3) Control Voltage for VCO
4) VG to set Bias for Buffer Amp

1) Because of the layout, the VCO can be tested without biasing the buffer amp. The probe station and a spectrum analzyer were used for the initial test. The device drew about 44 mA at +5V (IDSS bias). It oscillated at about 2.366 Ghz but was not tuneable. Turns out the diodes were in parallel with an inductor which essentially shorts out the bias dropping the entire bias voltage across the 100 ohm resistor to the bias. Tried breaking the airbridge inductor but still could not be tuned. The oscillation frequency did change however to about 2.44 Ghz. The oscillation was also sensitive to drain bias and shifted somewhat by varying the supply from +2V to +5V. Output power likewise changed from +3 dBM to +10 dBM. Cable losses and probe losses were not measured but were probably about 2 dB (i.e. add about 2 dB to measurements for actual power out). Essentially the VCO had the desired output power without the need for the buffer amp. The student was interested in redoing the design to fix the shorted out biasing scheme.

2) Broke airbridge from VCO to output pad to test buffer amp. Initially oscillated at 50Mhz but this was damped out by some capacitance at the DC bias probes. Amp bias was controllable and was set to about 20-40% IDSS at +5V but the only signal on the spectrum analyzer was -50dBm at about 4 Ghz. It appears that the biasing of the buffer amp may have changed the match to the VCO such that it no longer oscillated.

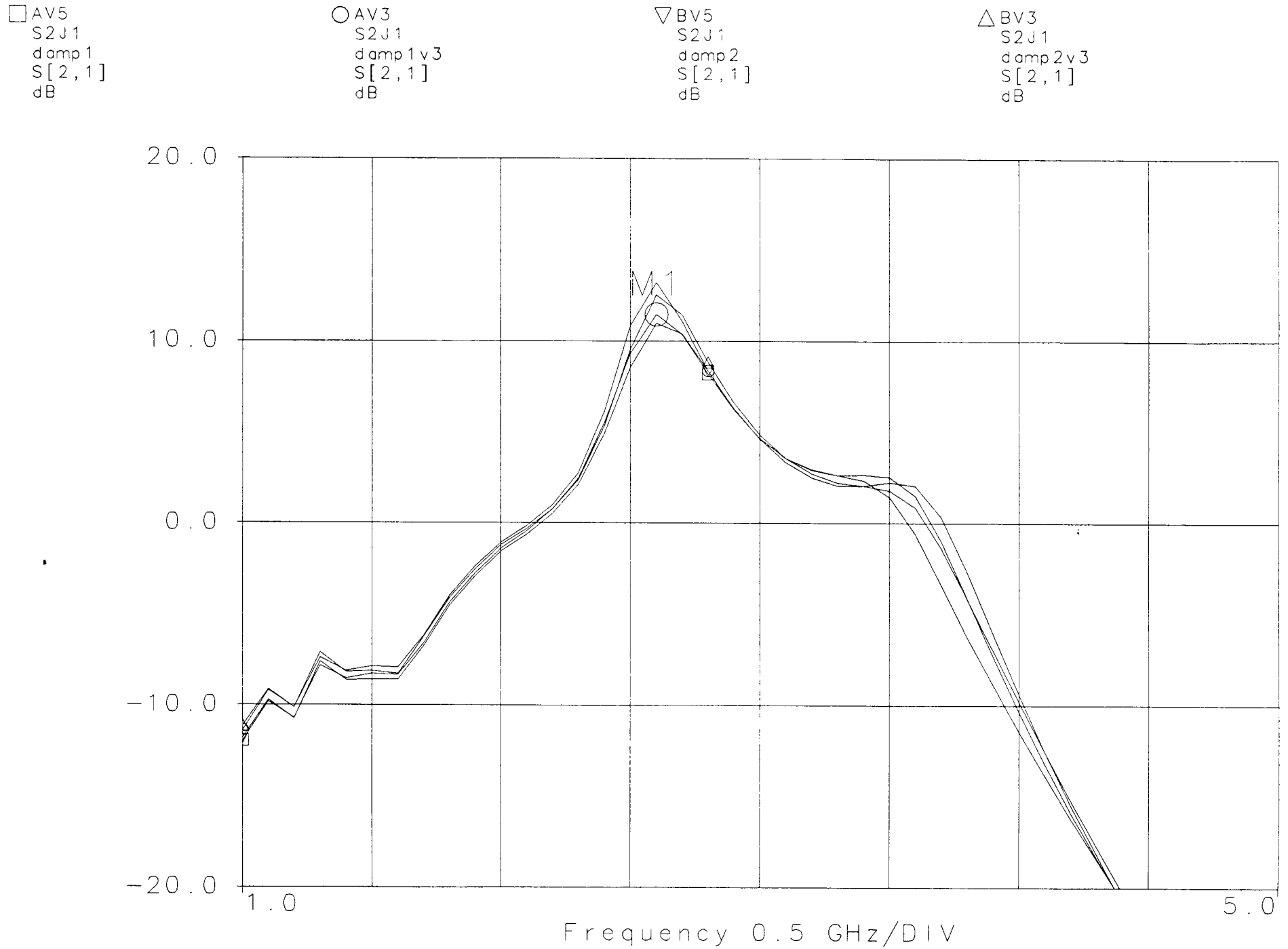
Summary: VCO oscillates with plenty of output power if the buffer amp is not used. Buffer amp needs to be redesigned as well as the inadvertant short in the oscillator tuning circuit.

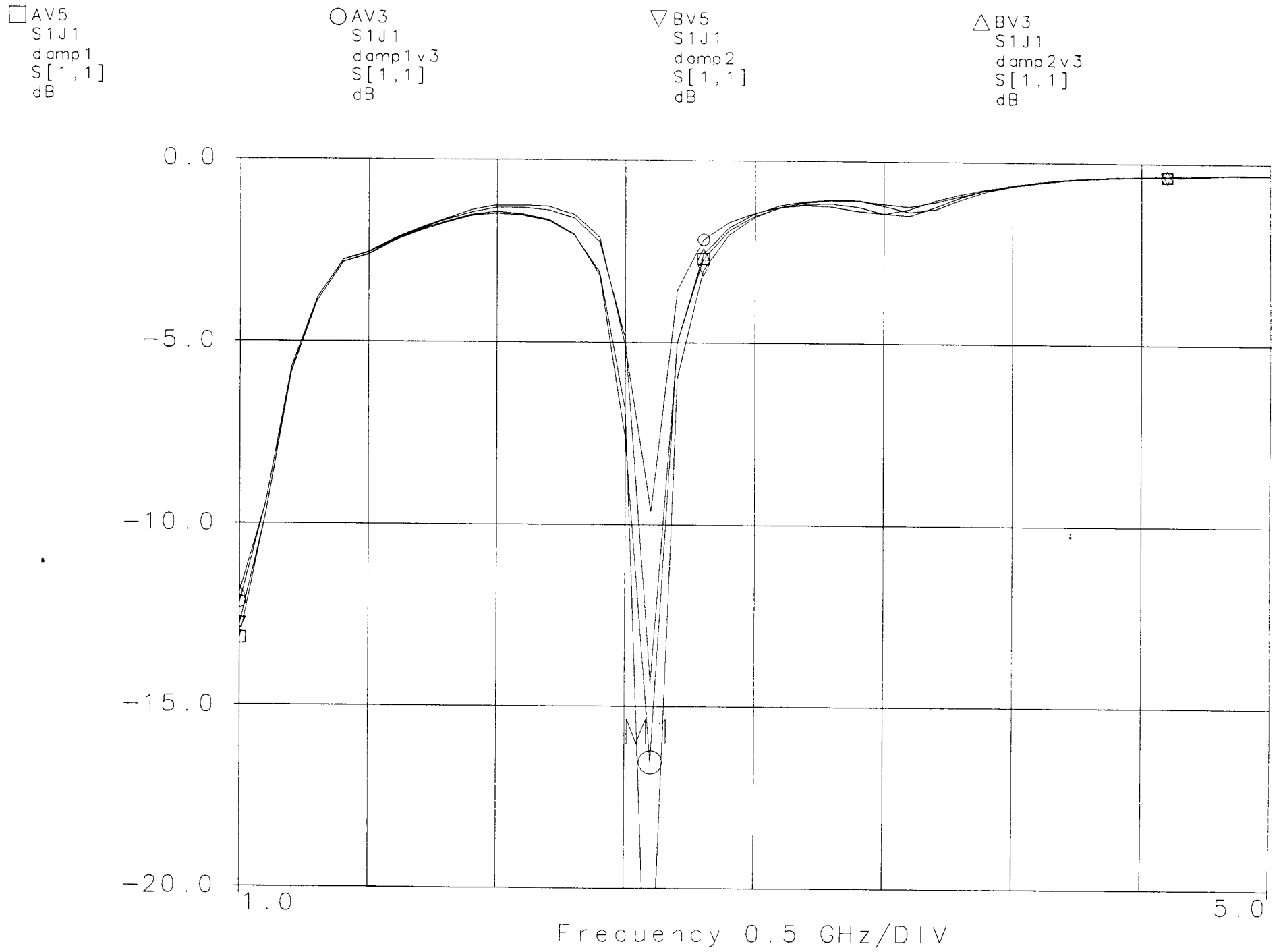
Driver Amp Testing Fall 96 MMIC Projects
Mar 9, 1998
Bias Conditions: 5V 131 mA, 3V 130 mA chip #1, saved S-parms as DAMP1, and DAMP1V3

Bias Conditions: 5V 136 mA, 3V 136 mA chip #2, saved S-parms as DAMP2, and DAMP2V3

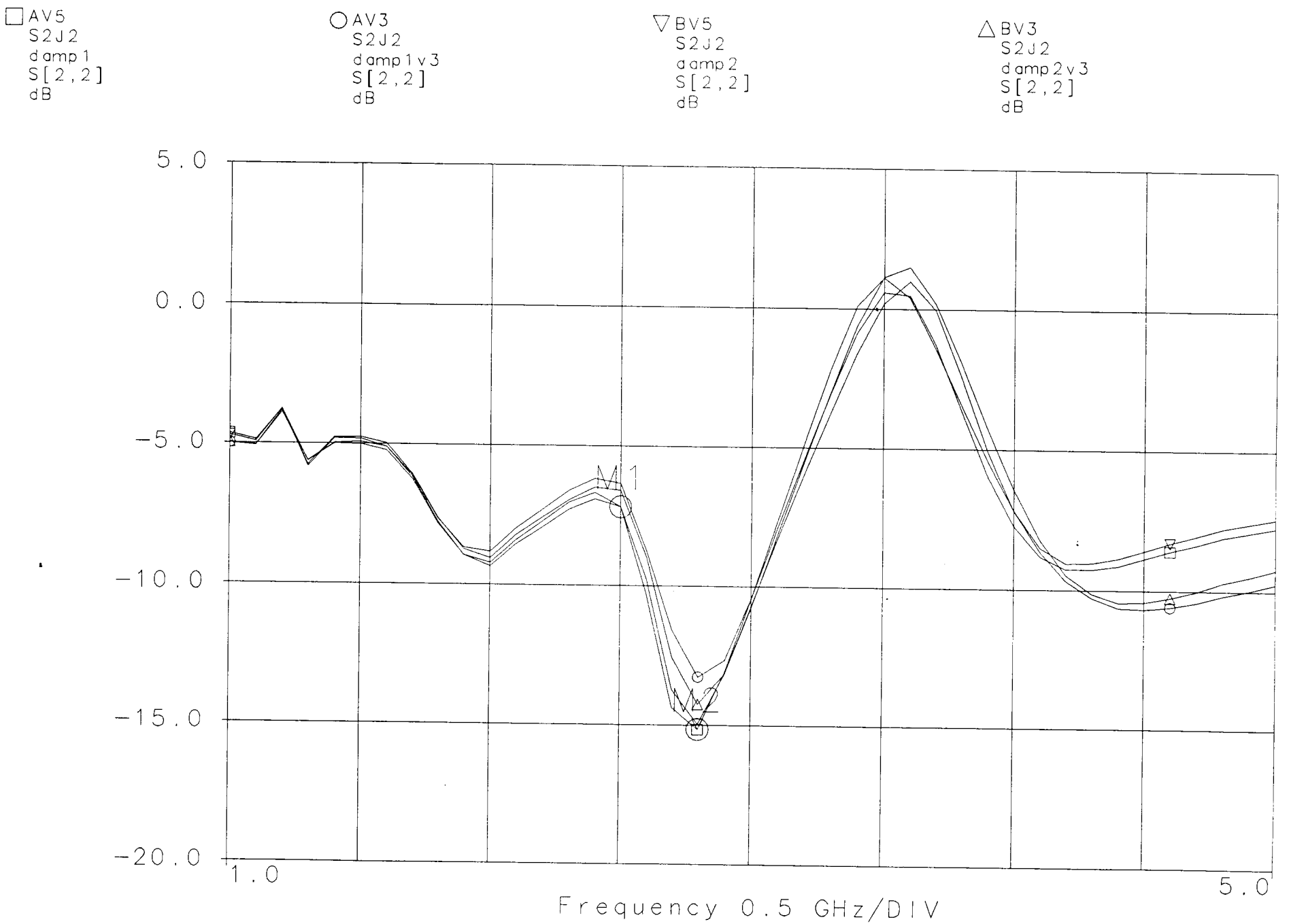
Part #	VD	I(mA)	S21	S-parms
1	5V	131	11.5 dB	DAMP1
1	4V	131	12.25 dB	
1	3V	130	13.5 dB	DAMP1V3
2	5V	136	10.9 dB	DAMP2
2	4V	137	11.4 dB	
2	3V	136	12.4 dB	DAMP2V3
3	5V	121	10.9 dB	
3	3V	119	12.4 dB	

Summary: Attached are the s-parameter plots. The part worked but was slightly high in frequency. Output power was not measured with this part but based on the power amp measurements from the same class/wafer it probably puts out something close to the students predictions. Not sure about the quality of the calibration for the S22 plot.


AV5
S2J1
damp1
S[2,1]
dB
AV3
S2J1
damp1v3
S[2,1]
dB
BV5
S2J1
damp2
S[2,1]
dB
BV3
S2J1
damp2v3
S[2,1]
dB
20.0
10.0
0.0
-10.0
-20.0
M1
1.0
5.0
Frequency 0.5 GHz/DIV
M1 Frequency=2.60000000 value=11.4476026



M1 Frequency=2.60000000 value=-16.5353610



M1 Frequency=2.50000000 value=-7.18349896

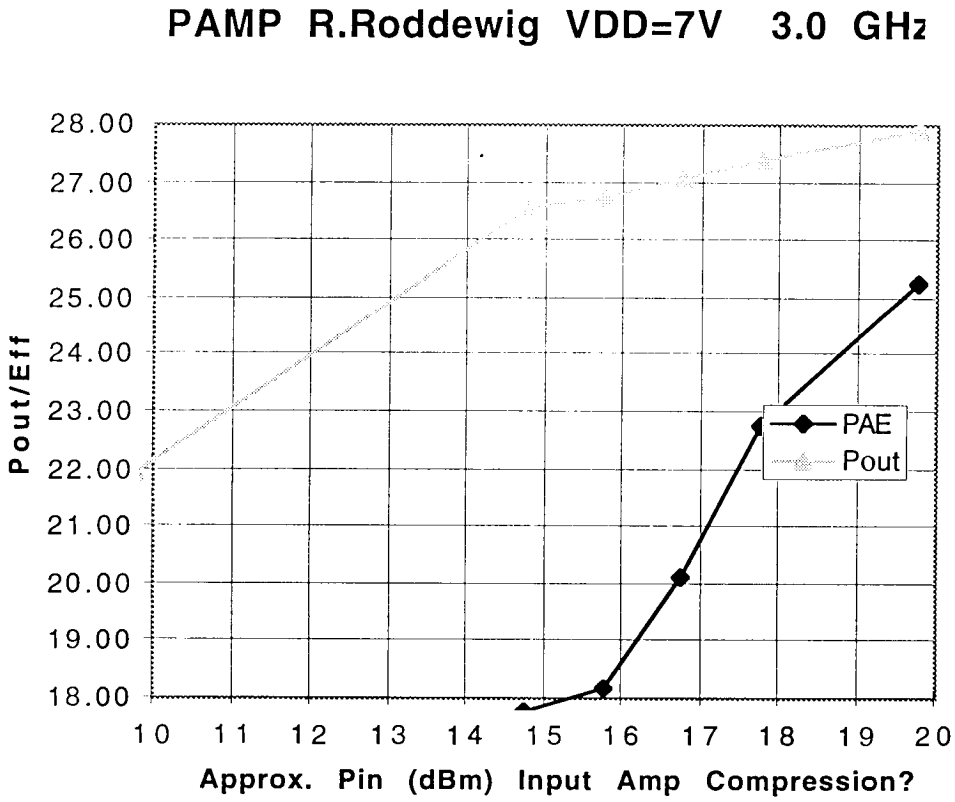
M2 Frequency=2.80000000 value=-15.1493612

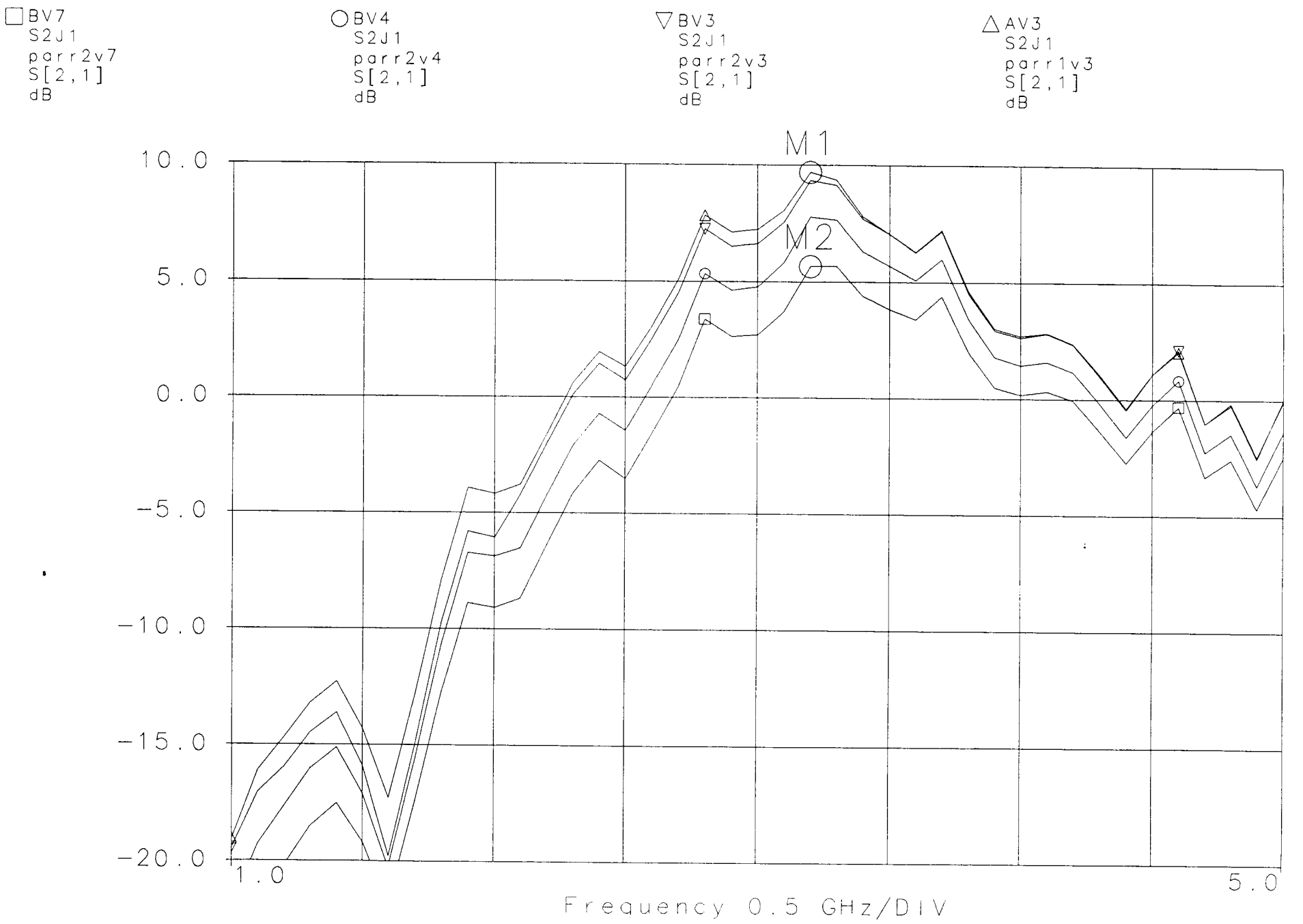
Power Amp1 Testing Fall 96 MMIC Projects (Robin Roddewig)
Mar 9, 1998

Part #	VD	I(mA)	S21	Gate	Gate (I)	S-parms
1	2.5	360	9.1	-5V	12.5	
1	3.0	360	10.5	-5V	12.5	PARR1V3
2	2.5	330	9	-5V	12.5	
2	3.0	330	10.5	-5V	12.5	PARR2V3
2	4.0	346	8.7	-3V	7.5	PARR2V4
2	7.0	168	6.0	-5V	12.5	
2	7.0	293	6.4	-2V	5.0	PARR2V7

Summary: The part worked but was high in frequency. Small signal measurements improved when the die were attached to a large kovar heat sink for probe power measurements. However attached small signal measurements were before die attach (see plots). We had trouble getting sufficient drive power into the amp but we were successful in getting 1/2 Watt out of the part. Not sure what the compression level was but it appeared that we were limited in input power drive not output capability. Cal was at 2.44 Ghz, not 3!

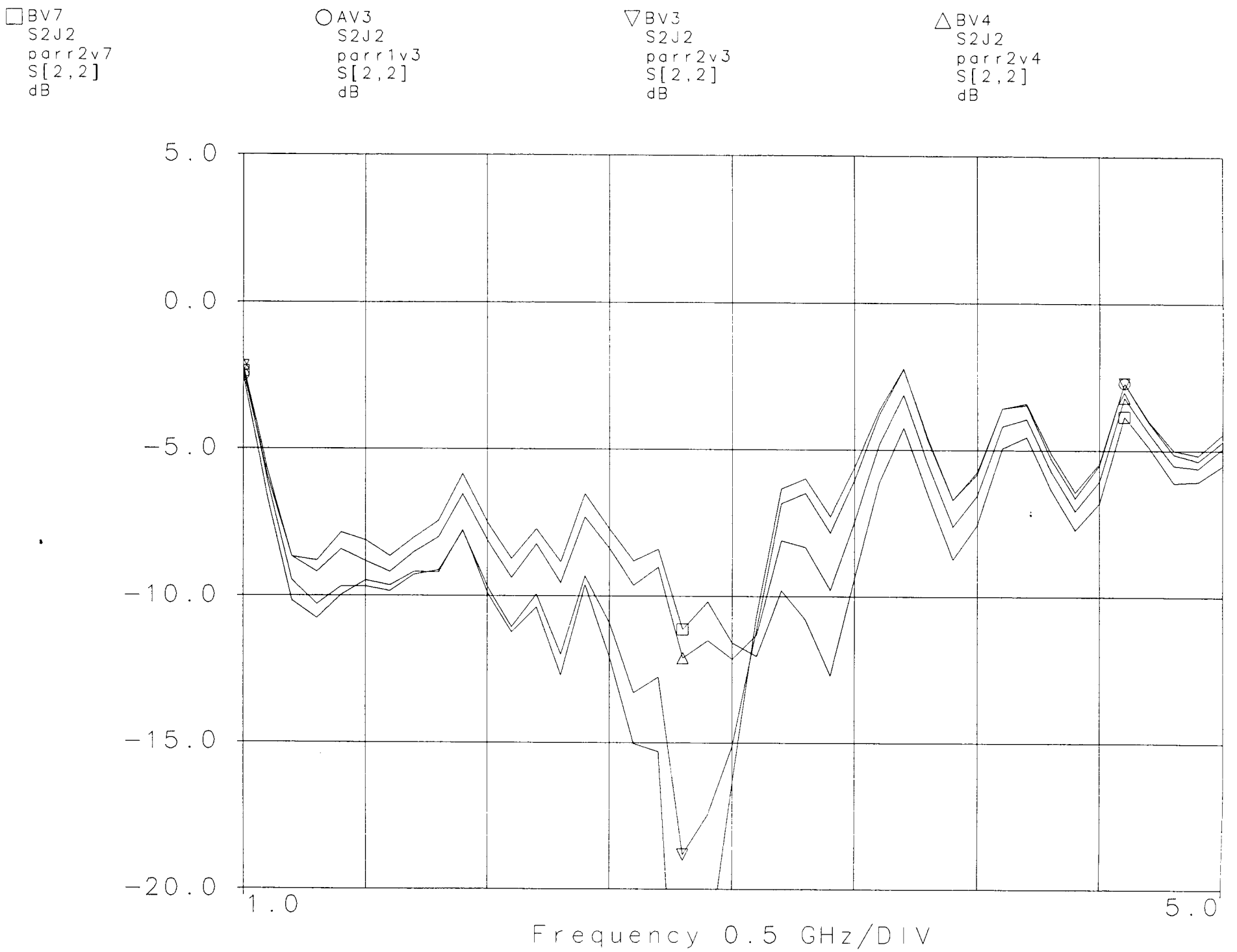
7.0 VD @ 402 mA; -5V gate network at 12.5 mA										
3.0 GHz										
Pin	Pin(comprsd)	Pout	Pout (corr)	Gain	ID	POUT	PDC	DRAIN EFF	PIN	PAE EFF
-5	9.75	3.17	21.92	12.17	369	0.16	2.65	5.88	0.01	5.53
0	14.75	7.83	26.58	11.83	333	0.45	2.39	19.01	0.03	17.77
1	15.75	8	26.75	11.00	333	0.47	2.39	19.77	0.04	18.20
2	16.75	8.33	27.08	10.33	320	0.51	2.30	22.18	0.05	20.12
3	17.75	8.67	27.42	9.67	300	0.55	2.16	25.54	0.06	22.78
5	19.75	9.17	27.92	8.17	288	0.62	2.08	29.81	0.09	25.27

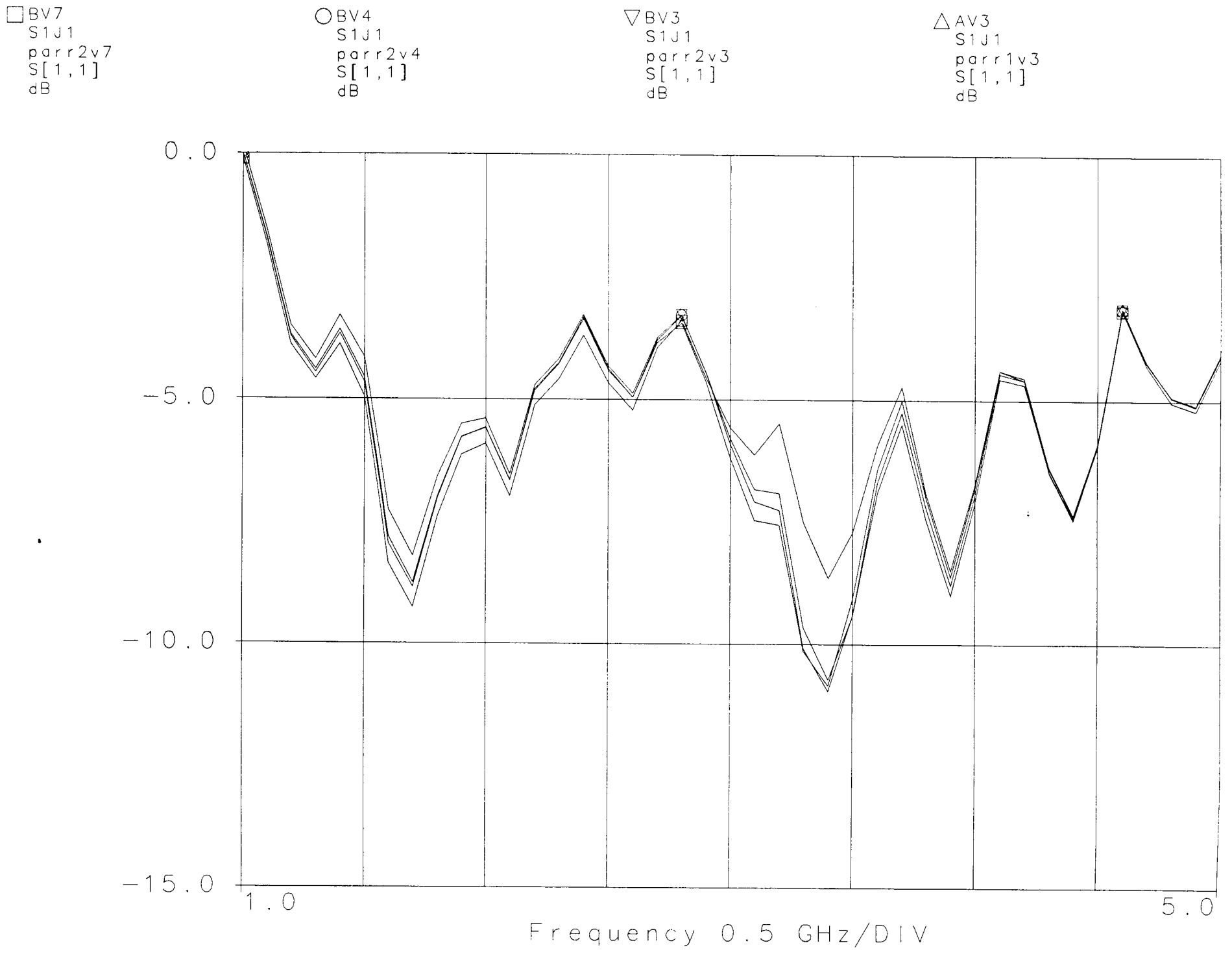


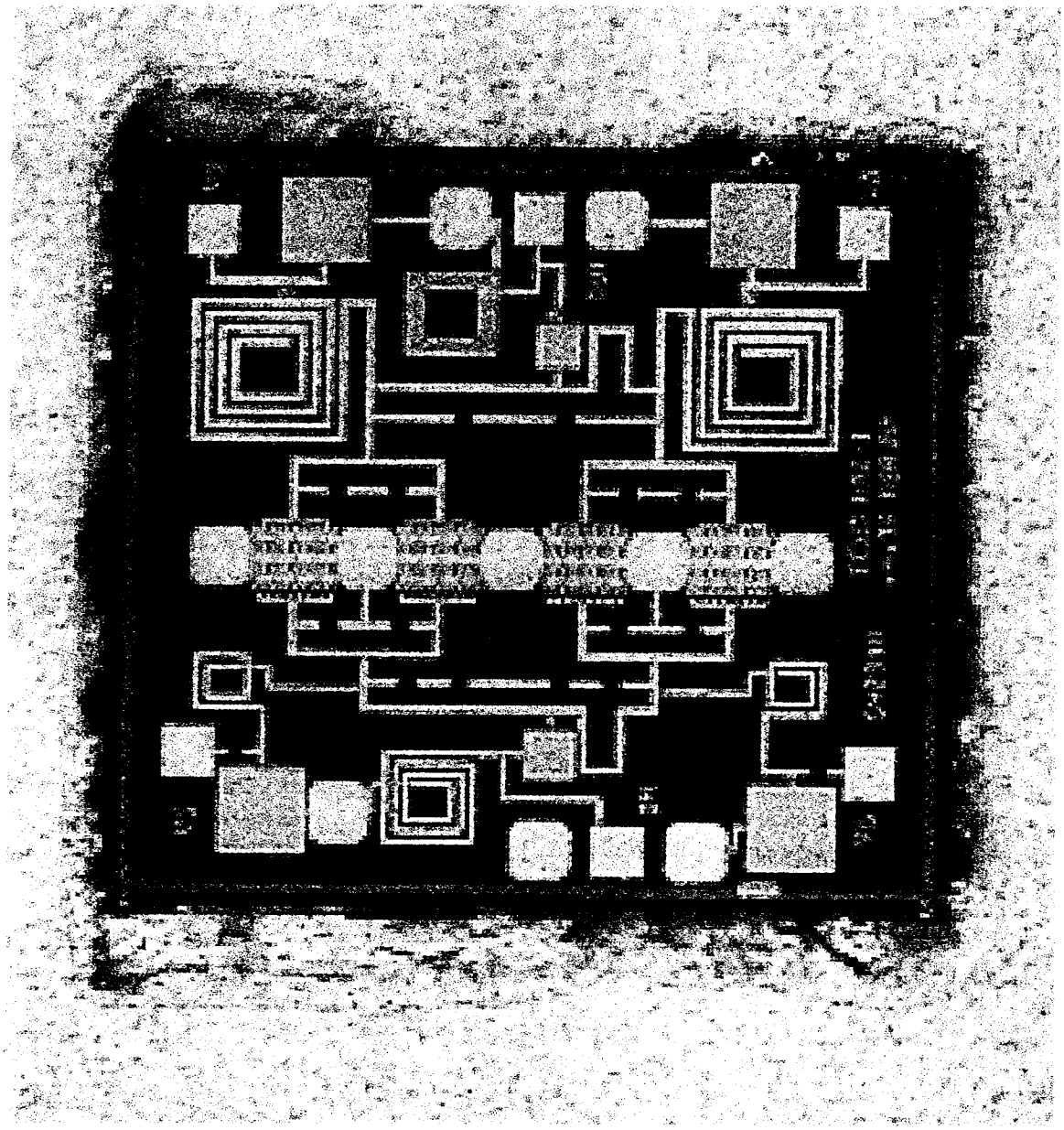


M1 Frequency=3.20000000 value=9.71572979

M2 Frequency=3.20000000 value=5.67484690


□BV7
S2J2
parr2v7
S[2,2]
dB
○AV3
S2J2
parr1v3
S[2,2]
dB
▽BV3
S2J2
parr2v3
S[2,2]
dB
△BV4
S2J2
parr2v4
S[2,2]
dB
5.0
0.0
-5.0
-10.0
-15.0
-20.0
1.0
5.0
Frequency 0.5 GHz/DIV


□BV7
S1J1
parr2v7
S[1,1]
dB
○BV4
S1J1
parr2v4
S[1,1]
dB
▽BV3
S1J1
parr2v3
S[1,1]
dB
△AV3
S1J1
parr1v3
S[1,1]
dB
0.0
-5.0
-10.0
-15.0
1.0
5.0
Frequency 0.5 GHz/DIV



LNA Testing Fall 96 MMIC Projects
Mar 9, 1998

Part #	VD	I(mA)	S21	Gate	Gate (I)	S-parms
1	7	49	9	-5V	1.5	LNA1V7
1	5	16	16	-5V	1.5	LNA1V5
2	7	49	9	-5V	1.5	LNA2V7
2	5	16	16	-5V	1.5	LNA2V5

3/16

Part #	VD	I(mA)	S21	Gate	Gate (I)	S-parms
1	7	21	18.3	-6.5V	2.0	LNA7I21
1	7	38	14.1	-6.0V	1.8	LNA7I38
1	7	50	10.6	-5.5V	1.7	LNA7I50
2	7	20	18.6	-6.5V	2.0	LNA7I21B
2	7	35	16.0	-6.0V	1.8	LNA7I38B
2	7	48	11.6	-5.5V	1.7	LNA7I50B

Summary: The low noise amplifier was farely broadband as seen in the attached plots. However, it seemed to work better at 5V on the drain rather than the 7V as designed. It appeared that the single bias supply may have been supplying too much current. When we ran the parts at 7V but increased the gate voltage to reduce the drain current, the gain of the part went up several dB to the expected range. It was noted in measurements of an individual FET from that wafer run that the threshold voltage appeared to be around -1.8V to -1.9V rather than the -1.5V nominal. Noise measurements were not taken.

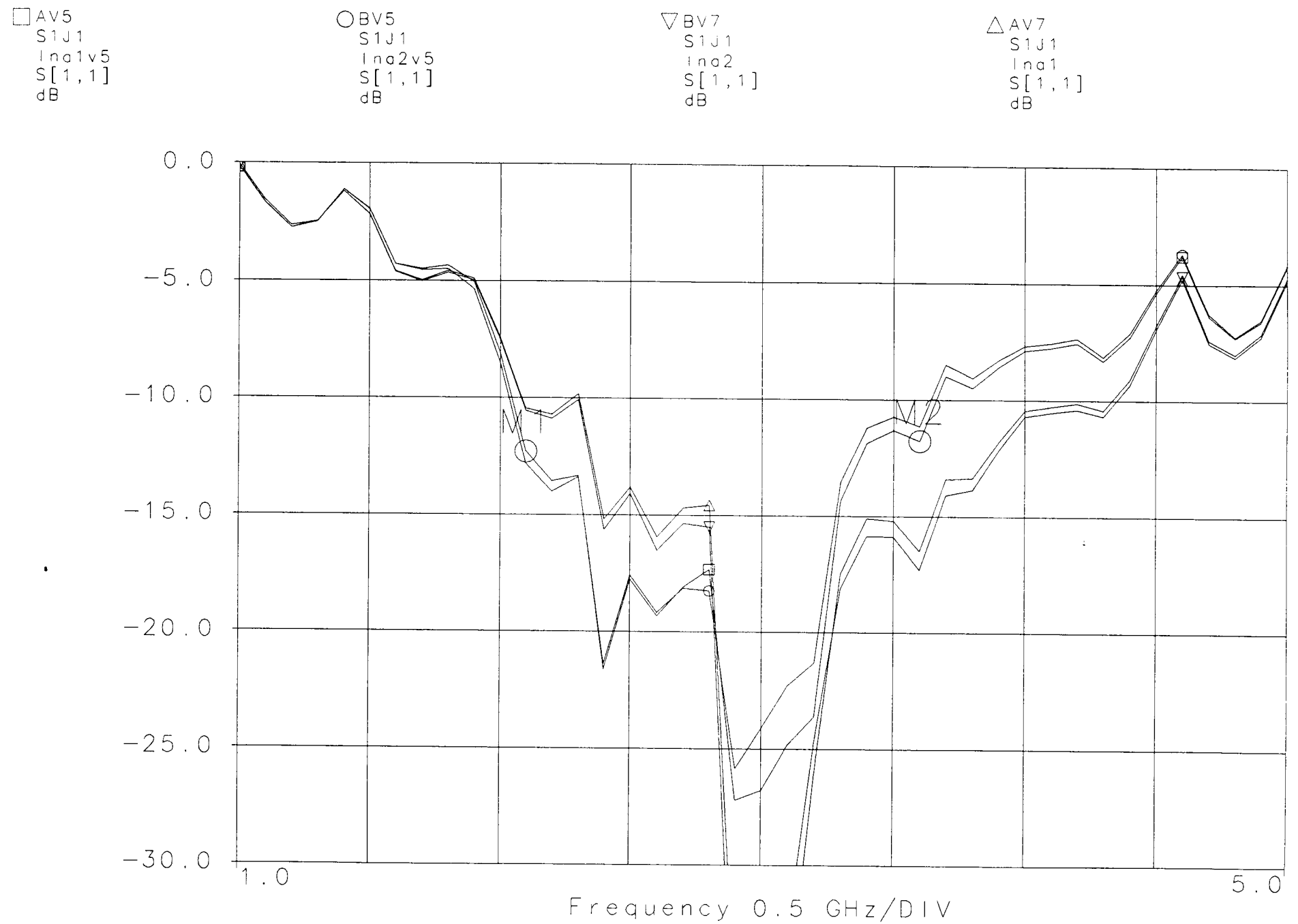
□ AV5
S2J1
Ina1v5
S[2,1]
dB

○ BV5
S2J1
Ina2v5
S[2,1]
dB

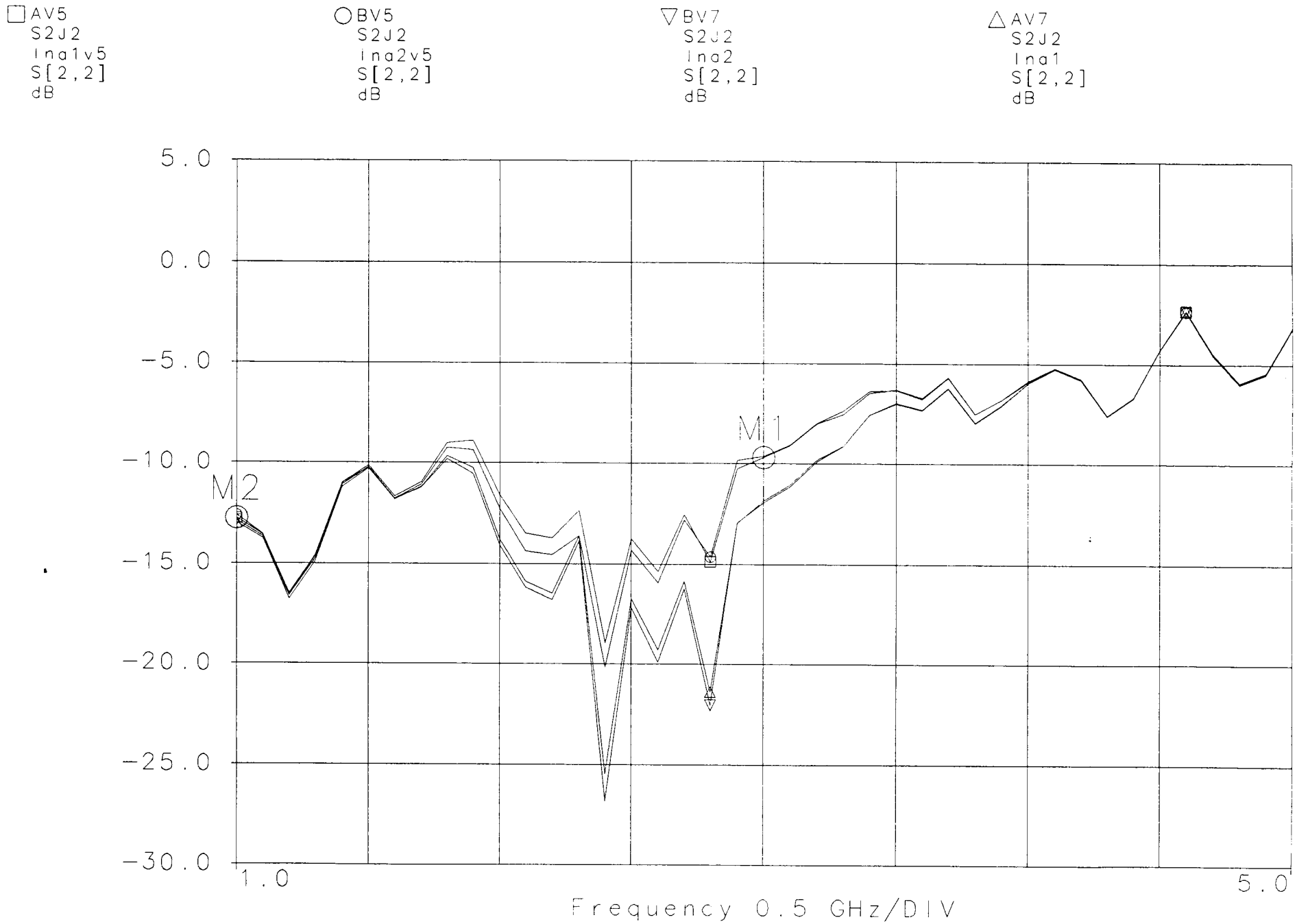
▽ AV7
S2J1
Ina1
S[2,1]
dB

△ BV7
S2J1
Ina2
S[2,1]
dB

M1 Frequency=2.40000000 value=15.9936785
M2 Frequency=2.40000000 value=8.84886787



M1 Frequency=2.10000000 value=-12.3026744
M2 Frequency=3.60000000 value=-11.7720707



M1 Frequency=3.00000000 value=-9.70618730
M2 Frequency=1.00000000 value=-12.7686380

Power Amp2 Testing Fall 96 MMIC Projects (John Cavey)
Mar 16, 1998
VG1, VG2 = -5.0V at 5.8mA per side, each supply is to 2 FETs

Part #	VD1,2	ID1,2(mA)	S21	S-parms
1	2.0	177,179	12	PAJC2I35
1	3.0	184,182	12.3	PAJC3I37
1	4.0	186,186	12.2	PAJC4I37
1	5.0	176,147	11.7	PAJC5I33

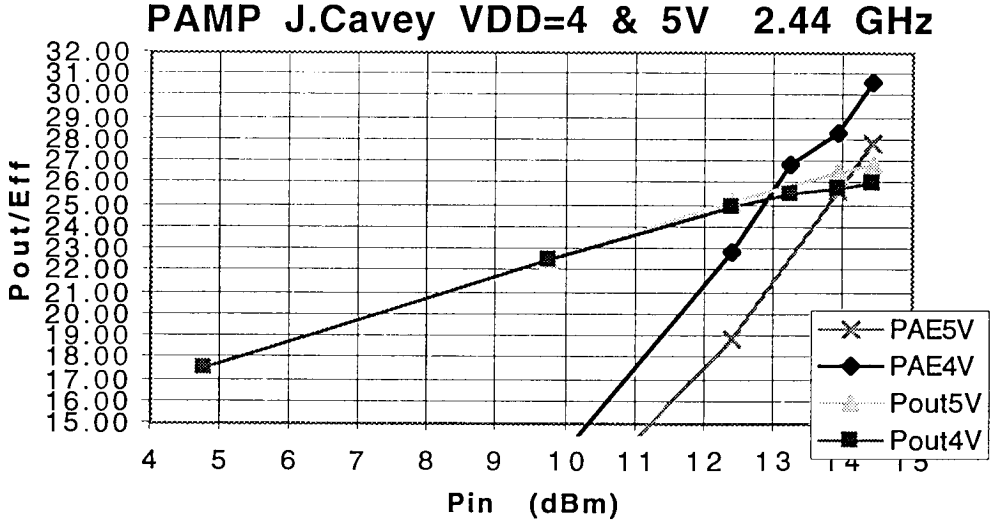
Power Measurements at 4.0V VD? did not measure losses in wiring.
Loss to Input 2.25 dB, Losses Added Output 9.75 dB Total = 12.0 dB, 2.5 dB in launches. Used Spectrum Analyzer to measure pout and signal generator to measure pin.

Pin	Pout	ID1, 2	Pin(adj)	Pout(adj)	Gain
-10	-11	183, 185	-12.25	-1.25	11.0?
0	0.8	182, 179	-2.25	10.6	12.9
10	11.5	170, 159	7.75	21.25	13.5
13.0	14.33	166, 146	10.75	24.1	13.4

Summary: The part was pretty much on frequency and we got 1/2 watt probed after attaching the die to a kovar to act as a heat sink. It was intended that the gate vias and drain bias were to be available at the top and bottom of the die but as this design was implemented the drain and gate bias at the top of the die supplies 2 of the FETs and the drain and gate bias pads at the bottom of the die supplies the other 2 FETs. Small signal measurements are attached. This device had more gain than the other power design and we calibrated at 2.44 Ghz so we were able to measure the gain compression. Unfortunately we were again limited by the input drive level of our test setup, not apparently by the part. It is just starting to compress when the 1/2 Watt level is achieved.

5.0 VD @ 326 mA; -5V gate network at 11.5 mA
2.44 GHz

Pin	Pin (corr)	Pout	Pout (corr)	Gain	ID	POUT	PDC	DRAIN EFF	PIN	PAE EFF
0	9.75	3.83	22.58	12.83	326	0.18	1.69	10.74	0.01	10.18
3	12.41	6.5	25.25	12.84	325	0.33	1.68	19.91	0.02	18.88
5	13.91	7.83	26.58	12.67	323	0.45	1.67	27.21	0.02	25.74
6	14.41	8.17	26.92	12.51	322	0.49	1.67	29.52	0.03	27.86

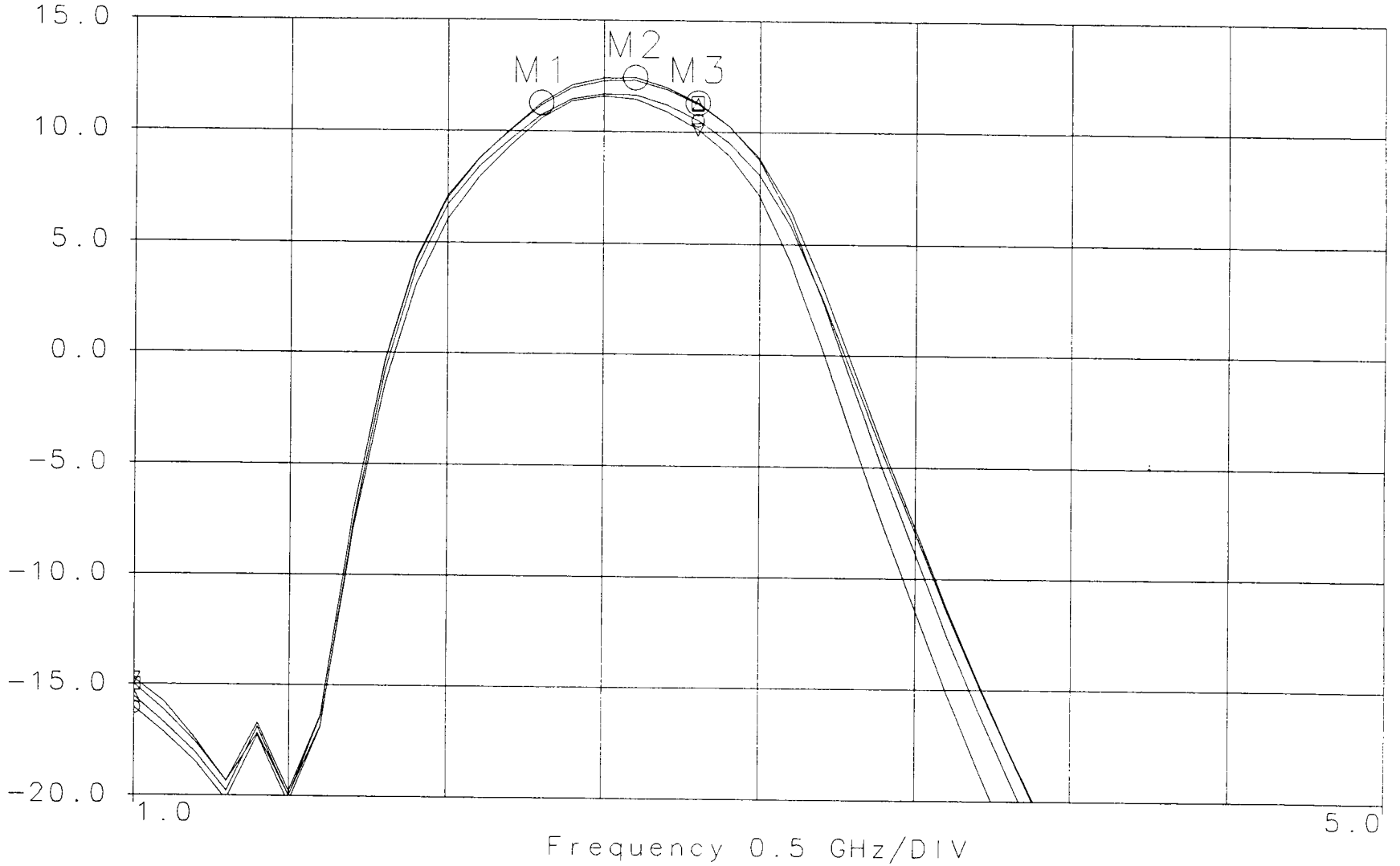


□AV3
S2J1
pajc3i37
S[2,1]
dB

○AV5
S2J1
pajc5i33
S[2,1]
dB

▽AV2
S2J1
pajc2i35
S[2,1]
dB

△AV4
S2J1
pajc4i37
S[2,1]
dB



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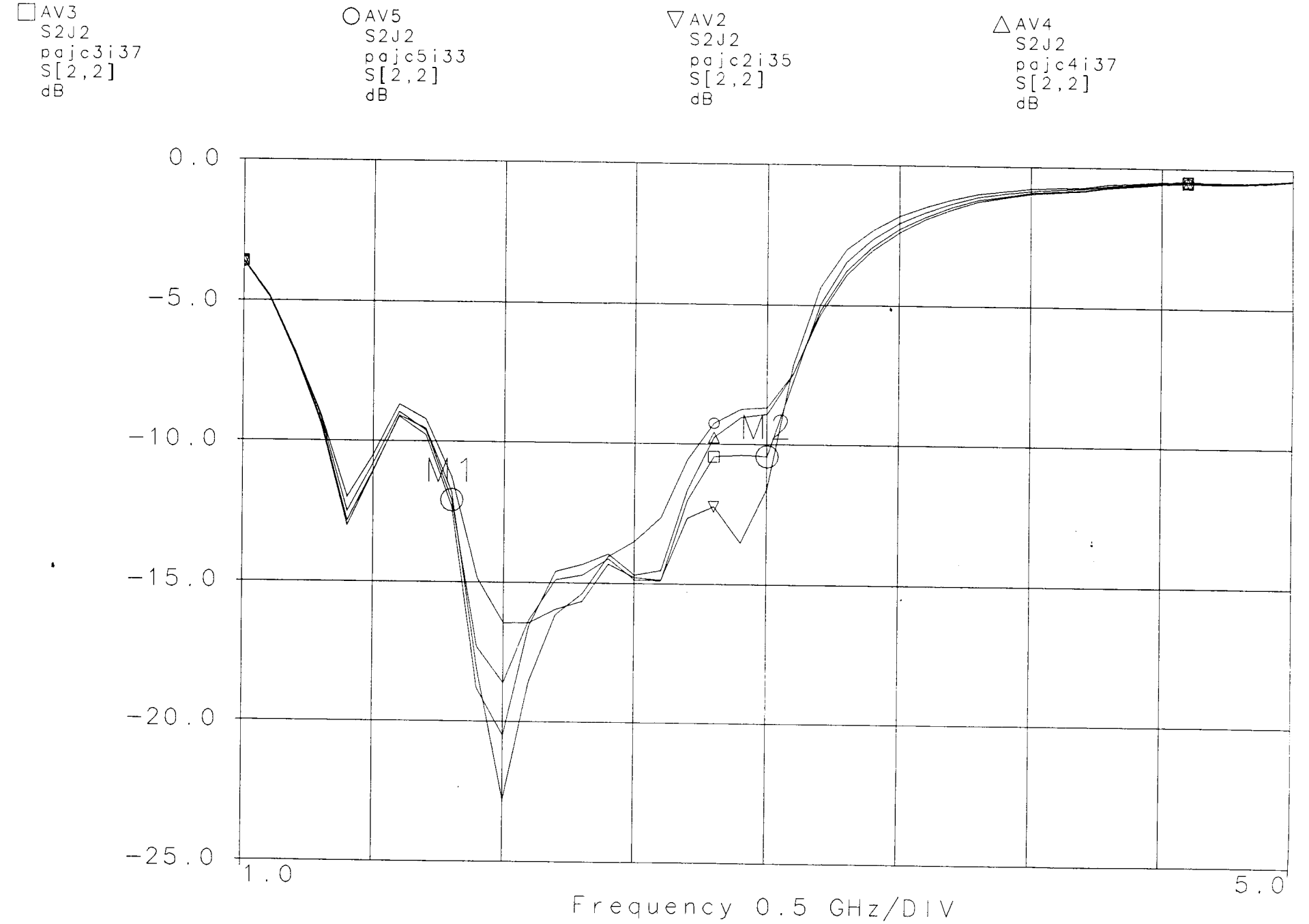
M2 Frequency=2.60000000 value=12.4382856
M3 Frequency=2.80000000 value=11.3189581



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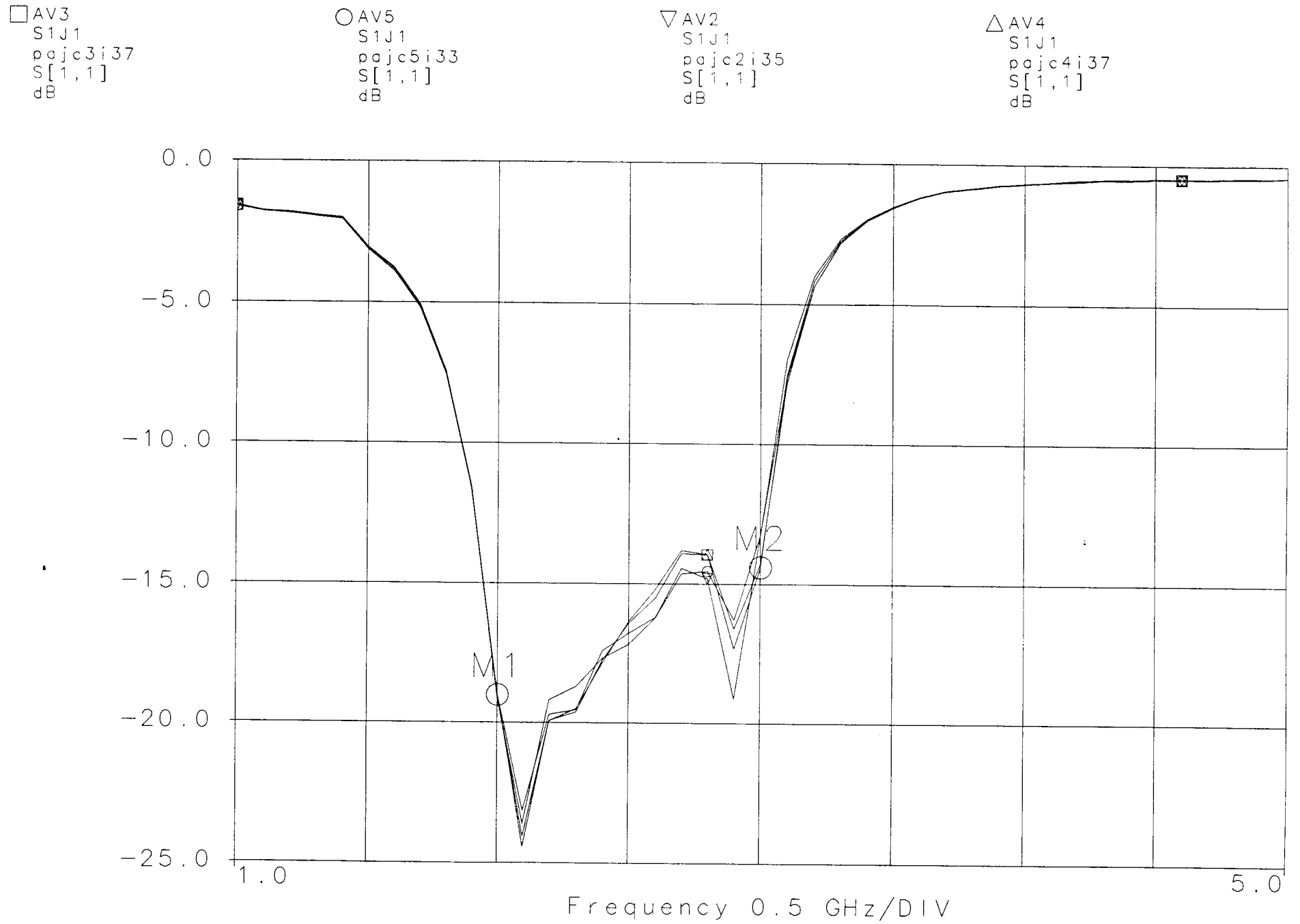

M1 Frequency=2.00000000 value=-19.0022983
M2 Frequency=3.00000000 value=-14.4095953