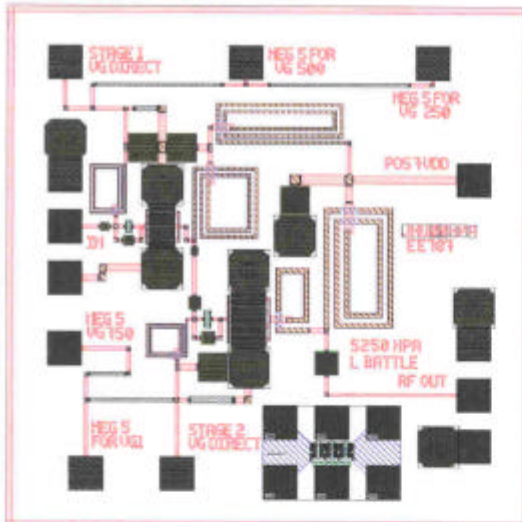


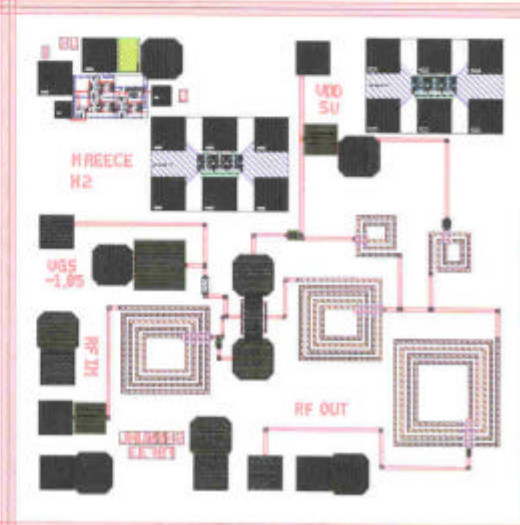
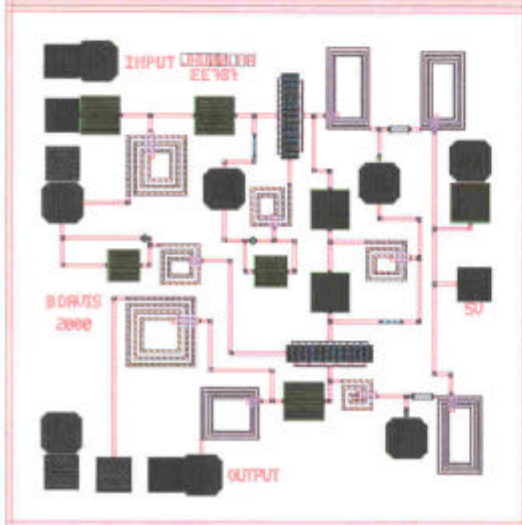
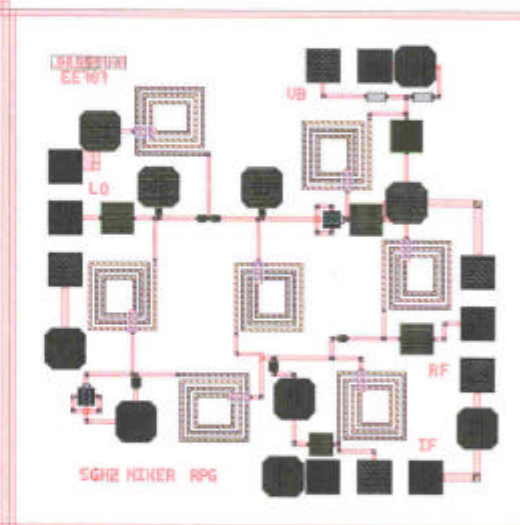
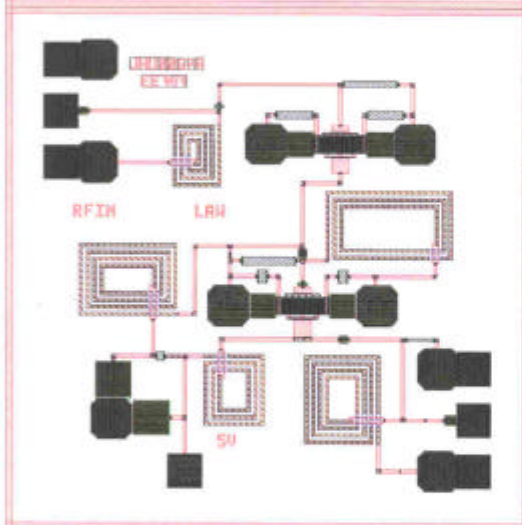
Measured Results Fall 2000 JHU MMIC Design EE787



MMIC DESIGN - JHU EE787 FALL 2000 PROJECTS

- C-BAND LOW NOISE AMP -- B. DAVIS
- C-BAND GEN PURPOSE AMP -- L. WALKER
- C-BAND HIGH POWER AMP -- L. BATTLE
- C-BAND UP/DOWN MIXER -- R. GABANY
- C-BAND FREQUENCY DOUBLER -- M. REECE

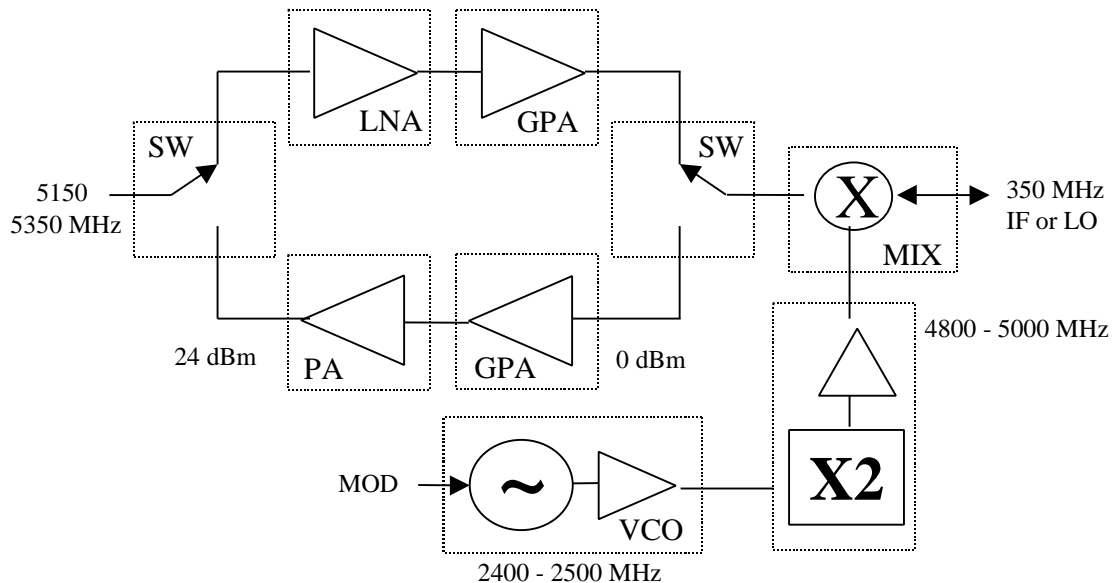
SUPPORT FROM TRIQUINT AND AGILENT



JHU EE787 MMIC Design Course
MMIC Test Measurements – Fall 2000
Measured May-July 2001
Craig Moore and John Penn
July 23, 2001

This is to summarize the recent testing of the MMIC designs from the Fall 2000 JHU MMIC Design Course #787. Following is the description of the system project for the class designs.

MMIC DESIGN (EE 787) FALL '00 PROJECT

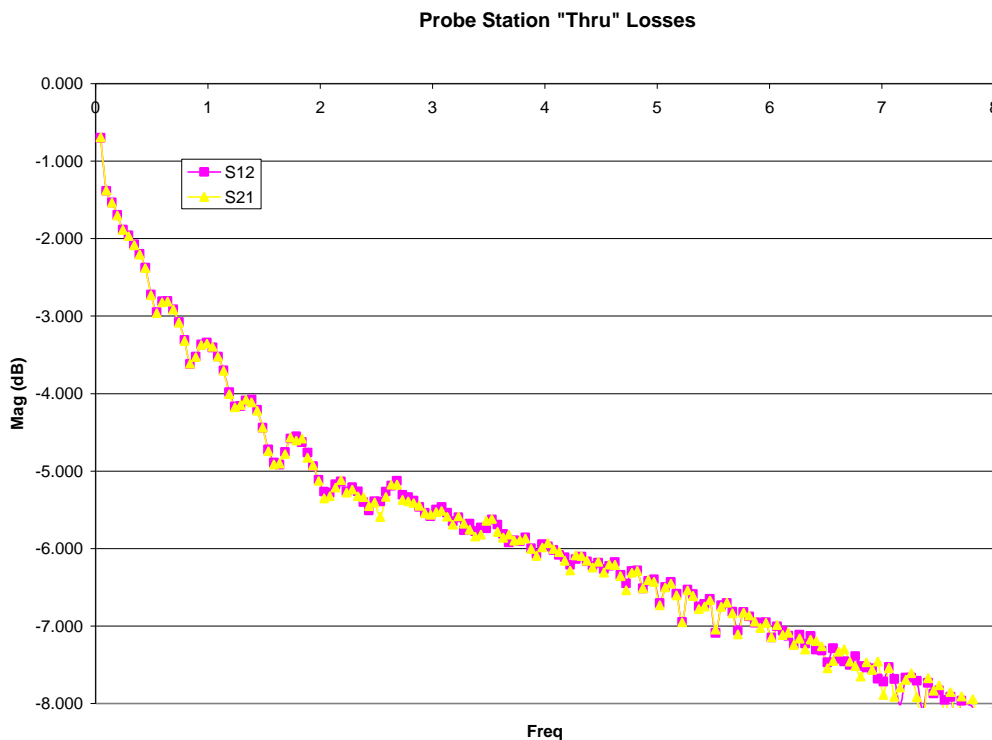


WLAN for 5150 - 5350 MHz HYPERLAN BAND

This year's project for the MMIC Design class at The Johns Hopkins University is a simplex transceiver for the C-band HYPERLAN wireless local area network (WLAN) frequencies. The up-down conversion scheme uses a C-band frequency converter, which produces a 350 MHz IF signal that can be down converted to baseband with a 350 MHz second LO. The second LO is upconverted to C-band in the transmit mode. Modulation can be introduced onto the second LO or by direct frequency modulation of the VCO in the transceiver. The up-down converter consists of a mixer, VCO, and frequency doubler. The VCO operates from 2.4 to 2.5 GHz, which is in the industrial, scientific, and industrial (ISM) band. Thus, the VCO has dual band usage. C-band SPDT switches are employed to route the receive and transmit signals appropriately. The receive chain consists of an LNA and a general purpose amplifier (GPA) in cascade. The transmit path employs the same GPA driving a ¼ watt power amplifier. Seven unique MMIC designs make up the nine chip C-band transceiver. Each design is to be contained on a 60 mil square die in the TQS TRx process. The proposed block diagram is shown above.

Summary of Testing:

An HP 8510 NWA was used to measure s-parameters for the MMICs using a Cascade Probe Station and Microwave Probes over the range 45 MHz to 10 GHz. Additional measurements were made with signal generators and a spectrum analyzer. Power measurements were made with the spectrum analyzer. A “through” measurement was made of the cables, DC bias blocks, and Probes. Half the total loss at the appropriate frequency was used to de-embed the spectrum analyzer measurements. For instance for measurements made with the frequency doubler at 2.5 GHz, input losses would be based on half the “through” measurement at 2.5 GHz, and output losses would be based on half the “through” measurement at 5.0 GHz. The NWA analyzer calibration appears to be adequate but not great. Possibly the Microwave probes being used are worn, and the ISS probe standard is several years old and worn also. Measurements of S11 and S21 seem reasonable but S22 measurements are not as good with errors increasing above 6 GHz. All the five MMICs worked fairly well and some additional measurements were made on a 300 um DFET and a 300 um GFET which were added as test structures on a couple of the student projects.



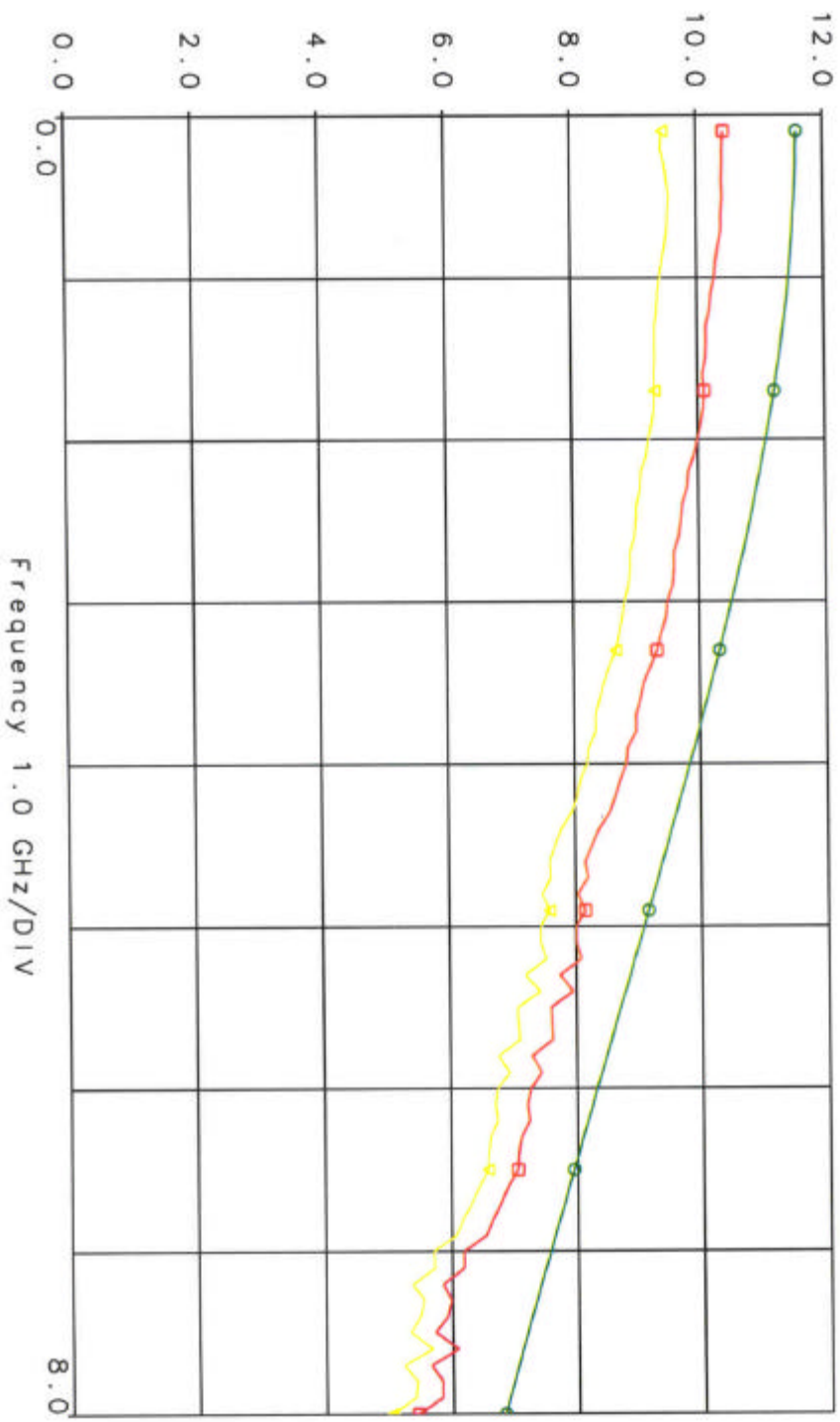
FET testing (7/23/01):

Measured results of the DFET and GFET appear reasonably close to expected levels for S11 and S21. Errors in S22 increase with frequency and are suspect. The GFET S21 gain appears closer to expected levels than say the DFET S21 gain. Since gain is a variable that changes considerably from wafer run to wafer run, it's possible that this batch was a little low in gain for DFETs. DFETs were used in the LNA design and its measured gain of 6 dB was lower than its expected gain of 10 dB from the simulations. All the designs appeared to be on target for bias and gain was pretty close for the remaining two amplifiers designs and frequency doubler that used GFETs. The mixer design used DFETs as diodes and its measured results matched well with expectations. Following are plots of the s-parameters for measured DFETs at 2V VDS and -0.2V and -0.4V VGS versus the nominal model at -0.2V VGS. Also the GFETs are measured at 5V VDS and -0.8V and -1.25V VGS versus a nominal model at 5V VDS and about -0.8V VGS.

□ fet_meas_1b
S2J1
qfet108v5
S[2.1]
dB

○ fet_s_1b
S2J1
qfet300
S[2.1]
dB

△ fet_meas2_1b
S2J1
qfet112v5
S[2.1]
dB

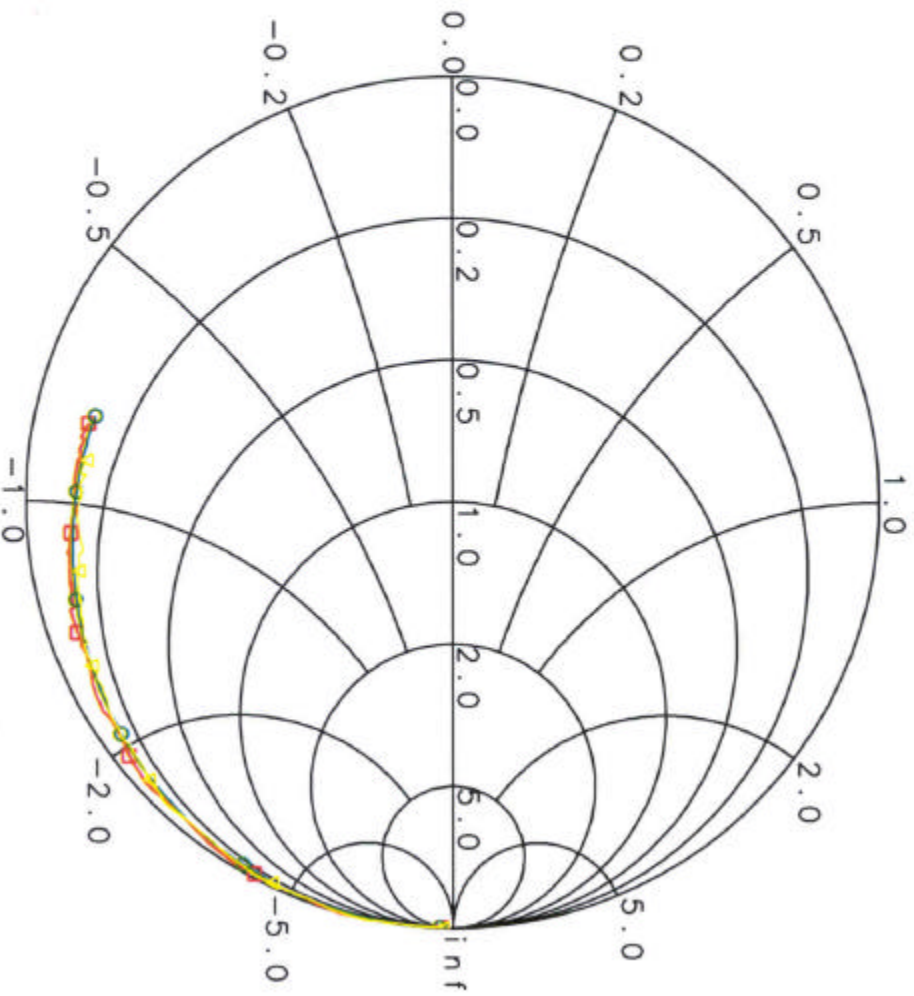


GFETS FALL 2000 MMIC Class--Meas. Vs. Model

□ fet_meas_1b
SIJ1
gfe108v5
S[1,1]

○ fet_s_1b
SIJ1
gfe1300
S[1,1]

△ fet_meas2_1b
SIJ1
gfe112v5
S[1,1]

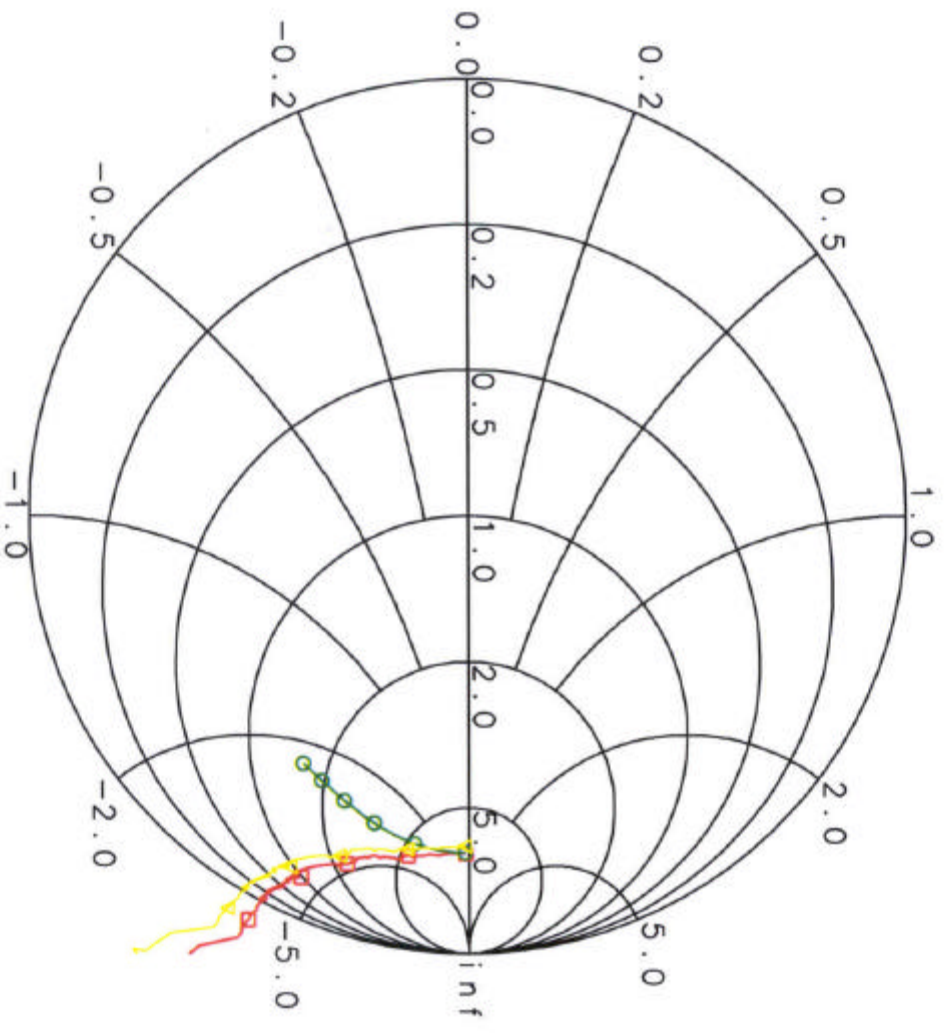


Frequency 0.1 to 8.0 GHz
GFETS FALL 2000 MMIC Class--Meas. Vs. Model

□ fet_meas_1b
S2J2
gfet08v5
S[2.2]

○ fet_s_1b
S2J2
gfet1300
S[2.2]

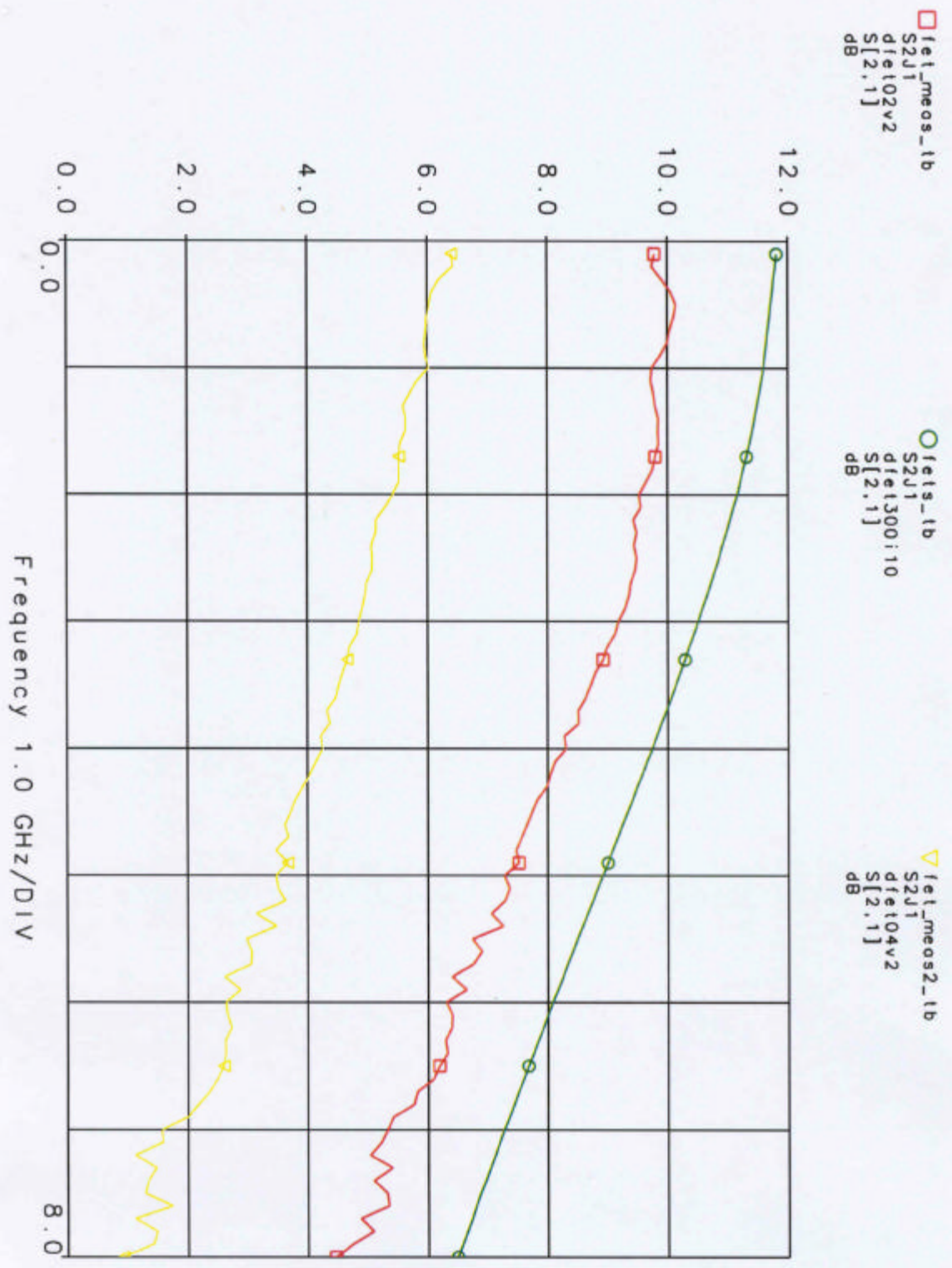
△ fet_meas2_1b
S2J2
gfet12v5
S[2.2]



Frequency 0.1 to 8.0 GHz

GFETS FALL 2000 MMIC Class--Meas Vs. Model

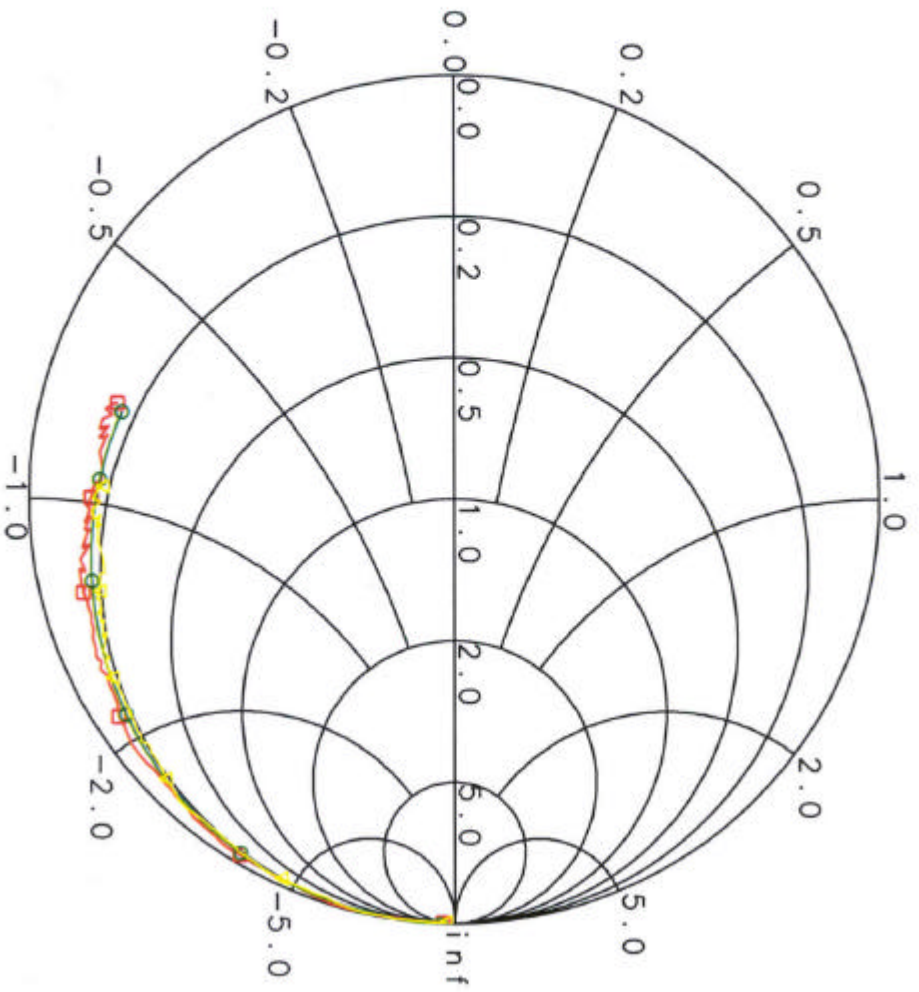
DFETS FALL 2000 MMIC Class--Meas. Vs. Model



□ fet_meas_1.tb
SIJT
dfe102v2
S[1,1]

○ fet_s_1.tb
SIJT
dfe1300i10
S[1,1]

△ fet_meas2_1.tb
SIJT
dfe104v2
S[1,1]

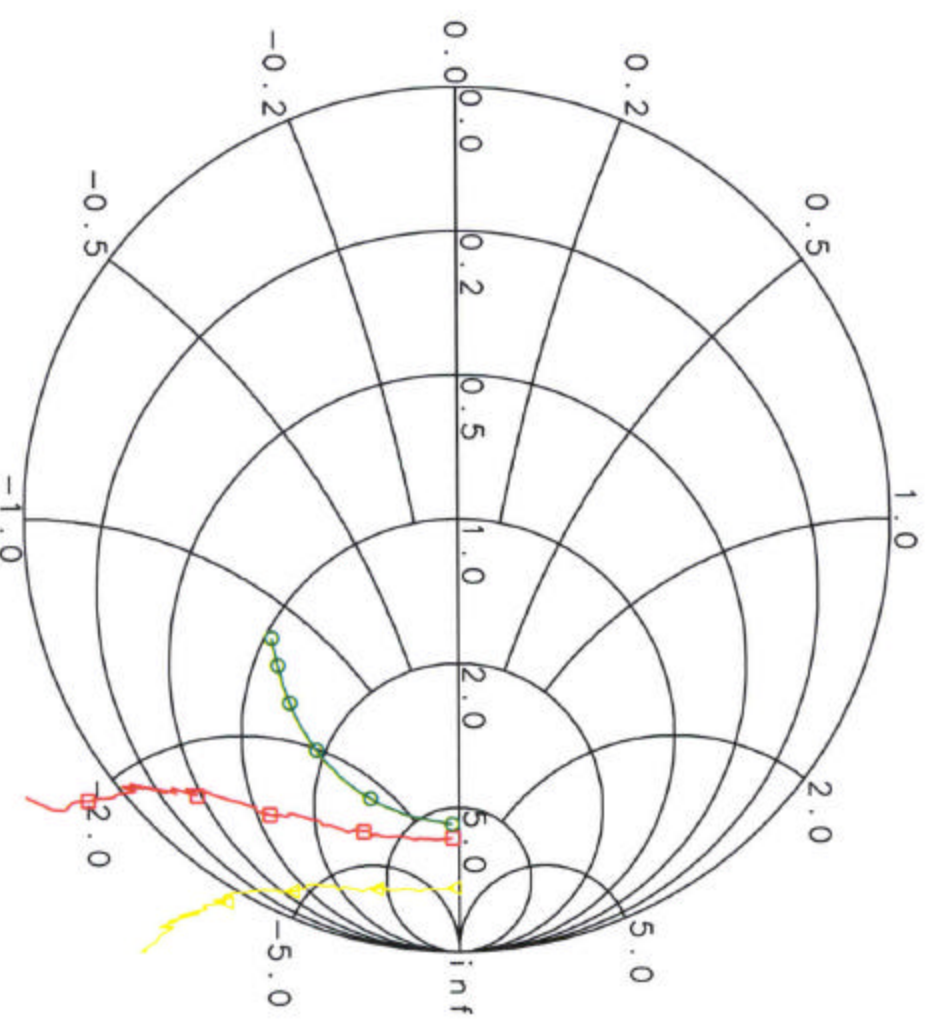


Frequency 0.1 to 8.0 GHz
DFETs FALL 2000 MMIC CLASS--Meas. Vs. Model

□ fet_meas_1b
S2J2
dfe102v2
S[2.2]

○ fet_s_1b
S2J2
dfe1300i10
S[2.2]

△ fet_meas2_1b
S2J2
dfe104v2
S[2.2]



Frequency 0.1 to 8.0 GHz

DFETS FALL 2000 MMIC Class--Meas Vs. Model

Notes From Doubler, Low Noise Amplifier, and Medium Power Amplifier Designs (5/30/01):

This is some preliminary data from [5/29/01] measurements. Three of the five designs were measured--the doubler, the low noise amplifier, and the medium power amplifier. At first glance, biases were very close to what we expected. LNA was 5.0V at 39-40 mA, expected to be 41.2 mA. GPA was 5.0V at 59-60 mA, expected to be 64 mA. Considering that both these designs were single supply biases using resistors to set the bias current, this is exceptional. The two things that seem to vary most with processing are threshold voltage and gain (S21). The threshold variance tends to have an exponential effect on the bias current of single supply bias designs so I'm guessing that threshold voltages for our last run are pretty nominal. For the doubler, the gate was at -1.85V (near GFET pinchoff), so the drain current was a mere 1-2mA until driven hard (~9-10 dBm) which increased the drain current to 7 or 8 mA. Unfortunately we had some low frequency oscillations with the doubler (~17MHz) in spite of the near pinchoff bias. Tried to add some additional capacitance at the bias supplies to damp out the low frequency oscillation but had to decrease the drain voltage from the desired 5V to 1.0V to 1.5V for the measurements. Possibly bonding to a 100 pF decoupling capacitor on the bias lines would allow the doubler to be probe tested at the full 5V without oscillations. At any rate, the doubler did double with about 10 dB conversion loss at 1.5 V on the drain, and 12 dB conversion loss at 1.0V on the drain.

LNA was a bit low on gain, maybe 6 to 6.5 dB versus the expected 10 dB gain but otherwise looked good in terms of gain shape and input/output match. GPA had 13-14 dB of gain versus a predicted 15.5 dB at 5.25 GHz. Output power for the GPA was about 16 dBm as predicted. For the LNA, a noise figure measurement was attempted trying to factor out about 6.5 dB of losses in the probe station, bias tees, probe heads, and cables. This would put the NF around 3.0 dB at 5.0 GHz versus an expected NF of 2.1 dB. Possibly we can remeasure this data at some point calibrating with a thru at the probe heads.

Measurement data was a little noisy. Couple of possibilities are the worn calibration ISS standards and worn probe heads. Data appears reasonably good though. Following are some spreadsheet calculations of NF of the LNA, Pout of the GPA, and Conversion Loss of the Doubler.

Additional Measurements:

LNA		Meas.		Calculated		
Freq (GHz)	NF	Gain	Loss Thru	Est. NF	Est. Gain	
5.00	6.36	-0.13	6.71	3.01	6.58	
5.10	6.64	0.20	6.44	3.42	6.64	
5.20	7.18	-0.64	6.95	3.71	6.31	
5.30	7.17	-0.29	6.60	3.87	6.31	
5.40	7.18	-0.66	6.72	3.82	6.06	
5.50	7.28	-1.20	7.08	3.74	5.88	

GPA		"@5.25 GHz"				
S/G In	Meas. PO	Pin (Est.)	Pout Est.	Gain	Comp.	
-20.00	-13.17	-23.27	-9.90	13.37		
-15.00	-8.17	-18.27	-4.90	13.37	0.00	
-10.00	-3.17	-13.27	0.10	13.37	0.00	
-8.00	-1.50	-11.27	1.77	13.04	-0.33	
-6.00	0.67	-9.27	3.94	13.21	-0.16	
-4.00	2.67	-7.27	5.94	13.21	-0.16	
-2.00	4.67	-5.27	7.94	13.21	-0.16	
0.00	6.67	-3.27	9.94	13.21	-0.16	
2.00	8.50	-1.27	11.77	13.04	-0.33	
4.00	10.50	0.73	13.77	13.04	-0.33	
6.00	12.00	2.73	15.27	12.54	-0.83	
8.00	12.83	4.73	16.10	11.37	-2.00	
10.00	13.30	6.73	16.57	9.84	-3.53	

X2 "@2.3 GHz VD=1.5V, 7mA"
 S/G In Meas. PO Est. Pin Est. Pout Conv. Loss
 12 -3.5 9.35 -0.4 9.75

X2 "@2.45 GHz VD=1.0V, 8mA"
 S/G In Meas. PO Est. Pin Est. Pout Conv. Loss
 12 -6.17 9.25 -2.97 12.22

Note: See later doubler measurements with additional decoupling capacitors to damp out oscillations.

Notes From Mixer Design (6/7/01):

We tested the Mixer MMIC last Friday and it worked well. The only bias voltage was a forward bias on the FET diodes through a resistor divider chain at 2.8V. The match improved dramatically on the network analyzer when bias was applied--a good sign. Some network analyzer measurements were made from LO to IF and RF to IF with the third probe port terminated in 50 ohms. Since the DC bias probe was needed on the IF port, measurements were not made between RF and LO. After network analyzer measurements were made of two separate and virtually identical die, two signal generators were used with a spectrum analyzer to test the up and down conversion. LO was set to 4.9 GHz at ~+10 dBm, IF was 350 MHz and RF was 5.25 GHz. The signal generator for the RF (down conversion) and IF (up conversion) was set to -15 dBm, so the actual drive level depended on cable losses etc. Based on previous measurements of the cables, DC bias block, and probe heads, thru losses are about 2.1 dB at 350 MHz, 6.4 dB at 4.9 GHz and 6.7 dB at 5.25 GHz. Losses for one cable, DC bias block, and probe head are assumed to be half of that amount. Using these values...

MIXER "@2.8V, 17 mA"

Down Conversion (2.8VIF 350 MHz		IN: LO 4.9 GHz	IN: RF 5.25 GHz	LO on IF 4.9 GHz	RF on IF 5.25 GHz
As measured	-28.5 dBm	+13 dBm	-15 dBm	-33.67 dBm	-44.0 dBm
Corrected (at MMIC)	-27.5 dBm	+9.8 dBm	-18.3 dBm	-30.5 dBm	-40.7 dBm

Calculated Conversion Loss (-18.3 to -27.5) = 9.2 dB
 LO to IF rejection (+9.8 to -30.5) = 40.3 dB
 RF to IF rejection (-18.3 to -40.7) = 22.4 dB

UP Conversion (2.8V)	IN: IF 350 MHz	IN: LO 4.9 GHz	RF 5.25(4.65) GHz	LO on RF 4.9 GHz	IF on RF 350 MHz
As measured	-15 dBm	+13 dBm	-26.33 dBm	-19.17 dBm	-62.17 dBm
Corrected (at MMIC)	-16 dBm	+9.8 dBm	-23 dBm	-16 dBm	-61 dBm

Calculated Conversion Loss (-16 to -23) = 7 dB
 LO to RF rejection (+9.8 to -16) = 25.8 dB
 IF to RF rejection (-16 to -61) = 45 dB

Notes From High Power Amplifier Design (6/13/01):

Tested the Power Amplifier MMIC from the Fall's JHU MMIC Design Course fabricated by TriQuint. As with many power amplifier designs, there was some marginal low frequency stability issues with the probe testing. Some additional capacitance closer to the device would presumably damp out these oscillations. For s-parameter measurements, the drain voltage was limited to 3.5V and 4V for the parts tested to avoid the oscillation problem. Design voltage was 7.0V at about 225 mA. We also did some power measurements with a signal generator and a spectrum analyzer and I [later] realized that there was a fair amount of DC power dissipation for that small 54x54 mil die. I think the part was probably running pretty hot so the actual performance mounted could be better--closer to predictions, and it would be easier to mount some 0.01 uF caps closer to the part to subdue the low frequency oscillations too. At some point, it would be nice to re-measure our frequency doubler design from this past fall's class again with some capacitors mounted closer to the part because it also exhibited some low frequency instability which we damped out by limiting the drain voltage [see later meas.]. In the past we have probe tested a JHU MMIC class power amplifier with 0.8W of output power (29 dBm) at 3.2W of DC power on the small 54x54 mil die. For that test, we die attached the MMIC to a small kovar piece of metal to dissipate heat. I think we should probably do the same for any part this size with more than 1W DC power consumption such as this Fall's Power MMIC. Measured performance was 24 dBm versus an expected 25 dBm but the current consumption was considerably lower than expected. I now think that the current drop as the drain voltage was increased on this part was due to poor thermal conduction of the more than 1W DC power supplied. At any rate, the part worked well but I suspect it's actual performance to be closer to design simulations. During power testing we were able to increase the drain to about 5.5V and made measurements without the stability problem. Then with RF drive supplied near compression we increased the drain voltage to 7.0V and made more measurements. The part was stable until RF drive was removed and we again saw the low frequency oscillations. Gain of the part was about 20 dB and worked well.

HPA Some Slight Low Frequency Stability Problems S-parameter Meas.
"#1 Drain 3.5V @ 190 mA, -5V @ 1.28 mA (VG1=-0.25V), -5V @ 2.5 mA (VG2=-0.75V)"
"#2 Drain 3.5V @ 199 mA, -5V @ 1.3 mA (VG1=-0.25V), -5V @ 2.6 mA (VG2=-0.75V)"
"#2 Drain 4.0V @ 192 mA, -5V @ 1.3 mA (VG1=-0.25V), -5V @ 2.6 mA (VG2=-0.75V)"
Power Meas. 5.5V, 178 mA--no stability problems, then 7V OK stability 5.25 GHz source (6.7 dB loss thru)

Sig Gen	Pms 5.5V	Pms 7.0V	Pin (corr)	Pout 5.5V	Pout 7.0V
-10	1.10		-13.35	4.45	
-8	3.10		-11.35	6.45	
-6	5.10		-9.35	8.45	
-4	7.10		-7.35	10.45	
-2	9.27		-5.35	12.62	
0	11.43	10.17	-3.35	14.78	13.52
2	13.43	12.33	-1.35	16.78	15.68
4	15.60	14.67	0.65	18.95	18.02
6	17.27	17.00	2.65	20.62	20.35
7	17.93	18.00	3.65	21.28	21.35
8	18.43	18.83	4.65	21.78	22.18
9	18.77	19.67	5.65	22.12	23.02
10	18.93	19.77	6.65	22.28	23.12
11		20.33	7.65		23.68
12		20.50	8.65		23.85

Notes From Doubler Re-Test and DFET and GFET Testing (7/20/01):

Put some 0.1 uF capacitors at the DC bias probes in attempt to remove the low frequency oscillations that were prevalent in the previous "probed" measurements. The several MHz oscillations were removed at the higher drain biases leading to a successful test at the desired 5V drain operation. Measurements were also taken at 2V initially. Actual losses were similar to previous measurements taken at 1.5V on the drain, but the input and output match is improved and closer to the expected results at the intended bias of VGS=-1.85V and VDS=5V.

**Remeasured X2 with 0.1 uF caps next to DC probes--
killed low frequency oscillations. 7/20/01**

X2 "@2.5 GHz VD=2.0V, 11mA"

S/G In	Meas. PO	Est. Pin	Est. Pout	Conv. Loss
12	-3.67	9.3	-0.42	9.72

X2 "@2.5 GHz VD=5.0V, 16mA"

S/G In	Meas. PO	Est. Pin	Est. Pout	Conv. Loss
12	-3.50	9.30	-0.25	9.55
11	-4.17	8.30	-0.92	9.22
10	-5.33	7.30	-2.08	9.38
9	-6.67	6.30	-3.42	9.72
8	-8.00	5.30	-4.75	10.05
7	-9.33	4.30	-6.08	10.38
6	-10.83	3.30	-7.58	10.88
5	-12.33	2.30	-9.08	11.38
4	-14.00	1.30	-10.75	12.05
3	-15.83	0.30	-12.58	12.88
2	-17.67	-0.70	-14.42	13.72

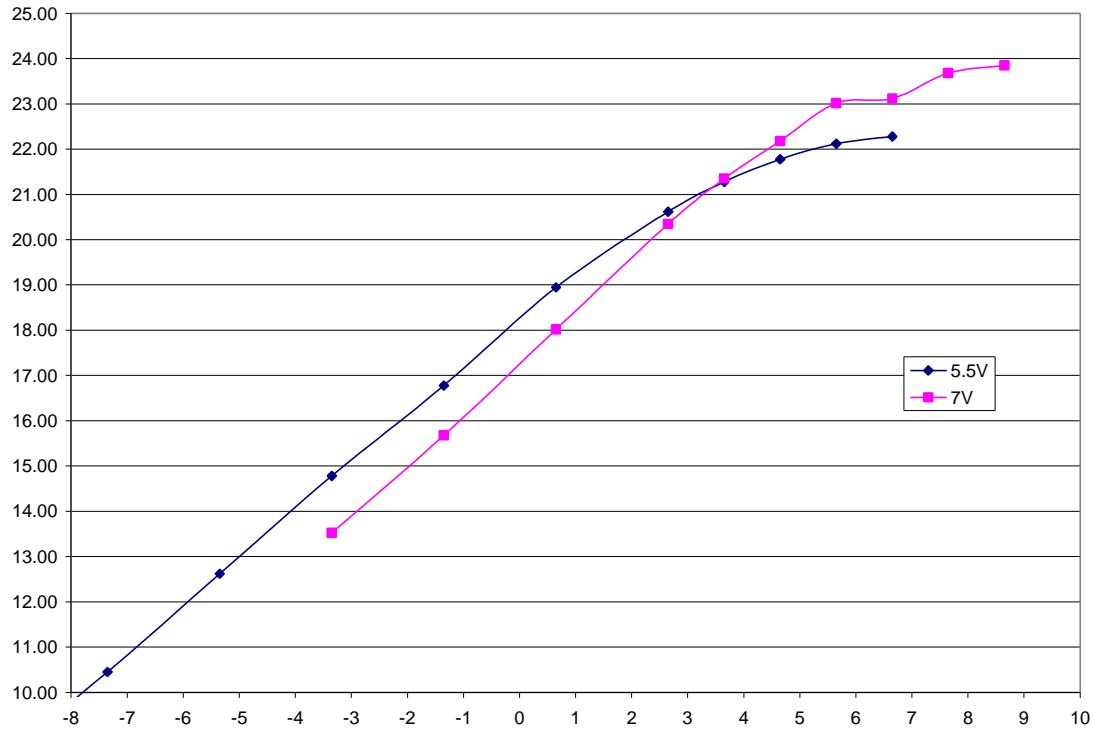
Summary of Fall 2000 MMICs:

The MMICs designed in the fall 2000 class of JHU's MMIC Design Course EE787 were very successful. Small signal s-parameter measurements were made along with some additional measurements for power, noise figure, non-linear mixing, etc. As is typical with probe testing, there were some issues with low frequency oscillations on the doubler and the high power amplifier which were overcome by applying some additional off-chip capacitance near the DC supplies to the MMIC chips. The performance of the high power amplifier was probably limited by the high DC power consumption without sufficient heat sinking during the probe measurements. This part probably should have been silver expoxied to a small piece of kovar or metal to improve the thermal path for this part during probe testing. Bias and performance for the parts were very similar to expected results from the simulations. Possibly gain was a little low but within normal deviations particularly for the DFETs used in the LNA. Measurements of individual test DFETs and GFETs included on the student designs are attached.

Thanks especially to TriQuint for fabricating the student chips and to Agilent EEsof for the library created by Gary Wray and for the ADS software. Attached following are some plots of the s-parameters and other measurements for the various MMIC designs. For additional information, see the student project reports.

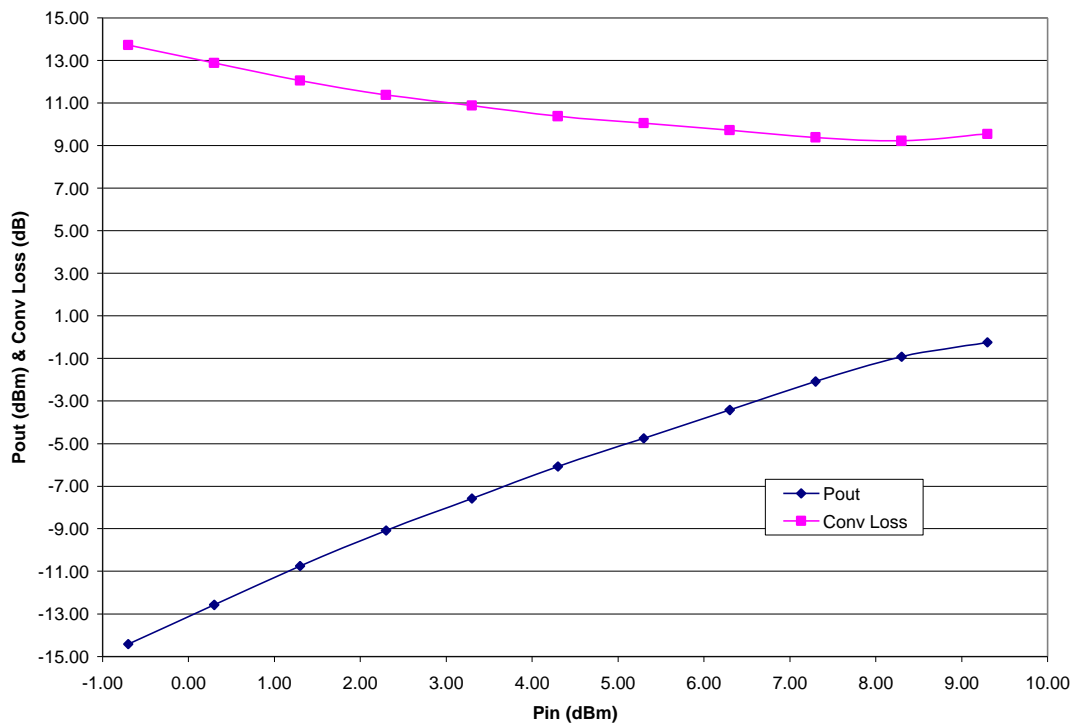
Power Out Vs. Power In of High Power Amp (7V and 5.5V VDS, 5.25 GHz)

Pout vs. Pin (5.5V & 7V) HPA



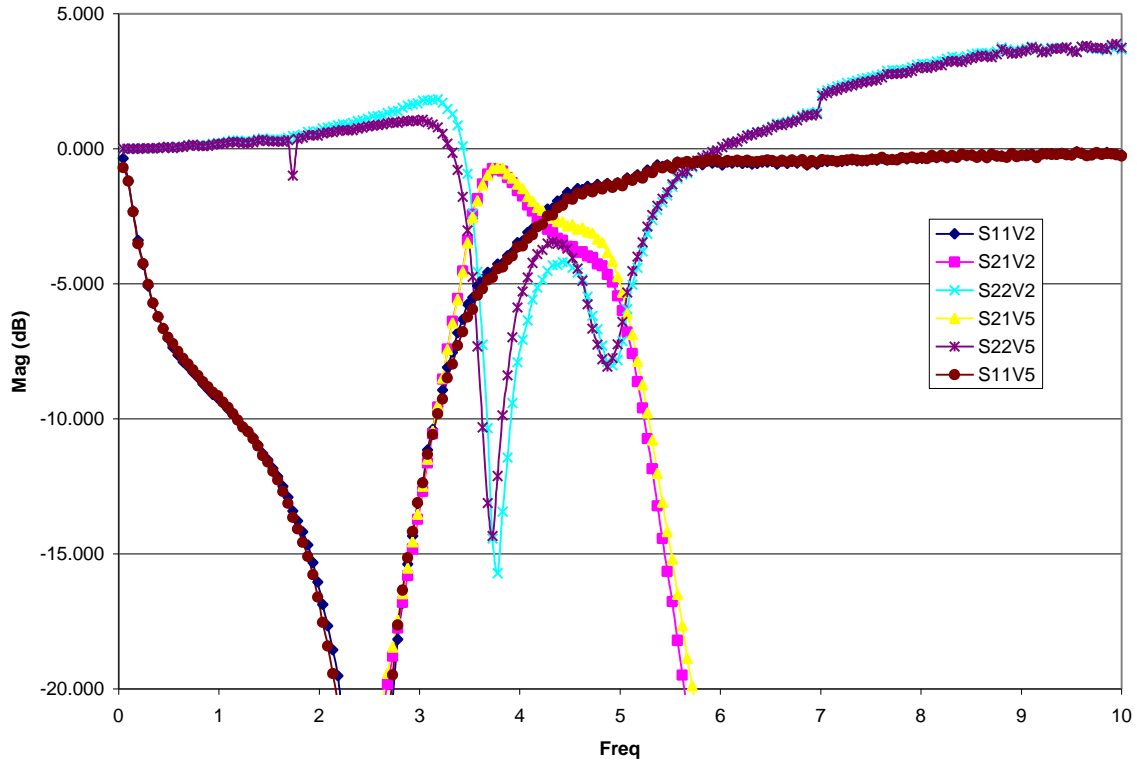
Conversion Loss and Power Out Vs. Power In Doubler (5V VDS, 2.5 GHz)

X2 (5V @ 16 mA)



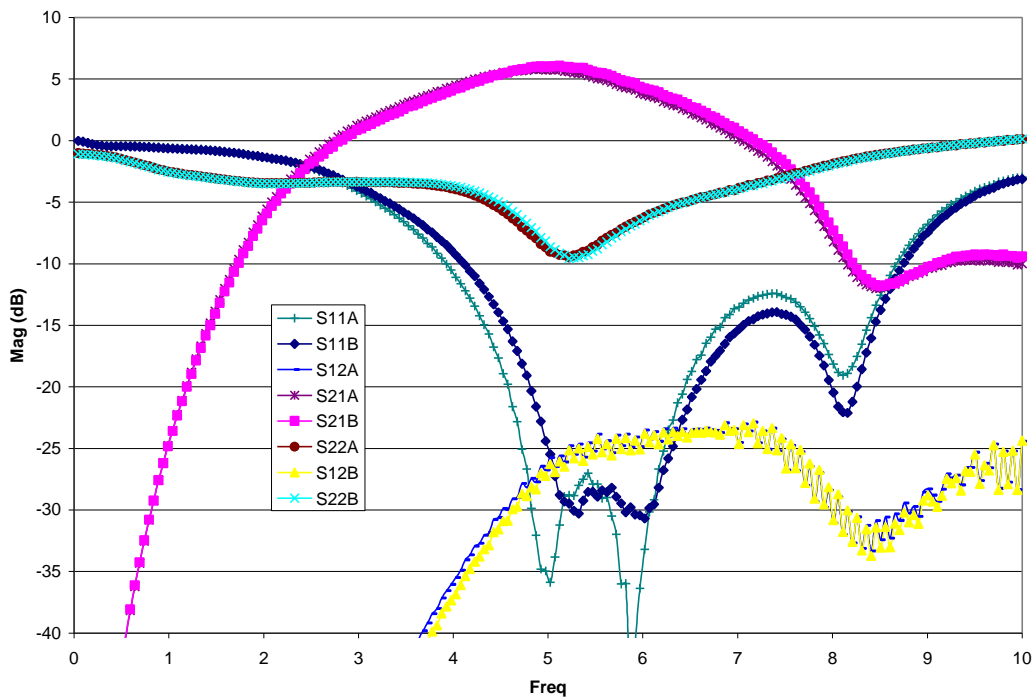
S-Parameters for Doubler (2V and 5V VDS)

X2 Doubler S-Parameters (2V @ 11 mA, V5 @ 16 mA)



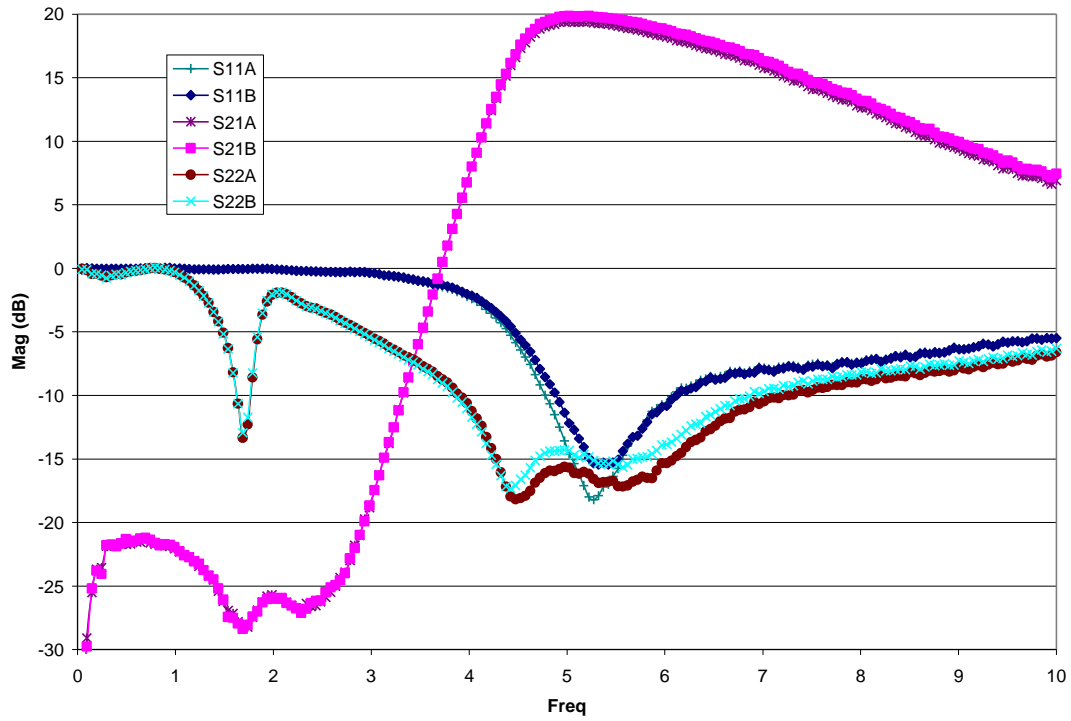
S-Parameters Low Noise Amplifier (5V Single Supply—2 die)

LNA2 & 1



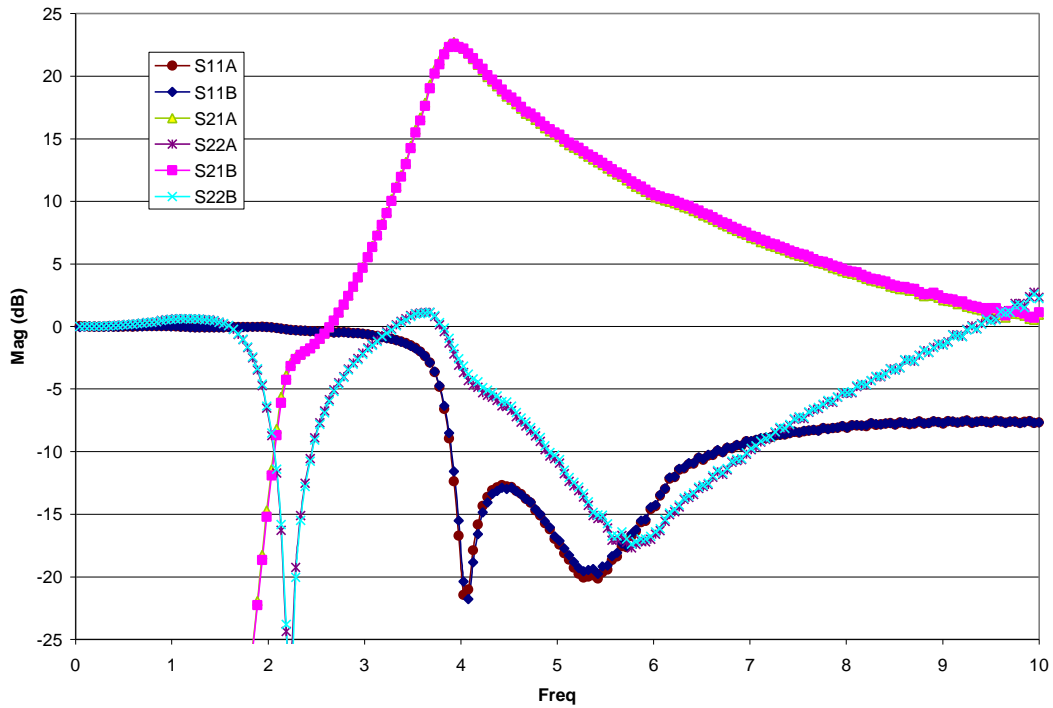
High Power Amplifier (~4V VDS—2 die)

HPA2 & 1

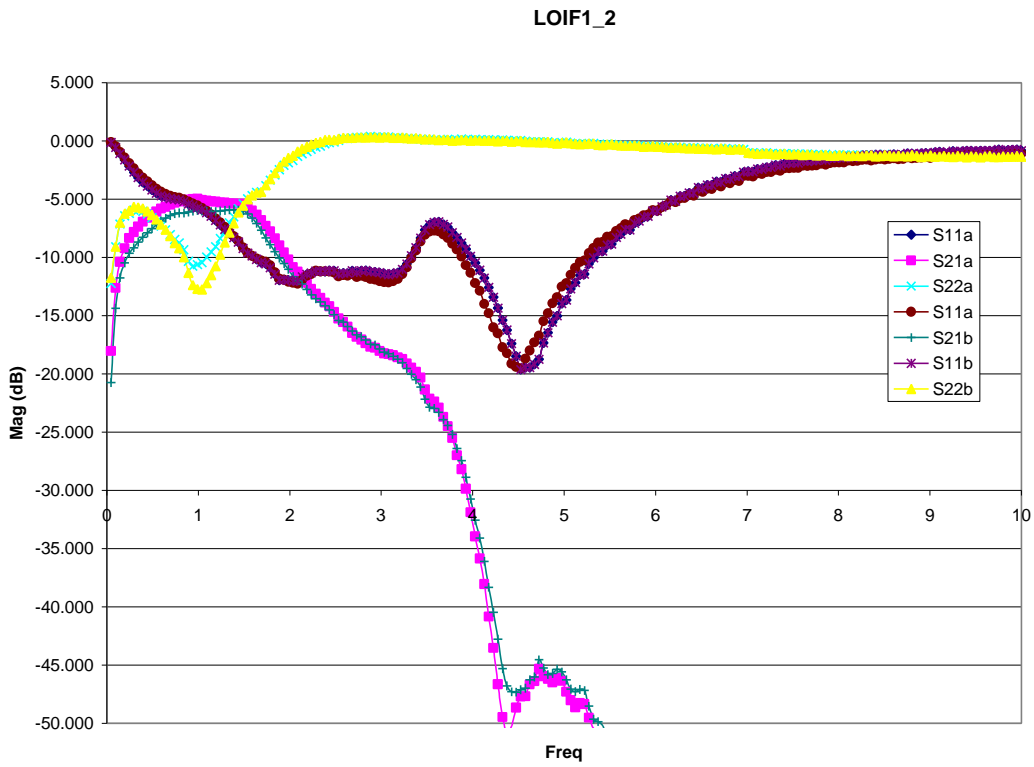


Medium Power Amplifier (5V VDS Single Supply—2 die)

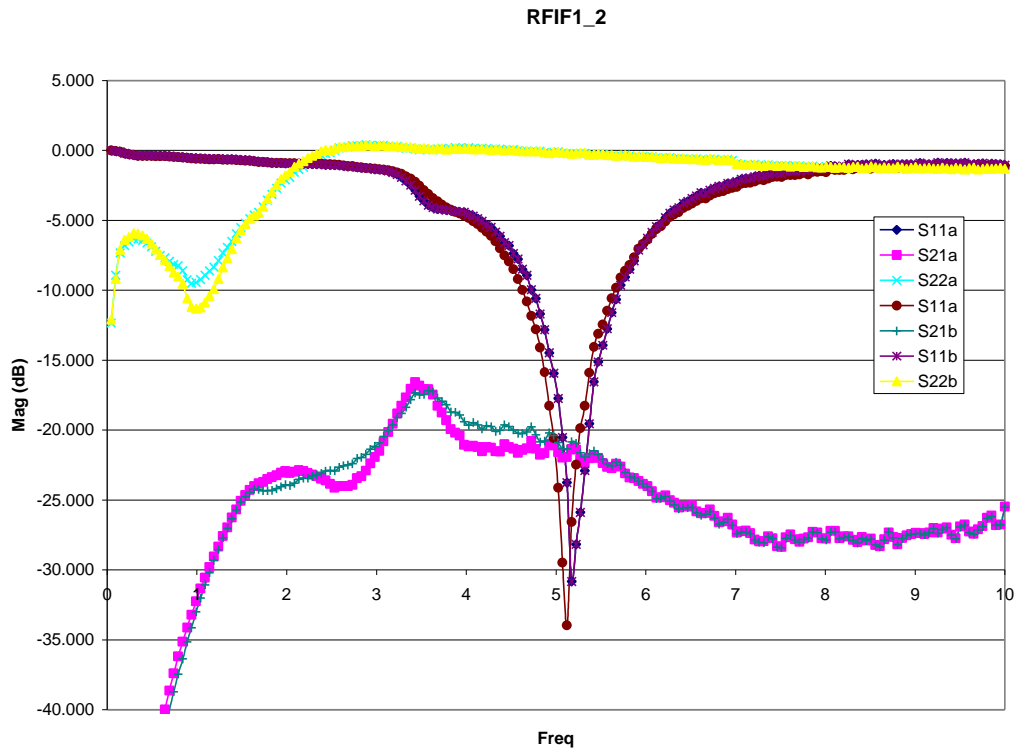
GPA2 & 1 S-Parameters



Mixer LO to IF Measurements (2.8V—2 die)

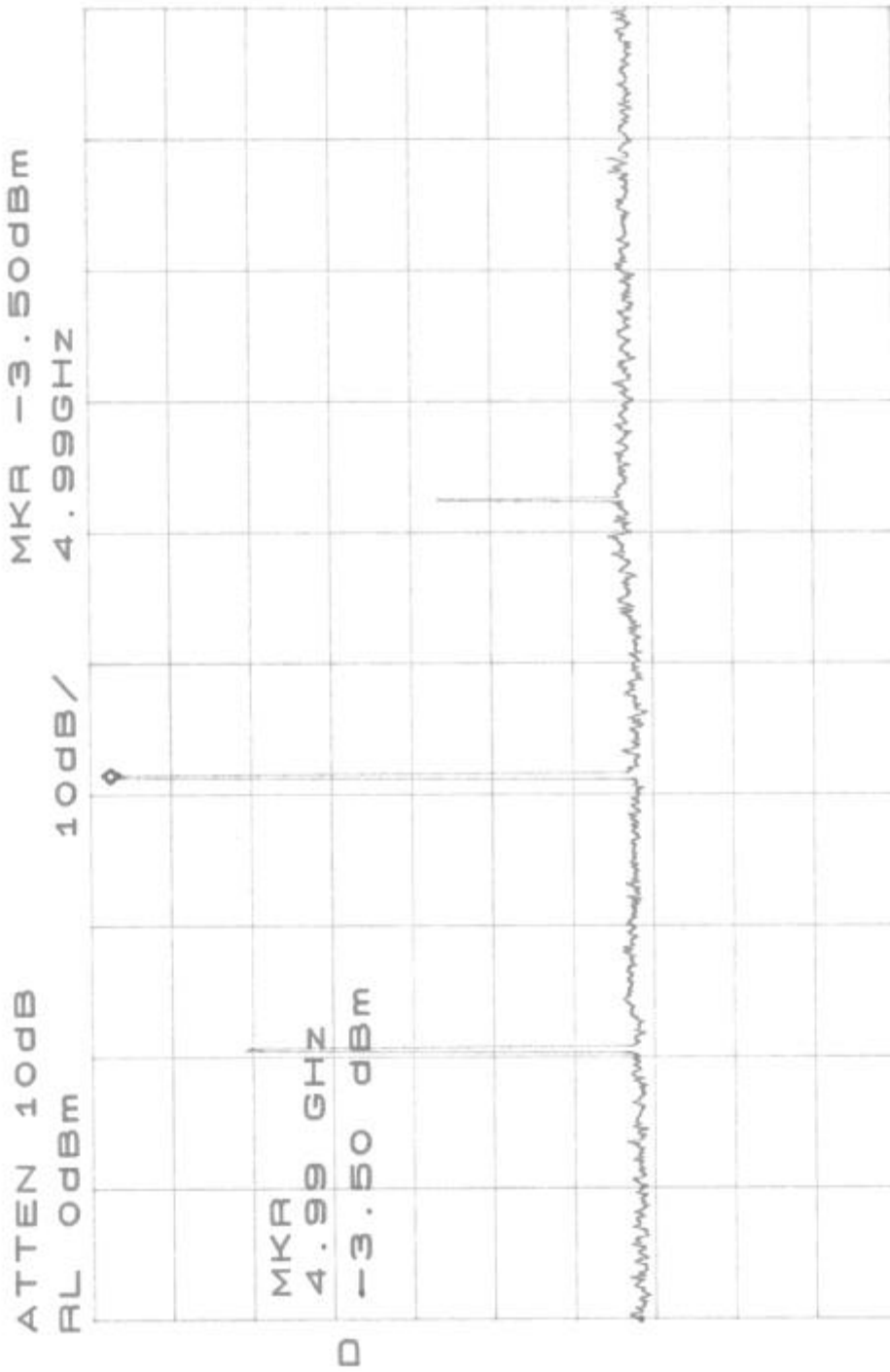


Mixer RF to IF Measurements (2.8V—2 die)



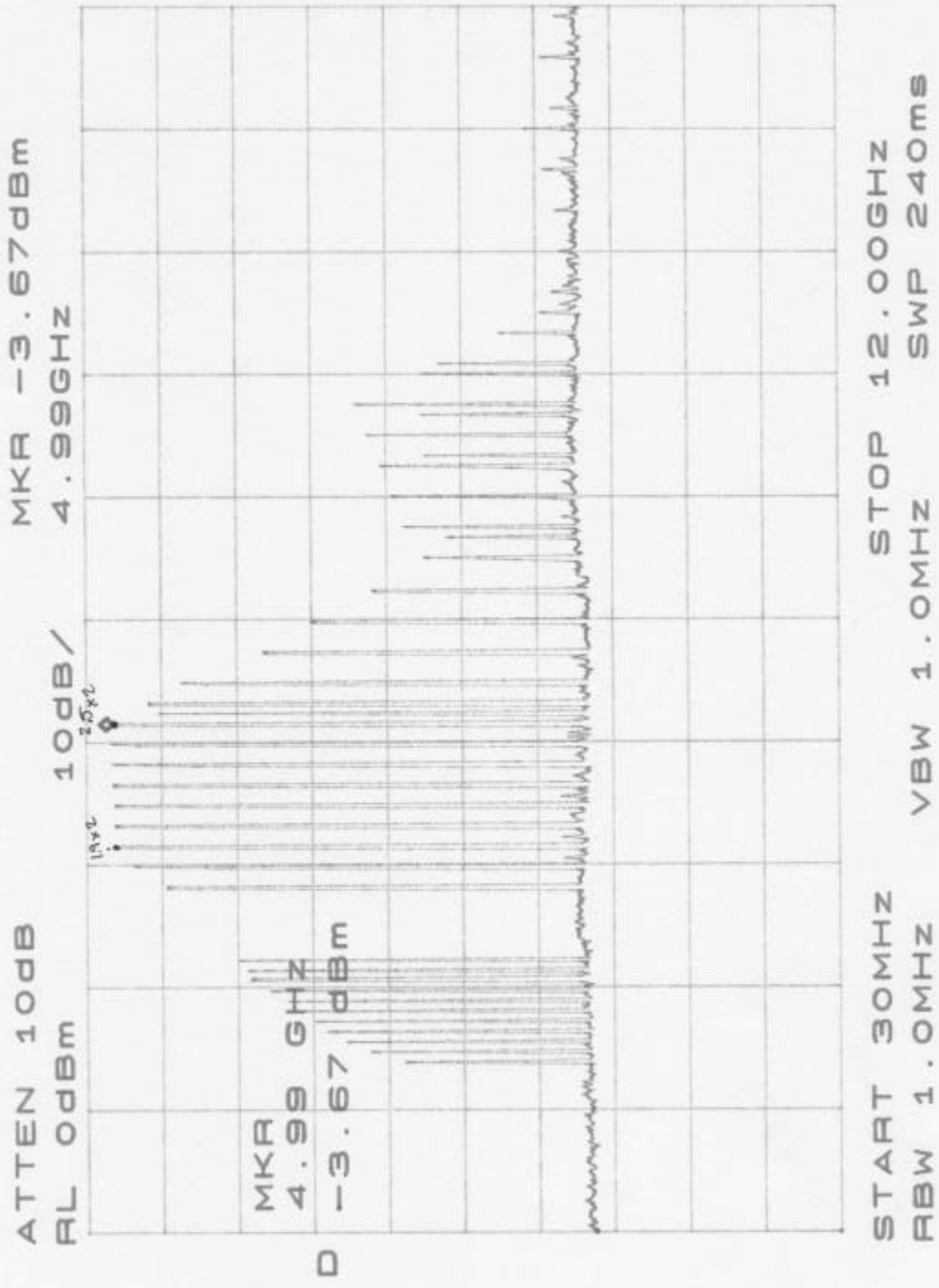
$V_{GS} = -1.85V$
 $V_D = 5.0V @ 16mA$

X2



X2 Doubler Spectrum at 5V VDS, 2.5 GHz Input

VDS = 5V
X2
2.0V @ 11mA
1.7 to 2.7 GHz

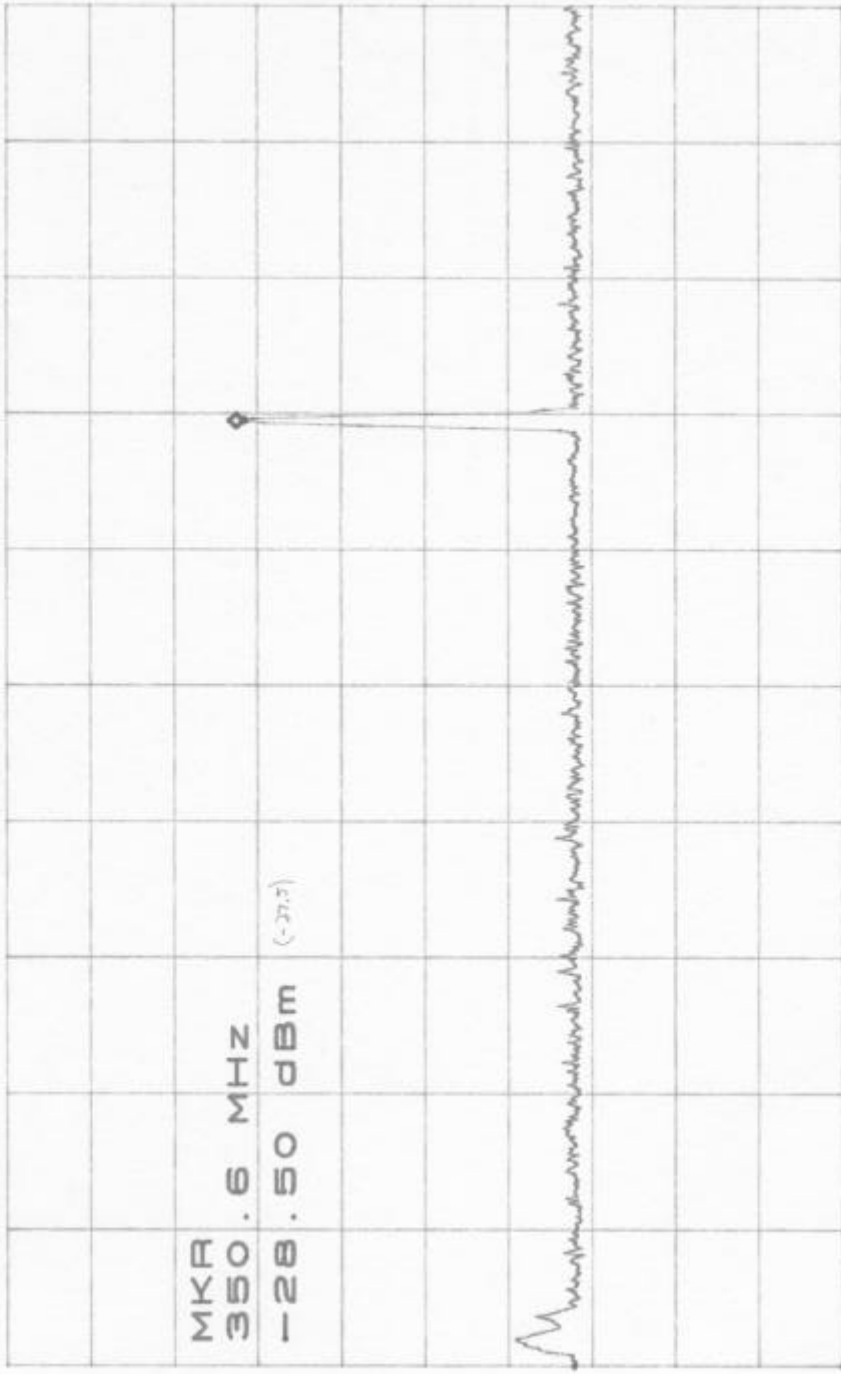


X2 Doubler Spectrum at 5V VDS, 1.7-2.7 GHz Stepped Input

2.8V @ 17mA
 (-18.3) RF 5.25 GHz -18dBm
 (9.8) LO 4.9 GHz +9.8dBm

MKR -28.50dBm IF=350MHz

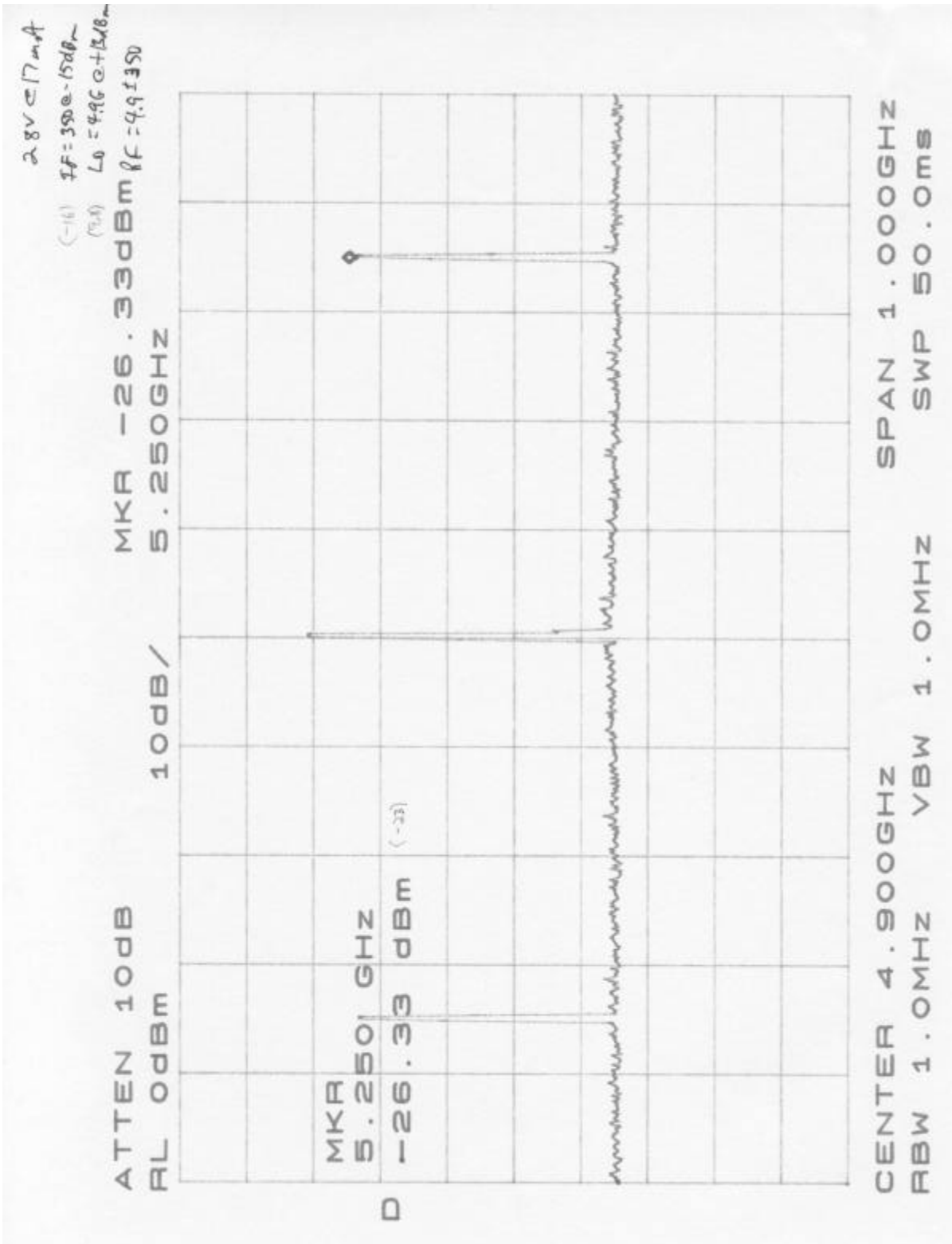
ATTEN 10dB
 RL 0dBm



MKR
 350.6 MHz
 D -28.50 dBm (-27.3)

START 10.0MHz STOP 500.0MHz
 RBW 1.0MHz VBW 1.0MHz SWP 50.0ms

Mixer Down Conversion (RF@5.25 GHz -18 dBm, LO@4.9 GHz +9.8 dBm)



Mixer Up Conversion (IF@350 MHz -16 dBm, LO@4.9 GHz +9.8 dBm)