JHU EE787 Fall 2003 MMIC Results

Craig Moore and John Penn

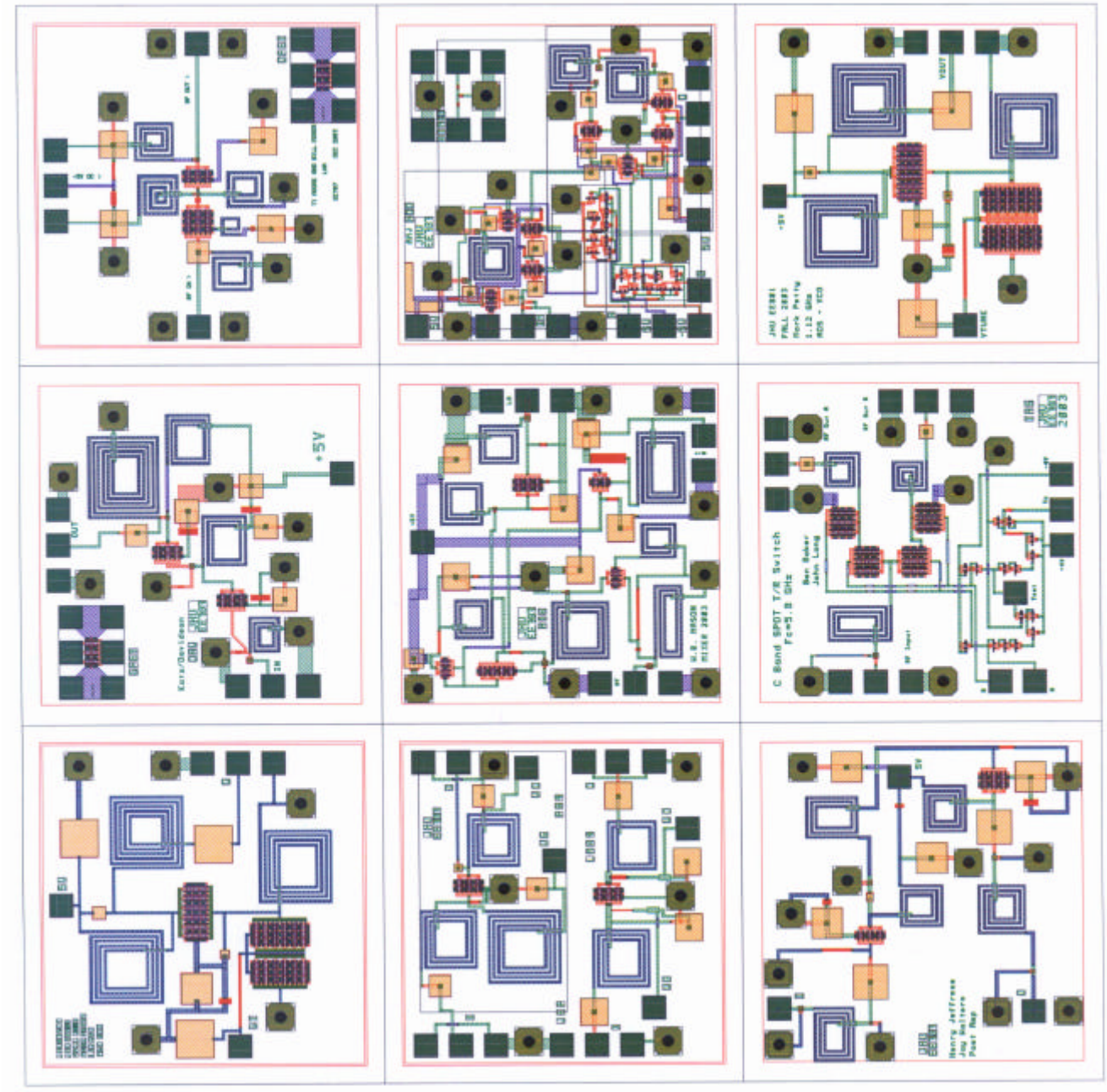
Designs Fabricated by TriQuint Semiconductor

ADS Support by Gary Wray—Agilent

TriQuint TQTRX Library and ADS software used for student designs

Six MMICs were designed by students for the Fall 2003 JHU MMIC Design Course as part of a simplex transceiver for the C-band industrial, scientific, and medical (ISM) band. All designs except for one were tested in the Spring of 2003 after fabrication by TriQuint Semiconductor. The one design not yet tested was the quadrature modulator. That design is difficult to test since it requires 6 DC probes and between the summer travel schedule of the professors and the student, a test time was never established. For the other MMICs, measurements compare favorably to simulations and all designs were successful with a minor problem in a TTL driver circuit for the RF switch design. A doubler design from the 2002 JHU MMIC course was re-fabricated with a minor fix to a layout problem on the output amplifier stage. Attached are plots of the results—small signal s-parameters and appropriate performance tests.

Thanks again to TriQuint and Agilent for their wonderful support of the JHU EE787 MMIC Design Course.

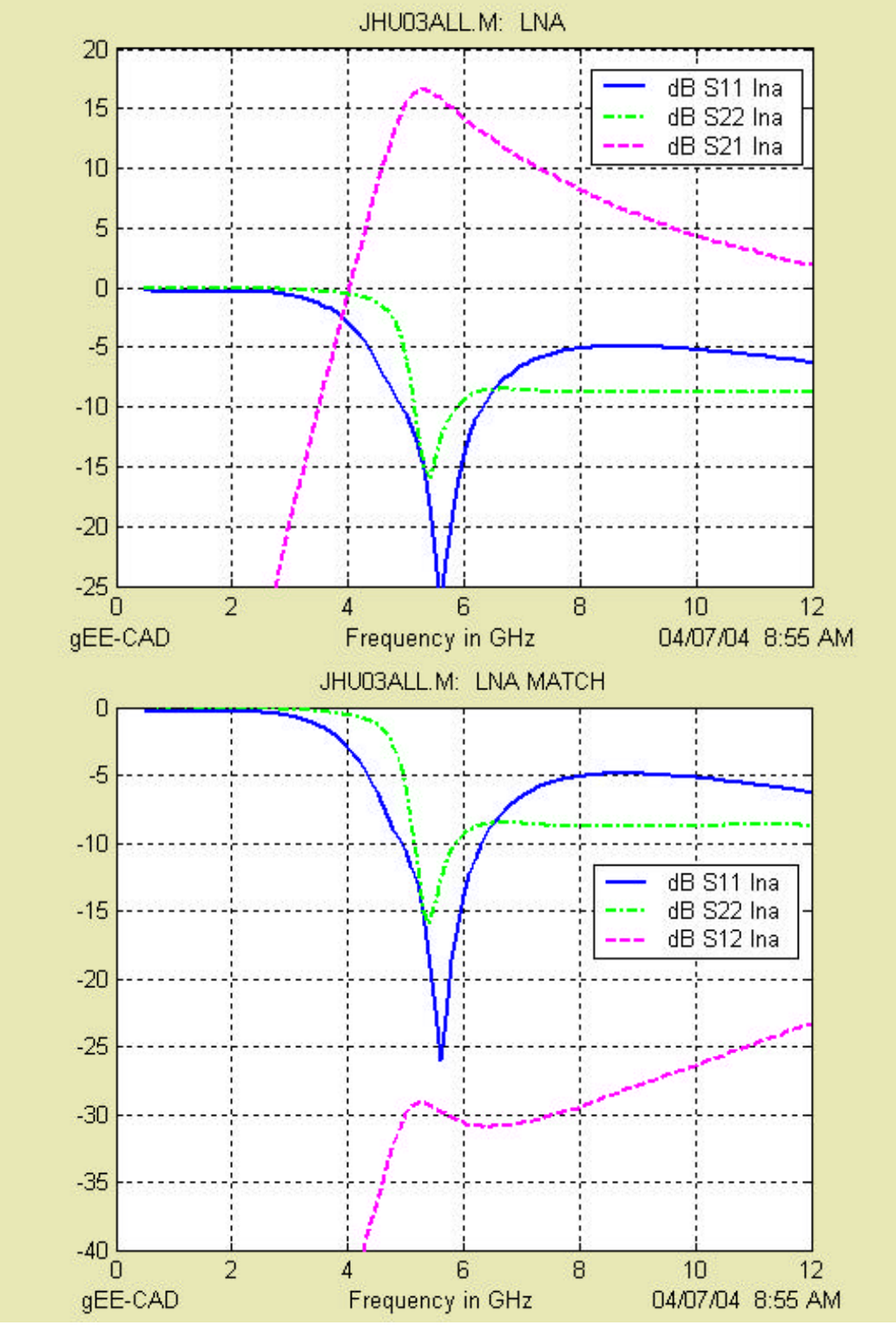


Fall 2003 JHU EE787 MMIC Design Student Project
Supported by TriQuint and Agilent Eesof
Professors Craig Moore and John Penn

Low Noise Amplifier—Ty Moore & Bill Moser
Mixer---Brad Mason
Post Amplifier—Henry Jeffress & Jay Walters
Driver Amplifier—Jeff Katz & John Davidson
QPSK Modulator—Aaron Johns
TR Switch—John Long & Ben Baker
Plus Special Project EE801 VCO—Mark Petty
S-Band Doubler--Ming-Zhi Lai, "fixed" Fall '02 design
4 GHz one stage LNA and PA design examples--John Penn

Low Noise Amplifier (C-Band) by Ty Moore and Bill Moser:

For this year's system project, a low noise amplifier (LNA) is connected to the receive antenna through the T/R switch. The LNA had about the correct bias and worked well comparing favorably with initial simulations. Bias was measured at 5V at 27 to 30 mA vs. a predicated 23 mA. Below are plots of the measured s-parameters followed by plots of the original simulations and re-plots of the measured data to a similar plot scale. Gain appears to be slightly lower and measured noise figure about 0.5 dB higher than simulations but they show very similar responses over frequency.



LNA Fall '03 Measured S-parameters (5V @ 30 mA)

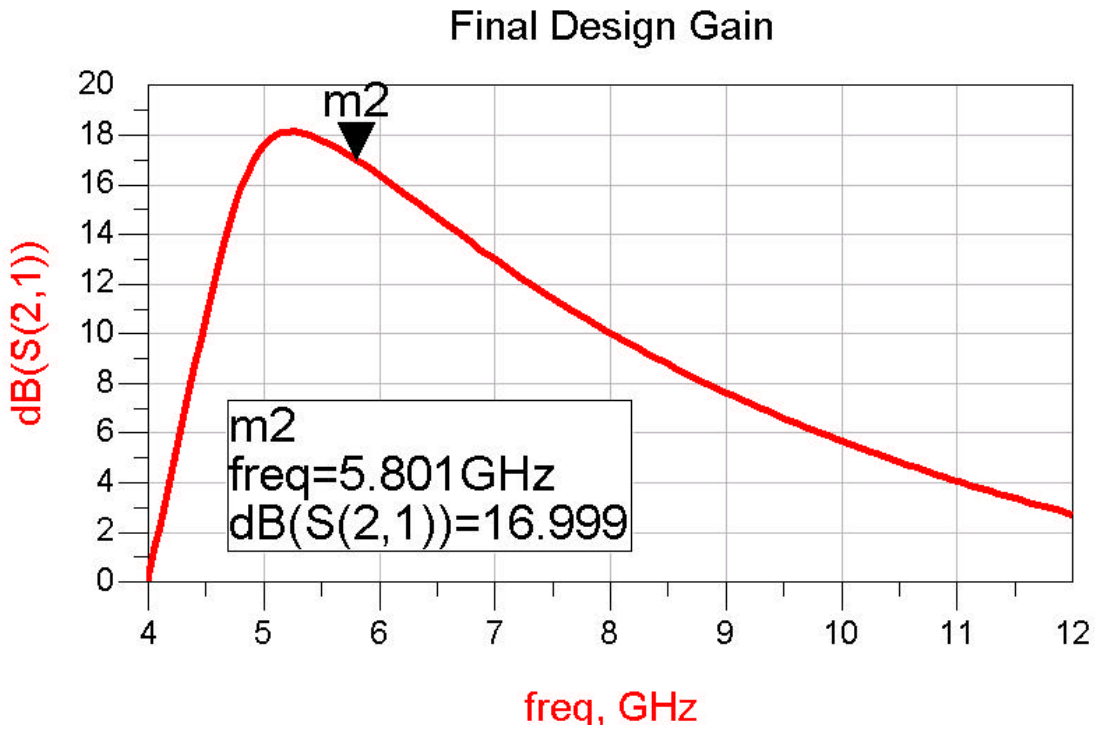
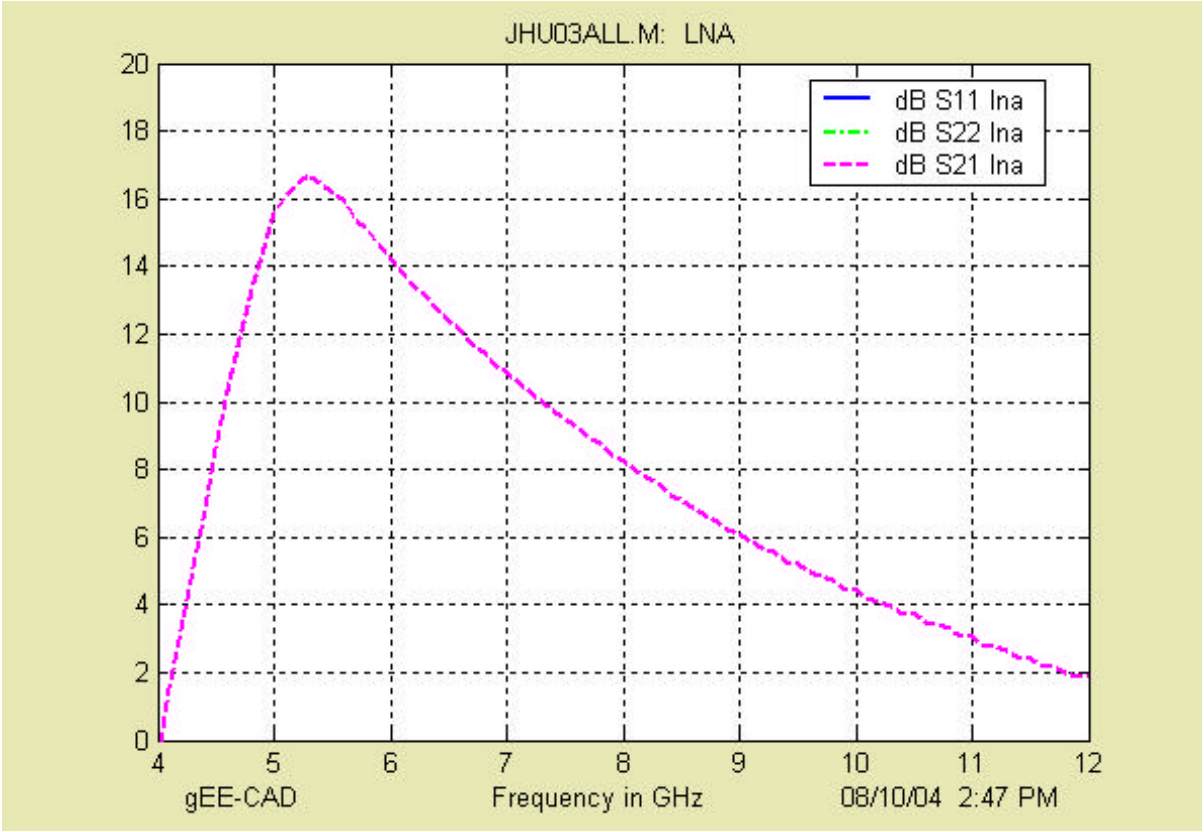


Figure 8 Gain – Complete Design



Plot of original Gain simulation vs. re-scaled measured data. Similar shape with slightly less gain.

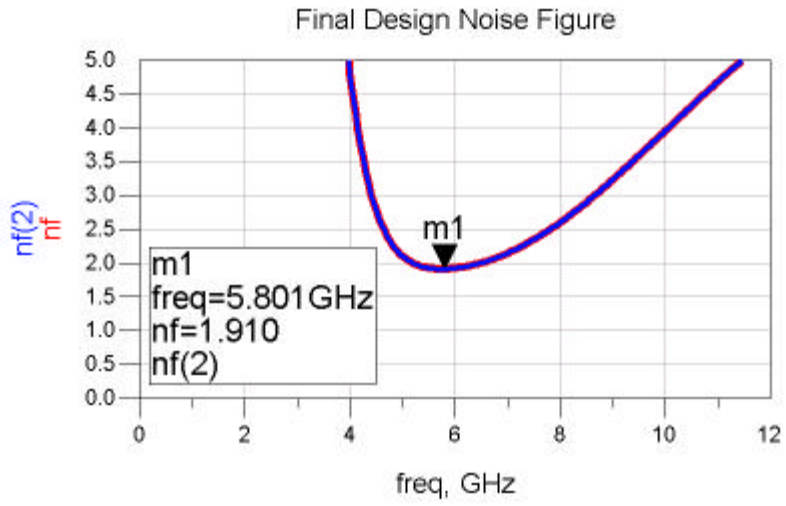
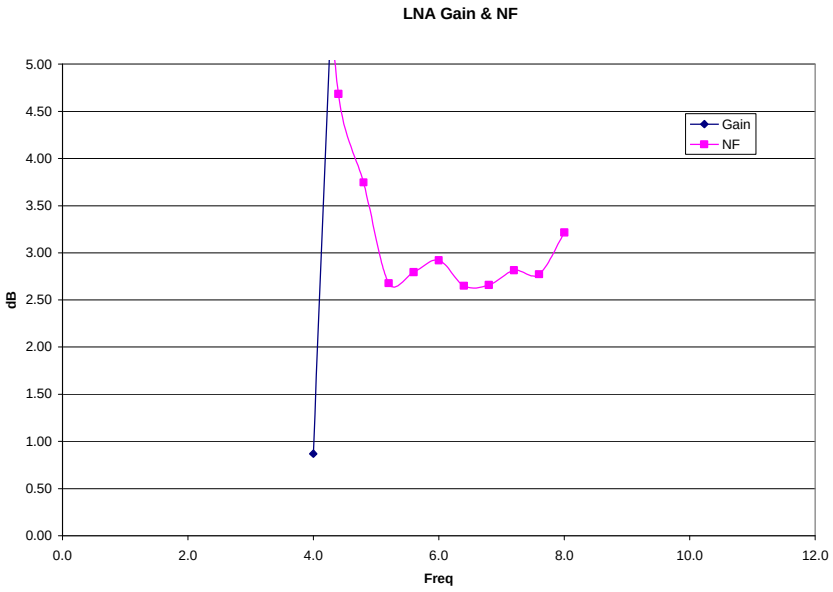
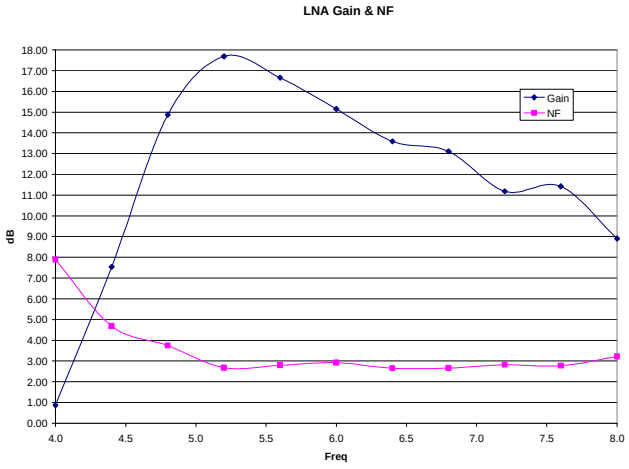


Figure 10 Noise Figure – Complete Design



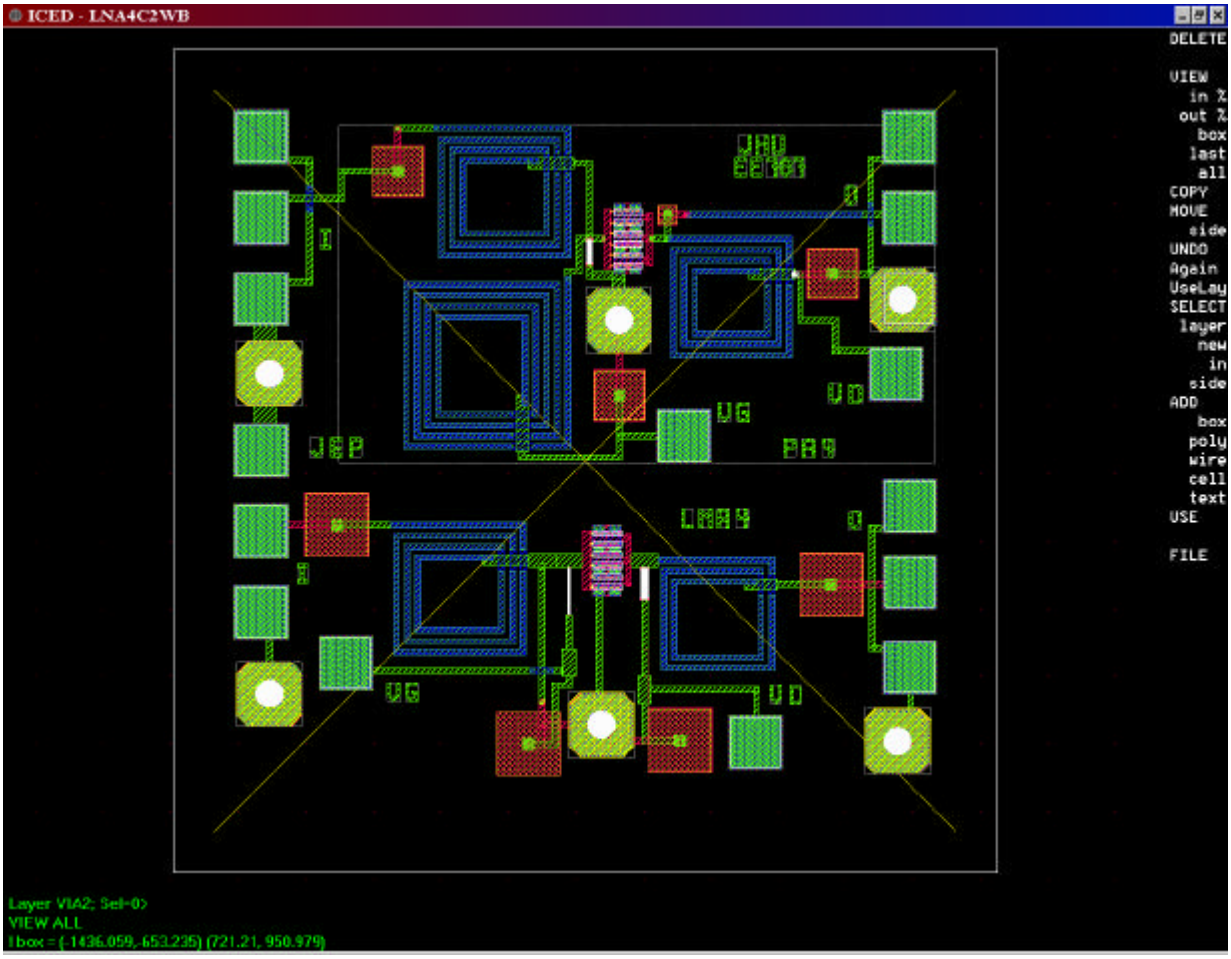


Plot of Original Noise Figure Simulation vs. Measured Gain and Noise Figure (2 Meas. Plots).

Class Design Examples: Low Noise Amplifier and Power Amplifier (4 GHz) by John Penn

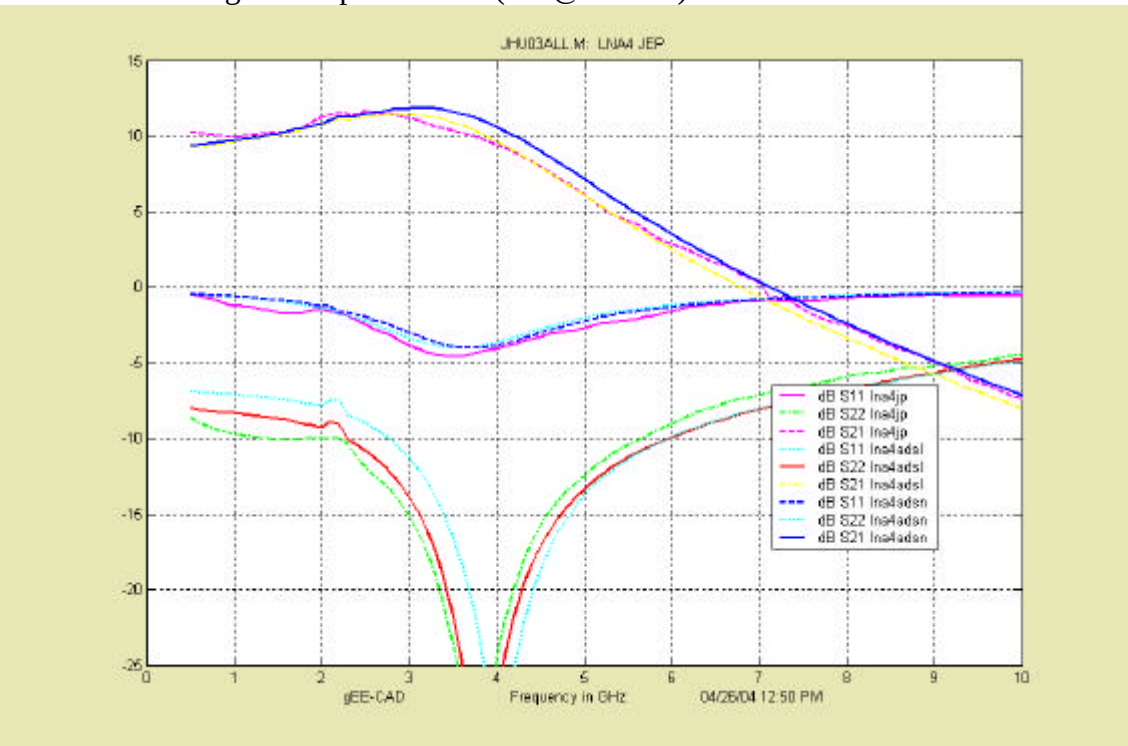
During the course the students are shown a design example of a low noise amplifier and a medium power amplifier at 4 GHz. This past year (2003) a layout was completed for each design and both were combined on a single 60 x 60 mil die (54 x 54 after dicing). Measured data was taken of the two designs and compared to original simulations. Results were similar to expectations. For future classes, these design examples will show measured data compared to simulations with ADS.

Original Layout (PA is top half, LNA bottom half):



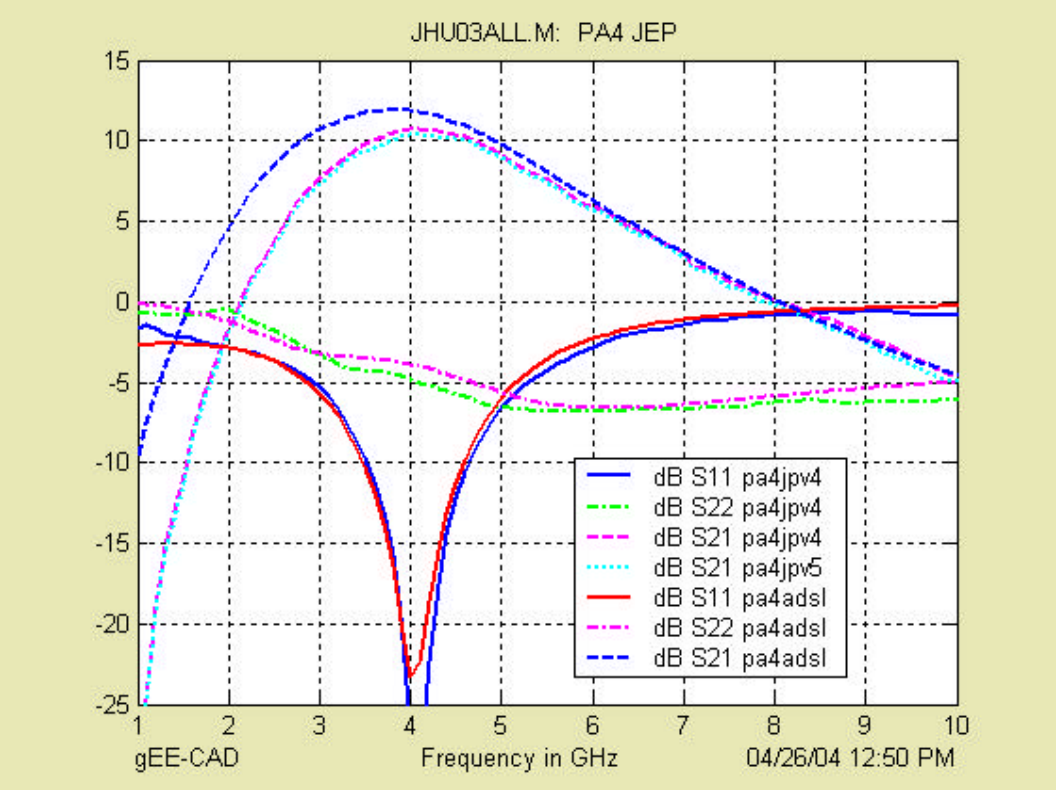
Following are plots of the measured s-parameters for the two designs. There is good agreement for both designs including the measured noise figure of the LNA vs. simulation. Power output of the PA design shows similar performance but with about 1db less output power than predicated. The power amplifier was biased at 5V VD and an IDS of 51 mA, while the LNA was biased at ~2V VDS (~3.6V VD) and an IDS of 10 mA.

LNA 4 GHz Design Example Fall ‘03 (2V @ 10 mA)

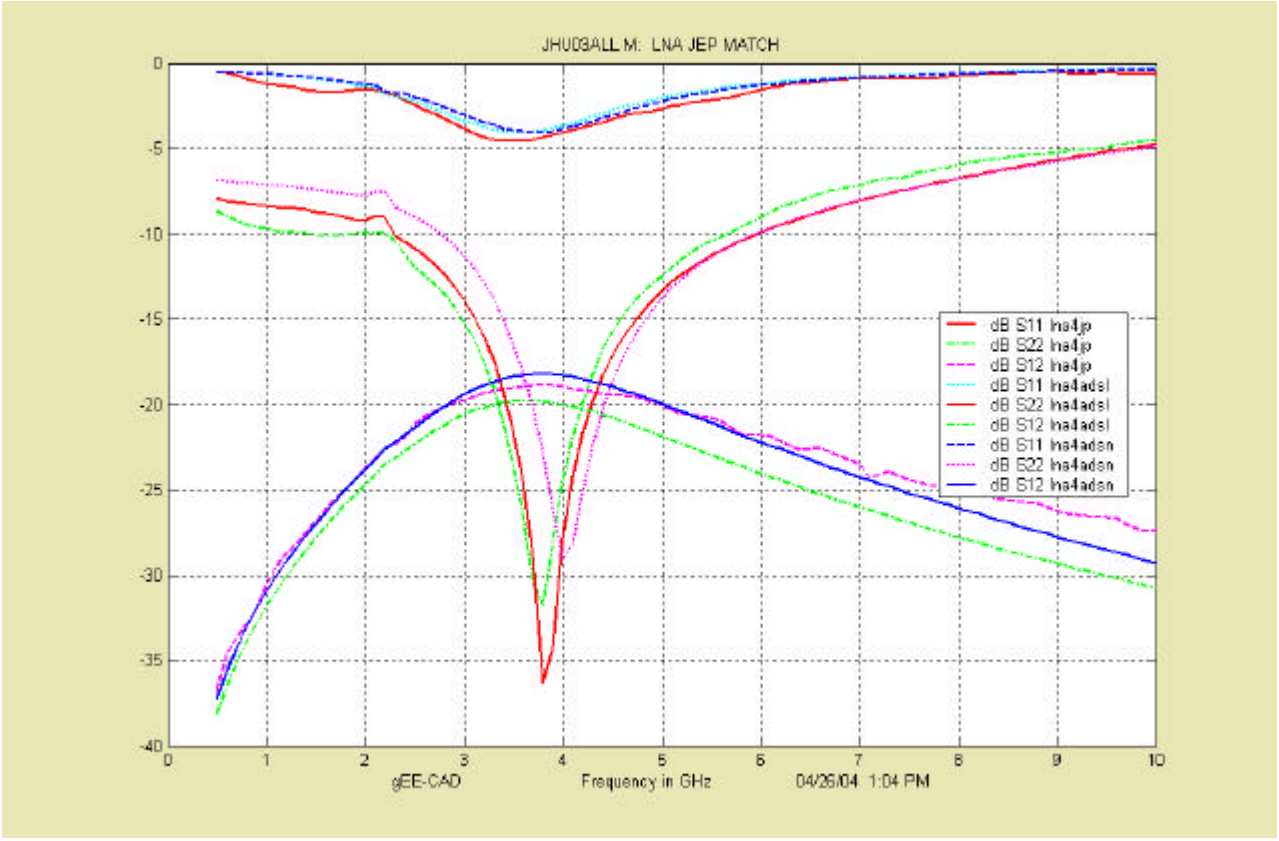


Good Agreement between ADS simulations and Measured Data. Linear s2p file for DFET does slightly better than non-linear model. Lna4jp = measured, lna4adsl = ADS Linear s2p file, lna4adsn = ADS DFET TOM model.

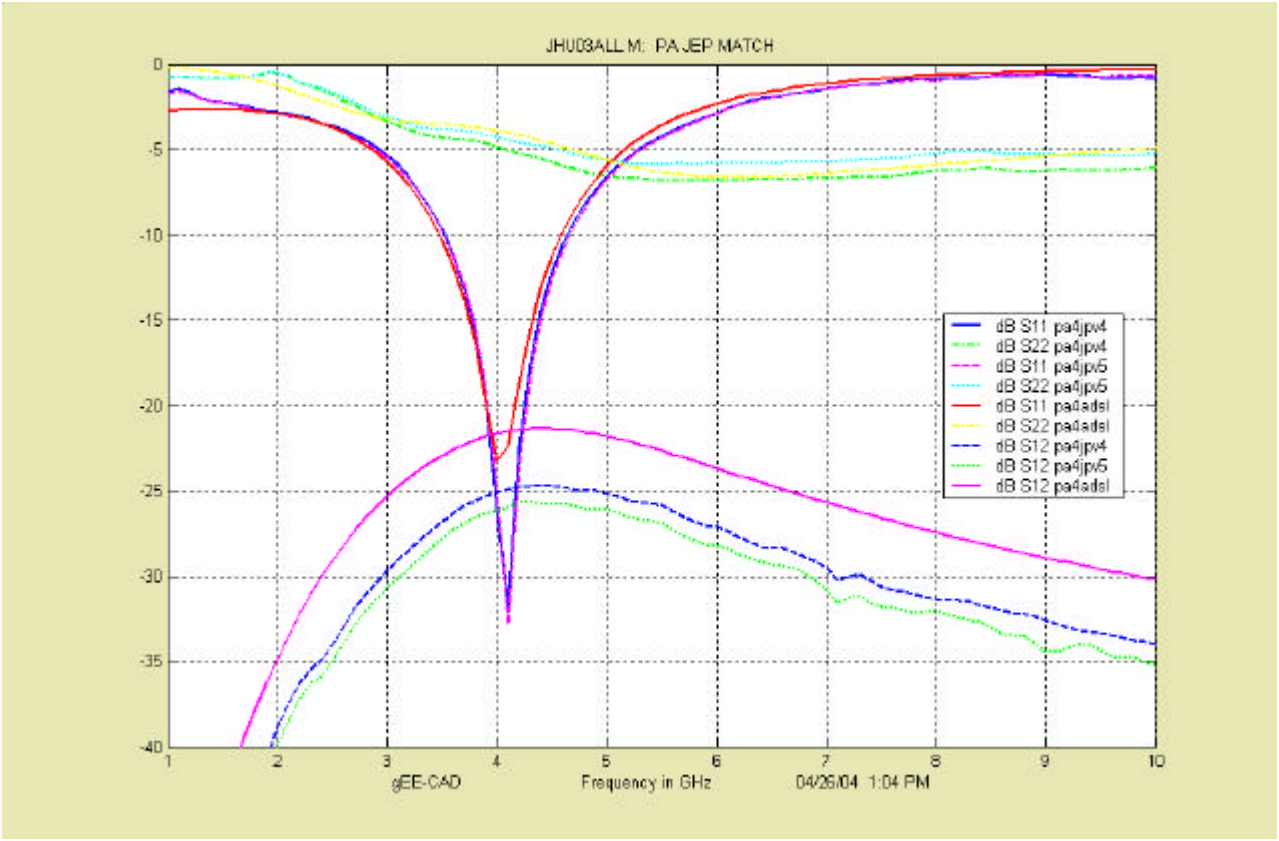
PA 4 GHz Design Example Fall ‘03 (5V @ 50 mA)



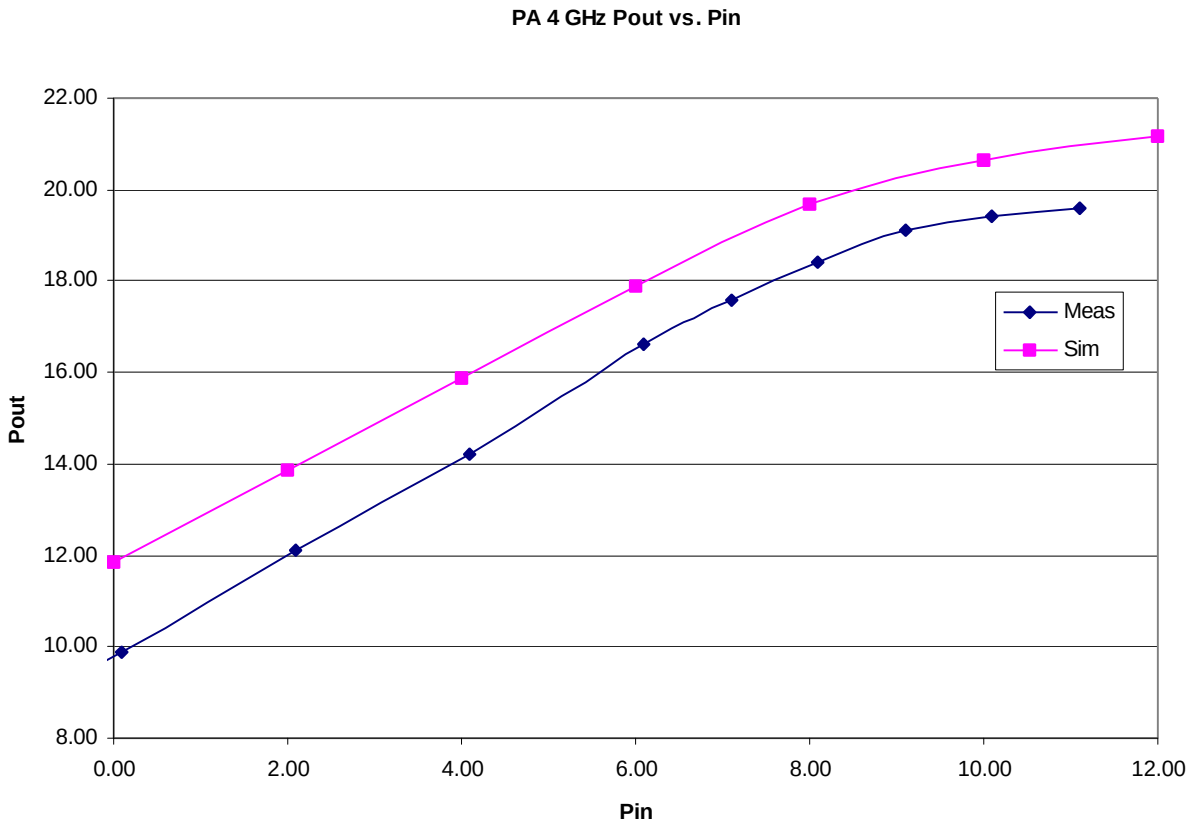
pa4jpv4 = 4V measured, pa4jpv5 = 5V measured, pa4adsl=ADS GFET TOM simulation.



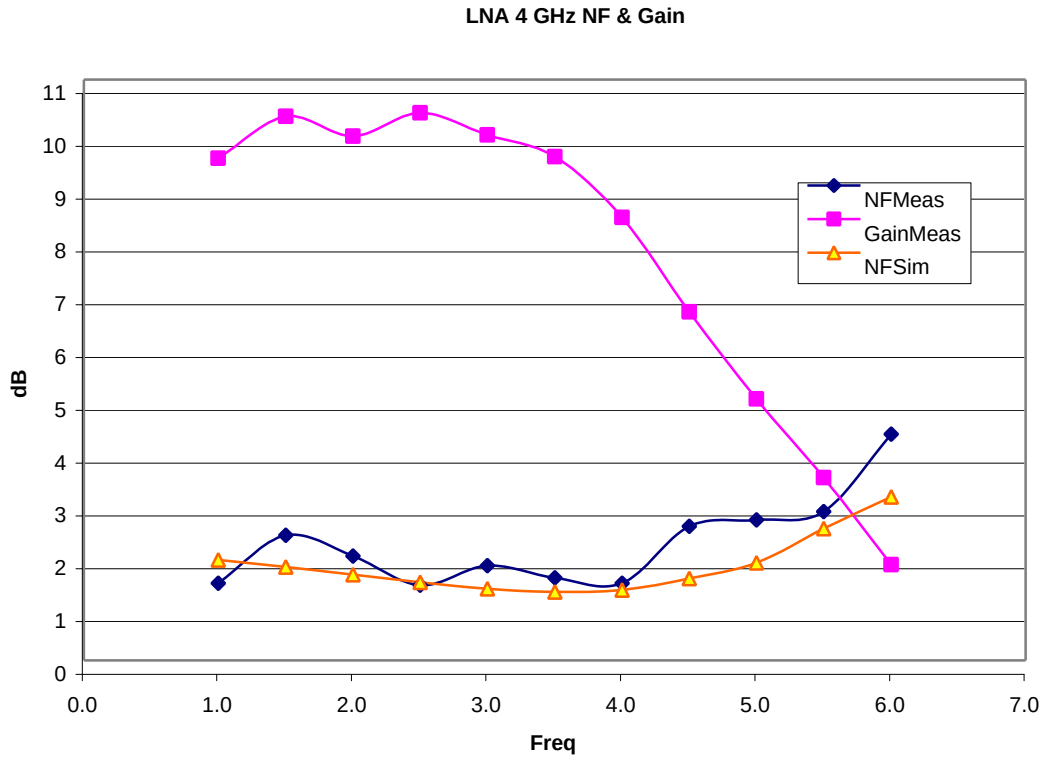
Good Agreement between ADS simulations and Measured Data. Linear s2p file for DFET does slightly better than non-linear model. Lna4jp = measured, lna4adsl = ADS Linear s2p file, lna4adsn = ADS DFET TOM model.



pa4jpv4 = 4V measured, pa4jpv5 = 5V measured, pa4adsl=ADS GFET TOM simulation.



Measured vs. Simulated Power Output PA 4 GHz Example TriQuint.



Measured vs. Simulated Noise Figure LNA 4 GHz Example TriQuint.

Mixer (C-Band) by Brad Mason:

For this year's system project, the mixer downconverts the received signal to a baseband IF signal (<20 MHz). The Mixer was measured at a nominal bias of 5V at 50 mA. Test 2 shows downconversion with varied LO power levels. The result is shown below as a plot of conversion loss/gain vs. LO power. The goal was to have some conversion gain and this is achieved with sufficient LO drive. Test 3 used a nominal LO setting of 0dBm (RF=-8dBm) and looked at conversion gain over the desired band of operation. Mixer operation was fairly insensitive to DC bias over a supply range of 4 to 5V with slightly lower performance at 3.5 to 5.5V.

Measured Mixer RF/LO Match & Isolation 5V at 46-50 mA

Brad Mason

1) LO 5.79 GHz 0 dBm setting RF 5.8 GHz -8 dBm setting Measured 10 MHz IF into Oscilloscope 5V at 50

LO (corr)	RF (corr)	IF (Vpk)
-1.9	-9.9	3

Freq (GHz)	Thru	
5.6	3.72	Use 1.9 dB at 5.8 GHz per side
6.0	3.92	

2) LO 5.75 GHz 0 dBm setting 5.8 GHz RF -8 dBm setting IF using bias tee (45 MHz-50 GHz) on spectrum analyz
5V at 50 mA

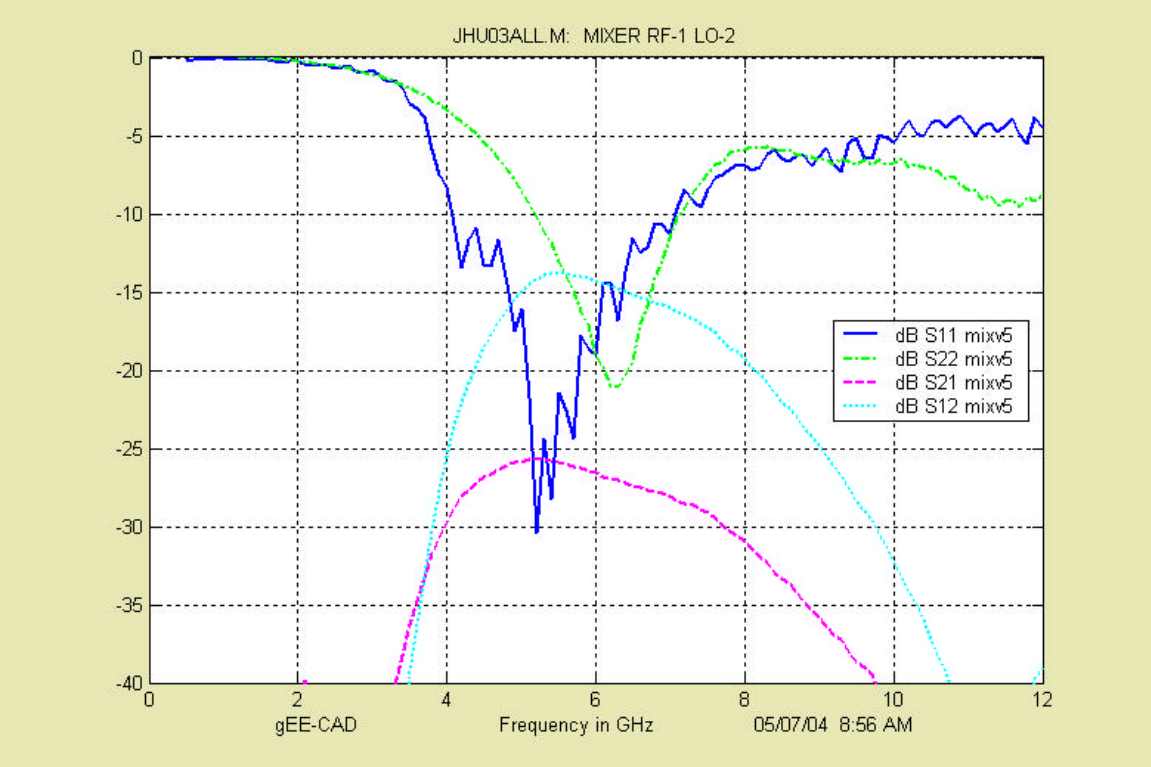
LO (corr)	RF (corr)	IF (dBm)	Loss (gain)
-1.9	-9.9	-14.2	-4.3
-0.9	-9.9	-13.2	-3.3
0.1	-9.9	-12.2	-2.3
1.1	-9.9	-11.5	-1.6
2.1	-9.9	-10.6	-0.7
3.1	-9.9	-10.2	-0.3
4.1	-9.9	-9.6	0.3

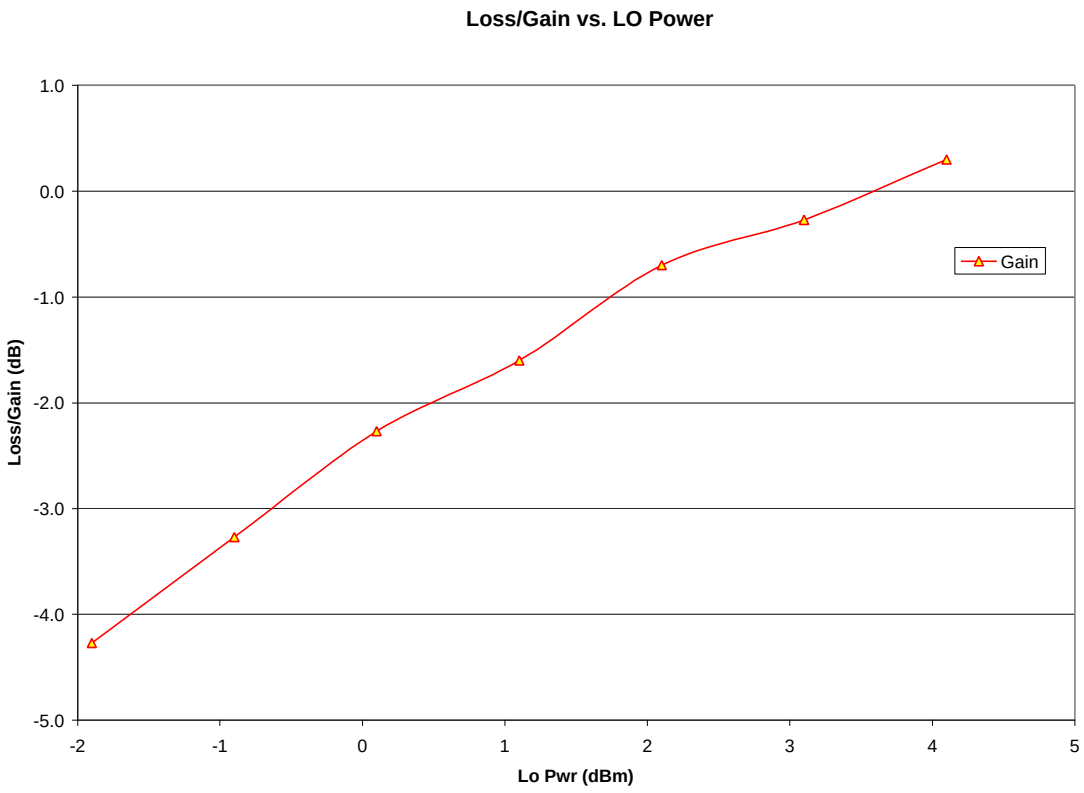
3) LO Freq at 0 dBm setting RF Freq at -8 dBm Setting IF (10/20 MHz)

LO (GHz)	RF (GHz)	IF (dBm)	Loss (gain)
5.82	5.83	-9.2	0.7
5.79	5.80	-9.2	0.7
5.78	5.80	-11.3	-1.4

Note: Adjusted Supply without much change from 4V to 5V. Fell off slightly at 5.5V and maybe 1 dB lower at 3.5V

Measured S-parameters for Mixer (5V @ 46 mA), small signal RF/LO match, isolation RF=1, LO=2

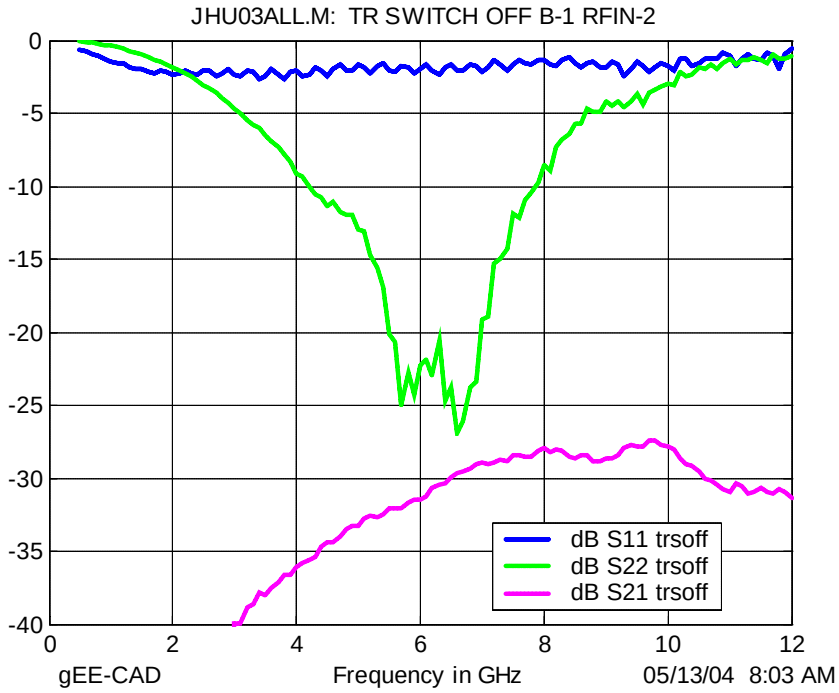




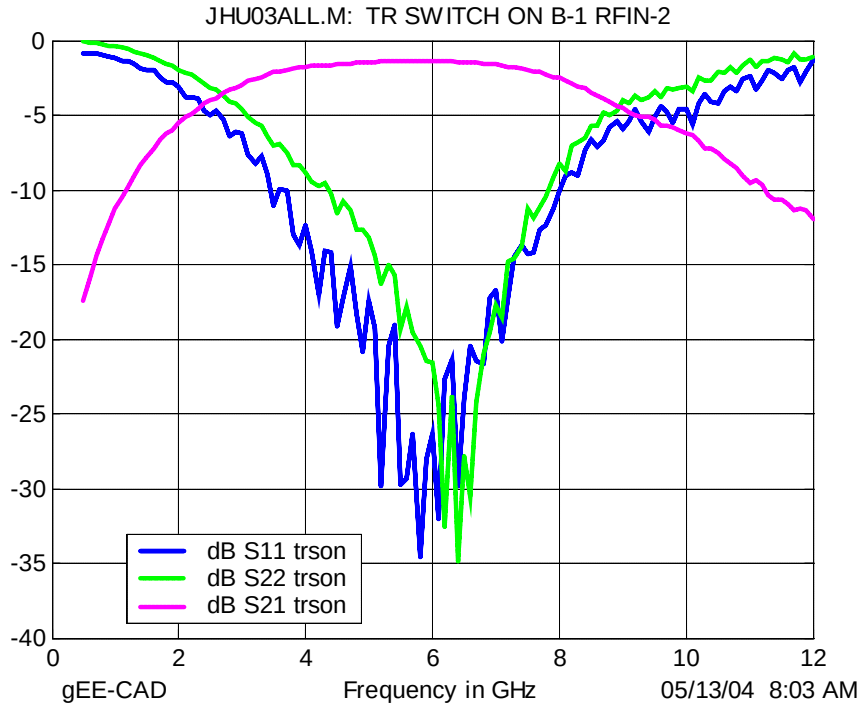
Measured Conversion Loss/Gain vs. LO Power.

TR Switch (C-Band) by Ben Baker and John Long:

The RF switch was a SPDT (single pull, double throw) with low insertion loss (~1 dB) and good isolation (~30 dB) for the off path. This circuit switches the system's antenna to the LNA for receive signals and to the power amplifier for transmission. A TTL to switch driver circuit was designed but did not have sufficient negative voltages to turn off the appropriate switches. Pads were designed into the layout so that the driver circuit could be driven directly. With direct bias, the RF performance matched expectations. Attached are s-parameters as measured and as predicted. The TTL driver voltages are shown also as measured and as simulated.



TRSwitch Off



TRSwitch ON, driven with 0, -4V.

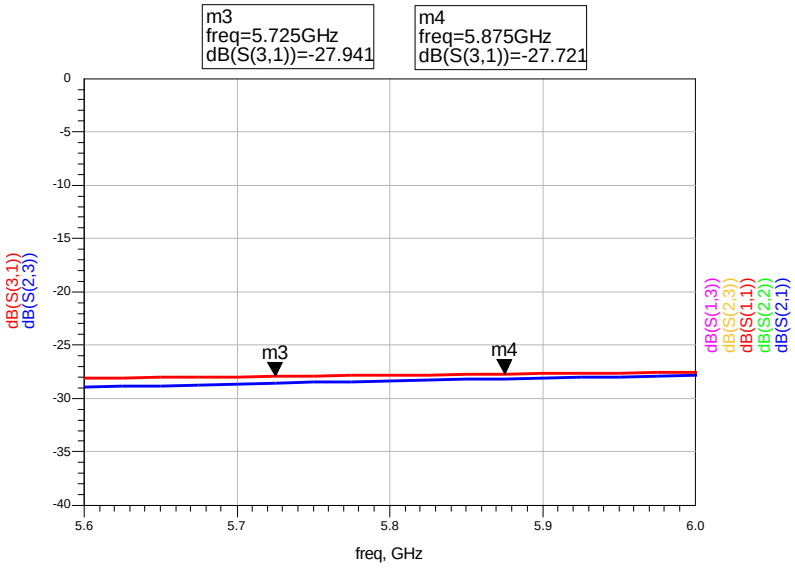
TTL Circuit Driver had proper bias currents +4V at 14-15mA and -4V at 9 mA, but output drive was only about 0, and -2V. Switches were not fully turned off, and RF performance was similar while driving the A/B inputs with 0, -2V instead of the desired 0,-4V. Insertion loss went from 1.3 dB to about 6 dB in “intermediate state”. Probably needs another diode drop. Test point varied from +1V to -1.1V and would presumably work better if shifted to 0, -2V.

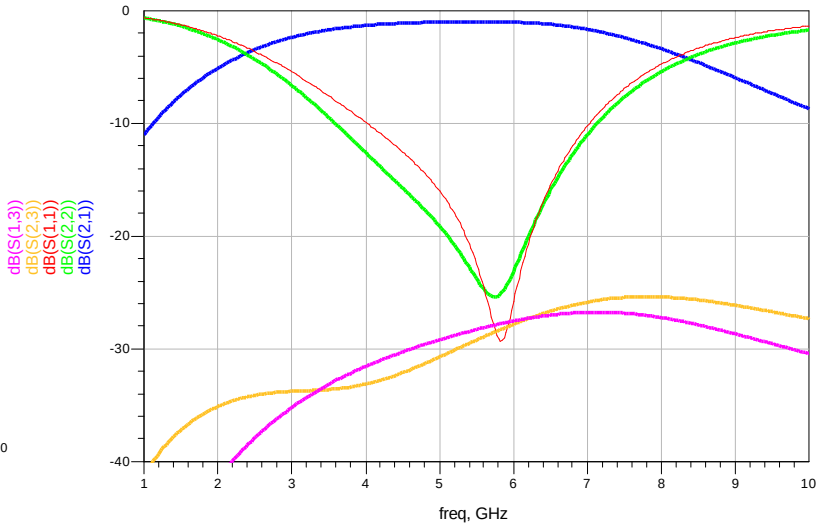
Driver (2 Die with similar responses)

VC	A	B	+4V (mA)	-4V(mA)	Test
0V	-2.0V	0.0V	15 mA	9mA	-1.1V
4V	0.0V	-2.4V	15 mA	9mA	+1.0V

Original Simulation of Isolation and All S-parameters:

Below: simulated TTL driver. RF performance matched expectations when the switches were biased directly.

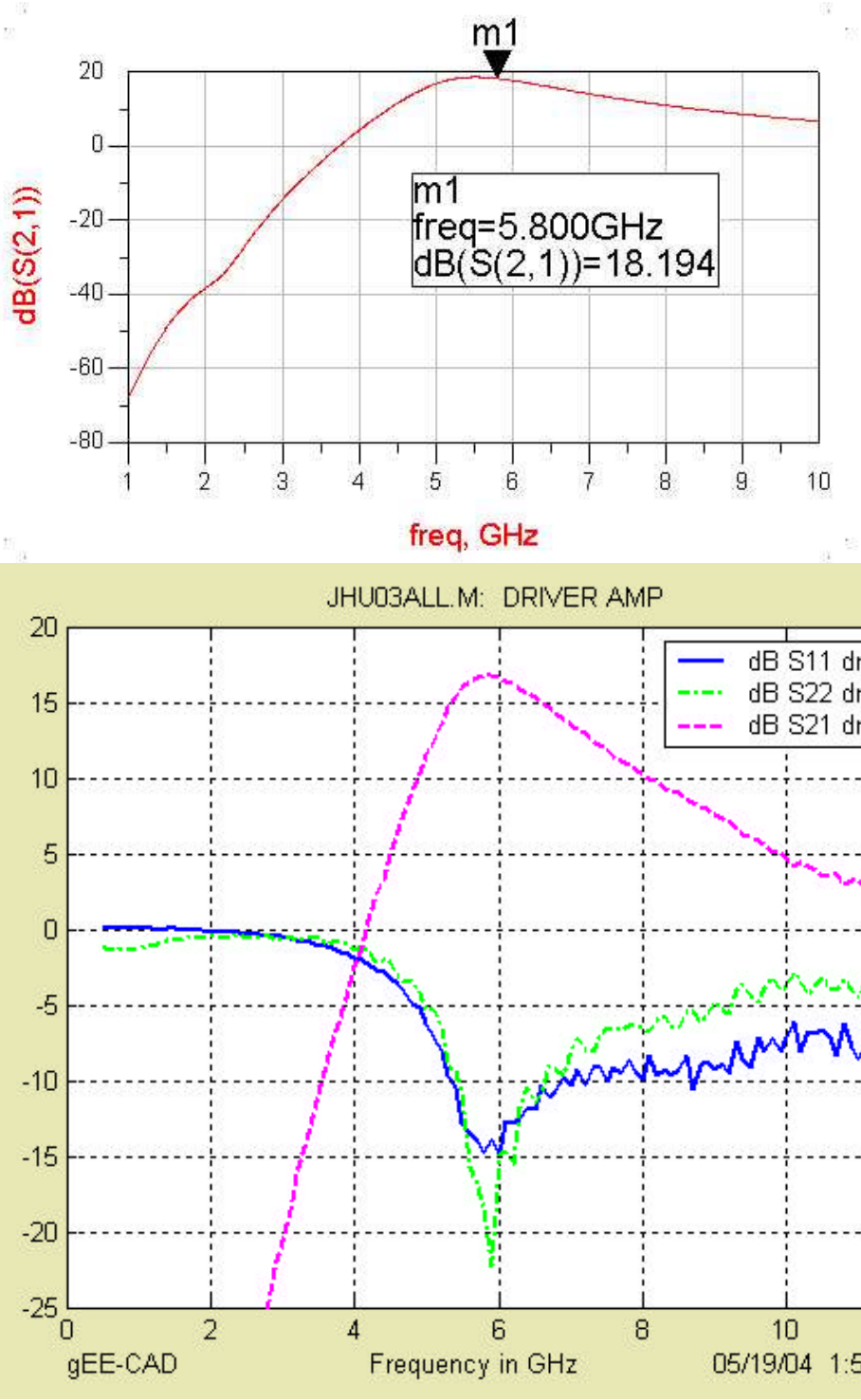




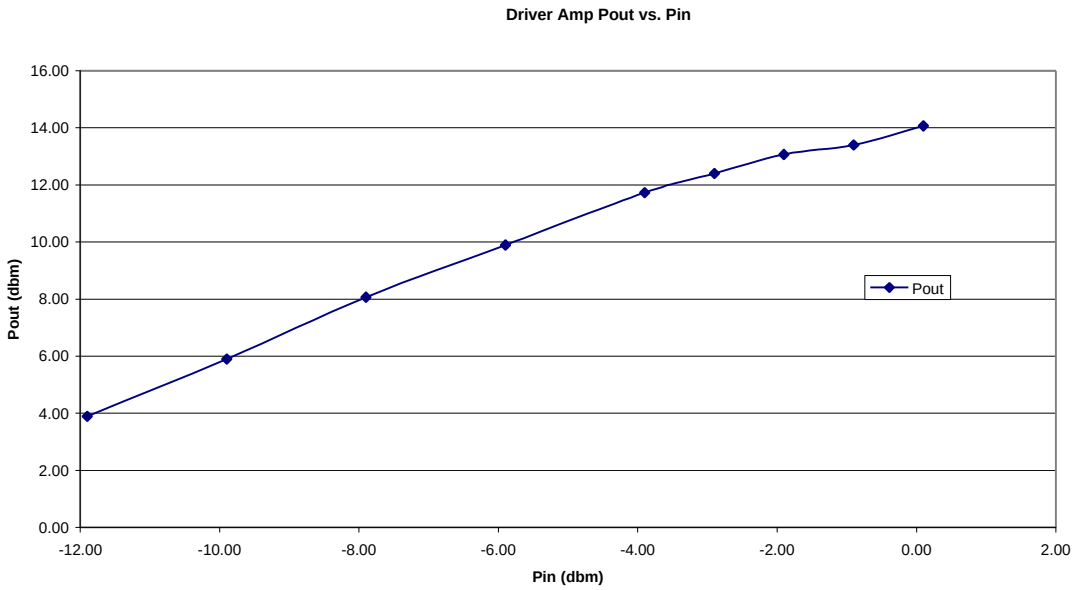
Control Bit Voltage	Vc1 [V]	Vc2 [V]	Low Loss Path
+4V	0V	-3V	S(21)
0 V	-3V	0V	S(31)

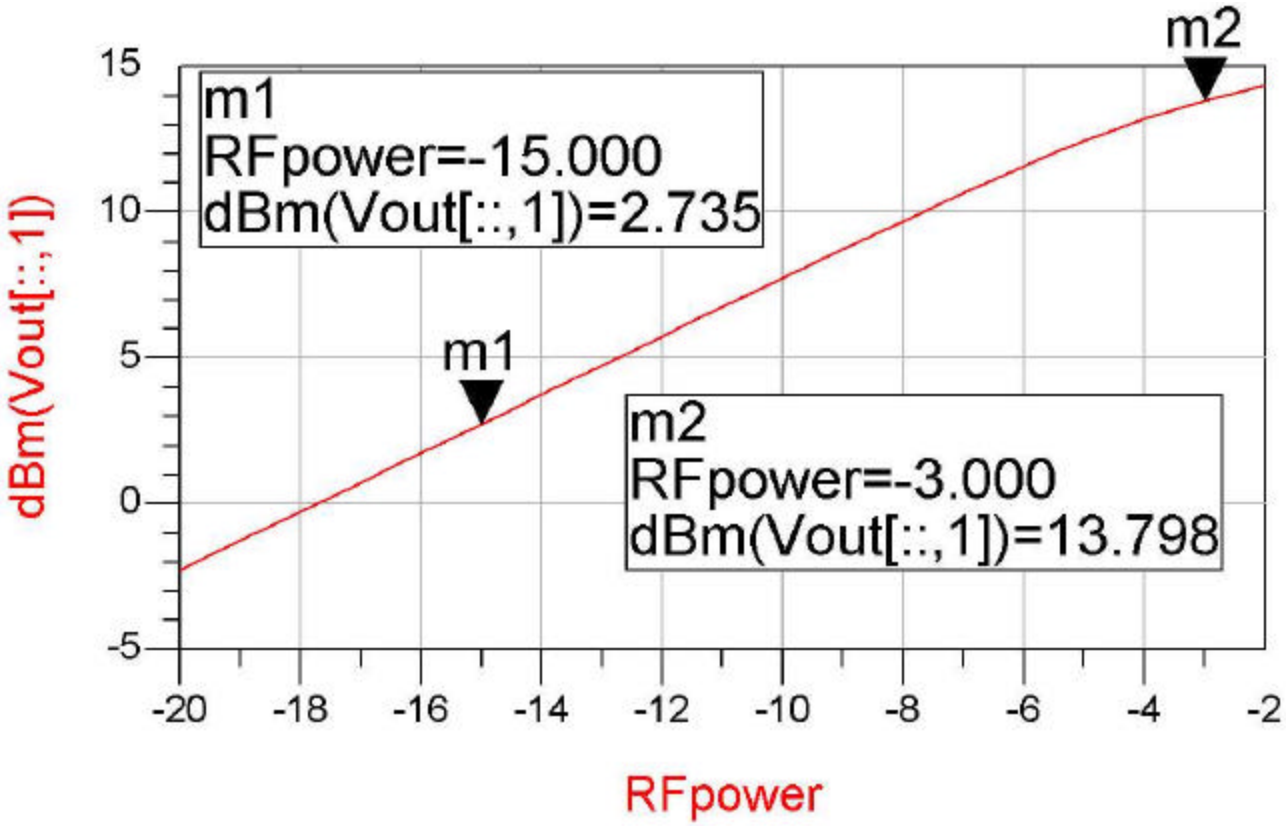
Driver Amplifier (C-Band) by Jeff Katz and John Davidson:

The driver amplifier is a medium power general purpose amplifier for the C-band transceiver. Bias was measured at 5V at 117 mA, very close to the predicted 5V at 113 mA. Gain and Power output were also very close to predicted level. Shown are some of the original simulations vs. measured data.



Simulated Gain (S21) and Measured S-parameters for the Driver Amp (5V at 117 mA)



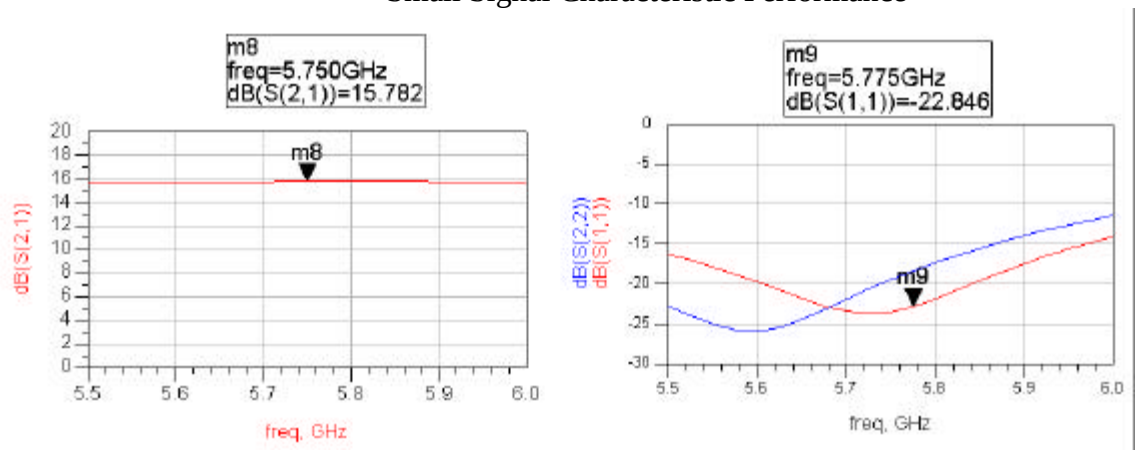


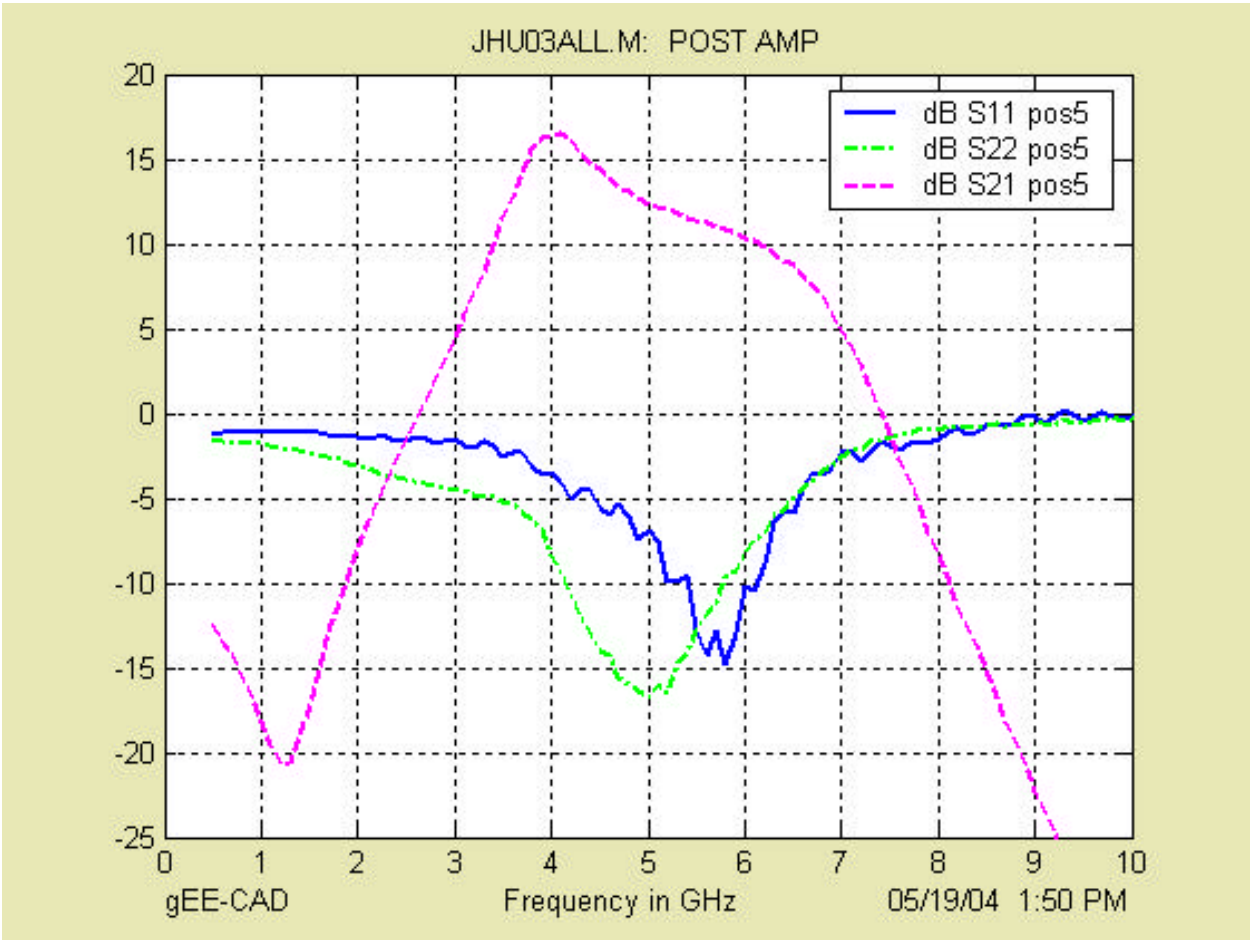
Measured and Simulated Power Output. Measured gain was slightly lower but output power was very close to expected.

Post Amplifier (C-Band) by Henry Jeffress and Jay Walters:

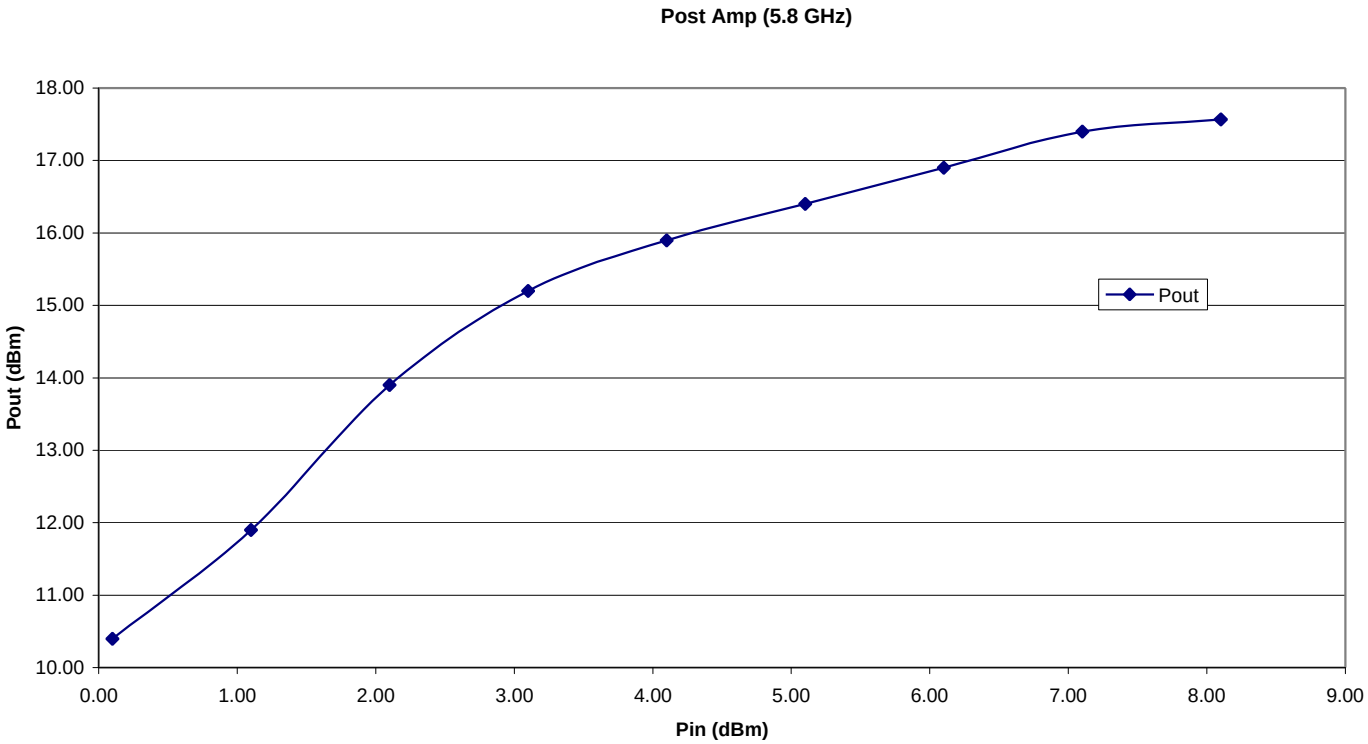
The post amplifier is a medium power general purpose amplifier for the C-band transceiver. Bias was measured at 5V at 85 mA, close to the the 5V at 84 to 91 mA predicted in simulations. Measured Gain was a bit lower than expected. Below shows the simulated performance (narrowband) vs. the measured performance (broadband). Power Output is shown as Measured.

Small Signal Characteristic Performance





Post Amplifier (5V at 85 mA). P1dB ~50 mW +17dBm



Power Output vs. Pin as Measured for the Post Amplifier. P1dB is greater than 15 dBm.

Voltage Controlled Oscillators (VCO)--MWO and ADS Layouts--by Mark Petty:

The VCO was designed to generate a signal tunable from 1.07 to 1.17 GHz which would then be doubled as part of the Fall '02 system concept. Mark Petty did a special graduate project in the Fall '03, improving on his Fall '02 design with ADS. He also performed a VCO layout of an identical circuit using Microwave Office. Unfortunately, Mark had trouble simulating the design with Microwave Office but he was able to use the TriQuint library and successfully layout a working design that used the same element values as his ADS based design.

Both designs worked well but with slightly different tuning. Attached are measured output power and frequency versus the tuning voltage of 0V to 5.5V. Bias is a single supply of +5V at 44 mA. Output power is as high as ~19 dBm (add 0.75 dB to measured data) which is very close to the +19 dBm expected output power. The signal was also very clean and sinusoidal.

Measured ADS and AWR VCOs
Mark Petty Designer
ADS VCO similar to Fall 02 MMIC class design. Improved robust design.
AWR VCO similar to ADS design but could not be simulated with AWR. Layout only.
Loss of output cables and probe estimated to ~0.75 to 1 dB. Add to Pout(measured).

ADS VCO	5V at 44mA	
Bias (V)	Freq (GHz	Pout(ms)
0.0	1.139	18.5
0.5	1.146	18.3
1.0	1.162	18.3
1.5	1.186	18.5
2.0	1.202	18.3
2.5	1.212	18.5
3.0	1.219	18.3
3.5	1.223	18.3
4.0	1.225	18.2
4.5	1.227	18.2
5.0	1.228	18.0
5.5	1.229	17.5
Range:	0.090	
Center:	1.184	

AWR VCO	5V at 43mA	
Bias (V)	Freq (GHz	Pout(ms)
0.0	1.056	18.3
0.5	1.059	18.3
1.0	1.073	18.5
1.5	1.086	18.3
2.0	1.100	18.3
2.5	1.115	18.2
3.0	1.125	18.0
3.5	1.130	18.0
4.0	1.133	17.5
4.5	1.135	17.8
5.0	1.136	18.0
5.5	1.138	18.0
Range:	0.082	
Center:	1.097	

Note: Harmonics	
X2	"-21.5 dBc"
X3	"-32.5 dBc"

Design Goal: 1.07 to 1.17 GHz

Fall '02 Re-fabrication--Frequency Doubler by Ming-Zhi Lai:

The frequency doubler from the Fall '02 MMIC Class was to take a VCO output (1.07 to 1.17 GHz) and double it to act as the LO for the Mixer (2.14 to 2.34 GHz). While the doubler portion of last Fall's design worked fine, there was an error in the power supply connection to the output amplifier stage. The power supply connection was re-routed and the die was fabricated along with the Fall '03 designs. Last year's performance is shown versus the refabricated circuit. Unfortunately, the circuit was only tested with about +4.5 dBm of input power. It may have worked better with more input drive based on last years measurements.

Measured data with output amplifier FET capacitively coupled to the output (OFF switch)

Input = 1.12 GHz 5V @ 30 mA, -5V @ 2mA, VG=-3.0V

SG (Pset)	X1	X2	X3	X4
0	-16.8	-17.7	-46.3	-45.3
2	-14.5	-14.3	-43.5	-39.7
4	-12.0	-11.0	-37.0	-35.2
6	-9.0	-7.3	-29.0	-31.7
8	-5.3	-2.8	-21.5	-27.8
10	-3.5	1.3	-17.2	-22.0

Measured Data with "fixed" output amplifier.

5V @ 90 mA, -5V @ ~2mA, VG=-1.0V

Freq(GHz)	SG (Pset)	X1	X2	X3	Pin (Corr)	Corr X1	Corr X2	Corr X3	Loss/Gain
1.07	10	-37.3	-21.3		-3.89	-36.47	-20.12		-16.23
1.12	10	-35.7	-18.8		-3.52	-34.84	-17.58		-14.06
1.17	10	-28.2	-15.5		-3.20	-27.31	-14.26		-11.06
1.07	12	-35.3	-17.2		-1.89	-34.47	-16.02		-14.13
1.12	12	-33.3	-14.7		-1.52	-32.44	-13.48		-11.96
1.17	12	-25	-11.2		-1.20	-24.11	-9.96		-8.76
1.07	14	-32.5	-12.7		0.12	-31.67	-11.52		-11.63
1.12	14	-29.7	-9.83		0.48	-28.84	-8.61		-9.09
1.17	14	-19.2	-5.7	-28.8	0.81	-18.31	-4.46	-27.27	-5.26
1.07	16	-27.2	-6.83	-31.7	2.12	-26.37	-5.65	-30.24	-7.76
1.12	16	-23	-4	-28.3	2.48	-22.14	-2.78	-26.79	-5.26
1.17	16	-14.3	-1.2	-27.5	2.81	-13.41	0.05	-25.97	-2.76
1.07	18	-23.7	-2.7	-32.5	**4.12**	-22.87	-1.52	-31.04	**-5.63**
1.12	18	-19.7	0.2	-29.3	**4.48**	-18.84	1.43	-27.79	**-3.06**
1.17	18	-13.3	1	-21.2	**4.81**	-12.41	2.25	-19.67	**-2.56**

The "fixed" doubler design draws about 90 mA at +5V, with VGS = -1.0 V. With about +4.5 dBm of input power, the doubled output at 1.12 GHz is +1.43 dBm vs. -11.0 dBm with an input of +4 dBm in the original flawed circuit. The corrected power levels for inputs of 1.07, 1.12, and 1.17 GHz are shown as input power (Pin(corr)), First Harmonic output (Corr X1), Doubled Output (Corr X2), and Third Harmonic output (Corr X3). Also shown is the corrected conversion loss in the last column.