JHU EE787 Fall 2002 MMIC Results

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Designs Fabricated by TriQuint Semiconductor

ADS Support by Gary Wray—Agilent

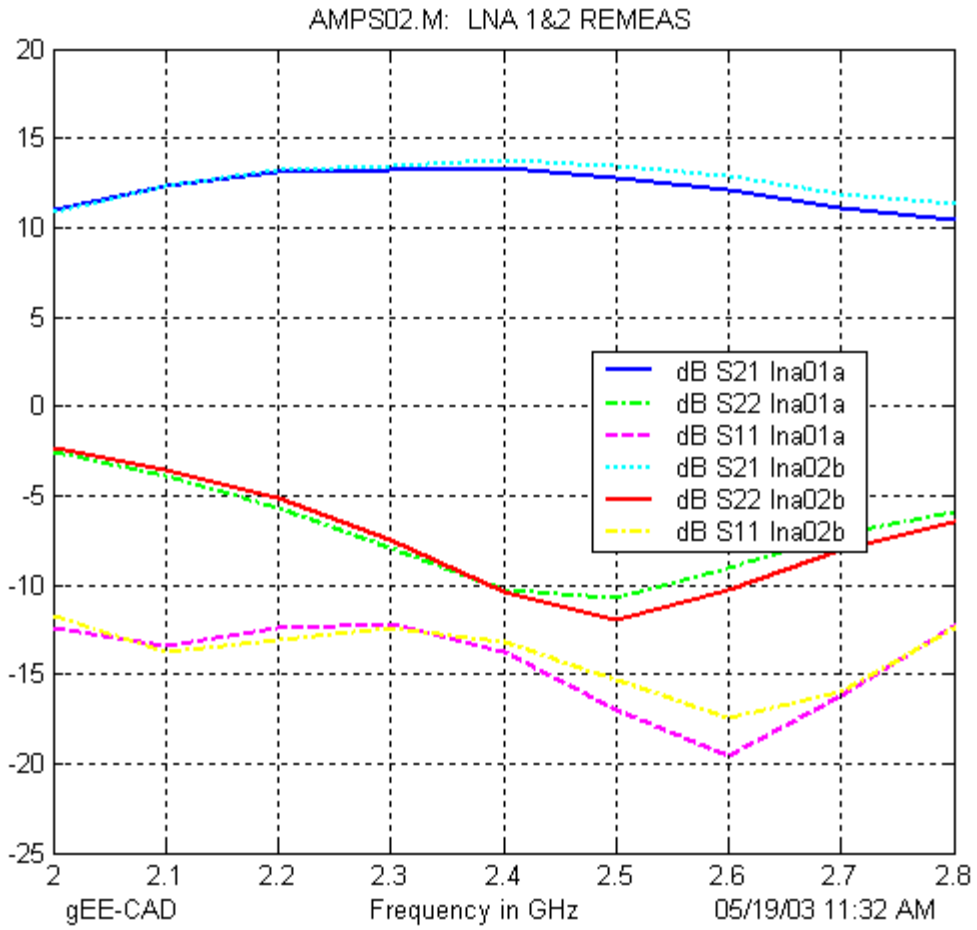
TriQuint TQTRX Library and ADS software used for student designs

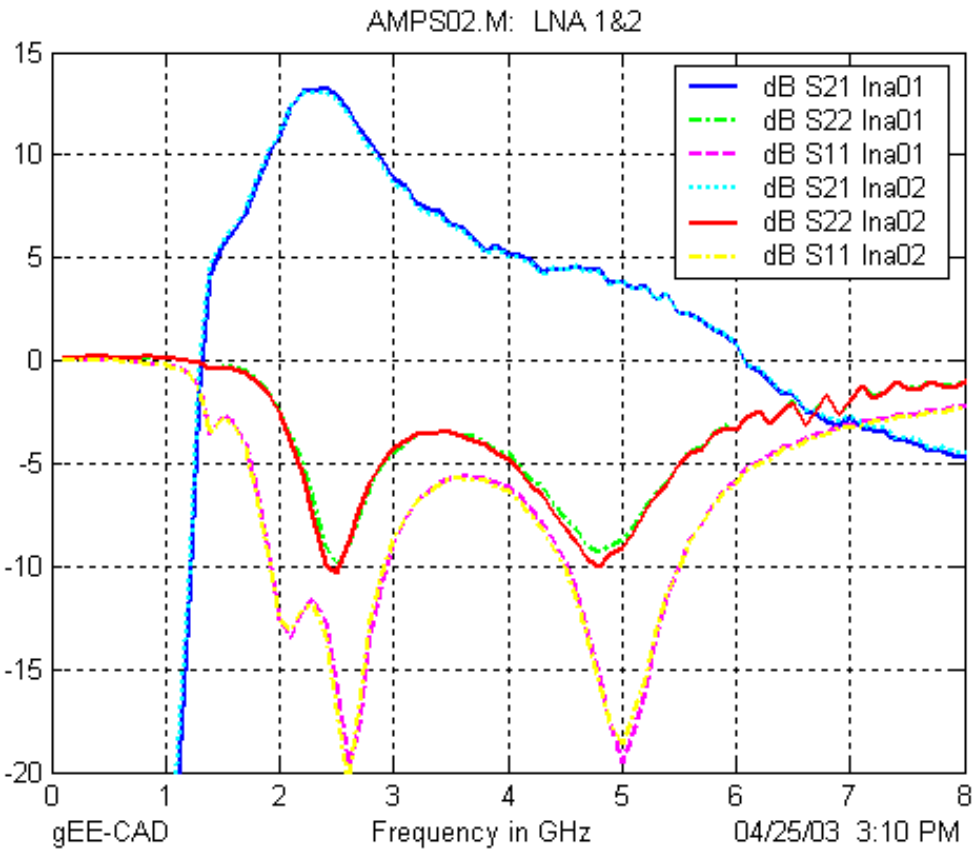
Six MMICs were designed by students for the Fall 2002 JHU MMIC Design Course as part of an S-Band duplex transceiver. The designs were intended to work in a system that could be used at the WCS band (2.305 to 2.360 GHz) or ISM band (2.4 to 2.497 GHz). All designs were tested in the Spring of 2003 after fabrication by TriQuint Semiconductor. Measurements compare favorably to simulations and all designs were successful with a minor layout glitch on the output amplifier stage of the doubler. Attached are plots of the results—small signal s-parameters and appropriate performance tests.

Thanks again to TriQuint and Agilent for their wonderful support of the JHU EE787 MMIC Design Course.

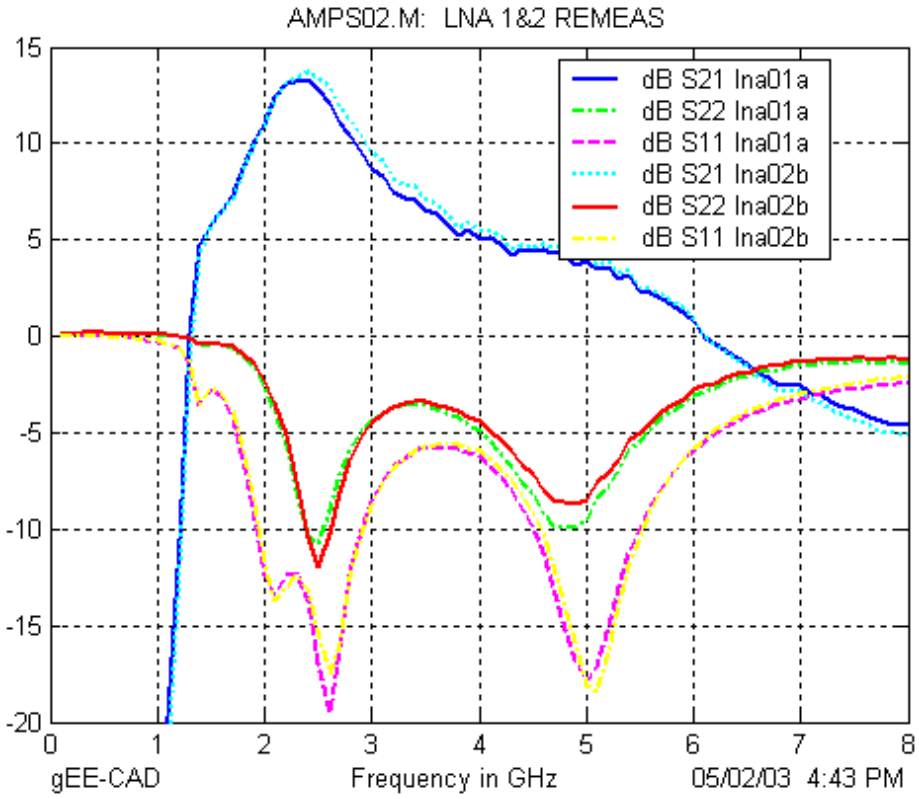
Low Noise Amplifier (S-Band) by Zhimin Li:

The LNA had about the correct bias and worked well comparing favorably with initial simulations. Bias at 5V was about 47 to 48 mA IDS which is only slightly higher than the simulated 43.4 mA for the single supply design. Following are plots showing 0 to 8 GHz measured performance. Below is an s-parameter plot to the same scale as in the original student report. Shape of S-parameters, particularly S11, is very similar to the final performance plots after layout. S21 is a couple of dB lower but similar in shape versus frequency. Measured noise figure is slightly higher than predicted but should have been slightly lower as it was measured with the probe station lights turned on. In fact the current dropped 1 or 2 mA with the lights out agreeing even more with the initial simulations. A later plot shows about 0.5 dB more gain with the lights out. Most of the measurements had the probe station lights on. Error in noise figure measurement is probably on the order of 0.25 dB or so.

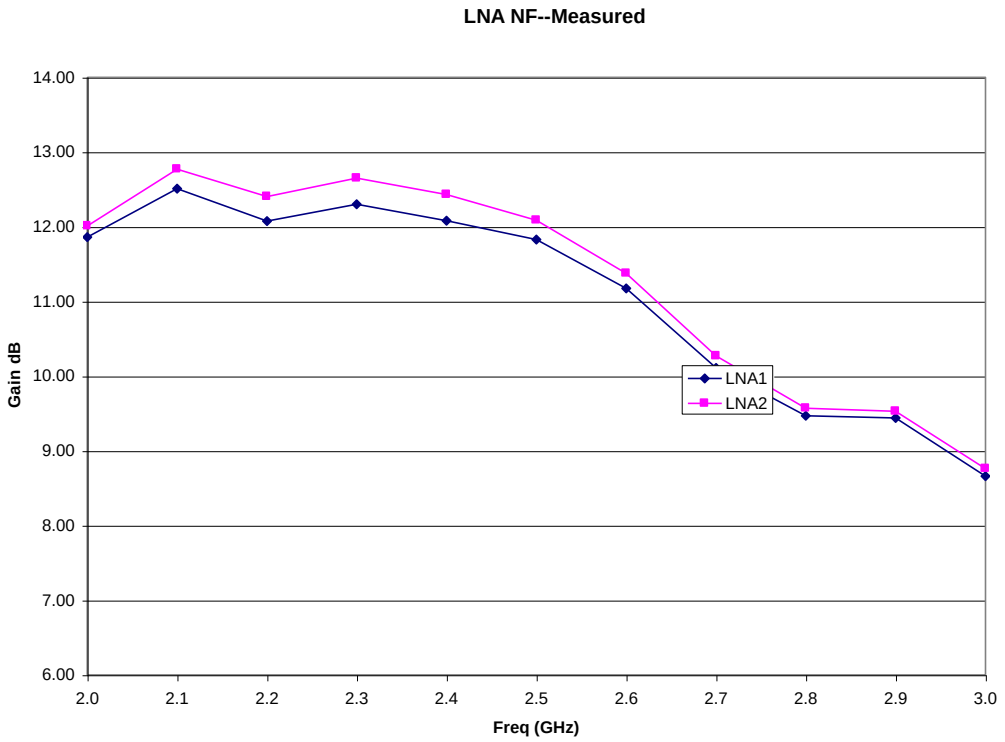




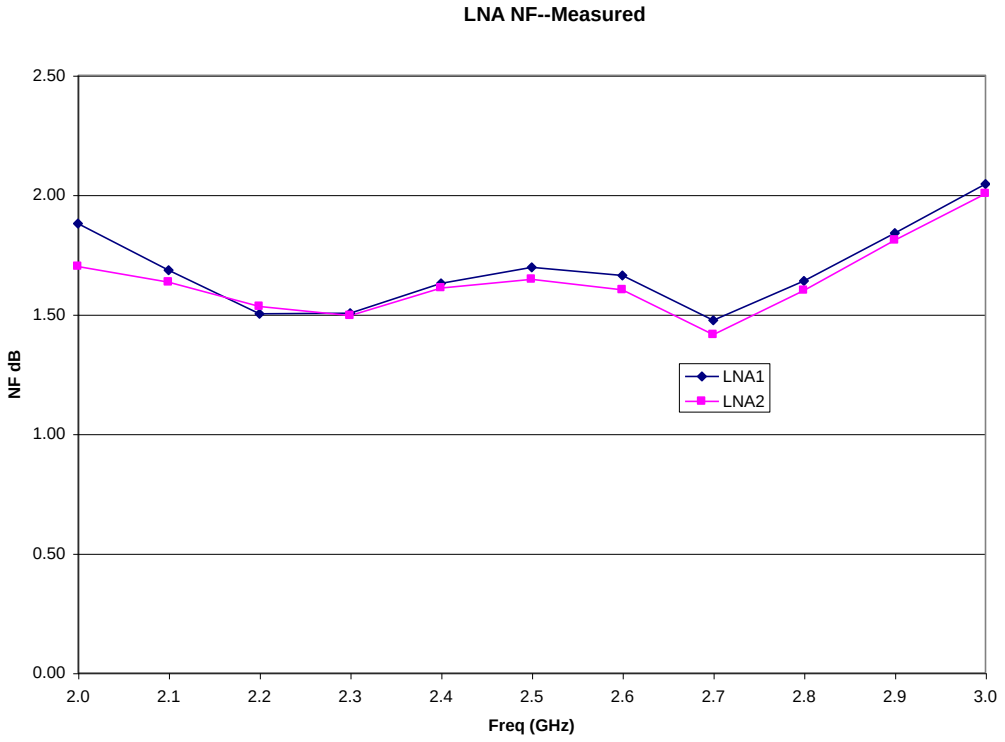
Measured at 5V at 47 - 48 mA for Two Die—LNA by Li Zhimin Fall 02 MMIC Class



ReMeasured at 5V at 46 - 48 mA for Two Die—LNA by Li Zhimin Fall 02 MMIC Class "B" with Lights OFF!



Gain Measured with Noise Figure Meter for LNA—Two Die (Corrected for Lossy Cable and Probe)



Noise Figure Measured for LNA—Two Die (Corrected for Lossy Cable and Probe)
Lights On—probably higher NF than with Light Off.

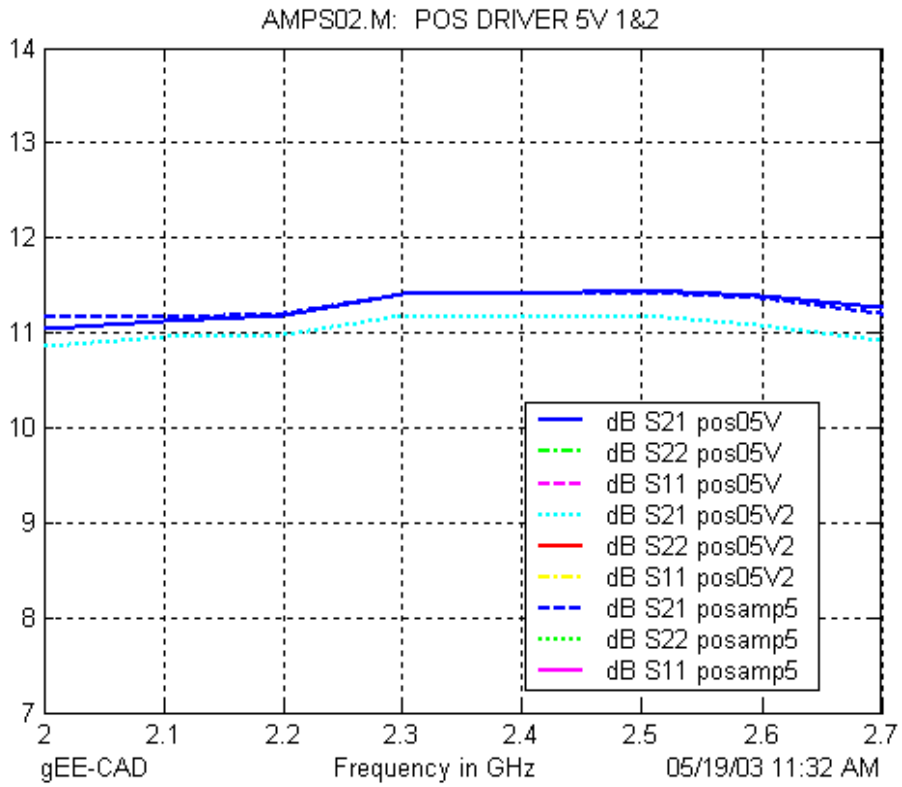
Post Amplifier (S-Band) by Kerron Duncan and Walter Tates:

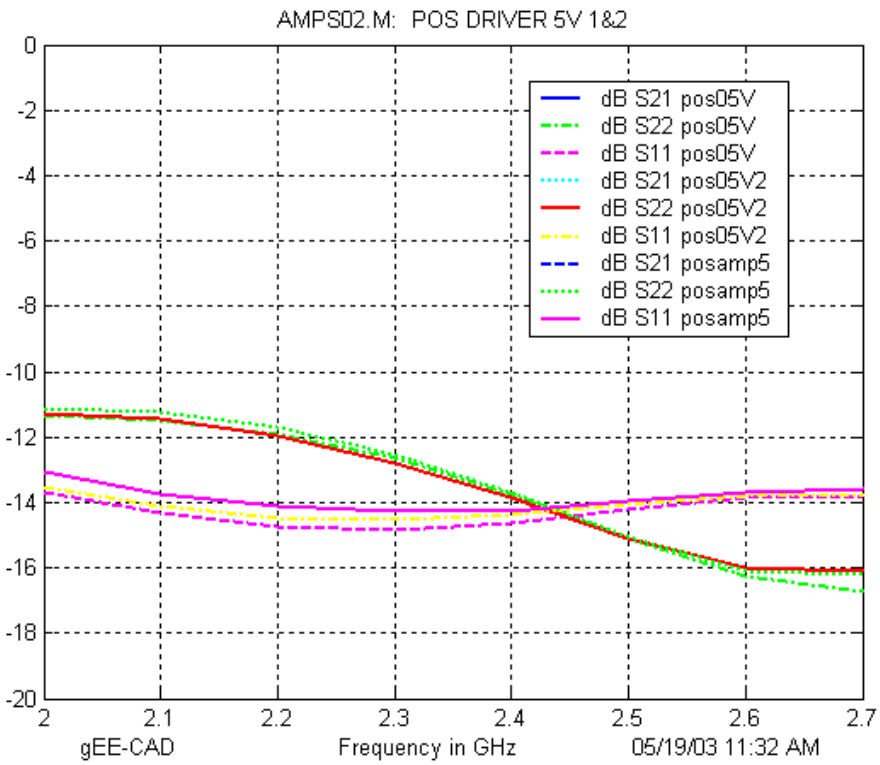
The driver amplifier had a simulated bias of 140 mA on the "+5V" supply and about 26 mA on the "–5V" supply. Measured bias for three die were close to the expected values (+5V at 120-125 mA, -5V at 25 mA). The DC power consumed by this small die was probably nearing the limit of power consumption for individual die with our JHU probe setup without attaching the die to a piece of metal as a heat sink. It seemed that the IDS current dropped slightly during measurement which may have affected the data somewhat. Gain was a little less than simulated as with the LNA. Plots below were over 2.0 to 2.7 GHz as were the original simulations in the student report (+5V,-5V). Later plots show the data over a broader frequency range and with the positive supply voltage at +3V, +4V, and +5V. Power output was measured versus input power at band center frequency 2.4 GHz and at a "sweet" spot of 2.43 GHz. A respectable 13.4% PAE was achieved at about 2 dB compression which compares well with an expected 15% PAE. Measured output power level was over 110 mW (+20.4 dBm).

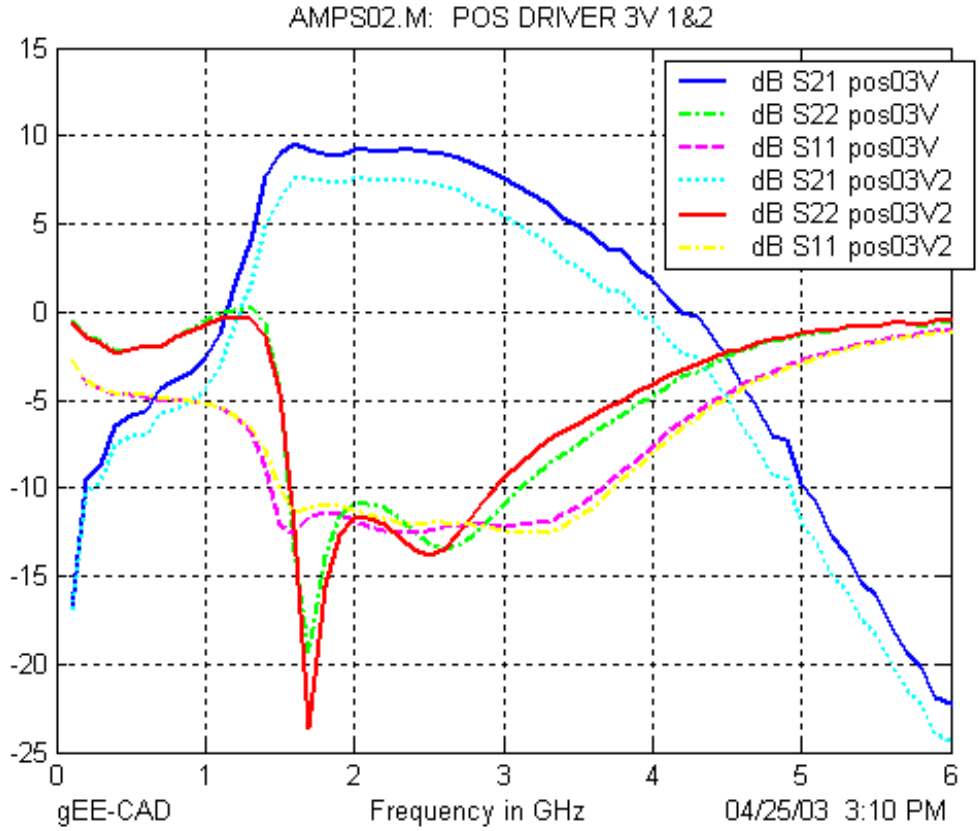
5V @ 120mA, -5V @ 25 mA #1 2.43 GHz

2.43 GHz Correction ~0.75 dB each side

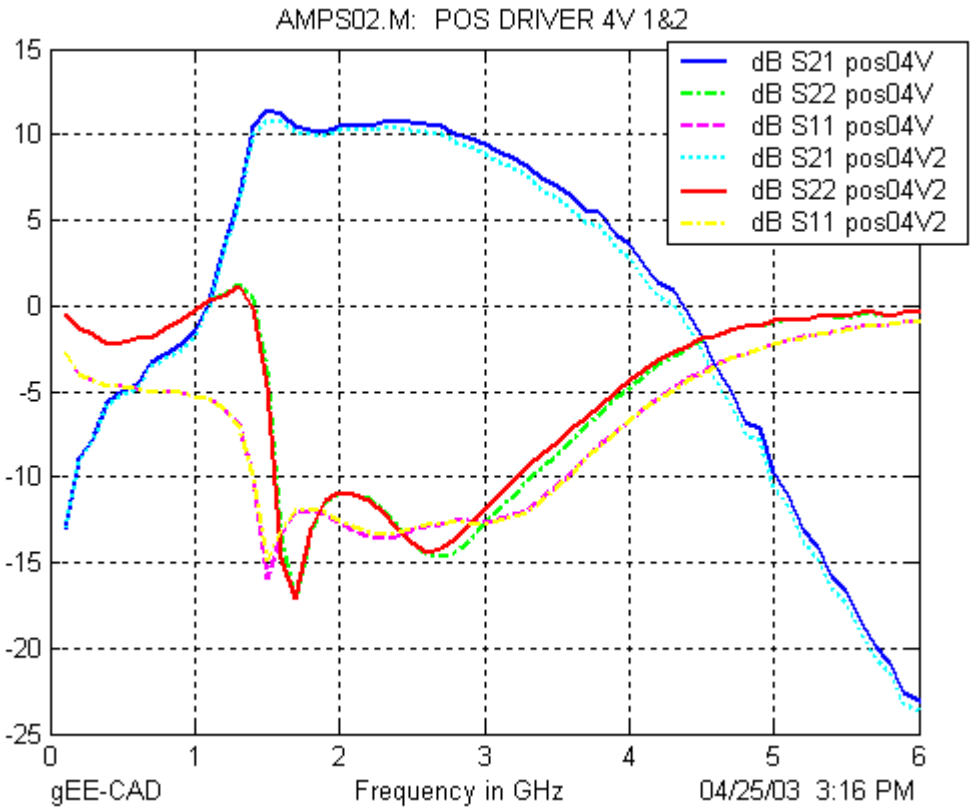
PIN (SG)	Pout (ms)	ID	Gain	Gain Cmp	Pout(Corr)	Pout(mW)	PAE
0.0	9.83	118	11.33		10.58	11.4	1.6%
2.0	11.83	118	11.33	0.00	12.58	18.1	2.5%
4.0	13.83	118	11.33	0.00	14.58	28.7	4.0%
6.0	16.00	118	11.50	0.17	16.75	47.3	6.6%
8.0	17.67	118	11.17	-0.16	18.42	69.5	9.7%
10.0	19.00	120	10.50	-0.83	19.75	94.4	12.7%
11.0	19.33	126	9.83	-1.50	20.08	101.9	12.9%
12.0	19.67	129	9.17	-2.16	20.42	110.2	13.4%



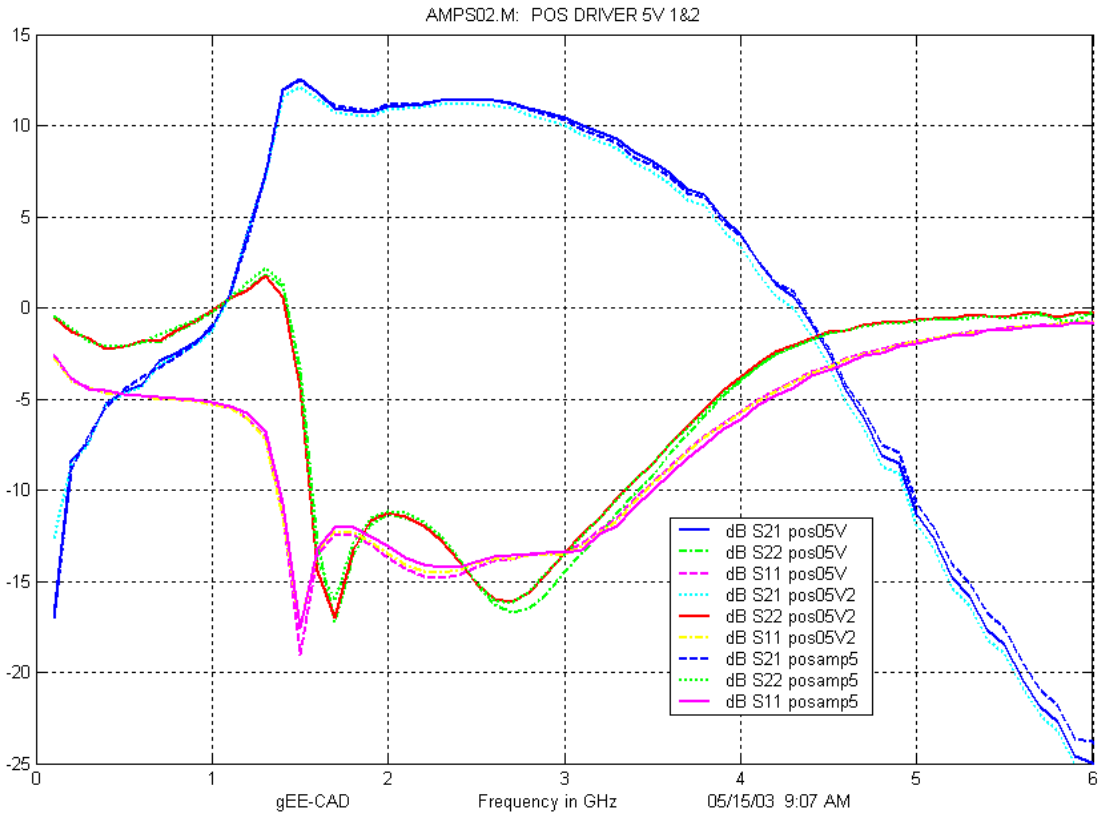




Measured at -5V/+3V for Two Die—Pos Driver Amp by W Tates & K Duncan Fall 02 MMIC Class



Measured at -5V/+4V for Two Die—Pos Driver Amp by W Tates & K Duncan Fall 02 MMIC Class



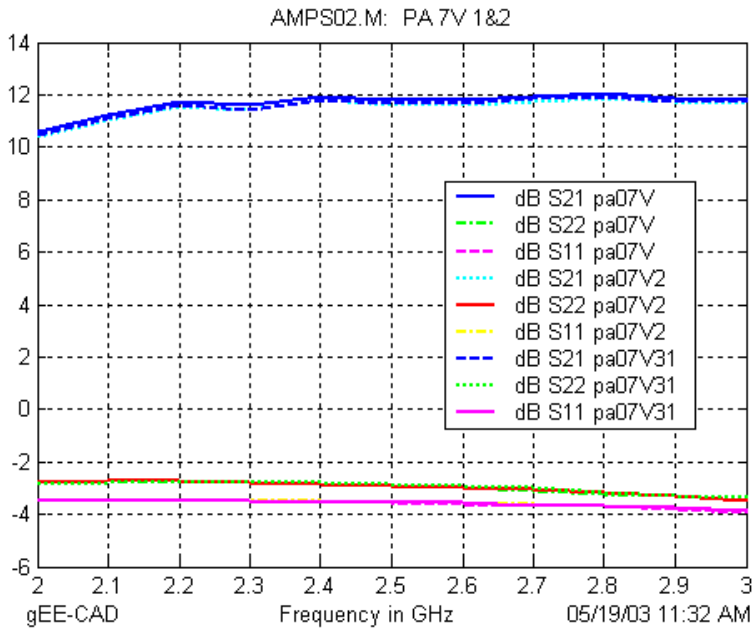
Measured at -5V/+5V for Three Die—Pos Driver Amp by W Tates & K Duncan Fall 02 MMIC Class

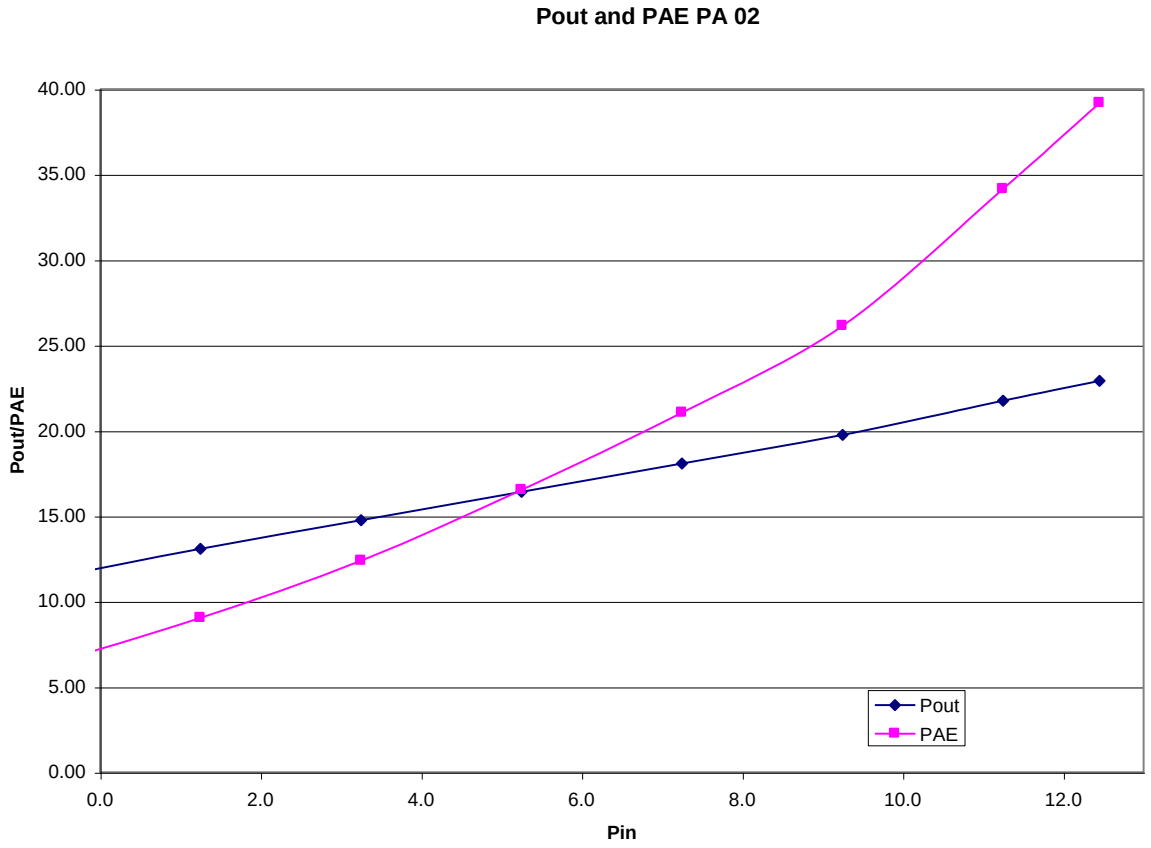
Power Amplifier (S-Band) by John Brice and Chris Giusto:

The power amplifier is a single stage design with a Class F output match. A bias of VGS—1.53V was simulated to have an IDS of 37 mA at the +7V drain bias. Two Measured die had drain currents of 31 and 33 mA which is close to expectations. Input and output match were poor as simulated in the original design but gain was reasonable as shown in the following broadband plots. Very high efficiencies were measured for this design and could probably be higher (see plot) but the signal generator used had a maximum output power of 13.2 dBm which presented about 12.5 dBm maximum at the die on the probe station. A simulated PAE of 37.5% was measured to be 39.2% at 2.44 GHz at a compression of about 1.5 dB. Measurements were made in the band center of 2.4 GHz and at a "sweet" spot in the band of 2.44 Ghz.

Power Amp Large Signal Measured 5/16/03
Measured CW at 2.4 GHz and then at 2.44 GHz sweet spot
Seemed pretty flat from 2.3 to 2.5 GHz over the band
7V @ 29mA, -1.53V @ 0 mA #1 2.4 GHz
2.4 GHz Correction ~0.75 dB each side

PIN (SG)	Pout (ms)	ID	Gain	Gain Cmp	Pout(Corr)	Pout(mW)	PAE
-10.0	-0.17	29	11.33		0.58	1.1	0.5%
-8.0	1.83	29	11.33	0.00	2.58	1.8	0.8%
-6.0	3.67	29	11.17	-0.16	4.42	2.8	1.3%
-4.0	5.67	29	11.17	-0.16	6.42	4.4	2.0%
-2.0	7.67	29	11.17	-0.16	8.42	7.0	3.2%
0.0	9.67	29	11.17	-0.16	10.42	11.0	5.0%
2.0	11.50	29	11.00	-0.33	12.25	16.8	7.6%
4.0	13.17	31	10.67	-0.66	13.92	24.7	10.4%
6.0	14.83	33	10.33	-1.00	15.58	36.1	14.2%
8.0	16.50	38	10.00	-1.33	17.25	53.1	18.0%
10.0	18.17	44	9.67	-1.66	18.92	78.0	22.6%
12.0	20.00	53	9.50	-1.83	20.75	118.9	28.4%
13.2	21.30	60	9.60	-1.73	22.05	160.3	34.0%





Measured Power Output and PAE—Amplifier does not appear to be saturated at highest Pin.

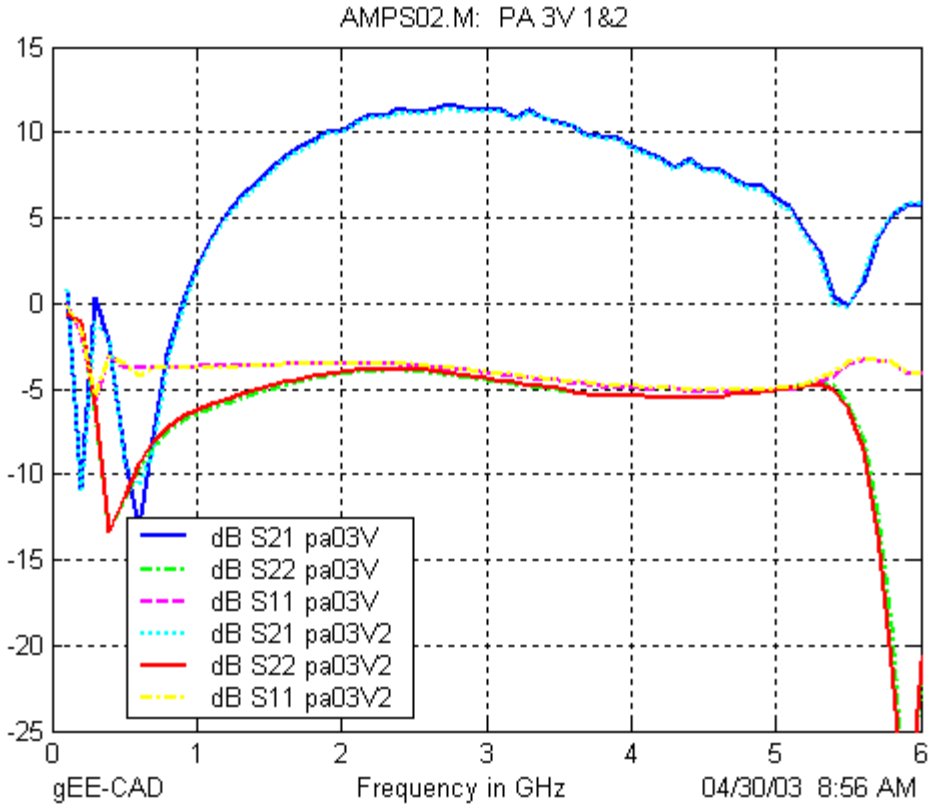
7V @ 29mA, -1.53V @ 0 mA #1 2.44 GHz
2.44 GHz Correction ~0.75 dB each side

PIN (SG)	Pout (ms)	ID	Gain	Gain Cmp	Pout(Corr)	Pout(mW)	PAE	PAE*100	Pin(corr)
0.0	10.50	29	12.00		11.25	13.3	6.2%	6.2	-0.8
2.0	12.33	30	11.83	-0.17	13.08	20.3	9.0%	9.0	1.3
4.0	14.00	32	11.50	-0.50	14.75	29.9	12.4%	12.4	3.3
6.0	15.67	35	11.17	-0.83	16.42	43.9	16.5%	16.5	5.3
8.0	17.33	40	10.83	-1.17	18.08	64.3	21.1%	21.1	7.3
10.0	19.00	47	10.50	-1.50	19.75	94.4	26.1%	26.1	9.3
12.0	21.00	57	10.50	-1.50	21.75	149.6	34.2%	34.2	11.3
13.2	22.17	65	10.47	-1.53	22.92	**195.9**	**39.2%**	39.2	12.5

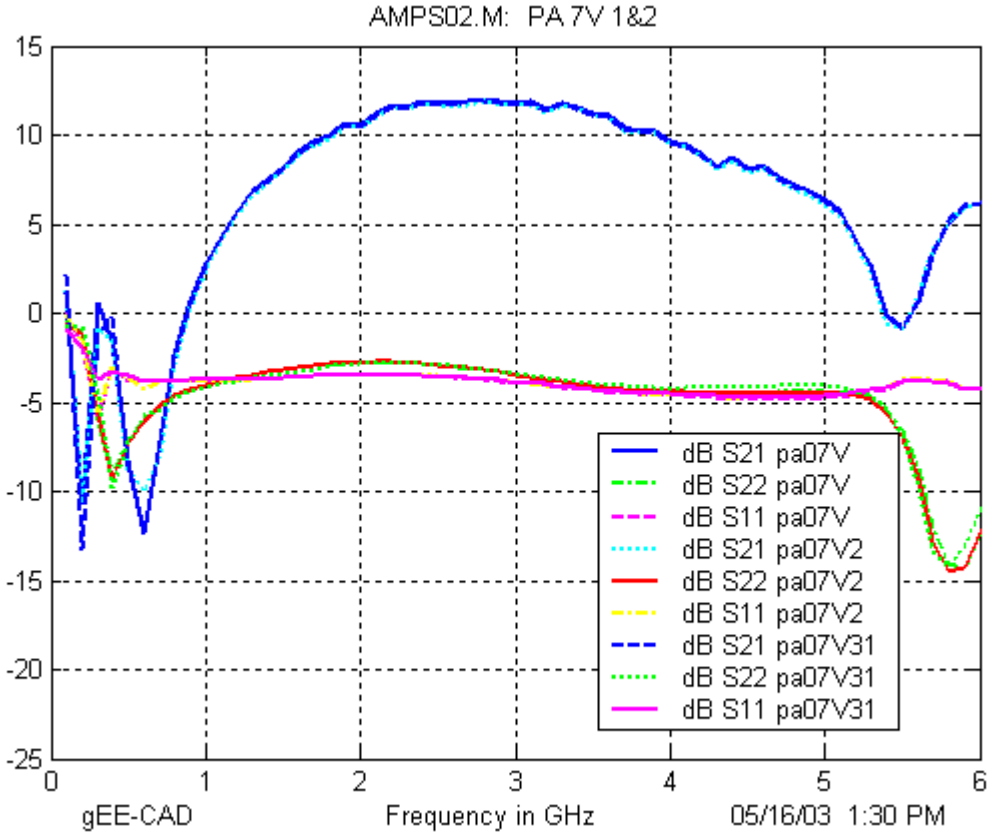
7V @ 32mA, -1.53V @ 0 mA #1 2.44 GHz
2.44 GHz Correction ~0.75 dB each side

PIN (SG)	Pout (ms)	ID	Gain	Gain Cmp	Pout(Corr)	Pout(mW)	PAE
0.0	10.67	32	12.17		11.42	13.9	5.8%
2.0	12.50	32	12.00	-0.17	13.25	21.1	8.8%
4.0	15.33	34	12.83	0.66	16.08	40.6	16.2%
6.0	16.00	37	11.50	-0.67	16.75	47.3	17.0%
8.0	17.67	42	11.17	-1.00	18.42	69.5	21.8%
10.0	18.83	50	10.33	-1.84	19.58	90.8	23.5%
12.0	20.83	59	10.33	-1.84	21.58	143.9	31.6%
13.2	22.00	67	10.30	-1.87	22.75	**188.4**	**36.4%**

Measured at –1.53V/+3V for Two Die—Power Amp by C Giusto & J Brice Fall 02 MMIC Class

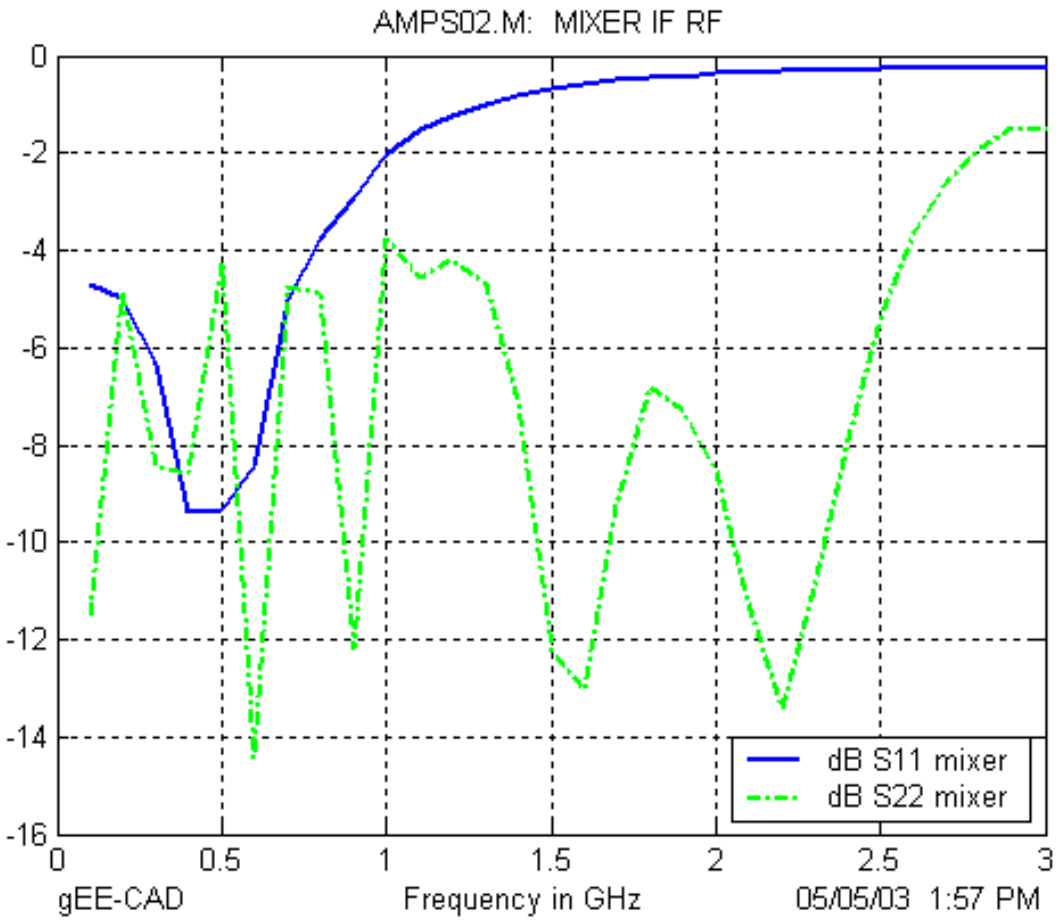


Measured at –1.53V/+7V for Two Die—Power Amp by C Giusto & J Brice Fall 02 MMIC Class



Up/Down Mixer (S-Band) by Jeff Jaso:

The mixer is a diode based design for up/down conversion with an LO of 2.24 Ghz nominal and an IF of 160 MHz. Conversion loss in the up/down cases was measured as well as s-parameters for the IF and RF inputs as shown in the following plot. Bias was 5V at about 1 mA which matches simulations. Mmeasured up/down conversion losses at various LO drives and with no DC bias (+7 dBm LO only) are shown.



Mixer Match—5V 1mA bias with LO ON, s11=IF, s22=RF

Measured Conversion Loss Up/Down

UP Conversion

IF(160M)=-15 dBm LO=2.24 GHz **Assume 1 dB loss for cable plus RF Probe, 0.4 dB at IF**

Bias 5V 1mA 2.08G 2.4G

LO Pwr	IF(160)	LO-IF	LO	LO+IF	ConvLoss	LO/RF Iso	IF/RF Iso
-4	-28.8	-28.0	-35.3	-29.2	13.2	30.3	13.4
-2	-28.8	-26.7	-32.5	-27.8	11.8	29.5	13.4
0	-29.0	-26.2	-30.5	-27.2	11.2	29.5	13.6
2	-29.0	-25.8	-28.8	-27.0	11.0	29.8	13.6
4	-29.0	-25.7	-27.5	-26.7	10.7	30.5	13.6
7	-29.0	-25.3	-25.5	-26.0	10.0	31.5	13.6
NO Bias							
7	-41.3	-29.8	-27.7	-29.2	13.2	33.7	25.9

DOWN Conversion

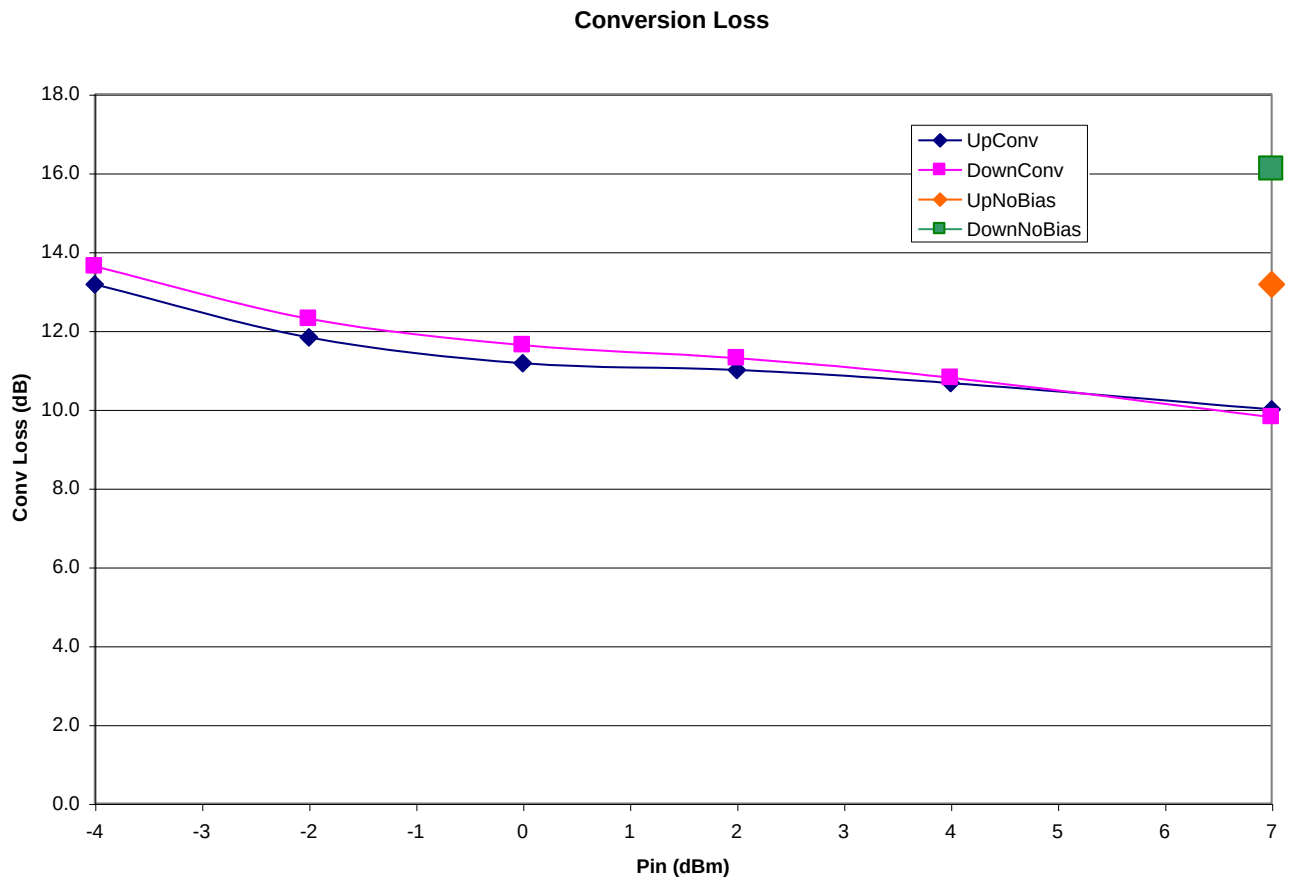
RF(2.4G)=-14.8 dBm LO=2.24 GHz **Assume 1 dB loss for cable plus RF Probe, 0.4 dB at IF**

Bias 5V 1mA

LO Pwr	IF(160)	LO	RF	ConvLoss	LO/IF Iso	RF/IF Iso
-4	-28.8	-53.5	-50.2	13.6	48.5	34.4
-2	-27.5	-51.7	-50.0	12.3	48.7	34.2
0	-26.8	-49.3	-49.8	11.6	48.3	34.0
2	-26.5	-47.3	-49.8	11.3	48.3	34.0
4	-26.0	-45.0	-49.8	10.8	48.0	34.0
7	-25.0	-42.0	-50.0	9.8	48.0	34.2

NO Bias

7	-31.3	-40.3	-51.7	16.1	46.3	35.9



Conversion Loss Up/Down with LO drive--+5V @ 1mA bias through diodes except as noted

Voltage Controlled Oscillator (VCO) by Mark Petty:

The VCO was designed to generate a signal tunable from 1.07 to 1.17 GHz which would then be doubled as part of the system concept. Output power was very respectable and tuning range covered most of the band of operation. Original simulations showed that the VCO might be a little low in frequency and possibly the capacitance variation. However, the design is within 2% of predictions which is remarkable for a first time student design. Attached are measured output power and frequency versus the tuning voltage of 0V to 5V. Bias is a single supply of +5V at 74 mA (a little lower than the 86 mA predicted but very close). Output power is as high as 18.5 dBm (add 0.5 dB to measured data) which is very close to the +19 dBm expected output power. The signal was also very clean and sinusoidal. Note the very low 2nd, 3rd, and 4th harmonics as measured.

ReTest 5/7/03 Assume ~0.5 dB loss for cable and probe?
Lights OFF!
5V @ 77 mA VCO #1

Tun (V)	Freq	P(meas)	X2	X3	X4
0.0	1.005	17.8	-40.0	-19.3	-25.5
0.5	1.012	17.8	-42.0	-18.2	-24.5
1.0	1.036	18.0	-41.2	-17.5	-23.3
1.5	1.058	18.0	-36.8	-18.3	-22.7
2.0	1.084	17.7	-34.2	-21.2	-23.7
2.5	1.113	17.0	-32.8	-25.3	-25.7
3.0	1.133	17.0	-29.8	-26.5	-25.7
3.5	1.142	16.8	-29.0	-27.8	-25.7
4.0	1.147	16.8	-28.7	-28.3	-25.8
4.5	1.151	16.7	-28.0	-28.5	-25.5
5.0	1.155	16.7	-27.8	-28.7	-25.3

A second die had similar performance but stopped oscillating when the tuning voltage exceeded 3.3V.

5V @ 76 mA VCO #2

Tun (V)	Freq	P(meas)
0.0	1.008	17.3
0.5	1.014	18.0
1.0	1.038	18.0
1.5	1.060	18.0
2.0	1.085	17.5
2.5	1.114	16.5
3.0	1.133	16.2
3.3	1.138	15.7

Stops Oscilating beyond 3.3V

Frequency Doubler by Ming-Zhi Lai:

The frequency doubler was to take the VCO output (1.07 to 1.17 GHz) and double it to act as the LO for the Mixer (2.14 to 2.34 GHz). For the doubler design, the input signal is split by a lumped element equivalent of a 180 degree hybrid then fed to two identical Class B amplifiers and combined to cancel the fundamental harmonic. An amplifier stage then amplifies the second harmonic and should further attenuate the undesired harmonics. Apparently a mistake slipped by the instructor, me, as I tried to squeeze the students original layout into the desired die size and tie all the DC biases together. The measured bias matched that of the doubler section with two Class B amplifiers but did not include the 110 mA of the output driver stage. Essentially with the final stage gate biased at –0.6V, the output combiner was not symmetric and the output FET was acting like a shunt switch to ground attenuating the desired signal. With –3.0V on the gate of the output stage, the output of the doubler section could be seen as leakage through the capacitance of the "OFF" output FET. A minor change to correct the output stage connection to +5V along with widening some lines to carry the additional 110 mA for the output stage has been completed. The hope is to re-fabricate and retest this design in the future. Not only should the output level be amplified as shown in the following measured data, but the harmonics will likely be attenuated relative to the desired "doubled" harmonic.

Measured Doubler--Error in +5V connection on output stage.

X2 #1 5V @ 26 mA, -5V @ 2 mA, and VG=-0.6V

X2 #2 5V @ 27 mA, -5V @ 2 mA, and VG=-0.6V

Measured S-parameters for 2 die, should have OK input match, output match should be OFF.

Looks like correct bias for class B amplifiers of doubler section.

Output stage looks like 6 element switch model in off position with 2nd meas with VG=-3V.

Input = 1.12 GHz 5V @ 30 mA, -5V @ 2mA, VG=-3.0V

SG (Pset)	X1	X2	X3	X4
0	-16.8	-17.7	-46.3	-45.3
2	-14.5	-14.3	-43.5	-39.7
4	-12.0	-11.0	-37.0	-35.2
6	-9.0	-7.3	-29.0	-31.7
8	-5.3	-2.8	-21.5	-27.8
10	-3.5	1.3	-17.2	-22.0

Input = 1.12 GHz 5V @ 28 mA, -5V @ 2mA, VG~-0.6V

SG (Pset)	X1	X2	X3	X4
0	-29.0	-27.5	-54.7	-55.7
2	-27.2	-24.2	-54.0	-51.3
4	-24.8	-21.0	-54.0	-46.7
6	-22.0	-18.0	-47.3	-41.5
8	-18.5	-14.8	-35.3	-37.3
10	-14.3	-11.3	-28.5	-37.5
1.17G 10	-15.7	-13.0	-29.3	-37.5
1.07G 10	-17.5	-13.0	-29.7	-35.0