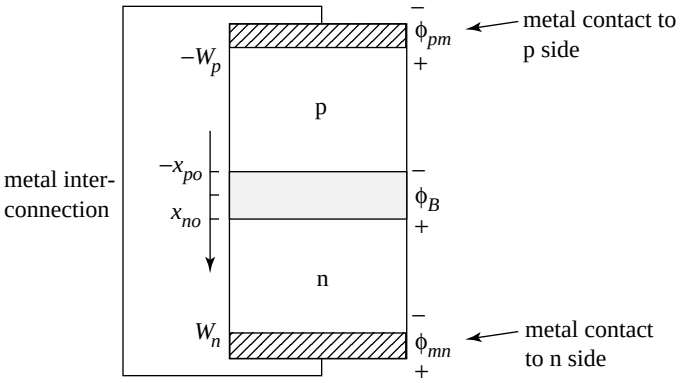
pn Junction under Reverse Bias

- First, we must understand the *complete* structure of the pn junction-- starting in thermal equilibrium:



- How can $V_D = 0$ and the built-in potential barrier be $\phi_B = 1$ V (approx.)?

  Answer: look at the complete circuit ... including the potential barriers at the p-type silicon-to-metal (ϕ_{pm}) and the metal-to-n-type silicon (ϕ_{mn}) junctions.

- Kirchhoff's Voltage Law:

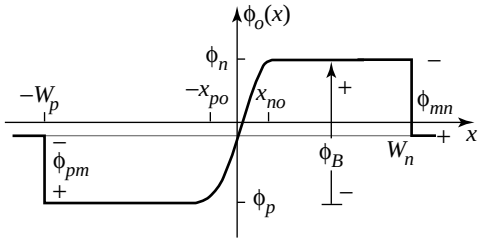
$$0 = \phi_{pm} + \phi_B + \phi_{mn}$$

  therefore, the built-in voltage is given by:

$$\phi_B = -\phi_{pm} - \phi_{mn}$$

Potential Plot through pn Junction

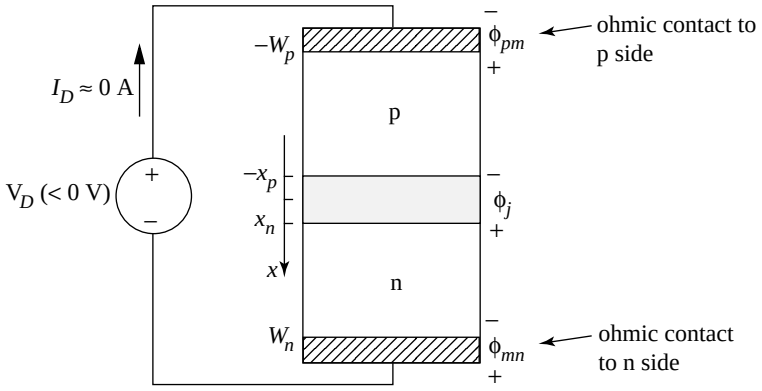
- The potential in the metal is the same on both ends of the pn junction in thermal equilibrium, with the metal-semiconductor contact potentials ("batteries") cancelling out the built-in potential



(b)

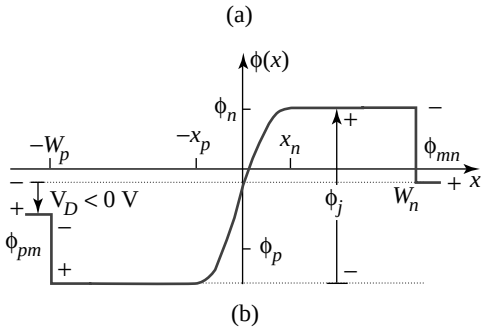
Note: we show potential changes at metal-silicon contacts as vertical, which is *not* correct. The details are left for an advanced device physics course.

- Now we apply a battery V_D ... with $V_D < 0$ (reverse bias)



pn Junction under Reverse Bias (cont.)

- Potential plot under reverse bias: contact potentials don't change ... they are *ohmic* contacts. Only place for change is at the pn junction

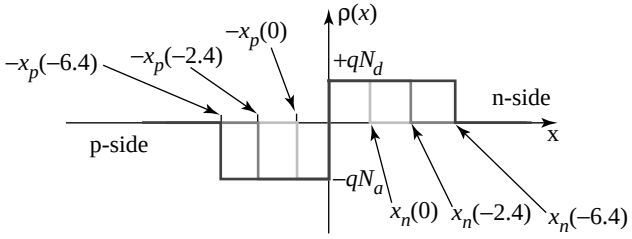


- The new potential barrier is called ϕ_j

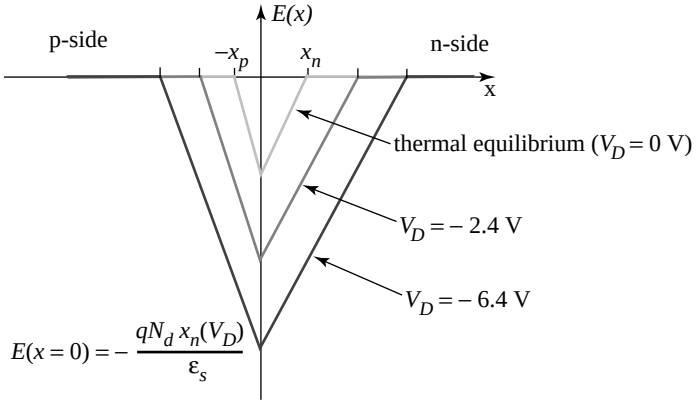
$$\text{KVL:} \qquad -V_D - \phi_{pm} - \phi_j - \phi_{mn} = 0$$

$$\phi_j = (-\phi_{pm} - \phi_{mn}) - V_D = \phi_B - V_D$$

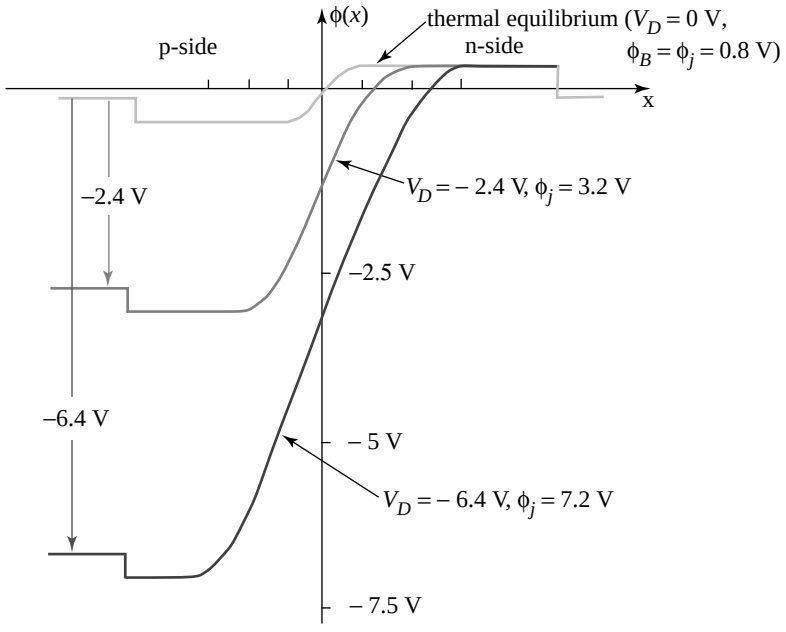
- The potential barrier is *increased* over the built-in barrier by the reverse bias ... which widens the depletion region ($x_n > x_{no}$, $x_p > x_{po}$)


ρ(x)
$-x_p(-6.4)$
$-x_p(-2.4)$
$-x_p(0)$
$+qN_d$
n-side
x
p-side
$-qN_a$
$x_n(0)$
$x_n(-2.4)$
$x_n(-6.4)$

(a)


E(x)
p-side
$-x_p$
x_n
n-side
x
thermal equilibrium ($V_D = 0$ V)
$V_D = -2.4$ V
$V_D = -6.4$ V
$E(x=0) = -\frac{qN_d\, x_n(V_D)}{\varepsilon_s}$

(b)


ϕ(x)
thermal equilibrium ($V_D = 0$ V,
$\phi_B = \phi_j = 0.8$ V)
p-side
n-side
x
$V_D = -2.4$ V, $\phi_j = 3.2$ V
–2.4 V
–2.5 V
–6.4 V
– 5 V
$V_D = -6.4$ V, $\phi_j = 7.2$ V
– 7.5 V

(c)

Quantitative Results

- Substitute ϕ_j for ϕ_B in the equilibrium depletion width and we find the depletion width under reverse bias (the math is the same):

$$x_p(V_D) = \sqrt{\left(\frac{2\varepsilon_s(\phi_B - V_D)}{qN_a}\right)\left(\frac{N_d}{N_d + N_a}\right)} = x_{po}\sqrt{1 - (V_D/\phi_B)}$$

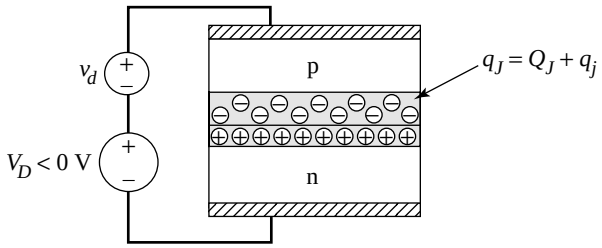
$$x_n(V_D) = \sqrt{\left(\frac{2\varepsilon_s(\phi_B - V_D)}{qN_d}\right)\left(\frac{N_a}{N_d + N_a}\right)} = x_{no}\sqrt{1 - (V_D/\phi_B)}$$

$$X_d(V_D) = \sqrt{\left(\frac{2\varepsilon_s(\phi_B - V_D)}{q}\right)\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} = X_{do}\sqrt{1 - (V_D/\phi_B)}$$

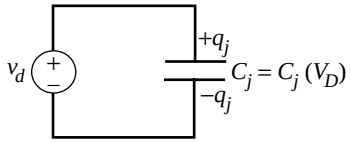
- Note x_{po}, x_{no}, and X_{do} are the widths in thermal equilibrium

Capacitance

- Basic circuits: $C = Q / V$ ... linear capacitor
- Semiconductor devices: $C = dq / dv$ ... nonlinear charge-storage --> capacitance is defined as a *small signal* quantity



(a)



(b)

Symbols:

* break up the total applied voltage (symbol: v_D) into two parts:

total voltage = DC voltage + small-signal voltage

$$v_D = V_D + v_d$$

* break up the charge q_J on the p-side of the junction similarly:

total charge in the depletion region = DC charge + small-signal charge

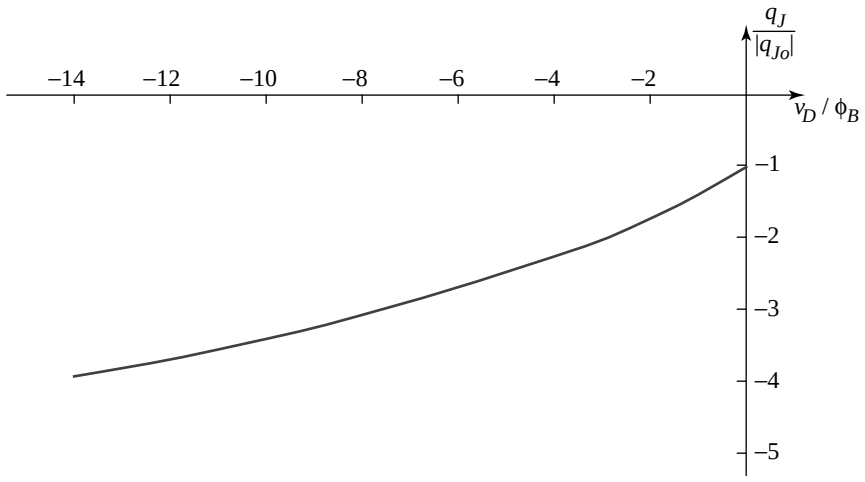
$$q_J = Q_J + q_j$$

Depletion Capacitance

- Find the function $q_J = q_J(v_D)$ from $x_p(v_D)$:

$$q_J(v_D) = -qN_a x_p(v_D) = -qN_a x_{po}\sqrt{1-(v_D/\phi_B)}$$

- Normalized plot:



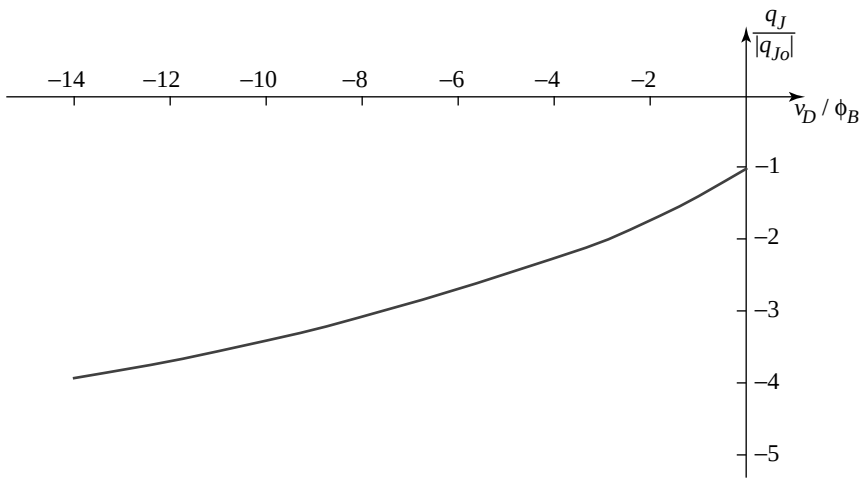
- To find the depletion capacitance C_j we simply take the derivative and evaluate it at the particular DC voltage

$$C_j = C_j(V_D) = \left.\frac{dq_J}{dv_D}\right|_{V_D}$$

- Math --> no insight into the *concept* of capacitance!

Graphical Interpretation

- Derivative is the *slope* of the plot of $q_J(v_D)$:

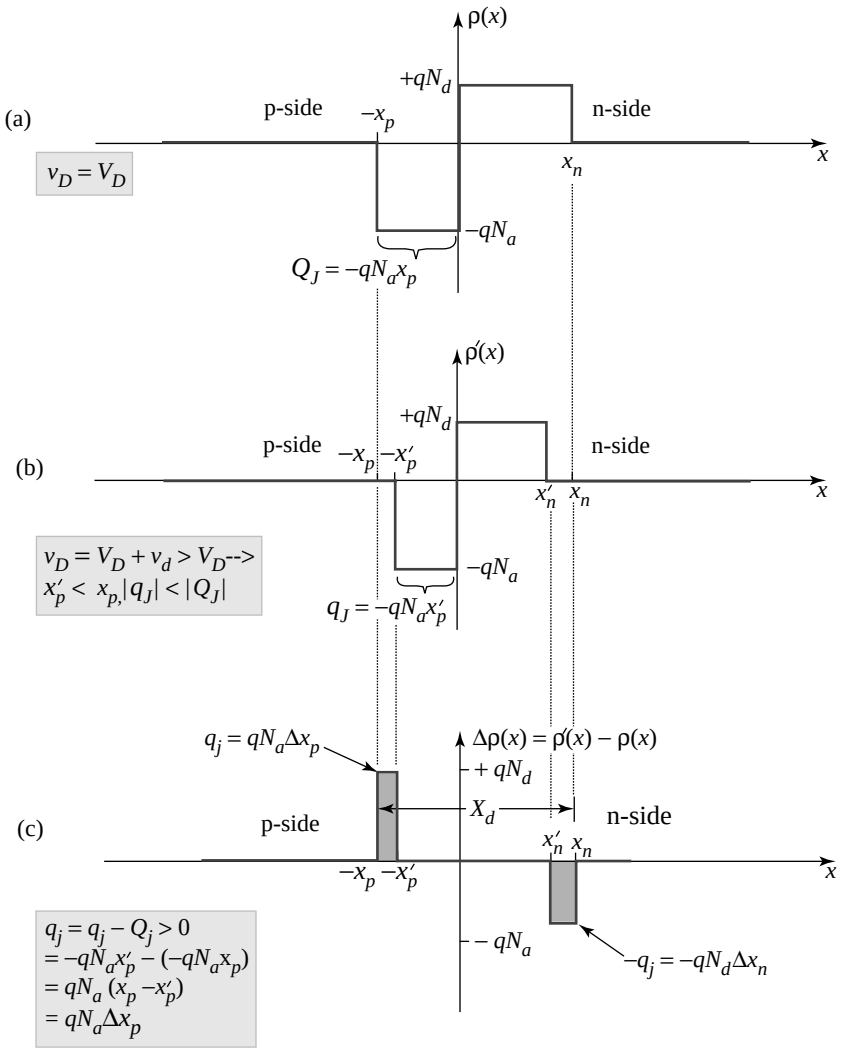


- The small-signal charge is related to the small-signal voltage by the slope at point (Q_J, V_J):

$$q_j = \left(\left. \frac{dq_J}{dv_D} \right|_{V_D} \right) \cdot v_d = C_j(V_D) \cdot v_d$$

Physical Interpretation

- Small-signal voltage changes the depletion width ($v_d > 0$ --> reverse bias is reduced --> depletion width is slightly narrower)

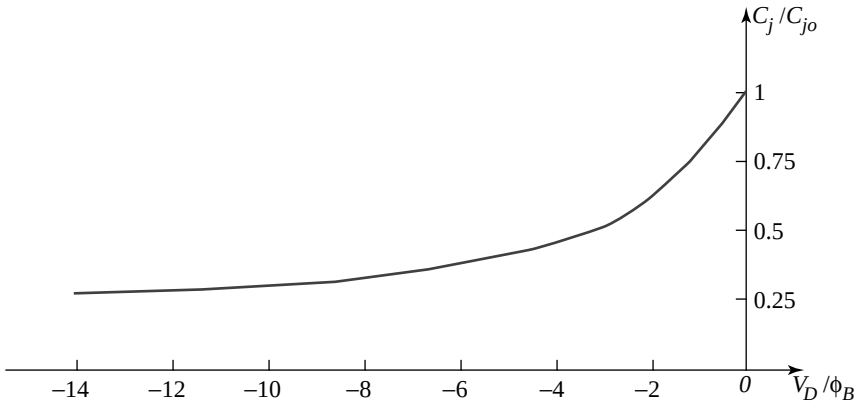


Depletion Capacitance Equation

- Derivative can be evaluated (see Chapter 3), but the incremental charge is two sheets separated by a distance $X_d(V_D)$ --> use parallel plate capacitor formula:

$$C_j = \frac{q_j}{v_d} = \frac{\varepsilon_s}{X_d(V_D)} = \frac{\varepsilon_s}{X_{do}\sqrt{1 - V_D/\phi_B}} = \frac{C_{jo}}{\sqrt{1 - V_D/\phi_B}}$$

- Plot of depletion capacitance (normalized to C_{jo}):

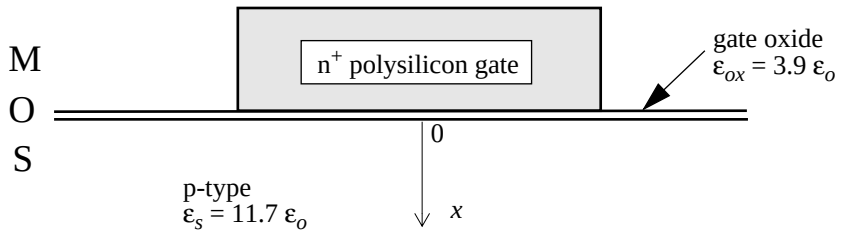


Typical numbers: X_{do} = 0.4 μm --> C_{jo} = 2.6 x 10^{-8} F/cm^2 = 0.26 fF/μm^2

ϕ_B = 0.8 V --> V_D = - 6.4 V = - 8 ϕ_B -->

$(1 - V_D / \phi_B)^{1/2}$ = 3 --> $C_j = C_{jo} / 3$ = 86 aF/μm^2

The MOS Capacitor



Oxide = SiO_2 ... a near-perfect insulator. We assume zero charge in the oxide for this course --> electric field is constant and potential is linear in the oxide.

n^+ polysilicon has a potential which is the maximum possible in silicon:

$$\phi_{n+} = 550 \text{ mV}$$

p-type substrate has potential which is $\phi_p = -60 \text{ mV} \log (N_a / 10^{10})$

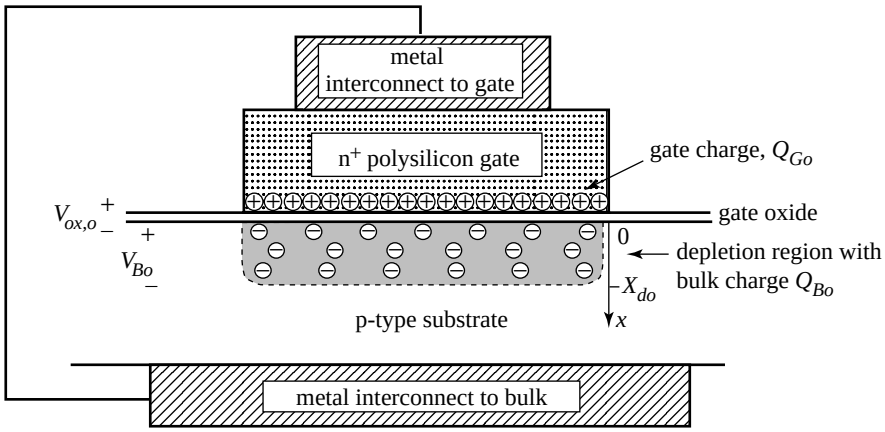
- Strategy: same as pn junction electrostatics

  first thermal equilibrium, then

  with an applied bias voltage

Qualitative Charge Distribution in Thermal Equilibrium

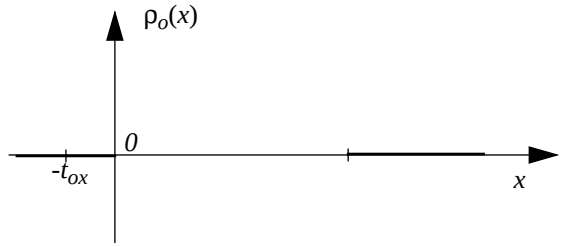
- Where to start: potential in n^+ polysilicon is known; potential in p-type substrate is known, too ... need + charge on gate, - charge in substrate --> since the silicon is p-type, this means that a depletion region forms under the gate



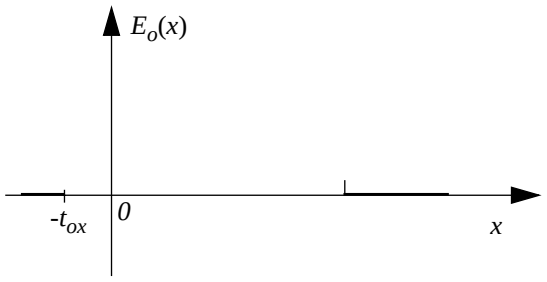
Thermal Equilibrium MOS Electrostatics

- Sketch charge density, electric field, and potential in equilibrium

charge density



electric field



potential