ADVANCES IN CHIP LEVEL PACKAGING

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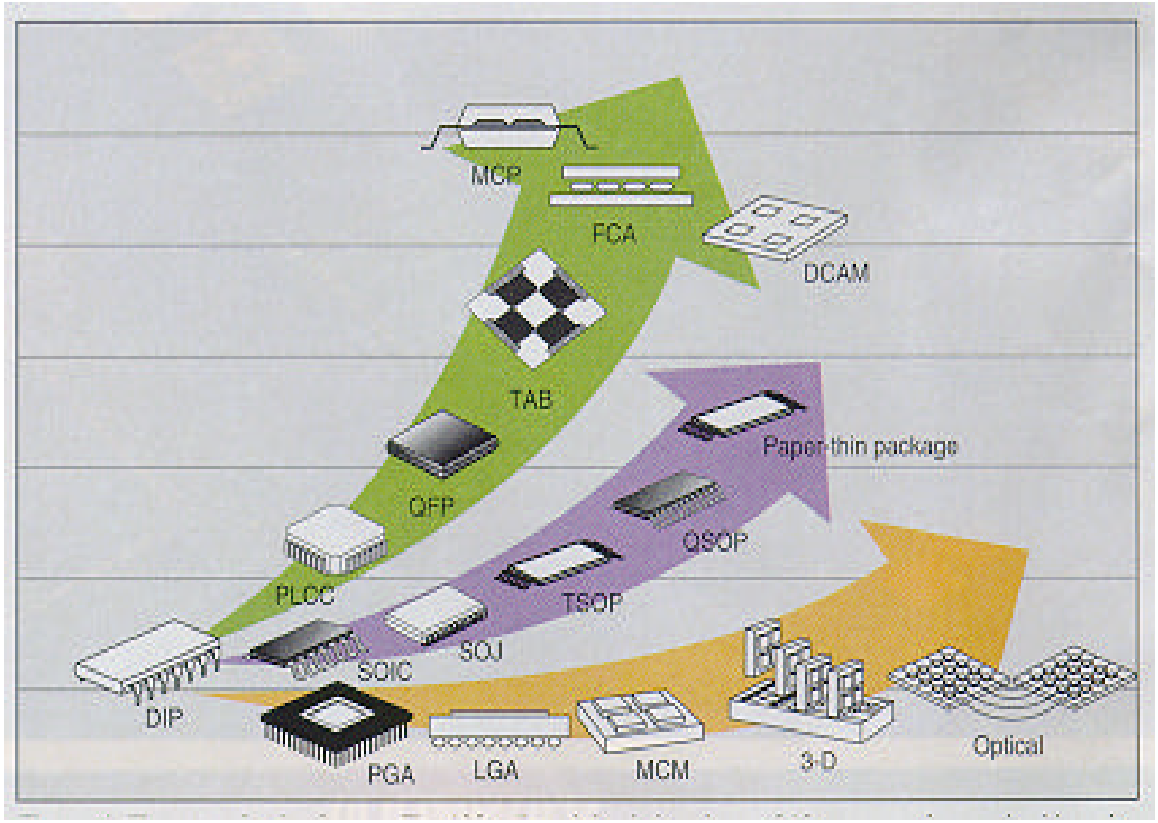
DIFFERENT TRENDS IN PACKAGING



(from R. Heitmann, Universal Instruments Inc. - EPP May 1996)

Excerpts from SIA Roadmap for Cost/Performance Category

	1995-2000	**2000-2005**	**2005-2010**
feature size (μm)	0.35-0.25	0.18-0.13	0.10-0.07
transistors/cm^2	4M-7M	13M- 25M	50M-120M
pin count	300-1000	1200-2000	2400-3600
package thickness (mm)	1.0- 2.0	1.0	0.5 - 1.0
package cost (cents/pin)	1.4 - 4	1-2	0.6-1.3
package size (mm)	23-45	29-50	35-50
lead pitch- peripheral (mm)	0.3- 1	0.3-0.65	0.3-0.5
lead pitch - array (mm)	1.0 - 1.5	1.0	0.5- 0.65
power (W)	2-18	2-28	2-55
Performance (MHz)	100-200	200-400	400-1000

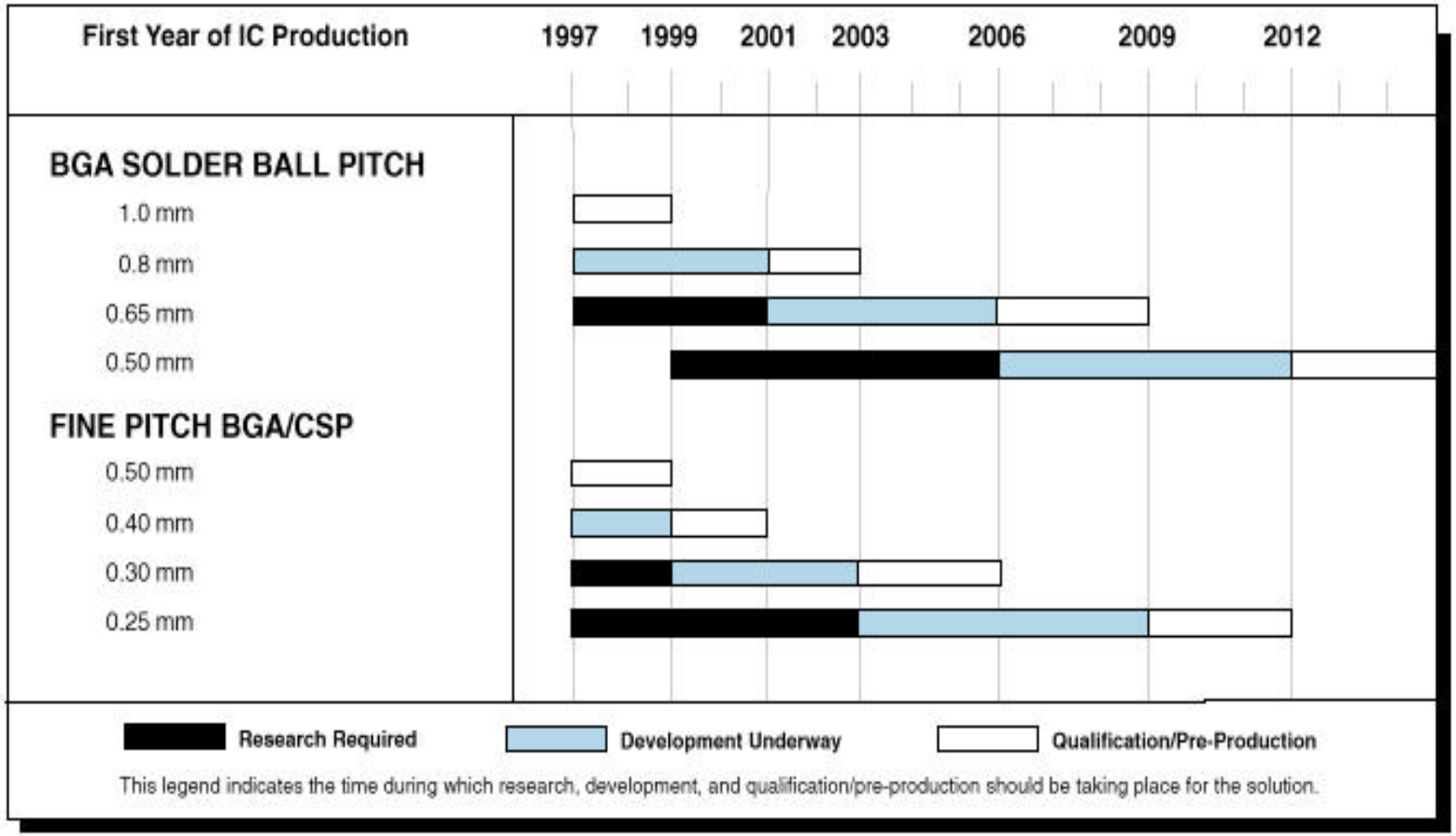
TRENDS OBSERVED

- Packages are getting thinner
- Number of leads is getting larger
- Package footprint decreasing to approach chip size
- Direct Chip attach techniques are emerging
- Package pin pitch is decreasing
- Package pins are being distributed in array format

HOWEVER, SUPPORTING SUBSTRATES ARE BECOMING MORE AND MORE LIMITING

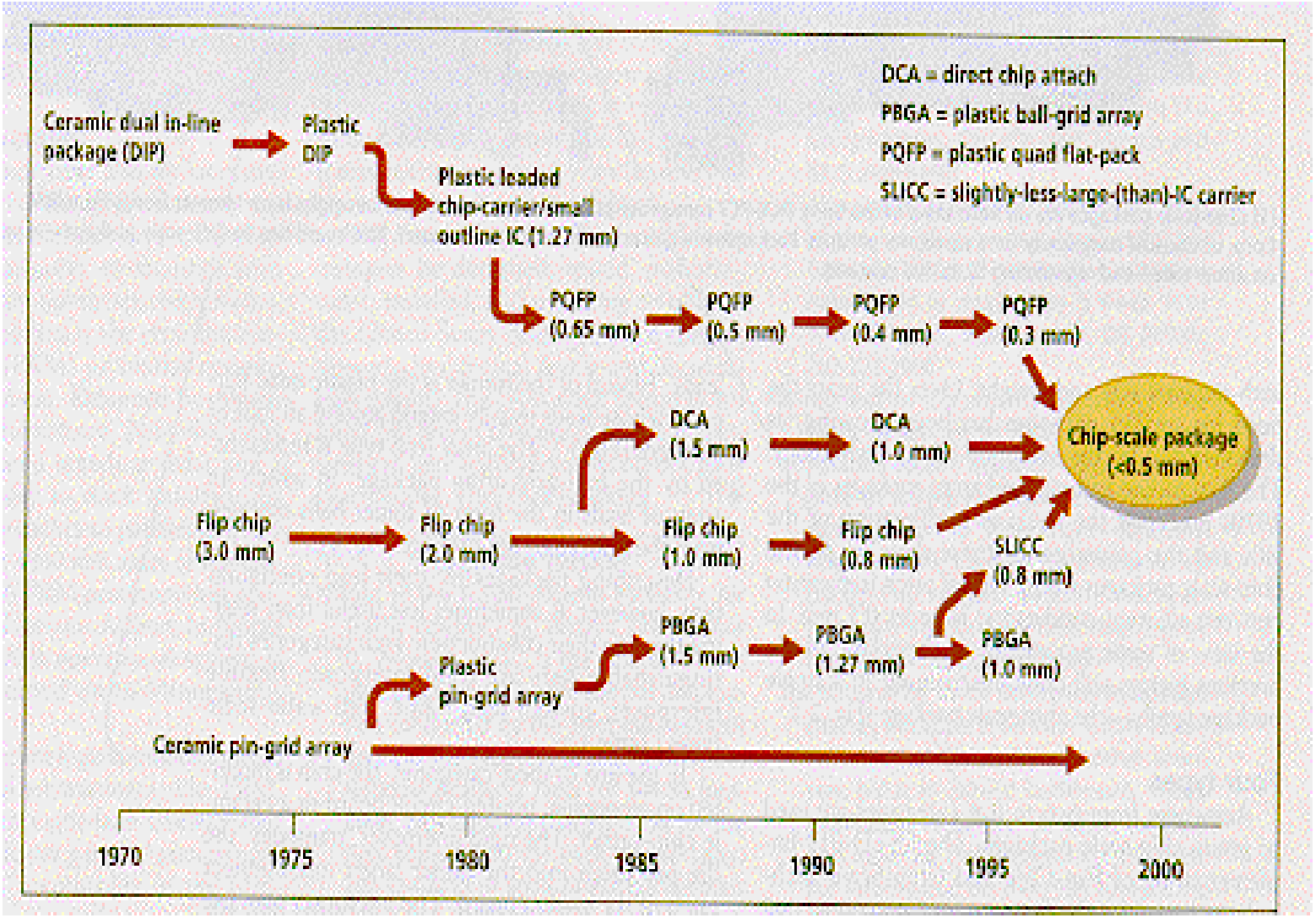
SYSTEM DESIGNERS ARE SEEKING SOLUTIONS IN MULTI-CHIP AND 3D PACKAGING TECHNIQUES ALONG WITH SYSTEM-IN-A-CHIP APPROACHES

FINE PITCH BGA AND CHIP SCALE PACKAGE POTENTIAL SOLUTIONS



SIA Roadmap 98”

EVOLUTION OF CHIP PACKAGES

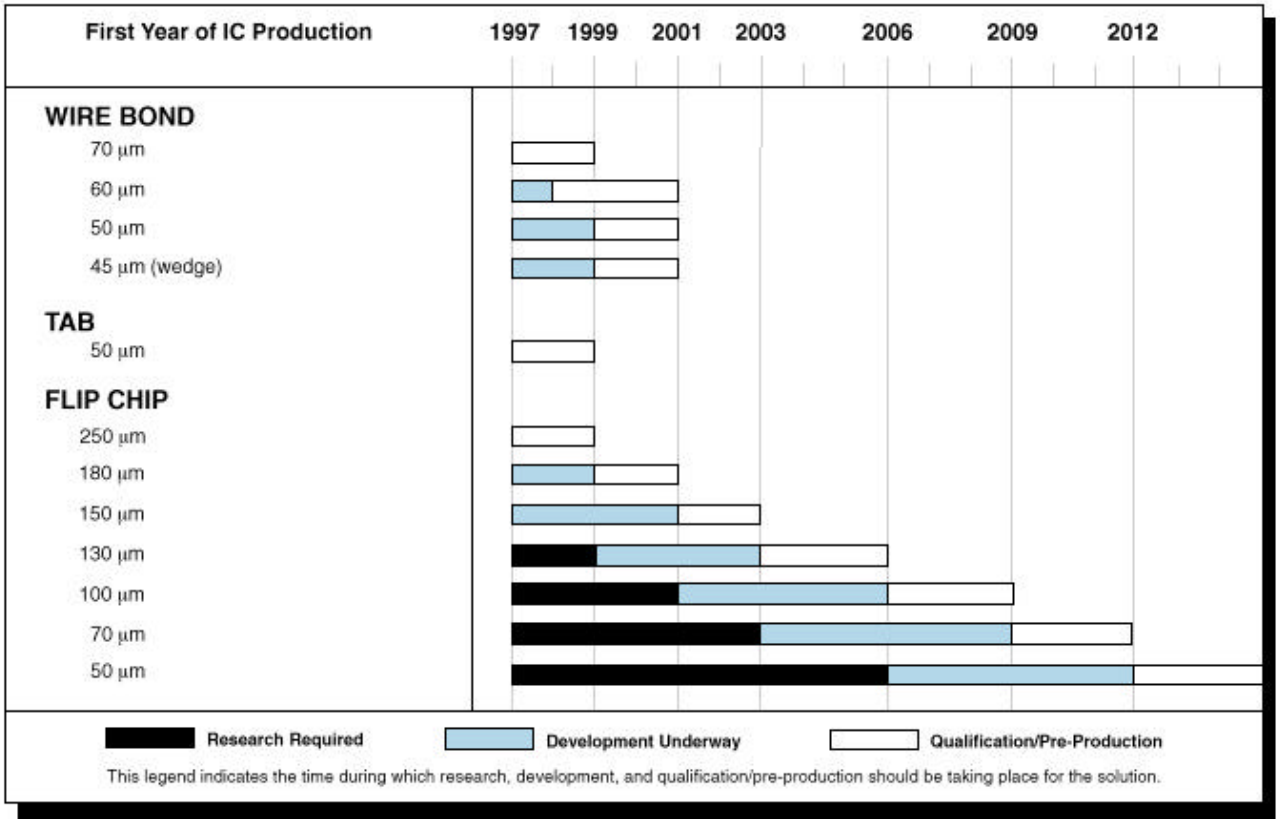


(P. Thompson, Motorola; IEEE Spectrum August 1977)

CHIP TO NEXT LEVEL INTERCONNECT NEEDS AND SOLUTIONS

Year of First Product Shipment *Technology Generation*	*1997* *250 nm*	*1999* *180 nm*	*2001* *150 nm*	*2003* *130 nm*	*2006* *100 nm*	*2009* *70 nm*	*2012* *50 nm*
Chip Interconnect Pitch (μm)							
Wire bond—ball	70	50	50	50	50	50	50
Wire bond—wedge	60	45	45	45	45	45	45
TAB*	50	50	50	50	50	50	50
Flip chip (area array)	250	180	150	130	100	70	50

** TAB—tape automated bonding*

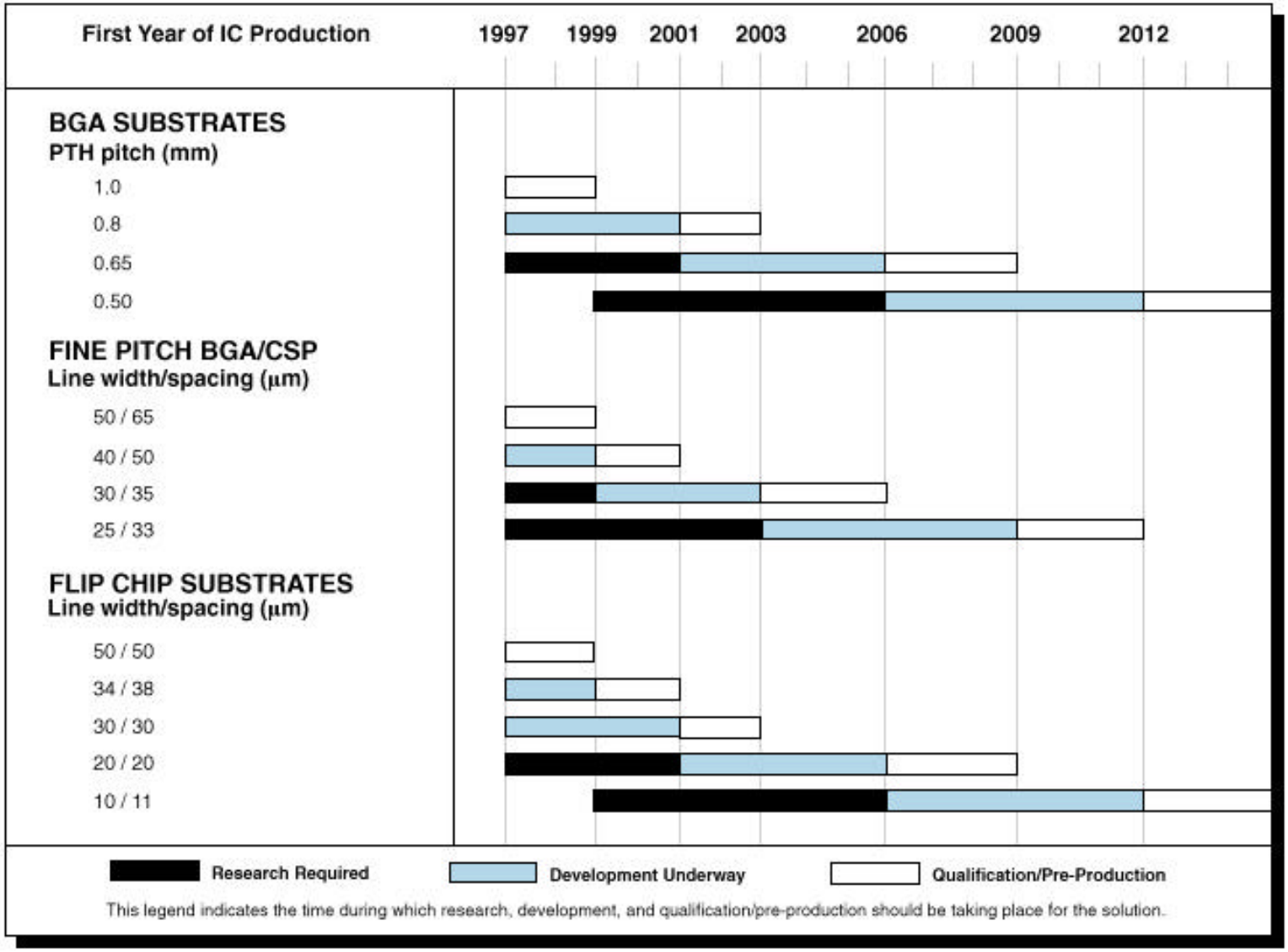


SIA Roadmap 98”

DIFFERENT DIRECT CHIP ATTACH TECHNIQUES

	Surface Mount	Chip on Flex	Flip-chip on Flex
Footprint	Large	Medium	Small
IC pad pitch (µm)	150	150	100
Cost factor	1.0	1.1	0.8-2.8
Pretesting of chips	Yes	No	No
Added wafer process	No	No	Yes
Thermal Resistance	60 C/W	45 C/W	75 C/W
Inductance (nH)	1.0- 3.0	1.0 - 2.0	0.1 - 0.2
Capacitance (pF)	0.2	0.2	0.03
Advantages	• readily available • high reliability • easy rework • established infrastructure	• small footprint • good electrical performance • compatible with most ICs • excellent thermal resistance	• good electrical performance • lowest cost in high volume • no post cleaning for flux
Disadvantages	• low electrical performance • high processing temperatures • requires flux cleaning • largest outline	• lower yields • no pretesting • no rework after glob-top	• poor thermal performance on flex • wafer bumping required • no pretesting

HIGH DENSITY SUBTRATE POTENTIAL SOLUTIONS



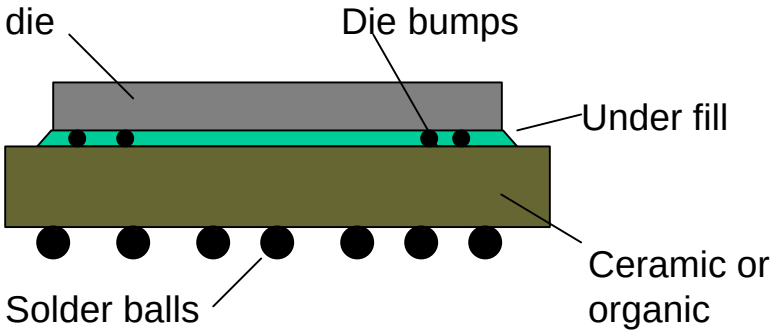
FOOTPRINTS OF CHIP SCALE AND CONVENTIONAL PACKAGES

Lead count	Conventional TSOP	Fine Pitch QFP	CSP
28	152	56	11
32	168	63	19
52	169	81	31
64	169	99	36

Areas in mm2,

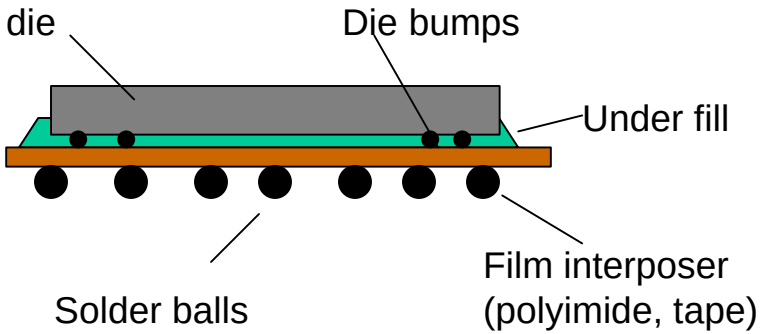
Adapted from P. Thompson (IEEE Spectrum August 1997)

TYPES OF CHIP SCALE PACKAGES



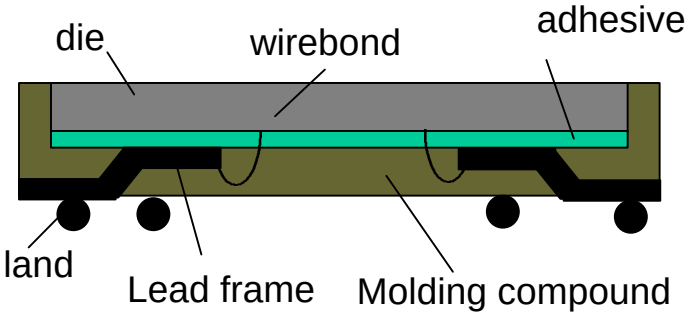
RIGID-INTERPOSER TYPE

NUCSP, Ceramic fine pitch BGA, mIni BGA SFFP, Stud bump bond, SLIC, Flip-chip BGA Chip size thin package



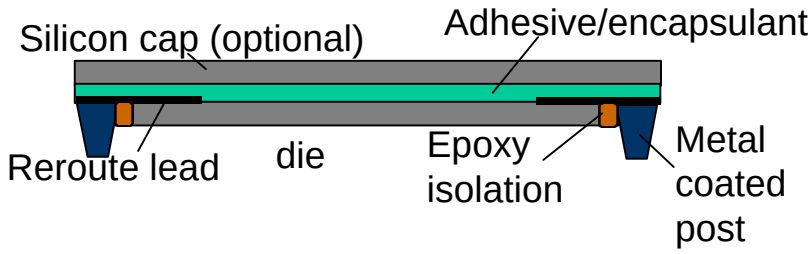
FLEXIBLE-INTERPOSER TYPE

Chip-on-flex, Flip-chip BGA, JACS-PAK, Fine pitch BGA, Resin Molded CSP, FBGA, µBGA, µstar BGA



CUSTOM LEAD FRAME

Small Outline Nolead, Lead on Chip, µstud BGA, Bottom Lead Package, Molded bump, Very Small Peripheral Array, Flip-Tape Carrier



WAFER LEVEL (MICRO SURFACE MOUNT)

Micro Surface Mount, SlimCase, Mini BGA

PACKAGES ARE GETTING THINNER

1.2 mm TSOP

0.5 mm Dual In Line Tape Carrier

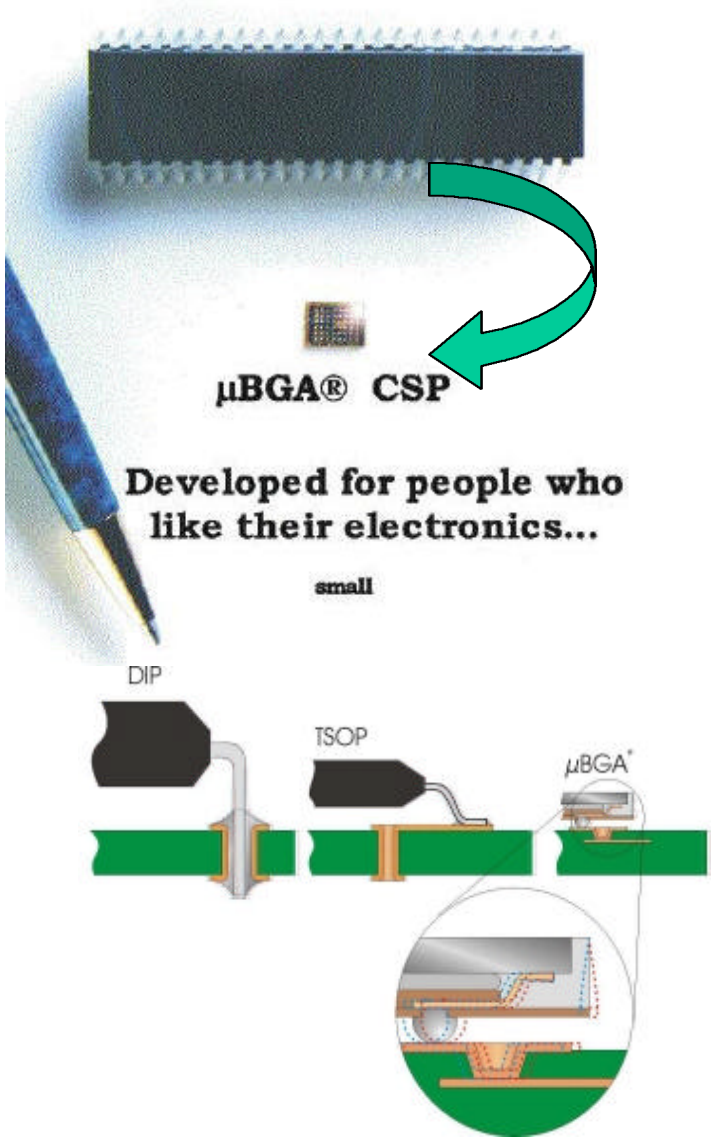
0.4 mm Ultra Thin Chip Package

0.3 mm Slim Case (from ShellCase)

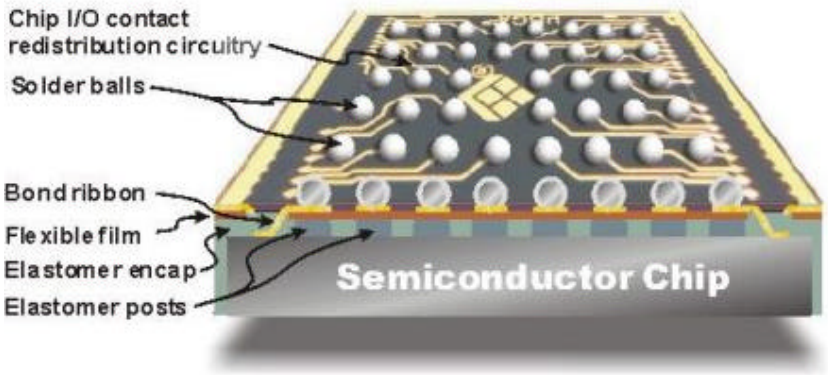
- **Thin packages can be made only 100 microns larger than the die in length, width and height**
- **Note that the incoming wafer thickness is 0.6 - 0.7 mm**
- **The die in thinner packages is in the range of 100 microns (0.1 mm) thin**
- **Advanced die thinning techniques required to support packaging development**

EXAMPLE OF CHIP SCALE PACKAGES

Micro Ball Grid Array (μBGA) from Tessera Inc.

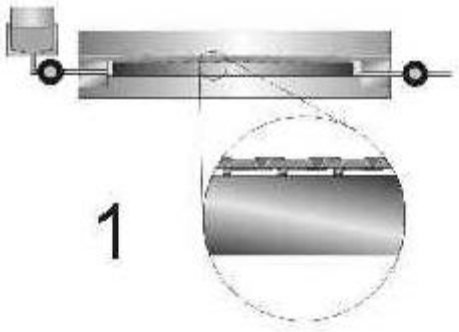


- **Direct path from the IC to the PCB provided by a flexible interposer**
- **Fast electrical interface (e.g. Rambus 0. 8 - 1.6 GHz leads)**
- **Compatible with "chip shooter"s**
- **0.5 - 1.0 mm pitch BGA**

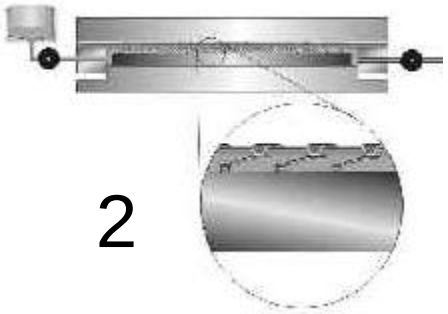


EXAMPLE OF CHIP SCALE PACKAGES

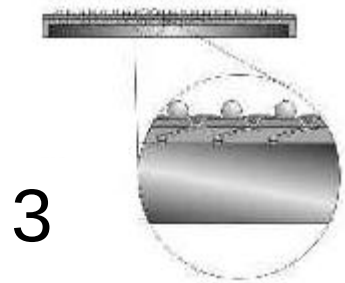
WAVE ™ (Wide Area Vertical Expansion) wafer level packaging technology from Tessera Inc



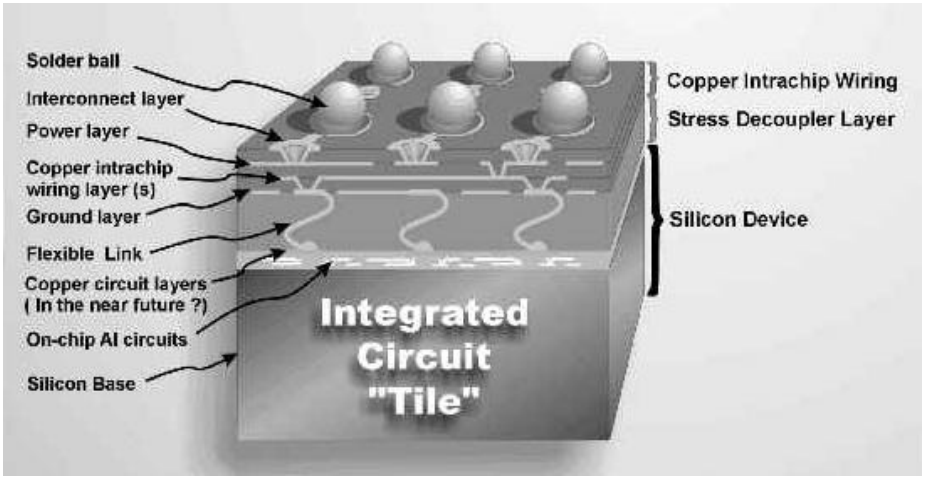
Align interposer and wafer



Expand the leads vertically while injecting low modulus encapsulant

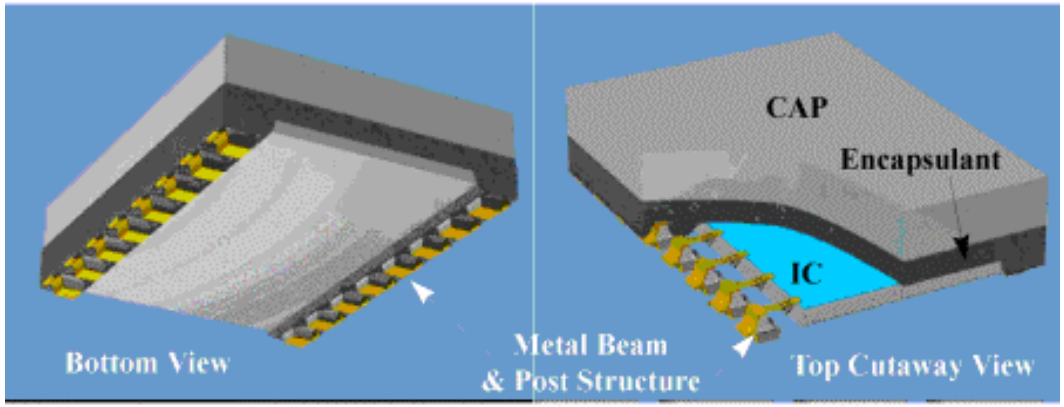


Attach solder balls and dice into single chips



Source: J. Fjelstad, Tessera Inc.

EXAMPLE OF CHIP SCALE PACKAGES



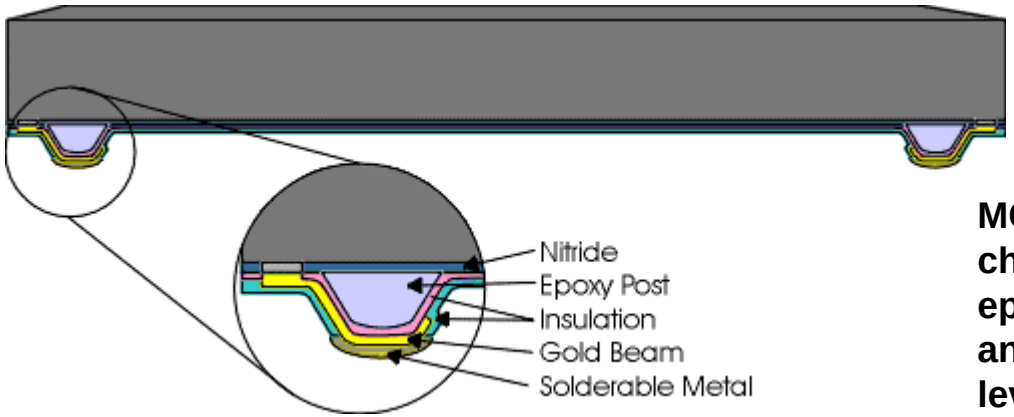
Parameter	*MSMT*	*0.3 QFP*	*Flip Chip*
Height (mm)	.5-.8	1.4	.5-.7
Inductance (nH)	0.1 to 0.2	1-7	0.1 to 0.2
Capacitance (pF)	0.02 to 0.03	0.5 to 1	0.3
Attachment	Solder	Solder	Solder and Underfill

Micro Surface Mount technology (MSMT) package from ChipScale Inc.
The package is formed in <u>wafer form</u>

MSMT yields active surface of the chip away from PCB

MGA technology produces packages with active face down to PCB

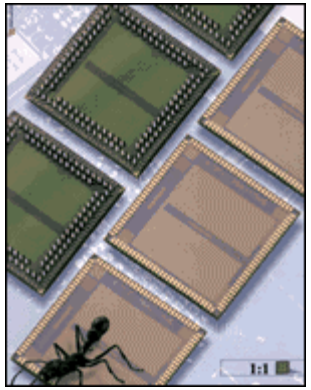
Micro Grid Array ™ (MGA)

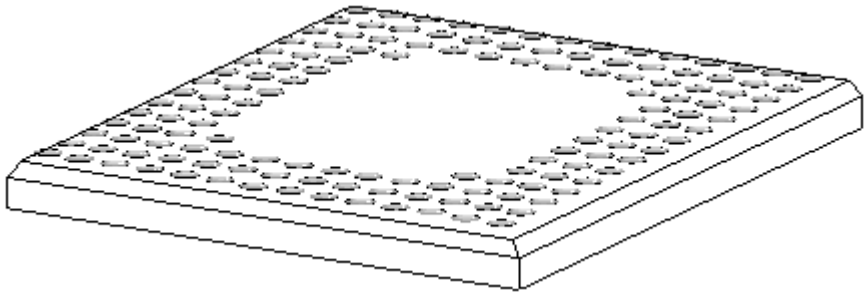


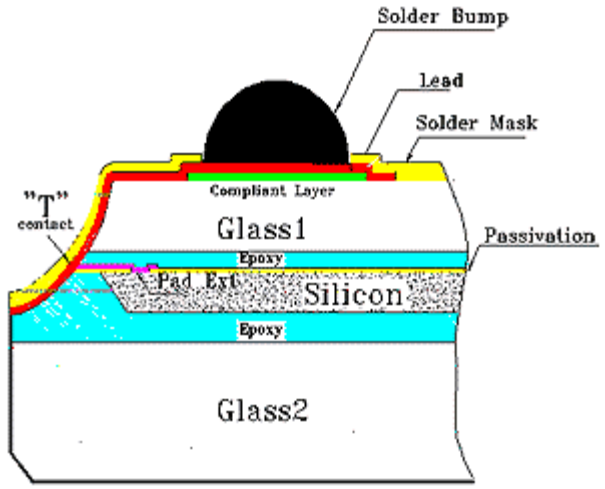
MGA provides a standoff from chip surface by using a compliant epoxy and can be placed anywhere on the chip using wafer level processing

EXAMPLE OF CHIP SCALE PACKAGES

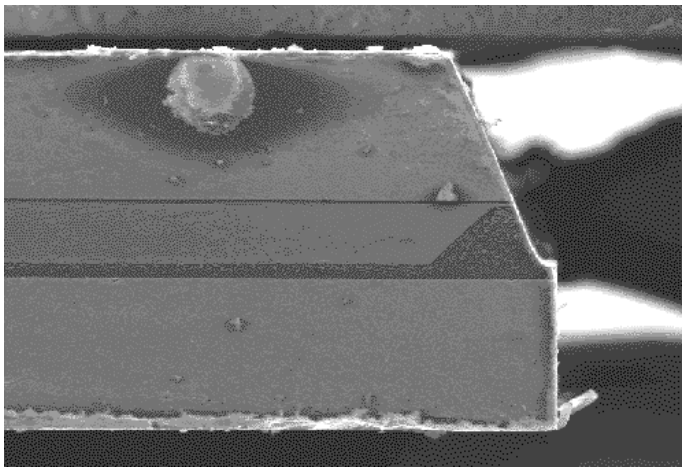
ShellCase BGA from ShellCase with pitches down to 500 microns





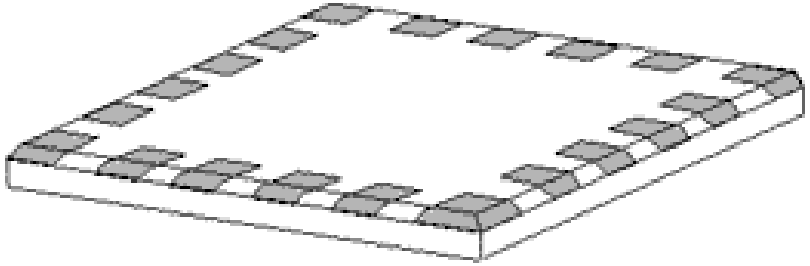


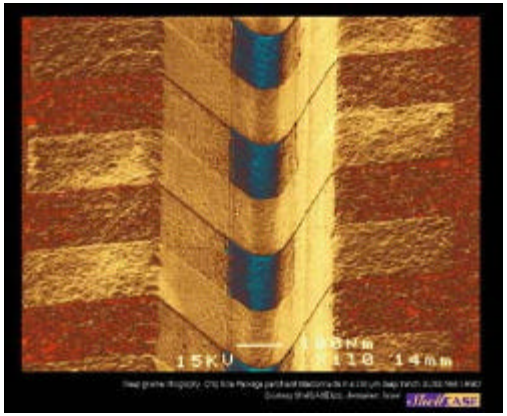
Compliant ShellCase CSP (crosssection)

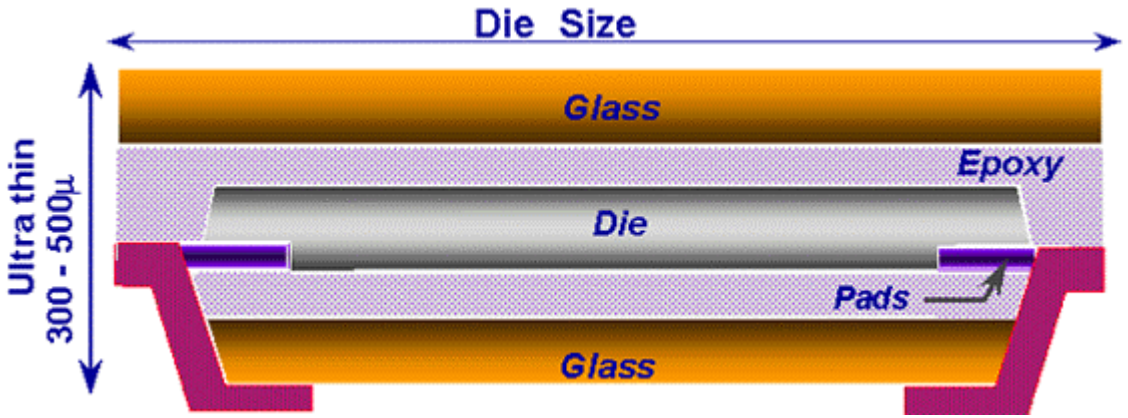


EXAMPLE OF CHIP SCALE PACKAGES

Ultrathin CSP from ShellCase







COMPARISON OF CONVENTIONAL AND WAFER LEVEL CHIP PACKAGING

Traditional IC Packaging	Wafer Level Packaging
Wafer is probed, diced and sorted	Wafer moved directly to packaging
ICs packaged away from fab	ICs packaged in fab
ICs are packaged one at a time	ICs are packaged en masse
Burn in performed in sockets	Burn in performed on wafer
Power and ground taken from PCB	Power and ground distributed in assembled structure
Device tested 2-3 times	Device tested once
High pin counts required	Lower external I/O possible
Higher power required	Reduced power requirements
All function in the chip	Function shared between package and chip
More complex substrate required	Simpler substrates possible (lower I/O)
Lead inductance concerns	Lead inductance nearly eliminated

Source: J. Fjelstad, Tessera Inc.

SUPPORTING TECHNOLOGIES FOR ADVANCED PACKAGING

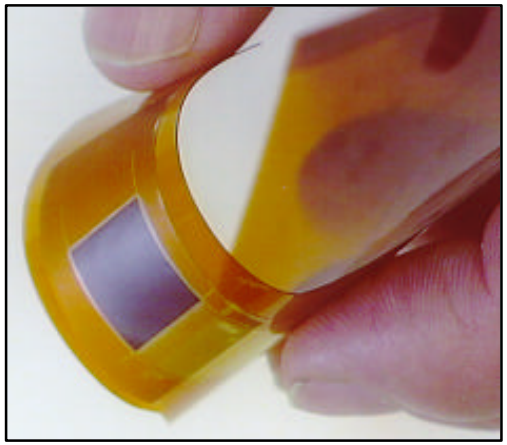
Advanced Packaging requires the utilization of the following techniques extensively :

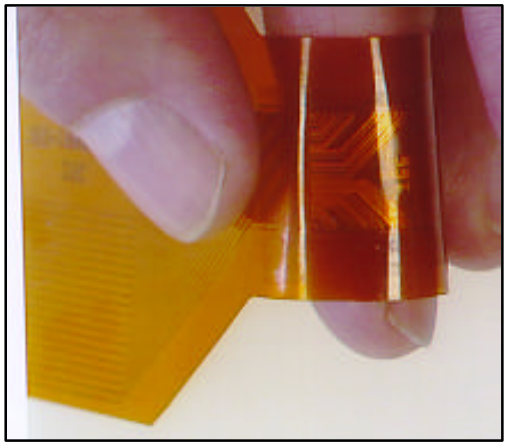
- **thinning of silicon wafers containing circuits**
- **bump bonding for high I/O density interface**
- **handling of KGD in die form**
- **handling of die of different sizes and origins, non-electronic chips (e.g. MEMS, Lasers, Detectors, Fluidic Devices)**

Therefore, advances in these techniques will help to increase the density and the functionality of advanced packages

ULTRA-THIN SILICON CIRCUITS

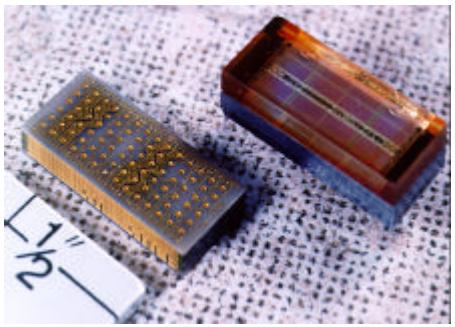
- A Kapton (50 micron thick) based flexible test vehicle has been used to test ultra-thin flash die
- 25 micron thin 16 Mb Flash die has been successfully tested after mounting on the test vehicle
- 25 Micron thin memory die mounted on the flexible substrate is bendable with the substrate. A bending radius of 1 mm can be obtained for each micron of silicon thickness



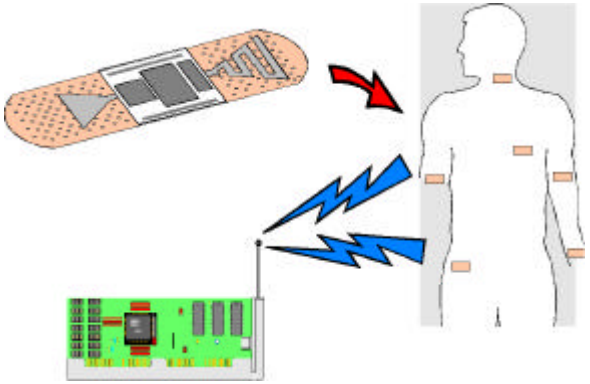


TECHNOLOGIES AND PRODUCTS BASED ON THIN SILICON CIRCUITS

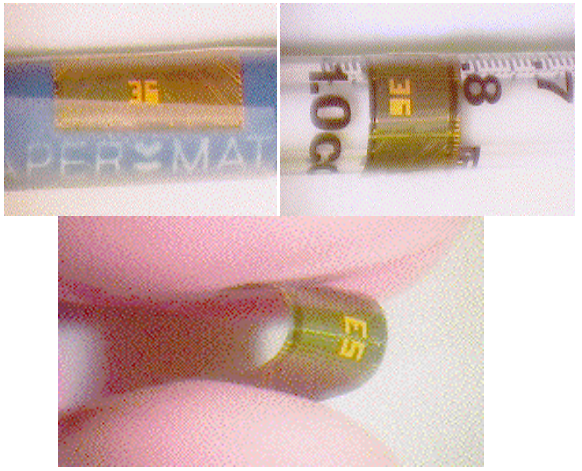
- **thin integrated circuit stacks with higher capacity (10 times more)**
- **flexible circuitry in conformal packaging**
  - **medical applications (shape conforming sensors)**
  - **space applications (SOI-like advantages)**
  - **wearable products**
  - **smart cards**



18 layers of 20 micron thin Si stack compared to ISC's standard short stack: within same height, the new thin stack can accommodate 10 times more layers



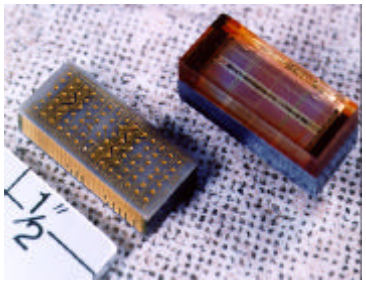
"Smart Band Aid" for body function monitoring

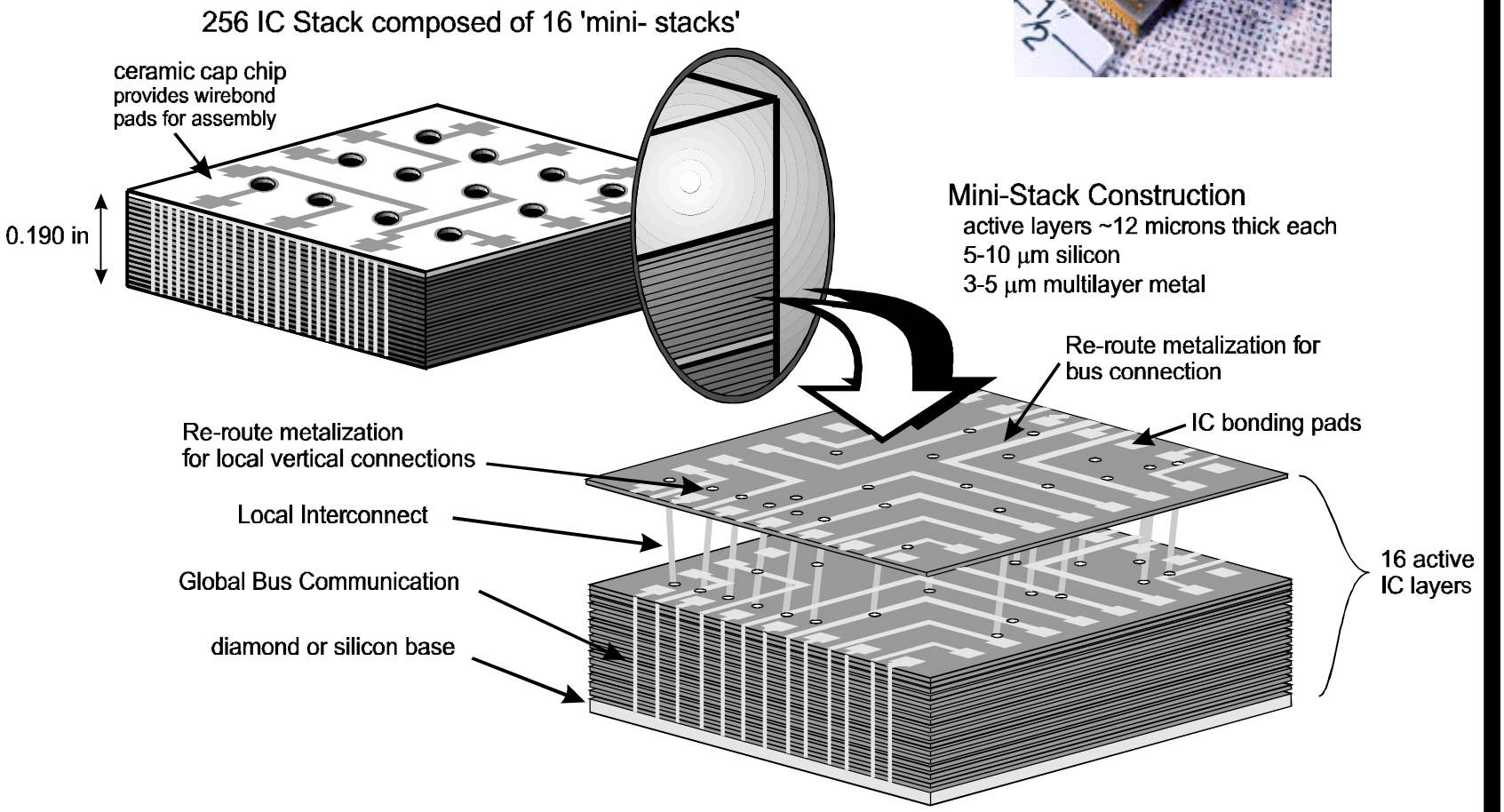


Bendable circuits for space microprobes, medical microprobes and smart projectiles

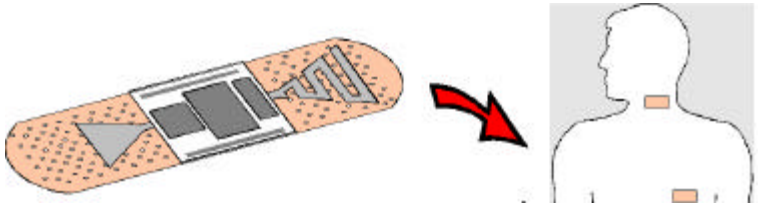
VERY HIGH DENSITY 3D STACKING BASED ON ULTRA THIN SILICON CIRCUITS

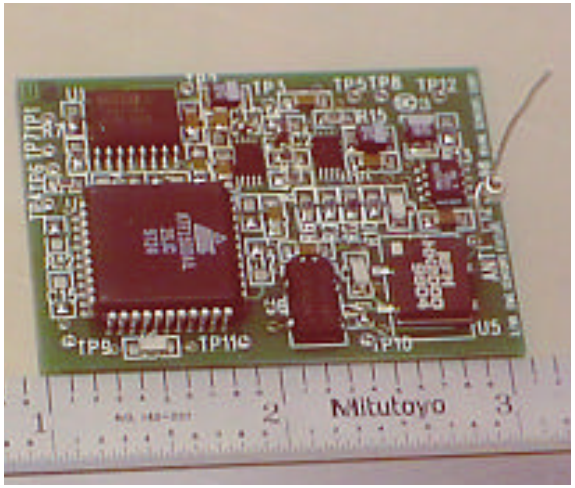
3D-VLSI?

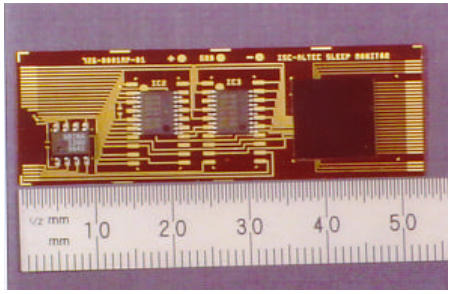




ULTRA THIN CIRCUITS - EVOLUTION OF A BIOMEDICAL SENSOR IMPLEMENTATION





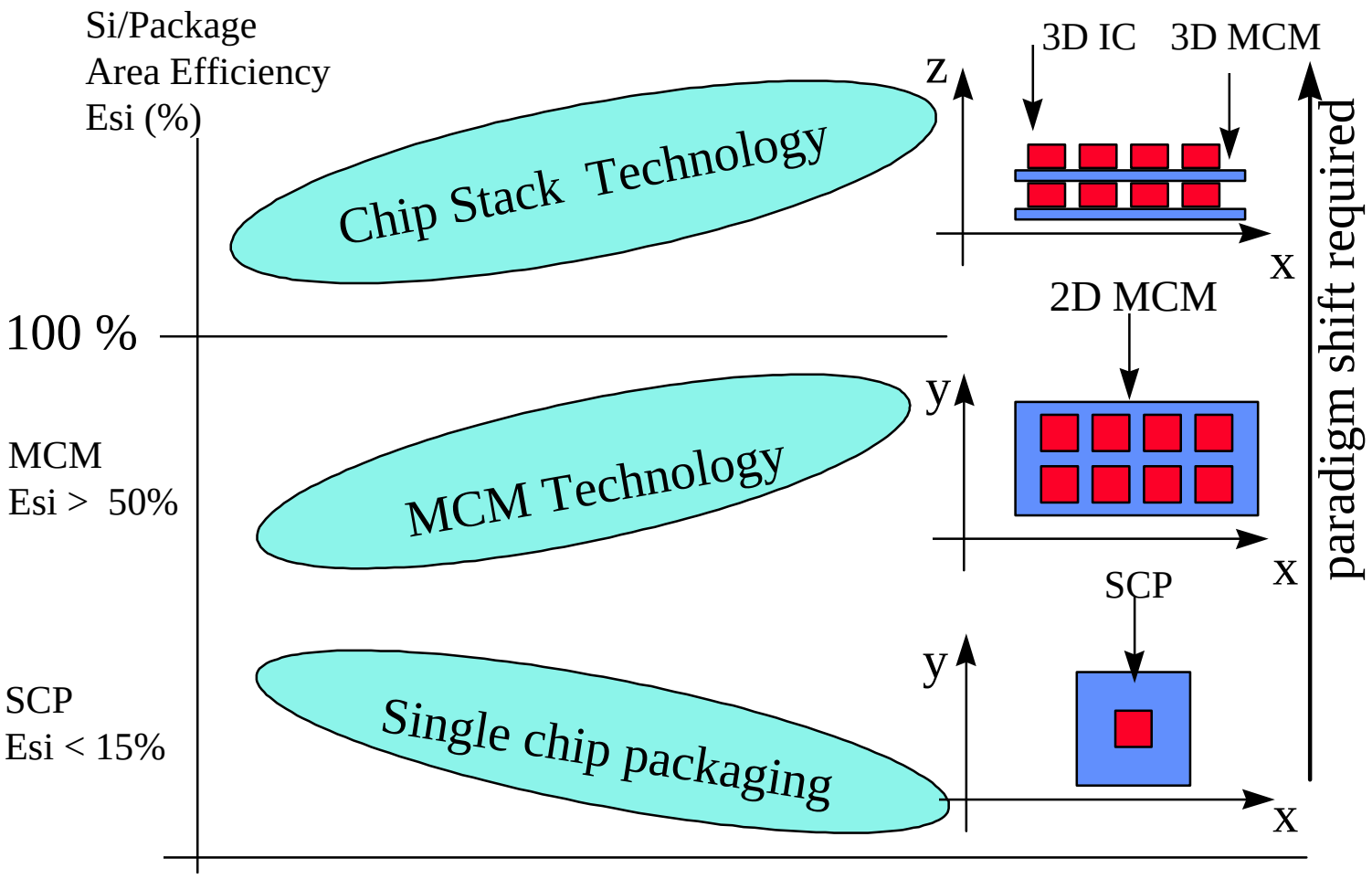


Prototype sensor input and RF transceiver circuit from off-the-shelf components

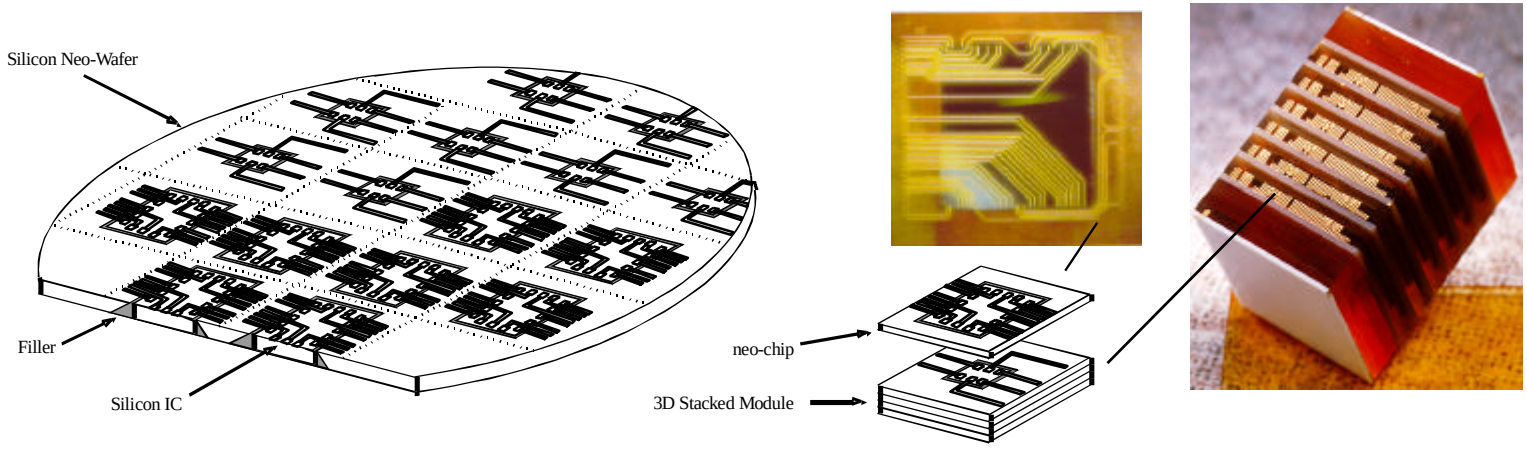
Custom ASIC replaces many ICs and a flex board replaces the rigid PC board

ISC's unique wafer thinning technology results in the silicon becoming flexible without damaging the circuit. Ultra-thin unpackaged ICs mounted on flexible boards

PARADIGM SHIFT IN PACKAGING



NEO-DIE NEO-WAFER AND NEO-STACK CONCEPT



A revolutionary chip-level layering and stacking concept to eliminate the same-size restriction and wafer level inventory requirements of existing processes

- **The process is designed to re-create a wafer from individual and heterogenous chips for batch processing by embedding them into an epoxy frame**
- **After lithography and metalization, the wafer will be diced into neo-die of identical sizes that contain each layer to be stacked**
- **Mature stacking technology and tools will be used to stack many layers and interconnect layers**

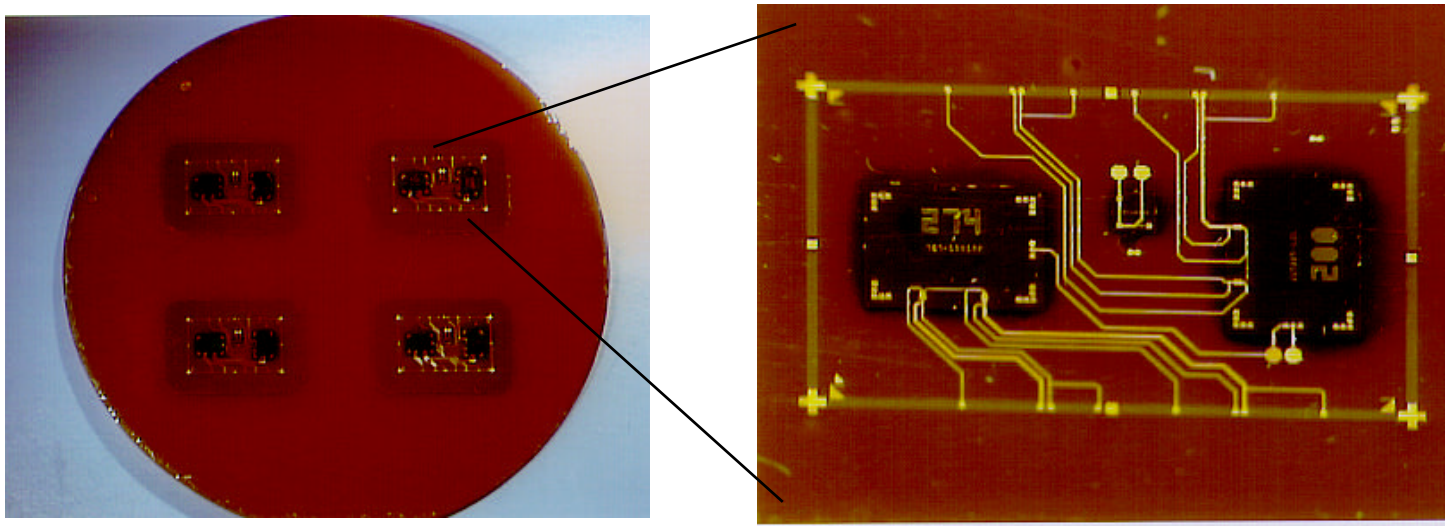
NEO STACKING APPROACH

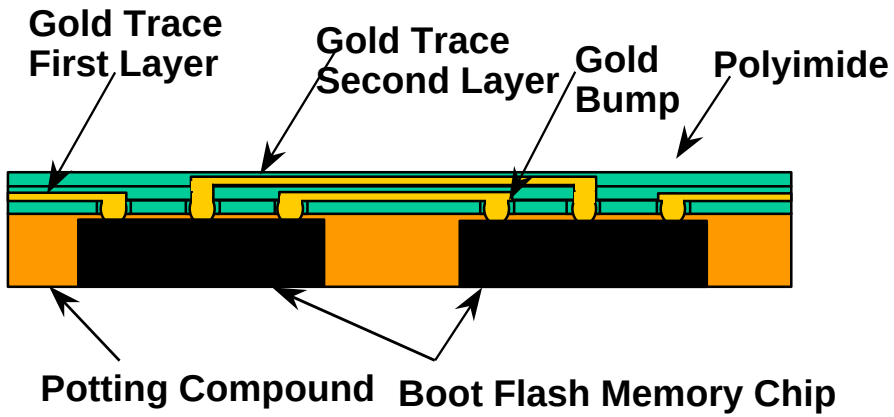
- **Starting with KGD, construct a new, or neo-wafer with many dice in a molding compound matrix**
- **Use a standard neo-die size, just slightly larger than the largest die in the stack**
- **Add blank silicon to open areas on layers where smaller die are used to enhance thermal conduction between layers if needed**
- **Perform metalization and thinning in neo-wafer form**
- **Dice into individual layers**
- **Laminate into a stack**

<u>Neo-stacking is a breakthrough in high density packaging technology</u>

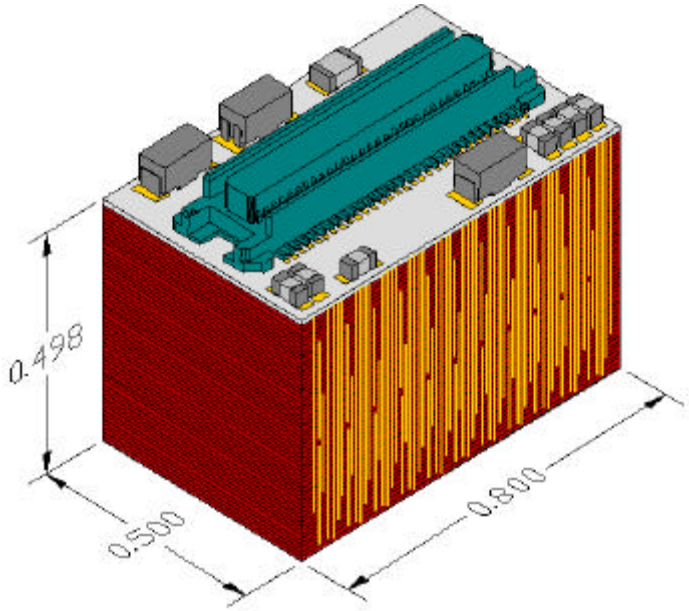
- **It allows complete systems in a cube**
- **It allows the combination of massive electronic functions with extreme miniaturization and integral logic and control functions**
- **dense layer-to-layer interconnects through the epoxy molding layer**
- **The process is highly manufacturable through industry standard automated tooling and batch processing**

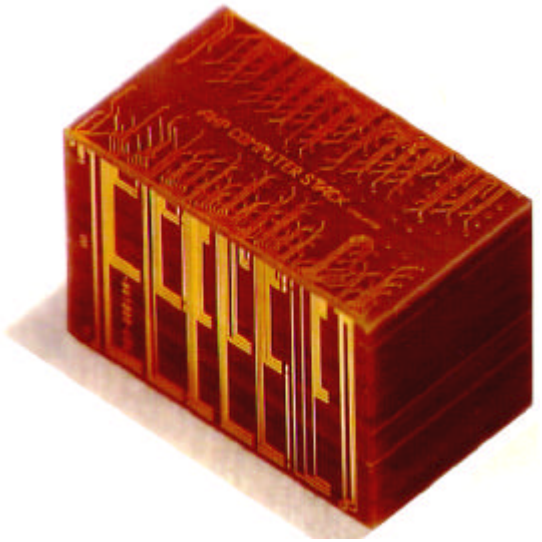
NEO STACKING FABRICATION EXAMPLES





NEO STACK FABRICATION EXAMPLE

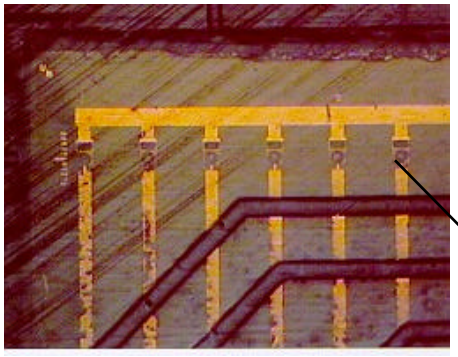




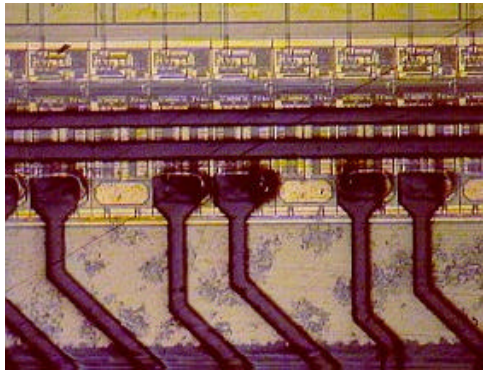
Number of Layers	Layer Type	Routing Layers	Total Chips	Chip Types
1	Cap Substrate	2-sided	-	-
4	Capacitor	1	1	1
32	Flash	1	1	1
1	Flash Driver	2	4	1
1	Microprocessor	1	1	1
1	FPGA	2	1	1
1	Bus Driver	2	4	2
1	Boot Flash	2	2	1
1	IEEE 1394 Interface	2	3	2
4	DRAM	1	1	1
1	Bottom Ceramic	-	-	-
48 Total Layers			**52 Total Chips**	**10 Chip Types**

NEO-STACKING TECHNOLOGY FOR IMPLEMENTING DIVERSE COMPONENTS IN ONE LAYER

Neo layers with lasers, detectors and electronic chips were built using vertical cavity surface emitting lasers and MSM detectors from Honeywell

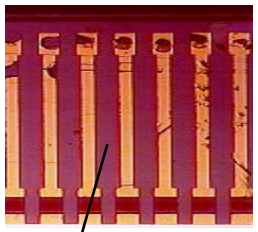


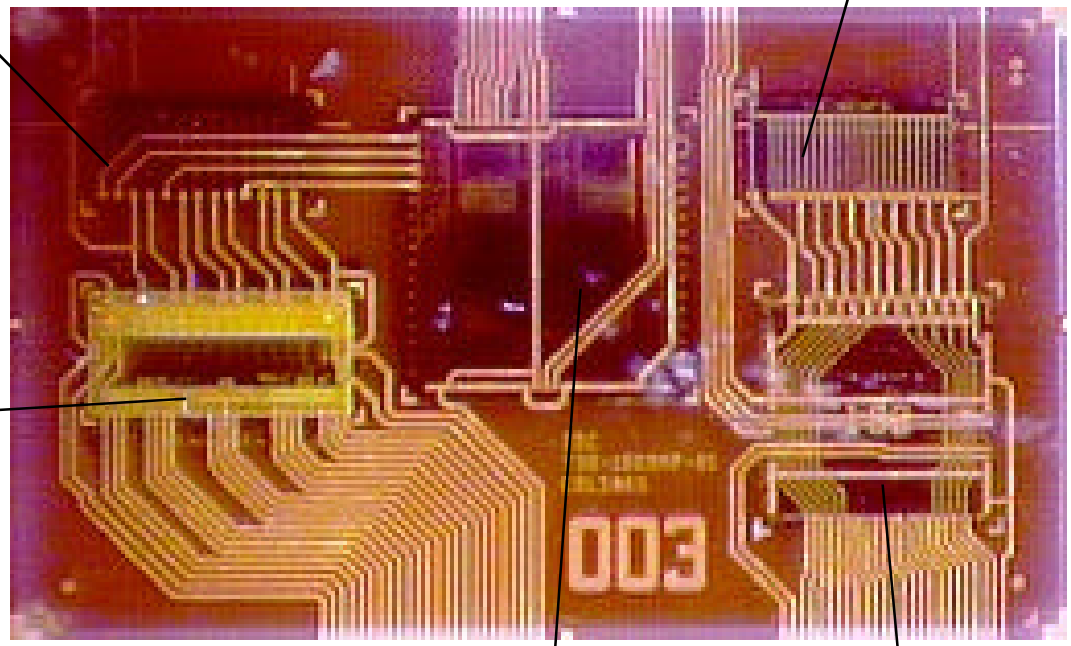
Laser array



Driver array

Detector array



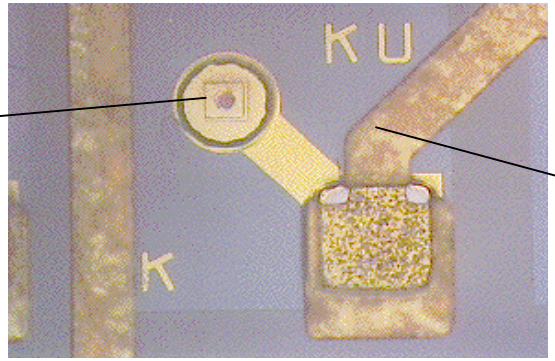


CLDA2 chip

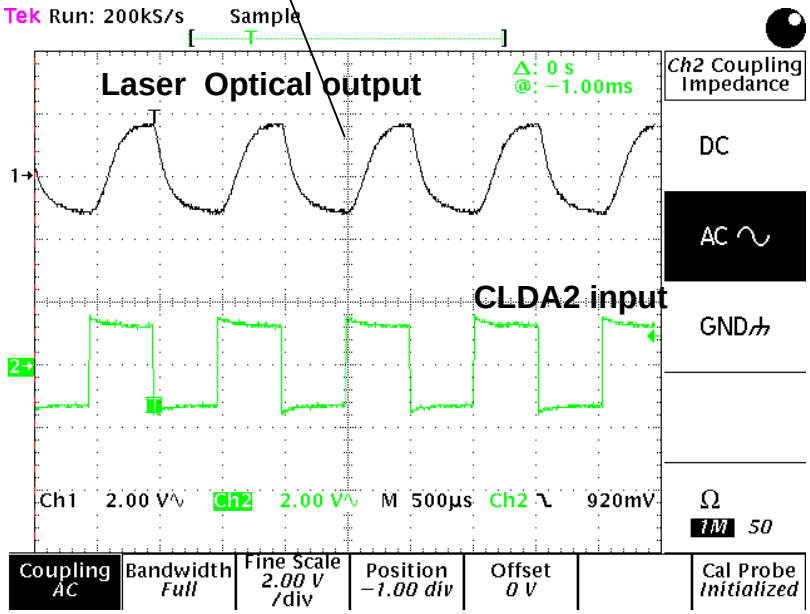
Receiver array

OPTOELECTRONIC NEO-LAYERS

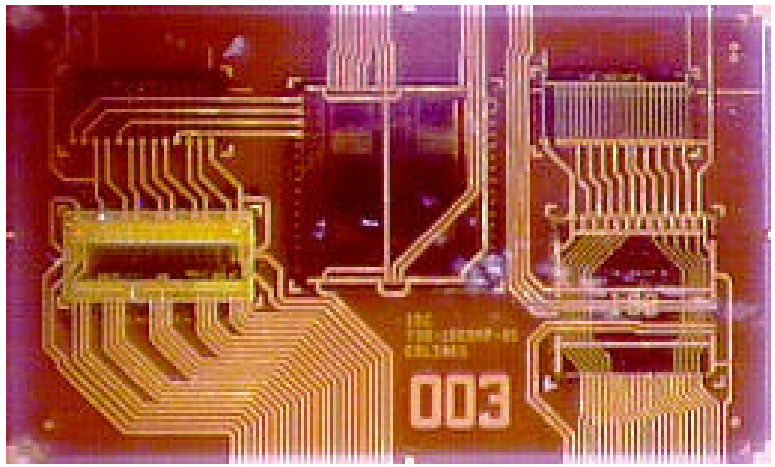
The characterization of the optical links is ongoing



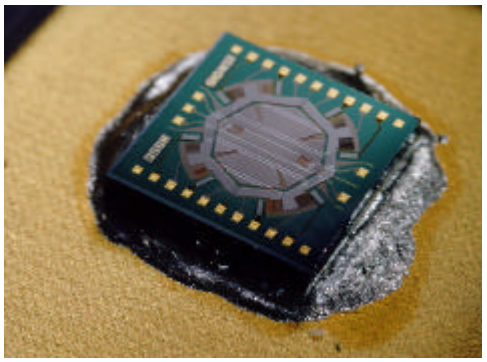
additional metalization



finished neo-chip

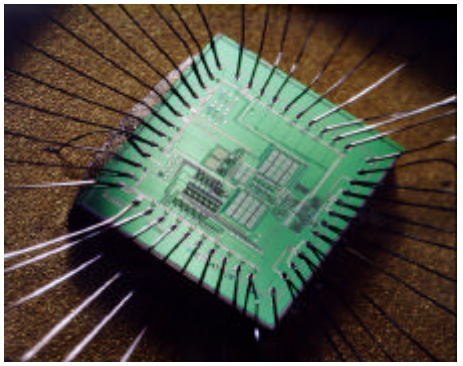


INTEGRATION OF DIFFERENT TECHNOLOGIES IN THE SAME STACK
Example: Multi-Axis Miniature Inertial navigation System

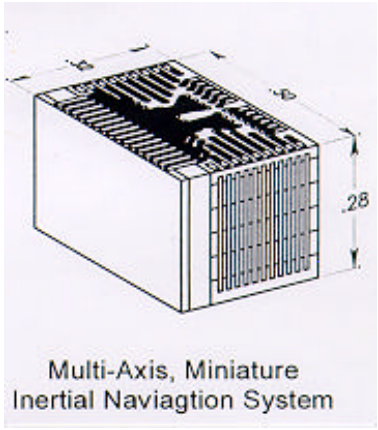


MEMS Based Micro-gyro

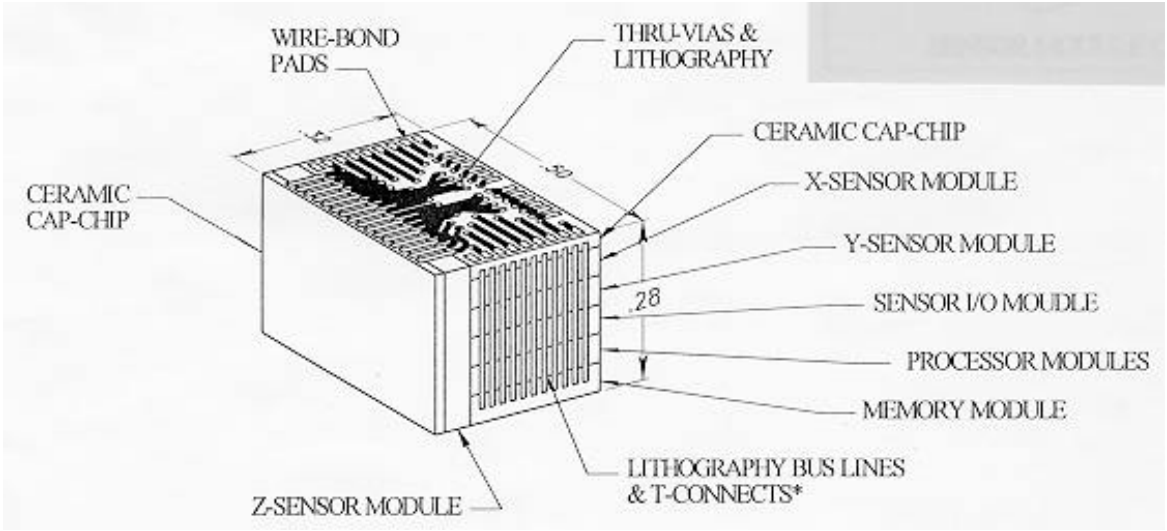
+



Read-out ASIC



Six-axis inertial measurement and navigation unit



HIGH SPEED OPERATION IN CHIP STACKS

- **ALCATEL-Espace demonstrated the basic operation of stacked microwave circuits in Ku-band (10.7 -12. 7 GHz) range**
- **Insertion losses were about -0.5 dB/mm**
- **Results indicate potential operation up to 30 GHz.**

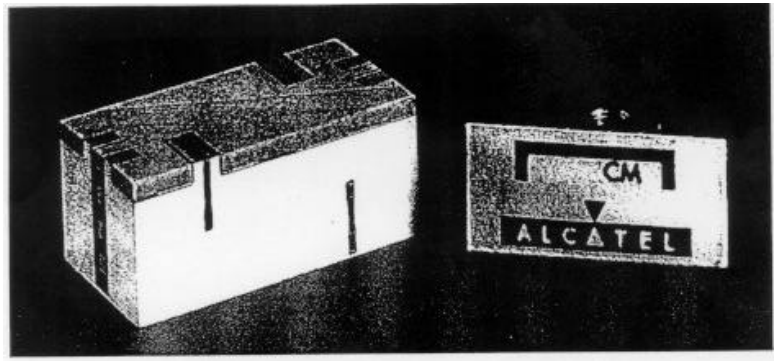
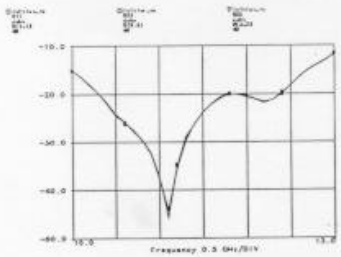
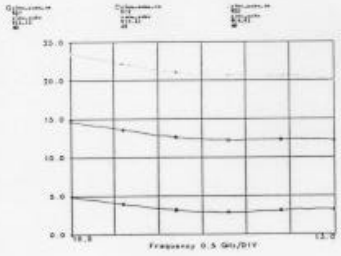


Figure 4 : 3D microwave module by ALCATEL ESPACE
(dimension : 20 mm * 10 mm * 9 mm).



Return loss



Gain according three source voltage commands on the attenuator

Figure 5 : Measurement of the 3D module.

From: 3D Microwave Modules for Space Applications , P.Monfraix et al

CHIP LEVEL 3D-PACKAGING ROADMAP

YEARS	1998	2000	2002	2004
In-plane line density (lines/cm)	500	1000	1500	2000
In-plane total number of metalization layers	2	3	4	5
Side-face line density (lines/cm)	200	400	800	1000
Side face total number of layers	1	2	2	3
Areal line density (new technology) (lines/cm^2)	900	1600	2500	5000
Maximum Operating Frequency -coplanar lines (GHz)	1	2	4	8
Maximum Operating Frequency –Microstrip lines (GHz)	10	20	30	50

ELECTRICAL CHARACTERISTICS OF TYPICAL PACKAGE INTERFACES

100 mm^2 chip	Bare die with 75 μm Wire bond	Flip-chip 0.5 mm bump	Quad Flat Pack with 75 μm wire bond	Micro Ball Grid array 1 mm bump
pitch (mm)	0.15	0.25	0.30	0.50
Footprint (mm^2)	125	125	785	150
Package/chip area	1.25	1.25	7.85	1.5
Height (mm)	0.4-0.6	0.5-0.7	1.4	0.84
Inductance (nH)	1-2	0.05-0.2	1-7	0.5-2.1
Capacitance (pF)	0.2	0.05- 0.1	0.5-1	0.05-0.2

COMPARISON OF ADVANCED PACKAGING APPROACHES

TECHNOLOGY	ADVANTAGES	DISADVANTAGES	APPLICATIONS
Flip-Chip	– Covers least area – Has excellent electrical performance	– Lacks die availability – Hard to assemble due to planarity – Die shrinks results in board redesign	– Low lead count used (watches, vehicle modules, displays – High reliability systems – Vertically integrated companies
Chip-Scale Package	– System size reduction with standard technology	– New technology lacks reliability and production infrastructure	– Memories – Portable computing and communications – Under 100 leads
Multi Chip	– Early system integration – Best electrical performance	– Needs KGD – Lacks die level availability – Difficult test	– Large systems (e.g. avionics) – Some automotive and communication systems

Adapted from P. Thompson, IEEE Spectrum 1997

EVOLUTION OF CHIP PACKAGING TRENDS

From	To	Impact
Al pads and metallurgy	Copper pads and metallurgy	bond wires bump materials passivation
Wire bond	flip-chip	low cost wafer bumping underfill materials
leaded packages	area array packages	low cost dense substrates encapsulants
single chip packages	direct chip attach Chip scale package	low cost wafer bumping low cost dense substrates low cost known good die
200 mm wafers	300 mm wafers very thin chips	chip thinning material handling equipment configuration