

**520/530/580.495
Microfabrication Laboratory**

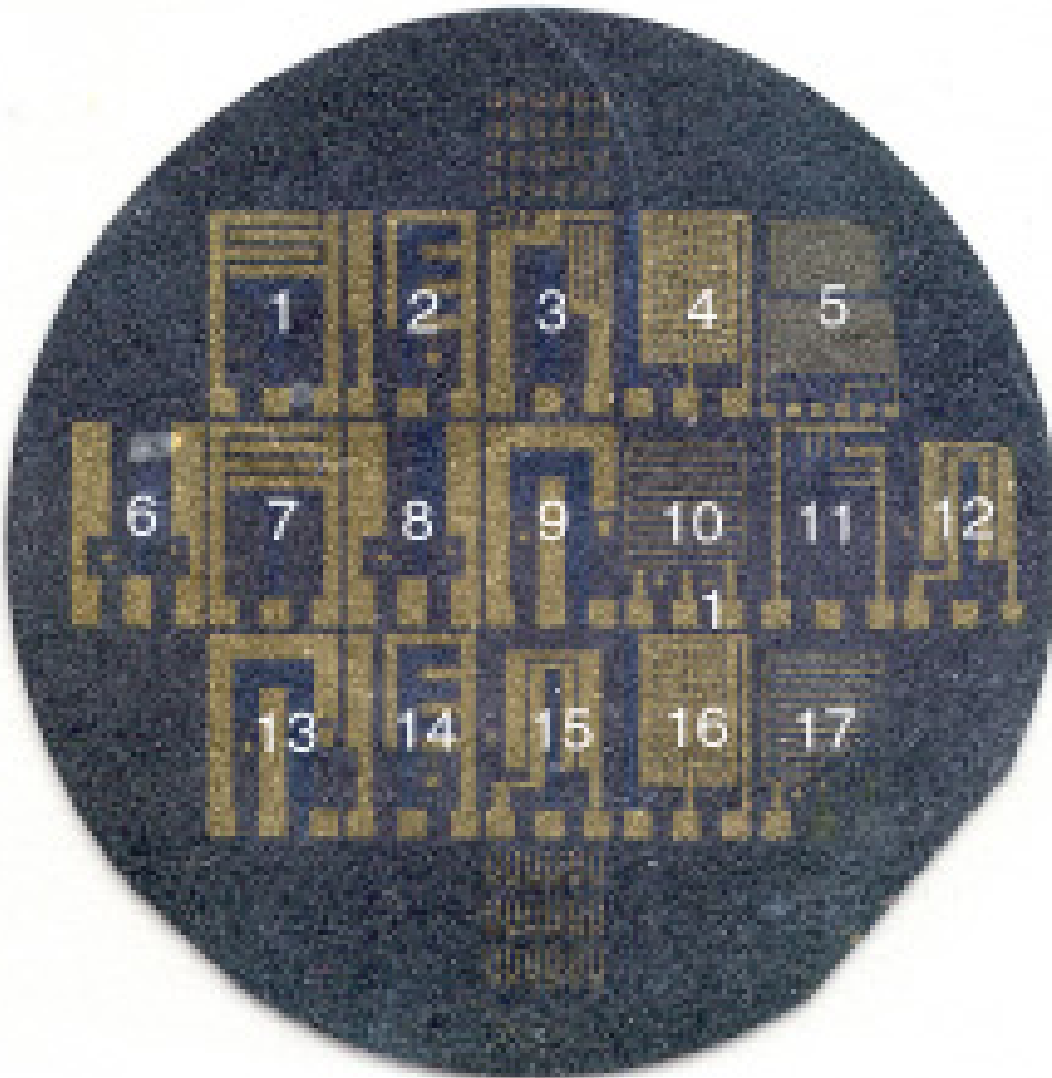
and

**520.773
Advanced Topics
In Fabrication and Microengineering**

Packaging

PACKAGING

- Wafer testing
- Die separation
- Die attachment
- Wire bonding



PACKAGING CHALLENGES

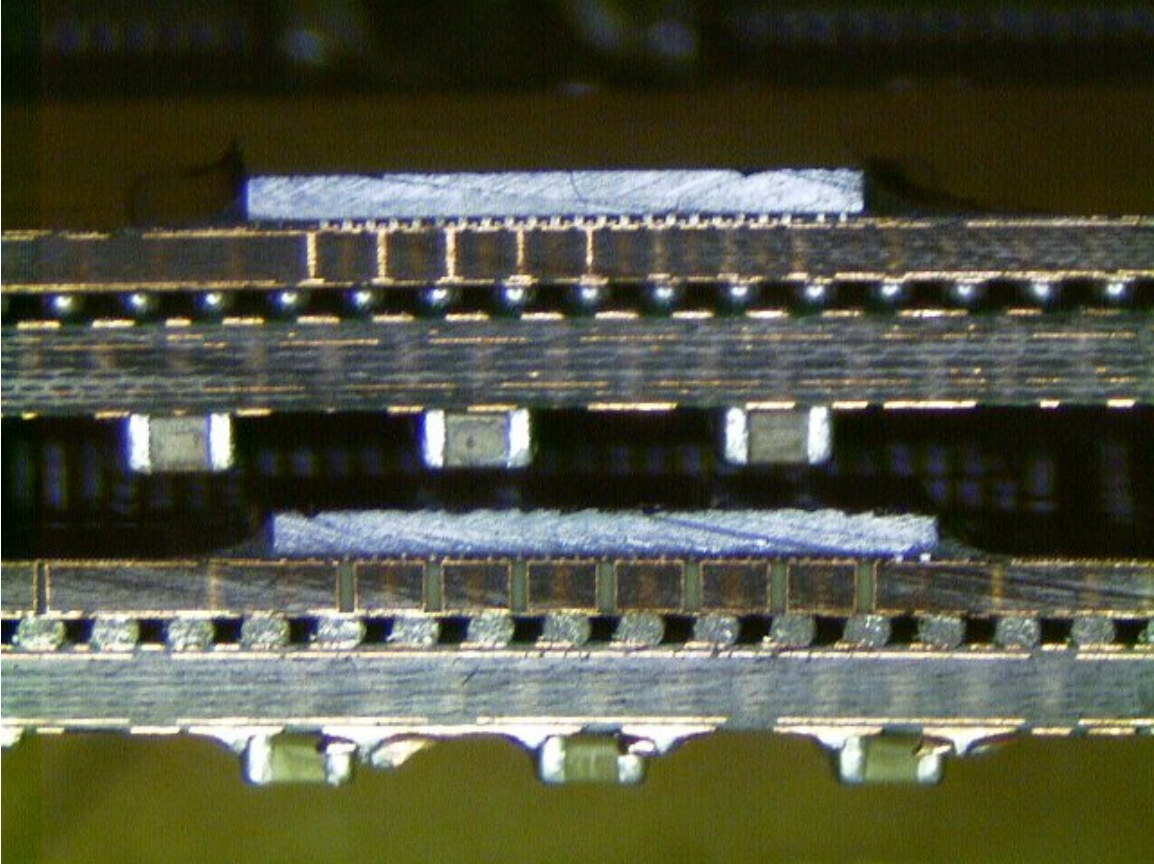
Microelectronics:

- Number of electrical connections
- Signal integrity (high speed and noise)
 1. parasitic capacitors
 2. parasitic inductors
- Thermal management
 1. heat extraction
 2. expansion coefficient matching
- Reliability
- Cost

MEMS:

- Mechanical ports
- Fluidic ports
- Optical access
- Vacuum environment

From Chip to Board

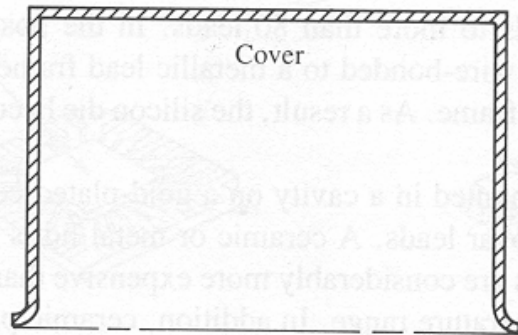


PIII Processor

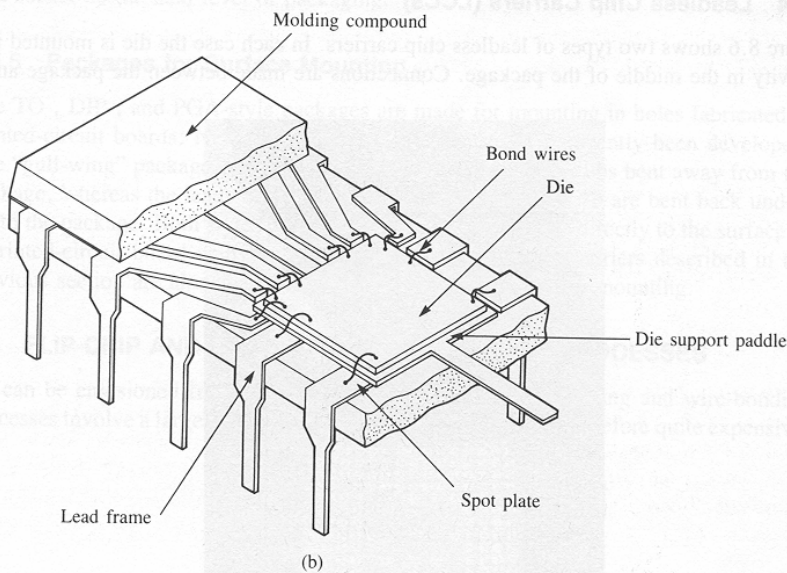
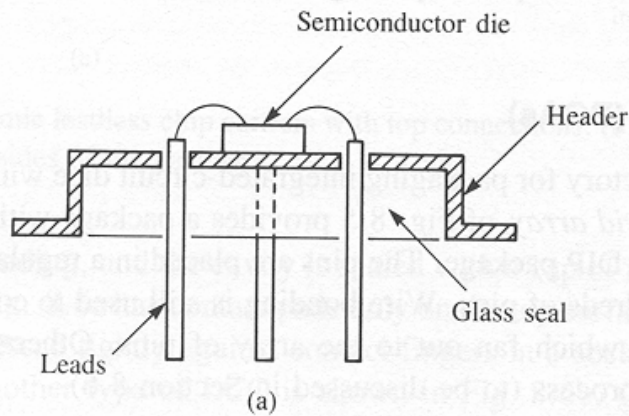
PACKAGES (I)

- “TO” style
 - DIP (Dual Inline Package)
 - PGA (Pin Grid Array)
 - LCC (Leadless Chip Carrier)
 - PCB (Printed Circuit Board)
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- Kovar leads (iron-nickel alloy); same thermal expansion coefficient as the glass feed-throughs.
 - Gold plated surfaces.
 - PCB is cheap (good for throw away electronics).

PACKAGES (II)

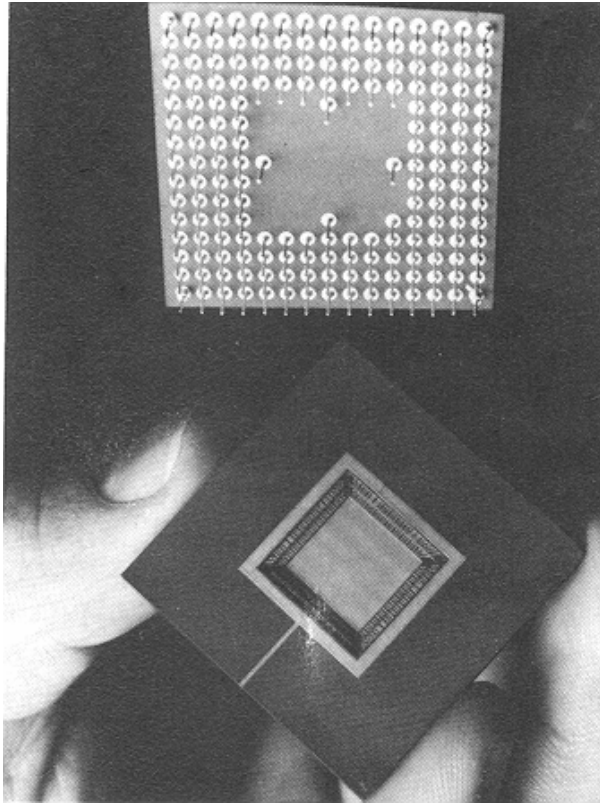


“TO” style

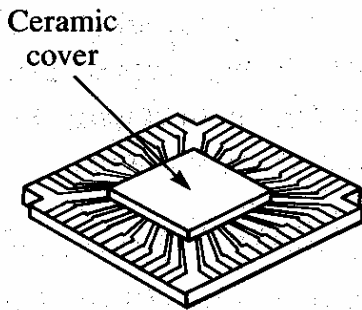


DIP

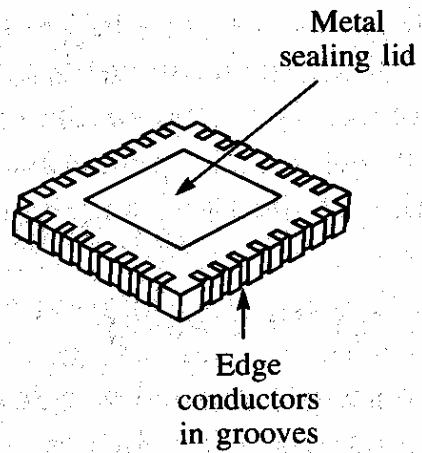
PACKAGES (III)



PGA



(a)

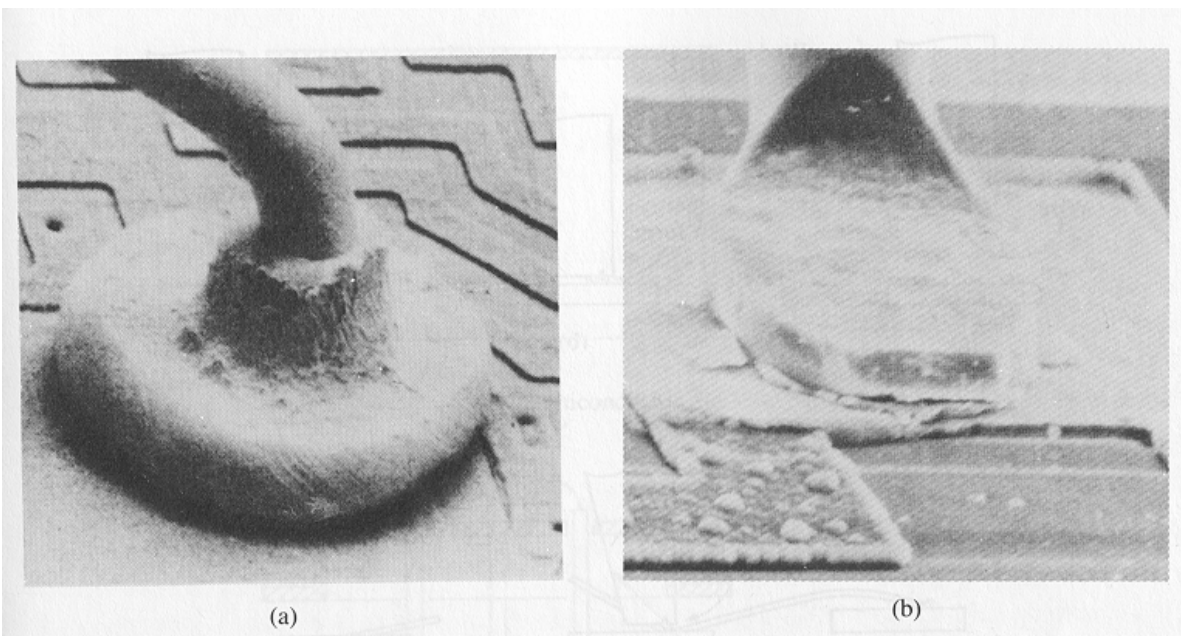
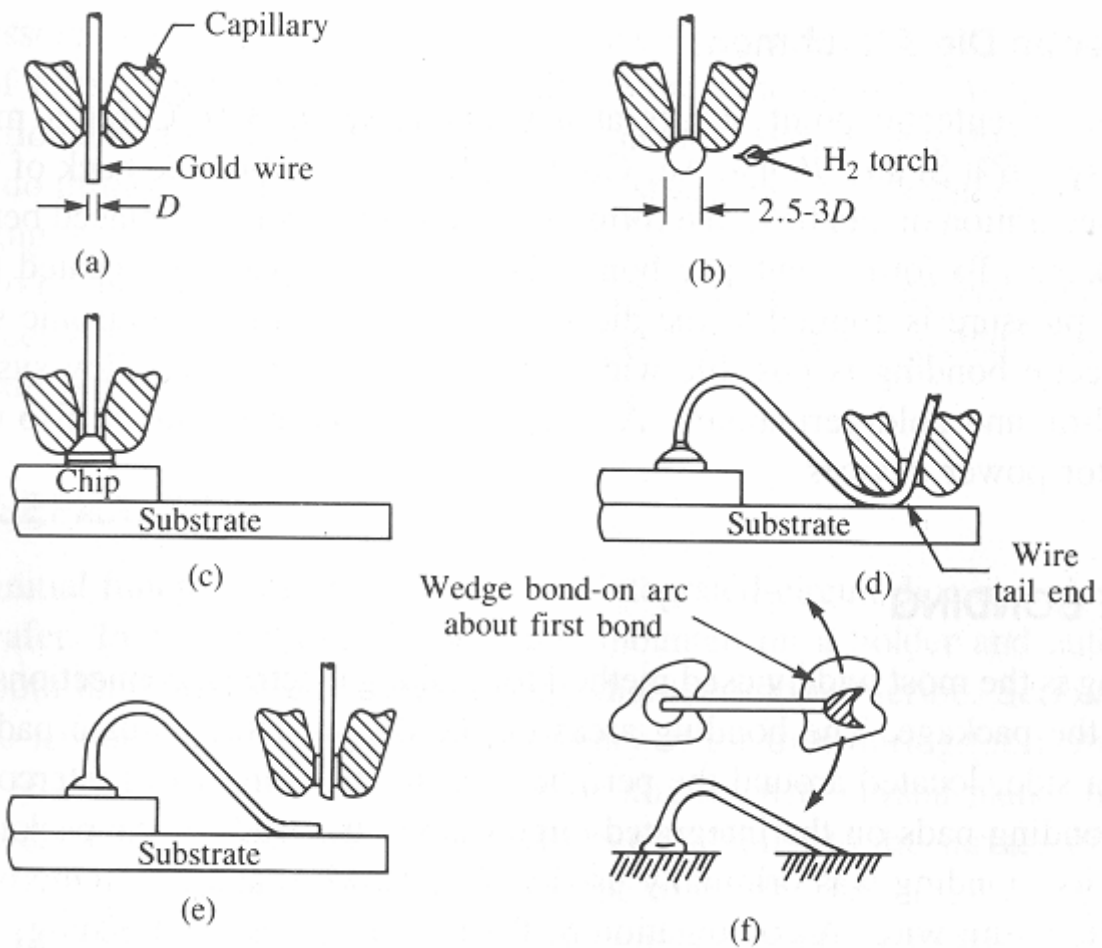


Edge conductors in grooves

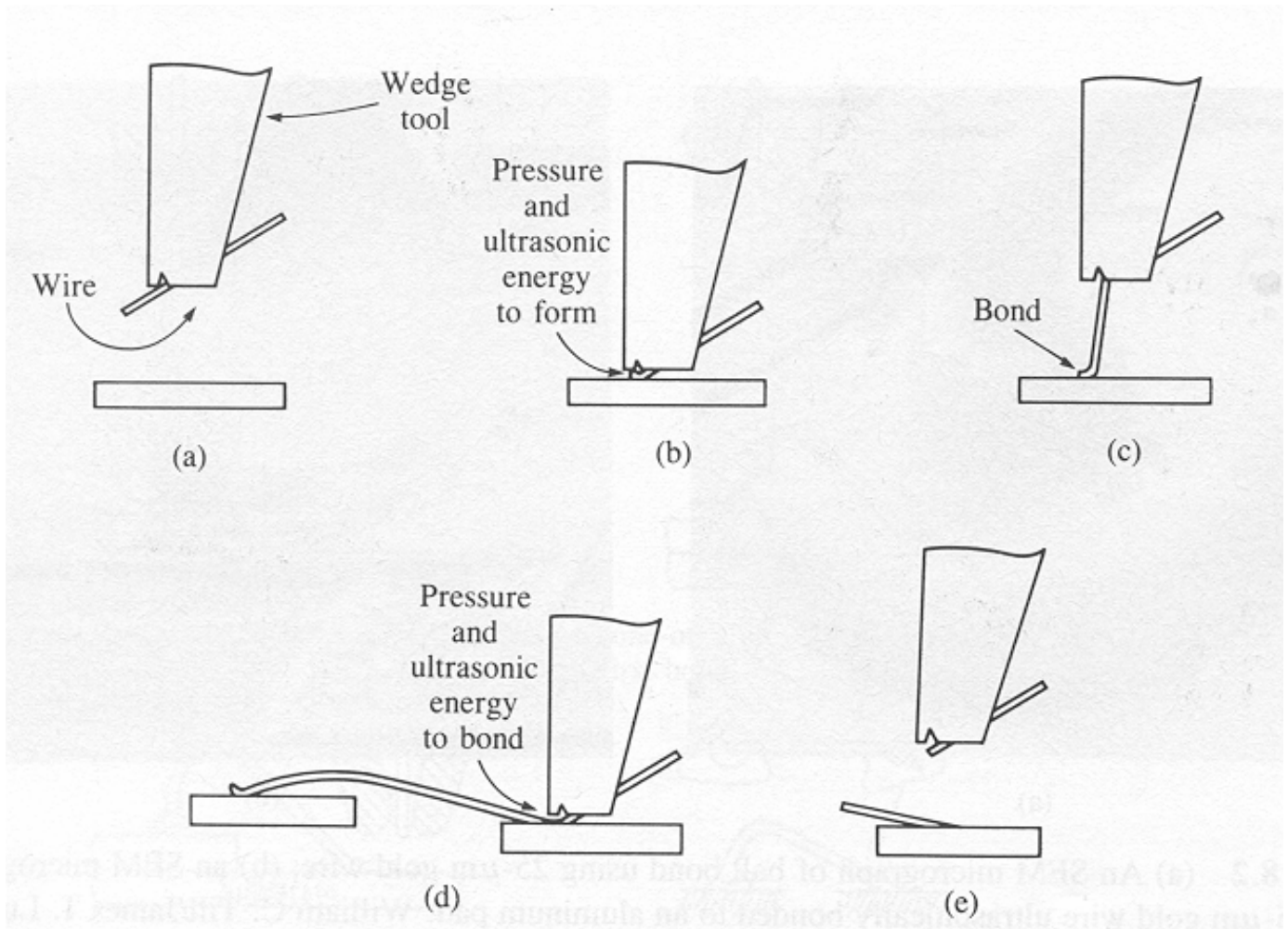
(b)

LCC

THERMOSONIC BONDING



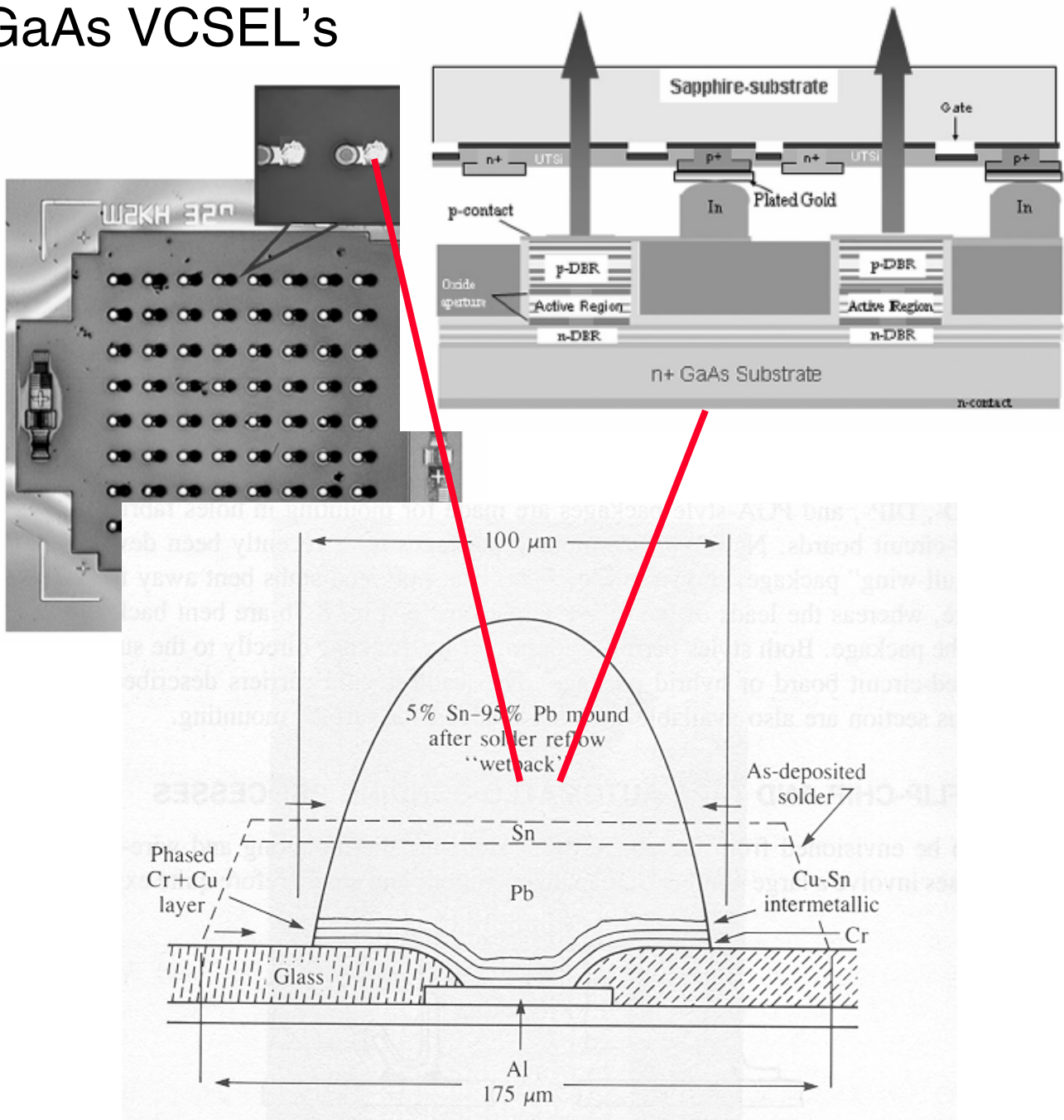
ULTRASONIC BONDING



This is what we have in our lab!

FLIP-CHIP BONDING (I)

GaAs VCSEL's



J.J Liu, Z. Kalayjian, B. Riely, W. Chang, G.J. Simonis, A.B. Apse and A.G. Andreou, *IEEE Journal of Selected Topics in Quantum Electronics*, Vol. 9, No. 2, pp. 380-386, March/April 2003.

Chip On Chip and Chip On Board

